

MOSFET - Power, Dualcool N-Channel, PQFN8 120 V, 6.1 mΩ, 92 A NTMFSC006N12MC

Features

- Advanced Dual-sided Cooled Packaging
- Ulra Low R_{DS(on)}
- MSL1 Robust Packaging Design

Typical Applications

- Primary DC-DC FET
- Synchronous Rectifier
- DC-DC Conversion

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	120	V	
Gate-to-Source Voltage		V _{GS}	±20	V	
Continuous Drain Cur-	Steady State	T _C = 25°C	I _D	92	Α
rent R _{θJC} (Notes 1, 3)	State	T _C = 100°C		57	
Power Dissipation		T _C = 25°C	P _D	104	W
R _{θJC} (Note 1)		T _C = 100°C		41	
Continuous Drain	Steady	T _A = 25°C	I _D	14	Α
Current R _{θJA} (Notes 1, 2, 3)	State	T _A = 100°C		9	
Power Dissipation		T _A = 25°C	P_{D}	2.7	W
R _{θJA} (Notes 1, 2)		T _A = 100°C		1.1	
Pulsed Drain Current	$T_C = 25^{\circ}C, t_p = 10 \mu s$		I _{DM}	1459	Α
Operating Junction / Storage Temperature Max		T _J , T _{stg}	+150	°C	
Source Current (Body Diode)		IS	86	Α	
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 53 A)		E _{AS}	114	mJ	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

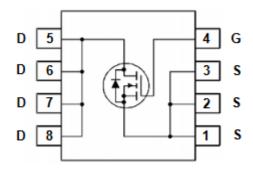
THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{ heta JC}$	1.2	°C/W
Junction-to-Case Top - Steady State	$R_{\theta JT}$	1.53	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	45	

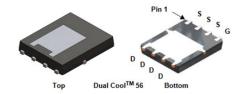
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
120 V	6.1 mΩ @ 10 V	92 A

N-CHANNEL MOSFET

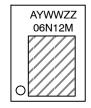


MARKING DIAGRAM



DFN8 5x6.15 CASE 506EG

MARKING DIAGRAM



06N12M = Specific Device Code

A = Assembly Location

Y = Year WW = Work Week ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFSC006N12MC	PQFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condit	tion	Min	Тур	Max	Unit
OFF CHARACTERISTICS					-	<u> </u>	-
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		120			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /	I _D = 250 μA, ref to 25°C			16		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 120 V	$T_{J} = 25^{\circ}C$ $T_{J} = 125^{\circ}C$			5 100	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS}	= 20 V			100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250 \mu A$		2		4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 250 μA, ref	to 25°C		9.8		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 44 A		4.7	6.1	mΩ
Gate-Resistance	R_{G}	T _A = 25°0			1.4		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 60 V			3040		pF
Output Capacitance	C _{OSS}				1460		1
Reverse Transfer Capacitance	C _{RSS}				11.5		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 6 V, V _{DS} = 60 V, I _D = 44 A			24.3		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 60 V, I _D = 44 A			39		
Gate-to-Source Charge	Q_{GS}				13.2		1
Gate-to-Drain Charge	Q_{GD}				6.3		
Plateau Voltage	V_{GP}				4.65		V
SWITCHING CHARACTERISTICS (Note 4)							
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS}	s = 60 V,		15.2		ns
Rise Time	t _r	$I_D = 44 \text{ A, } R_G = 2.5 \Omega$			5.3		
Turn-Off Delay Time	t _{d(OFF)}				25.5		
Fall Time	t _f				5.7		
DRAIN-SOURCE DIODE CHARACTERISTIC	s						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.86		V
		I _S = 44 A	T _J = 125°C		0.74		
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_{S}/dt =$	1000 A/μs,		33.4		ns
Reverse Recovery Charge	Q_{RR}	I _S = 44 A			350.2		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

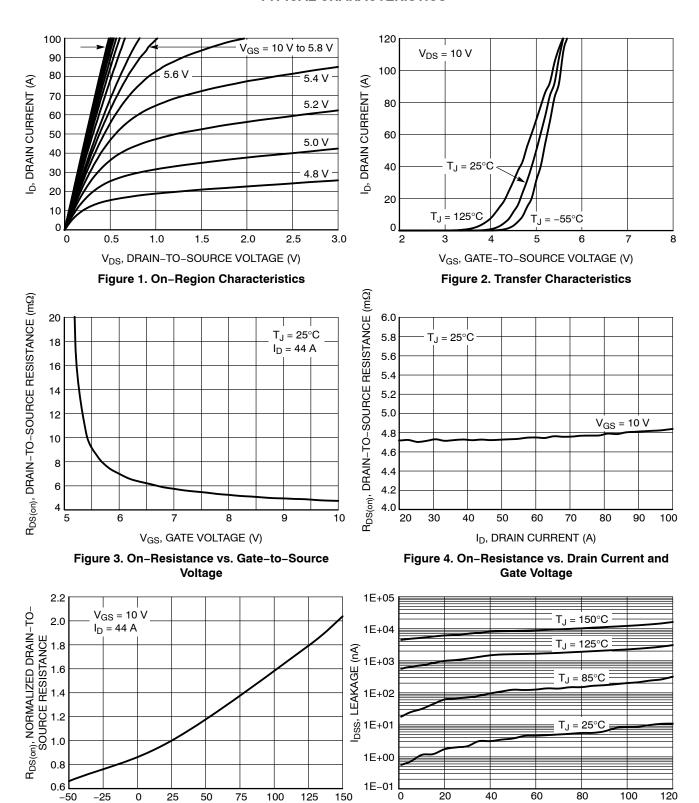


Figure 5. On–Resistance Variation with Temperature

T_J, JUNCTION TEMPERATURE (°C)

Figure 6. Maximum Continuous Drain Current vs. Case Temperature

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

TYPICAL CHARACTERISTICS

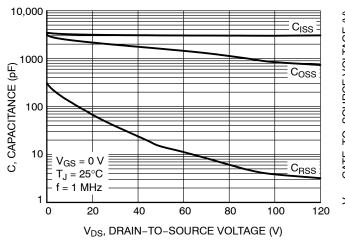


Figure 7. Capacitance Variation

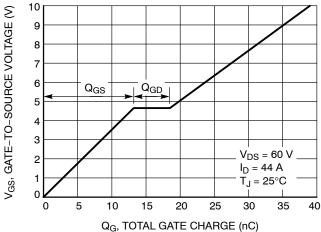


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

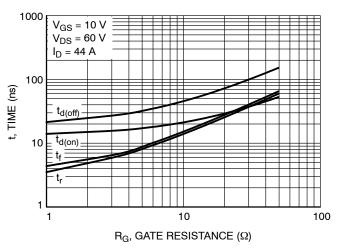


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

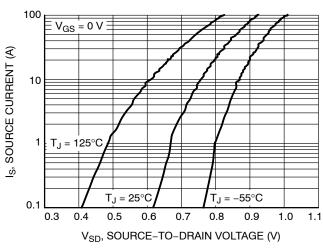


Figure 10. Diode Forward Voltage vs. Current

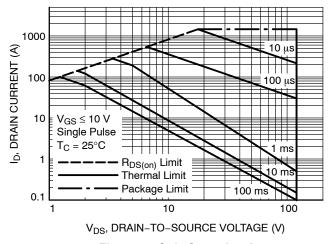


Figure 11. Safe Operating Area

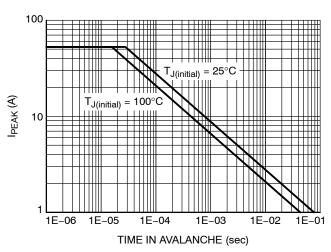


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

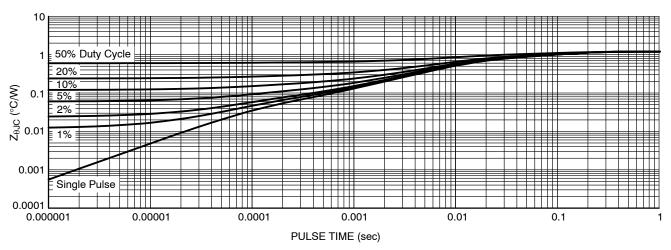


Figure 13. Thermal Characteristics

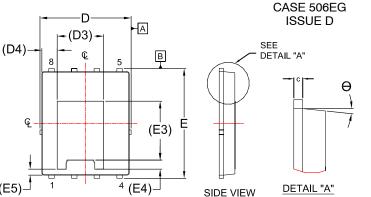
PACKAGE DIMENSIONS

DFN8 5x6.15, 1.27P, DUAL COOL

SCALE: 2:1

A2

DETAIL "B"



// 0.10 C

NOTES:

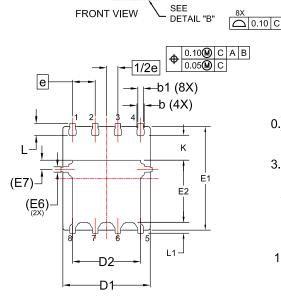
Θ

C

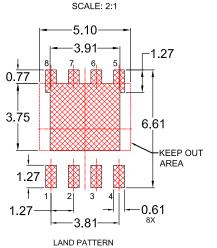
SEATING PLANE

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 5. SEATING PLANE IS DEFINED BY THE TERMINALS.

 "A1" IS DEFINED AS THE DISTANCE FROM THE
 SEATING PLANE TO THE LOWEST POINT ON THE
 PACKAGE BODY.



TOP VIEW



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRMID.

RECOMMENDATION

DIM	MILLIMETERS			
-	MIN.	NOM.	MAX.	
Α	0.85	0.90	0.95	
A1	-	-	0.05	
A2	-	1	0.05	
b	0.31	0.41	0.51	
b1	0.21	0.31	0.41	
С	0.20	0.25	0.30	
D	4.90	5.00	5,10	
D1	4.80	4.90	5.00	
D2	3.67	3.82	3.97	
D3	2.60 REF			
D4	0.86 REF			
Е	6.05	6.15	6.25	
E1	5.70	5.80	5.90	
E2	3.38	3.48	3.58	
E3	;	3.30 REF		
E4	0.50 REF			
E5	0.34 REF			
E6	0.30 REF			
E7	0.52 REF			
е	1.27 BSC			
1/2e	0.635 BSC			
K	1.30	1.40	1.50	
L	0.56	0.66	0.76	
L1	0.52	0.62	0.72	
θ	0°		12°	

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