

MOSFET – Power, Single N-Channel, DUAL COOL®

40 V, 0.78 mΩ, 310 A

NTMFSC0D8N04XM

Features

- Dual Sided Cooling Package
- Latest 40 V Power MOSFET Technology for Motor Drive Applications
- Extreme Lower On-Resistance to Minimize Conduction Losses
- Lower Gate Charge to Minimize Gate Driving and Switching Losses
- Soft Body Diode Reverse Recovery
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Applications

- Motor Drive
- ORing FET
- Battery Protection

MAXIMUM RATINGS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain-to-Source Voltage		40	V
V _{GS}	Gate-to-Source Voltage	DC	±20	V
I _D	Continuous Drain Current (Note 2)	T _C = 25 °C	310	A
		T _C = 100 °C	219	
P _D	Power Dissipation (Note 2)	T _C = 25 °C	135	W
I _{DM}	Pulsed Drain Current	T _C = 25 °C, t _p = 10 μs	1463	A
T _J , T _{stg}	Operating Junction and Storage Temperature Range		–55 to +175	°C
I _S	Continuous Source-Drain Current (Body Diode)		150	A
E _{AS}	Single Pulse Avalanche Energy (I _{PK} = 69 A)		248	mJ
T _L	Lead Temperature Soldering Purposes (1/8" from case for 10 s)		260	°C

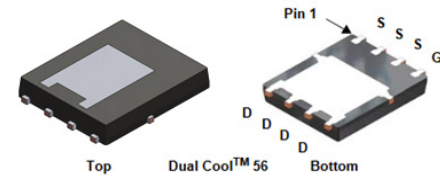
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

THERMAL CHARACTERISTICS

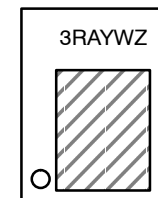
Symbol	Parameter	Max	Unit
R _{θJC}	Junction-to-Case (Bottom) – Steady State (Note 2)	1.1	°C/W
R _{θJC}	Junction-to-Case (Top) – Steady State (Note 2)	1.7	
R _{θJA}	Junction-to-Ambient – Steady State (Notes 1, 2)	39	

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
40 V	0.78 mΩ @ 10 V	310 A



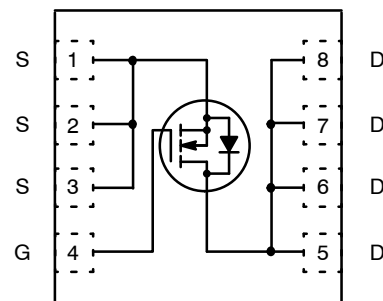
DFN8 5x6
CASE 506EG

MARKING DIAGRAM



3R = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

N-Channel MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NTMFSC0D8N04XM

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA	40			V
ΔV _{(BR)DSS} /ΔT _J	Drain-to-Source Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25 °C		15		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 40 V, T _J = 25 °C			10	μA
		V _{DS} = 40 V, T _J = 125 °C			100	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 3)

R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 50 A		0.63	0.78	mΩ
		V _{GS} = 7 V, I _D = 50 A		0.86	1.25	
V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 180 μA	2.5	3.0	3.5	V
ΔV _{GS(TH)} /ΔT _J	Gate Threshold Voltage Temperature Coefficient	V _{GS} = V _{DS} , I _D = 180 μA		-7		mV/°C
g _{FS}	Forward Trans-conductance	V _{DS} = 5 V, I _D = 50 A		244		S

CHARGES & CAPACITANCES

C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz		4651		pF
C _{OSS}	Output Capacitance			3319		
C _{RSS}	Reverse Transfer Capacitance			69		
Q _{OSS}	Output Charge			100		
Q _{G(TOT)}	Total Gate Charge	V _{GS} = 10 V, V _{DD} = 20 V, I _D = 50 A		72		nC
Q _{G(TH)}	Threshold Gate Charge			14		
Q _{GS}	Gate-to-Source Charge			21		
Q _{GD}	Gate-to-Drain Charge			13		
V _{GP}	Gate Plateau Voltage			4.5		V
R _G	Gate Resistance	f = 1 MHz		0.65	1.2	Ω

SWITCHING CHARACTERISTICS (Note 3)

t _{d(ON)}	Turn-On Delay Time	Resistive Load V _{GS} = 0/10 V, V _{DD} = 20 V, I _D = 50 A, R _G = 2.5 Ω		28		ns
t _r	Rise Time			10		
t _{d(OFF)}	Turn-Off Delay Time			45		
t _f	Fall Time			9.5		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 50 A, T _J = 25 °C		0.81	1.2	V
		V _{GS} = 0 V, I _S = 50 A, T _J = 125 °C		0.66	1.0	
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A, V _{DD} = 50 V		69		ns
t _a	Charge Time			36		
t _b	Discharge Time			33		
Q _{RR}	Reverse Recovery Charge			144		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

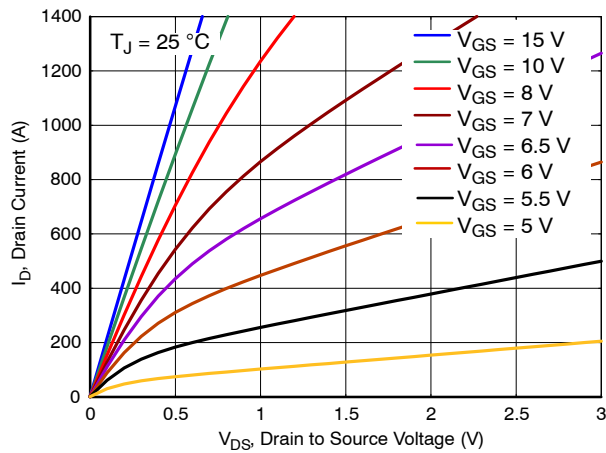


Figure 1. On-Region Characteristics

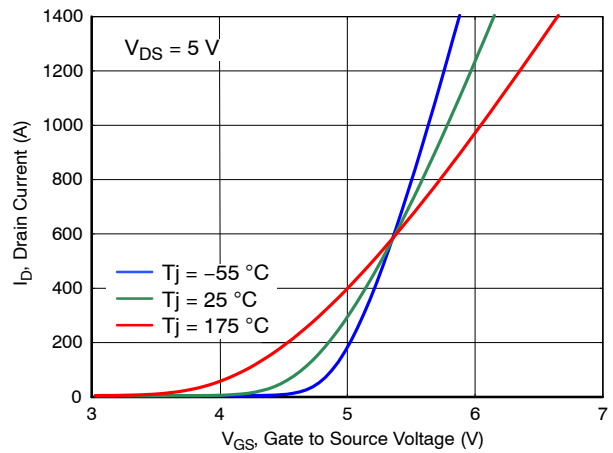


Figure 2. Transfer Characteristics

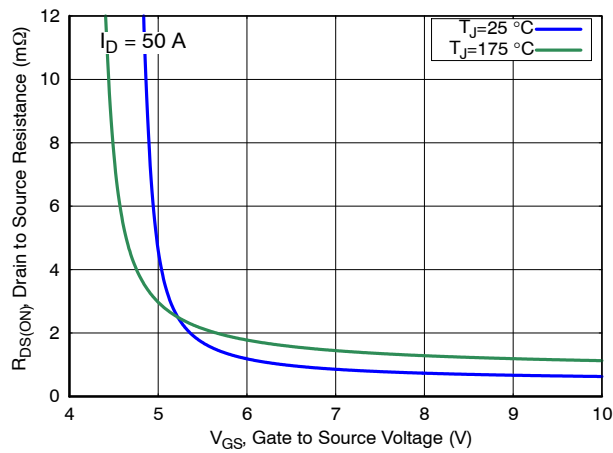


Figure 3. On-Resistance vs. Gate Voltage

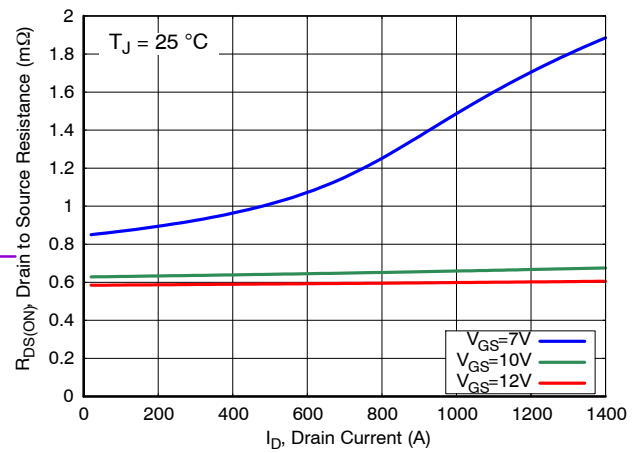


Figure 4. On-Resistance vs. Drain Current

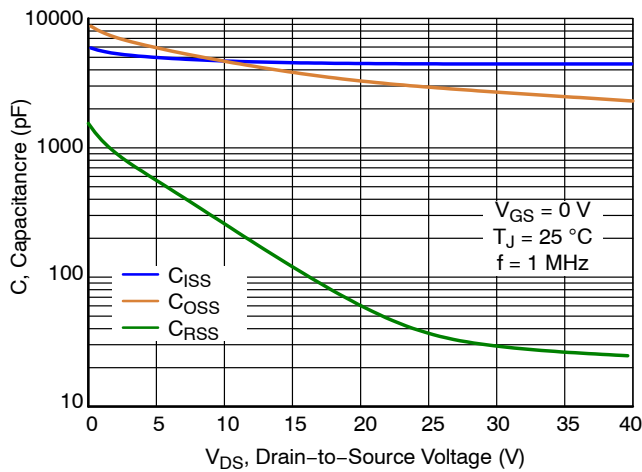


Figure 5. Capacitance Characteristics

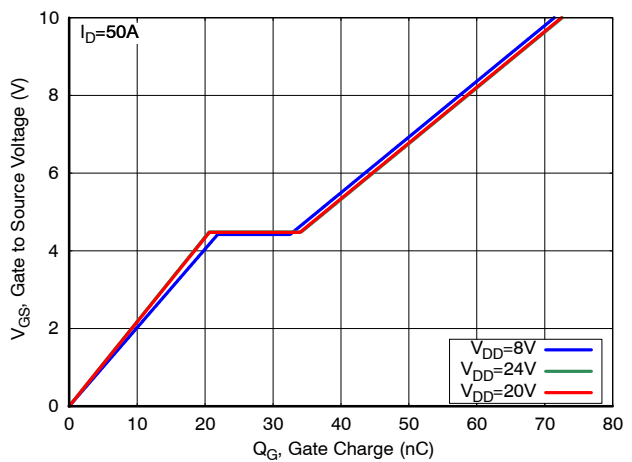


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

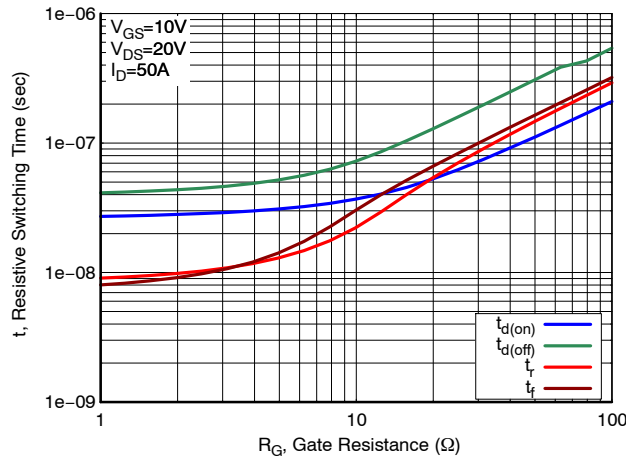


Figure 7. Resistive Switching Time Variation vs. Gate Resistance

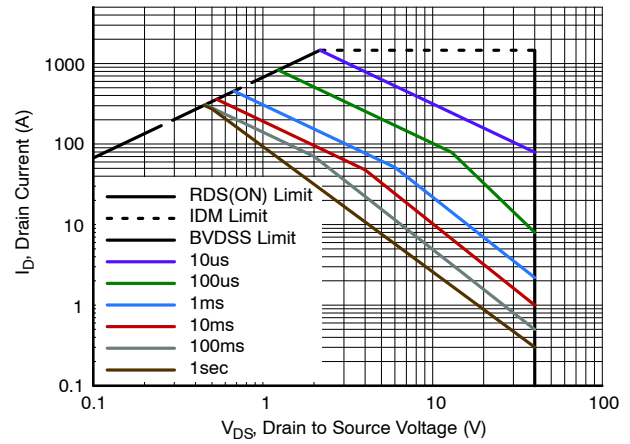


Figure 8. Safe Operating Area (SOA)

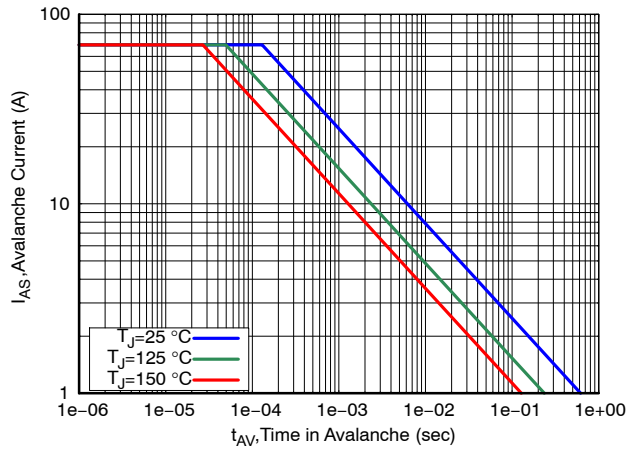


Figure 9. Avalanche Current vs Pulse Time (UIS)

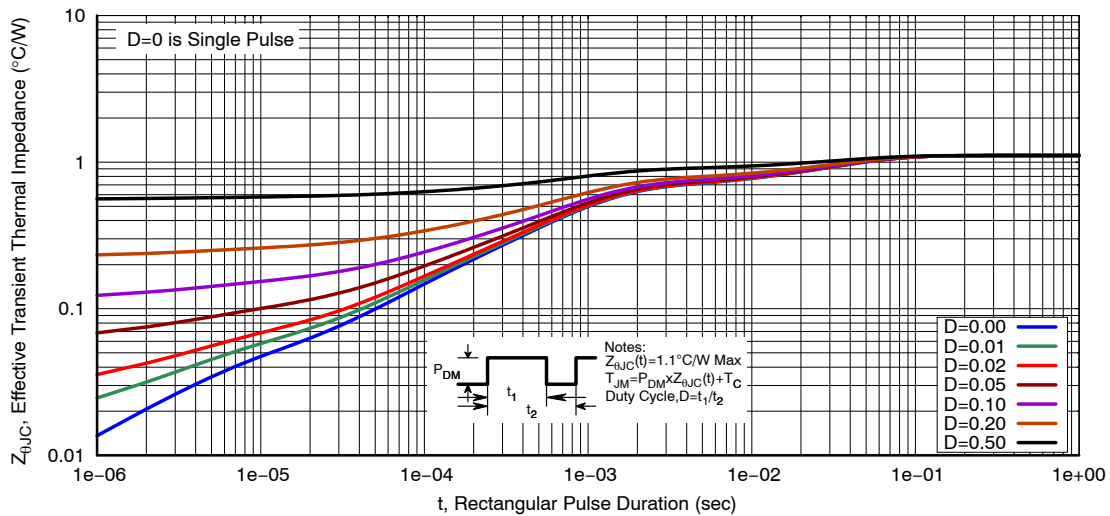


Figure 10. Transient Thermal Response

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ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC0D8N04XMTWG	3R	DFN8 5x6 (Pb-Free/Halogen Free)	3,000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

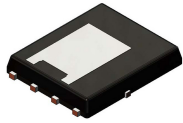
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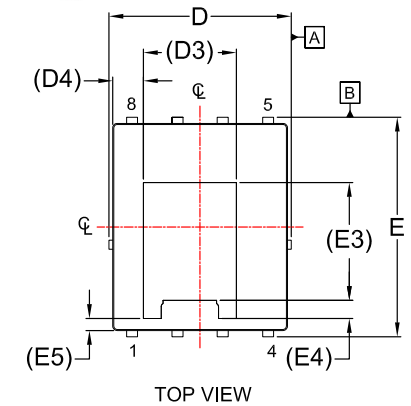
REVISION HISTORY

Revision	Description of Changes	Date
2	Revision to add figure in the existing datasheet.	8/27/2025

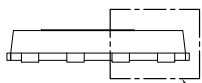
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.


DFN8 5x6.15, 1.27P, DUAL COOL
CASE 506EG
ISSUE D

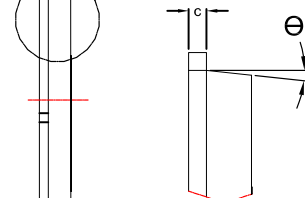
DATE 25 AUG 2020



TOP VIEW



FRONT VIEW

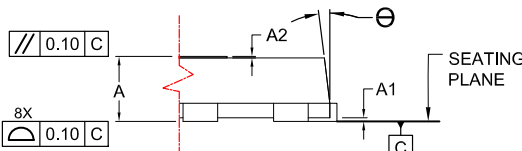
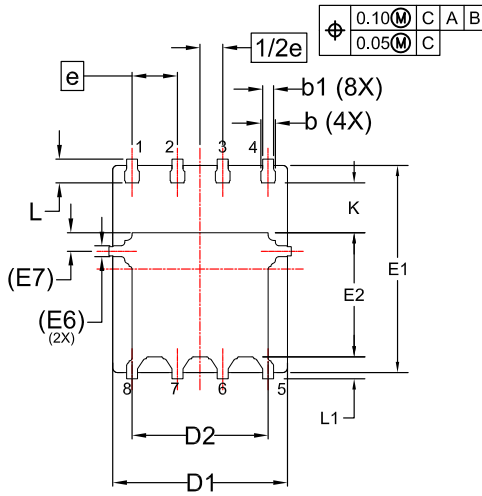
SEE
DETAIL "A"


SIDE VIEW

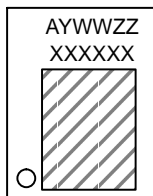
DETAIL "A"
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.


DETAIL "B"
SCALE: 2:1


BOTTOM VIEW

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION: DFN8 5x6.15, 1.27P, DUAL COOL

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