

# MOSFET - Power, Single N-Channel, DUAL COOL®, DFN8 5x6

80 V, 1.4 mΩ, 263 A

Product Preview

# NTMFSCH1D4N08X

#### **Features**

- Advanced Dual-Sided Cooled Packaging with Lowest Junction-to-TOP Thermal Resistance
- Low Q<sub>RR</sub>, Soft Recovery Body Diode
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- MSL1 Robust Packaging Design
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

# **Typical Applications**

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- ORing FET Load Switching

#### MAXIMUM RATINGS (T<sub>.J</sub> = 25°C, Unless otherwise specified)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage		V <sub>DSS</sub>	80	V
Gate-to-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current T <sub>C</sub> =		I <sub>D</sub>	263	Α
(Notes 1, 2)	T <sub>C</sub> = 100°C		186	
Power Dissipation (Notes 1, 2)	T <sub>C</sub> = 25°C	$P_{D}$	208	W
Pulsed Drain Current $ \begin{array}{c} T_A = 25^{\circ}C, \\ t_p = 100 \; \mu s \end{array} $		I <sub>DM</sub>	807	Α
Operating Junction and Storage Temperature		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)		I <sub>S</sub>	358	Α
Single Pulse Avalanche Energy (I <sub>pk</sub> = 84 A) (Note 3)		E <sub>AS</sub>	352	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C

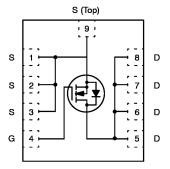
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal & electromechanical application board design.
- 3. EAS of 352 mJ is based on started  $T_J$  = 25C,  $I_{AS}$  = 84 A,  $V_{DD}$  = 64 V,  $V_{GS}$  = 10 V, 100% avalanche tested.

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

V <sub>SSS</sub>	R <sub>SS(ON)</sub> MAX	I <sub>D</sub> MAX
80 V	1.4 mΩ @ 10 V	263 A

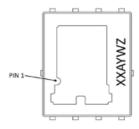
#### **N-CHANNEL MOSFET**





DFN8 5.1x6.15 CASE 506FF

#### **MARKING DIAGRAM**



3V = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

Z = Assembly Lot Code

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

# THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	0.72	°C/W
Thermal Resistance, Junction-to-Top	$R_{ heta JT}$	0.85	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	

#### **ELECTRICAL CHARACTERISTICS** (T<sub>.1</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•			•		•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	80			٧
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV <sub>(BR)DSS</sub> / ΔΤ <sub>J</sub>	I <sub>D</sub> = 1 mA. Referenced to 25°C		33		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 25°C			1.0	μΑ
		V <sub>DS</sub> = 80 V, T <sub>J</sub> = 125°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 69 \text{ A}, T_J = 25^{\circ}\text{C}$		1.1	1.4	$m\Omega$
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 34 A, T <sub>J</sub> = 25°C		1.6	2.6	
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 340 \mu A,$ $T_J = 25^{\circ} C$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	ΔV <sub>GS(TH)</sub> / ΔΤ <sub>J</sub>	$V_{GS} = V_{DS}$ , $I_D = 340 \mu A$		-7		mV/°C
Forward Transconductance	9FS	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 69 A		220		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE			•		•
Input Capacitance	C <sub>ISS</sub>			6310		pF
Output Capacitance	C <sub>OSS</sub>	<b>1</b>		1830		1
Reverse Transfer Capacitance	C <sub>RSS</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}, f = 1 \text{ MHz}$		28		
Output Charge	Q <sub>OSS</sub>			130		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 6 V, V <sub>DD</sub> = 40 V; I <sub>D</sub> = 69 A		55		
		$V_{GS} = 10 \text{ V}, V_{DD} = 40 \text{ V};$		89		
Threshold Gate Charge	Q <sub>G(TH)</sub>	I <sub>D</sub> = 69 A		19		1
Gate-to-Source Charge	$Q_{GS}$			30		
Gate-to-Drain Charge	$Q_{GD}$			14		
Gate Plateau Voltage	$V_{GP}$			4.7		V
Gate Resistance	$R_{G}$	f = 1 MHz		0.50		Ω
SOURCE-TO-DRAIN DIODE CHARACTE	ERISTICS					
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_S = 69 \text{ A}, T_J = 25^{\circ}\text{C}$		0.82	1.2	٧
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 69 A, T <sub>J</sub> = 125°C		0.66		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V}, \text{ dI/dt} = 1000 \text{ A/}\mu\text{s},$		29		ns
Charge Time	ta	$I_S = 69 \text{ A}, V_{DD} = 40 \text{ V}$		16		1
Discharge Time	t <sub>b</sub>	1		13		1
Reverse Recovery Charge	Q <sub>RR</sub>	1		253		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### **TYPICAL CHARACTERISTICS**

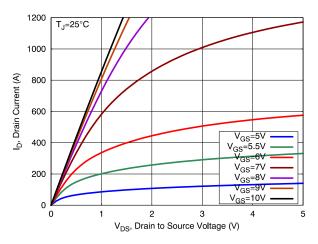


Figure 1. On-Region Characteristics

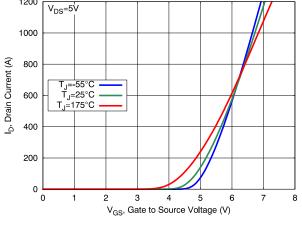


Figure 2. Transfer Characteristics

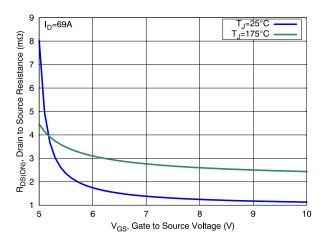


Figure 3. On-Resistance vs. Gate Voltage

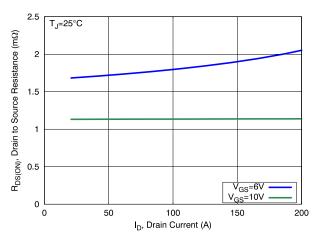


Figure 4. On-Resistance vs. Drain Current

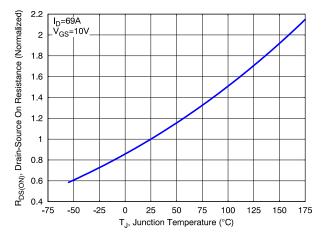


Figure 5. Normalized ON Resistance vs. Junction Temperature

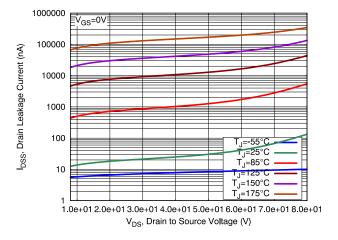


Figure 6. Drain Leakage Current vs Drain Voltage

#### **TYPICAL CHARACTERISTICS**

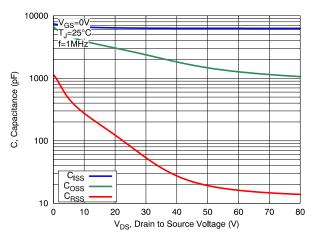


Figure 7. Capacitance Characteristics

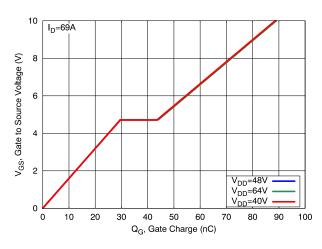


Figure 8. Gate Charge Characteristics

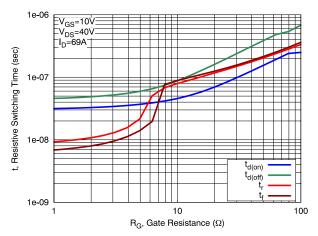


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

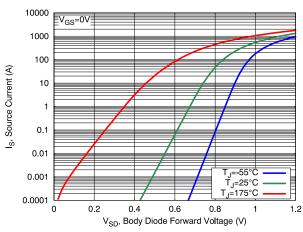


Figure 10. Diode Forward Characteristics

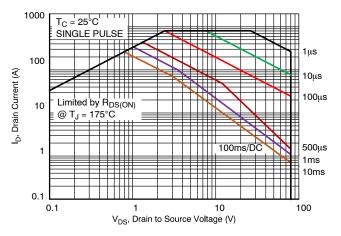


Figure 11. Safe Operating Area (SOA)

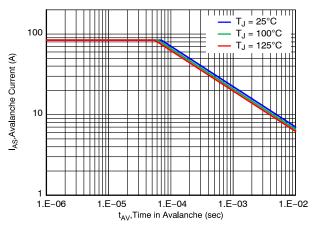
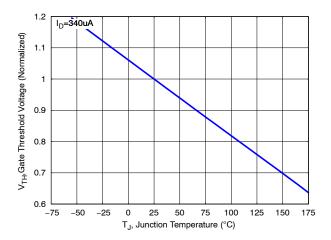


Figure 12. Avalanche Current vs Pulse Time (UIS)

#### **TYPICAL CHARACTERISTICS**



300 250 250 250 250 150 50 0 25 50 75 100 125 150 175 T<sub>C</sub>, Case Temperature (°C)

Figure 13. Gate Threshold Voltage vs Junction Temperature

Figure 14. Maximum Current vs. Case Temperature

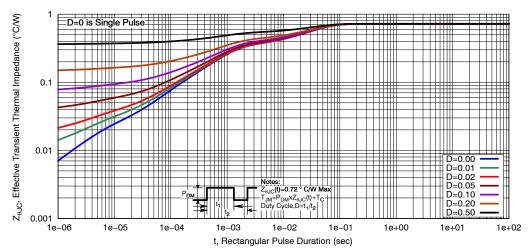


Figure 15. Transient Thermal Response

#### **ORDERING INFORMATION**

Device	Device Marking	Package	Shipping <sup>†</sup>
NTMFSCH1D4N08XTWG	3V	DFN8 5.1x6.15 (Pb–Free/Halogen Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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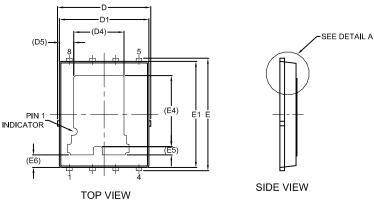
# PACKAGE DIMENSIONS

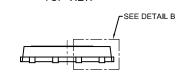
# DFN8 5.1x6.15, 1.27P CASE 506FF **ISSUE O**

**DATE 23 JUN 2023** 

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

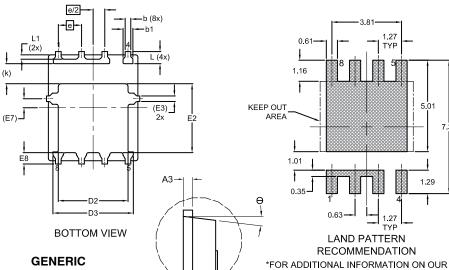




FRONT VIEW

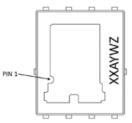
// 0.10 C 0.08 C C SEATING PLANE **DETAIL B** 

SCALE: 2:1



DIM	IM MILLIMETERS		
DIIVI	MIN.	NOM.	MAX.
Α	0.80	0.90	1.00
A1	-	-	0.05
А3	0.20	0.25	0.30
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.10	5.30
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4	2.75 REF		
D5	0.79 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.67	3.77	3.87
E3	0.30 REF		
E4	3.89 REF		
E5	0.45 REF		
E6	0.69 REF		
E7	0.50 REF		
E8	0.52	0.62	0.72
е	1.27 BSC		
e/2	0.635BSC		
k	1.10 REF		
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
θ	0°		7°

**GENERIC MARKING DIAGRAM\*** 



- = Specific Device Code XXΑ
  - = Assembly Location

**DETAIL A** 

SCALE: 2:1

- Υ = Year
- W = Work Week
- Ζ = Assembly Lot Code
- \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

PB-FREE STRATEGY AND SOLDERING DETAILS,

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SOLDERING AND MOUNTING TECHNIQUES

REFERENCE MANUAL, SOLDERRM/D.

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