

MOSFET - Power, Single N-Channel

100 V, 1.7 mΩ, 267 A

NTMTSC1D6N10MC

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- New Power 88 Dual Cool Package
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	100	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 100^\circ\text{C}$	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 100^\circ\text{C}$	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 100^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to $+175$	$^\circ\text{C}$
Source Current (Body Diode)	I_S	243	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 22.3 \text{ A}$)	E_{AS}	1550	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

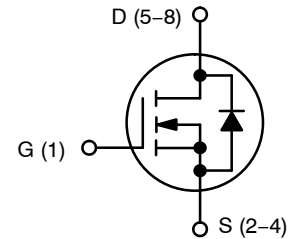
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

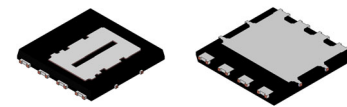
Parameter	Symbol	Value	Unit
Junction-to-Case - Bottom - Steady State	$R_{\theta JCB}$	0.5	$^\circ\text{C}/\text{W}$
Junction-to-Case - Top - Steady State	$R_{\theta JCT}$	0.8	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	1.7 mΩ @ 10 V	267 A

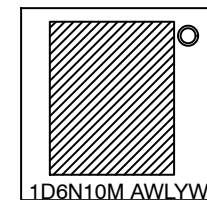


N-CHANNEL MOSFET



TDFNW8
CASE 507AS

MARKING DIAGRAM



1D6N10M = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMTSC1D6N10MC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			64.5		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V			5	μA
					10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 650 μA	2.0		4.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-10		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 90 A		1.42	1.7	mΩ
		V _{GS} = 6 V, I _D = 58 A			4.3	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 100 A		233		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 100 KHz, V _{DS} = 50 V		7630		pF
Output Capacitance	C _{OSS}			4260		
Reverse Transfer Capacitance	C _{RSS}			80		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 116 A		106		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 116 A		20		
Gate-to-Source Charge	Q _{GS}			35		
Gate-to-Drain Charge	Q _{GD}			22		
Plateau Voltage	V _{GP}			5		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 50 V, I _D = 116 A, R _G = 6 Ω		34		ns
Rise Time	t _r			24		
Turn-Off Delay Time	t _{d(OFF)}			69		
Fall Time	t _f			29		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 90 A	T _J = 25°C		0.83	1.2	V
			T _J = 125°C		0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 58 A			82		ns
Charge Time	t _a				55		
Discharge Time	t _b				27		
Reverse Recovery Charge	Q _{RR}				147		nC
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 1000 A/μs, I _S = 58 A			43		ns
Charge Time	t _a				23		
Discharge Time	t _b				19		
Reverse Recovery Charge	Q _{RR}				385		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

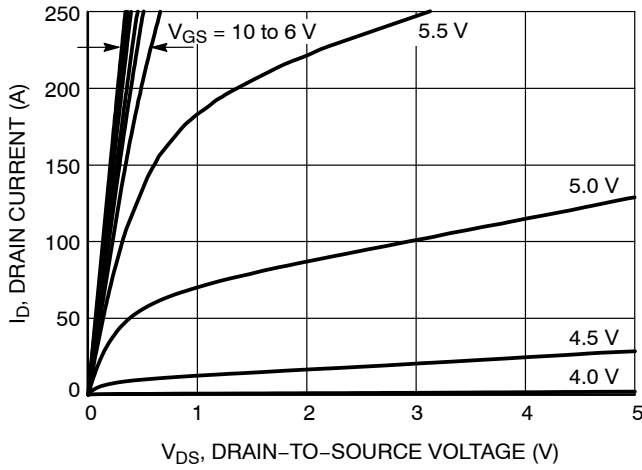


Figure 1. On-Region Characteristics

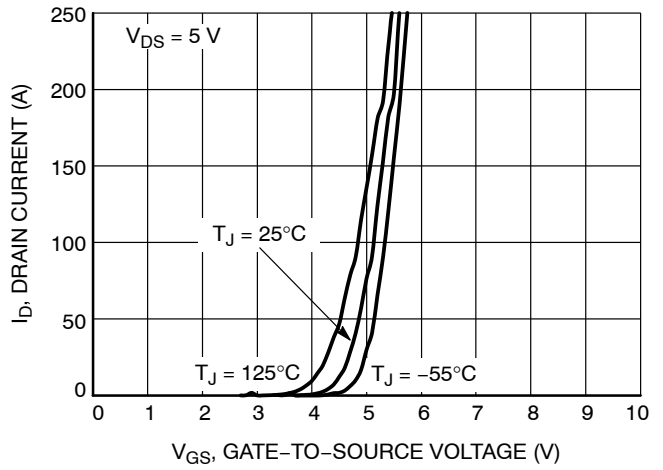


Figure 2. Transfer Characteristics

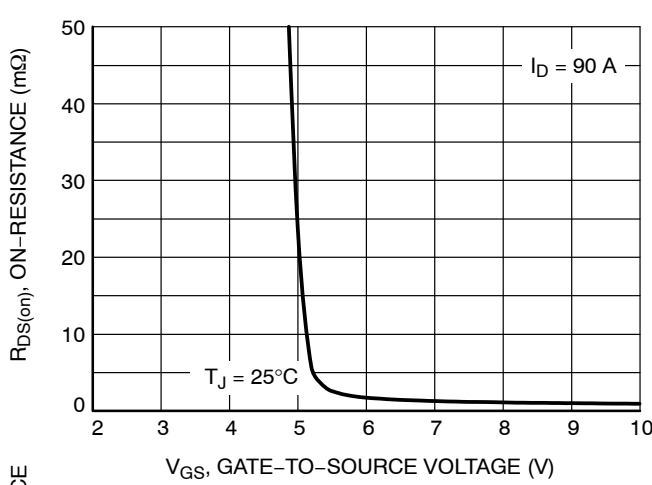


Figure 3. On-Resistance vs. Gate-to-Source Voltage

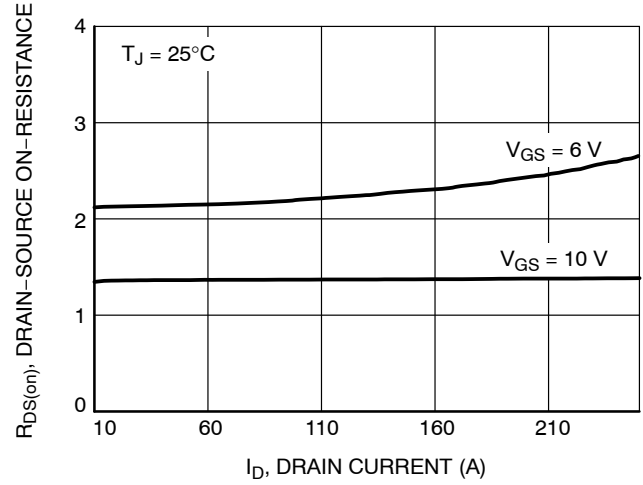


Figure 4. On-Resistance vs. Drain Current

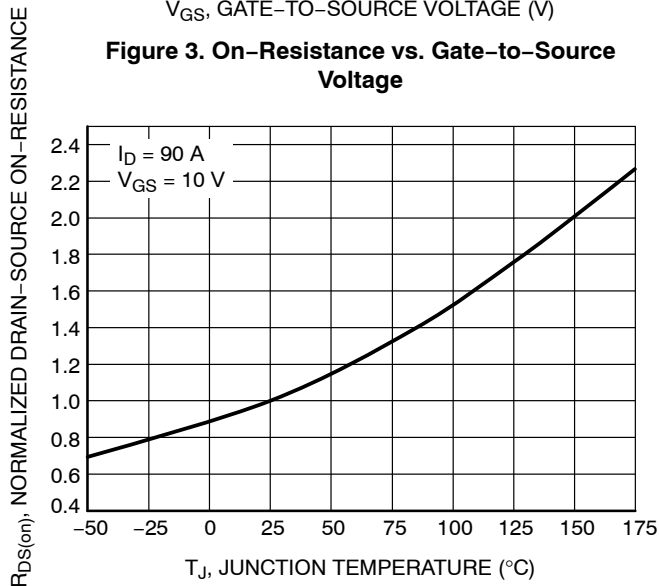


Figure 5. On-Resistance Variation with Temperature

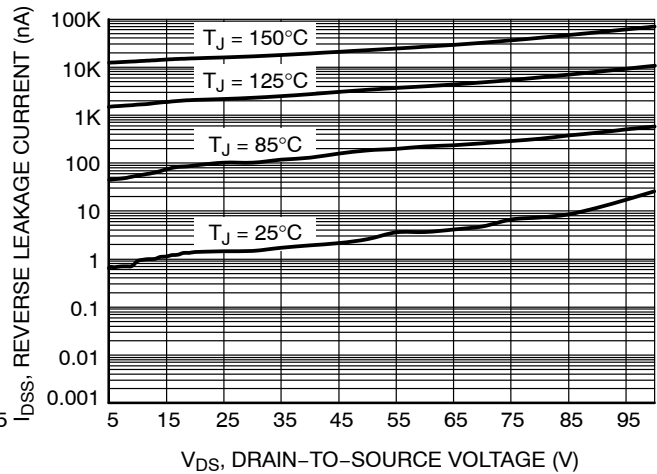


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTMTSC1D6N10MC

TYPICAL CHARACTERISTICS

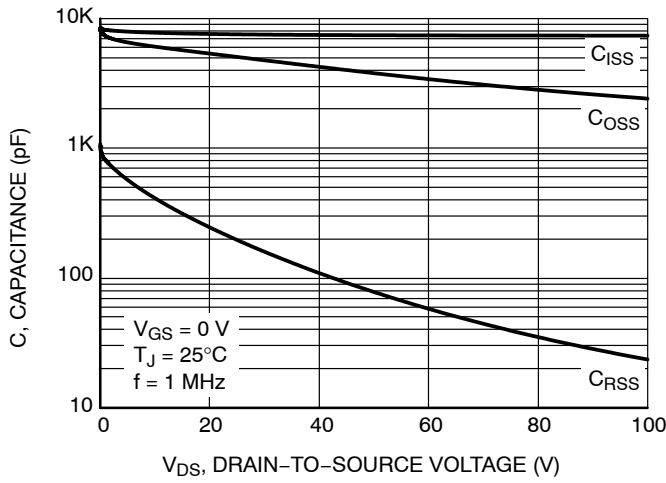


Figure 7. Capacitance Variation

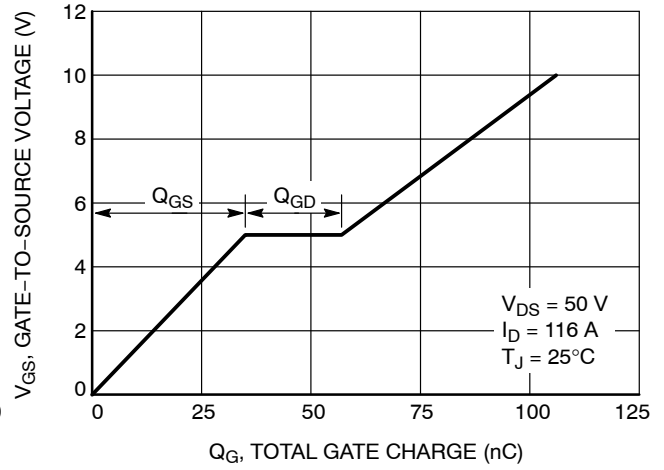


Figure 8. Gate-to-Source Voltage vs. Total Charge

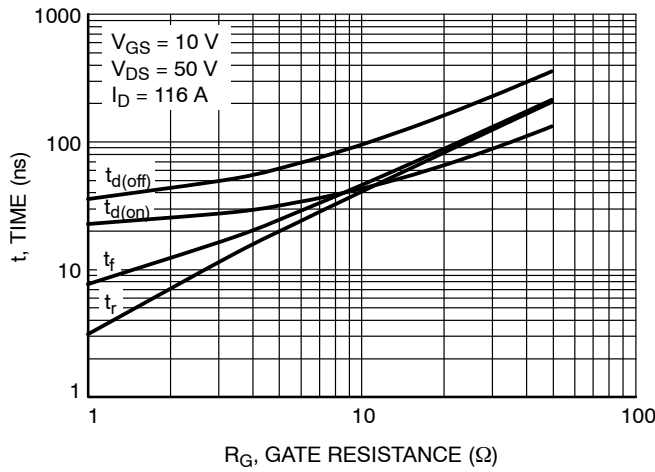


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

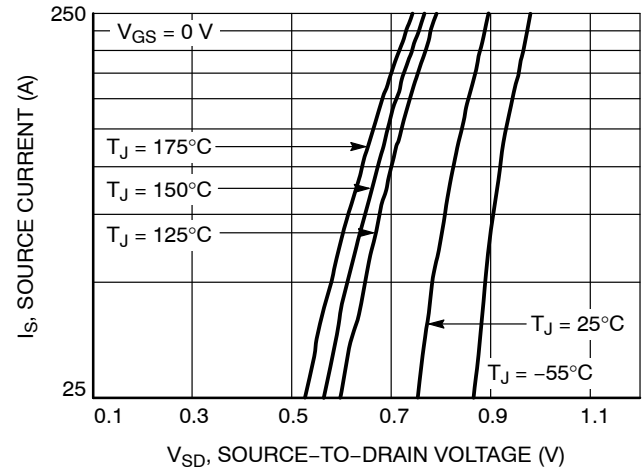


Figure 10. Diode Forward Voltage vs. Current

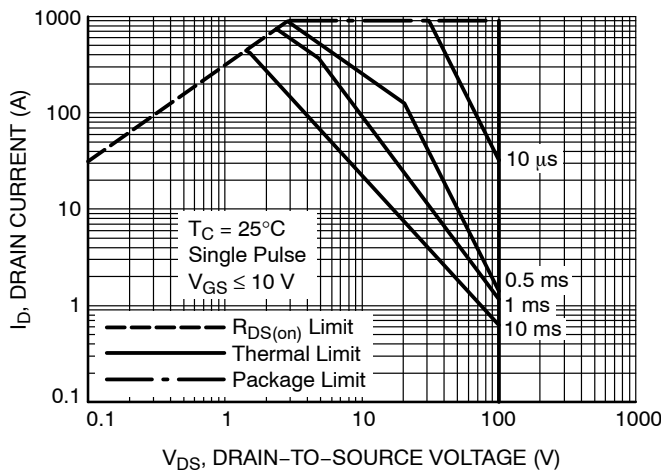


Figure 11. Safe Operating Area

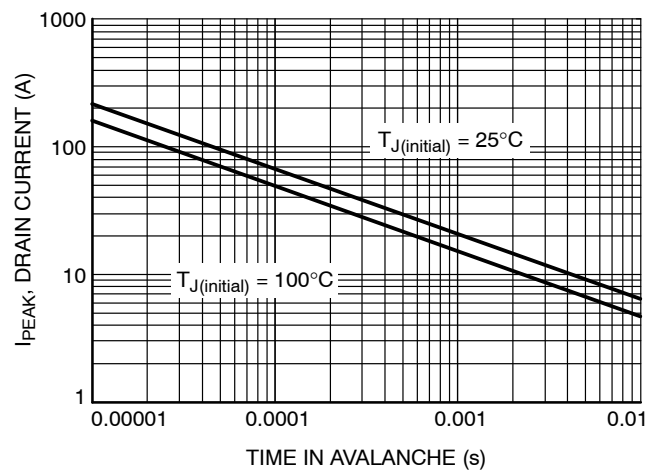


Figure 12. Maximum Drain Current vs. Time in Avalanche

NTMTSC1D6N10MC

TYPICAL CHARACTERISTICS

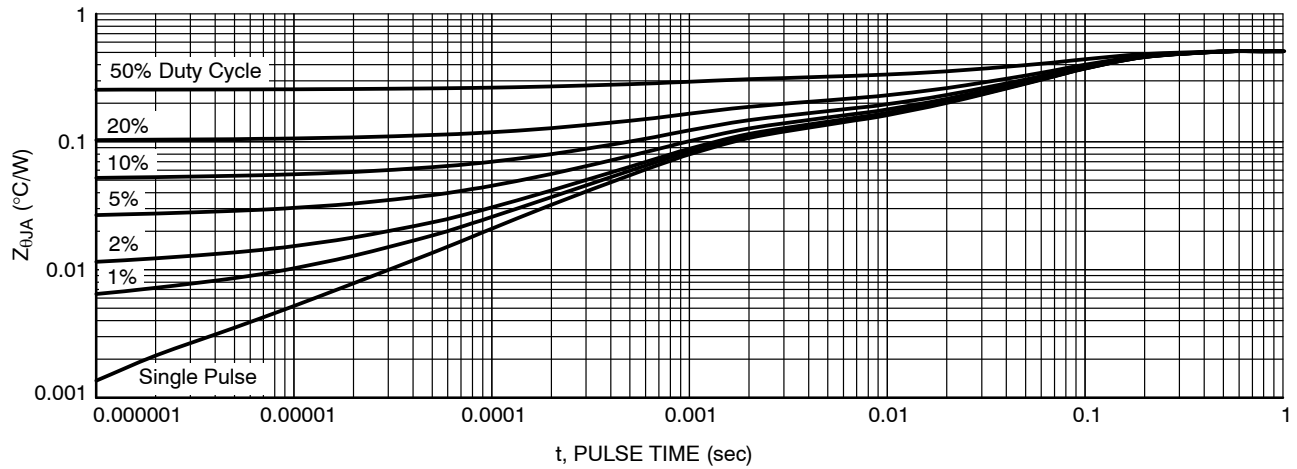
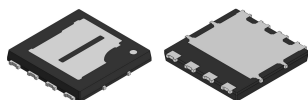


Figure 13. Junction-to-Ambient Transient Thermal Response

DEVICE ORDERING INFORMATION

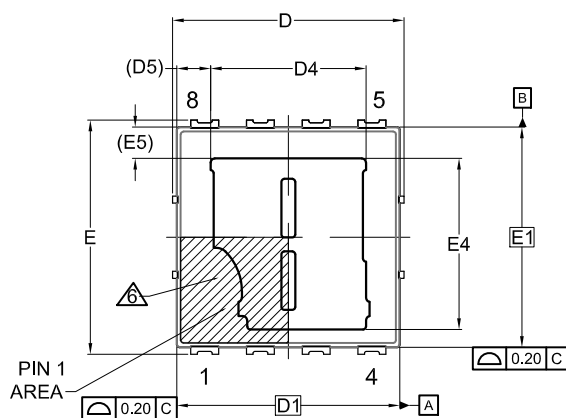
Device	Marking	Package	Shipping [†]
NTMTSC1D6N10MCTXG	1D6N10M	TDFNW8 (Pb-Free)	3,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TDFNW8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE C

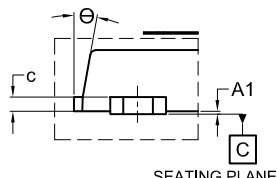
DATE 28 MAY 2024



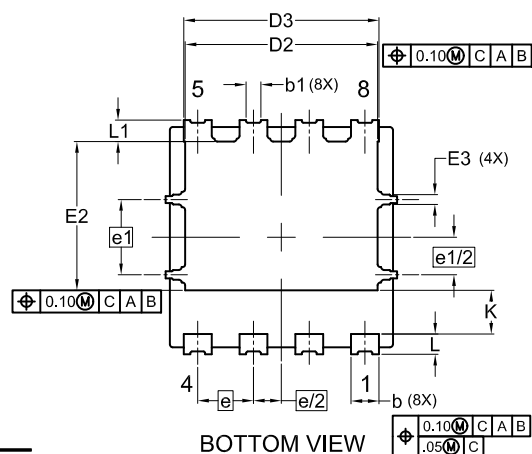
TOP VIEW



SEE DETAIL A FRONT VIEW



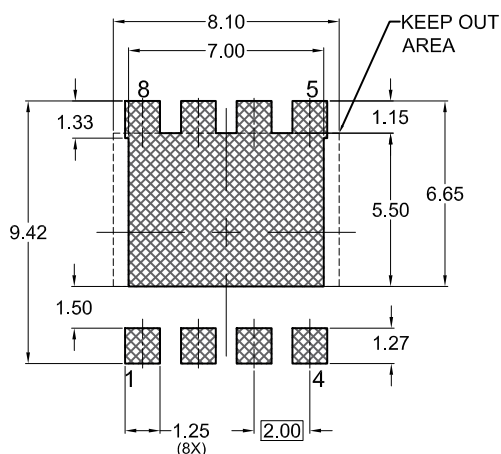
DETAIL A
(SCALE: 2X)



BOTTOM VIEW

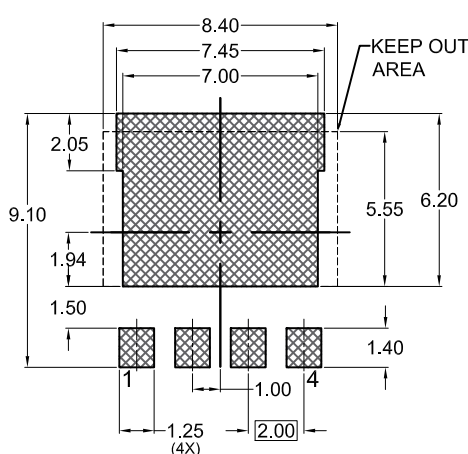
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS.
 "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. SLOT PARTITION IS OPTIONAL.



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL. SOLDERRM/D.



UNIVERSAL LAND PATTERN*

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	8.00 BSC		
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	5.52	5.67	5.82
D5	1.16 REF		
E	8.30	8.40	8.50
E1	7.90 BSC		
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	6.08	6.23	6.38
E5	1.13 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Ø	0°	—	12°

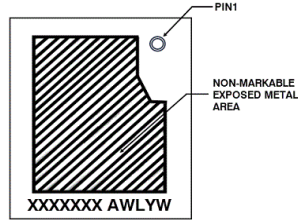
DOCUMENT NUMBER:	98AON95716G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TDFNW8 8.30x8.40x0.92, 2.00P	PAGE 1 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

TDFNW8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE C

DATE 28 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON95716G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TDFNW8 8.30x8.40x0.92, 2.00P	PAGE 2 OF 2

onsemi and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales