NTP8824

High Performance, High Fidelity Power Driver Integrated Full Digital Audio Amplifier

Datasheet
ver. 1.1

NEOFIDELITY, INC.

Document Number: DS8824 ver. 1.1
2018-07-18

General Description

The NTP8824 is a single chip full digital audio amplifier including power stage for stereo amplifier system. NTP8824 is integrated with versatile digital audio signal processing functions, high-performance, high-fidelity fully digital PWM modulator and two high-power full-bridge MOSFET power stages.

The NTP8824 receives digital serial audio data with sampling frequencies of 32kHz, 44.1kHz, 48kHz, and 96kHz. It delivers 2 x 20 watts in stereo mode.

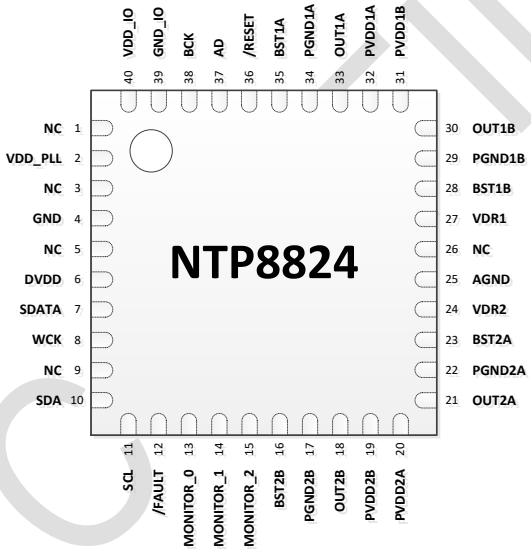
The NTP8824 has a mixer and Bi-Quad filters which can be used to implement the essential audio signal processing functions like loudness control, compensation of a loud speaker response and parametric equalization.

All the functions of the NTP8824 can be controlled by internal register values via I^2C host interface bus.

Features

- 2 CH Stereo (20W x 2 BTL)
- Wide Operating Supply Voltage Range (7V to 28V)
- SDATA Generator (I^2S output)
- Floating Point Operation
- 24 Programmable Bi-Quad Filters
  - ✓ Speaker Compensation
  - ✓ LPF, HPF, DC Cut
  - ✓ Advanced Parametric Equalizer
- 3 Band Dynamic Range Control
- Loudness Control
- 3D Surround
- Protection Circuit
  - ✓ OCP(Over Current Protection)
  - ✓ OTP(Over Temperature Protection)
  - ✓ UVP(Under Voltage Protection)
  - ✓ BQ/DRC Check Sum
- Vol/Soft Mute/Power Meter/NS Feedback
- Smart PWM Switch on/off
- High Efficiency
- DC protection
  - ✓ DC cut filter
  - ✓ Coefficient memory checksum
  - ✓ Modulation Index check

Package



(40 pin SAW QFN 6mm x 6mm Package)

Applications

- PDP TV or LCD TV or Monitor TV
- Docking Station
- Mini-Component Audio Solution

Ordering Information

Product ID	Package Type	Pin	Size
NTP8824	SAW QFN	40	6 x 6mm

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1. BLOCK DIAGRAM

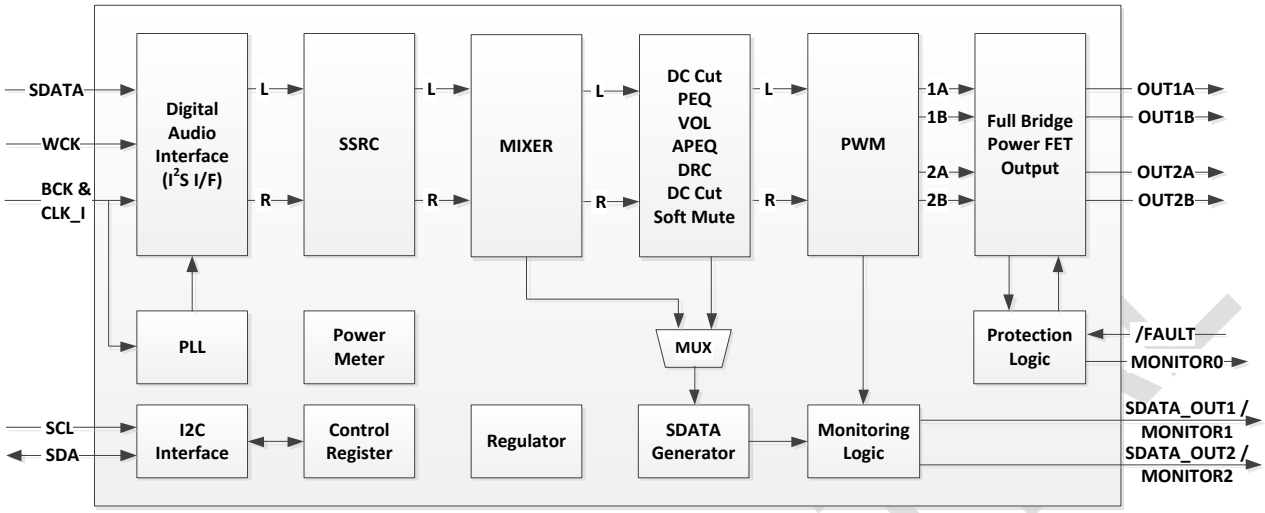


Figure 1. NTP8824 Block Diagram

2. PIN ASSIGNMENTS

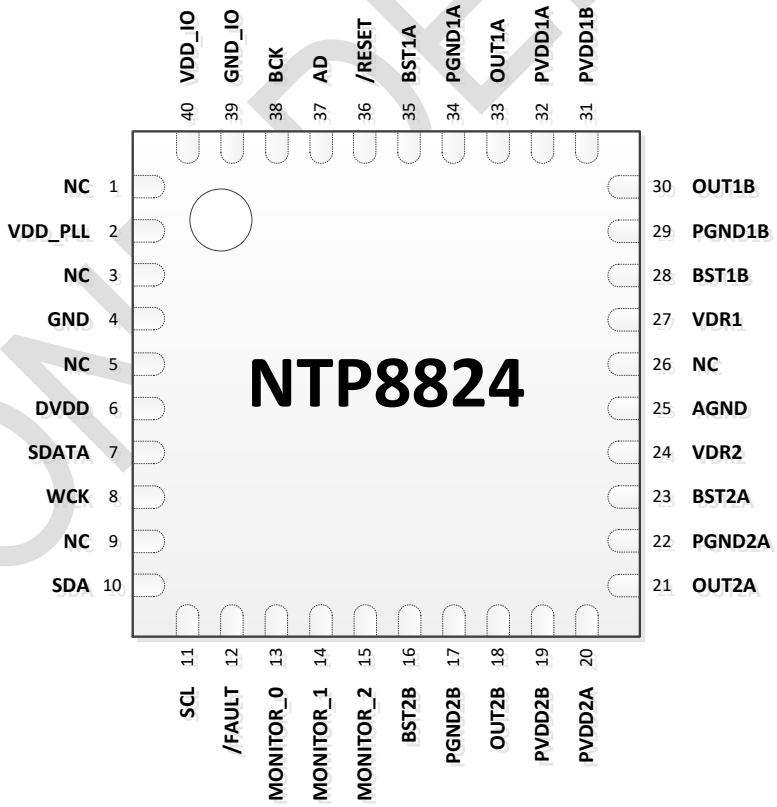


Figure 2. NTP8824 Pin Assignments

3. PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	NC	-	Not connected
2	VDD_PLL	P	Regulator output for PLL digital block, 1.2V
3	NC	-	Not connected
4	GND	P	This pin should be connected to Ground
5	NC	-	Not connected
6	DVDD	P	Regulator output for Core block, 1.2V
7	SDATA	I	I^2S serial data input
8	WCK	I	I^2S word clock
9	NC	-	Not connected
10	SDA	I/O	I^2C data
11	SCL	I	I^2C clock
12	/FAULT	I	Active low to reset internal power stage, Pull-up
13	MONITOR_0	O	No Connection, monitoring signal out from protection logic
14	MONITOR_1	O	monitoring signal out from processor block / I^2S output (SDATA word)
15	MONITOR_2	O	monitoring signal out from processor block / I^2S output (SDATA word)
16	BST2B	P	Bootstrap supply, external capacitor to OUT2B is required
17	PGND2B	P	Ground
18	OUT2B	O	Power stage PWM output 2B
19	PVDD2B	P	Power supply for PWM Power stage 2B
20	PVDD2A	P	Power supply for PWM Power stage 2A
21	OUT2A	O	Power stage PWM output 2A
22	PGND2A	P	Ground
23	BST2A	P	Bootstrap supply, external capacitor to OUT2A is required
24	VDR2	P	Gate drive voltage regulator decoupling pin, capacitor to GND is required
25	AGND	P	Ground
26	NC	-	Not connected
27	VDR1	P	Gate drive voltage regulator decoupling pin, capacitor to GND is required
28	BST1B	P	Bootstrap supply, external capacitor to OUT1B is required
29	PGND1B	P	Ground
30	OUT1B	O	Power stage PWM output 1B
31	PVDD1B	P	Power supply for PWM Power stage 1B
32	PVDD1A	P	Power supply for PWM Power stage 1A
33	OUT1A	O	Power stage PWM output 1A
34	PGND1A	P	Ground
35	BST1A	P	Bootstrap supply, external capacitor to OUT1A is required
36	/RESET	I	Active low to reset NTP8824, Schmitt trigger input
37	AD	I	I^2C device address selection
38	BCK	I	System master clock, Schmitt trigger input
39	GND_IO	P	Ground for digital interface I/O
40	VDD_IO	P	Power supply for digital interface I/O, 3.3V
-	Thermal Pad	P	This pad should be connected to Ground

P = Power or Ground, I = Input, O = Output, I/O = Input / Output

Table 1. NTP8824 Pin Description

4. CHARACTERISTICS AND SPECIFICATIONS

4.1. Absolute Maximum Ratings

Parameter	Reference	Rating	Unit
DVDD voltage	DGND	-0.3 ~ 1.5	V
VDD_IO voltage	GND_IO	-0.3 ~ 5.25	V
Logic input voltage	GND	-0.3 ~ 5.25	V
Logic output voltage	GND	-0.3 ~ 5.25	V
PVDDXX voltage	PGNDXX	30	V
OUTXX voltage	PGNDXX	-0.3 ~ PVDDXX	V
BSTXX voltage	PGNDXX	36	V
VDRX voltage	PGNDXX	-0.3 ~ 6.0	V
Junction temperature	Tj	150	°C
ESD	HBM	±2,000	V
	CDM	±500	V

4.2. Recommended Operating Conditions

Parameter	Reference	Rating			Unit
VDD_IO voltage	GND_IO	3.0 ~ 3.6			V
PVDDXX voltage	PGNDXX	7 ~ 28			V
VDRX voltage	PGNDXX		5.1		V
Ambient operating temperature	Tamb	0 ~ 85			°C
Load impedance (BTL)	Output Filter L :10uH, C : 470nF	6	8		Ω
Load impedance (PBTL)	Output Filter L :10uH, C : 470nF		4		Ω

4.3. DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Logic Block (VDD_IO=3.3V, T_A=+25°C, unless otherwise specified.)						
Input High voltage	V_{IH}	-	2.08			V
Input Low voltage	V_{IL}	-	-0.3		0.89	V
Schmitt trig. Hysteresis	ΔV	-		0.29		V
Input current	I_I	V_{IN}=V_{IL} MAX, DVDD=MIN	-50			uA
		V_{IN}=V_{IH} MIN, DVDD=MIN			50	uA
Input leakage current	I_L	V_{IN}=VSS, DVDD=MIN	-10		10	uA
Output Low voltage	V_{OL}	I_{OL} = -4mA	0		0.4	V
Output High voltage	V_{OH}	I_{OH} = 4mA	2.4		3.6	V
LDO output voltage	V_{LDO}	DVDD	1.08		1.32	V
Driver Block (PVDDXX=24V, T_A=+25°C, unless otherwise specified.)						
Current consumption		VDD_IO=3.3V, No Input, No Load		30		mA
		PVDD=24V, No Input, 8 Ω Load with 10uH inductor		95		
Peak current limit	OCP	-	5.0	6.5	9.0	A
Thermal shutdown temperature	OTP		140	150	160	°C
Under voltage lockout	UVP		4.75	5.0		V

4.4. Performance Specification

Speaker Amplifier					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
SNR	AES17, A-weighting filter		96		dB
THD+N	PS ≤ 0x7C, 20Hz~20kHz		0.3		%
Cross talk	Dolby standard		70		dB

4.5. Switching Characteristics – I²C Control

Parameter	Symbol	Condition	Min		Max	Unit
I²C Control Port						
SCL clock frequency	F_{scl}		-		400	kHz
Hold time for START condition	T_{hdsta}		600		-	ns
Low period of the SCL clock	T_{low}		1300		-	ns
High period of the SCL clock	T_{high}		600		-	ns
Rise time of SDA and SCL signals	T_{rise}		-		300	ns
Fall time of SDA and SCL signals	T_{fall}		-		300	ns
Setup time for STOP condition	T_{susto}		600		-	ns

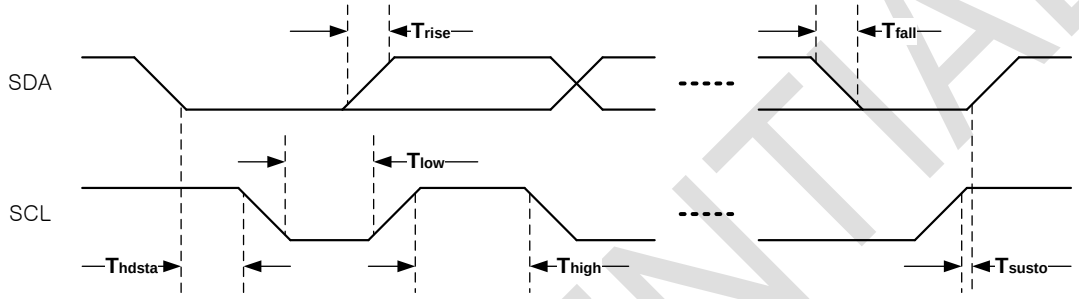


Figure 3. I²C Mode Timing

4.6. Switching Characteristics – Audio Interface

Parameters	Symbol	Min	Max	Unit
BCK high time	t_{bh}	20	-	ns
BCK low time	t_{bl}	20	-	ns
SDATA setup time before BCK rising edge	t_{ds}	10	-	ns
SDATA hold time after BCK rising edge	t_{dh}	10	-	ns
WCK setup time before BCK rising edge	t_{ws}	20	-	ns
BCK rising edge before WCK edge	t_{wh}	20	-	ns
BCK falling edge before WCK edge	t_{wl}	-20	20	ns
Rising/Falling time for BCK/WCK	$t_{br}/t_{bf}/t_{wrf}$	-	50	ns

※ Schmitt trigger characteristics (V_{SIH} Min = 1.85V, V_{SIH} Max = 0.9V)

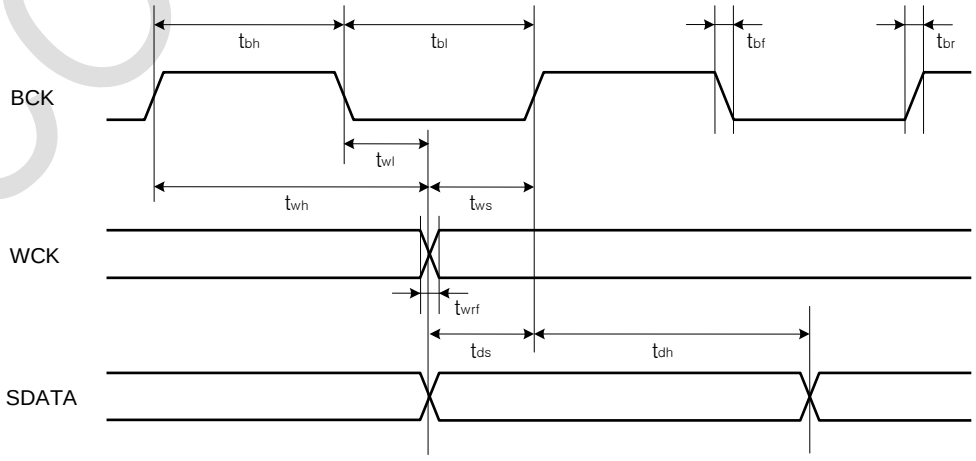


Figure 4. Audio Interface Timing

5. I²C BUS OF NTP8824

The NTP8824 uses an industry standard Inter IC Control (I²C) bus to communicate with host IC. A host IC can write or read internal registers of the NTP8824 via the I²C bus.

5.1. General Description of I²C Bus

The I²C bus uses two signal lines – a serial clock line (SCL) and a serial data line (SDA). Because the SDA line is open-drain type port, both the NTP8824 and a host IC can only drive these pins low or leave them open.

In I²C bus, a master device means the device which generates serial clock on the SCL. A slave device means the device which receives serial clock. There can be many master and slave devices on an I²C bus. But, when one master device works on the bus, the other master devices should not generate signal on the lines. These unexpected interrupts can make other slave devices to fail to communicate with the mater device.

The NTP8824 supports only slave mode of I²C bus. So, the NTP8824 always receives serial clock from a host IC. The slave mode is enough to write/read data to/from the NTP8824.

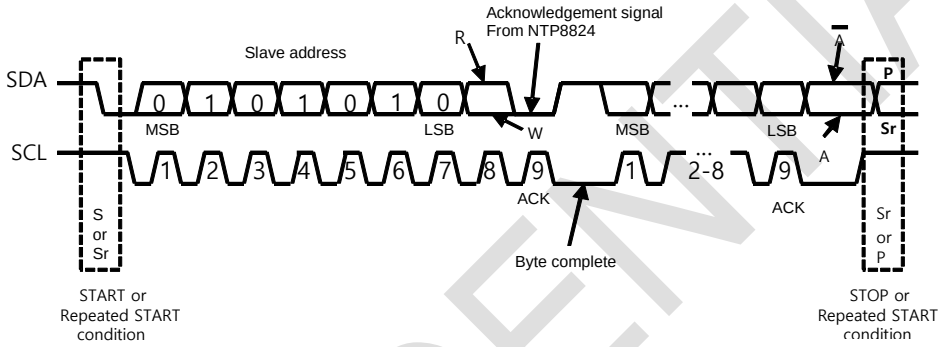


Figure 5. Basic Signaling Elements of I²C Bus

If there are no communication on I²C bus, lines must keep in high state. I²C bus begins communication with the start condition and ends communication with the stop condition. The start condition can be generated by changing the SDA state high to low, during the SCL state remains in high. The stop condition can be generated by changing the SDA state low to high during the SCL remains in high state. Be aware that the stop condition always reset the internal status of I²C bus control logic. Except these two conditions, the SDA may not change during the SCL in high state. Otherwise, abnormal start or stop condition will be generated.

I²C bus transfers the MSB of a byte on 1st data slot and the LSB of a byte on 8th data slot. I²C bus checks success or fail of transfer on every 1 byte transfer. The device which found an expected data on SDA must generate acknowledgement (keep low on SDA) on 9th clock. If there is no acknowledgement on 9th clock, the device which generated a data on SDA may stop transfer. The NTP8824 will generate acknowledgement for every successful data transfer of 1 byte in write mode. But, in read mode, because data is generated by the NTP8824, the NTP8824 will not generate an acknowledgement. In this case, on the contrary, the NTP8824 will check SDA state on 9th clock that the master device received a read data properly.

Because there can be many other slave device on the I²C bus, the master device sends a target slave address on the 1st byte. 7 bits from 1st to 7th bit of 1st byte are used for the slave address. The NTP8824 will response with slave address 0101010 or 0101011. If the AD pin was on low state in low to high transient of the RESET pin, the NTP8824 will use 0101010 for a slave address. Else if the AD pin was on high state in low to high transient of the RESET pin, the NTP8824 will use 0101011 for a slave address.

AD	I²C Address
0	0x54
1	0x56

Table 2. I²C Address

Last 8th bit of the 1st byte is used to indicate whether the master device want to write or read data.

5.1.1. Writing Operation

When last 8th bit of the 1st byte is set to low state, the writing operation of I^2C bus begins. The NTP8824 supports 3 kind of writing operations which presented on **Figure 6**.

The type presented on **Figure 6-(a)** is single byte write operation. “Sub address” on 2nd byte means the internal register address of the NTP8824. The “Data” on 3rd byte will be written into the internal register address on “Sub address”. If stop condition is not generated, writing “data” on specific “sub address” can be repeated like **Figure 6-(b)**. “Data #n” will be written on “sub address #n”.

The type presented on **Figure 6-(c)** is single byte write operation under address auto increment mode. The AIF on 1st bit of 2nd byte is the address auto increment flag. If SDA is set to high state on AIF slots, the NTP8824 write data continuously with register addresses which increased from initial “sub address” for every byte; “Data #n” will be written on “sub address” + n – 1. The internal address will cycle automatically.

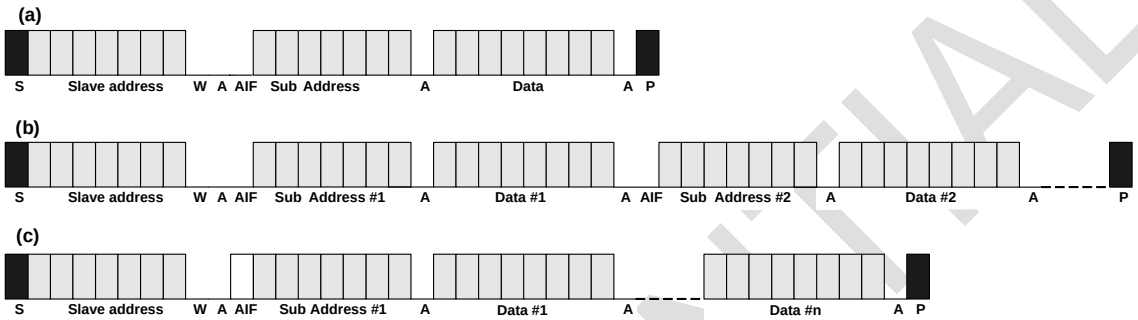


Figure 6. Single Byte Write Mode Sequence

Figure 7-(a), Figure 7-(b), and **Figure 7-(c)** represent 4 byte writing operations. Coefficient Mode Register address 0x00~0x5B are used to configure Bi-Quad filter coefficients, those are BQ, QMF_BQ, Loudness filter gain, attack gain, power meter gain and BQ/DRC check. The data size of these coefficients and gains is 4 byte for each. The difference between 4byte writing operation and single byte writing operation is only the size of transferring data. So, after sending “Sub address”, 4 sequential bytes must be transferred from the MSB(most significant byte) to the LSB(least significant byte) sequence.

The type presented on **Figure 7-(c)** is quad byte write operation under address auto increment mode, AIF function. Please compare the data transfer size between **Figure 6** and **Figure 7.**

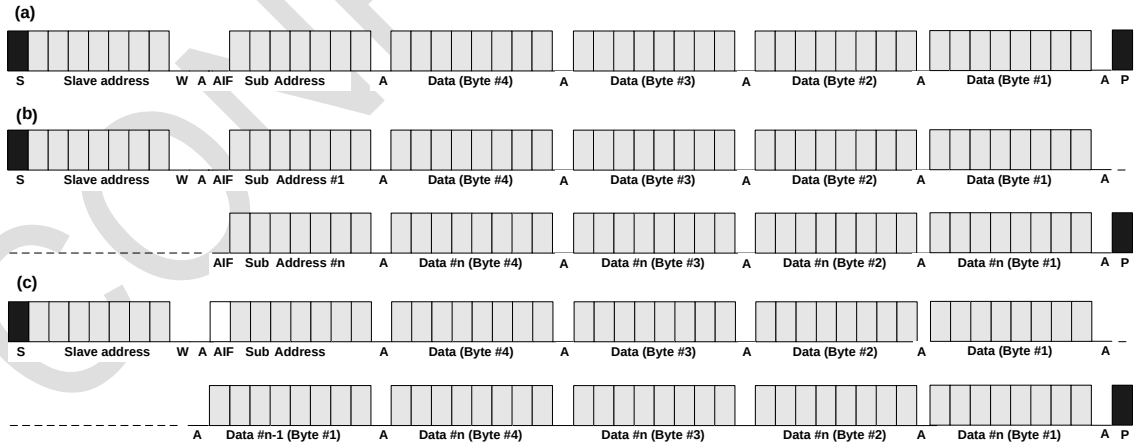


Figure 7. Quad Byte Write Mode Sequence

The coefficient mode register address from 0x00 to 0x31 and from 0x5C to 0x65 are used for the Bi-Quad filter coefficients in the coefficient mode. Each Bi-Quad filter uses 5 coefficients. Any unexpected coefficient value changes on any part of 5 coefficients can generate unstable Bi-Quad filter response. For example, if only one of 5 coefficients for a Bi-quad filter is changed and downloaded, its combined 5-coefficient set can have unstable operation while old and new coefficients are mixed together. Therefore to prevent this kind of problem, the NTP8824 writes coefficients to coefficient registers only

when the last 5th coefficients of each Bi-quad filter are downloaded, which means all of 5 coefficients are fully ready. Please refer to 9.1 for more detailed operation.

5.1.2. Reading Operation

Figure 8-(a) represents single byte reading operation from the NTP8824. To read data from the NTP8824, generate start condition to start transfer. After then, send “slave address” with write mode flag and send the register address(sub address). By regenerating start condition (Sr) again and transferring “slave address” with read mode flag, reading operation begins. The NTP8824 will generate data on SDA signal synchronizing with serial clocks on the SCL. Because the SDA signal generated from the NTP8824, the master device must generate ACK on 9th slot to confirm that the master received read 1 byte successfully. However, if this is just one byte reading operation, NAK (not acknowledged) signal must be generated. Then stop condition must be generated to end transfer.
When AIF set to high on sub address like **Figure 8-(b)**, data will be read continuously with register addresses which are increased from initial “sub address” for every byte. To continue reading operation in this case, the master must generate ACK signal on every 9th slot to confirm that master received 1 byte successfully. Otherwise, reading operation will be terminated. To end address auto incrementing reading operation, generate NAK on 9th slot and generate stop condition.

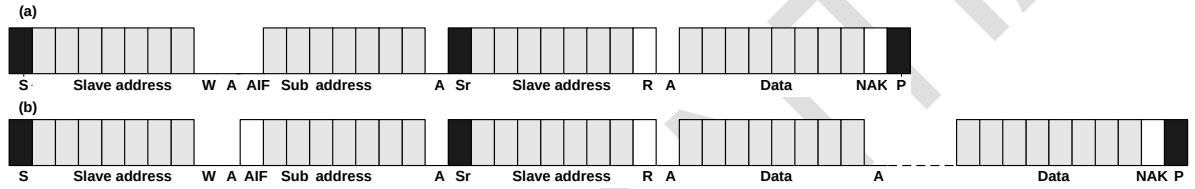


Figure 8. Single Byte Read Mode Sequence

Figure 9 represents quad byte reading operation. The difference between quad byte reading operation and single byte reading operation is only the size of receiving data. So, after sending “Sub address”, 4 sequential bytes must be received from the MSB to the LSB sequence.
The type presented on **Figure 9-(b)** is quad byte read operation under address auto increment mode, AIF function. Please compare the data receive size between **Figure 8** and **Figure 9.**

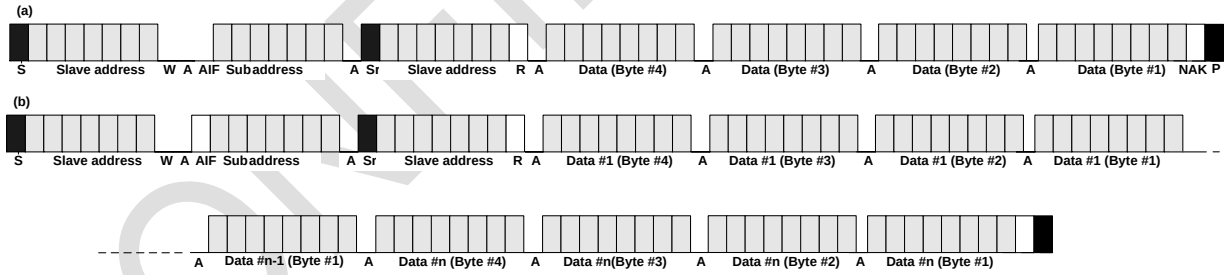


Figure 9. Quad Byte Read Mode Sequence

5.1.3. I²C Glitch Filter

To clean out the threats of noise in today’s high-speed-board system, the NTP8824 has a glitch elimination filter on the I²C ports. Glitches in the transmission lines of the I²C port can be safely removed with this function. Please refer to the register 0x66.

6. CLOCK, RESET & CONTROL

6.1. System Clock

The internal system clock of the NTP8824 is generated from an external master clock by the on-chip PLL. The NTP8824 supports external master clock frequency from 3.072 MHz to 24.576MHz. For proper operation, the registers for the PLL should be set correctly according to master clock frequency (Address 0x02).

6.2. Timing Sequence 1 (recommend)

For proper power up, initialization and power down of NTP8824, it is recommend to use the following sequence as shown in **Figure 10**.

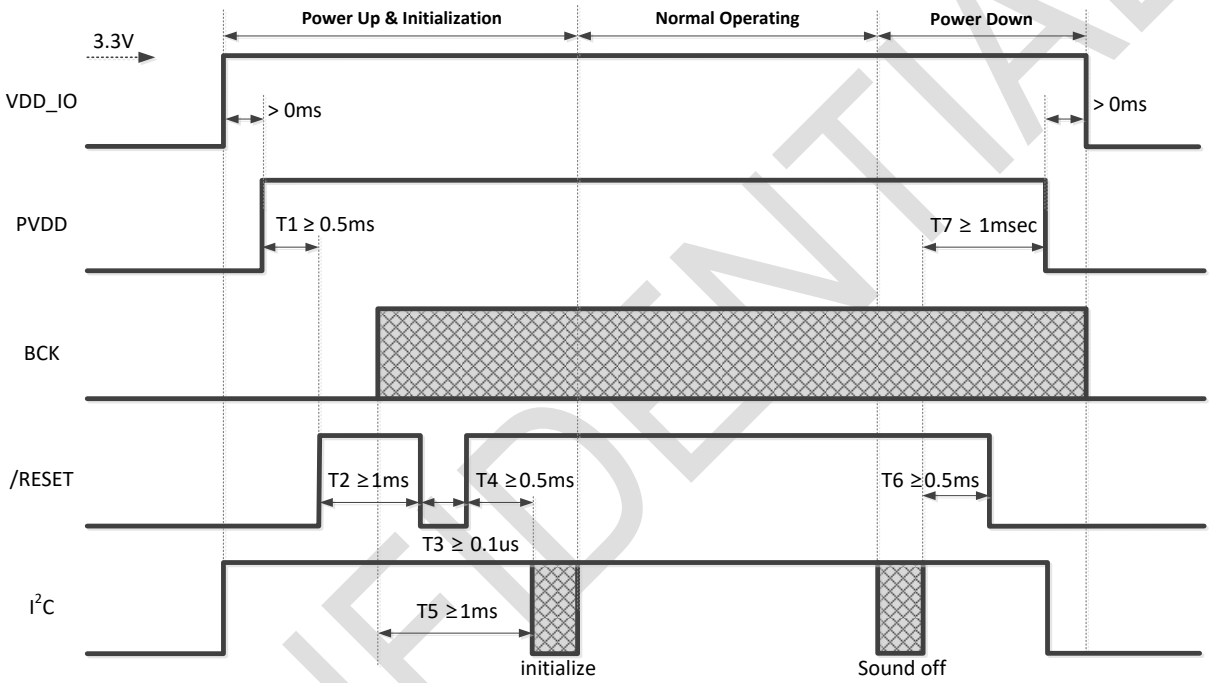


Figure 10. Timing Sequence 1

6.2.1. Power-Up & Initialization Sequence

1) Ramp up VDD_IO to at least 3.3V.
2) Ramp up PVDD.
3) After 0.5msec (T1≥0.5msec), drive /RESET = High, and then wait for at least 1msec (T2≥1msec).
4) Hold /RESET Low for at least 0.1usec (T3≥0.1usec)
5) Drive /RESET = High, and then wait for at least 0.5msec for I2C communication (T4≥0.5msec).
6) BCK signal should arrive at least 1msec before I2C initialization sequence (T5≥1msec).
7) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on (Address: 0x04, Data: 0xFF) sequence.

6.2.2. Power-Down Sequence

1) When both DC and AC power are off, make sure to execute sound off sequence (Address: 0x04, Data: 0x00).
2) Switch /RESET to Low after sound off sequence (T6≥0.5msec).
3) BCK and I2C should be Low after sound off sequence (T7≥0.5msec).
4) After I2C is Low, ramp down VDD_IO.

6.3. Timing Sequence 2 (reference)

Following figure illustrates another timing sequence, which is conforming to the legacy reset timing.

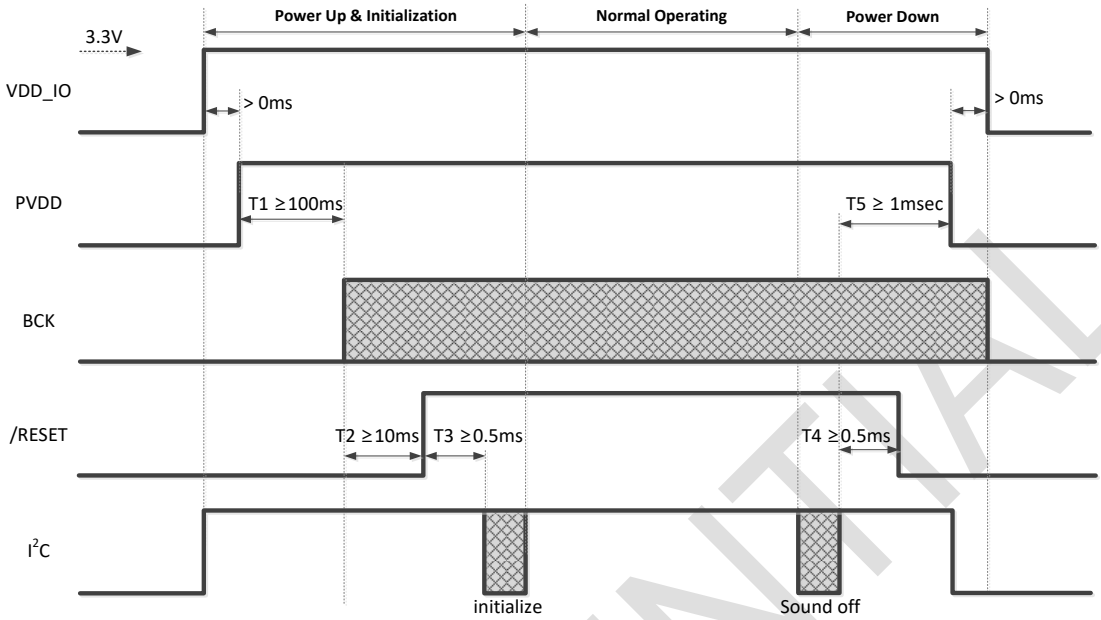


Figure 11. Timing Sequence 2

6.3.1. Power-Up & Initialization Sequence

1) Ramp up VDD_IO to at least 3.3V.
2) Ramp up PVDD.
3) Drive BCK signal at least 100ms after PVDD (T1≥100msec).
4) At least 10ms after BCK, Drive /RESET = High(T2≥10msec).
5) Wait for at least 0.5msec for I^2C communication (T3≥0.5msec) and keep the status.
6) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

6.3.2. Power-Down Sequence

1) When both DC and AC power are off, make sure to execute sound off sequence.
2) Switch /RESET to Low at least 0.5 msec after sound off sequence (T4≥0.5msec).
3) Ramp down PVDD at least 1 msec after sound off sequence (T5≥1msec).
4) After I^2C is Low, ramp down VDD_IO.

6.3. Sound On/Off Sequence

For proper sound on/off of NTP8824, use the following sequence as shown in **Figure 12**.

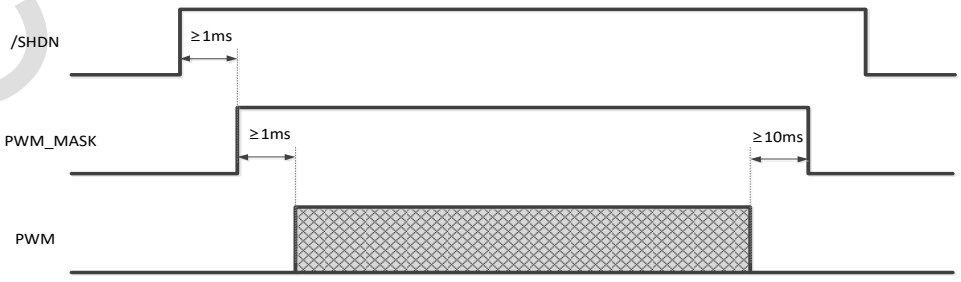


Figure 12. Sound On & Off Sequence

To prevent pop noise when enabling or disabling the amplifier, the following sequences are recommended.

7. AUDIO INPUT

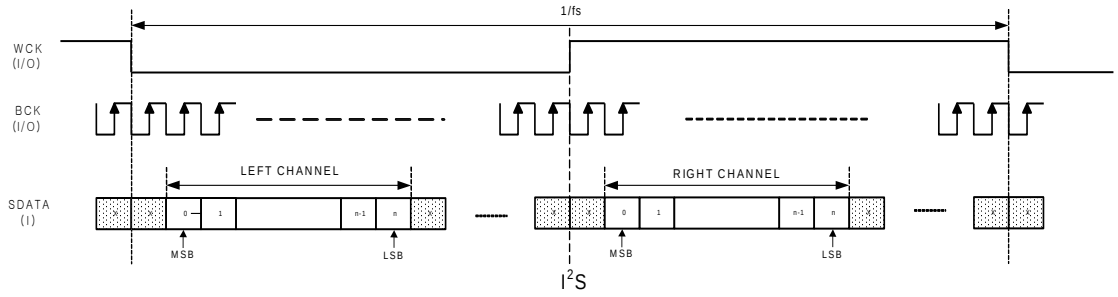
7.1. I^2S

NTP8824 receives audio data through digital audio interface. There is a standard digital audio interface - the Inter-IC Sound (I^2S) Interface.

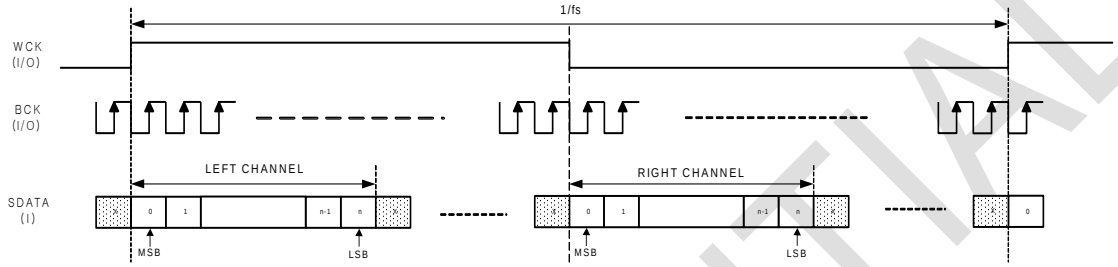
These interfaces use 2 clock lines and 1 data line to receive the audio data. One of these clock lines is the WCK. A period of the WCK is same with sampling period of audio data i.e. 64bits (32bits for each channel). One of the main function of WCK to define the channels, the low state of WCK indicates the 1^{st} channel i.e. left channel and the high state indicate the 2^{nd} channel i.e. right channel. This feature enable the clock receiving device to synchronize the data word-wise for transmitting or receiving from clock generating device.

The other clock line is BCK. This clock line used to synchronize the bit-wise data. The number of clock for one WCK period is 64 clock of BCK. The name of data transfer line is SDATA. The data being synchronized with the BCK must be loaded on this line. NTP8824 receive data on rising edge of the BCK. The bit range for I^2S is predefined.

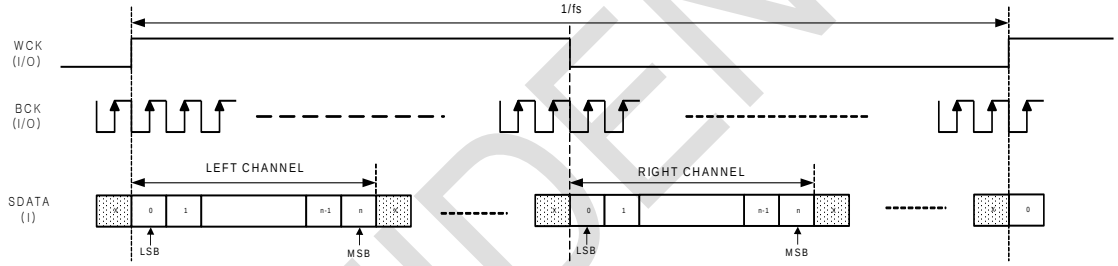
NTP8824 can only work as a slave on bus. In slave mode, NTP8824 receives WCK and BCK from external source. Please refer the following **Figure 13**.



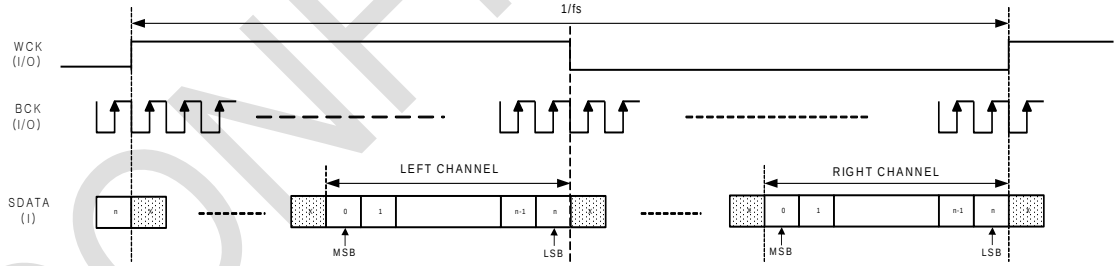
I²S



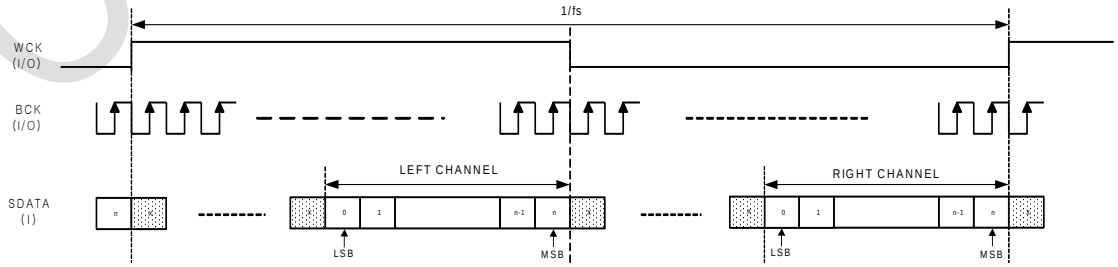
GSA, Left Justified, MSB first



GSA, Left Justified, LSB first



GSA, Right Justified, MSB first



GSA, Right Justified, LSB first

Figure 13. I²S Audio Interface Format

7.2. SDATA Generator

The SDATA generator of NTP8824 sends out I2S out signal. In order for SDATA out process to function stably, the falling of BCK should either synchronize or occur ahead of falling or rising of WCK. Refer to the register Address 0x76 and 0x7C in the **Appendix A** and refer to the **4.6. Switching Characteristics – Audio Interface**.

SDATA Generator (Sdata out)	Register value	
	0x0F	0xF0
Register Address 0x76	Sdata out => Monitor 1 pin	Sdata out => Monitor 2 pin

Table 3. SDATA Generator Control

8. MIXER

Channel mixer can be used in lots of application needs like pseudo stereo and etc. User can mix input channels into each output channels with designated gains and polarity. Step size of mixer gain is variable according to the gain level as shown below.

Volume Range (dB)	Step (dB)
+18 ~ +6	1
+5.5 ~ -5.5	0.5
-6 ~ -32	1
≤ 32	-∞

Table 4. Variable Step Mixing Gain

In total, 4 mixing gain coefficients denoted as M00, M01, M10 and M11 are defined as shown in the equation below. Each Mxx stores volume value in dB scale, and the number values versus gain in dB are shown in the **Appendix B**. By default, each input channel connected to each output channel directly; M00 and M11 are set as 0 dB in plus polarity, M01 and M10 are set as -∞ dB.

[Output Channels] = [Mixer Matrix] x [Input Channels]

$$\begin{bmatrix} \text{CH1 OUT} \\ \text{CH2 OUT} \end{bmatrix} = \begin{bmatrix} \text{M00} & \text{M01} \\ \text{M10} & \text{M11} \end{bmatrix} \cdot \begin{bmatrix} \text{CH1 IN} \\ \text{CH2 IN} \end{bmatrix}$$

Figure 14. Serial Mixer Matrix

In order to load mixer coefficients into internal memory, send the index value in the gain value table to the register address 0x03~0x06. Each address matched to M00, M01, M10 and M11 sequentially.

9. PRE-PROCESSING

9.1. Bi-Quad Filter Chain

The Bi-Quad filter means 2nd order IIR filter. NTP8824 implemented a serial chain of Bi-Quad filters with proprietary floating point operation schemes. The Bi-Quad filter chains can be used in various purposes; loudness control, parametric EQ, loud-speaker EQ, APEQ and etc. The Bi-Quad filter structure is shown in **Figure 15**.

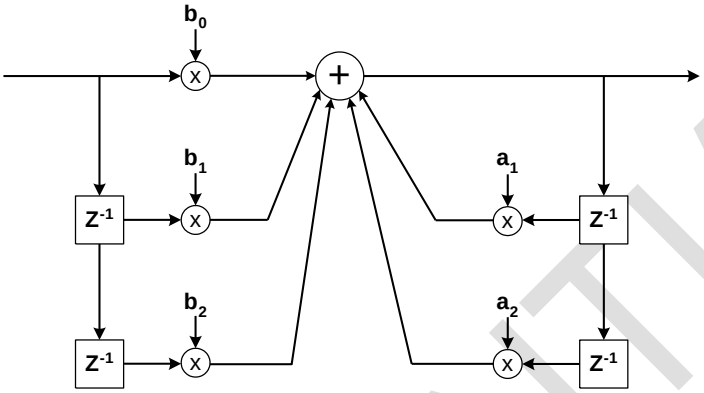


Figure 15. Bi-Quad Filter Structure

Twelve Bi-Quad filters are linked serially for one channel. The Bi-Quad filters can be configured differently for each filter. As shown in **Figure 16**, first three filters can be used for loudness control, last six filters for APEQ control.

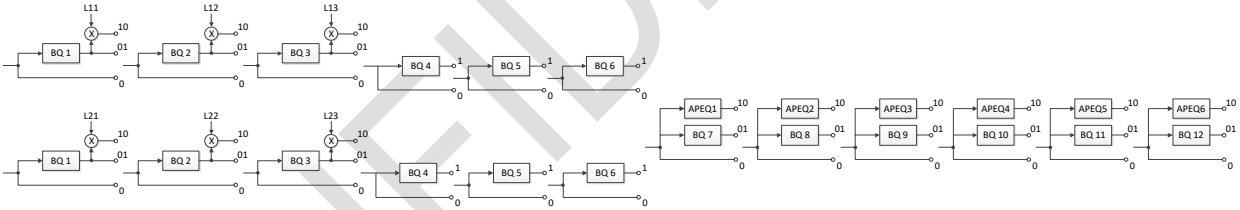


Figure 16. Bi-Quad Filter Chain

Filter coefficients are 32-bit floating point numbers and can be downloaded thru I^2C interface. To download Bi-Quad filter coefficients to NTP8824, select download channel by using CH flag in register Address 0x7E first. Then, write actual coefficient values to 60 register addresses, from 0x00 to 0x65 in the coefficient register addresses.

The coefficient mode register addresses from 0x00 through 0x04 designate the five coefficients of the first Bi-Quad (BQ1) and represent coefficients b0, b1, b2, a1, a2 respectively. The coefficient mode register addresses from 0x05 through 0x09 designate coefficients of the 2nd Bi-Quad (BQ2) filter, and so on. The enable/disable operation of these Bi-Quad filters can be made by using BQF flag in register addresses of 0x0E~0x15.

Coefficient Mode register	0x00 ~ 0x04	0x05 ~ 0x09	0x0A ~ 0x0E	0x0F ~ 0x13	0x14 ~ 0x18	0x19 ~ 0x1D	
When system address 0x7E = 0x01, 0x7E = 0x02	BQ1 of CH1/2	BQ2 of CH1/2	BQ3 of CH1/2	BQ4 of CH1/2	BQ5 of CH1/2	BQ6 of CH1/2	
Coefficient Mode register	0x1E ~ 0x22	0x23 ~ 0x27	0x28 ~ 0x2C	0x2D ~ 0x31	0x50 ~ 0x52	0x5C ~ 0x60	0x61 ~ 0x65
When system address 0x7E = 0x01	BQ7	BQ8	BQ9	BQ10	Loudness Gain	BQ11	BQ12

Coefficient Mode register	0x00 ~ 0x05	0x06 ~ 0x0B	0x0C ~ 0x011	0x12 ~ 0x17	0x1F ~ 0x24
When system address 0x7E = 0x08	Coefficient 0 of APEQ 1 ~ 6	Coefficient 1 of APEQ 1 ~ 6	Coefficient 2 of APEQ 1 ~ 6	Coefficient 3 of APEQ 1 ~ 6	Coefficient 4 of APEQ 1 ~ 6

Table 5. Address of Coefficients for Bi-Quad Filter Chain

9.2. Loudness Control

NTP8824 provides loudness control function using coefficient values. Loudness control means the compensation of frequency characteristics in low volume level to fit the acoustic characteristics of human ears.

There are 3 coefficient values for loudness gain per each channel. To download a loudness gain of each coefficient, the page flag register 0x7E should be set as same in the case of downloading the filter coefficients. The loudness gain values are applied for both channel 1 and 2, and when downloading the loudness gain values, a user should set the register 0x7E as 0x03.

loudness gains of CH1/CH2	Coefficient Mode Register Address		
	0x50	0x51	0x52
Register Address 0x7E= 0x03 case	L1	L2	L3

Table 6. Address for Loudness Gain

9.3. Advanced Parametric Equalizer

NTP8824 has a new scheme for APEQ function using coefficient values. APEQ function means the compensation of frequency characteristics based on input signal level to fit the acoustic characteristics of human ears.

APEQ needs a Bi-Quad filter coefficient and five additional coefficients, which comprise a gain coefficient and a threshold coefficient. To download each coefficient, the page flag register 0x7E should be set as same in the case of downloading the filter coefficients. The coefficient values are applied for both channel 1 and 2.

APEQ coefficient of CH1/CH2	Coefficient mode register address				
	0x00 ~ 0x05	0x06 ~ 0x0B	0x0C ~ 0x11	0x12 ~ 0x17	0x1F ~ 0x24
Register Address 0x7E = 0x08 case	Coefficient 0 *f*(Gain)	Coefficient 1 *f*(Gain)	Coefficient 2 *f*(Gain)	Coefficient 3 *f*(Gain)	Coefficient 4 *f*(Threshold)

Table 7. Address for APEQ Coefficient

10. VOLUME & DYNAMIC RANGE CONTROL

Master and channel volumes of the NTP8824 are independently controlled and softly changed. The system register address 0x0C is the master volume control that affects both channels simultaneously and the address 0x17 and 0x18 correspond to the channel volume control register for channel 1 and 2 respectively.
The possible Maximum Gain is +48.375dB with using master volume fine control, master volume and channel volume because the master volume applies the gain to an input signal independent from a channel volume. However, in such a case, a clipping might occur to prevent a signal overflow error if the magnitude of the input signal is large enough to exceed 0dB under the combined volume setting.

10.1. Master Volume Control

By setting volume control register (address 0x0C), master volume is controlled from negative infinity through 0dB with selectable step size as follows. For details on the master volume setting, see the register value table shown in **Appendix B**.

Step	Range
0.5 dB	0 ~ -125 dB

Table 8. Level Dependent Master Volume Steps

10.2. Channel Volume Control

By setting volume control registers (address 0x17 and 0x18), channel volumes are independently controlled from negative infinity through +48dB with two selectable step sizes as described below, and in the **Appendix B**, exact values for channel volume setting are described.

Step	Range
0.5 dB	+48 ~ -79 dB

Table 9. Level Dependent Channel Volume Steps

10.3. Master Volume Fine Control

Fine control for master volume is possible (+0.125dB step up to maximum +0.375dB boost). Refer the system register Address 0x16 in the **Appendix A**.

10.4. Mute and Soft Volume Change

The NTP8824 enters mute state by setting soft mute flag of register Address 0x33. Soft mute is implemented so that the volume gradually increases or decreases when mute is turned off or on respectively. Also the soft mute speed and soft volume change speed rates are programmable. Designers can minimize the pop noise by controlling the soft mute speed and volume change intervals. Refer SM flag of register Address 0x33 and SVI flag of register Address 0x30.

10.5. Auto Mute

The NTP8824 can mute the sound automatically when the level of input audio signal is lower than the register-controlled threshold value. The mute can be done by PWM switching with 50 % duty ratio.
Auto mute is supported for internal channels 1~2 after 2x2 mixer block. Refer register Address 0x3A.

10.6. Dynamic Range Control

NTP8824 has a new scheme for dynamic range control, which comprise a high band DRC, a low band DRC, a sub band DRC and a post DRC. The input data is filtered by HPF, LPF and SPF, and then processed by H-DRC, L-DRC and SDRC respectively. Three processed results are merged and followed by post DRC, which produces the output data with the fully controlled dynamic range. For detailed setting of the DRC registers, please refer to the system register addresses in **Table 10**.

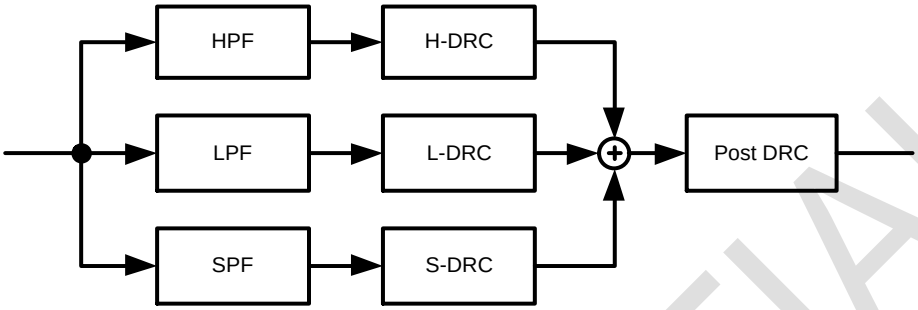


Figure 17. Block Diagram of Dynamic Range Control

3B' DRC Coefficient mode register	0x32 ~ 0x36	0x37 ~ 0x3B	0x3C ~ 0x40	0x41 ~ 0x45	0x46 ~ 0x4A	0x4B ~ 0x4F
When System Address 0x7E = 0x03	LPF1 of L-DRC	LPF2 of L-DRC	HPF1 of H-DRC	HPF2 of H-DRC	SPF1 of S-DRC	SPF2 of S-DRC

Table 10. Coefficient Register Map for Dynamic Range Control

10.7. Power Meter

The power meter measures signal's energy of internal, send value of energy through register address 0x2E and always operates without on/off control, and read value through register address 0x2F.
(refer to the **Table 20. Power Meter Reading Table**)
Because audio signals swing very rapidly in process of time, a user can use the power meter gain to get stable value of energy. The more power meter gain approaches to maximum value, the more value of energy changes slowly.
Power meter gain is 32-bit floating point numbers and can be downloaded thru I^2C interface. To download power meter gain, page flag register 0x7E should be set 0x01 or 0x03. And then write gain value to 0x58 register address.

11.OUTPUT INTERFACE

11.1. Output Configuration

The output of NTP8824 has various options. To produce proper output signal, register 0x3C, 0x34, 0x3E, 0x3F, 0x40 and 0x43 should be set to appropriate values.

11.2. PWM Output Mapper

Any internal channel that produces a PWM output can be assigned to any PWM output hardware port (or pin) by mapping output port register. This feature is very helpful for the hardware designer because it can relieve difficulties in the power stage signal routing and channel assignment if the output channel order is fixed. See the system register address 0x40 in the **Appendix A**.

11.3. Switching Output Mode

There are two selectable switching output modes in NTP8824. The difference between two output modes lies in the relationship of the relative signal pattern between PWM OUTxA and PWM OUTxB for a channel x. The first one is called as AD mode. This AD mode can be applied to both half bridge and full bridge output stage.

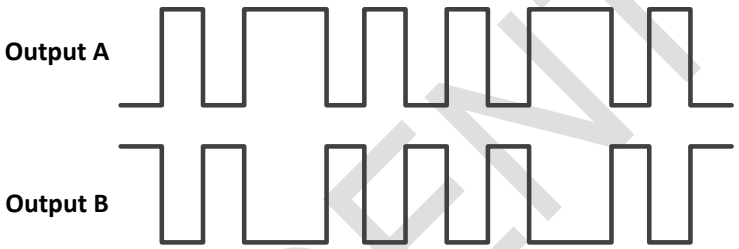


Figure 18. PWM Output Signals in AD Mode

AD asynchronous pair means the normal AD mode PWM output. In other words, A output and B output of each PWM output pair are mutually complementary. In the case of AD synchronous pair, A output and B output is perfectly identical, and its relation is not complementary. This is useful in some special case including single-ended power stage design.
The other one is called as NTX (Neo Trinity Amplification), which is D-BTL mode. This mode is applied only for BTL, and its operation is dynamically-biased BTL, compared to the normal BTL. An example of output signals in D-BTL mode is shown in **Figure 19.**

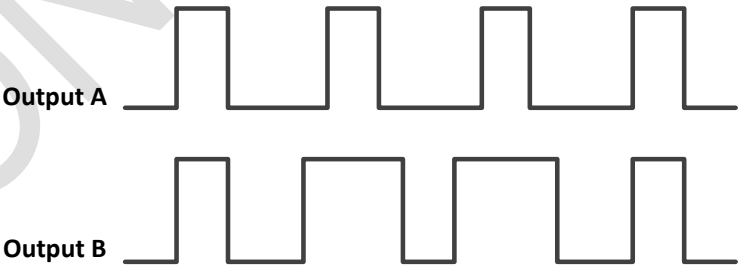


Figure 19. PWM Output Signals in D-BTL Mode

For D-BTL mode, there are two additional parameters, which is MLP (Minimum Linear Pulse Length). MLP defines the minimum pulse length that can guarantee a linear relationship between the input and output pulse length. Generally, the width of the output pulse is proportional to that of the input pulse. However, as the width of input pulse becomes narrower, such linear relation is not maintained due to the characteristic of a power device. The minimum MLP value is preferred as long as linear relationship between the input and the output pulse is satisfied. In addition, in terms of power consumption, a minimal MLP value is preferred.
This compensation is illustrated in **Figure 20.**

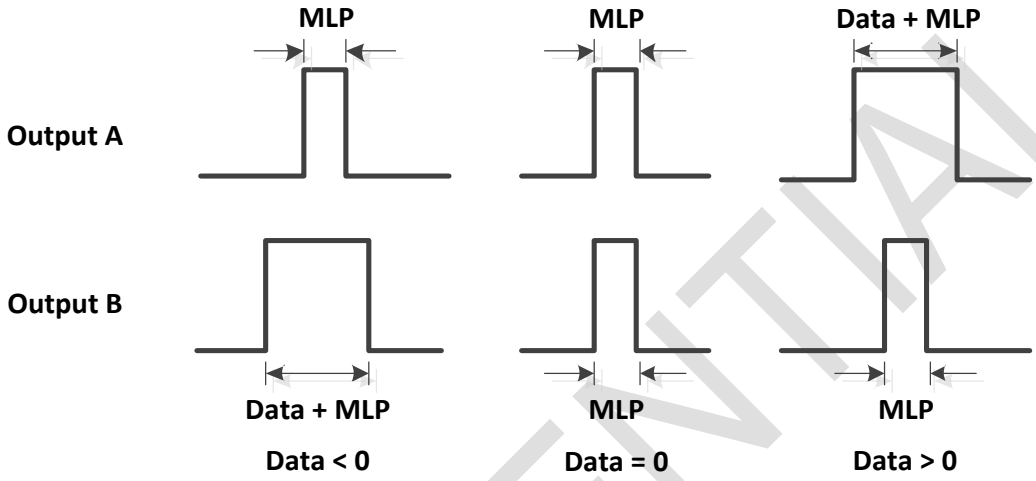


Figure 20. Compensation by MLP

11.4. Soft Start

The soft_start reduces pop noise by controlling rapidly increased energy of PWM.
To begin soft_start operation, PWM soft start enable register (0x4A: PSE) should be set to high, and then PWM switching on/off register (0x34: POF) should be set to low. The duty ratio of PWM output increases from 127:1 (Low:High) to 50:50 (Low:High). Step repeat time register (0x4A: SRT) means repeat number of PWM output in one duty sector. Soft_start operation with 17 repetitions is shown in the **Figure 21**.

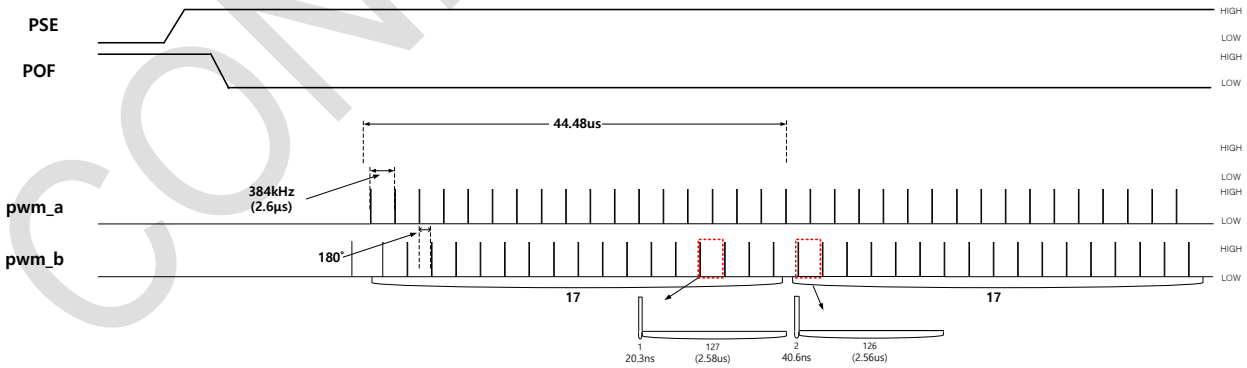


Figure 21. Soft Start Operation Timing

12. DC PROTECTION

This DC protection block prevents the system from outputting DC signal, which can cause a speaker unit burnt. Three sub functions are employed to prevent DC output, which are monitoring a memory checksum, observing a modulation index, and cutting DC output via hard-wired filters. Except for the hard-wired DC cut filter, the other two blocks only reports the error status, and external MCU may reset the amplifier chip by setting the DC soft reset register to high.

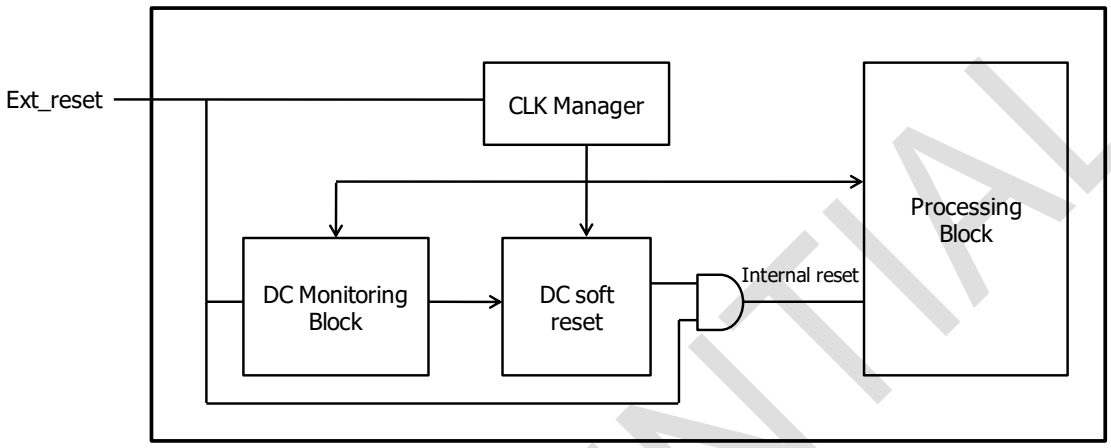


Figure 22. Block Diagram for DC PROTECTION

12.1 Memory Checksum

While initializing the system, the checksum data of coefficients are downloaded from the external MCU from the address 0x53 through 0x5A. This memory checksum block compares the checksum data of current memory block and the checksum data at the initial time. If there happens a discrepancy between two values due to some memory fault, the error flag of address 0x5B is set to high. The external MCU can monitor this error flag and reset the chip by setting the DC soft reset to high at address 0x52. This DC soft reset will initialize the whole chip, and initialization process of the memory should be done thereafter.

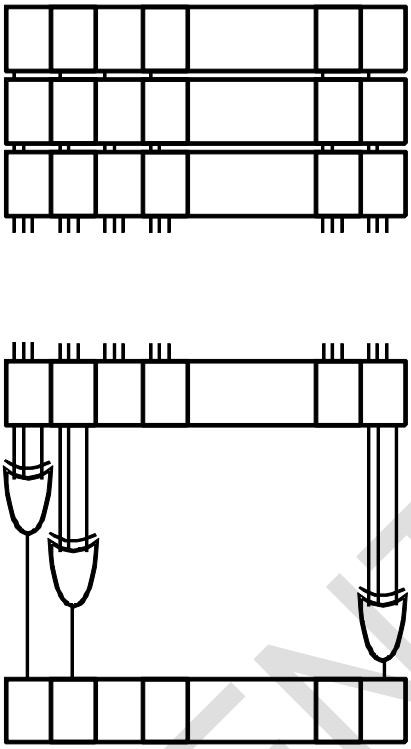


Figure 23. Structure of Memory Checksum

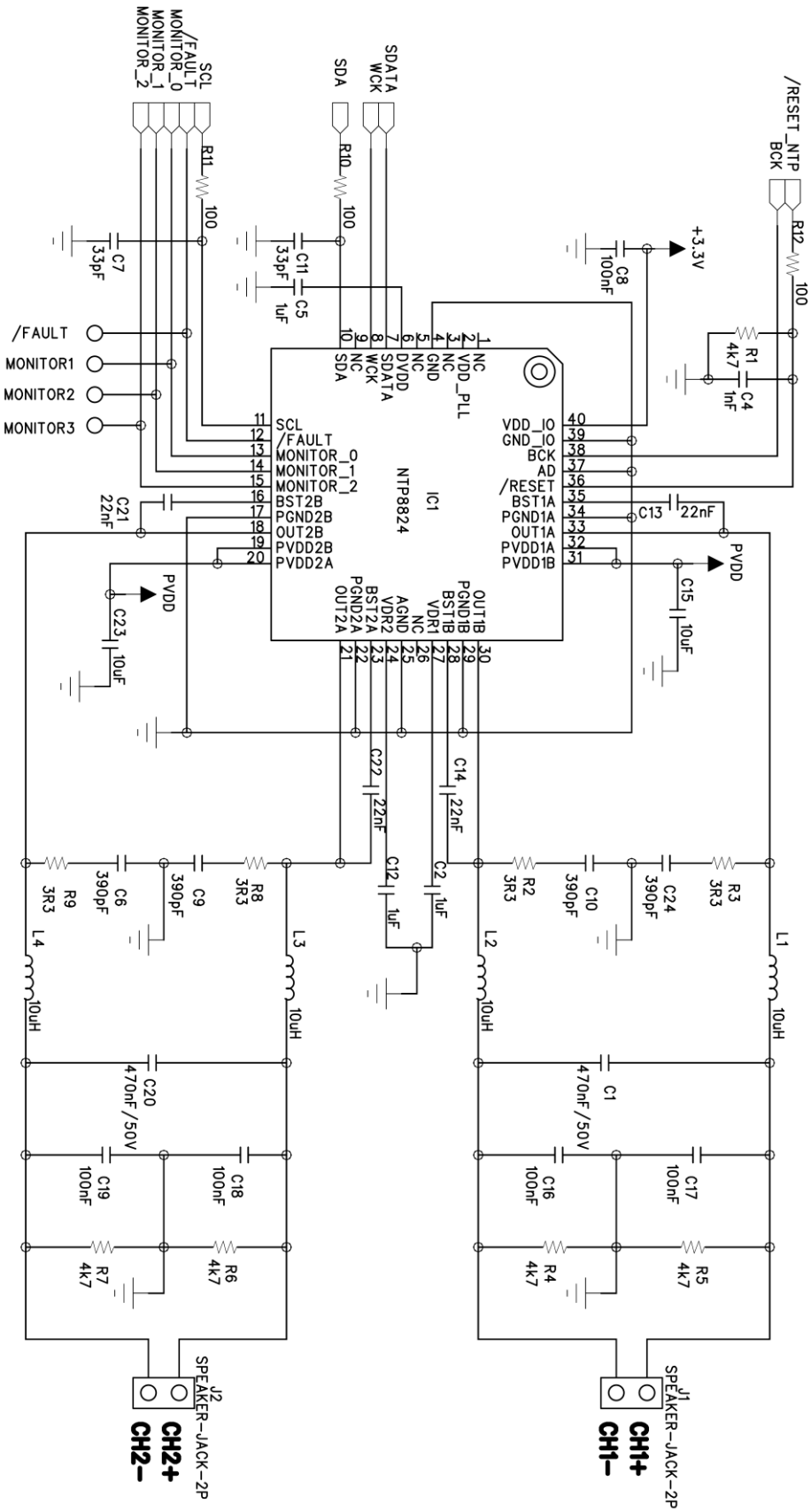
12.2 Modulation Index Check

When there is a DC component in the output, the modulation index tends to stay over or under certain value. The modulation index check block constantly monitors the PWM modulation index, and if the index value continues to stay over or under certain period of time, it sets modulation index error flag of address 0x5B to high. The external MCU can monitor this error flag and reset the chip by setting the DC soft reset the register value of address 0x52 to high. The PWM modulation duty at address 0x50 and 0x51 can be set to decide the level of DC monitoring for AD and D-BTL mode respectively.

12.3 Hard-wired DC cut

The hard-wired DC cut filters prevent the system from outputting the signal of less than 1Hz frequency. The hard-wired DC cut filters exist in the Bi-quad filter chain.

13. TYPICAL APPLICATION SCHEMATICS



14. APPENDIX

A. Configuration Register Summary

Addr 0x00: Audio Input Format

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	INS

Name	Description	Value	Meaning	Ref.
INS	Input format	**b'0**	I^2S, slave mode	
		b'1	General serial audio, slave mode	

Addr 0x01: General Serial Audio Format

Bit	7	6	5	4	3	2	1	0
Name	X	X	BCKS		BS		MLF	LRJ

Name	Description	Value	Meaning	Ref.
LRJ	Serial data justify	**b'0**	Left justify	
		b'1	Right justify	
MLF	Serial bit order	**b'0**	MSB first	
		b'1	LSB first	
BS	Serial bit size	**b'00**	24 bit	
		b'01	20 bit	
		b'10	18 bit	
		b'11	16 bit	
BCKS	Bit clock size select	**b'00**	64 BCK/WCK	
		b'01	48 BCK/WCK	
		b'10	32 BCK/WCK	

Addr 0x02: Master Clock Frequency Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	MCF		

Name	Description	Value	Meaning	Ref.
MCF	Master Clock Frequency	**b'000**	3.072 MHz (WCK 48 kHz) / 2.8224 MHz (WCK 44.1 kHz)	
		b'001	6.144 MHz (WCK 96 kHz)	
		b'010	2.048 MHz (WCK 32 kHz)	

Addr 0x03~0x06: Mixer Gain

Bit	7	6	5	4	3	2	1	0
Name	X	MG						

Name	Description	Value	Meaning	Ref.
MG	Mixer gain	h'00 ~ h'7E	Mixer gain (refer to gain table)	

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0x03 & 0x04 \\ 0x05 & 0x06 \end{bmatrix} \bullet \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Mixer equation

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0dB(0x4E) & -\infty dB(0x00) \\ -\infty dB(0x00) & 0dB(0x4E) \end{bmatrix} \bullet \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Reset default

Reserved Address 0x07 ~ 0x0B

Addr 0x0C: Master Volume & SPK PWM Switching On/Off Control

Bit	7	6	5	4	3	2	1	0
Name	MVOL						SPOF	

Name	Description	Value	Meaning	Ref.
SPOF	Smart Switching Output on/off Control	**b'00000000**	PWM off (softmute on → pwm off → pwm_mask low)	
		b'00000001	PWM off (softmute on → pwm off→ pwm_mask high)	
		b'00000010	PWM on (softmute on → pwm_mask high → pwm on)	
		b'00000011	PWM on (pwm_mask high → pwm on → softmute off)	
MVOL	Volume control	b'00000100 ~ b'11111111	refer to master volume table. Reset default is 0x00 (= −∞ dB). 0xFF means 0dB with 0.5dB step	

Reserved Address 0x0D

Addr 0x0E~0x0F: PEQ Filter Control 0 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	BQ3		BQ2		BQ1	

Name	Description	Value	Meaning	Ref.
BQ1	On/off Bi-Quad 1 of ch. n (n= 1,2)	**b'00**	Bypass Bi-Quad 1 of channel n	
		b'01	Enable Bi-Quad 1 of channel n	
		b'10	Enable Bi-Quad 1 as Loudness Filter	
BQ2	On/off Bi-Quad 2 of ch. n (n= 1,2)	**b'00**	Bypass Bi-Quad 2 of channel n	
		b'01	Enable Bi-Quad 2 of channel n	
		b'10	Enable Bi-Quad 2 as Loudness Filter	
BQ3	On/off Bi-Quad 3 of ch. n (n= 1,2)	**b'00**	Bypass Bi-Quad 3 of channel n	
		b'01	Enable Bi-Quad 3 of channel n	
		b'10	Enable Bi-Quad 3 as Loudness Filter	

Addr 0x10~0x11: PEQ Filter Control 1 for Ch1, Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	BQ6	BQ5	BQ4

Name	Description	Value	Meaning	Ref.
BQ4	On/off Bi-Quad 4 of ch. n (n= 1,2)	**b'0**	Bypass Bi-Quad 4 of channel n	
		b'1	Enable Bi-Quad 4 of channel n	
BQ5	On/off Bi-Quad 5 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 5 of channel n	
		b'1	Enable Bi-Quad 5 of channel n	
BQ6	On/off Bi-Quad 6 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 6 of channel n	
		b'1	Enable Bi-Quad 6 of channel n	

Addr 0x12~0x13: APEQ Filter Control 0 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	BQ10		BQ9		BQ8		BQ7	

Name	Description	Value	Meaning	Ref.
BQ7	On/off Bi-Quad 7 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 7 of channel n	
		b'01	Enable Bi-Quad 7 of channel n	
		b'10	Enable Bi-Quad 7 of channel n as APEQ	
		b'11	Reserved	
BQ8	On/off Bi-Quad 8 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 8 of channel n	
		b'01	Enable Bi-Quad 8 of channel n	
		b'10	Enable Bi-Quad 8 of channel n as APEQ	
		b'11	Reserved	
BQ9	On/off Bi-Quad 9 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 9 of channel n	
		b'01	Enable Bi-Quad 9 of channel n	
		b'10	Enable Bi-Quad 9 of channel n as APEQ	
		b'11	Reserved	
BQ10	On/off Bi-Quad 10 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 10 of channel n	
		b'01	Enable Bi-Quad 10 of channel n	
		b'10	Enable Bi-Quad 10 of channel n as APEQ	
		b'11	Reserved	

Addr 0x14~0x15: APEQ Filter Control 1 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	BQ12		BQ11	

Name	Description	Value	Meaning	Ref.
BQ11	On/off Bi-Quad 11 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 11 of channel n	
		b'01	Enable Bi-Quad 11 of channel n	
		b'10	Enable Bi-Quad 11 of channel n as APEQ	
		b'11	Reserved	
BQ12	On/off Bi-Quad 12 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 12 of channel n	
		b'01	Enable Bi-Quad 12 of channel n	
		b'10	Enable Bi-Quad 12 of channel n as APEQ	
		b'11	Reserved	

Addr 0x16: Master Volume Fine Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	MVFC	

Name	Description	Value	Meaning	Ref.
MVFC	Master volume fine control	**b'00** ~ b'11	0 dB ~ 0.375 dB with 0.125 dB step	

Addr 0x17~0x18: Ch1/2 Volume, respectively

Bit	7	6	5	4	3	2	1	0
Name	VOL							

Name	Description	Value	Meaning	Ref.
VOL	Volume control	b'00000000 ~ b'11111111	refer to channel volume table. Reset default is **0x9F** (= 0dB). 0xFF means 48dB with 0.5dB step.	

Addr 0x19: APEQ Path Option

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	OPT		

Name	Description	Value	Meaning	Ref.
Opt	APEQ Path Option	b'000	cut1=>Vol=>PEQ6=>APEQ6=>DRC=>cut2	Set b'000 for APEQ op. (Same effect btw b'000 & b'010)
		b'001	Reserved	
		b'010	cut1=>PEQ6=>Vol=>APEQ6=>DRC=>cut2	
		b'011	Reserved	
		b'100	cut1=>PEQ6=>APEQ6=>Vol=>DRC=>cut2	
		b'101	Reserved	

Addr 0x1A: APEQ Filter Control 2 for APEQ1 (BQ7)

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_DP1			A1C_DP1			

Name	Description	Value	Meaning	Ref.
A1C_DP1	APEQ attack time	**b'0000** ~ b'1010	Attack time control (refer to APEQ attack time table below)	
C1C_DP1	APEQ release time	**b'000** ~ b'111	Release time control (refer to APEQ release time table below)	

Value of Register	Attack time 6dB, fs = 96,000
0011	15msec
0010	8msec
0001	4msec
0000	2msec
0111	1msec
0110	0.5msec
0101	0.25msec
0100	0.125msec
1000	2.5msec
1001	3msec
1010	3.5msec

Table 11. APEQ Attack Time Table

Value of Register	Release time 6dB, fs = 96,000
011	5.0sec
010	2.0sec
001	1.0sec
000	0.5sec
111	0.2sec
110	0.1sec
101	0.05sec
100	0.025sec

Table 12. APEQ Release Time Table

Addr 0x1B: APEQ Filter Control 3 for APEQ2 (BQ8)

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_DP2			A1C_DP2			

Name	Description	Value	Meaning	Ref.
A1C_DP2	APEQ attack time	**b'0000** ~ b'1010	Attack time control (refer to APEQ attack time table in Addr 0x1A)	
C1C_DP2	APEQ release time	**b'000** ~ b'111	Release time control (refer to APEQ release time table in Addr 0x1A)	

Addr 0x1C: APEQ Filter Control 4 for APEQ3 (BQ9)

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_DP3			A1C_DP3			

Name	Description	Value	Meaning	Ref.
A1C_DP3	APEQ attack time	**b'0000** ~ b'1010	Attack time control (refer to APEQ attack time table in Addr 0x1A)	
C1C_DP3	APEQ release time	**b'000** ~ b'111	Release time control (refer to APEQ release time table in Addr 0x1A)	

Addr 0x1D: APEQ Filter Control 5 for APEQ4 (BQ10)

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_DP4			A1C_DP4			

Name	Description	Value	Meaning	Ref.
A1C_DP4	APEQ attack time	**b'0000** ~ b'1010	Attack time control (refer to APEQ attack time table in Addr 0x1A)	
C1C_DP4	APEQ release time	**b'000** ~ b'111	Release time control (refer to APEQ release time table in Addr 0x1A)	

Addr 0x1E: APEQ Filter Control 6 for APEQ5 (BQ11)

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_DP5			A1C_DP5			

Name	Description	Value	Meaning	Ref.
A1C_DP5	APEQ attack time	**b'0000** ~ b'1010	Attack time control (refer to APEQ attack time table in Addr 0x1A)	
C1C_DP5	APEQ release time	**b'000** ~ b'111	Release time control (refer to APEQ release time table in Addr 0x1A)	

Addr 0x1F: APEQ Filter Control 7 for APEQ6 (BQ12)

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_DP6			A1C_DP6			

Name	Description	Value	Meaning	Ref.
A1C_DP6	APEQ attack time	**b'0000** ~ b'1010	Attack time control (refer to APEQ attack time table in Addr 0x1A)	
C1C_DP6	APEQ release time	**b'000** ~ b'111	Release time control (refer to APEQ release time table in Addr 0x1A)	

Addr 0x20: DRC Control 0

Bit	7	6	5	4	3	2	1	0
Name	CPR_L	CTS_L						

Name	Description	Value	Meaning	Ref.
CTS_L	DRC threshold for Low band	**b'0000000** ~ b'1111111	-57 ~ 12dB unsigned 7-bit DRC threshold for 1 band mode. In 2 band mode, It will control the threshold of low band. Refer to DRC threshold table for threshold values.	
CPR_L	DRC enable for Low band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x21: DRC Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_L			A1C_L			

Name	Description	Value	Meaning	Ref.
A1C_L	DRC attack time (Low band)	b'0000 ~ b'1010	Attack time control for 1 band mode. In 2 band mode, it will control the attack time of low band. (refer to DRC attack time table below) default = **b'0001**	
C1C_L	DRC release time (Low band)	b'**000** ~ b'111	Release time control for 1 band mode. In 2 band mode, it will control the release time of low band. (refer to DRC release time table below)	

Value of Register	Attack time 6dB, fs = 96,000
0011	30msec
0010	15msec
0001	8msec
0000	4msec
0111	2msec
0110	1msec
0101	0.5msec
0100	0.25msec
1000	5msec
1001	6msec
1010	7msec

Table 13. DRC Attack Time Table

Value of Register	Release time 6dB, fs = 96,000
011	5.0sec
010	2.0sec
001	1.0sec
000	0.5sec
111	0.2sec
110	0.1sec
101	0.05sec
100	0.025sec

Table 14. DRC Release Time Table

Addr 0x22: DRC Control 2

Bit	7	6	5	4	3	2	1	0
Name	CPR_H	CTS_H						

Name	Description	Value	Meaning	Ref.
CTS_H	DRC threshold for High band	**b'0000000** ~ b'1111111	-57 ~ 12dB unsigned 7-bit DRC threshold for high band. It has effect only in 2 band mode. Refer to DRC threshold value table for threshold values.	
CPR_H	DRC enable for High band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x23: DRC Control 3

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_H			A1C_H			

Name	Description	Value	Meaning	Ref.
A1C_H	DRC attack time (High band)	b'0000 ~ b'1010	Attack time control for high band mode. It has effect only in 2 band mode. (See DRC attack time table in Addr 0x21) default = **b'0001**	
C1C_H	DRC release time (High band)	b'**000** ~ b'111	Release time control for high band mode. It has effect only in 2 band mode. (refer to DRC release time table in Addr 0x21)	

Reserved Address 0x24 ~ 0x25

Addr 0x26: DRC Control 6

Bit	7	6	5	4	3	2	1	0
Name	CPR_P	CTS_P						

Name	Description	Value	Meaning	Ref.
CTS_P	DRC threshold for Post band	**b'0000000** ~ b'1111111	-57 ~ 12dB unsigned 7-bit DRC threshold Refer to DRC threshold table.	
CPR_P	DRC enable for Post band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x27: DRC Control 7

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_P			A1C_P			

Name	Description	Value	Meaning	Ref.
A1C_P	DRC attack time (Post band)	b'0000 ~ b'1010	Attack time control (refer to DRC attack time table in Addr 0x21) default = **b'0001**	
C1C_P	DRC release time (Post band)	b'000 ~ b'111	Release time control (refer to DRC release time table in Addr 0x21) default = **b'100**	

Addr 0x28: DRC Control 8

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	DLL				

Name	Description	Value	Meaning	Ref.
DLL	Delay line length	b'00000~ **b'10100**	Delay line length. 0~20(decimal)	

Addr 0x29: DRC Control 9

Bit	7	6	5	4	3	2	1	0
Name	CCO	DTS1	DTS2	2BM	X	X	X	CAS

Name	Description	Value	Meaning	Ref.
CAS	Coupled All pass Structure enable	**b'0**	Enable coupled all pass structure	
		b'1	Disable coupled all pass structure	
2BM	2band mode enable	**b'0**	1 band DRC	
		b'1	2 band DRC	
DTS2	P-DRC type select	**b'0**	P-DRC new mode	
		b'1	P-DRC old mode	
DTS1	LH-DRC type select	**b'0**	LH-DRC new mode	
		b'1	LH-DRC old mode	
CCO	Clip control option	**b'0**	Clip off	
		b'1	Clip on	

Addr 0x2A: DRC Control 10

Bit	7	6	5	4	3	2	1	0
Name	CPR_S	CTS_S						

Name	Description	Value	Meaning	Ref.
CTS_S	DRC threshold for Sub band	b'0000000 ~ b'1111111	-57 ~ 12dB unsigned 7-bit DRC threshold for Sub band. It has effect only in 3 band mode. refer to DRC threshold table for threshold values. default= **b'1101010**	
CPR_S	DRC enable for Sub band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Addr 0x2B: DRC Control 11

Bit	7	6	5	4	3	2	1	0
Name	X	C1C_S			A1C_S			

Name	Description	Value	Meaning	Ref.
A1C_S	DRC attack time (Sub band)	b'0000 ~ b'1010	Attack time control for sub band mode. It has effect only in 3 band mode. (refer to DRC attack time table in Addr 0x21.) default = **b'0001**	
C1C_S	DRC release time (Sub band)	**b'000** ~ b'111	Release time control for sub band mode. It has effect only in 3 band mode. (refer to DRC release time table in Addr 0x21.)	

Addr 0x2C: DRC Control 12

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	DTS3	SBM

Name	Description	Value	Meaning	Ref.
SBM	Sub band mode enable	**b'0**	Sub band mode Disable	
		b'1	Sub band mode Enable	
DTS3	Sub DRC type select	**b'0**	Sub DRC new mode	
		b'1	Sub DRC old mode	

Reserved Address 0x2D

Addr 0x2E : Power Meter Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	PDPOS	X	X	PDCH	

Name	Description	Value	Meaning	Ref.
PDCH	Power meter Detect Channel	**b'00**	L+R (default)	
		b'01	L channel	
		b'10	R channel	
PDPOS	Power meter Detect Position	**b'0**	After volume (default)	
		b'1	Before volume (from digital input)	

Addr 0x2F : Power Meter (read only)

Bit	7	6	5	4	3	2	1	0
Name	Power meter							

Addr 0x30: Soft Volume Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	SVI	

Name	Description	Value	Meaning	Ref.
SVI	Soft volume change	**b'00**	Medium speed	
		b'01	High speed	
		b'10	Low speed	
		b'11	soft volume change disable	

Reserved Address 0x31 ~ 0x32

Addr 0x33 : Soft Mute Control

Bit	7	6	5	4	3	2	1	0
Name	SMH	X	X	X	X	X	SM2	SM1

Name	Description	Value	Meaning	Ref.
SMn	Softmute	b'0	increase for channel n	
		b'1	decrease for channel n	
SMH	Soft Mute Change speed	**b'0**	42/46 msec (at 96/88.2kHz)	
		b'1	Hard change	

Addr 0x34 : PWM Switching On/Off Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	POF2	POF1

Name	Description	Value	Meaning	Ref.
POFn	Switching output On/off control	b'0	Channel n PWM switching on	
		b'1	Channel n PWM switching off	

Addr 0x35 : PWM_MASK Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	SRD	FPMLD	PWMM	

Name	Description	Value	Meaning	Ref.
PWMM	PWM MASK register	**b'10**	PWM MASK output is low.	
		Otherwise	PWM MASK output is high.	
FPMLD	Permanent PWM_MASK Low disable flag	**b'0**	No effect	
		b'1	Reset the Auto PWM_MASK restore counter to 0	
SRD	FAULT disable	**b'0**	FAULT is effective for PROTECT	
		b'1	FAULT is ineffective for PROTECT	

Addr 0x36 : PWM_MASK Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	APM	POF

Name	Description	Value	Meaning	Ref.
POF	PWM off flag	**b'0**	Even if Auto PWM_MASK condition is met, the PWM output of all channels is not affected.	
		b'1	When Auto PWM_MASK condition is met, the PWM output of all channels goes to the defined state which is set by the PWM off state control registers (Addr 0x37 & 0x6F).	
APM	PWM_MASK flag	**b'0**	Even if Auto PWM_MASK condition is met, the PWM_MASK output of all channels is not affected.	
		b'1	When Auto PWM_MASK condition is met, the PWM_MASK output goes to Low state.	

Addr 0x37 : PWM_MASK Control 2

Bit	7	6	5	4	3	2	1	0
Name	X	VMSK2	VMSK1	VMSK0	X	PMSK2	PMSK1	PMSK0

Name	Description	Value	Meaning	Ref.
PMSKn	Masking bit of PWM off control	**b'0**	Mask bit indicating the validity of n-th bit of Addr 0x75 system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x75 system register is invalid. The n-th bit of Addr 0x75 is valid only when the n-th mask bit is one.	
		b'1		
VMSKn	Masking bit of PWM_MASK signal	**b'0**		
		b'1		

Addr 0x38 : PWM_MASK Control 3

Bit	7	6	5	4	3	2	1	0
Name	IRC		AVRCT			PHT		

Name	Description	Value	Meaning	Ref.
PHT	PWM_MASK Low Hold Time	b'000	0.5 msec Hold Time	
		b'001	1 msec Hold Time	
		b'010	2 msec Hold Time	
		b'011	4 msec Hold Time (Default)	
		b'100	8 msec Hold Time	
		b'101	16msec Hold Time	
AVRCT	Auto PWM_MASK Restore Counter Threshold	b'000	2	
		b'001	5 (Default)	
		b'010	10	
		b'011	15	
		b'100	20	
		b'101	25	
		b'110	30	
		b'111	Infinity	
IRC	Auto PWM_MASK Restore Interval Ratio Control	**b'00**	2 (Default)	
		b'01	4	

Addr 0x39 : PWM_MASK Control 4

Bit	7	6	5	4	3	2	1	0
Name	SHE	POE	X	X	X	HT2		

Name	Description	Value	Meaning	Ref.
HT2	Hold Time 2 apply start point (restore counter)	b'000	100 msec Hold Time	
		b'001	200 msec Hold Time	
		b'010	400 msec Hold Time	
		b'011	600 msec Hold Time (Default)	
		b'100	800 msec Hold Time	
		b'101	1 sec Hold Time	
		b'110	2 sec Hold Time	
		b'111	4 sec Hold Time	
POE	PWM off when Fault detected and PWM on when PWM_MASK recover	b'0	Disable	
		b'1	Enable (Default)	
SHE	Second Hold time Enable	**b'0**	Disable	
		b'1	Enable	

Addr 0x3A: Auto-Mute Control for CH1 & CH2

Bit	7	6	5	4	3	2	1	0
Name	X	EAMC	II		AT			

Name	Description	Value	Meaning	Ref.
AT	Auto-mute detection threshold	**b'0000 ~** b'1111	Unsigned integer between 0 and 15 Refer to Auto Mute detection threshold table for threshold values.	
II	Auto-mute response time	**b'00**	5 msec	
		b'01	50 msec	
		b'10	500 msec	
		b'11	2 sec	
EAMC	Effect of Auto-mute condition	**b'0**	Auto mute disable (No-Effect)	
		b'1	Stop PWM switching when auto-mute condition is met.	

Reserved Address 0x3B

Addr 0x3C: CH1&CH2 Prescaler Value Control

Bit	7	6	5	4	3	2	1	0
Name	PS12							

Name	Description	Value	Meaning	Ref.
PS12	Prescaler value	b'00000000 ~ b'11111111	default = **0x4C**	

Reserved Address 0x3D

Addr 0x3E: PWM Output Port Control for PWM Port 1A & 1B

Bit	7	6	5	4	3	2	1	0
Name	X	X	OPM1B			OPM1A		

Name	Description	Value	Meaning	Ref.
OPM1A	Select source channel for PWM output port 1A	**b'000**	PWM1A is connected to PWM port 1A	
		b'001	PWM1B is connected to PWM port 1A	
		b'010	PWM2A is connected to PWM port 1A	
		b'011	PWM2B is connected to PWM port 1A	
OPM1B	Select source channel for PWM output port 1B	b'000	PWM1A is connected to PWM port 1B	
		b'001	PWM1B is connected to PWM port 1B	
		b'010	PWM2A is connected to PWM port 1B	
		b'011	PWM2B is connected to PWM port 1B	

Addr 0x3F: PWM Output Port Control for PWM Port 2A & 2B

Bit	7	6	5	4	3	2	1	0
Name	X	X	OPM2B			OPM2A		

Name	Description	Value	Meaning	Ref.
OPM2A	Select source channel for PWM output port 2A	b'000	PWM1A is connected to PWM port 2A	
		b'001	PWM1B is connected to PWM port 2A	
		b'010	PWM2A is connected to PWM port 2A	
		b'011	PWM2B is connected to PWM port 2A	
OPM2B	Select source channel for PWM output port 2B	b'000	PWM1A is connected to PWM port 2B	
		b'001	PWM1B is connected to PWM port 2B	
		b'010	PWM2A is connected to PWM port 2B	
		b'011	PWM2B is connected to PWM port 2B	

Addr 0x40: NS Soft Mute Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	Time_Lim	Enable	CNT_THR			

Name	Description	Value	Meaning	Ref.
CNT_THR	Minimum counting value	b'0000~ b'1111	Minimum counting value of continuous zeros for forcing NS_OUT as 0. default = **b'0110**	
Enable	Enable NS soft mute	**b'0**	Disable	
		b'1	Enable	
Time_Lim	Time limit on finding continuous zeros	**b'0**	Time Limit = 200ms	
		b'1	Time Limit = 400ms	

Addr 0x41: Modulation Index & NS-Type Control

Bit	7	6	5	4	3	2	1	0
Name	X	M0		FB	X	NTF_Order	MD12	

Name	Description	Value	Meaning	Ref.
MD12	Modulation index control by Minimum pulse width for Ch 1&2	b'00	Minimum pulse width = 80 ns	
		b'01	Minimum pulse width = 60 ns	
		b'10	Minimum pulse width = 40 ns	
		b'11	Minimum pulse width = 20 ns	
NTF_Order	Select NTF Order	**b'0**	NTF Order = 4	
		b'1	NTF Order = 5	
FB	Feed Back on/off	b'0	NS Feed Back off	
		b'1	NS Feed Back on	
M0	Dither Position Selector	**b'00**	No left shift on dither value = Dither off	
		b'01	1bit left shift on dither value	
		b'10	2bit left shift on dither value	
		b'11	3bit left shift on dither value	

Addr 0x42: NS Feedback Limit

Bit	7	6	5	4	3	2	1	0
Name	X	FBMAX						

Name	Description	Value	Meaning	Ref.
FBMAX	Feedback on/off	b'0000000 ~b'1111111	Feedback limit, default = **0x04**	

Addr 0x43: Miscellaneous PWM Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	BHL	AHL	MD	

Name	Description	Value	Meaning	Ref.
MD	PWM output mode	**b'00**	AD mode with asynchronous signal pair	
		b'01	AD mode with synchronous signal pair	
		b'10	PWM D-BTL MODE (see 0x45)	
AHL	A-out state When switching off	**b'0**	Low	
		b'1	High	
BHL	B-out state when switching off	**b'0**	Low	
		b'1	High	

Addr 0x44: PWM D-BTL MODE Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	MLP						

Name	Description	Value	Meaning	Ref.
MLP	Minimum Linear pulse length	**b'0001110**	Unsigned 0~64	

Addr 0x45: PWM D-BTL MODE Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	NSS	

Name	Description	Value	Meaning	Ref.
NSS	NS Select	**b'00**	7bits NS (AD mode)	
		b'01	Reserved	
		b'10	8bits NS	
		b'11	New 8bits NS (D-BTL mode)	

Reserved Address 0x46 ~ 0x49

Addr 0x4A: Soft Start Control 0

Bit	7	6	5	4	3	2	1	0
Name	PSE	SRT						

Name	Description	Value	Meaning	Ref.
SRT	Step Repeat Time	b'000000 ~b'111111	Repeat time of each step (default = **b'0010000** – means repeat 17 times)	
PSE	PWM soft start Enable	b'0	Disable	
		b'1	Enable (only under AD mode)	

Addr 0x4B: Soft Start Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	MP_PD	

Name	Description	Value	Meaning	Ref.
MP_PD	Soft start minimum pulse of Power device	b'00	First pulse width = 20 ns	
		b'01	First pulse width = 40 ns	
		b'10	First pulse width = 60 ns	
		b'11	First pulse width = 80 ns	

Reserved Address 0x4C ~ 0x4F

Addr 0x50: AD DC Protection Control 0

Bit	7	6	5	4	3	2	1	0
Name	PDH				PDL			

Name	Description	Value	Meaning	Ref.
PDL	PWM Duty Low	b'0000	40%	
		b'0001	35%	
		b'0010	30%	
		b'0011	25%	
		b'0100	20%	
		b'0101	15%	
		b'0110	10%	
		b'0111	5%	
		b'1000	45%	
PDH	PWM Duty High	b'0000	60%	
		b'0001	65%	
		b'0010	70%	
		b'0011	75%	
		b'0100	80%	
		b'0101	85%	
		b'0110	90%	
		b'0111	95%	
		b'1000	55%	

Addr 0x51: D-BTL DC Protection Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	MLPA			

Name	Description	Value	Meaning	Ref.
MLPA	D-BTL Duty MLP	**b'0000**	5%	
		b'0001	10%	
		b'0010	15%	
		b'0011	20%	
		b'0100	25%	
		b'0101	30%	
		b'0110	35%	
		b'0111	40%	
		b'1000	45%	
		b'1001	50%	

Addr 0x52: DC Protection Control 2

Bit	7	6	5	4	3	2	1	0
Name	SRE	SRF	X	X	X	PFE	DFE	MFE

Name	Description	Value	Meaning	Ref.
MFE	PWM duty Error Enable	**b'0**	PWM duty Error Disable	
		b'1	PWM duty Error Enable	
DFE	DRC Coefficient Error Enable	**b'0**	MDRC Coefficient Error Disable	
		b'1	MDRC Coefficient Error Enable	
PFE	PBQ Coefficient Error Enable	**b'0**	PBQ Coefficient Error Disable	
		b'1	PBQ Coefficient Error Enable	
SRF	DC Soft Reset Flag	**b'0**		
		b'1	DC Soft Reset start in Modulation	
SRE	DC Soft Reset Enable	**b'0**	DC Soft Reset Flag Disable	
		b'1	DC Soft Reset Flag Enable	

Addr 0x53: DC Protection Control 3

Bit	7	6	5	4	3	2	1	0
Name	X	X	PCS3					

Name	Description	Value	Meaning	Ref.
PCS3	PBQ RX Check Sum(29:24)		default = **0x32**	

Addr 0x54: DC Protection Control 4

Bit	7	6	5	4	3	2	1	0
Name	PCS2							

Name	Description	Value	Meaning	Ref.
PCS2	PBQ RX Check Sum (23:16)		default = **0x00**	

Addr 0x55: DC Protection Control 5

Bit	7	6	5	4	3	2	1	0
Name	PCS1							

Name	Description	Value	Meaning	Ref.
PCS1	PBQ RX Check Sum (15:8)		default = **0x00**	

Addr 0x56: DC Protection Control 6

Bit	7	6	5	4	3	2	1	0
Name	PCS0							

Name	Description	Value	Meaning	Ref.
PCS0	PBQ RX Check Sum (7:0)		default = **0x00**	

Addr 0x57: DC Protection Control 7

Bit	7	6	5	4	3	2	1	0
Name	X	X	DCS3					

Name	Description	Value	Meaning	Ref.
DCS3	MDRC RX Check Sum (29:24)		default = **0x14**	

Addr 0x58: DC Protection Control 8

Bit	7	6	5	4	3	2	1	0
Name	DCS2							

Name	Description	Value	Meaning	Ref.
DCS2	MDRC RX Check Sum (23:16)		default = **0x8E**	

Addr 0x59: DC Protection Control 9

Bit	7	6	5	4	3	2	1	0
Name	DCS1							

Name	Description	Value	Meaning	Ref.
DCS1	MDRC RX Check Sum (15:8)		default = **0x9C**	

Addr 0x5A: DC Protection Control 10

Bit	7	6	5	4	3	2	1	0
Name	DCS0							

Name	Description	Value	Meaning	Ref.
DCS0	MDRC RX Check Sum (7:0)		default = **0x10**	

Addr 0x5B: DC Protection Control 11 (read only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	PEF	DEF	MEF

Name	Description	Value	Meaning	Ref.
MEF	PWM duty Error Flag	**b'0**		
		b'1	PWM duty Error	
DEF	DRC Coefficient Error Flag	**b'0**		
		b'1	MDRC Coefficient Error	
PEF	PEQ Coefficient Error Flag	**b'0**		
		b'1	PEQ Coefficient Error	

Addr 0x5C: Checksum Download Type Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	CDT

Name	Description	Value	Meaning	Ref.
CDT	Checksum download type	**b'0**	1byte * 4 (addr 0x53~0x56, 0x57~0x5A)	
		b'1	4byte (Coefficient mode)	

Addr 0x5D: Driver Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	KMS	SHDN

Name	Description	Value	Meaning	Ref.
SHDN	Shutdown	b'0	SHDN pin go to low	
		b'1	SHDN pin go to high	
KMS	PWM MASK output select	**b'0**	PWM_MASK0,1 pin <= PWM_MASK0,1	
		b'1	PWM_MASK0,1 pin <= SHDN	

Reserved Address 0x5E ~ 0x5F

Addr 0x60: SSRC Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	X	DCESW	X	FSFHM	FSFSM	X	X

Name	Description	Value	Meaning	Ref.
FSFSM	frequency stable effect on soft mute flag	**b'0**	no effect on soft mute flag	
		b'1	soft mute flag = 1 when unstable state	
FSFHM	frequency stable effect on hard mute flag	b'0	no effect on hard mute flag	
		b'1	hard mute flag = 1 when unstable state	
DCESW	DC Check Enable of SRC WCK	b'0	DC Check Disable in SRC WCK	
		b'1	DC Check Enable in SRC WCK	

Addr 0x61: SSRC Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	FVT			

Name	Description	Value	Meaning	Ref.
FVT	Frequency variation threshold	b'0000 ~ b'1111	threshold value for frequency stable check (unsigned integer) default : **b'0111**	

Addr 0x62: 3D Control 0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	TDO

Name	Description	Value	Meaning	Ref.
TDO	3D On/Off	**0**	3D off	
		1	3D on	

Addr 0x63: 3D Control 1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	M12			

Name	Description	Value	Meaning	Ref.
M12	3D Gain	b'0000 ~ b'1000	-0.5 (Minimum 3D effect) ~ -0.9 (Maximum 3D effect) default = **b'0101** (-0.75 with 0.05 step)	

Reserved Address 0x64 ~ 0x65

Addr 0x66: I2C Glitch Filter

Bit	7	6	5	4	3	2	1	0
Name	GFO	DUR						

Name	Description	Value	Meaning	Ref.
DUR	glitch width	b'0000000 ~ b'1111111	minimum pulse width = DUR + 20 ns reset default = 15 * 10 ns (DUR default = **b'0001111**)	
GFO	Glitch filter enable/disable	**b'0**	Glitch filter on	
		b'1	Bypass	

Reserved Address 0x67

Addr 0x68: PWM Phase Control

Bit	7	6	5	4	3	2	1	0
Name	PPC				PFC			

Name	Description	Value	Meaning	Ref.
PFC	PWM phase Fine Control	**b'0000** ~ b'1001	Range is 0°~14.94° with 1.66° step (In PWM768kHz, PFC range is 0~4 with 3.78° step)	In Single ended mode, fixed as PFC = b'0000, and PPC = b' 0110 (90°)
PPC	PWM Phase Control	b'0000 ~ b'1100	Range is 0°~180° with 15° step. default = **b'0110** (90°)	

Reserved Address 0x69 ~ 0x6D

Addr 0x6E Watch Dog Error System Status (read only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	IWK	IBK	WDE

Name	Description	Value	Meaning	Ref.
WDE	Watch Dog Ratio Error	b'0		
		b'1	Watch Dog Error	
IBK	IIS BCK Ratio Error	b'0		
		b'1	IIS BCK Ratio Error	
IWK	IIS WCK Ratio Error	b'0		
		b'1	IIS WCK Ratio Error	

Addr 0x6F: PWM_MASK Control 5

Bit	7	6	5	4	3	2	1	0
Name	X	VMSK2	VMSK1	VMSK0	X	PMSK2	PMSK1	PMSK0

Name	Description	Value	Meaning	Ref.
PMSKn	Masking bit of PWM off control	**b'0**	Mask bit indicating the validity of n-th bit of Addr 0x6E system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x6E system register is invalid. The n-th bit of Addr 0x6E is valid only when the n-th mask bit is one.	
		b'1		
VMSKn	Masking bit of PWM_MASK signal	**b'0**		
		b'1		

Addr 0x70: System Status Register (0x6E, 0x75) Holding Control 1

Bit	7	6	5	4	3	2	1	0
Name	HIWK	HIBK	HWDE	X	X	HMPW	HULCK	X

Name	Description	Value	Meaning	Ref.
HULCK	Enable bit of Holding the ULCK status	**b'0**	Update the new value without holding the ULCK status bit of 0x75	
		b'1	Hold the first different value	
HMPW	Enable bit of Holding the MPW status	**b'0**	Update the new value without holding the MPW status bit of 0x75	
		b'1	Hold the first different value	
HWDE	Enable bit of Holding the WDE status	**b'0**	Update the new value without holding the WDE status bit of 0x6E	
		b'1	Hold the first different value	
HIBK	Enable bit of Holding the IBK status	**b'0**	Update the new value without holding the IBK status bit of 0x6E	
		b'1	Hold the first different value	
HIWK	Enable bit of Holding the IWK status	**b'0**	Update the new value without holding the IWK status bit of 0x6E	
		b'1	Hold the first different value	

Addr 0x71: POP Control 0

Bit	7	6	5	4	3	2	1	0
Name	RST							

Name	Description	Value	Meaning	Ref.
RST	Release Time	**unsigned 0x10**	WDE becomes 0 if Watch Dog detects no error during RST*10msec after WDE has been occurred.	

Addr 0x72: POP Control 1

Bit	7	6	5	4	3	2	1	0
Name	ULM[15:8]							

Name	Description	Value	Meaning	Ref.
ULM		**unsigned 0x00**	Upper limit on ratio of BCK to CLK_FR_4	

Addr 0x73: POP Control 2

Bit	7	6	5	4	3	2	1	0
Name	ULM[7:0]							

Name	Description	Value	Meaning	Ref.
ULM	Upper Limit	**unsigned 0x20**	Upper limit on ratio of BCK to CLK_FR_4	

Addr 0x74: POP Control 3

Bit	7	6	5	4	3	2	1	0
Name	LLM[3:0]				0	0	0	WON

Name	Description	Value	Meaning	Ref.
LLM	Lower Limit	**unsigned b'1001**	Lower limit on ratio of BCK to CLK_FR_4	
WON	Watch-dog On	b'0	OFF	
		b'1	ON	

Addr 0x75: System Error Status (read only)

Bit	7	6	5	4	3	2	1	0
Name	FSI		PSB	PDM		MPW	ULCK	PPM

Name	Description	Value	Meaning	Ref.
PPM	Permanent PWMMASK Indication flag	b'0		
		b'1	Indicated that PWM_MASK is in Permanent LOW state	
ULCK	Sampled PLL Unlock error	b'0	PLL is locked state.	
		b'1	PLL is unlocked state.	
MPW	MCK/WCK Ratio error	b'0	Ratio is incorrect.	
		b'1	Ratio is correct.	
PDM	Power Die Monitor (Temperature, Current, Voltage, Protection Error)	b'00	Current protection error	
		b'01	Voltage protection error	
		b'10	Temperature protection error	
		b'11	Normal state	
PSB	PWM switching on/off State Bit	b'0	PWM switching off state	
		b'1	PWM switching on state	
FSI	Sampling Frequency Information	b'00	48 kHz (44.1kHz)	
		b'01	96 kHz	
		b'10	32 kHz	

Addr 0x76: Monitor

Bit	7	6	5	4	3	2	1	0
Name	Monitor2				Monitor1			

Name	Description	Value	Meaning	Ref.
Monitor 1	This output doesn't come through Power Device.	b'0000	Reserved	
		b'0001	Pwm1a=> Monitor 1 pin	
		b'0010	Pwm1b => Monitor 1 pin	
		b'0011	pwm2a => Monitor 1 pin	
		b'0100	Pwm2b => Monitor 1 pin	
		b'1111	Sdata out => Monitor 1 pin	
Monitor 2	This output doesn't come through Power Device.	b'0000	Reserved	
		b'0001	Pwm1a=> Monitor 2 pin	
		b'0010	Pwm1b => Monitor 2 pin	
		b'0011	pwm2a => Monitor 2 pin	
		b'0100	Pwm2b => Monitor 2 pin	
		b'1111	Sdata out => Monitor 2 pin	

Reserved Address 0x77 ~ 0x7B

Addr 0x7C: IIS Sdata_Out Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	OUT_SEL

Name	Description	Value	Meaning	Ref.
OUT_SEL	Select data for IIS OUT	**b'0**	Data after soft mute stage is selected	
		b'1	Data before EQ stage is selected	

Reserved Address 0x7D

Addr 0x7E: Bi-Quad Filter Coefficient Page

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	APEQ_P	X	CH2	CH1

Name	Description	Value	Meaning	Ref.
CH1	Coefficient write enable	**b'0**	Disable coefficient write for ch1	
		b'1	Enable coefficient write for ch1	
CH2	Coefficient write enable	**b'0**	Disable coefficient write for ch2	
		b'1	Enable coefficient write for ch2	
APEQ_P	Coefficient write enable for APEQ Parameters	**b'0**	Disable coefficient write for APEQ Para.	
		b'1	Enable coefficient write for APEQ Para.	

Note : When writing into BQ1~BQ6 coefficients, Should write for both ch1 and ch2 separately.
When writing into BQ7~BQ12 coefficients, Just write for ch1.
(BQ7~BQ12 coefficients are same for both CH1 and CH2)
When writing into APEQ Parameters, Just write for APEQ_P.

Coefficient Mode:

0x00 ~ 0x31: BQ1 ~BQ10
0x32 ~ 0x4F: QMF_BQ1 ~ 6
0x50 ~ 0x52: Loudness filter gain 1 ~ 3
0x53 ~ 0x57 : Reserved
0x58 : Power Meter Gain
0x59 : Reserved
0x5A : BQ Check sum
0x5B : DRC Check sum
0x5C ~ 0x65: BQ11 ~ BQ12

0x00 ~ 0x24: APEQ Parameters

B. Configuration Register Value Reference

Table 15. Master Volume

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
0xFF	0.0	0xD4	-21.5	0xA9	-43.0	0x7E	-64.5	0x53	-86.0	0x28	-107.5
0xFE	-0.5	0xD3	-22.0	0xA8	-43.5	0x7D	-65.0	0x52	-86.5	0x27	-108.0
0xFD	-1.0	0xD2	-22.5	0xA7	-44.0	0x7C	-65.5	0x51	-87.0	0x26	-108.5
0xFC	-1.5	0xD1	-23.0	0xA6	-44.5	0x7B	-66.0	0x50	-87.5	0x25	-109.0
0xFB	-2.0	0xD0	-23.5	0xA5	-45.0	0x7A	-66.5	0x4F	-88.0	0x24	-109.5
0xFA	-2.5	0xCF	-24.0	0xA4	-45.5	0x79	-67.0	0x4E	-88.5	0x23	-110.0
0xF9	-3.0	0xCE	-24.5	0xA3	-46.0	0x78	-67.5	0x4D	-89.0	0x22	-110.5
0xF8	-3.5	0xCD	-25.0	0xA2	-46.5	0x77	-68.0	0x4C	-89.5	0x21	-111.0
0xF7	-4.0	0xCC	-25.5	0xA1	-47.0	0x76	-68.5	0x4B	-90.0	0x20	-111.5
0xF6	-4.5	0xCB	-26.0	0xA0	-47.5	0x75	-69.0	0x4A	-90.5	0x1F	-112.0
0xF5	-5.0	0xCA	-26.5	0x9F	-48.0	0x74	-69.5	0x49	-91.0	0x1E	-112.5
0xF4	-5.5	0xC9	-27.0	0x9E	-48.5	0x73	-70.0	0x48	-91.5	0x1D	-113.0
0xF3	-6.0	0xC8	-27.5	0x9D	-49.0	0x72	-70.5	0x47	-92.0	0x1C	-113.5
0xF2	-6.5	0xC7	-28.0	0x9C	-49.5	0x71	-71.0	0x46	-92.5	0x1B	-114.0
0xF1	-7.0	0xC6	-28.5	0x9B	-50.0	0x70	-71.5	0x45	-93.0	0x1A	-114.5
0xF0	-7.5	0xC5	-29.0	0x9A	-50.5	0x6F	-72.0	0x44	-93.5	0x19	-115.0
0xEF	-8.0	0xC4	-29.5	0x99	-51.0	0x6E	-72.5	0x43	-94.0	0x18	-115.5
0xEE	-8.5	0xC3	-30.0	0x98	-51.5	0x6D	-73.0	0x42	-94.5	0x17	-116.0
0xED	-9.0	0xC2	-30.5	0x97	-52.0	0x6C	-73.5	0x41	-95.0	0x16	-116.5
0xEC	-9.5	0xC1	-31.0	0x96	-52.5	0x6B	-74.0	0x40	-95.5	0x15	-117.0
0xEB	-10.0	0xC0	-31.5	0x95	-53.0	0x6A	-74.5	0X3F	-96.0	0x14	-117.5
0xEA	-10.5	0xBF	-32.0	0x94	-53.5	0x69	-75.0	0X3E	-96.5	0x13	-118.0
0xE9	-11.0	0xBE	-32.5	0x93	-54.0	0x68	-75.5	0X3D	-97.0	0x12	-118.5
0xE8	-11.5	0xBD	-33.0	0x92	-54.5	0x67	-76.0	0X3C	-97.5	0x11	-119.0
0xE7	-12.0	0xBC	-33.5	0x91	-55.0	0x66	-76.5	0X3B	-98.0	0x10	-119.5
0xE6	-12.5	0xBB	-34.0	0x90	-55.5	0x65	-77.0	0X3A	-98.5	0x0F	-120.0
0xE5	-13.0	0xBA	-34.5	0x8F	-56.0	0x64	-77.5	0X39	-99.0	0x0E	-120.5
0xE4	-13.5	0xB9	-35.0	0x8E	-56.5	0x63	-78.0	0X38	-99.5	0x0D	-121.0
0xE3	-14.0	0xB8	-35.5	0x8D	-57.0	0x62	-78.5	0X37	-100.0	0x0C	-121.5
0xE2	-14.5	0xB7	-36.0	0x8C	-57.5	0x61	-79.0	0X36	-100.5	0x0B	-122.0
0xE1	-15.0	0xB6	-36.5	0x8B	-58.0	0x60	-79.5	0X35	-101.0	0x0A	-122.5
0xE0	-15.5	0xB5	-37.0	0x8A	-58.5	0x5F	-80.0	0X34	-101.5	0x09	-123.0
0xDF	-16.0	0xB4	-37.5	0x89	-59.0	0x5E	-80.5	0X33	-102.0	0x08	-123.5
0xDE	-16.5	0xB3	-38.0	0x88	-59.5	0x5D	-81.0	0X32	-102.5	0x07	-124.0
0xDD	-17.0	0xB2	-38.5	0x87	-60.0	0x5C	-81.5	0X31	-103.0	0x06	-124.5
0xDC	-17.5	0xB1	-39.0	0x86	-60.5	0x5B	-82.0	0X30	-103.5	0x05	-125.0
0xDB	-18.0	0xB0	-39.5	0x85	-61.0	0x5A	-82.5	0x2F	-104.0	0x04	-125.5
0xDA	-18.5	0xAF	-40.0	0x84	-61.5	0x59	-83.0	0x2E	-104.5	0x03	NA
0xD9	-19.0	0xAE	-40.5	0x83	-62.0	0x58	-83.5	0x2D	-105.0	0x02	NA
0xD8	-19.5	0xAD	-41.0	0x82	-62.5	0x57	-84.0	0x2C	-105.5	0x01	NA
0xD7	-20.0	0xAC	-41.5	0x81	-63.0	0x56	-84.5	0x2B	-106.0	0x00	NA
0xD6	-20.5	0xAB	-42.0	0x80	-63.5	0x55	-85.0	0x2A	-106.5		
0xD5	-21.0	0xAA	-42.5	0x7F	-64.0	0x54	-85.5	0x29	-107.0		

Table 16. Channel Volume

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
0xFF	48.0	0xD4	26.5	0xA9	5.0	0x7E	-16.5	0x53	-38.0	0x28	-59.5
0xFE	47.5	0xD3	26.0	0xA8	4.5	0x7D	-17.0	0x52	-38.5	0x27	-60.0
0xFD	47.0	0xD2	25.5	0xA7	4.0	0x7C	-17.5	0x51	-39.0	0x26	-60.5
0xFC	46.5	0xD1	25.0	0xA6	3.5	0x7B	-18.0	0x50	-39.5	0x25	-61.0
0xFB	46.0	0xD0	24.5	0xA5	3.0	0x7A	-18.5	0x4F	-40.0	0x24	-61.5
0xFA	45.5	0xCF	24.0	0xA4	2.5	0x79	-19.0	0x4E	-40.5	0x23	-62.0
0xF9	45.0	0xCE	23.5	0xA3	2.0	0x78	-19.5	0x4D	-41.0	0x22	-62.5
0xF8	44.5	0xCD	23.0	0xA2	1.5	0x77	-20.0	0x4C	-41.5	0x21	-63.0
0xF7	44.0	0xCC	22.5	0xA1	1.0	0x76	-20.5	0x4B	-42.0	0x20	-63.5
0xF6	43.5	0xCB	22.0	0xA0	0.5	0x75	-21.0	0x4A	-42.5	0x1F	-64.0
0xF5	43.0	0xCA	21.5	0x9F	0.0	0x74	-21.5	0x49	-43.0	0x1E	-64.5
0xF4	42.5	0xC9	21.0	0x9E	-0.5	0x73	-22.0	0x48	-43.5	0x1D	-65.0
0xF3	42.0	0xC8	20.5	0x9D	-1.0	0x72	-22.5	0x47	-44.0	0x1C	-65.5
0xF2	41.5	0xC7	20.0	0x9C	-1.5	0x71	-23.0	0x46	-44.5	0x1B	-66.0
0xF1	41.0	0xC6	19.5	0x9B	-2.0	0x70	-23.5	0x45	-45.0	0x1A	-66.5
0xF0	40.5	0xC5	19.0	0x9A	-2.5	0x6F	-24.0	0x44	-45.5	0x19	-67.0
0xEF	40.0	0xC4	18.5	0x99	-3.0	0x6E	-24.5	0x43	-46.0	0x18	-67.5
0xEE	39.5	0xC3	18.0	0x98	-3.5	0x6D	-25.0	0x42	-46.5	0x17	-68.0
0xED	39.0	0xC2	17.5	0x97	-4.0	0x6C	-25.5	0x41	-47.0	0x16	-68.5
0xEC	38.5	0xC1	17.0	0x96	-4.5	0x6B	-26.0	0x40	-47.5	0x15	-69.0
0xEB	38.0	0xC0	16.5	0x95	-5.0	0x6A	-26.5	0X3F	-48.0	0x14	-69.5
0xEA	37.5	0xBF	16.0	0x94	-5.5	0x69	-27.0	0X3E	-48.5	0x13	-70.0
0xE9	37.0	0xBE	15.5	0x93	-6.0	0x68	-27.5	0X3D	-49.0	0x12	-70.5
0xE8	36.5	0xBD	15.0	0x92	-6.5	0x67	-28.0	0X3C	-49.5	0x11	-71.0
0xE7	36.0	0xBC	14.5	0x91	-7.0	0x66	-28.5	0X3B	-50.0	0x10	-71.5
0xE6	35.5	0xBB	14.0	0x90	-7.5	0x65	-29.0	0X3A	-50.5	0x0F	-72.0
0xE5	35.0	0xBA	13.5	0x8F	-8.0	0x64	-29.5	0X39	-51.0	0x0E	-72.5
0xE4	34.5	0xB9	13.0	0x8E	-8.5	0x63	-30.0	0X38	-51.5	0x0D	-73.0
0xE3	34.0	0xB8	12.5	0x8D	-9.0	0x62	-30.5	0X37	-52.0	0x0C	-73.5
0xE2	33.5	0xB7	12.0	0x8C	-9.5	0x61	-31.0	0X36	-52.5	0x0B	-74.0
0xE1	33.0	0xB6	11.5	0x8B	-10.0	0x60	-31.5	0X35	-53.0	0x0A	-74.5
0xE0	32.5	0xB5	11.0	0x8A	-10.5	0x5F	-32.0	0X34	-53.5	0x09	-75.0
0xDF	32.0	0xB4	10.5	0x89	-11.0	0x5E	-32.5	0X33	-54.0	0x08	-75.5
0xDE	31.5	0xB3	10.0	0x88	-11.5	0x5D	-33.0	0X32	-54.5	0x07	-76.0
0xDD	31.0	0xB2	9.5	0x87	-12.0	0x5C	-33.5	0X31	-55.0	0x06	-76.5
0xDC	30.5	0xB1	9.0	0x86	-12.5	0x5B	-34.0	0X30	-55.5	0x05	-77.0
0xDB	30.0	0xB0	8.5	0x85	-13.0	0x5A	-34.5	0x2F	-56.0	0x04	-77.5
0xDA	29.5	0xAF	8.0	0x84	-13.5	0x59	-35.0	0x2E	-56.5	0x03	-78.0
0xD9	29.0	0xAE	7.5	0x83	-14.0	0x58	-35.5	0x2D	-57.0	0x02	-78.5
0xD8	28.5	0xAD	7.0	0x82	-14.5	0x57	-36.0	0x2C	-57.5	0x01	-79.0
0xD7	28.0	0xAC	6.5	0x81	-15.0	0x56	-36.5	0x2B	-58.0	0x00	-295.0
0xD6	27.5	0xAB	6.0	0x80	-15.5	0x55	-37.0	0x2A	-58.5		
0xD5	27.0	0xAA	5.5	0x7F	-16.0	0x54	-37.5	0x29	-59.0		

Table 17. Mixer Gain & Polarity

Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB
7E	+	18	7D	-	18	3E	+	-4	3D	-	-4
7C	+	17	7B	-	17	3C	+	-4.5	3B	-	-4.5
7A	+	16	79	-	16	3A	+	-5	39	-	-5
78	+	15	77	-	15	38	+	-5.5	37	-	-5.5
76	+	14	75	-	14	36	+	-6	35	-	-6
74	+	13	73	-	13	34	+	-7	33	-	-7
72	+	12	71	-	12	32	+	-8	31	-	-8
70	+	11	6F	-	11	30	+	-9	2F	-	-9
6E	+	10	6D	-	10	2E	+	-10	2D	-	-10
6C	+	9	6B	-	9	2C	+	-11	2B	-	-11
6A	+	8	69	-	8	2A	+	-12	29	-	-12
68	+	7	67	-	7	28	+	-13	27	-	-13
66	+	6	65	-	6	26	+	-14	25	-	-14
64	+	5.5	63	-	5.5	24	+	-15	23	-	-15
62	+	5	61	-	5	22	+	-16	21	-	-16
60	+	4.5	5F	-	4.5	20	+	-17	1F	-	-17
5E	+	4	5D	-	4	1E	+	-18	1D	-	-18
5C	+	3.5	5B	-	3.5	1C	+	-19	1B	-	-19
5A	+	3	59	-	3	1A	+	-20	19	-	-20
58	+	2.5	57	-	2.5	18	+	-21	17	-	-21
56	+	2	55	-	2	16	+	-22	15	-	-22
54	+	1.5	53	-	1.5	14	+	-23	13	-	-23
52	+	1	51	-	1	12	+	-24	11	-	-24
50	+	0.5	4F	-	0.5	10	+	-25	0F	-	-25
4E	+	0	4D	-	0	0E	+	-26	0D	-	-26
4C	+	-0.5	4B	-	-0.5	0C	+	-27	0B	-	-27
4A	+	-1	49	-	-1	0A	+	-28	09	-	-28
48	+	-1.5	47	-	-1.5	08	+	-29	07	-	-29
46	+	-2	45	-	-2	06	+	-30	05	-	-30
44	+	-2.5	43	-	-2.5	04	+	-31	03	-	-31
42	+	-3	41	-	-3	02	+	-32	01	-	-32
40	+	-3.5	3F	-	-3.5	00	+	-150			

Table 18. Dynamic Range Control Threshold

dB	Value	dB	Value	dB	Value	dB	Value
-57	FF	-5.5	DF	-2.3	BF	0.9	9F
-54	FE	-5.4	DE	-2.2	BE	1	9E
-51	FD	-5.3	DD	-2.1	BD	1.25	9D
-48	FC	-5.2	DC	-2	BC	1.5	9C
-45	FB	-5.1	DB	-1.9	BB	1.75	9B
-42	FA	-5	DA	-1.8	BA	2	9A
-39	F9	-4.9	D9	-1.7	B9	2.25	99
-36	F8	-4.8	D8	-1.6	B8	2.5	98
-33	F7	-4.7	D7	-1.5	B7	2.75	97
-30	F6	-4.6	D6	-1.4	B6	3	96
-27	F5	-4.5	D5	-1.3	B5	3.25	95
-24	F4	-4.4	D4	-1.2	B4	3.5	94
-21	F3	-4.3	D3	-1.1	B3	3.75	93
-18	F2	-4.2	D2	-1	B2	4	92
-15	F1	-4.1	D1	-0.9	B1	4.25	91
-12	F0	-4	D0	-0.8	B0	4.5	90
-11.5	EF	-3.9	CF	-0.7	AF	4.75	8F
-11	EE	-3.8	CE	-0.6	AE	5	8E
-10.5	ED	-3.7	CD	-0.5	AD	5.5	8D
-10	EC	-3.6	CC	-0.4	AC	6	8C
-9.5	EB	-3.5	CB	-0.3	AB	6.5	8B
-9	EA	-3.4	CA	-0.2	AA	7	8A
-8.5	E9	-3.3	C9	-0.1	A9	7.5	89
-8	E8	-3.2	C8	0	A8	8	88
-7.5	E7	-3.1	C7	0.1	A7	8.5	87
-7	E6	-3	C6	0.2	A6	9	86
-6.5	E5	-2.9	C5	0.3	A5	9.5	85
-6	E4	-2.8	C4	0.4	A4	10	84
-5.9	E3	-2.7	C3	0.5	A3	10.5	83
-5.8	E2	-2.6	C2	0.6	A2	11	82
-5.7	E1	-2.5	C1	0.7	A1	11.5	81
-5.6	E0	-2.4	C0	0.8	A0	12	80

※ CPR bit(MSB) = 1

Table 19. Auto Mute Detection Threshold Table

Name	Description	Value	dB
AT	Auto-mute Detection threshold	0000	-126
		0001	-120
		0010	-114
		0011	-108
		0100	-102
		0101	-96
		0110	-90
		0111	-84
		1000	-78
		1001	-72
		1010	-66
		1011	-60
		1100	-54
		1101	-48
		1110	-42
		1111	**Auto-mute**

※ Do not use value 1111.

Table 20. Power Meter Reading Table

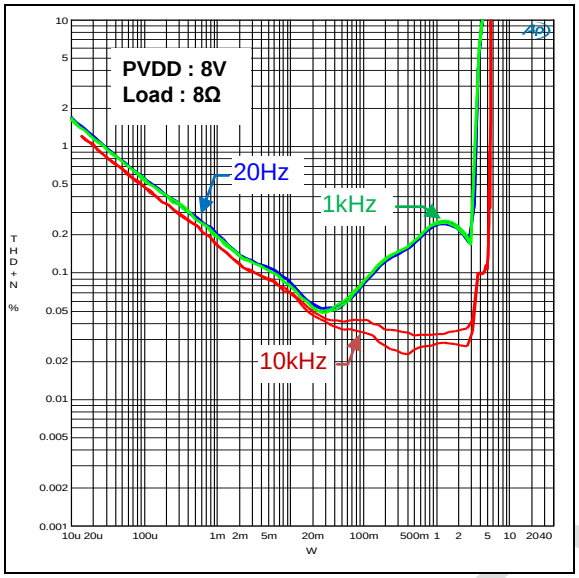
addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB	addr 0x54 (Decimal)	addr 0x54 (Hex)	dB
0	0x00	-0.0	64	0x40	-32.0	128	0x80	-64.0	192	0xC0	-96.0
1	0x01	-0.5	65	0x41	-32.5	129	0x81	-64.5	193	0xC1	-96.5
2	0x02	-1.0	66	0x42	-33.0	130	0x82	-65.0	194	0xC2	-97.0
3	0x03	-1.5	67	0x43	-33.5	131	0x83	-65.5	195	0xC3	-97.5
4	0x04	-2.0	68	0x44	-34.0	132	0x84	-66.0	196	0xC4	-98.0
5	0x05	-2.5	69	0x45	-34.5	133	0x85	-66.5	197	0xC5	-98.5
6	0x06	-3.0	70	0x46	-35.0	134	0x86	-67.0	198	0xC6	-99.0
7	0x07	-3.5	71	0x47	-35.5	135	0x87	-67.5	199	0xC7	-99.5
8	0x08	-4.0	72	0x48	-36.0	136	0x88	-68.0	200	0xC8	-100.0
9	0x09	-4.5	73	0x49	-36.5	137	0x89	-68.5	201	0xC9	-100.5
10	0x0A	-5.0	74	0x4A	-37.0	138	0x8A	-69.0	202	0xCA	-101.0
11	0x0B	-5.5	75	0x4B	-37.5	139	0x8B	-69.5	203	0xCB	-101.5
12	0x0C	-6.0	76	0x4C	-38.0	140	0x8C	-70.0	204	0xCC	-102.0
13	0x0D	-6.5	77	0x4D	-38.5	141	0x8D	-70.5	205	0xCD	-102.5
14	0x0E	-7.0	78	0x4E	-39.0	142	0x8E	-71.0	206	0xCE	-103.0
15	0x0F	-7.5	79	0x4F	-39.5	143	0x8F	-71.5	207	0xCF	-103.5
16	0x10	-8.0	80	0x50	-40.0	144	0x90	-72.0	208	0xD0	-104.0
17	0x11	-8.5	81	0x51	-40.5	145	0x91	-72.5	209	0xD1	-104.5
18	0x12	-9.0	82	0x52	-41.0	146	0x92	-73.0	210	0xD2	-105.0
19	0x13	-9.5	83	0x53	-41.5	147	0x93	-73.5	211	0xD3	-105.5
20	0x14	-10.0	84	0x54	-42.0	148	0x94	-74.0	212	0xD4	-106.0
21	0x15	-10.5	85	0x55	-42.5	149	0x95	-74.5	213	0xD5	-106.5
22	0x16	-11.0	86	0x56	-43.0	150	0x96	-75.0	214	0xD6	-107.0
23	0x17	-11.5	87	0x57	-43.5	151	0x97	-75.5	215	0xD7	-107.5
24	0x18	-12.0	88	0x58	-44.0	152	0x98	-76.0	216	0xD8	-108.0
25	0x19	-12.5	89	0x59	-44.5	153	0x99	-76.5	217	0xD9	-108.5
26	0x1A	-13.0	90	0x5A	-45.0	154	0x9A	-77.0	218	0xDA	-109.0
27	0x1B	-13.5	91	0x5B	-45.5	155	0x9B	-77.5	219	0xDB	-109.5
28	0x1C	-14.0	92	0x5C	-46.0	156	0x9C	-78.0	220	0xDC	-110.0
29	0x1D	-14.5	93	0x5D	-46.5	157	0x9D	-78.5	221	0xDD	-110.5
30	0x1E	-15.0	94	0x5E	-47.0	158	0x9E	-79.0	222	0xDE	-111.0
31	0x1F	-15.5	95	0x5F	-47.5	159	0x9F	-79.5	223	0xDF	-111.5
32	0x20	-16.0	96	0x60	-48.0	160	0xA0	-80.0	224	0xE0	-112.0
33	0x21	-16.5	97	0x61	-48.5	161	0xA1	-80.5	225	0xE1	-112.5
34	0x22	-17.0	98	0x62	-49.0	162	0xA2	-81.0	226	0xE2	-113.0
35	0x23	-17.5	99	0x63	-49.5	163	0xA3	-81.5	227	0xE3	-113.5
36	0x24	-18.0	100	0x64	-50.0	164	0xA4	-82.0	228	0xE4	-114.0
37	0x25	-18.5	101	0x65	-50.5	165	0xA5	-82.5	229	0xE5	-114.5
38	0x26	-19.0	102	0x66	-51.0	166	0xA6	-83.0	230	0xE6	-115.0
39	0x27	-19.5	103	0x67	-51.5	167	0xA7	-83.5	231	0xE7	-115.5
40	0x28	-20.0	104	0x68	-52.0	168	0xA8	-84.0	232	0xE8	-116.0
41	0x29	-20.5	105	0x69	-52.5	169	0xA9	-84.5	233	0xE9	-116.5
42	0x2A	-21.0	106	0x6A	-53.0	170	0xAA	-85.0	234	0xEA	-117.0
43	0x2B	-21.5	107	0x6B	-53.5	171	0xAB	-85.5	235	0xEB	-117.5
44	0x2C	-22.0	108	0x6C	-54.0	172	0xAC	-86.0	236	0xEC	-118.0
45	0x2D	-22.5	109	0x6D	-54.5	173	0xAD	-86.5	237	0xED	-118.5
46	0x2E	-23.0	110	0x6E	-55.0	174	0xAE	-87.0	238	0xEE	-119.0
47	0x2F	-23.5	111	0x6F	-55.5	175	0xAF	-87.5	239	0xEF	-119.5
48	0x30	-24.0	112	0x70	-56.0	176	0xB0	-88.0	240	0xF0	-120.0
49	0x31	-24.5	113	0x71	-56.5	177	0xB1	-88.5	241	0xF1	-120.5
50	0x32	-25.0	114	0x72	-57.0	178	0xB2	-89.0	242	0xF2	-121.0
51	0x33	-25.5	115	0x73	-57.5	179	0xB3	-89.5	243	0xF3	-121.5
52	0x34	-26.0	116	0x74	-58.0	180	0xB4	-90.0	244	0xF4	-122.0
53	0x35	-26.5	117	0x75	-58.5	181	0xB5	-90.5	245	0xF5	-122.5
54	0x36	-27.0	118	0x76	-59.0	182	0xB6	-91.0	246	0xF6	-123.0
55	0x37	-27.5	119	0x77	-59.5	183	0xB7	-91.5	247	0xF7	-123.5
56	0x38	-28.0	120	0x78	-60.0	184	0xB8	-92.0	248	0xF8	-124.0
57	0x39	-28.5	121	0x79	-60.5	185	0xB9	-92.5	249	0xF9	-124.5
58	0x3A	-29.0	122	0x7A	-61.0	186	0xBA	-93.0	250	0xFA	-125.0
59	0x3B	-29.5	123	0x7B	-61.5	187	0xBB	-93.5	251	0xFB	-125.5
60	0x3C	-30.0	124	0x7C	-62.0	188	0xBC	-94.0	252	0xFC	-126.0
61	0x3D	-30.5	125	0x7D	-62.5	189	0xBD	-94.5	253	0xFD	-126.5
62	0x3E	-31.0	126	0x7E	-63.0	190	0xBE	-95.0	254	0xFE	-127.0
63	0x3F	-31.5	127	0x7F	-63.5	191	0xBF	-95.5	255	0xFF	-127.5 under

※ Output 8bit value : (-dB * 2), n dB = output 8bit *0.5

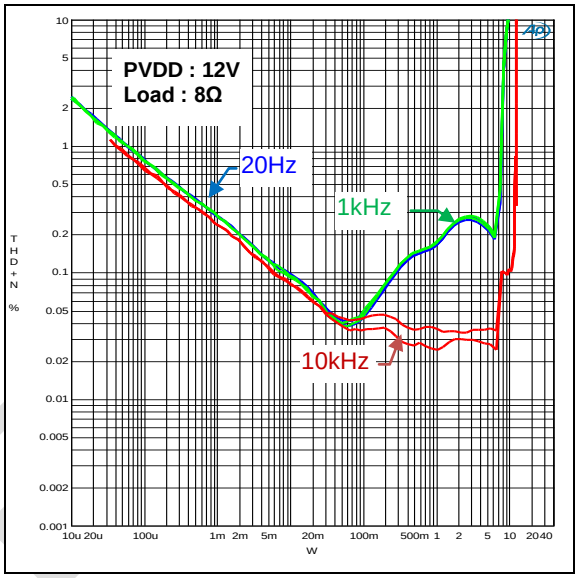
C. Typical Characteristics Graph

Total Harmonic Distortion + Noise vs. Power, BTL D-BTL Mode Configuration, 8Ω

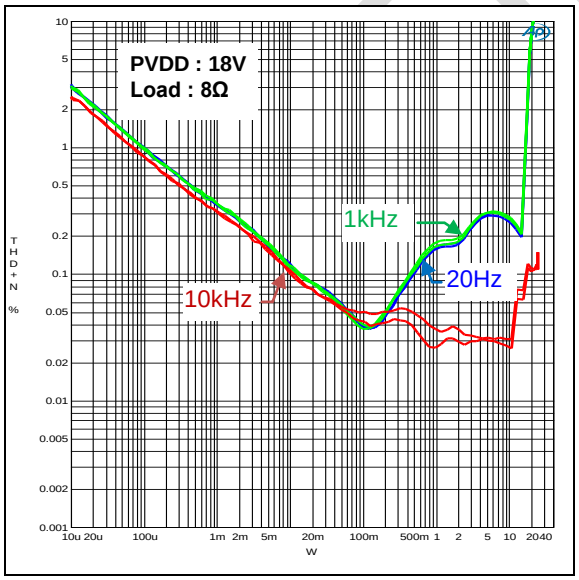
THD+N vs. Power



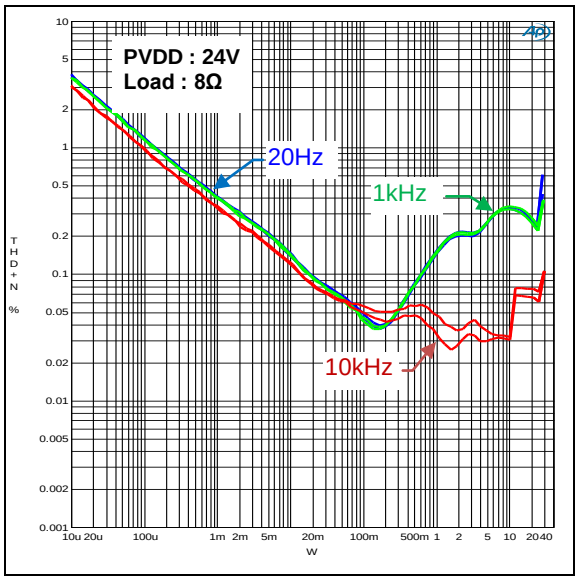
THD+N vs. Power



THD+N vs. Power

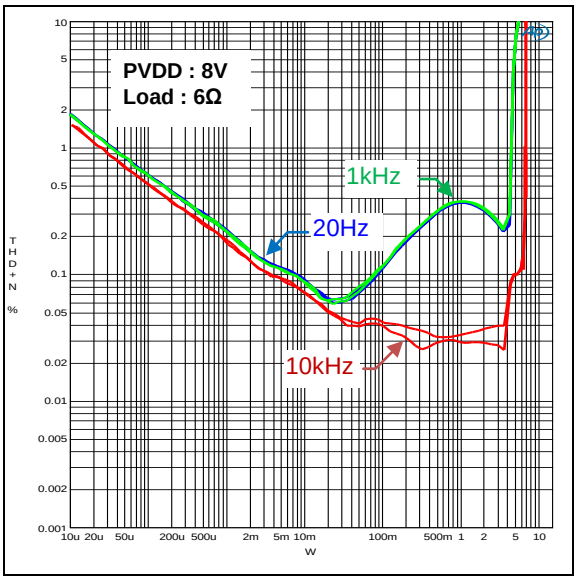


THD+N vs. Power

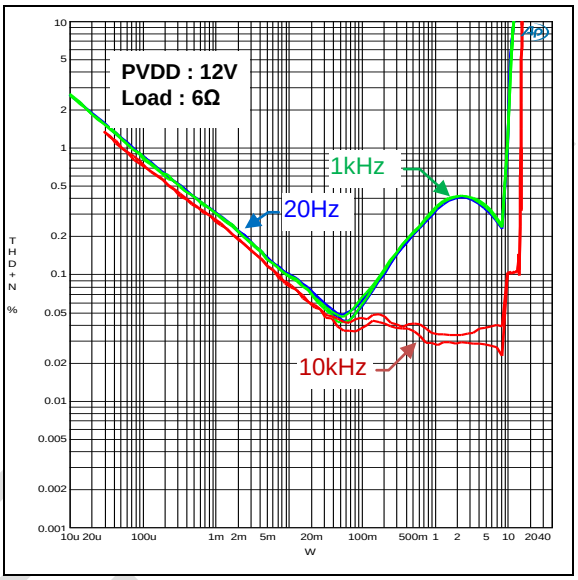


Total Harmonic Distortion + Noise vs. Power, BTL D-BTL Mode Configuration, 6Ω

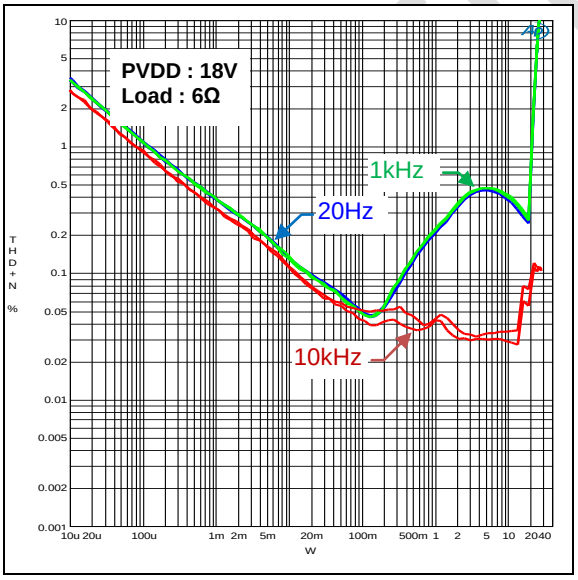
THD+N vs. Power



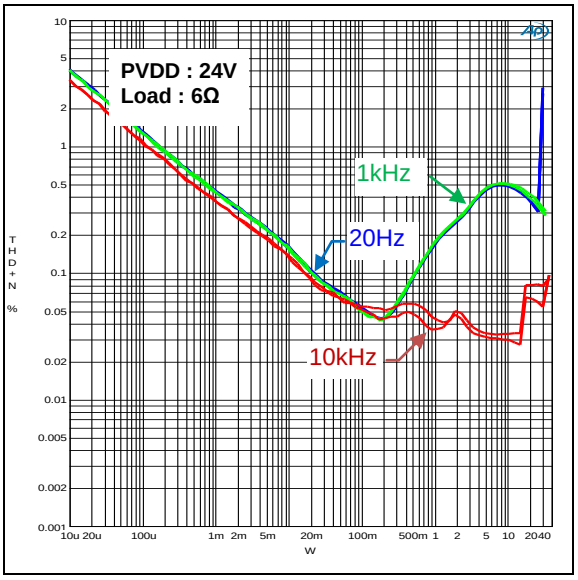
THD+N vs. Power



THD+N vs. Power

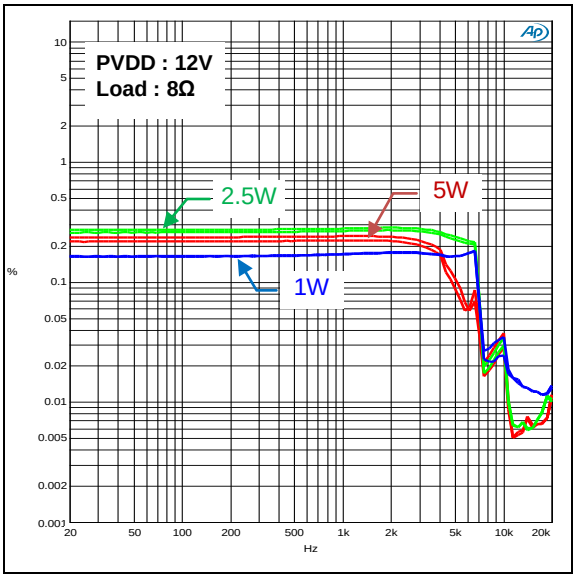


THD+N vs. Power

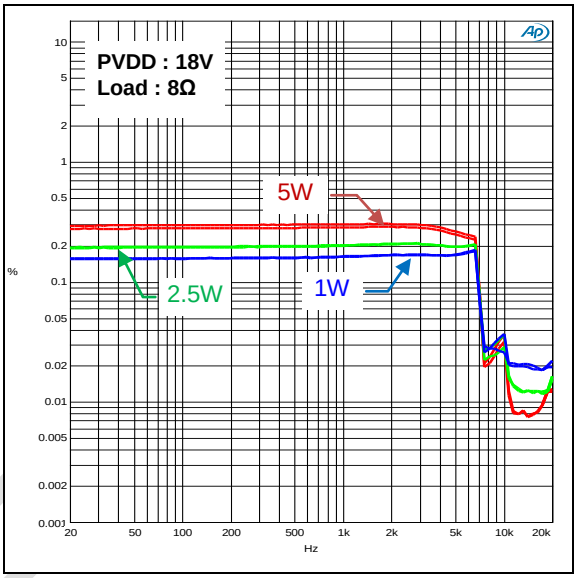


Total Harmonic Distortion + Noise vs. Frequency, BTL D-BTL Mode Configuration, 8Ω

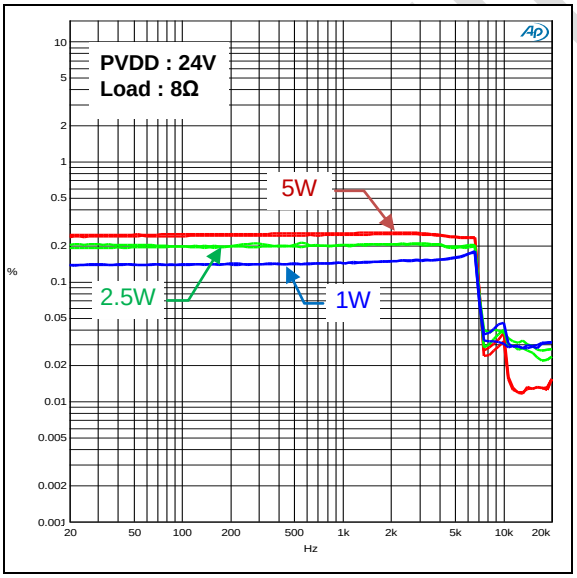
THD+N vs. Frequency



THD+N vs. Frequency

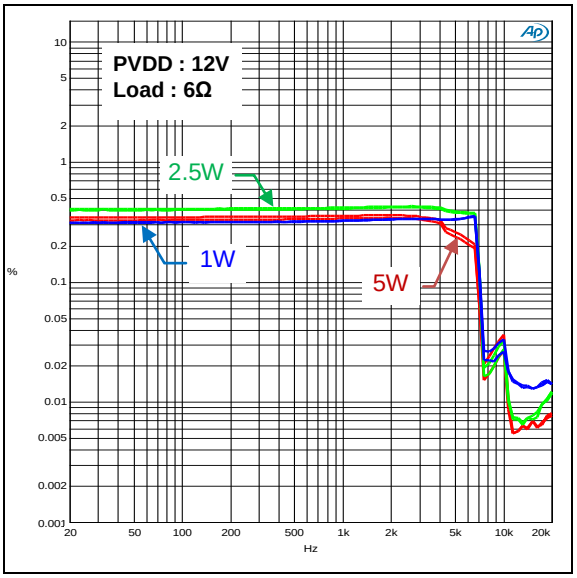


THD+N vs. Frequency

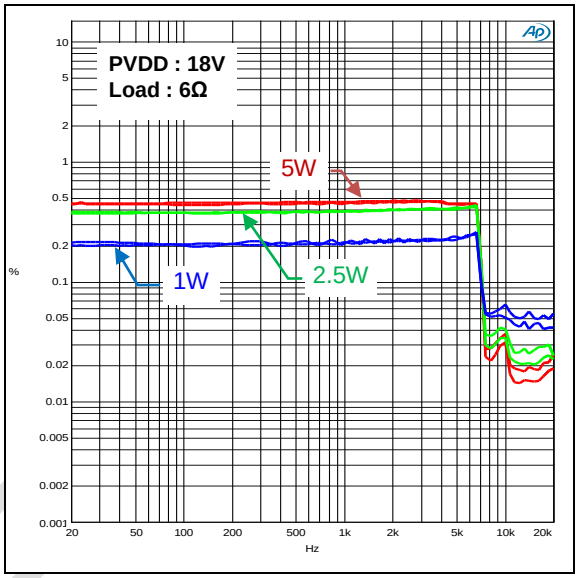


Total Harmonic Distortion + Noise vs. Frequency, BTL D-BTL Mode Configuration, 6Ω

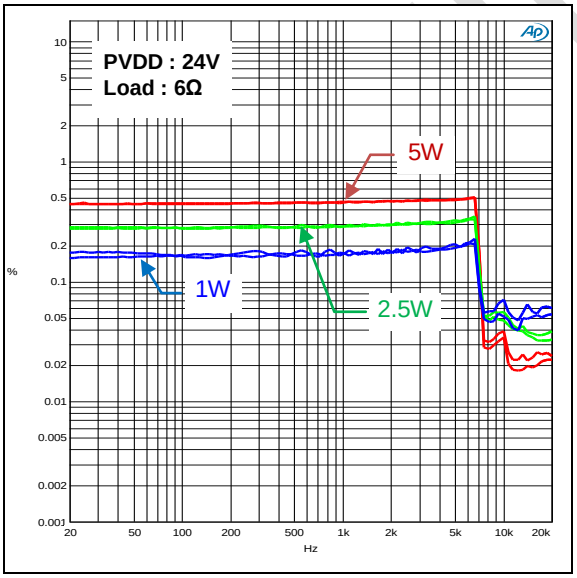
THD+N vs. Frequency



THD+N vs. Frequency

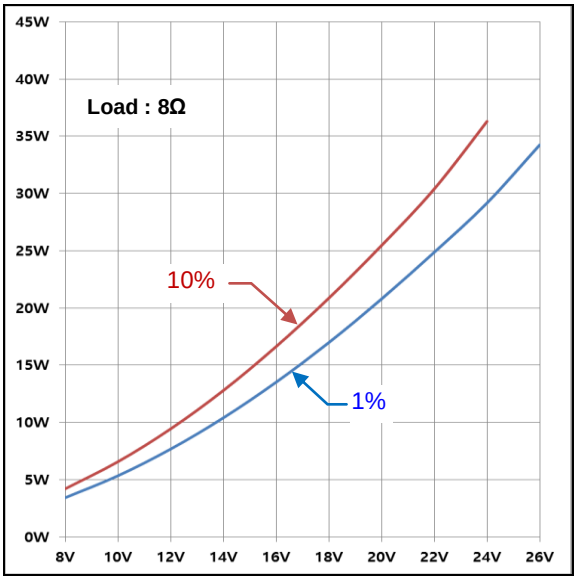


THD+N vs. Frequency

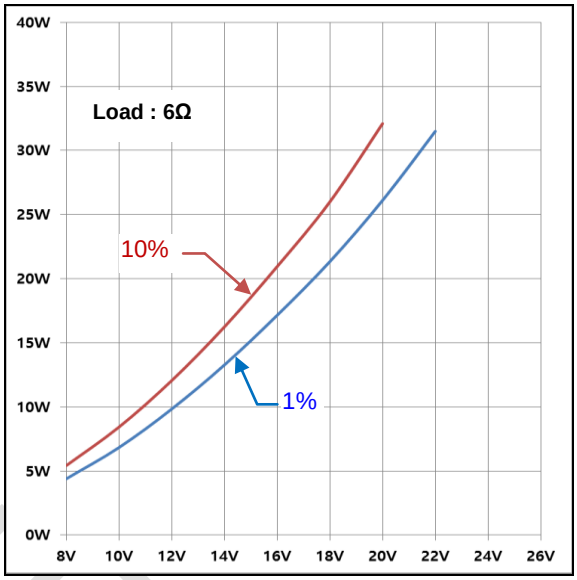


Output Power vs. PVDD, BTL D-BTL Mode Configuration

Output Power vs. PVDD

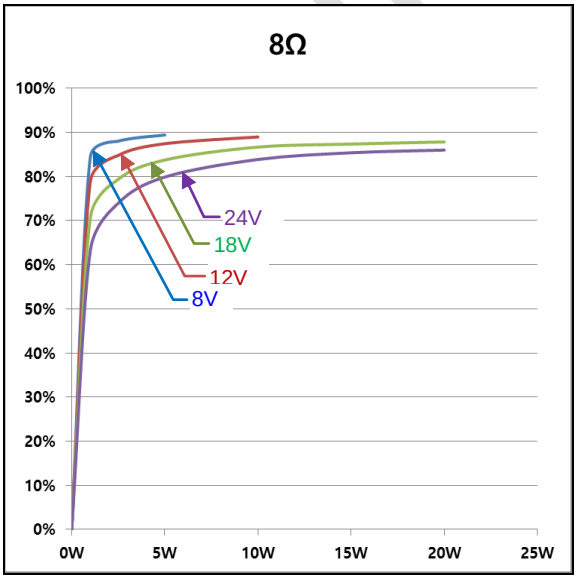


Output Power vs. PVDD

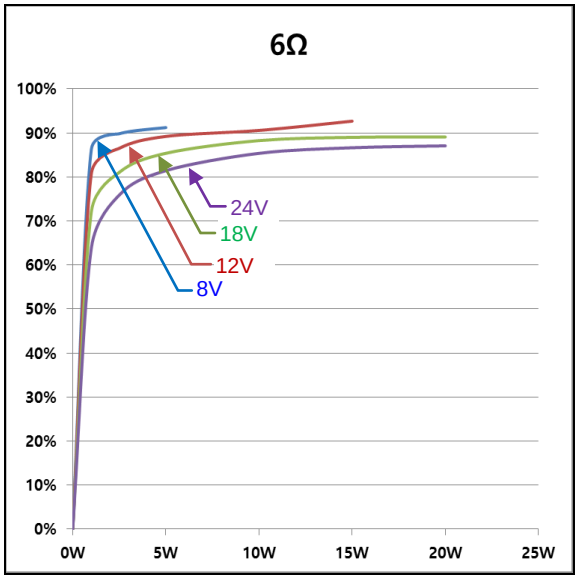


Efficiency vs. Total Power, BTL D-BTL Mode Configuration

Efficiency vs. Output Power

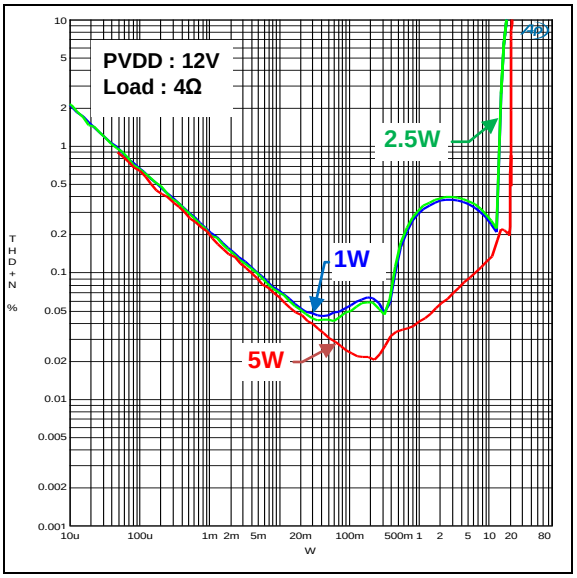


Efficiency vs. Output Power

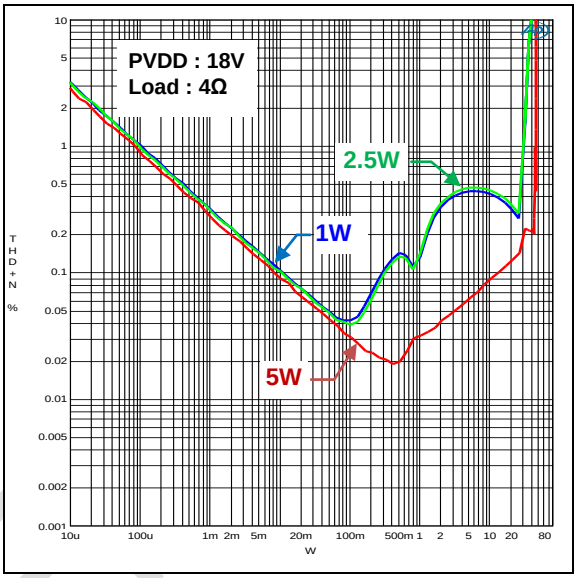


Total Harmonic Distortion + Noise vs. Power, PBTL AD Mode Configuration, 4Ω

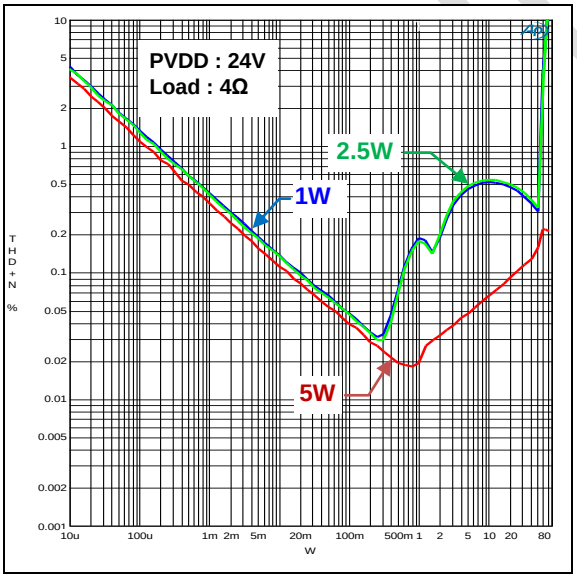
THD+N vs. Power



THD+N vs. Power

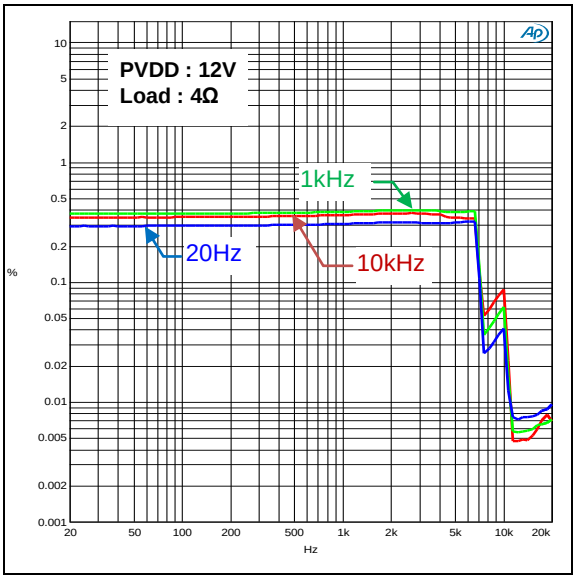


THD+N vs. Power

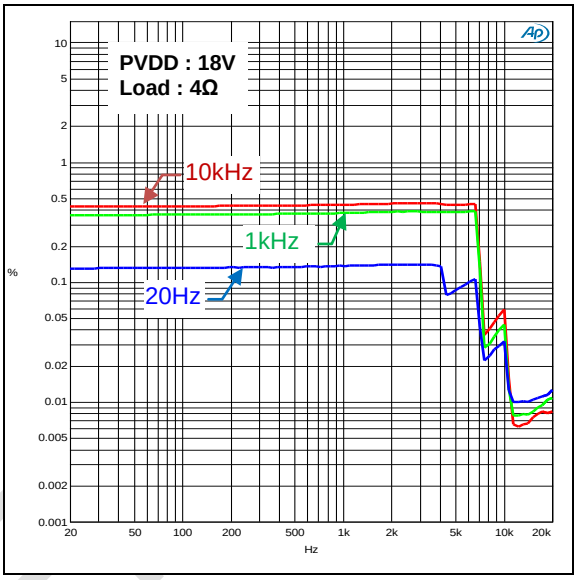


Total Harmonic Distortion + Noise vs. Frequency, PBTL AD Mode Configuration, 4Ω

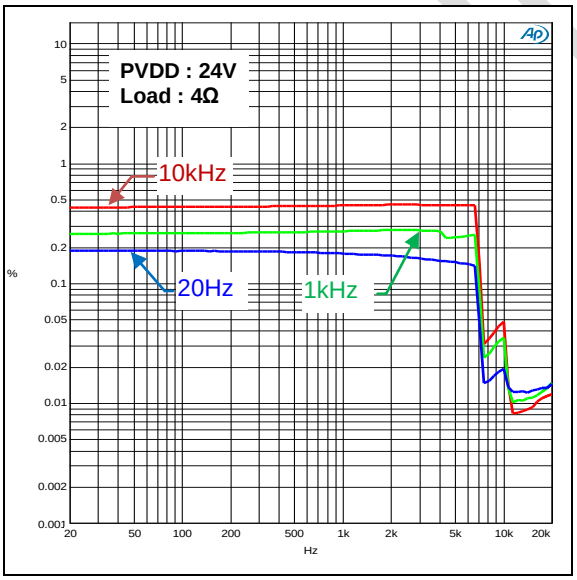
THD+N vs. Frequency



THD+N vs. Frequency

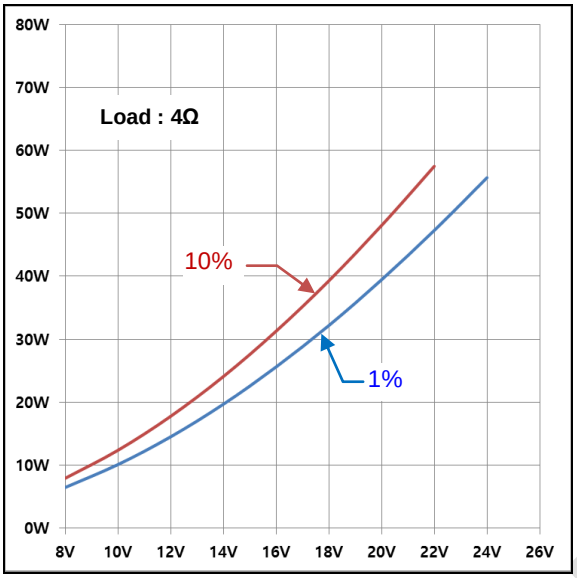


THD+N vs. Frequency



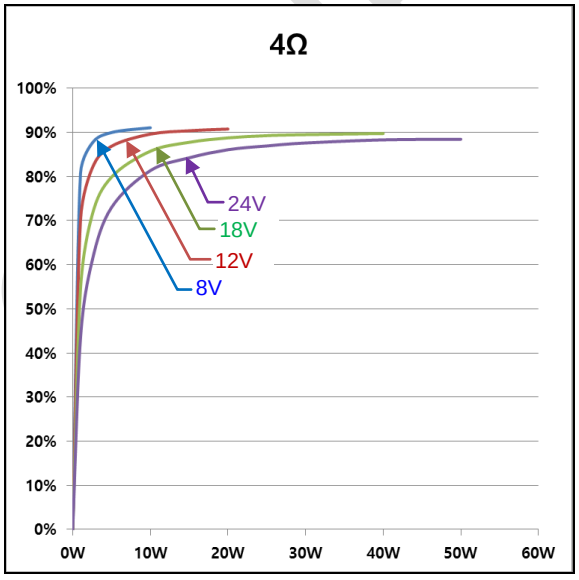
Output Power vs. PVDD, PBTL AD Mode Configuration

Output Power vs. PVDD

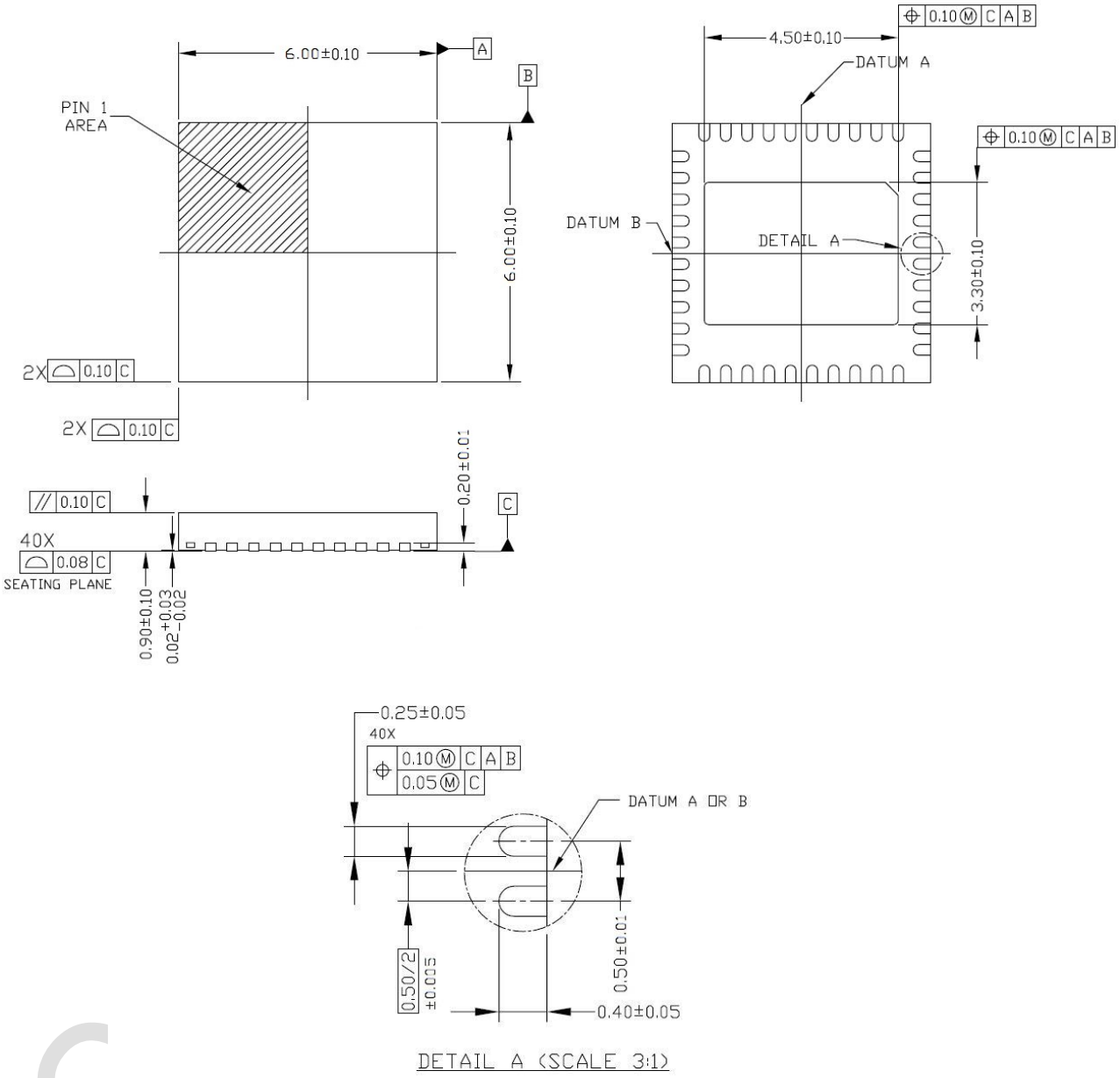


Efficiency vs. Total Power, PBTL AD Mode Configuration

Efficiency vs. Output Power



D. Outline and Mechanical Data



DETAIL A (SCALE 3:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

3. Reliability Report

RELIABILITY REPORT

	Relability Test Report	Written by	Checked by	Approved by
			-	

Purpose	The Qualification of a new product.				
Product Name	NTP8824	Date	2017.11.1	Written by	Y.T.KIM
Test Period	2017.7.10 ~ 2017.10.31	Q'ty	483ea	Result	Pass

1. Product Information

Product Name	NTP8824	**Package Type**	40QFN-EP
Assembly Site	ASEKr, ANST, AMKOR	**FT Site**	GMTEST

2. Power Die Information

Fab Site	SKHynix	**EDS Site**	PFJ, OKINS, TRT

3. Modulator Information

Fab Site	DBH	**EDS Site**	GMTEST

4. Reliability Test Items and Condition

TEST ITEM	TEST CONDITION	S/S	Result	JEDEC
HTOL	VDD : 3.6V , PVDD : 28V , Temperature : 125℃±5℃ 1008hrs	77*3	Pass	JESD22-A108
HTS	Temperature : 150℃, 504hrs	25*3	Pass	JESD22-A103
Pre-condition. + U-HAST	Temperature : 130 ℃ / 85 % R.H 96hrs Precon. [L3]30℃/60%RH, 192Hrs Reflow 3Cycles	25*3	Pass	JESD22-A118
Pre-condition + TC	Temperature= -65℃(15MIN)/150℃(15MIN) 500cycles Precon. [L3]30℃/60%RH, 192Hrs Reflow 3Cycles	25*3	Pass	JESD22-A104
ESD	HBM(±2000V), MM(±200V), CDM(±500V), Latchup (V-Test, I-Test)	27	Pass	JESD22-A114F JESD22-A115C JESD22-C101E JESD78D

5. Conclusion

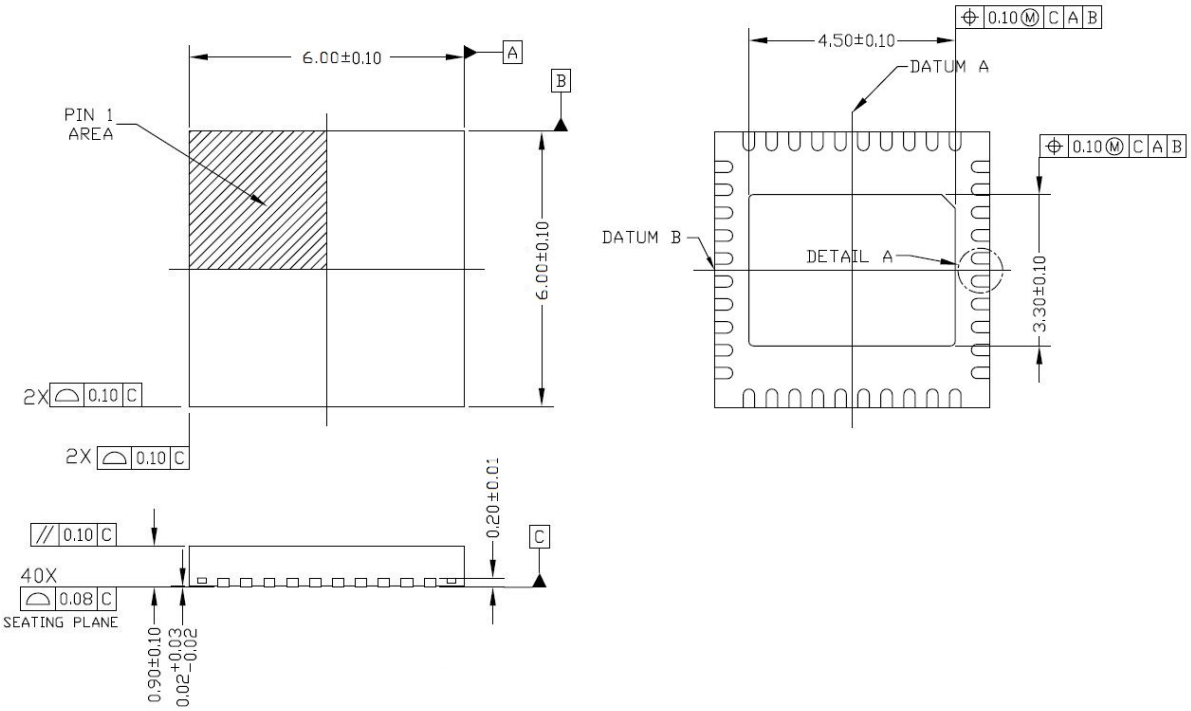
4.1 HTOL/HTS/U-HAST/TC Test Pass

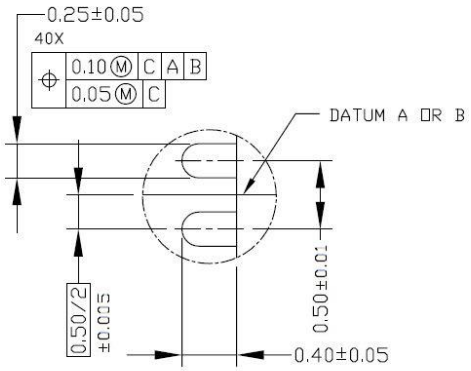
4.2 NTP8824 Qualified

4. Package Dimension

Package Dimension

NOTES) UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN MILLIMETERS (Unit : mm)





DETAIL A (SCALE 3:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

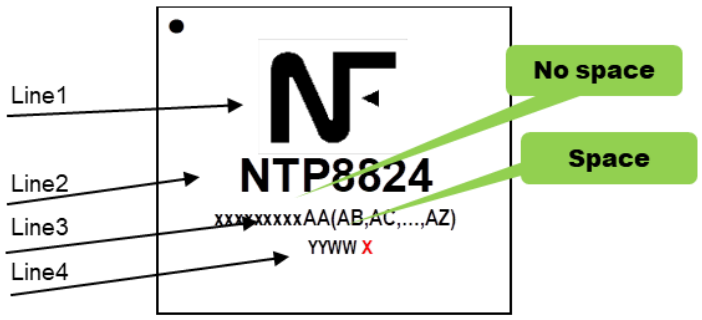
5. Marking Information

Marking Information

MARKING INSTRUCTION

Customer	**NeoFidelity, Inc.**	**Instruction Number**	**NTP8824 Rev.01**
Device Code	**NTP8824**	**Design Center**	**ASE/ AMKOR/ ANST**
PKG Type	**MLF SAW 40LD 6X6**	**Issue**	**2017. 04. 24.**

PACKAGE TOP SIDE



COMMENT

- Line1 : LOGO
- Line2 : Device Name
- Line3 : Main Die Lot Number **AA (AB, AC,...,ZZ)**
- Line4 : Package weekly code and Ass'y site

CHARACTER FONT

TOP SIDE	Line 1	Line 2	Line 3	Line 4	Line 5	Space 1	Space 2	Space 3	Blank 1	Blank 2
TYPE	LOGO	ROMANSIMPLEX (STD.)or Customer requirements								
SIZE (mm)										

BOTTOM SIDE	Line 1	Line 2	Line 3	Line 4	Line 5	Space 1	Space 2	Space 3	Blank 1	Blank 2
TYPE										
SIZE (mm)										

6. Process Control Plan

PROCESS CONTROL PLAN

Control Plan 控制计划	Document NO.： S-CP-QC-001 Revision： BH Page 1 of 24

☐ GENERATION ☒ REVISION ☐ ABSOLUTION ☐ QUALIFICATION ☒ MASS PRODUCTION

	NAME	DEPT		NAME	DEPT
ORIGINATOR	Yin J	A-PE	REVIEWER	Zhong Y	SCM
DOC.CENTER	Fan J	DCC	REVIEWER		
REVIEWER	Xu G	A-PE	REVIEWER		
REVIEWER	Wang CX	LOG	REVIEWER		
REVIEWER	Lu ZF	QRA	APPROVAL	Wu JZ	VP
REVIEWER	Zhang LC	QC	APPROVAL	Luo WL	VP
REVIEWER	Wang JX	ATC	APPROVAL		

EFFECTIVE DATE：2016.08.31

CONTROLLED STAMP

DESCRIPTION OF CONTROL PLAN (FROM/TO)

Add:

Update defect item, add Failure mode about NSOP/Missing wire, NSOL/Lifted stitch, Sagging wire, Broken wire, No bonding

REV.	EFFECTIVE DATE	REVISION HISTORY	PREPARED
AA	2006.9.25	New Release	Song CL
AB	2007.01.10	Update Wafer Incoming Inspection	Zhang QX
AC	2007.01.30	Update the sampling Freq of laser depth	Zhang QX
AD	2007.04.17	Wafer IQA 从 CP 中分离，单独写	He D
AE	2007.04.23	Change PMC Temperature profile Rep, Pb free bake Temperature profile Rep, MARKING Temperature profile Rep	He D
AF	2007.05.21	Add some control items in Back grinding, Molding, Plating and Marking process.	He D
AG	2007.09.05	Add U.V. Release process (Option) after wafer saw. Add die coating process (Option) after QA 3'rd gate Add S-TCM-DA-PL-01 in DA visual inspection log No Add 3 units/every package conversion in sampling plan size of DA wet epoxy thickness Update Plating process responsibility of chemical bath concentrate on analysis Update MD Visual Criteria, measuring method Update MK auto pad marking, measuring method Update EVI visual inspection measuring method	Liu D
AH	2007.10.22	Total update	Liu D
AI	2007.11.23	Update Spec No	Liu D

AJ	2007.12.11	Update L/F characteristic and Spec No Update WB wire loop height Sampling plan size Update WB BAR Sampling plan size/Frep and log sheet Update Mold misalign/mismatch Criteria Plating From 3x magnifier To Min 3X magnifier Update Marking Visual Check/marking (QA) Sampling plan size/Frep and log sheet Update Marking Visual Check/marking (prod) log sheet Update Marking laser depth Sampling plan size/Frep and log sheet Update parameter monitor sampling plan size/Frep and log sheet	Liu D
AK	2008.01.21	Update C-SAM monitor plan	Liu D
AL	2008.02.24	Update document no from S-PES-WS-005 to S-PEW-WS-008 Update D/A adhesive analyse method From T-card To Log Sheet Update D/A adhesive log no From T-card To S-PDW-GEN-034-15 Update Visual monitor (RTI) measuring method From High power scope (50x-200x) To Low/High power scope (10x-40x/50x-200x) Deleted Visual monitor (RTI) OCAP No Update D/A adhesive batch age Sampling Plan Size/Frep From 1X/Before lot start or epoxy change To 1X/ Epoxy receiving or issue Update pick up tool Sampling Plan Size/Frep. Update D/A adhesive shift life and type Sampling Plan Size/Frep From 1X/Before lot start or epoxy change To 1X/ beginning of shift or epoxy change Update Packing Q'ty/material/marking Spec No From S-PES-IPK-003/004/007/008/010/012/013 To S-PES-IPK-003 S-PES-IPK-017 Update Molding Compound Aging Sampling plan size /Frep From 1X/Before lot start or 1X/Replenish compound To 1X/beginning of shift or 1X/compound change Update Dedambar punch Life time measuring method From Machine Auto counter To Record Update Plating Parameter Monitor Sampling Plan Size/Frep From 1X/set up/machine To 1x/PKG type/machine/shift or 1X/chemical solution make up Update Plating Chemical bath concentration analysis analyse method（lead）From Log Sheet To Out source Update Plating Chemical bath concentration Log No （lead） From Log Sheet To NA Update Plating Chemical bath concentration OCAP No Chemical） From S-TCM-PT-PO-06 To S-TCM-PT-PO-09 Update Packing Visual gate Spec No From S-QAW-QC-028 S-PES-IPK-003/004/007/008/010/012/013 To	Liu D

		S-QAW-IPK-001 S-PES-IPK-017	
		Update Dedambar punch log sheet From NA To S-EES-TF-004-2	
AM	2008.04.30	Update Back Grind visual inspection log No	Liu D
		Update Back Grind thickness log No	
		Update water saw parameter sampling plan size/frep	
		Update INSP. QA 2nd Gate Visual inspection analyse method	
		Update INSP. QA 2nd Gate Visual inspection log no	
AN	2008.07.03	Total update	Liu D
AO	2008.10.06	DA: QC Visual inspection from 1 strip. 1X / machine / shift to 1 strip. 2x / machine / shift Add log sheet S-TCM-DA-OCPL-05	Liu D
		Die tilt from 5 units. 1X/machine/shift to 5 units. 1X/machine/day	
		Wet epoxy thickness from 5 units. 1X/machine/shift to 5 units. 1X/machine/day	
		DA cure: QC Parameter from 1 reading/oven/shift to 1 reading/oven/day	
		Epoxy void from 5 units. 1X/machine/shift to 5 units. 1X/machine/day	
		Die shear strength from 5 units. 1X/machine/shift to 5 units. 1X/machine/day	
		WB: QC Parameter from 1x/ machine/shift to NA	
		BAR from 5 balls 1x/ machine/shift to NA	
		MD: QC Misalign/Mismatch from 2 units,1X/machine/shift to 2 units,1X/machine/shift （manual mold） 2 units,1X/machine/day （auto mold）	
		QC Parameter from 1X/machine/shift to 1X/machine/day	
		Mold Temperature from 10 piont/1X/machine/shift to 10 piont/1X/machine/shift（manual mold） 10 piont/1X/machine/day（auto mold）	
		QC Oven temperature from 1X/oven/shift to 1 reading/oven/day	
		Trim: QC: Visual inspection from 2strip, 4x/machine/shift to 2strip, 3x/machine/shift	
		Machine Deflash: QC Parameter Monitor from 1X/machine/shift to NA	
		PT: QC Rinse Effectiveness from 1X/machine/shift to 1X/machine/day	
		MK: QC: Visual Check/marking Deleted log sheet S-TCM-MK-QCPL-05	

		Form: QC Visual inspection from 45units, 4x/machine/shift or 1X/buy off to 1 stroke(min 5 unites), 4x/machine/shift or 1X/buy off	
AP	2009.03.10	Combine C line control plan, document name from S-line Control Plan to Control plan	Liu D
		Back grind process parameter delete spec No S-QAW-WS-001	
		Back grind process parameter log No from S-TCM-BG-QCPL-02 to S-TCM-BG-PL-01; S-TCM-BG-PL-02; S-TCM-BG-PL-03	
		Back grind process parameter Rep from QA to PROD	
AQ	2009.05.14	1. Add Tape laminate control step in back grinding process	Liu D
		2. Add Tape remove control step in back grinding process	
		3. Delete MD visual inspection log no S-TCM-MD-QCPL-02	
		4. Delete MD internal defect log no S-TCM-MD-QCPL-02	
		5. Delete MD misalign/mismatch log no S-TCM-MD-QCPL-04	
		6. Delete MD mold temperature log no S-TCM-MD-QCPL-02	
AR	2009.09.30	WB pad cratering test from 1unit, 1x/machine/week to 1unit, 1x/machine/2 weeks	Liu D
		Mold parameter from 1x/machine/day ; 1x/buy off to 1x/buy off	
AS	2010.04.09	Wafer saw Visual inspection spec No. change to S-PES-WS-003	Yu Q
		Wafer saw Visual inspection High power scope check frequency change to first wafer. 1x / buy-off	
		INSP. QA 2nd Gate Log No. change to S-PES-WS-007-1	
		Split control of D/A adhesive shelf life and type	
		DA pick up tool check frequency change to Refer to SPEC	
		Delete WB loop height monitor measure	
		Change EVI Visual inspection spec No. and frequency	
		Packing Q'ty/material/marking log No. change to MES	

		Change marking spec No. ,Log No. and OCAP No.	
		Delete Marker ink and Marking ink dry	
		Change molding Log no	
		Change Dejunk/Dedambar die Auto trim system Log no.	
		Change Plating Log no	
		Change Manual form; Auto shuttle system; Auto progressive system Log no	
		Add Note	
AT	2011.03.08	Plating visual frequency change from 5 strips /lot to 9 strips /lot Plating Solderability test delete 1X/chemical solution make up Test 3units Plating delete Rinse Effectiveness (contamination Test) 1X/chemical solution make up 3strips	Yu Q
		Change marking “visual / marking” spec and lead depth check frequency from 3 points/2 units/1X /machine/day to 3 points/2 units/1X /machine/shift Update “visual / marking” OCAP No.	
		Update Dedambar punch life time control	
		Update Packing sample plan: Add Plug: ALL	
		Change “Bar code printer(Optional)” sequence to after wafer saw and update the Log No to S-TCM-WS-PL-03 Change Post D/A cure epoxy void check frequency from 5units.1x/machine/day(Except DAD-90B2) to 5units.1x/oven/day(Except DAD-90B2/insulating glue) Change Post D/A cure die shear check frequency from 5units. 1x/machine/day to 5units. 1x/oven/day	
		Delete the S-QAW-EVI-001 from EVI visual inspection spec No.	
AU	2013.03.14	1. Add Note: ☆ means special characteristics. 2.Change EVI spec no. from S-PEW-EVI-002 to S-PEW-EVI-001 Change EVI spec no. from S-PES-EVI-002/003/004/005/009/010 to S-PES-EVI-002/003/004/005/009/010/011 3. For dedamabar/dejunk and form/singulation process: Change Size/Freq from 3X/lot to Assy lot size≥10000,6X/lot & Assy lot size<10000, 3X/lot &	Yu Q

		Assy lot size≤315, 1x/lot; Log No from S-TCM-TF-PL-01 to T-Card. 4. For mold process: Visual Inspection form 1shot,2X/machine/shift 1X/Buy off To 1shot,1X/machine/shift 1X/Buy off 1X/ mold die cleaning Internal Defect form 1shot,2X/machine/shift 1X/Buy off To 1shot,1X/machine/shift 1X/Buy off 5. For Machine Deflash and Plating Visual Monitor Log no from S-TCM-PT-PL-01 to T-CARD For Plating Parameter Monitor Log no from S-TCM-PT-PL-14/S-TCM-PT-PL-15/S-TCM-PT-PL-17 to T-CARD 6. Update Wire bonding Visual inspection log no from S-TCM-WB-PL-01 to S-TCM-WB-PL-07 and buy off system 7. Update Wire bonding Visual monitor (RTI) log no from S-TCM-WB-PL-02 to T-card 8. Delete Wire bonding Machine parameter monitor 9. Update wire bonding Bond pull strength log no from S-TCM-WB-PL-01 to MES 10.Update wire bonding Ball shear strength log no from S-TCM-WB-PL-01 to MES 11.Update wire bonding Wire loop height log no from S-TCM-WB-PL-01 to MES 12.Delete wire bonding Pad cratering test 13.Update wire bonding BAR(Ball diameter/ball thickness) log no from S-TCM-WB-PL-01 to MES 14.Update wire bonding Capillary log no from S-TCM-WB-PL-01 to S-TCM-WB-PL-07 15.Update wire bonding WB tooling log no from S-TCM-WB-PL-01 to S-EES-WB-002-1 16.Update wire bonding Golden wire log no from S-TCM-WB-PL-01 to MES 17.Update 3rd OPT NSP QA 3'rd Gate log no from S-TCM-WB-QCPL-04 to MES	
AV	2013.06.28	1. For marking process: Visual marking form 2 strips/machine/shift To Auto:2 strips/machine/shift & Manual: 2 strips/30strips 2. For EVI process: Visual Inspection from S-PES-EVI-001 to S-PES-EVI-001/011 Visual Inspection from 2000units ,1X/lot to 5% or 2000units ,1X/lot Visual Inspection from S-PES-EVI-001/002/003/004/005/009/010 to S-PES-EVI-001/002/003/004/005/009/010/011 Visual Inspection from TCM-TST-QCPL-03 to MES 3. For molding process: Molding Compound Aging Time/ Shelf Life/ Type from Reading to Reading & E-TCM monitor Molding Compound Aging Time/ Shelf Life/ Type from 1X/beginning of shift to 1X/shift change Molding Compound Aging Time/ Shelf Life/ Type from Log Sheet&T-card to E-TCM&Log Sheet&T-card Visual Inspection from First2shot/PKG change/compound type change/mold die cleaning to First2shot/PK change/compound change/mold die change/ recipe change/set up/repair/ mold cleaning/mold release Visual Inspection from S-TCM-MD-QCPL-05&S-TCM-MD-PL-02&MES to S-TCM-MD-QCPL-04&Monitor System Parameter from 1XBeginning of shift/PKG change/compound type change to First2shot/PKG change/compound change/mold die change/ recipe change/set up/repair/ mold cleaning/mold release Compound Temperature from 1X/machine/week(For manual mold) to 1X/machine/week&1X/buy off(For manual	Yu Q

		mold) Internal Defect from S-TCM-MD-QCPL-05&S-TCM-MD-PL-02&MES to Monitor System Molding inspection log sheet change from S-TCM-MD-PL-02 to S-TCM-MD-PL-01 4. For TF process: Dejunk/Dedambar die Auto trim system from S-TCM-TF-QCPL-02&T-Card to Monitor System Dedambar punch from S-TCM-TF-QCPL-01&S-TCM-TF-QCPL-02 to S-TCM-TF-QCPL-01 Solderability Test from 3units, 1x/descale type/machine/shift to 5units, 1x/descale type/machine/shift Visual monitor from S-TCM-TF-QCPL-02&T-Card to Monitor System 5. For packing process: Visual gate from Tube: 2 tubes / Box: All / Qty: Partial tube / Label: All to Visual: 1 tube or tray / Qty: 1 box per 5 boxes/ Label: All Visual gate from TCM-IPK-QCPL-01 to MES 6. Delete Grinder Roughness/ Flatness 7. For INSP. QA 2nd Gate: Visual inspection from Log Sheet to Log Sheet/Monitor system and S-TCM-WS-QCPL-01 to S-TCM-WS-QCPL-01/Monitor system 8. For WB process: Visual inspection from Log Sheet to Log Sheet/Monitor system and S-TCM-WB-QCPL-01 to S-TCM-WB-QCPL-01/Monitor system 9. Update Dedambar/Dejunk to Trim	
AW	2013.12.11	1. For DA process: Update all S-TCM-DA-PL-01 to S-TCM-DA-PL-10 2. For Marking process, Visual/marking from Auto:2 strips/machine/shift Manual: 2 strips/30strips to Auto(except MZC001/MZC002):2 strips/machine/shift, MZC001/MZC002: 2strips/1X/magazine/lot, Manual: 2 strips/30strips 3.For PT process: Update Machine deflash spec no. from S-PES-PT-005 to S-PEW-PT-001 Update Measuring method from Visua (Naked eye & magnifier (Min3X) or Low power scope 10X-40X) to Visual (Naked eye & or Low power scope 10X-40X) Update Pb free bake spec no from S-PES-PT-005 to S-PEW-PT-002	Yu Q
AX	2013.12.30	1. Update Back grind Grinder Parameter log no from S-TCM-BG-PL-01 to T-card S-PES-BG-011-3 S-PES-BG-011-4; For Back grind Grinder Parameter from 1X/shift/machine to 1x/Lot and1X/shift/machine. 2. Update Tape remove Visual inspection log no from S-TCM-BG-PL-03 to T-card. 3. Update Wafer saw and INSP. QA 2nd Gate Visual inspection Measuring methods from Naked eye &microscope (50X-200X) to Naked eye &microscope (100X-200X). 4. Update INSP. QA 2nd Gate Visual inspection log no from S-PES-WS-007-1 to T-card	Yu Q
AY	2014.01.28	1. Update D/A adhesive, type sample plan size/freq from 1X/beginning of shift or epoxy change to 1X/ epoxy change	Yu Q

		Update D/A leadframe, type sample plan size/freq from 1X/beginning of shift or device change to 1X/every loading lead-frame or device change Update D/A leadframe, type Analysis Method and Log no.	
AZ	2014.07.08	Update Plating CP：1The process name：plating 2 deflash，add parametor monitor 3 visual monitor：S-TCM-PT-PO 4 parametor monitor ：S-TCM-PT-PL-14/15/17 5 thickness composition record：MES 6 solderability test：Solderability tester& Low power scope 10X-40X	Xu L
BA	2015.05.08	Update: 1.Molding : Visual Inspection : Sampling Plan Size/Freq: 1shot, 1x/machine/shift, 1x/buy off,1x/mold die cleaning, 2.Delete: Molding Compound Temperature 3.Delete: Plating Parameter Monitor 4.Marking : Visual /marking Sampling Plan Size/Freq. 1strips/buy off 5.Marking : Laser depth (TQFP/LQFP/MSOP/TSOP/TSSOP/TSOT/QFN) : Sampling Plan Size/Freq. 3ponits/2units/1x/buy-off 6.Post D/A Cure(Cure Oven) :LOG NO 7 Wire Bonding: Visual inspection : Sampling Plan Size/Freq: 1 strip / 1X / Shift / machine or 1 strip / 1X / buy off Bond pull strength :Sampling Plan Size/Freq: 1 strip / 1X / day/ machine or 1 strip / 1X / buy off Ball shear strength:Sampling Plan Size/Freq: 1 strip / 1X / day/ machine or 1 strip / 1X / buy off Wire loop height :Sampling Plan Size/Freq: 5Wire:1X/Device change BAR(Ball diameter/ball thickness) :Sampling Plan Size/Freq: 5 Ball :1X/Device change	ZhangYX
BB	2015.06.30	ADD:1.OCAP NO. 2.Marking: The Characteristic of marker control plan. 3.Plating:Chemical Deflash control plan; Set up check control plan.	Yin J
BC	2015.10.19	Update: Marking: The Characteristic of Parameter	Yin J

BD	2015.11.05	Update: 1.Wire Bonding: visual Inspection/Bond pull strength/Ball shear strength : Sampling Plan Size/Freq change 2. INSP.QA 2nd Gate:Visual inspection:Analysis method/log No change 3.Post D/A Cure:Cure Oven Epoxy void analysis metod and log No change; 4.Molding :Misalign/Mismatch/Parameter:Log No change 5.Plating:Solderability Test/Rinse Effectiveness(contamination Test)/Chemicai bath concentration anylysis:Log no change 6.Marking:Marker Visual/marking:Log No change.	Yin J
BE	2016.03.29	Marking: Add PROD visual inspection control.	Yin J
BF	2016.05.09	Update： 1. Plasma Clean(optional) add Contact Angle control 2. Plating Add Peeling test control	Yin J
BG	2016.07.25	Add： The control item and parameter	Yin J
BH	2016.08.31	Add: Update defect item, add Failure mode about NSOP/Missing wire, NSOL/Lifted stitch, Sagging wire, Broken wire, No bonding	Yin J

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
Back grind	Tape laminate	N/A	N/A	Tape type/life time	S-PES-BG-011	Refer to SPEC	Reading	1x/Lot	T-card	T-card	S-TCM-BG-PO-01,03	PROD	NS/NE
			Visual inspection	N/A	S-PES-BG-011	Refer to SPEC	Naked eye	Each wafer/Lot	T-card	T-card	S-TCM-BG-PO-01,03	PROD	SM/NS/NE/OCAP/100%I
	Grinder		NA	Parameter	S-PES-BG-011.	Refer to SPEC	MC Reading	1x/Lot and 1X/shift/machine	T-Card	T-card S-PES-BG-011-3 S-PES-BG-011-4	S-TCM-BG-PO-05	PROD	SM/NS/NE/OCAP
			NA	D.I. Water resistivity	S-PES-BG-013	≥13MΩ・cm	MC Reading	1 Readings / machine / shift	Log sheet	S-PES-BG-011-3 S-PES-BG-011-4	S-TCM-BG-PO-06	PROD	SM/NS/NE/OCAP
			NA	Grind wheel life	S-PES-WS-014	Min:600 um	Machine Auto Measure	1 Readings / machine / shift	Log sheet	S-PES-BG-011-3 S-PES-BG-011-4	S-TCM-BG-PO-07	PROD	SM/NS/NE/OCAP
			Visual inspection,	N/A	S-QAW-WS-001 S-PES-BG-011 S-PEW-BG-013	Refer to SPEC	Naked eye	1 wafer,1X/shift/machine	Log Sheet	S-TCM-BG-QCPL-02	S-TCM-BG-PO-01,03	QA	SD/NS/NE/OCAP/QRR
					S-PES-BG-011 S-PEW-BG-013	Refer to SPEC	Naked eye	First wafer/set up	T-card	T-card	S-TCM-BG-PO-01,03	PROD	SM/NS/NE/OCAP/100%I
			Thickness	N/A	BD & S-PES-BG-011 S-PEW-BG-013	±25.4um	Thickness tester	5 points /first wafer/set up	T-card	T-card	S-TCM-BG-PO-02	PROD	SM/NS/NE/OCAP/100%I
								5 points/1 wafer/1X/lot	T-card	T-card			
					BD & S-PES-BG-011 S-QAW-WS-001 S-PEW-BG-013		Thickness tester	1 wafer, 5 points, 1X/shift/machine	Log Sheet	S-TCM-BG-QCPL-02	S-TCM-BG-PO-02	QA	SD/NS/NE/OCAP/QRR
	Tape remove		Visual inspection	N/A	S-PES-BG-011	Refer to SPEC	Naked eye	Each wafer/Lot	T-card	T-card	S-TCM-BG-PO-03	PROD	SM/NS/NE/OCAP/100%I
Wafer Mount	Wafer mount	NA	NA	Tape type/life time	S-PES-WS-008	Refer to SPEC	Reading	1x/Lot	T-card	T-card	S-TCM-WS-PO-21	PROD	NS/NE
		N/A	Die orientation	N/A	S-PEW-WS-007	Refer to Bond Diagram	High power scope (50x-200x)	First wafer/lot	T-card	T-card	S-TCM-WS-PO-14	PROD	NS/NE
		N/A	Wafer thickness	N/A	BD&S-PES-WS-008 S-PEW-WS-007	±25.4um	Thickness tester	1 point/1X/lot Before WM	T-card	T-card	S-TCM-BG-PO-02	PROD	SM/NS/NE
		N/A	Air Bubble/ Void/FM	N/A	S-PES-WS-008	≤芯片面积的25%; ≤wafer 总面积的10%	Naked eye	Every wafer	T-card	T-card	S-TCM-WS-PO-02	PROD	SM/NS/NE/OCAP

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

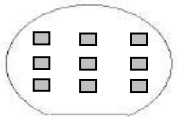
Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
Post mount Cure(optional)	Oven	N/A	N/A	Temp / Time	S-PES-WS-008	1.SPV 224 tape: 60±10℃ 2.T-80 tape Die size≤1mm, temp setting:100±10℃;1mm<die size ≤ 2mm, temp setting:80 ± 10 ℃ ; 2mm<die size≤4mm,temp setting:60±10℃	MC Reading	1x/batch	T-card	T-card	S-TCM-WS-PO-18	PROD	SM/NS/NE/AE
Wafer Saw	Wafer Sawing	N/A	N/A	Parameter	S-PES-WS-007	Refer to SPEC	Reading	1X / wafer lot or 1X/shift	Log Sheet	S-TCM-WS-PL-02	S-TCM-WS-PO-22	PROD	SM/NS/NE/AE/OCAP
		N/A	N/A	D.I. Water resistivity	S-PES-WS-003	≥13MΩ・cm	Reading	1 X / machine / shift	Log Sheet	S-TCM-WS-PL-02	S-TCM-WS-PO-13	PROD	SM/NS/NE/AE/OCAP
		N/A	N/A	D.I. Water resistivity（+CO2）	S-PES-WS-003	0.3-1.0MΩ·cm	Reading	1 X / machine / shift	Log Sheet	S-TCM-WS-PL-02	S-TCM-WS-PO-06	PROD	SM/NS/NE/AE/OCAP
		N/A	N/A	D.I. Water pressure	S-PES-WS-003	双轴(0.15MPa~0.6MPa); 单轴：0.2Mpa~0.6Mpa	Reading	1 X / machine / shift	Log Sheet	S-TCM-WS-PL-02	S-TCM-WS-PO-16	PROD	SM/NS/NE/AE/OCAP
		☆	Kerf Width	N/A	S-PES-WS-007	Refer to SPEC	Machine monitor	5 Readings / machine / shift	X-BAR & R	MES	S-SPC-OCAP-008	PROD	SM/NS/NE/OCAP
		NA	Visual inspection	N/A	S-PES-WS-003	Refer to SPEC	Naked eye microscope (100X-200X)	Top side: 5 units/9 points/first wafer/lot Back side: 5 units/9 points/first wafer/lot	Log sheet	S-TCM-WS-PL-02	S-TCM-WS-PO-04& 05& 06& 07	PROD	SM/NS/NE/OCAP/100%I
					S-PES-WS-003	Refer to SPEC	High power scope (100X-200X)	First wafer. 1x / buy-off	Log sheet	S-TCM-WS-PL-02	S-TCM-WS-PO-04& 05& 06& 07	QA	QRR/100%I

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
	Saw Blade	N/A	N/A	Life time	S-PES-WS-007	Refer to SPEC	Machine counter	Life time over	Log Sheet	S-TCM-WS-PL-02	S-TCM-WS-PO-12	PROD	NS/NE/SM/AE/OCAP
Bar code printer (Optional)	Bar code printer machine	N/A	Printed Wafer No	N/A	S-PEW-DA-021	Refer to SPEC	Naked eye or Min 10x Microscope	Each wafer/Lot	T-card	T-card	S-TCM-WS-PO-03	PROD	SM/NS/NE/AE
U.V. Release (Optional)	UV Release Machine	N/A	N/A	U.V Power Density	S-PEW-WS-008	Refer to SPEC	Radiation-density meter	6 points,1x/machine/week	Log Sheet	S-EES-WS-006-1	S-TCM-WS-EO-10	EE	NS/NE/SM/AE
INSP. QA 2nd Gate	NA	N/A	Visual inspection	N/A	S-PES-WS-003	Refer to SPEC	High power scope (Min 100X)	LTPD=5% 5 wafers/mother lot, 9 points/wafer, 5 units/point. If less than 5 wafers, need inspect 225 dies 	T-card	T-card	S-TCM-WS-PO-08&09&10&11	PROD	100%I/NS/NE/OCAP
			Visual inspection	N/A	S-PES-WS-003 S-QAW-WS-001	Refer to SPEC	High power scope (Min 100X)		Monitor system	Monitor system	S-TCM-WS-PO-08&09&10&11	QA	NS/NE/QRR
Die Attach	D/A adhesive	N/A	N/A	Batch number	S-PES-DA-002	Refer to the label	Reading	1X/ Epoxy receiving or issue	Log Sheet	Material control system	S-TCM-DA-PO-42	PROD MH	NS/NE
				Shelf life	S-PES-DA-002	Refer to SPEC	System check	Every 10 seconds	Epoxy expired system	Epoxy expired system	S-TCM-DA-PO-42	MH	NS/NE
				Type	S-PES-DA-008	Refer to SPEC	Reading	1X/epoxy change	Log Sheet	S-TCM-DA-PL-10		PROD	NS/NE
	Pick up tool	N/A	N/A	Life span	S-PES-DA-008	Min.1time/2days	Reading	Refer to SPEC	Log Sheet	S-TCM-DA-PL-10	S-TCM-DA-PO-42	PROD	NS/NE./100%I
	Lead-frame	N/A	N/A	Type	S-PES-DA-008 S-PEW-DA-012	Refer to the T-Card	Reading	1X/every loading lead-frame or device change	T-card	T-card	S-TCM-DA-PO-42	PROD	NS/NE
								1X/device change	T-card	T-card		QA	SD//NS/NE/QRR
								1X/shift/machine	Log Sheet	S-TCM-DA-QCPL-01		QA	
	Die Bonder	N/A	Visual inspection	N/A	S-QAW-DA-001 S-PES-DA-008	Refer to SPEC	Low/High power scope (10x-40x /50x-200x)	1 strip. 2x / machine / shift 1 strip. 1x / buy-off	Log Sheet	S-TCM-DA-QCPL-01 S-TCM-DA-QCPL-05 S-TCM-DA-PL-10	S-TCM-DA-PO-01 to S-TCM-DA-PO-04/ S-TCM-DA-PO-11 to	QA	QRR/100%I
			Epoxy coverage	N/A	S-QAW-DA-001 S-PES-DA-008	min.75 % of die periphery		1 strip. 2x / machine / shift 1 strip. 1x / buy-off		S-TCM-DA-QCPL-01 S-TCM-DA-QCPL-05 S-TCM-DA-PL-10			

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
			Epoxy fillet height	N/A	S-QAW-DA-001 S-PES-DA-008	max. 85% of die thickness		1 strip. 2x / machine / shift 1 strip. 1x / buy-off		S-TCM-DA-QCPL-01 S-TCM-DA-QCPL-05 S-TCM-DA-PL-10	S-TCM-DA-PO-22		
			Visual monitor (RTI)	N/A	S-PES-DA-008	Refer to SPEC	Low/High power scope (10x-40x /50x-200x)	Min. 1 strip/ 3 magazines	T-card	T-card	S-TCM-DA-PO-01 to S-TCM-DA-PO-04/ S-TCM-DA-PO-11 to S-TCM-DA-PO-22	PROD	NS/100%I/O CAP
			Epoxy coverage	N/A	S-PES-DA-008	min.75 % of die periphery		Min. 1 strip/ 3 magazines	T-card	T-card			
			Epoxy fillet height	N/A	S-PES-DA-008	max. 85% of die thickness		Min. 1 strip/ 3 magazines	T-card	T-card			
			Die tilt	N/A	S-QAW-DA-001 S-PES-DA-008	Max.30um.	Measuring microscope	5 units. 1x/machine/day 5 units. 1x/device change	Log Sheet	S-TCM-DA-QCPL-01 S-TCM-DA-PL-10	S-TCM-DA-PO-16	QA	QRR/SD /AE
Die Attach		N/A	Wet epoxy thickness	N/A	S-QAW-DA-001 S-PES-DA-008	Die < 100mil, 0.3~2.0mil (7.6~50.8um) Die >=100mil, 0.6~2.0mil (15.2~50.8um)	Measuring microscope	5 units. 1x/machine/day 5 units. 1x/device change	MES	MES	S-TCM-DA-PO-28	QA	SD,OCAP,QRR
									Log Sheet	S-TCM-DA-PL-10			AE
		N/A	Pin mark monitor	N/A	S-QAW-DA-001 S-PES-DA-008	No pin mark	High Power Microscope(Min 200X)	2 units 1x/machine/shift 2 units / device change	Log Sheet	S-TCM-DA-QCPL-01 S-TCM-DA-PL-10	S-TCM-DA-PO-10	QA	SD,OCAP,QRR
		N/A	N/A	Parameter	S-PES-DA-008	Refer to SPEC	Reading	1x/device change	Log Sheet	S-TCM-DA-PL-10	S-TCM-DA-EO-11	EE	NS/NE/AE
		N/A	N/A	Map orientation	S-PEW-DA-021	Refer to SPEC	Reading	1x/device change	Log Sheet	S-TCM-DA-PL-10	S-TCM-DA-PO-06	EE	NS/NE/AE
								1x/device change	Log Sheet	S-TCM-DA-PL-10	S-TCM-DA-PO-06	QA	SD,OCAP,QRR
		N/A	N/A	Three point in a line	S-PES-DA-008	Refer to SPEC	Visual check	1X/device change	Log Sheet	S-TCM-DA-PL-10	S-TCM-DA-EO-12	EE	NS/NE/AE
								1x/ beginning of shift or pick up tool change		S-TCM-DA-PL-10		PROD	

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
Post D/A Cure	Cure Oven	N/A	N/A	Parameter	S-QAW-DA-001 S-PEW-DA-009	Refer to SPEC	Reading	1 reading/oven/day	Log Sheet	S-TCM-DA-QCPL-04	S-TCM-DA-PO-29	QA	SD/NS/NE/QRR
			Epoxy void	N/A	S-QAW-DA-001 S-PES-DA-008	For single void, Max. 5% of the die size. For multi void, Max. 10% of the die size	X-Ray machine	5 units. 1x/oven/day (Except DAD-90B2 / insulating glue)	Log Sheet	S-TCM-DA-QCPL-04	S-TCM-DA-PO-41	QA	SD/NS/NE/QRR
		☆	Die shear strength	N/A	S-QAW-FOL-002 S-PES-DA-008	Refer to SPEC	Die Shear Tester	5 units. 1x/oven/day （For oversea customer only）	Log Sheet (Report CPK)	MES	S-TCM-DA-PO-07	QA	NS/NE/QRR
Plasma Clean (optional)	Plasma Cleaning Machine	N/A	N/A	Plasma Clean Time/Para	S-PES-WB-009	Refer to SPEC	MC Reading	1x/ sub-lot	E-system	Plasma cleaning system	N/A	PROD	SD/NS/NE/AE
		N/A	Contact Angle	N/A	S-PES-WB-009	≤30°	MC Reading	1X/Machine/Day	Lot Sheet	S-TCM-WB-QCPL-06	N/A	QA	SD/NS/NE/AE
Wire Bonding	Wire Bonder	N/A	Visual inspection	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	Refer to spec S-PES-WB-001	Low power scope(10x-40x)	1 strip / 1X / Shift / machine or 1 strip / 1X / buy off	Log Sheet Monitor system Log Sheet Buy off system	S-TCM-WB-QCPL-01 Monitor system S-TCM-WB-PL-07 Buy off system	S-TCM-WB-PO-01 to S-TCM-WB-PO-38	QA	SD/OCAP/NS/NE/QRR
			Visual monitor (RTI)	N/A	S-PEW-WB-001 S-PES-WB-001	Refer to spec S-PES-WB-001	Low power scope(10x-40x)	Min. 1 Strip / Magazine	Log Sheet	T-CARD	S-PEW-NP-004-02 to S-PEW-NP-004-08	PROD	SM/OCAP/NS/NE/100%I/AE
		N/A	Wire loop height	N/A	S-PES-WB-001 S-PEW-WB-001	Refer to spec S-PES-WB-001	Measure microscope	5 wires. 1x/Device change	Buy off system	MES Buy off system	OCAP-S-TCM-WB-PO-06	QA	SD/NS/NE/QRR /OCAP
		N/A	BAR(Ball diameter/ball thickness) BAR	N/A	S-PES-WB-001 S-PEW-WB-002	3.5~6	Measure microscope	5 Ball 1x/Device change	Log sheet	MES Buy off system	S-TCM-WB-PO-13/14	QA	SD/NS/NE/QRR
		☆	Bond pull strength	N/A	S-PES-WB-008 S-PEW-WB-001	Refer to spec S-PES-WB-008	Bond Pull Tester	10wires / 1X / day/ machine or 10wires / 1X / buy off	X-BAR & R Buy off system	MES Buy off system	S-SPC-OCAP-002	QA	SD/NS/NE/QRR /OCAP

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
		☆	Ball shear strength	N/A	S-PEW-WB-002	Refer to spec	Ball Shear Tester	10 Balls/ 1X / day / machine or 10 Balls / 1X / buy off	X-BAR & R X-BAR & R Log sheet	MES Buy off system MES Buy off system	S-SPC-OCAP-003	QA	SD/NS/NE/QRR
		N/A	Bonding temperature	N/A	S-PES-WB-008	Refer to spec S-PES-WB-008 or recipe	MC Reading	1X/Machine/Shift	Log sheet	S-TCM-WB-PL-08	N/A	PROD	SD/OCAP/NS/NE/QRR
		N/A	Bond Diagram	BD No	S-PES-WB-001	Refer to T-Card	Reading	1X/Machine/Shift	Log sheet	S-TCM-WB-PL-08	S-TCM-WB-PO-17	PROD	SD/OCAP/NS/NE/QRR
		N/A	Parameter	N/A	S-PES-WB-008	Refer to spec S-PES-WB-008 or bonding recipe	Reading Cu Recipe	1X/Machine/Shift	Log sheet	S-TCM-WB-PL-08	S-TCM-WB-PO-01 to S-TCM-WB-PO-38	PROD	SD/OCAP/NS/NE/QRR
	Forming Gas	N/A	Ag_Au N2/H2 gas	N/A	S-PEW-WB-002 S-QAW-WB-004	ASM(L/M): 0.2-0.3 KNS(L/M): 0.2-0.3;	Reading flow meter	1 X/machine/shift	Log sheet	S-TCM-WB-PL-08	S-TCM-WB-33	PROD	NS/NE
							Reading flow meter	1 X/machine/shift	Log sheet	S-TCM-WB-QCPL-05		QA	SD/NS/NE/QR
		N/A	Cu N2/H2 gas	N/A	S-PEW-WB-002 S-QAW-WB-004	ASM(L/M): CH1 : 0.3-0.5; CH2: 0.7-0.9; CH3: 0.5-0.7 KNS(L/M): 0.57-0.85;	Reading flow meter	1 X/machine/shift	Log sheet	S-TCM-WB-PL-08	S-TCM-WB-33	PROD	NS/NE
							Reading flow meter	1 X/machine/shift	Log sheet	S-TCM-WB-QCPL-05		QA	SD/NS/NE/QR
	Bonding Wire	N/A	Wire dimension&type	N/A	S-PEW-WB-001	Refer to spec	Reading	1X/wire change	Monitor system	MH System MES	N/A	PROD	NS/NE
		N/A	Wire dimension &type	N/A	S-PEW-WB-002	Refer to spec	Material code	1X/wire change	Monitor system	MH System MES	N/A	PROD	NS/NE
		N/A	Floor life	N/A	S-PEW-WB-002	PdCu wire 7 days Cu wire 2 days	Check the accumulated exposed time record	1 X/machine/shift	Log sheet	S-TCM-WB-PL-08 S-PEW-WB-002-2	N/A	PROD	NS/NE
	Capillary	N/A	N/A	Life time	S-PES-WB-008 S-PEW-WB-001	Refer to spec S-PES-WB-008	Machine counter	Life time over	Log sheet	S-TC0M-WB-PL-07	N/A	PROD	NS/NE

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
	WB tooling	N/A	Tooling No.	N/A	S-PEW-WB-001	Refer to spec	Reading	1X/PKG change	Log sheet	S-EES-WB-002-1	S-TCM-WB-PO-39	EE	NS/NE
	N/A	N/A	Golf Bond	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	Refer to spec S-PES-WB-001	Low power scope(10x-40x	1 strip / 1X / Shift / machine or 1 strip / 1X / buy off	Log Sheet	T-CARD MES	S-TCM-WB-PO-20	PROD	SD/OCAP/NS/NE/QRR
			Bond Short	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	Refer to spec S-PES-WB-001	Low power scope(10x-40x	1 strip / 1X / Shift / machine or 1 strip / 1X / buy off	Log Sheet	T-CARD MES	S-TCM-WB-PO-10	PROD	SD/OCAP/NS/NE/QRR
			Pad crater	N/A	S-PES-WB-001 S-PEW-WB-002	No crater	High Power Scope (min 500X)	2units ,1 X/machine/day(BOAC)	Log sheet	S-TCM-WB-QCPL-05	S-TCM-WB-PO-32	QA	SD/NS/NE/QRR
								2units ,1x / buy off	Log sheet	MES S-TCM-WB-PL-07		QA	SD/NS/NE/QRR
			NSOP/ Missing wire	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	Refer to spec S-PES-WB-001	Low power scope(10x-40x)	1 strip / magazine	Log sheet	T-CARD	S-TCM-WB-PO-01	PROD	SD/NS/NE/QRR
			NSOL/Lifted stitch	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	Refer to spec S-PES-WB-001	Low power scope(10x-40x)	1 strip / magazine	Log sheet	T-CARD	S-TCM-WB-PO-04	PROD	SD/NS/NE/QRR
			Sagging wire	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	Refer to spec S-PES-WB-001	Low power scope(10x-40x)	1 strip / magazine	Log sheet	T-CARD	S-TCM-WB-PO-05	PROD	SD/NS/NE/QRR
			Broken wire	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	No broken wire	Low power scope(10x-40x)	1 strip / magazine	Log sheet	T-CARD	S-TCM-WB-PO-09	PROD	SD/NS/NE/QRR
			No bonding	N/A	S-PES-WB-001 S-QAW-WB-004 S-PEW-WB-001	No unbond	Low power scope(10x-40x)	1 strip / magazine	Log sheet	T-CARD	S-TCM-WB-PO-18	PROD	SD/NS/NE/QRR
	Golden wire	N/A	Wire dimension&type	N/A	S-PEW-WB-001	Refer to spec	Reading	1X/wire change	MES	MES	N/A	PROD	NS/NE
3rd OPT NSP QA 3'rd Gate	N/A	N/A	Visual inspection	N/A	S-PES-WB-001 S-QAW-WB-004	Refer to spec S-PES-WB-001	Low power scope (10x-40x)	AQL 0.065%: 1X/lot, (Acc/Rej : 0/1)	MES	MES	S-TCM-WB-PO-01 to S-TCM-WB-PO-38	QA	NS/NE/QRR/OCAP
Plasma Clean (optional)	Plasma Cleaning Machine	N/A	N/A	Plasma Clean Time/Para	S-PES-WB-009	Refer to SPEC	MC Reading	1x/ sub-lot	Log Sheet	S-TCM-WB-PL-03	N/A	PROD	SD/NS/NE/AE

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
Molding	Molding Compound	N/A	N/A	Aging Time/ Shelf Life Type	S-PES-MD-002 S-PEW-MD-001	24h for aging time; 48h for floor life; type refer to spec	Reading E-TCM monitor	1X/shift change or 1X/compound change	E-TCM Log Sheet T-card	S-TCM-MD-PL-01 T-card	S-TCM-MD-PO-25	PROD	NS/NE
	Molding	N/A	Visual Inspection	N/A	S-PES-MD-001 S-PEW-MD-001 S-QAW-MD-001	Refer to Spec	Naked eyes /Magnifier(Min5X) / Low Power Scope (10X-40X))	1shot,1X/machine/shift 1X/Buy off 1X/ mold die cleaning	Log Sheet	S-TCM-MD-QCPL-01 S-TCM-MD-QCPL-04 Monitor System	S-TCM-MD-PO-01/02/07/09	QA	SD/NS/NE/QRR
		N/A	Internal Defect	N/A	S-PES-MD-001 S-PEW-MD-001 S-QAW-MD-001	Refer to Spec	X-Ray	1 shot ,1X/machine/shift 1X/buy off	Log Sheet	S-TCM-MD-QCPL-01 Monitor System	S-TCM-MD-PO-03/04/05	QA	SD/NS/NE/QRR
		N/A	Misalign/ Mismatch	N/A	S-PES-MD-001 S-QAW-MD-001	PDIP≤ 5mil(0.127mm) TSSOP16≤ 2mil(0.0508mm) Other≤ 3mil(0.0762mm)	Measuring microscope	2 units,1X/machine/week	Log Sheet	S-TCM-MD-QCPL-01	S-TCM-MD-PO-06-08	QA	SD/NS/NE/QRR
								2 units,1X/buy off					
		N/A	N/A	Parameter	S-QAW-MD-001 Mold instruction	Refer to spec	Machine reading	1X/buy off	Log Sheet	S-TCM-MD-QCPL-01	S-TCM-MD-EO-04/05/07	QA	SD/NS/NE/QRR
								First2shot/PKG change/compound change/mold die change/ recipe change/set up/repair/ mold cleaning/mold release	Log Sheet	S-TCM-MD-PL-01	S-TCM-MD-EO-04/05/07	PROD	NS/NE
		N/A	N/A	Mold Temperature	Mold instruction S-QAW-MD-001	Refer to Spec	Thermometer	5 Points of Top die 5 Points of Bottom die, 10 pionts;1X/machine/week 10 pionts/1X /Buy off	Log Sheet	S-TCM-MD-QCPL-01	S-TCM-MD-EO-03	QA	SD/NS/NE/QRR
PMC	Oven	N/A	N/A	Curing profile	S-PEW-MD-014	Non-green:4h@175℃; Green:5h@175℃; special parts refer to spec	Thermocouple meter	Continuous Monitoring	PC monitor	N/A	S-TCM-MD-PO-20	PROD	SM/NS/NE/AE

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
		N/A	N/A	Temperature	S-PEW-MD-014 S-QAW-MD-001	175 +/- 5 ℃	Reading	1 reading/oven/day	Log Sheet	S-TCM-MD-QCPL-03	S-TCM-MD-EO-08	QA	SD/NS/NE/QRR
		N/A	Delaminating (SMD)	N/A	S-QAW-FA-025	Refer to Spec	Ultra-sonic Scan	2 strips/machine/day	Log Sheet	S-QAW-FA-025-1	S-TCM-MD-PO-12	QA	SD/NE
Trim	Dejunk/Dedambar die Auto trim system	N/A	Visual monitor	N/A	S-QAW-TF-001 S-PES-TF-001	Refer to SPEC	Low power scope (10X-40X)	2 strips, 3x/machine/shift 2strips, 1x/Buy off	Log Sheet	S-TCM-TF-QCPL-01 Monitor System	S-TCM-TF-P0-01/05/03/07/08/09 10/11/12	QA	SD/NS/NE/QRR
					S-PES-TF-001	Refer to SPEC	Visual (Naked eye & magnifier (Min3X) or Low power scope 10X-40X)	2 strips, Assy lot size≥10000, 6X/lot Assy lot size<10000, 3X/lot Assy lot size≤315, 1x/lot	Log Sheet	T-Card	S-TCM-TF-P0-01/05/03/07/08/09 10/11/12	PROD	SM/NS/NE/OCAP/100%I
	Dedambar punch	N/A	N/A	Life time	S-EES-TF-004	Refer to SPEC	Auto record	Life time alarm/over	Monitor system	ERS monitor system	N/A	EE	SM/AE/NE/NS
			Window flash buy off	N/A	S-QAW-TF-001 S-PES-TF-001	≤ 0.254mm	Profile Project	5units,1x/machine/shift 5units ,1x/Buy off	Log Sheet	S-TCM-TF-QCPL-01	S-TCM-TF-P0-12	QA	SD/NS/NE/OCAP/QRR
Soften	Chemical Deflash	N/A	N/A	Parameter	S-PES-PT-005	Refer to SPEC	Visual (reading & checking)	1x/shift	Log sheet	S-TCM-PT-SC-04	S-TCM-PT-PO-08	PROD	NS/NE
			N/A	Temperature	S-PES-PT-005	100-120℃& 60-80℃	Reading	1x/shift	Log sheet	S-TCM-PT-SC-04	S-TCM-PT-PO-08	PROD	NS/NE
Machine Deflash (option)	Deflash	N/A	Visual Inspection	N/A	S-PEW-PT-001 S-QAW-PT-001	Refer to SPEC	Visual (Naked eye & or Low power scope 10X-40X)	3 strips/lot	Log sheet	T-CARD	S-TCM-PT-PO-08	PROD	NS/NE
			N/A	Parameter	S-PEW-PT-001	200-400kg/cm3	Reading	1x/PKG type/machine/shift	Log sheet	S-TCM-PT-PL-18	S-TCM-PT-EO-10	PROD	NS/NE
Plating	Plating	N/A	N/A	Parameter	S-V-PT-002 S-V-PT-005	Refer to SPEC	Recipe	1x/PKG type/machine/shift	Log sheet	S-TCM-PT-PL-15	S-TCM-PT-PO-01	PROD	NS/NE
			N/A	Belt Speed	S-V-PT-002 S-V-PT-005	3-7M/min	Reading & checking	1x/PKG type/machine/shift	Log sheet	S-TCM-PT-PL-15	S-TCM-PT-PO-01	PROD	NS/NE

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
			N/A	Plating Current	S-V-PT-002 S-V-PT-005	50-200A	Reading & checking	1x/PKG type/machine/shift	Log sheet	S-TCM-PT-PL-15	S-TCM-PT-PO-01	PROD	NS/NE
		N/A	Visual Inspection	N/A	S-PES-PT-005 S-QAW-PT-001	Refer to SPEC	Visual (Naked eye & magnifier (Min3X) or Low power scope 10X-40X)	200 units from Min 10strips,1x/PKG type/machine/shift or 1X chemical solution make up	Log Sheet	S-TCM-PT-QCPL-01 S-TCM-PT-PL-01	S-TCM-PT-PO	QA	NS/NE/SD/OCA P/QRR
			Missing Plating	N/A	S-PES-PT-005 S-QAW-PT-001	Refer to SPEC	Visual (Naked eye & magnifier (Min3X) or Low power scope 10X-40X)	200 units from Min 10strips,1x/PKG type/machine/shift or 1X chemical solution make up	Log Sheet	S-TCM-PT-QCPL-01 S-TCM-PT-PL-01	S-TCM-PT-PO	QA	NS/NE/SD/OCA P/QRR
			Bridging	N/A	S-PES-PT-005 S-QAW-PT-001	≤50% leads gap	Visual (Naked eye & magnifier (Min3X) or Low power scope 10X-40X)	200 units from Min 10strips,1x/PKG type/machine/shift or 1X chemical solution make up	Log Sheet	S-TCM-PT-QCPL-01 S-TCM-PT-PL-01	S-TCM-PT-PO	QA	NS/NE/SD/OCA P/QRR
			Peeling test	N/A	S-QAW-PT-001	No Peeling	Bistoury	1unit, 1x/PKG type/machine/shift or chemical solution make up	Log Sheet	S-TCM-PT-QCPL-01	S-TCM-PT-PO-11	QA	NS/NE/SD/OCAP/QRR
			Visual Inspection	N/A	S-PES-PT-005	Refer to SPEC：	Visual (Naked eye & magnifier (Min3X) or Low power scope 10X-40X)	9strips /lot	Log Sheet	T-CARD	S-TCM-PT-PO	PROD	NS/NE/OCA P
			Leadframe /Lead Damage：	N/A	S-PES-PT-005	No Damage	Visual (Naked eye & magnifier (Min3X) or Low power scope 10X-40X)	9strips /lot	Log Sheet	T-CARD	S-TCM-PT-PO	PROD	NS/NE/OCA P
		☆	Thickness Monitor	N/A	S-PES-PT-005 S-QAW-PT-001	5-15um& 10.2-17.8um	Thickness tester	10 points from 5 strips 1x/PKG type/machine/shift or chemical solution make up	X-Bar	MES	S-TCM-PT-PO-01; S-SPC-OCAP-004	QA	NS/NE/SD/OCAP/QRR

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
		☆	Composition Monitor	N/A	S-PES-PT-005 S-QAW-PT-001	Pb free products: Sn 98~100%	Composition tester	10 points from 5 strips 1x/PKG type/machine/shift or chemical solution make up	X-Bar	MES	S-TCM-PT-PO-02; S-SPC-OCAP-005	QA	NS/NE/SD/OCAP/QRR
		N/A	Solderability Test	N/A	S-PES-PT-005; S-PEW-PT-020; S-QAW-PT-001;	>=95%	Solderability tester& Low power scope 10X-40X	5units 1x/descale type/machine/shift	Log Sheet	S-TCM-PT-QCPL-02A	S-TCM-PT-QCPL-02A	QA	NS/NE/SD/OCAP/QRR
		N/A	Rinse Effectiveness (contamination Test)	N/A	S-PES-PT-005 S-QAW-PT-001 S-QAW-QC-012	Refer to SPEC	Ion contamination tester	3strips：1X/machine/week	Log Sheet	S-TCM-PT-QCPL-02B	S-TCM-PT-QCPL-02B	QA	NS/NE/SD/QRR
Plating	Plating	N/A	Peeling test	N/A	S-QAW-PT-001	No Peeling	Bistoury	1unit, 1x/PKG type/machine/shift or chemical solution make up	Log Sheet	S-TCM-PT-QCPL-01	S-TCM-PT-PO-11	QA	NS/NE/SD/OCAP/QRR
	N/A	N/A	N/A	Chemical bath concentration analysis	S-PEW-PT-014 S-QAW-PT-002	Refer to SPEC	Chemical analysis	Chemical (for Pure Tin bath) 1x/bath/machine/day	Log Sheet	S-TCM-PT-QCPL-09 S-TCM-PT-QCPL-10A S-TCM-PT-QCPL-10B S-TCM-PT-QCPL-10C S-TCM-PT-QCPL-11A S-TCM-PT-QCPL-11B S-TCM-PT-QCPL-12	S-TCM-PT-PO-09	QA	NS/NE/SD/OCA P/QRR
								Lead: 1x/bath/machine/6month Cu/Fe/Ni:1x/bath/machine /6 months Carbon:1x/bath/machine /6months	Out source	NA	S-TCM-PT-PO-06		
Pb free bake(Option)	Oven	N/A	N/A	Temperature profile	S-PEW-PT-002	150℃*1Hour	Thermocouple meter	Continuous Monitoring	PC monitor	N/A	NA	PROD	SM/AE/NS/NE
			N/A	Time	S-PEW-PT-002	1Hour	Stopwatch	1x/Lot	Log Sheet	T-CARD	N.A	PROD	SM/AE/NS/NE

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process									
Marking	Marker	N/A	Visual /marking	N/A	T-card S-QAW-MK-001 S-PES-MK-001 S-PEW-MK-001	Refer to SPEC	Naked eye / magnifier (Min3X)	1 strips/buy off	Log Sheet	S-TCM-MK-PL-03 T-Card	S-TCM-MK-PO-01/02/04/05	QA	QRR/OCAP/SD
				NA	T-card S-PES-MK-001 S-PEW-MK-001	Refer to SPEC	Naked eye / magnifier (Min3X)	2 strips/3x/lot	T-Card	T-Card	S-TCM-MK-PO-01/02/04/05	PROD	SD/NS/NE/AE/100%I
		N/A	Laser depth (TQFP/LQFP/MSOP/TSOP/TSSOP/TSOT/QFN)	N/A	S-PES-MK-001 S-QAW-MK-001	0.012~0.050mm	Measuring scope	3ponits/2units/1x/buy-off	Log Sheet	S-TCM-MK-QCPL-01 S-TCM-MK-PL-03	S-TCM-MK-PO-07	QA	SD/QRR
		N/A	N/A	Parameter	S-V-MK-031 S-V-MK-032 S-V-MK-033 S-V-MK-034	Refer to SPEC	Reading	1x / marking change	Log Sheet	S-TCM-MK-PL-03	S-TCM-MK-PO-08	PROD	SD/NS/NE/AE
Form/ Singulation	Manual form; Auto shuttle system; Auto progressive system	N/A	Visual monitor	N/A	S-QAW-TF-001 S-PES-TF-001	Refer to SPEC	Low power scope (10X-40X)	1 stroke(min 5 unites), 4x/machine/shift or 1x/Buy off	Log sheet	S-TCM-TF-QCPL-01 Monitor System	S-TCM-TF-P0-01/02/04/06/07/08/09/10/12	QA	SD/NS/NE/OCAP/QRR
					S-PES-TF-001	Refer to SPEC	Visual (Naked eye & magnifier (Min3X) or Low power scope 10X-40X)	1 stroke, Assy lot size≥10000, 6X/lot Assy lot size<10000, 3X/lot Assy lot size≤315, 1x/lot	Log sheet	T-Card	S-TCM-TF-P0-01/02/04/06/07/08/09/10/12	PROD	NS/NE/OCAP/ 100%I
		N/A	N/A	Life time	S-EES-TF-004	Refer to SPEC	Auto record	Life time alarm/over	Monitor system	ERS monitor system	N/A	EE	SM/AE/NE/NS
		N/A	Dimension inspection	N/A	S-QAW-TF-001 S-PES-EVI-002/003/004/005/009	Refer to SPEC	Profile Project	5units, 1x/machine/shift 5units, 1x/Buy off	Log sheet	S-TCM-TF-QCPL-01	S-TCM-TF-P0-01/02/04/06/07/08/09/10/12	QA	AE/SD/NS/NE/OCAP/QRR
		☆	Lead Span	N/A	S-QAW-TF-001 S-PES-EVI-002/003/004/005/009	Refer to SPEC	Profile Project	5units, 1x/machine/shift	X bar & R	MES	S-SPC-OCAP-006	QA	AE/SD/NS/NE/OCAP/QRR
									Log sheet	S-TCM-TF-QCPL-01			
		☆	Coplanarity	N/A	S-QAW-TF-001 S-PES-EVI-002/003/	Refer to SPEC	Profile Project	5units, 1x/machine/shift	X bar & R	MES	S-SPC-OCAP-007	QA	AE/SD/NS/NE

Control Plan
控制计划

Qualification ☐ Mass Production ■ Customer ： ALL

Ass'y ■ Test ☐ Raw Material ☐ Package ： ALL

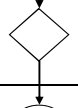
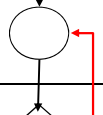
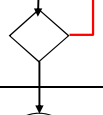
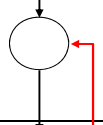
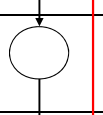
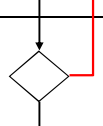
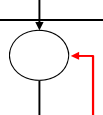
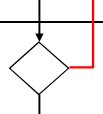
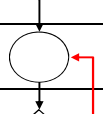
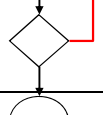
CFT Member ： Yin Jing(PE), Weihua Gu(PD), LinChun Zhang(QC), Fei R(EE), Gang Xu(PE), Bo Hu(CQE), Xiaobo Xing(PE)

Process	Machine/Tool for manufacturing	Special Characteristics	Characteristic		Spec No.	Product/Process Criteria	Measuring methods	Sampling Plan Size/Freq.	Analysis Method	Log No	OCAP No.	Rep	Reaction Plan
			Product	Process	004/005/009				Log sheet	S-TCM-TF-QCPL-01			/OCAP/QRR
EVI	N/A	N/A	Visual Inspection	N/A	S-PES-EVI-001/011 S-PEW-EVI-001	Refer to SPEC	Magnifier(Min3X)/ Low power scope (10X-40X)	5% or 2000units ,1X/lot	Log sheet	MES	S-TCM-EVI-P0-01/02	PROD	NS/NE
					S-PES-EVI-002/003/004/005/009/010/011 S-PEW-EVI-001	Refer to SPEC	Naked eyes/ Magnifier(Min3X)/ Low power scope (10X-40X)	100% Inspection	Log sheet	MES	S-TCM-EVI-P0-01/02	PROD	NS/NE
					S-PES-EVI-001/002/003/004/005/009/010/011 S-QAW-EVI-001	Refer to SPEC	Magnifier(Min3X)/ Low power scope (10X-40X)	AQL 0.04%1X/lot, (ACC/REJ:0/1)	Log sheet	MES	S-TCM-EVI-P0-01	QA	NS/NE/QRR
Packing	Incoming check	N/A	Q'ty/tube/plugial/marking	N/A	S-PES-IPK-003 S-PES-IPK-017 S-PES-IPK-023	Refer to T-card	Visual (Naked eyes)	Tube ALL / Plug: ALL; Qty: ALL;Marking: Partial tube: 1 unit; Full tube: 1 unit/ tube；2 tubes/lot	Log sheet	MES	S-TCM-PK-PO-03/04	PROD	NS/NE
	Box	NA	Box type/Q'ty	N/A	S-PES-IPK-003 S-PES-IPK-017 S-PES-IPK-023	Refer to T-card	Reading	All	Log sheet	MES	S-TCM-PK-PO-05	PROD	NS/NE
	Label	NA	Label format / quality	N/A	S-PES-IPK-003 S-PES-IPK-023 S-V-IPK-001	Refer to spec.	Check with T-card and visual inspection	All	Log sheet	MES	S-TCM-PK-PO-01	PROD	NS/NE
	N/A	N/A	Visual gate	N/A	S-QAW-IPK-001 S-PES-IPK-017 S-PES-IPK-023	Refer to T-card	Visual (Naked eyes)	1 tube or tray/1 box per 5 boxes	Log sheet	MES	S-TCM-PK-PO-03/04	QA	NS/NE/QRR

NOTE : REACTION PLAN : A.E. =ADJUST EQUIPMENT; N.S.= NOTIFY SUPERVISOR; N.E. = NOTIFY ENGINEER; S.D.= SHUTDOWN; 100%I = 100% INSPECTION; OCAP = Out Of Control Action Plan; QRR = Quality Rejection Report

QRR procedure is applied to take corrective action of nonconforming product during QA monitor and inspect at production line. Each department shall take corrective action based on process OCAP and related procedure.

☆ means special characteristics.

NO	FLOW CHART	PROCESS	CONTROL ITEM (Para./Criteria)	MAN	MACHINE	MATERIAL	METHOD	SAMPLE		
								SIZE	Acc/Rej	FREQ.
1		**Incoming**	Receiving document check & No. of box check	PC	Naked Eye	PKG	GID-O001	100%	-	Every Shipment
2		**IQC**	Visual defects . +/- CV, Ball defects, Marking defects, Chip,crack etc	QA Inspector	Naked Eye or 3~10X Scope	PKG	GIC-A001 GVC-C001	AQL 0.065% II 200ea/Lot	0/1	Every Lot
3		**Final Test**	Electrical test .Room Temp	Operator	Tester Handler Load board	PKG	GFB-R001 GFC-C003	100%	**Hold Limit** **Customer Requiment**	Every Lot
4		**QA E/L Test** ***Cust Opt**	Electrical test .Room Temp	QA Inspector	Tester Handler Load board	PKG	GFC-C001	AQL 0.065% II 200ea/Lot	0/1	Every Lot
5		**LIS** **(Vision)**	Package dimension . Ball placement/coplanarity . Missing/Double ball, etc	Operator	Vision System	PKG	GVC-C007	100%	**Hold Limit** A : Yld ≥ 99.0% R : Yld < 99.0%	Every Lot
6		**Bake** ***Cust Opt**	Temp : 125 +/- 5'C Time : 6 hours +15/-0 min Window time : =< 24 hours	Operator	Bake oven	PKG	GAC-E001	-	Temp/ time display Condition	Every Lot
7		**QVI**	Visual defects . +/- CV, Ball defects, Marking defects, Chip,crack etc Visual defects	QA Inspector	Naked Eye or 3~10X Scope	PKG	GVC-C001	AQL 0.065% II 200ea/Lot	0/1	Every Lot
8		**Tape & Reel** ***Cust Opt**	. Label, Sealing condition	Operator	Tape&Reel Handler Barcod System	PKG	GPC-C004	100%	0/1	Every reel
9		**RQC**	. Label, Sealing condition	QA Inspector	Naked Eye Barcod System	PKG	GPC-C001	1Reel/1Lot	0/1	Every Lot
9		**Packing**	. Label, Packing condition	Operator	Vacuum sealer	PKG	GPC-C002	100%	0/1	Every reel or Box
9		**QPI**	. Label, Packing condition	QA Inspector	Naked Eye Barcod System	PKG	GPD-R002	100%	0/1	Every Lot
10		**Shipping**	Visual defects . Label, Packing condition	Operator	Naked Eye	PKG	GIC-R001	100%	0/1	Every reel or Box

7. Packing Information

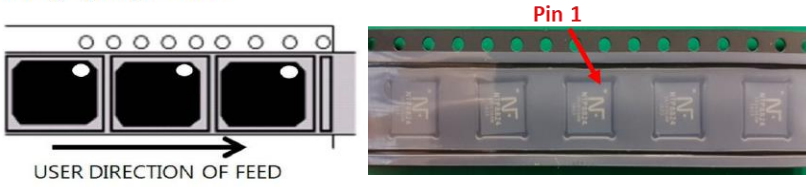
Packing Information

1. Minimum Packing Quantity

DEVICE NAME	Package	Q'ty / Reel	PIN 1	MBB	Inner Box	Outer Box
NTP8824	QFN 6X6	3,000 Unit/1Reel	Top Right	3,000 Unit	1 Reel / 3,000 Unit	18,000 Unit

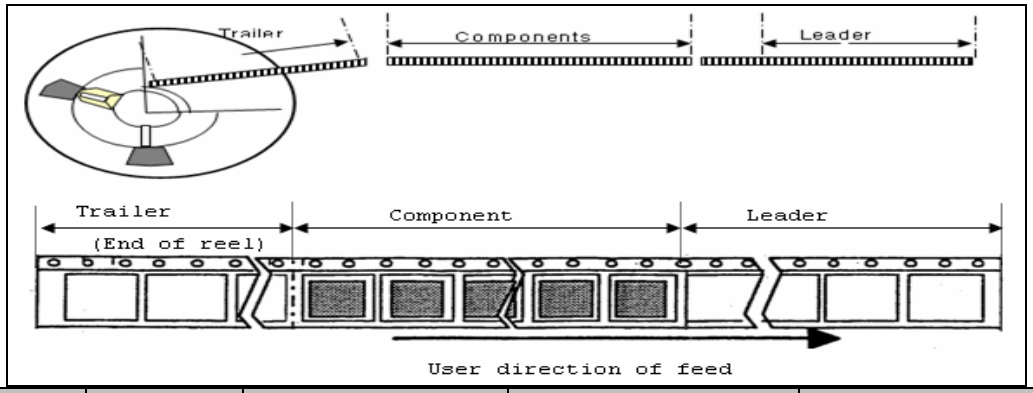
2. Pin1 Orientation

Package pin position



Pin1 orientation: "Right Top"

3. Leader and Trailer

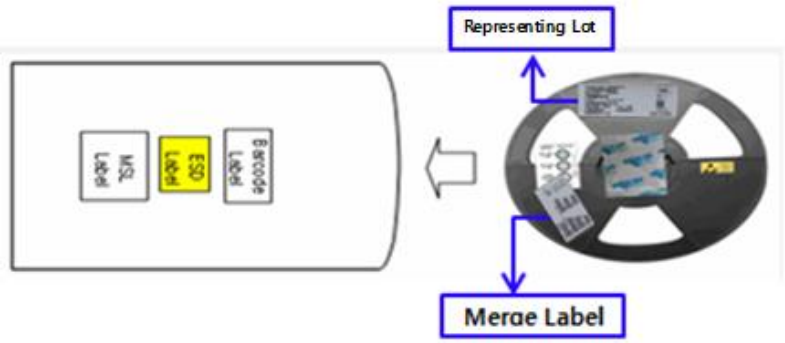


DEVICE NAME	Package	Trailer	Components	Leader
NTP8824	QFN 6X6	180mm	3,000Units	410mm

4. Packing Process (NTP8824)

4.1. Reel (HIC : 5%, 10%, 60%)

4.1.1 Guard Band Form Pad



4.2. Vacuum packing

– Merge Label Attach on the Reel / AL Bag / Inner Box separately (For Merge Reel)

4.3. Inner Box Packing

– Merge Label Attach on the Reel / AL Bag / Inner Box separately (For Merge Reel)

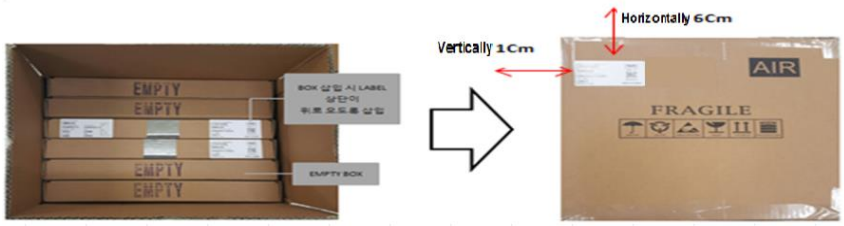
4.3.1 Inner Box Label (Included one more Label in the inner box)

(Normal Inner Box)

(Merge Inner Box)

4.4. Outer Box Packing (Attached the Inner Box Labels of the box) Vertically Horizontally

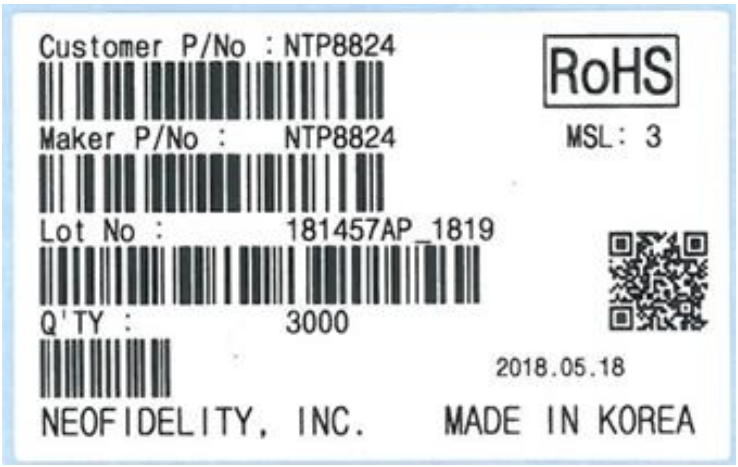
4.4.1 Outer Box Label : Attached Label 6cm away from the top / 1cm away from the left side



Attach 1

[Bar Code Label]

1) NTP8824 (80*50mm) Standard LABEL

REEL/MBB/Inner box & Outer box


ITEM	DESCRIPTION	Remark
Customer P/No	Device Name	Device: NTP8824 / Device No: NTP8824
Maker P/N	Device Name	Device: NTP8824 / Device No: NTP8824
Lot No	**Acceptable for 2 Lots merge** Representing Lot should be shown	예) AAAA(5,000ea) / B(1,000ea) -> AAAA
DATE CODE	**Week Code on Chip Marking**	
Q'TY	**Total Qty**	
Seal Date	**Packing Date**	
RoHS Mark	RoHS Marked on Top Right Side	
Level	**MSL Information**	**MSL : 3** **Hours : 168** **Temp : 260**
Country of Origin	"MADE IN KOREA"	

2) NTP8824 (100*50mm) Combine LABEL

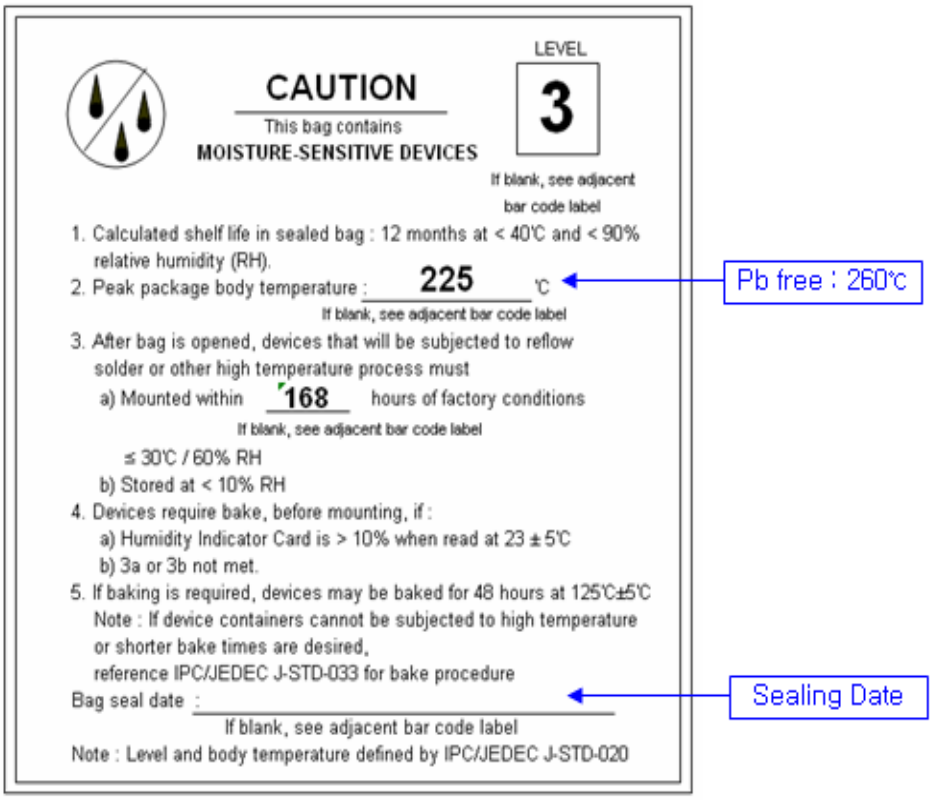
REEL/MBB/Inner box & Outer box


ITEM	DESCRIPTION	Remark
Device No	Device Name	Device: NTP8824 / Device No: NTP8824
Lot No	Acceptable for 2 Lots merge Each Lot No should be shown Ex) For Merge Lot : AAAA BBBB	Representing Lot No. Should be specified firstly
Date Code	Week Code on Chip Marking 2 Week Codes of each lot should be shown Ex) 1612 1611	1612 / 1611 (If Both Lots Week Code are same, 2 Week Codes should be shown)
Q'TY	Each Lot's Qty should be shown separately	Ex) 2,000 / 1,000
MSL	MSL Information MSL : 3 Hours : 168 Temp : 260	
Seal Date	Packing Date	

Attach 2

[Moisture Sensitive Caution Label & ESD Caution Label and Pb Free Label]

1) Moisture Sensitive Caution Label

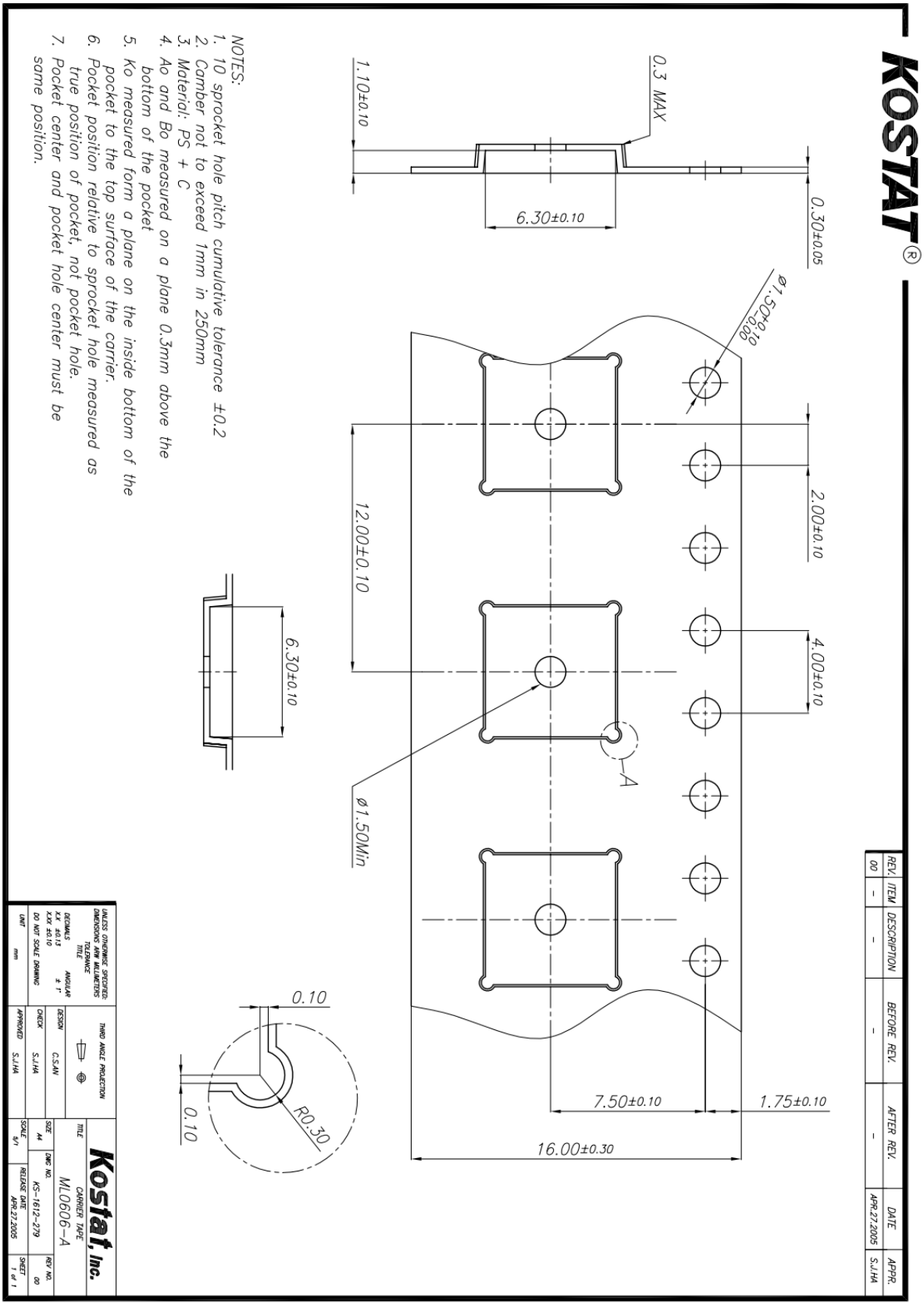


2) Humidity Indicator Card(3Dots 5%-10%-60%)

3) Power dry_sorb(Desiccant) : 50g

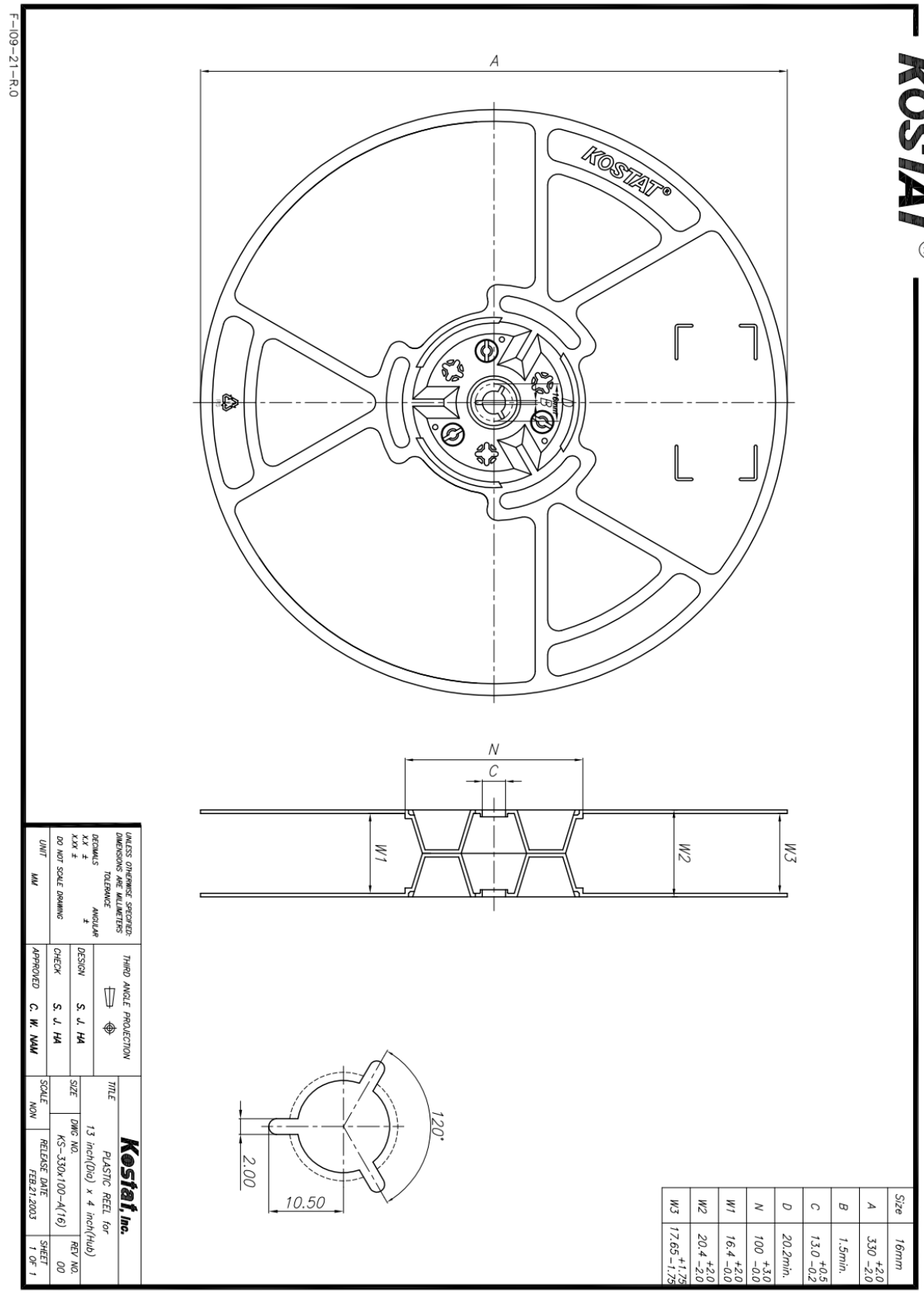
Attach 3

[Carrier Tape Drawing]



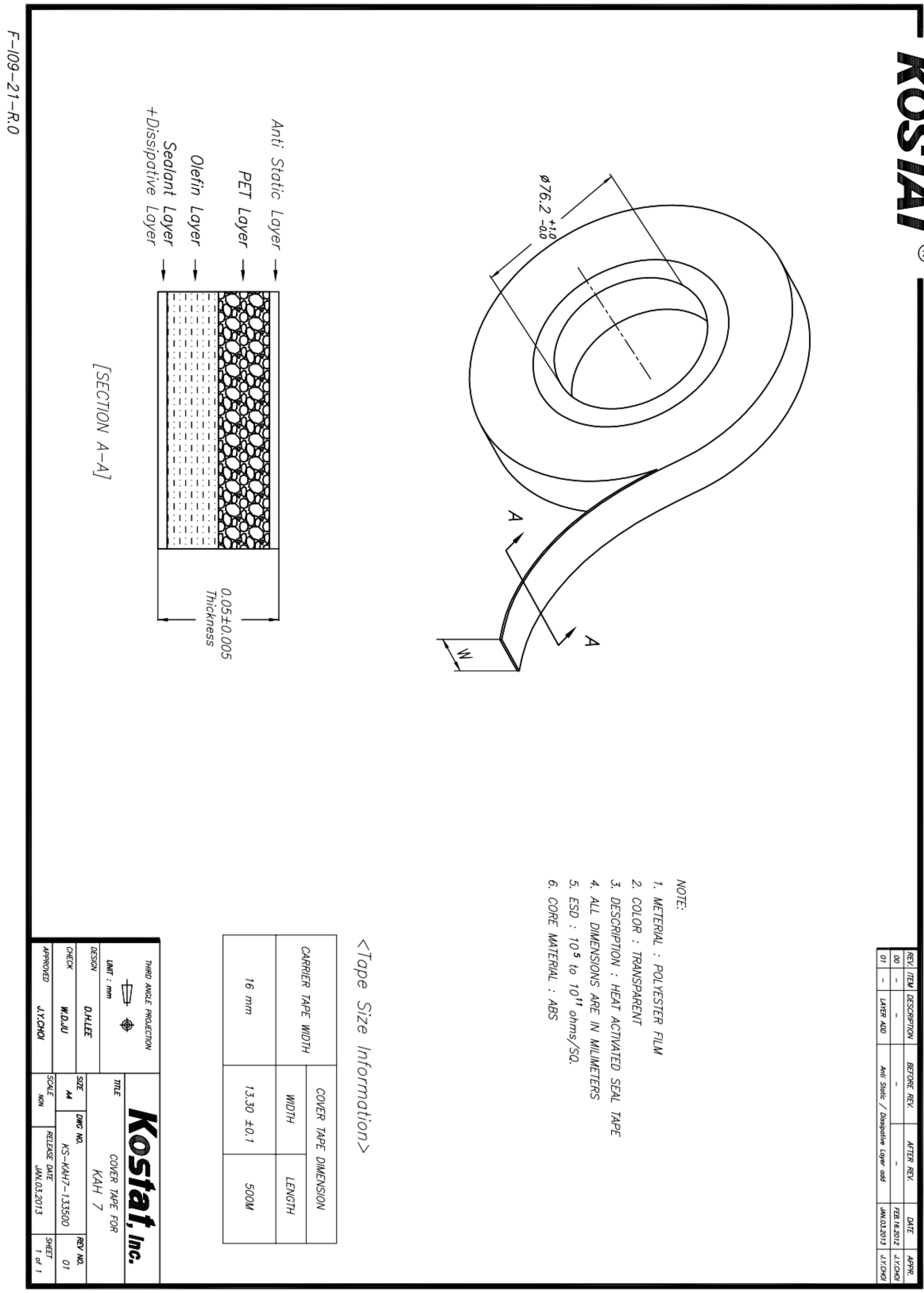
Attach 4

[Reel Drawing]



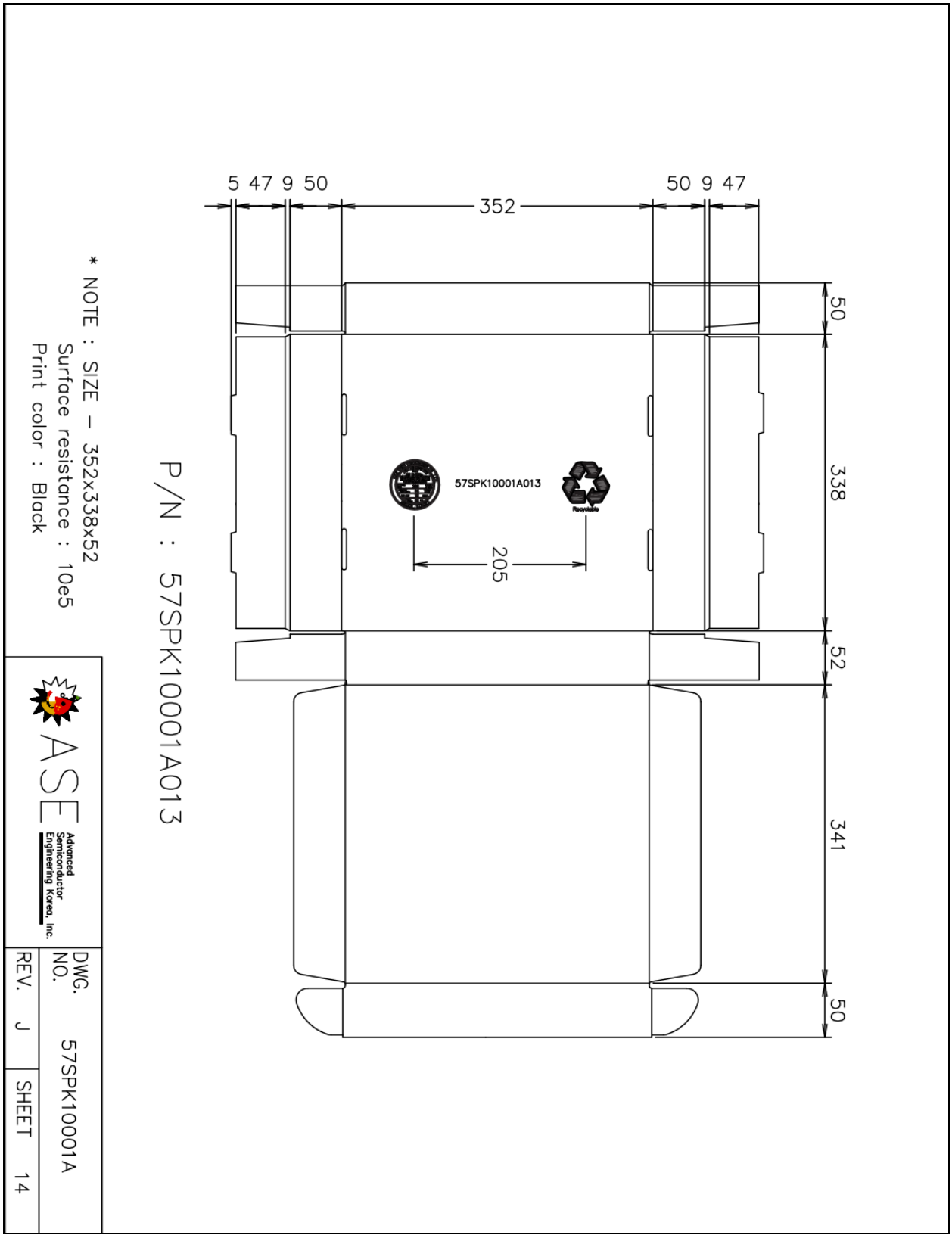
Attach 5

[Cover Tape Drawing]



Attach 6

[Inner Box Drawing] _ Size : 352(L)x338(W)x52(D)



Attach 7

[Outer Box Drawing] _ Size : 375(L)x335(W)x362(D)