NTQD6968N

Power MOSFET

7.0 A, 20 V, Common Drain, Dual N−Channel, TSSOP−8

Features

- Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- 3 mm Wide TSSOP−8 Surface Mount Package
- High Speed, Soft Recovery Diode
- TSSOP−8 Mounting Information Provided
- Pb−Free Package is Available

Applications

- Battery Protection Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	20	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±12	Vdc
Drain Current − Continuous @ T_A 25°C (Note 1) − Continuous @ T_A 70°C (Note 1) − Pulsed (Note 3)	 I_D I_D I_{DM}	 7.0 5.6 20	Adc
Total Power Dissipation @ T_A 25°C (Note 1)	P_D	1.81	W
Drain Current − Continuous @ T_A 25°C (Note 2) − Continuous @ T_A 70°C (Note 2) − Pulsed (Note 3)	 I_D I_D I_{DM}	 6.2 4.9 18	Adc
Total Power Dissipation @ T_A 25°C (Note 2)	P_D	1.39	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Thermal Resistance − Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	$R_{\theta JA}$	 69 90	°C/W
Maximum Lead Temperature for Soldering Purposes for 10 seconds	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted onto a 2″ square FR−4 Board (1 in sq, 2 oz. Cu 0.06″ thick single sided), t ≤ 10 sec.
2. Mounted onto a 2″ square FR−4 Board (1 in sq, 2 oz. Cu 0.06″ thick single sided), Steady State.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

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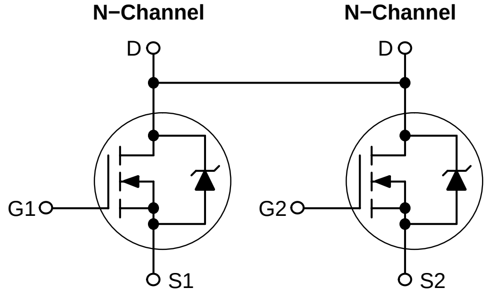
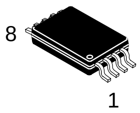
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	17 mΩ @ 4.5 V	7.0 A



MARKING DIAGRAM & PIN ASSIGNMENT



TSSOP−8
CASE 948S
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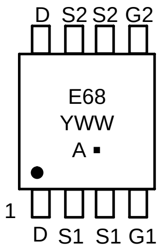

E68	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTQD6968N	TSSOP−8	100 Units / Rail
NTQD6968NR2	TSSOP−8	4000/Tape & Reel
NTQD6968NR2G	TSSOP−8 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 −	 − 16	 − −	Vdc mV/°C
Zero Gate Voltage Collector Current (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 25°C) (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 − −	 − −	 1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ±12 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	 −	 −	 ±100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 0.6 −	 0.75 3.0	 1.2 −	Vdc mV/°C
Static Drain−to−Source On−State Resistance (V_{GS} = 4.5 Vdc, I_D = 7.0 Adc) (V_{GS} = 2.5 Vdc, I_D = 7.0 Adc) (V_{GS} = 2.5 Vdc, I_D = 3.5 Adc)		$R_{DS(on)}$	 − − −	 0.017 0.022 0.022	 0.022 0.030 0.030	Ω
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 7.0 Adc)		g_{FS}	−	19.2	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	630	−	pF
Output Capacitance		C_{oss}	−	260	−	
Transfer Capacitance		C_{rss}	−	95	−	
SWITCHING CHARACTERISTICS (Notes 4 and 5)						
Turn−On Delay Time	(V_{DD} = 16 Vdc, I_D = 7.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	8.0	−	ns
Rise Time		t_r	−	25	−	
Turn−Off Delay Time		$t_{d(off)}$	−	60	−	
Fall Time		t_f	−	65	−	
Gate Charge	(V_{DS} = 16 Vdc, V_{GS} = 4.5 Vdc, I_D = 7.0 Adc)	Q_{tot}	−	12.5	17	nC
		Q_{gs}	−	1.0	−	
		Q_{gd}	−	5.0	−	
BODY−DRAIN DIODE RATINGS (Note 4)						
Forward On−Voltage	(I_S = 7.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	−	0.82	1.2	Vdc
Reverse Recovery Time	(I_S = 7.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	−	35	−	ns
		t_a	−	15	−	
		t_b	−	20	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.02	−	μC

4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
5. Switching characteristics are independent of operating junction temperature.

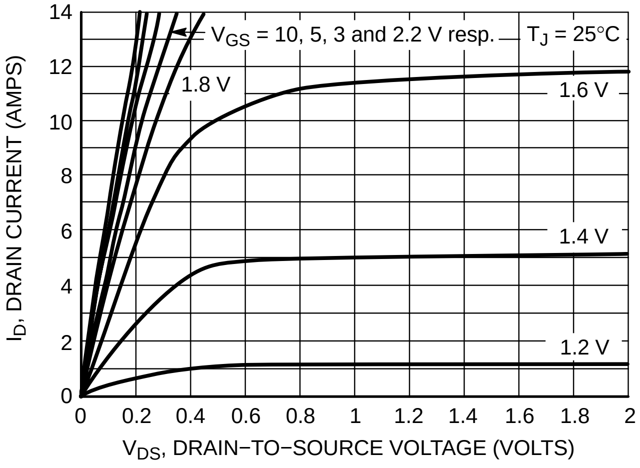

Figure 1. On−Region Characteristics

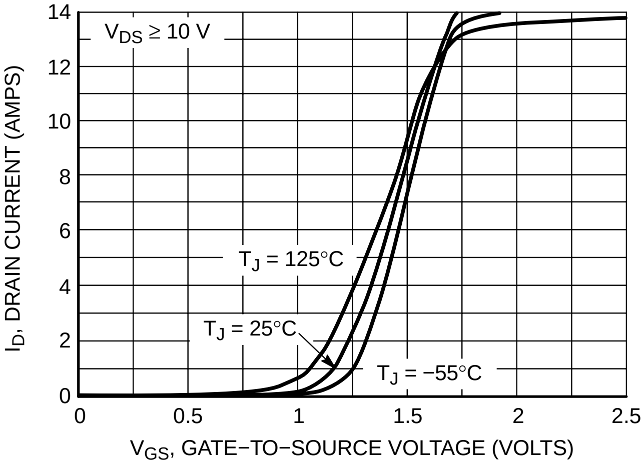

Figure 2. Transfer Characteristics

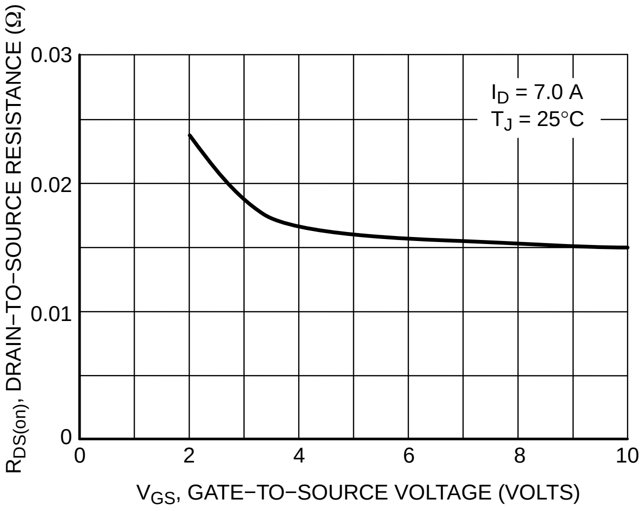

Figure 3. On−Resistance versus Gate−to−Source Voltage

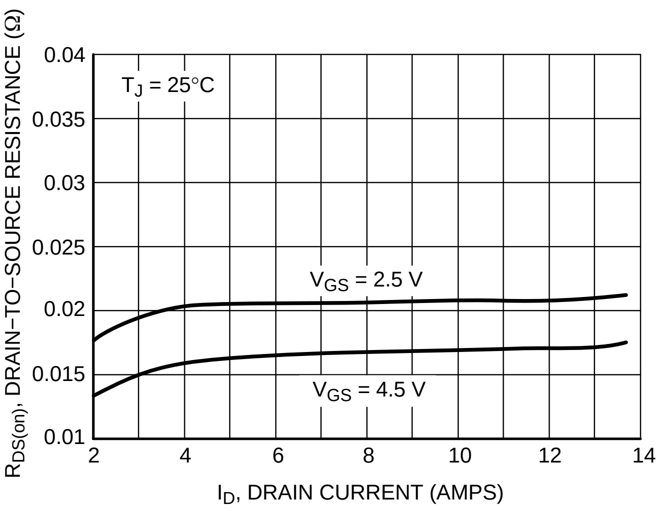

Figure 4. On−Resistance versus Drain Current and Gate Voltage

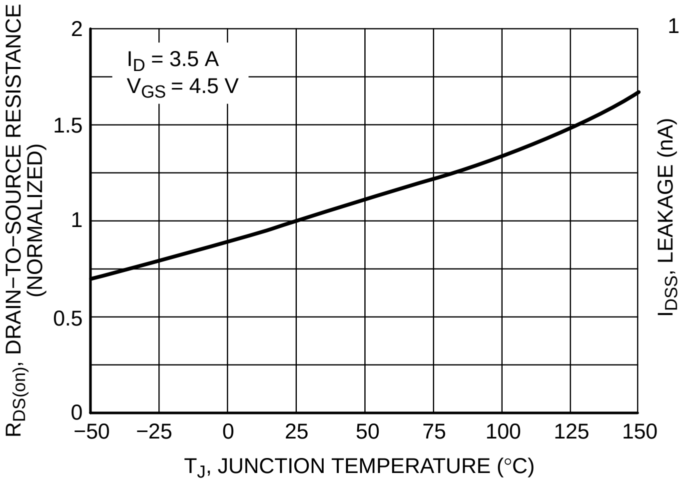

Figure 5. On−Resistance Variation with Temperature

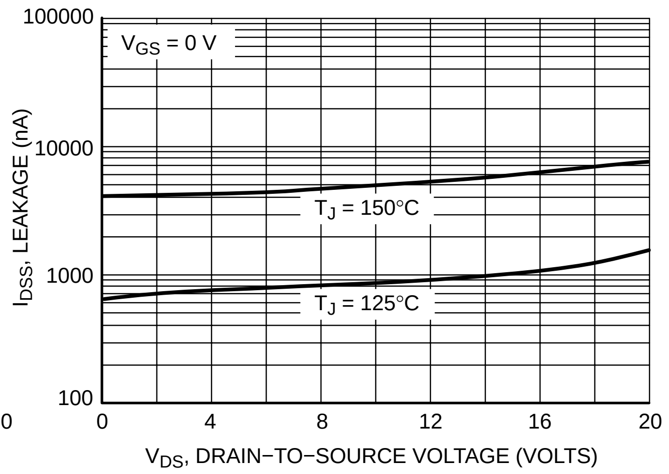

Figure 6. Drain−to−Source Leakage Current versus Voltage

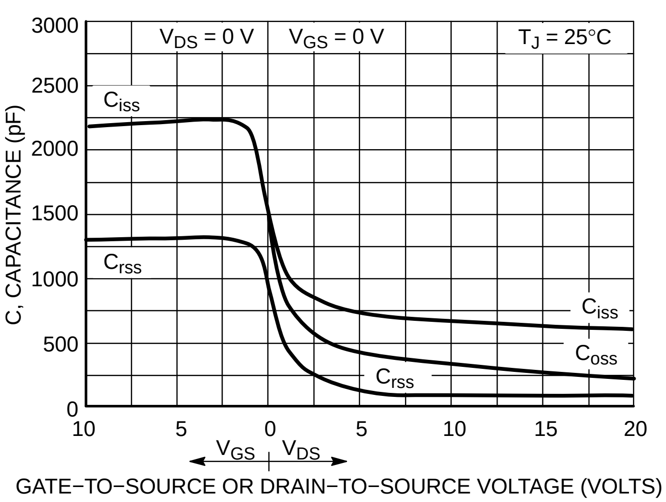

Figure 7. Capacitance Variation

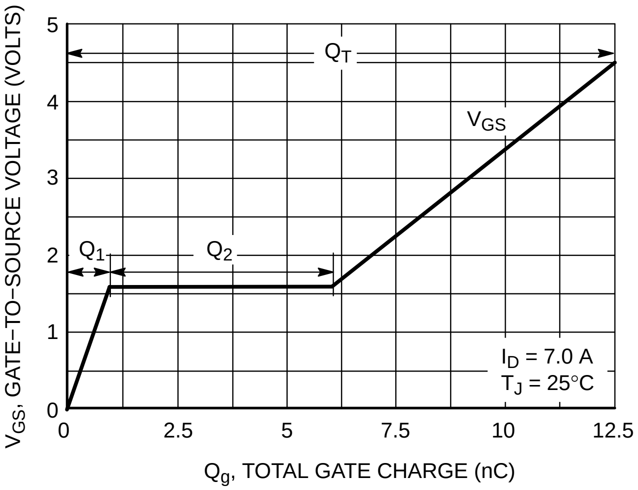

Figure 8. Gate−to−Source Voltage versus Total Charge

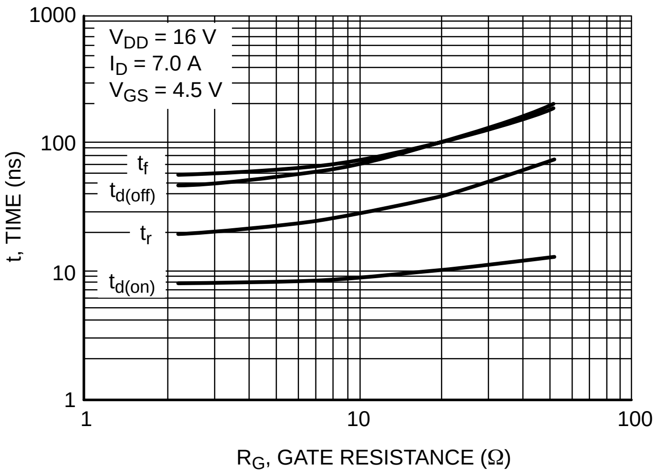

Figure 9. Resistive Switching Time Variation versus Gate Resistance

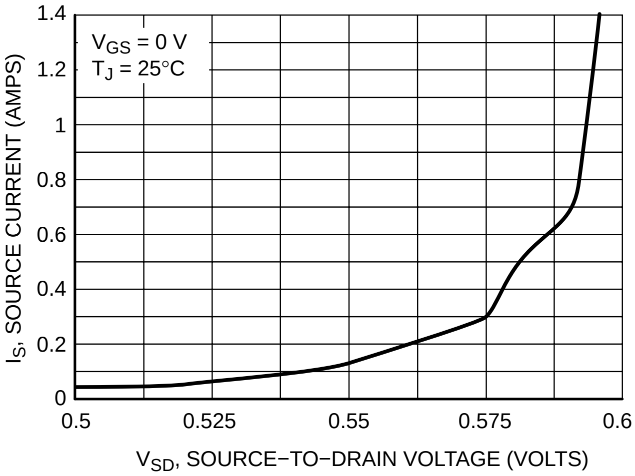

Figure 10. Diode Forward Voltage versus Current

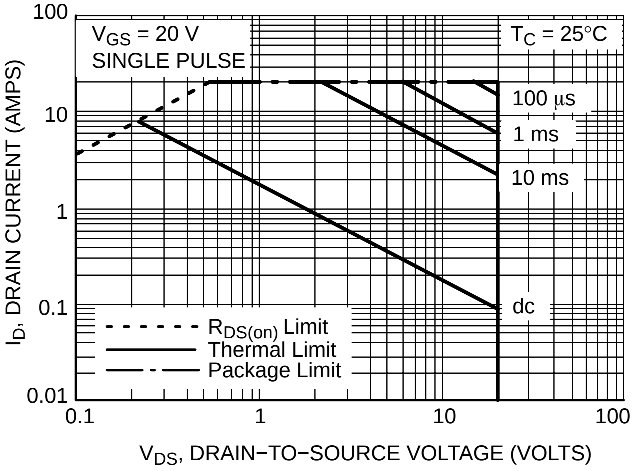

Figure 11. Maximum Rated Forward Biased Safe Operating Area

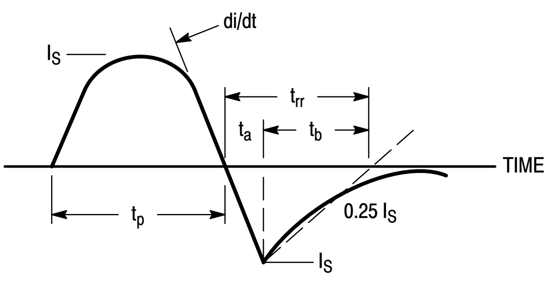

Figure 12. Diode Reverse Recovery Waveform

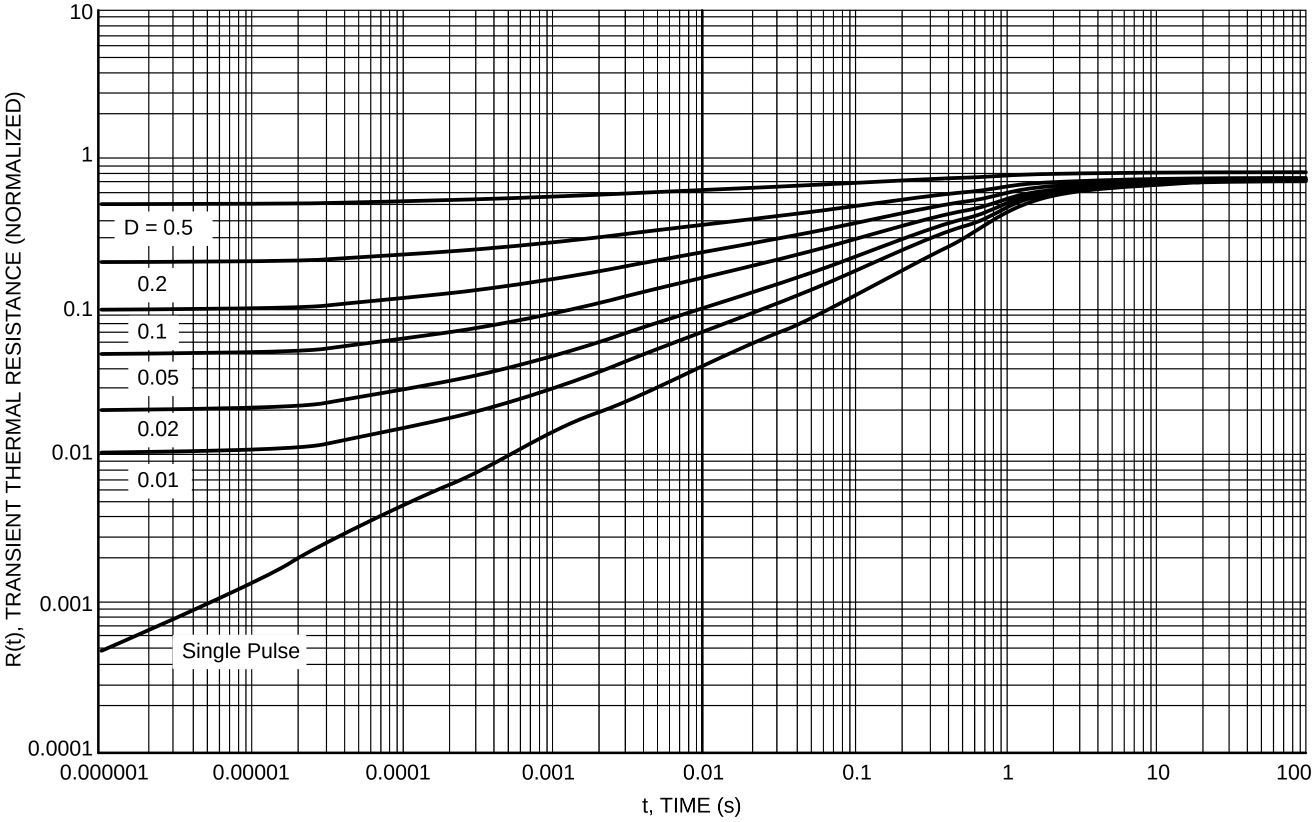

Figure 13. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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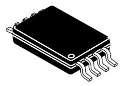
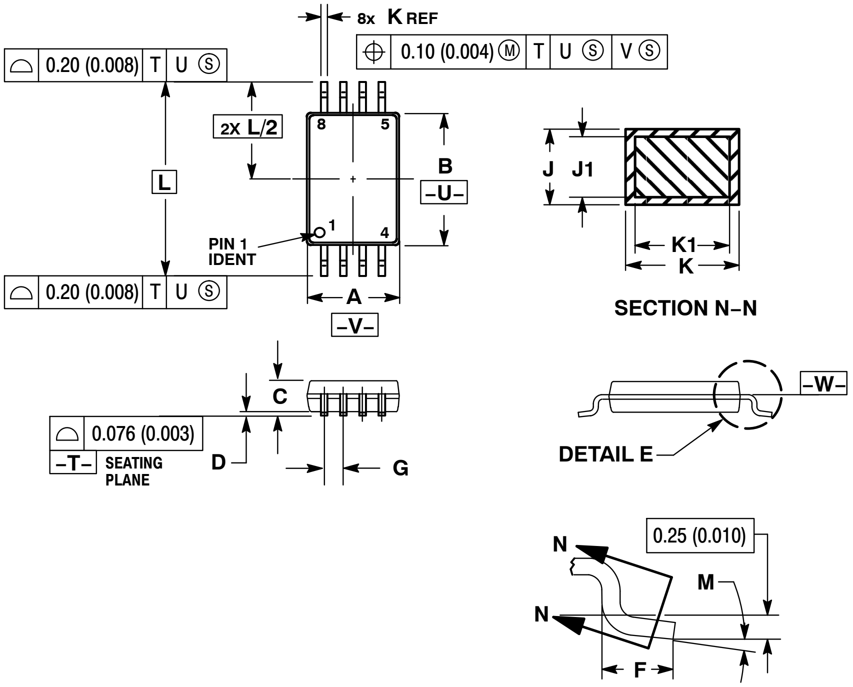


SCALE 2:1

TSSOP−8
CASE 948S−01
ISSUE C

DATE 20 JUN 2008

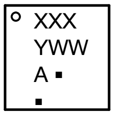


DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXX	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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NEW STANDARD:		
DESCRIPTION:	**TSSOP−8**	**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION.	18 APR 2000
A	ADDED MARKING DIAGRAM INFORMATION. REQ. BY V. BASS.	13 JAN 2006
B	CORRECTED MARKING DIAGRAM PIN 1 LOCATION AND MARKING. REQ. BY C. REBELLO.	13 MAR 2006
C	REMOVED EXPOSED PAD VIEW AND DIMENSIONS P AND P1. CORRECTED MARKING INFORMATION. REQ. BY C. REBELLO.	20 JUN 2008

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