

# NTR1P02L, NVTR01P02L

## Power MOSFET

**-20 V, -1.3 A, P-Channel  
SOT-23 Package**

These miniature surface mount MOSFETs low  $R_{DS(on)}$  assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

### Features

- Low  $R_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature SOT-23 Surface Mount Package Saves Board Space
- NVTR Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Pb-Free and Halide-Free Packages are Available

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-20	V
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 12$	V
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Pulsed Drain Current ( $t_p \leq 10 \mu\text{s}$ )	$I_D$ $I_{DM}$	-1.3 -4.0	A A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	400	mW
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Thermal Resistance - Junction-to-Ambient	$R_{\theta JA}$	300	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

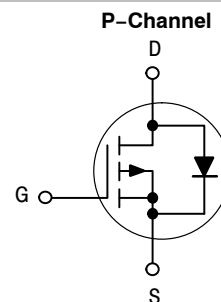
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



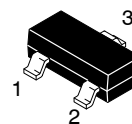
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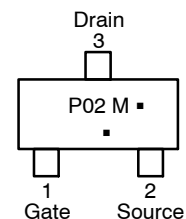
$V_{(BR)DSS}$	$R_{DS(on)}$ Max	$I_D$ Max
-20 V	220 m $\Omega$ @ -4.5 V	-1.3 A



### MARKING DIAGRAM & PIN ASSIGNMENT



**SOT-23  
CASE 318  
STYLE 21**



P02 = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)  
\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTR1P02LT1G	SOT-23 (Pb-Free)	3000 Tape & Reel
NTR1P02LT3G	SOT-23 (Pb-Free)	10,000 Tape & Reel
NVTR01P02LT1G	SOT-23 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTR1P02L, NVTR01P02L

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$(V_{GS} = 0\text{ V}, I_D = -10\ \mu\text{A})$	$V_{(BR)DSS}$	-20			V
Zero Gate Voltage Drain Current	$(V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V})$ $(V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C})$	$I_{DSS}$			-1.0 -10	$\mu\text{A}$
Gate-Body Leakage Current	$(V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V})$	$I_{GSS}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 1)

Gate Threshold Voltage	$(V_{DS} = V_{GS}, I_D = -250\ \mu\text{A})$	$V_{GS(th)}$	-0.7	-1.0	-1.25	V
Static Drain-to-Source On-Resistance	$(V_{GS} = -4.5\text{ V}, I_D = -0.75\text{ A})$ $(V_{GS} = -2.5\text{ V}, I_D = -0.5\text{ A})$	$r_{DS(on)}$		0.140 0.200	0.22 0.35	$\Omega$

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = -5.0\text{ V})$	$C_{iss}$		225		pF
Output Capacitance	$(V_{DS} = -5.0\text{ V})$	$C_{oss}$		130		
Transfer Capacitance	$(V_{DS} = -5.0\text{ V})$	$C_{rss}$		55		

### SWITCHING CHARACTERISTICS (Note 2)

Turn-On Delay Time	$(V_{GS} = -4.5\text{ V}, V_{DD} = -5.0\text{ V}, I_D = -1.0\text{ A}, R_L = 5.0\ \Omega, R_G = 6.0\ \Omega)$	$t_{d(on)}$		7.0		ns
Rise Time		$t_r$		15		
Turn-Off Delay Time		$t_{d(off)}$		18		
Fall Time		$t_f$		9		
Total Gate Charge	$(V_{DS} = -16\text{ V}, I_D = -1.5\text{ A}, V_{GS} = -4.5\text{ V})$	$Q_T$		3.1		nC

### SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Current		$I_S$			-0.6	A
Pulsed Current		$I_{SM}$			-0.75	
Forward Voltage (Note 2)	$(V_{GS} = 0\text{ V}, I_S = -0.6\text{ A})$	$V_{SD}$			-1.0	V
Reverse Recovery Time	$(I_S = -1.0\text{ A}, V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s})$	$t_{rr}$		16		ns
		$t_a$		11		
		$t_b$		5.5		
Reverse Recovery Stored Charge		$Q_{RR}$		8.5		nC

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
2. Switching characteristics are independent of operating junction temperature.

# NTR1P02L, NVTR01P02L

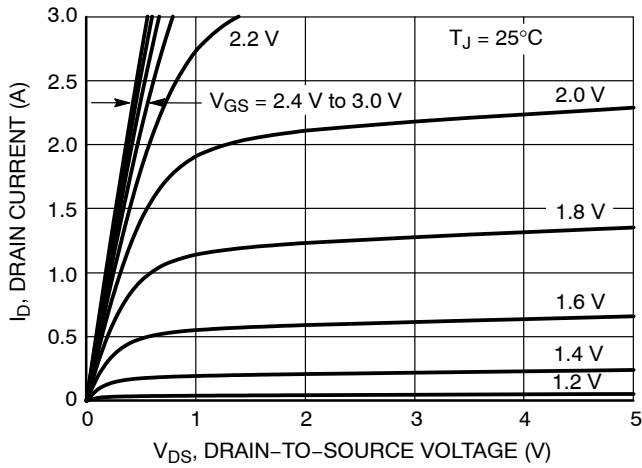


Figure 1. On-Region Characteristics

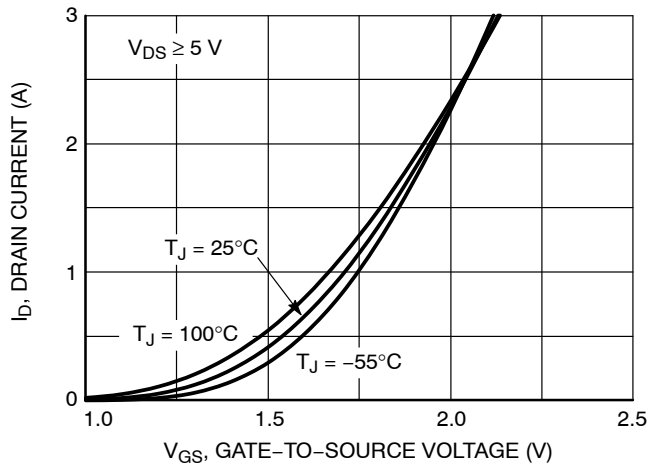


Figure 2. Transfer Characteristics

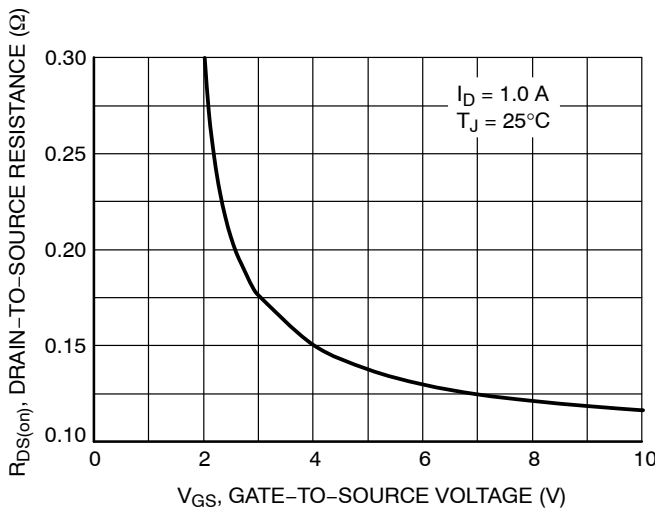


Figure 3. On-Resistance vs. Gate-to-Source Voltage

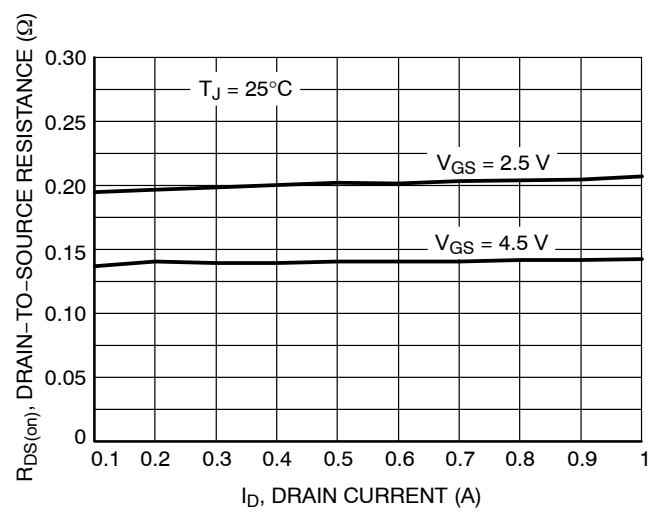


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

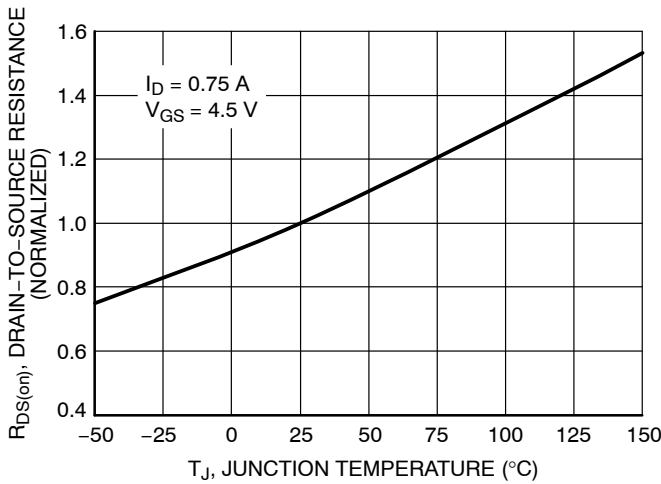


Figure 5. On-Resistance Variation with Temperature

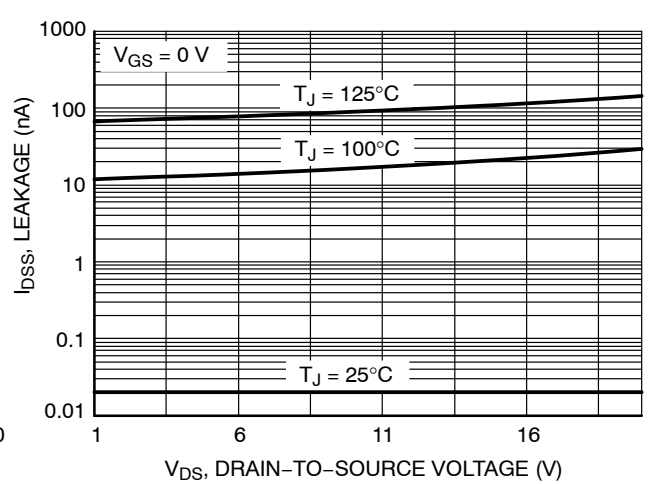


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTR1P02L, NVTR01P02L

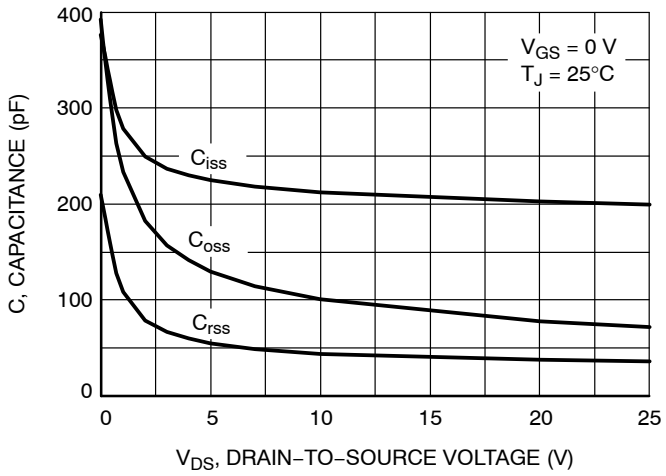


Figure 7. Capacitance Variation

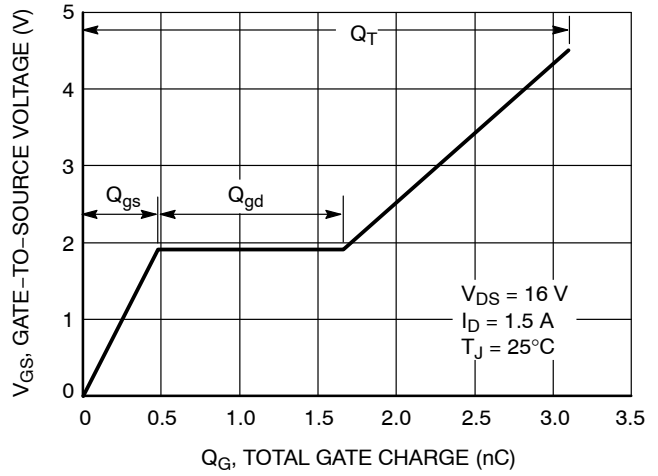


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

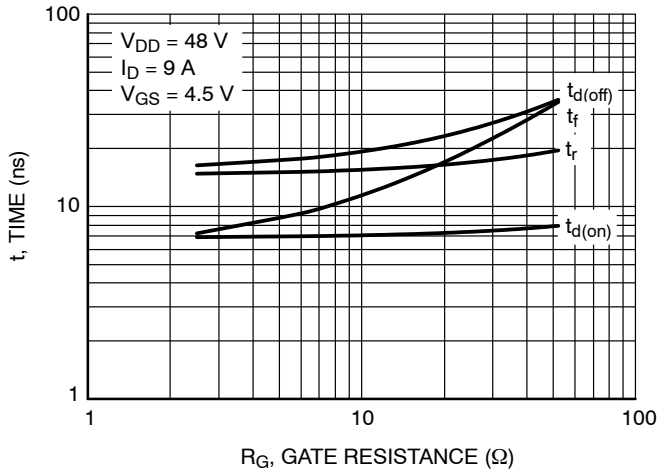


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

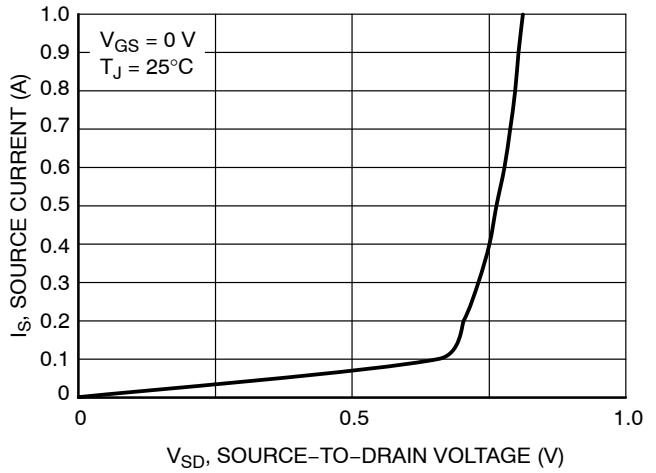


Figure 10. Diode Forward Voltage vs. Current

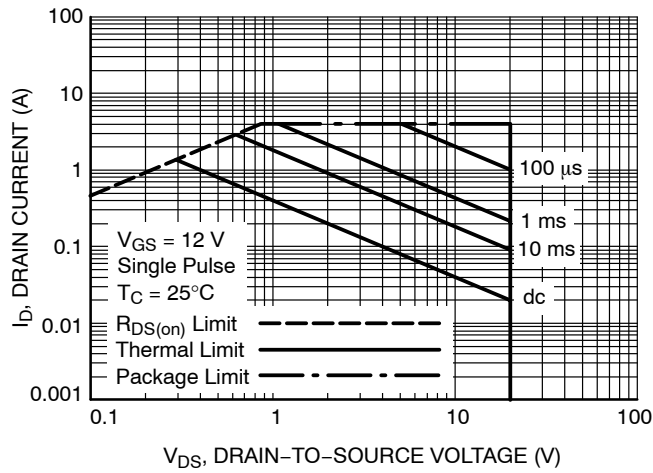
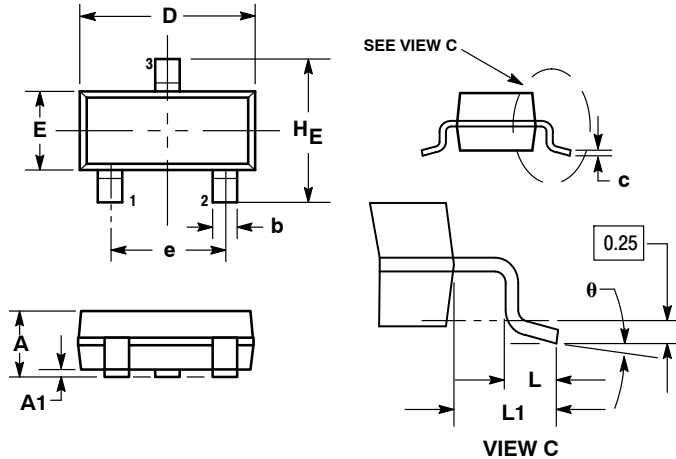


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTR1P02L, NVTR01P02L

## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AP



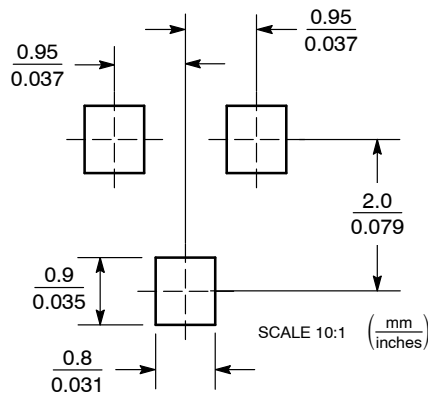
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 21:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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