

**ARM Cortex<sup>®</sup>-M0**  
**32-bit Microcontroller**

**NuMicro<sup>®</sup> Family**  
**NUC121/125 Series**  
**Datasheet**

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## 1 GENERAL DESCRIPTION

The NuMicro® NUC121/125 series is a 32-bit Cortex®-M0 microcontroller with USB 2.0 Full-speed device, a 12-bit ADC and 4 sets of 6-channel BPWM. The NUC121/125 series provides the high 50 MHz operating speed, 8 Kbytes SRAM, 8 USB endpoints and 24 channels of BPWM, which make it powerful in USB communication and data processing. The NUC121/125 series is ideal for industrial control, consumer electronics, and communication system applications such as printers, touch panel, gaming keyboard, gaming joystick, USB audio, PC peripherals, and alarm systems.

The NUC121/125 series runs up to 50 MHz and supports 32-bit multiplier, structure NVIC (Nested Vector Interrupt Control), dual-channel APB and PDMA (Peripheral Direct Memory Access) with CRC function. Besides, the NUC121/125 series is equipped with 32 Kbytes Flash memory, 8 Kbytes SRAM, and 4 Kbytes loader ROM for the ISP. It operates at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40°C ~ +105°C. It is also equipped with plenty of peripheral devices, such as 8-channel 12-bit ADC, USCI, UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S, USB 2.0 FS device, and offers low-voltage reset and Brown-out detection, PWM (Pulse-width Modulation), capture and compare features, four sets of 32-bit timers, Watchdog Timer, and internal RC oscillator. All these peripherals have been incorporated into the NUC121/125 series to reduce component count, board space and system cost.

Additionally, the NUC121/125 series is equipped with ISP (In-System Programming), IAP (In-Application-Programming) and ICP (In-Circuit Programming) functions, which allows the user to update the program under software control through the on-chip connectivity interface, such as SWD, UART and USB. Also all series support SPROM. Moreover, the NUC125 support Voltage Adjustable Interface with individual I/O (1.8V-5.5V) for saving additional cost on adjusting the interface voltage difference of peripheral components.

### 1.1 Key Features Support Table

\* USCI can be set to UART, I<sup>2</sup>C or SPI

| Product Line | USBD | USCI | UART | I <sup>2</sup> C | SPI/ I <sup>2</sup> S | Timer | BPWM | ADC |
|--------------|------|------|------|------------------|-----------------------|-------|------|-----|
| NUC121       | 1    | 1    | 1    | 2                | 1                     | 4     | 24   | 12  |
| NUC125       | 1    | 1    | 1    | 2                | 1                     | 4     | 23   | 11  |

Table 1.1-1 Key Features Support Table

The NuMicro® NUC121/125 series is suitable for a wide range of applications such as:

- USB Keyboard / Mouse
- Gaming - Joystick
- Industrial Automation
- Home Automation
- VR peripheral application
- USB audio
- Alarm system

## 2 FEATURES

### 2.1 NuMicro® NUC121/125 Features

- Core
  - ARM® Cortex®-M0 core running up to 50 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 4 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
  - Supports Serial Wire Debug(SWD) with 2 watch-points/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
  - Supports 32 KB application ROM (APROM)
  - Supports 4.5 KB Flash for loader (LDROM)
  - Supports 512 bytes Security Protection Rom (SPROM)
  - Supports 12 bytes User Configuration block to control system initiation
  - Supports Data Flash with configurable memory size
  - Supports 512 bytes page erase for all embedded flash
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory
  - Supports CRC-32 checksum calculation function
  - Supports flash all one verification function
  - Hardware external read protection of whole flash memory by Security Lock Bit
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 8 KB embedded SRAM
  - Supports byte-, half-word- and word-access
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 5 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports single and burst transfer type
  - Supports Normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports incrementing mode for the source and destination address for each channel
  - Supports time-out function for channel 0 and channel 1
  - Supports software and SPI/I2S, UART, USCI, USB, ADC, PWM and TIMER request
- Clock Control
  - Built-in 48 MHz internal high speed RC oscillator (HIRC) for USB device operation (Frequency variation < 2% at -40oC ~ +105oC)
    - ◆ Dynamically calibrating the HIRC OSC to 48 MHz  $\pm 0.25\%$  from -40°C to 105°C by external 32.768K crystal oscillator (LXT) or Start of Frame (SOF)
  - Built-in 10 kHz internal low speed RC oscillator for Watchdog Timer and Wake-up operation
  - Supports one interface to connect external crystal oscillator for high speed or low

- speed application
    - ◆ Built-in 4~24 MHz external high speed crystal oscillator (HXT) for precise timing operation
    - ◆ Built-in 32.768 kHz external low speed crystal oscillator (LXT) for low-power system operation
  - Supports one PLL up to 100 MHz for high performance system operation, sourced from HIRC and HXT
  - Supports clock on-the-fly switch
  - Supports clock failure detection for high/low speed external crystal oscillator
  - Supports auto clock switch once clock failure detected
  - Supports exception (NMI) generated once a clock failure detected
  - Supports divided clock output
- GPIO
  - Four I/O modes
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level trigger setting
  - Supports high driver and high sink current I/O (up to 20 mA at 5V)
  - Supports software selectable slew rate control
  - Supports up to 52/38/22 GPIOs for LQFP64/48 and QFN33 respectively
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function to count the event from external pin
  - Supports input capture function to capture or reset counter value
  - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
  - Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger BPWM, PWM, ADC and PDMA function
  - Supports Inter-Timer trigger mode
- Watchdog Timer
  - Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT
  - Supports 8 selections of time-out period (1.6ms ~ 26.0sec for LIRC)
  - Supports wake up from Power-down or Idle mode
  - Supports Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
  - Supports Window set by 6-bit counter with 11-bit prescale
  - Supports Interrupt
- BPWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two BPWM modules, each module provides one 16-bit counter and 6 output channels
  - Supports independent mode for BPWM output/Capture input channel
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution BPWM counter
    - ◆ Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each BPWM pin
  - Supports interrupt on the following events:

- ◆ BPWM counter match zero, period value or compared value
  - Supports trigger ADC on the following events:
    - ◆ BPWM counter match zero, period value or compared value
  - Supports capture mode with 16-bit resolution for each BPWM pin
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- PWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two PWM modules, each module provides three 16-bit counter and 6 output channels
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 3 complementary paired PWM output channel
    - ◆ Dead-time insertion with 12-bit resolution
    - ◆ Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - ◆ Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - ◆ Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
    - ◆ Noise filter for brake source from pin
    - ◆ Edge detect brake source to control brake state until brake interrupt cleared
    - ◆ Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - ◆ PWM counter match zero, period value or compared value
    - ◆ Brake condition happened
  - Supports trigger ADC on the following events:
    - ◆ PWM counter match zero, period value or compared value
  - Supports capture mode with 16-bit resolution for each PWM pin
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
  - Supports PDMA for capture mode
- USCI
  - UART Mode
    - ◆ Supports one transmit buffer and two receive buffer for data payload
    - ◆ Supports hardware auto flow control function
    - ◆ Supports programmable baud-rate generator
    - ◆ Support 9-Bit Data Transfer (Support 9-Bit RS-485)
    - ◆ Baud rate detection possible by built-in capture event of baud rate generator
    - ◆ Supports Wake-up function (Data and nCTS Wakeup Only)
    - ◆ Supports PDMA transfer
  - SPI Mode
    - ◆ Supports Master or Slave mode operation (the maximum frequency -- Master =  $f_{PCLK} / 2$ , Slave =  $f_{PCLK} / 5$ )
    - ◆ Supports one transmit buffer and two receive buffers for data payload
    - ◆ Configurable bit length of a transfer word from 4 to 16-bit
    - ◆ Supports MSB first or LSB first transfer sequence
    - ◆ Supports Word Suspend function
    - ◆ Supports 3-wire, no slave select signal, bi-direction interface

- ◆ Supports wake-up function by slave select signal in Slave mode
  - ◆ Supports one data channel half-duplex transfer
  - ◆ Supports PDMA transfer
- I<sup>2</sup>C Mode
  - ◆ Full master and slave device capability
  - ◆ Supports of 7-bit addressing, as well as 10-bit addressing
  - ◆ Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
  - ◆ Supports multi-master bus
  - ◆ Supports one transmit buffer and two receive buffer for data payload
  - ◆ Supports 10-bit bus time-out capability
  - ◆ Supports bus monitor mode.
  - ◆ Supports Power down wake-up by data toggle or address match
  - ◆ Supports setup/hold time programmable
  - ◆ Supports multiple address recognition (two slave address with mask option)
- UART
  - Supports one set of UART
  - Supports maximum clock frequency up to 10 Mbps
  - Full-duplex asynchronous communications
  - Separates receive and transmit 16/16 bytes entry FIFO for data payloads
  - Supports hardware auto-flow control (RX, TX, CTS and RTS)
  - Programmable receiver buffer trigger level
  - Supports programmable baud rate generator for each channel individually
  - Supports 8-bit receiver buffer time-out detection function
  - Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART\_TOUT [15:8])
  - Supports Auto-Baud Rate measurement and baud rate compensation function
  - Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
  - Fully programmable serial-interface characteristics
    - ◆ Programmable number of data bit, 5-, 6-, 7-, 8- bit character
    - ◆ Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
    - ◆ Programmable stop bit, 1, 1.5, or 2 stop bit generation
  - Supports IrDA SIR function mode
    - ◆ Supports for 3/16 bit duration for normal mode
  - Supports LIN function mode
    - ◆ Supports LIN master/slave mode
    - ◆ Supports programmable break generation function for transmitter
    - ◆ Supports break detection function for receiver
  - Supports RS-485 mode
    - ◆ Supports RS-485 9-bit mode
    - ◆ Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
  - Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
  - Supports PDMA transfer
- SPI / I<sup>2</sup>S
  - SPI
    - ◆ Supports one set of SPI controller
    - ◆ Supports Master or Slave mode operation
    - ◆ Configurable bit length of a transfer word from 8 to 32-bit
    - ◆ Provides separate 4-/8-level depth transmit and receive FIFO buffers

- ◆ Supports MSB first or LSB first transfer sequence
- ◆ Supports Byte Reorder function
- ◆ Supports PDMA transfer
- I<sup>2</sup>S
  - ◆ Supports Master or Slave mode operation
  - ◆ Capable of handling 8-, 16-, 24- and 32-bit word sizes in I<sup>2</sup>S mode
  - ◆ Provides separate 4-level depth transmit and receive FIFO buffers in I<sup>2</sup>S mode
  - ◆ Supports monaural and stereo audio data in I<sup>2</sup>S mode
  - ◆ Supports PCM mode A, PCM mode B, I<sup>2</sup>S and MSB justified data format in I<sup>2</sup>S mode
  - ◆ Supports PDMA transfer
- I<sup>2</sup>C
  - Supports up to two sets of I<sup>2</sup>C devices
  - Supports speed up to 1Mbps
  - Supports Master/Slave mode
  - Supports bidirectional data transfer between masters and slaves
  - Supports multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Supports 14-bit time-out counter requesting the I<sup>2</sup>C interrupt if the I<sup>2</sup>C bus hangs up and timer-out counter overflows
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition, four slave address with mask option
  - Supports two-level buffer function
  - Supports setup/hold time programmable
  - Supports wake-up function
- USB 2.0 FS Device Controller
  - Compliant with USB 2.0 Full-Speed specification
  - Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
  - Supports Control/Bulk/Interrupt/Isochronous transfer type
  - Supports suspend function when no bus activity existing for 3 ms
  - Supports 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 768 bytes buffer size
  - Provides remote wake-up capability
  - Start of Frame (SOF) locked clock pulse generation
  - Supports USB 2.0 Link Power Management (LPM)
  - Supports Crystal-less function
  - Supports PDMA transfer
- ADC
  - Supports 12-bit SAR ADC
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Analog input voltage range: 0~ AV<sub>DD</sub>
  - Up to 12 single-end analog input channels or 6 differential analog input channels
  - Maximum ADC peripheral clock frequency is 16 MHz
  - Conversion rate up to 800K SPS at 5V
  - Configurable ADC internal sampling time

- Supports single, burst, single-cycle scan, and continuous scan modes on enabled channels
- Supports individual conversion result register with valid and overrun indicators for each channel
- Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting
- An A/D conversion can be triggered by:
  - ◆ Software enable
  - ◆ External pin (STADC)
  - ◆ Timer 0~3 overflow pulse trigger
  - ◆ PWM triggers with optional start delay period
- Supports 2 internal channels for
  - ◆ Band-gap VBG input
  - ◆ Temperature sensor input
- Supports PDMA transfer
- Supports 96-bit Unique ID (UID)
- Supports 128-bit Unique Customer ID (UCID)
- One built-in temperature sensor with 1°C resolution
- Brown-out detector
  - With 4 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40°C ~105°C
- Packages
  - All Green package (RoHS)
  - LQFP 64-pin (7mm x 7mm)
  - LQFP 48-pin (7mm x 7mm)
  - QFN 33-pin (5mm x 5 mm)

### 3 ABBREVIATIONS

#### 3.1 Abbreviations

| Acronym | Description                                     |
|---------|-------------------------------------------------|
| ACMP    | Analog Comparator Controller                    |
| ADC     | Analog-to-Digital Converter                     |
| AES     | Advanced Encryption Standard                    |
| APB     | Advanced Peripheral Bus                         |
| AHB     | Advanced High-Performance Bus                   |
| BOD     | Brown-out Detection                             |
| DAP     | Debug Access Port                               |
| DES     | Data Encryption Standard                        |
| EBI     | External Bus Interface                          |
| EPWM    | Enhanced Pulse Width Modulation                 |
| FIFO    | First In, First Out                             |
| FMC     | Flash Memory Controller                         |
| FPU     | Floating-point Unit                             |
| GPIO    | General-Purpose Input/Output                    |
| HCLK    | The Clock of Advanced High-Performance Bus      |
| HIRC    | 48 MHz Internal High Speed RC Oscillator        |
| HXT     | 4~24 MHz External High Speed Crystal Oscillator |
| IAP     | In Application Programming                      |
| ICP     | In Circuit Programming                          |
| ISP     | In System Programming                           |
| LDO     | Low Dropout Regulator                           |
| LIN     | Local Interconnect Network                      |
| LIRC    | 10 kHz internal low speed RC oscillator (LIRC)  |
| MPU     | Memory Protection Unit                          |
| NVIC    | Nested Vectored Interrupt Controller            |
| PCLK    | The Clock of Advanced Peripheral Bus            |
| PDMA    | Peripheral Direct Memory Access                 |
| PLL     | Phase-Locked Loop                               |
| PWM     | Pulse Width Modulation                          |
| QEI     | Quadrature Encoder Interface                    |
| SD      | Secure Digital                                  |

|      |                                             |
|------|---------------------------------------------|
| SPI  | Serial Peripheral Interface                 |
| SPS  | Samples per Second                          |
| TDES | Triple Data Encryption Standard             |
| TMR  | Timer Controller                            |
| UART | Universal Asynchronous Receiver/Transmitter |
| UCID | Unique Customer ID                          |
| USB  | Universal Serial Bus                        |
| WDT  | Watchdog Timer                              |
| WWDT | Window Watchdog Timer                       |

Table 3.1-1 List of Abbreviations

## 4 PARTS INFORMATION LIST AND PIN CONFIGURATION

### 4.1 NuMicro® NUC121/125 Selection Guide

#### 4.1.1 NuMicro® NUC121/125 Naming Rule

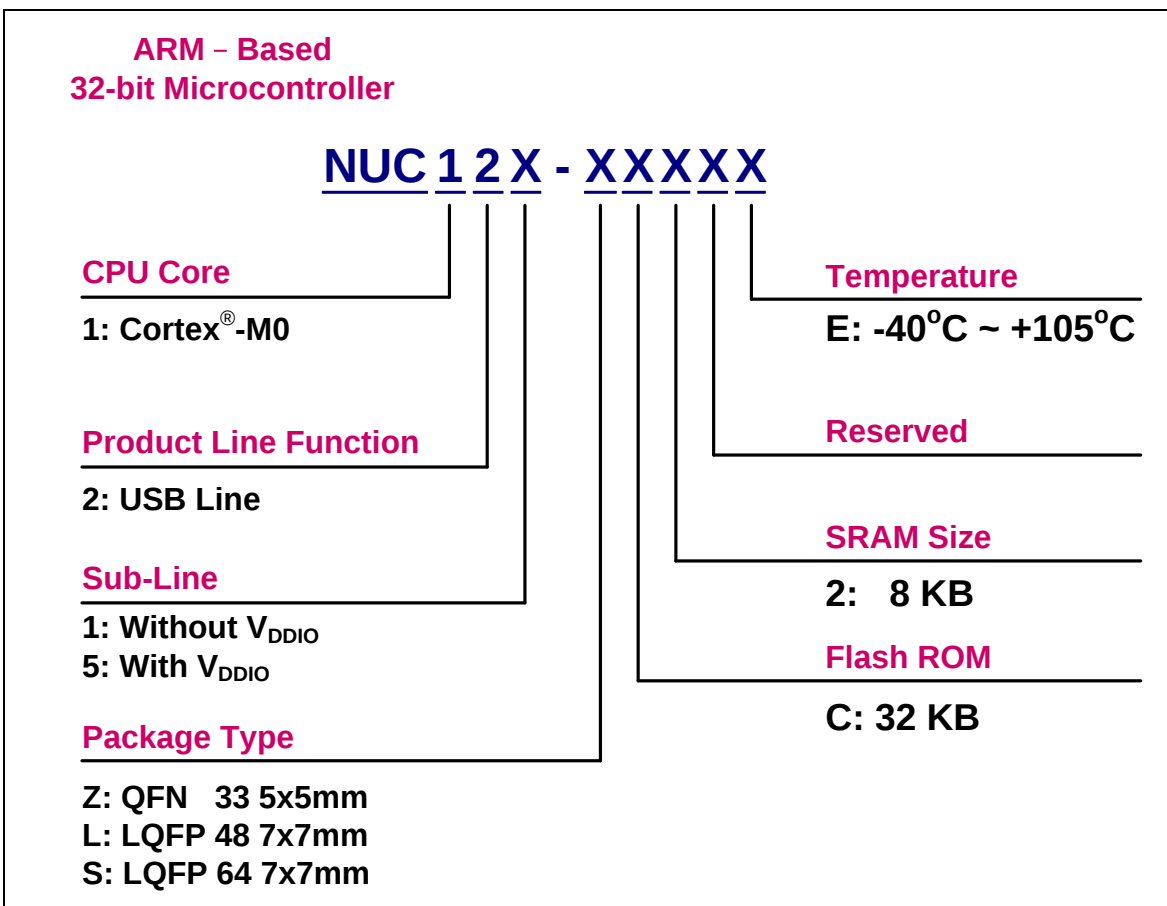


Figure 4.1-1 NuMicro® NUC121/125 Selection Code

### 4.1.2 NuMicro® NUC121 USB Series Selection Guide

\* USCI can be set to UART, I<sup>2</sup>C or SPI

| Part Number | Flash (KB) | SRAM (KB) | ISP Loader ROM (KB) | I/O | Timer/PWM | Connectivity |      |                      |                  |     | PWM | ADC (12-Bit) | PDMA | ICP/ISP/IAP | 1.8V Power Pin | Package |
|-------------|------------|-----------|---------------------|-----|-----------|--------------|------|----------------------|------------------|-----|-----|--------------|------|-------------|----------------|---------|
|             |            |           |                     |     |           | USCI*        | UART | SPI/I <sup>2</sup> S | I <sup>2</sup> C | USB |     |              |      |             |                |         |
| NUC121ZC2AE | 32         | 8         | 4.5                 | 22  | 4         | 1            | 1    | 1                    | 2                | 1   | 17  | 4-ch         | 5-ch | √           | -              | QFN 33  |
| NUC121LC2AE | 32         | 8         | 4.5                 | 38  | 4         | 1            | 1    | 1                    | 2                | 1   | 24  | 10-ch        | 5-ch | √           | -              | LQFP 48 |
| NUC121SC2AE | 32         | 8         | 4.5                 | 52  | 4         | 1            | 1    | 1                    | 2                | 1   | 24  | 12-ch        | 5-ch | √           | -              | LQFP 64 |

Table 4.1-1 NuMicro® NUC121 USB Series Selection Guide

### 4.1.3 NuMicro® NUC125 USB Series Selection Guide

\* USCI can be set to UART, I<sup>2</sup>C or SPI

| Part Number | Flash (KB) | SRAM (KB) | ISP Loader ROM (KB) | I/O | Timer/PWM | Connectivity |      |                      |                  |     | PWM | ADC (12-Bit) | PDMA | ICP/ISP/IAP | 1.8V Power Pin | Package |
|-------------|------------|-----------|---------------------|-----|-----------|--------------|------|----------------------|------------------|-----|-----|--------------|------|-------------|----------------|---------|
|             |            |           |                     |     |           | USCI*        | UART | SPI/I <sup>2</sup> S | I <sup>2</sup> C | USB |     |              |      |             |                |         |
| NUC125ZC2AE | 32         | 8         | 4.5                 | 22  | 4         | 1            | 1    | 1                    | 2                | 1   | 17  | 4-ch         | 5-ch | √           | √              | QFN 33  |
| NUC125LC2AE | 32         | 8         | 4.5                 | 37  | 4         | 1            | 1    | 1                    | 2                | 1   | 23  | 10-ch        | 5-ch | √           | √              | LQFP 48 |
| NUC125SC2AE | 32         | 8         | 4.5                 | 51  | 4         | 1            | 1    | 1                    | 2                | 1   | 23  | 12-ch        | 5-ch | √           | √              | LQFP 64 |

Table 4.1-2 NuMicro® NUC125 USB Series Selection Guide

## 4.2 Pin Configuration

### 4.2.1 NuMicro® NUC121 QFN 33-Pin Diagram

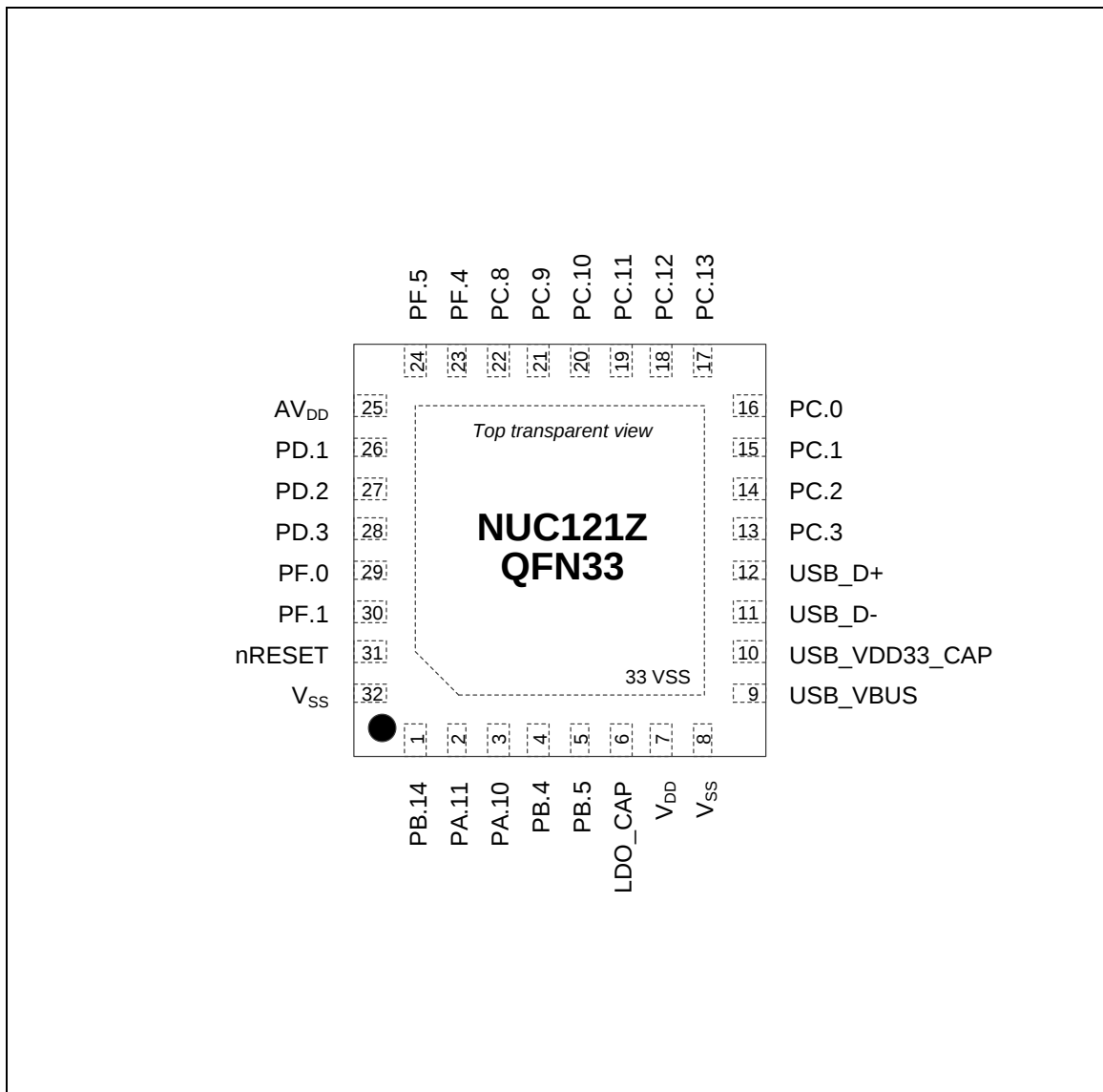


Figure 4.2-1 NuMicro® NUC121 QFN 33-Pin Diagram

## 4.2.2 NuMicro® NUC121 QFN 33-Pin Function Diagram

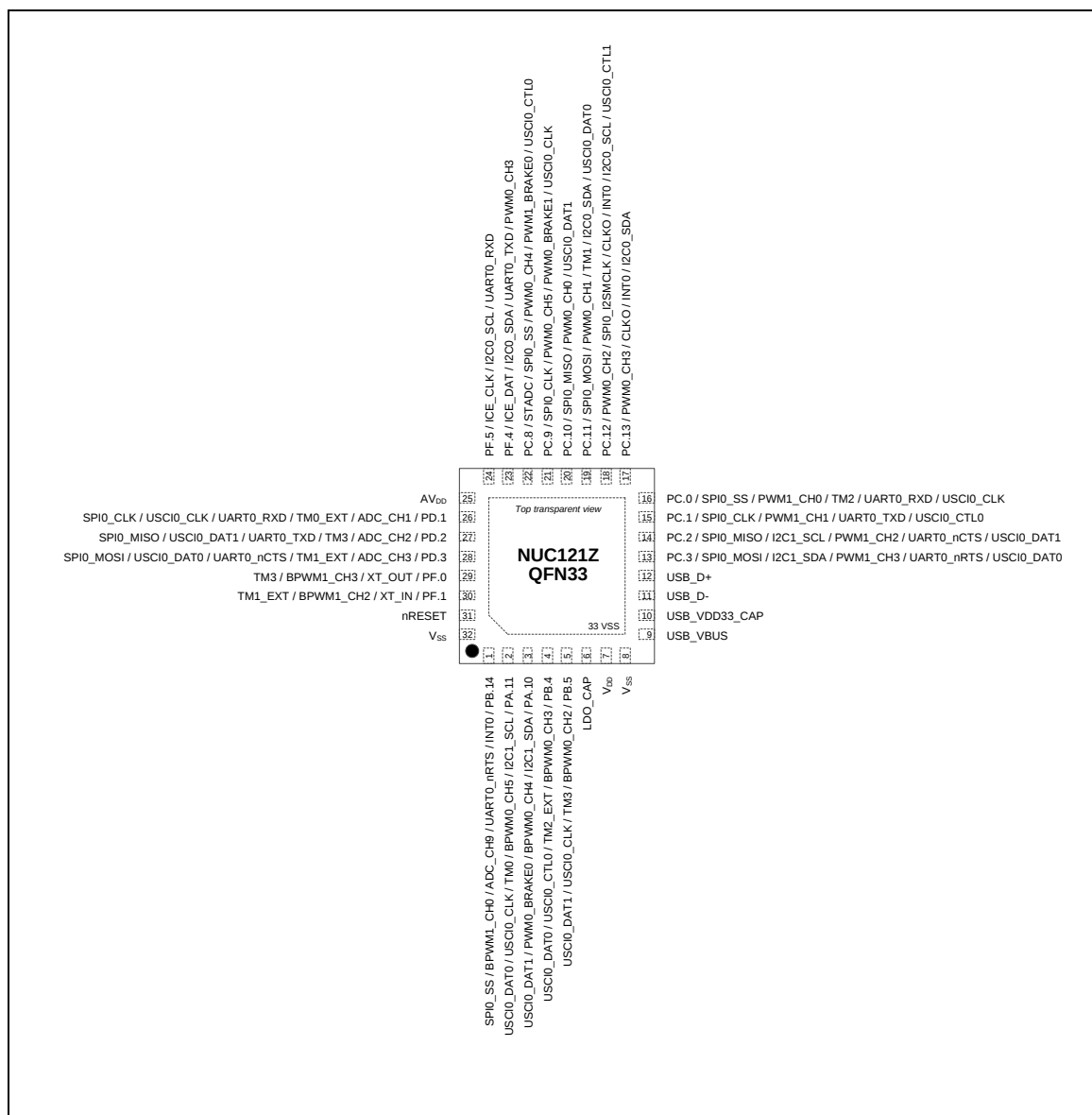


Figure 4.2-2 NuMicro® NUC121 QFN 33-Pin Function Diagram

### 4.2.3 NuMicro® NUC121 LQFP 48-Pin Diagram

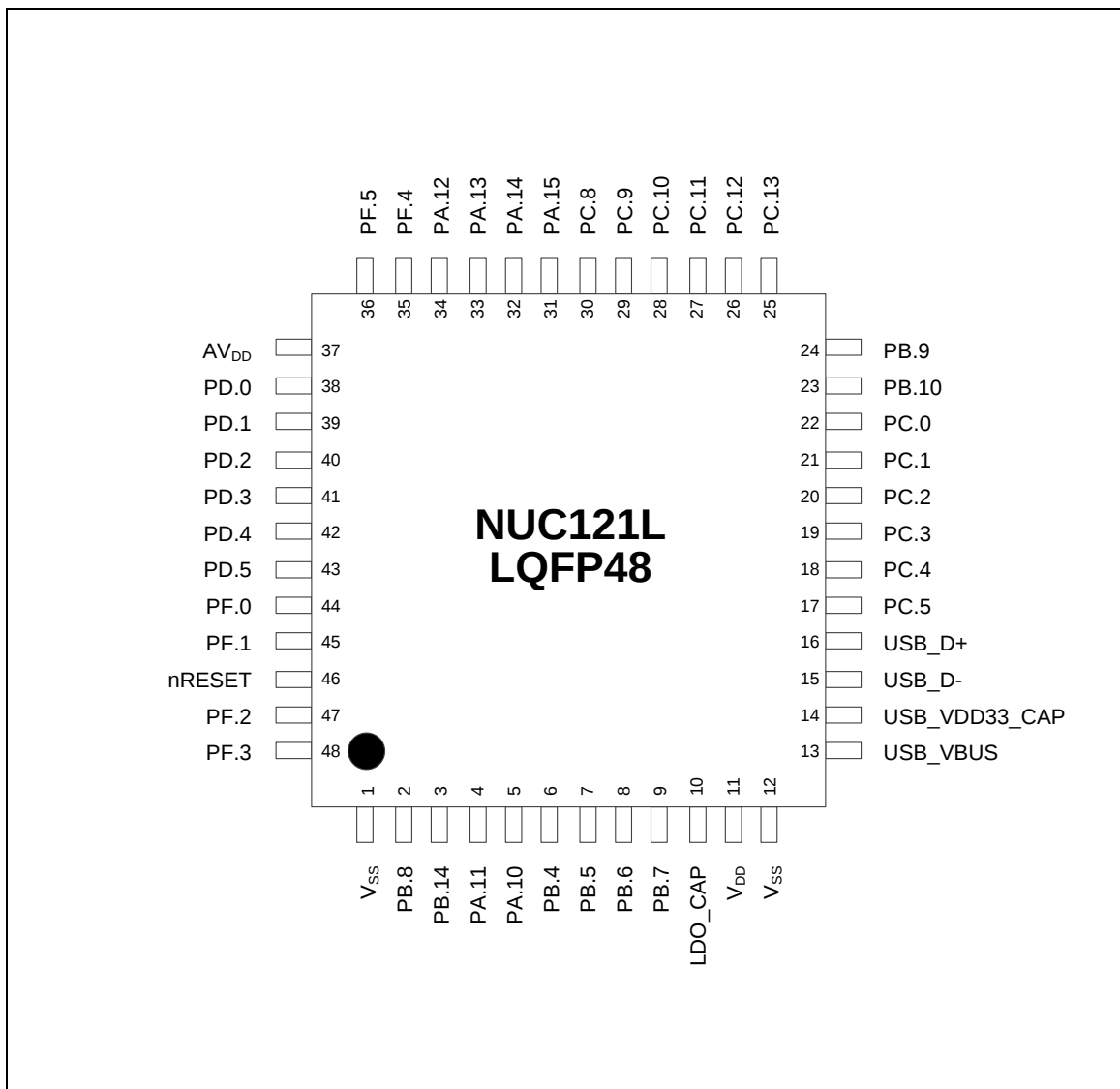


Figure 4.2-3 NuMicro® NUC121 LQFP 48-Pin Diagram

#### 4.2.4 NuMicro<sup>®</sup> NUC121 LQFP 48-Pin Function Diagram

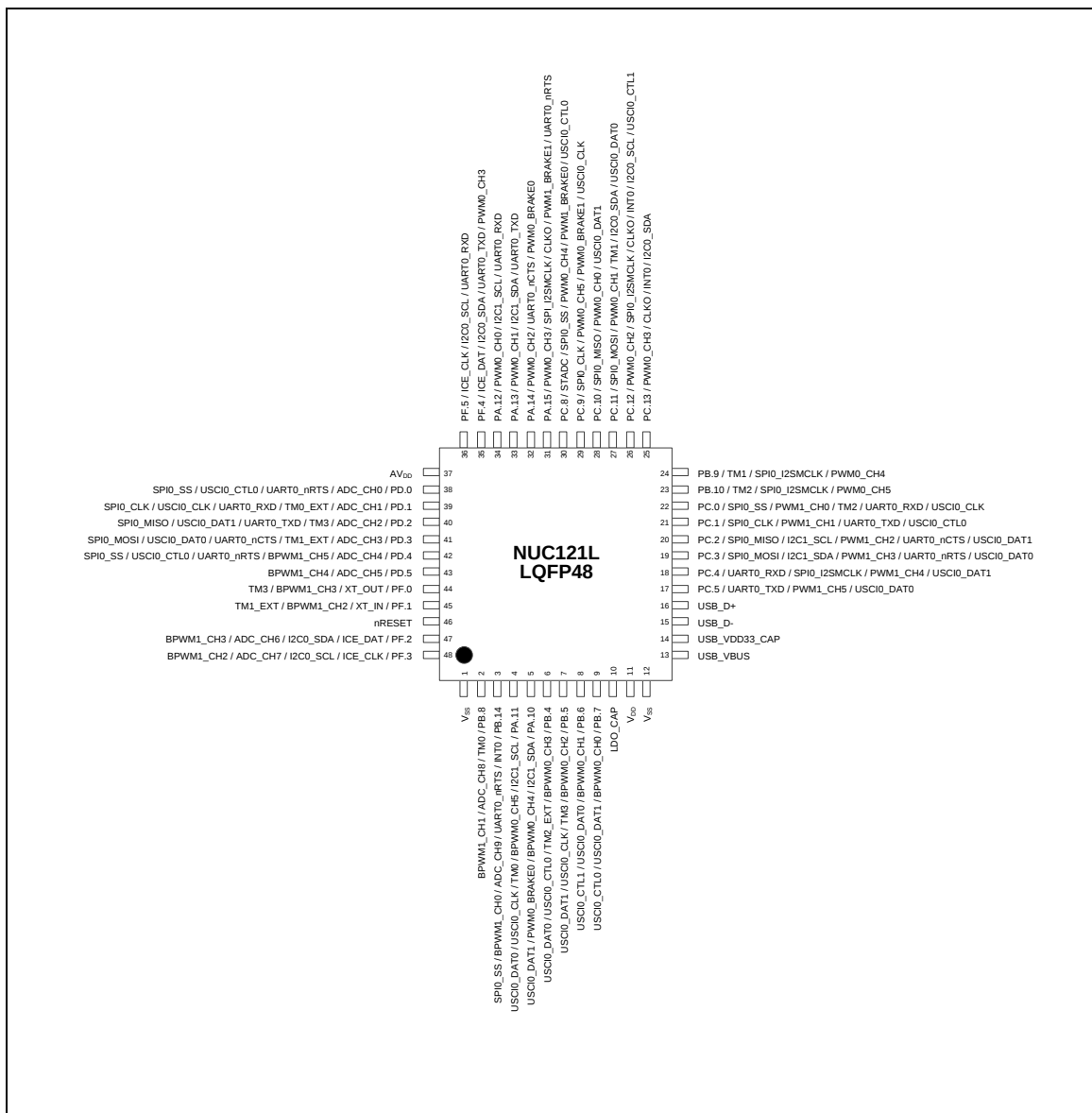


Figure 4.2-4 NuMicro<sup>®</sup> NUC121 LQFP 48-Pin Function Diagram

#### 4.2.5 NuMicro® NUC121 LQFP 64-Pin Diagram

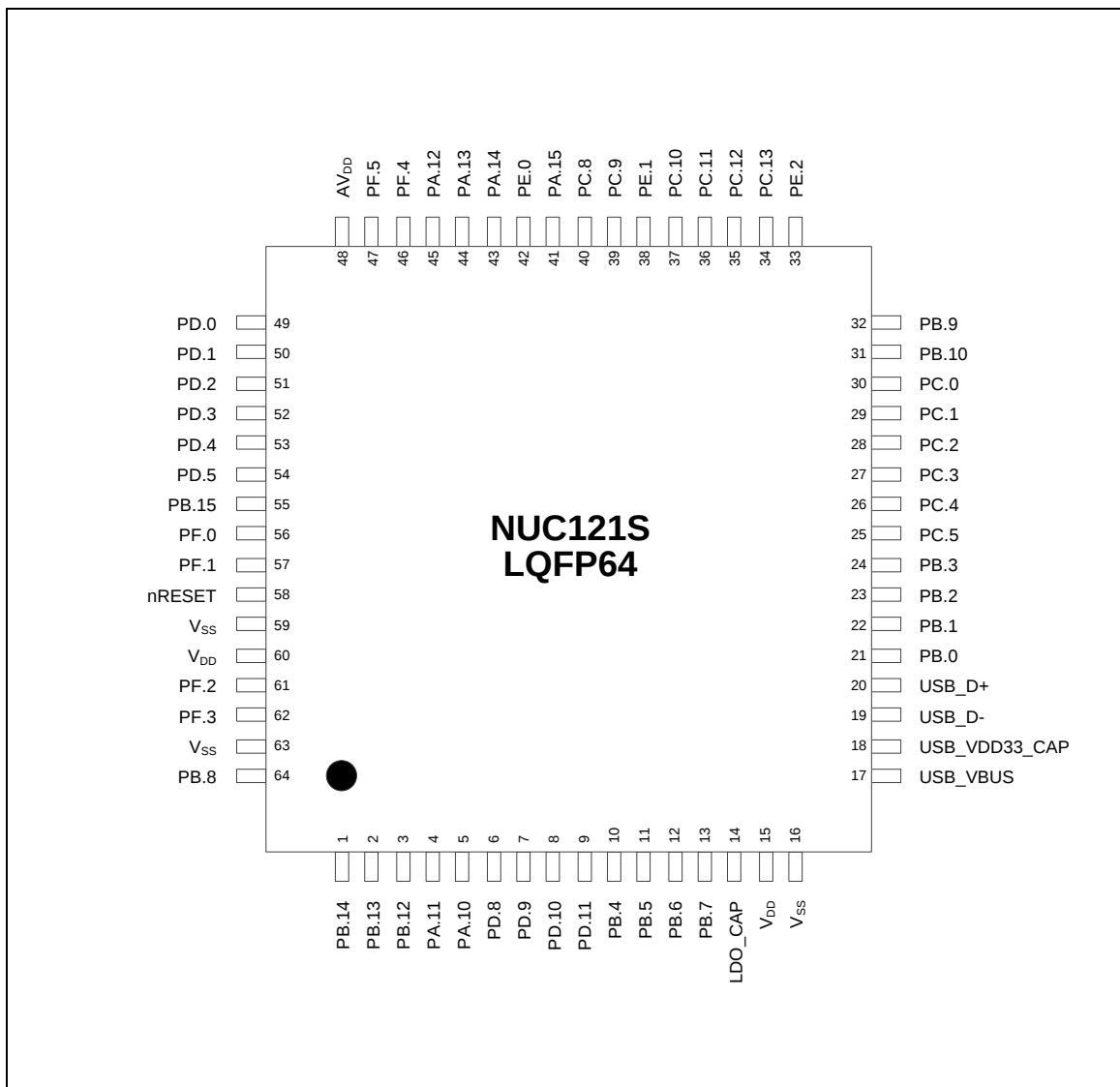


Figure 4.2-5 NuMicro® NUC121 LQFP 64-Pin Diagram

## 4.2.6 NuMicro® NUC121 LQFP 64-Pin Function Diagram

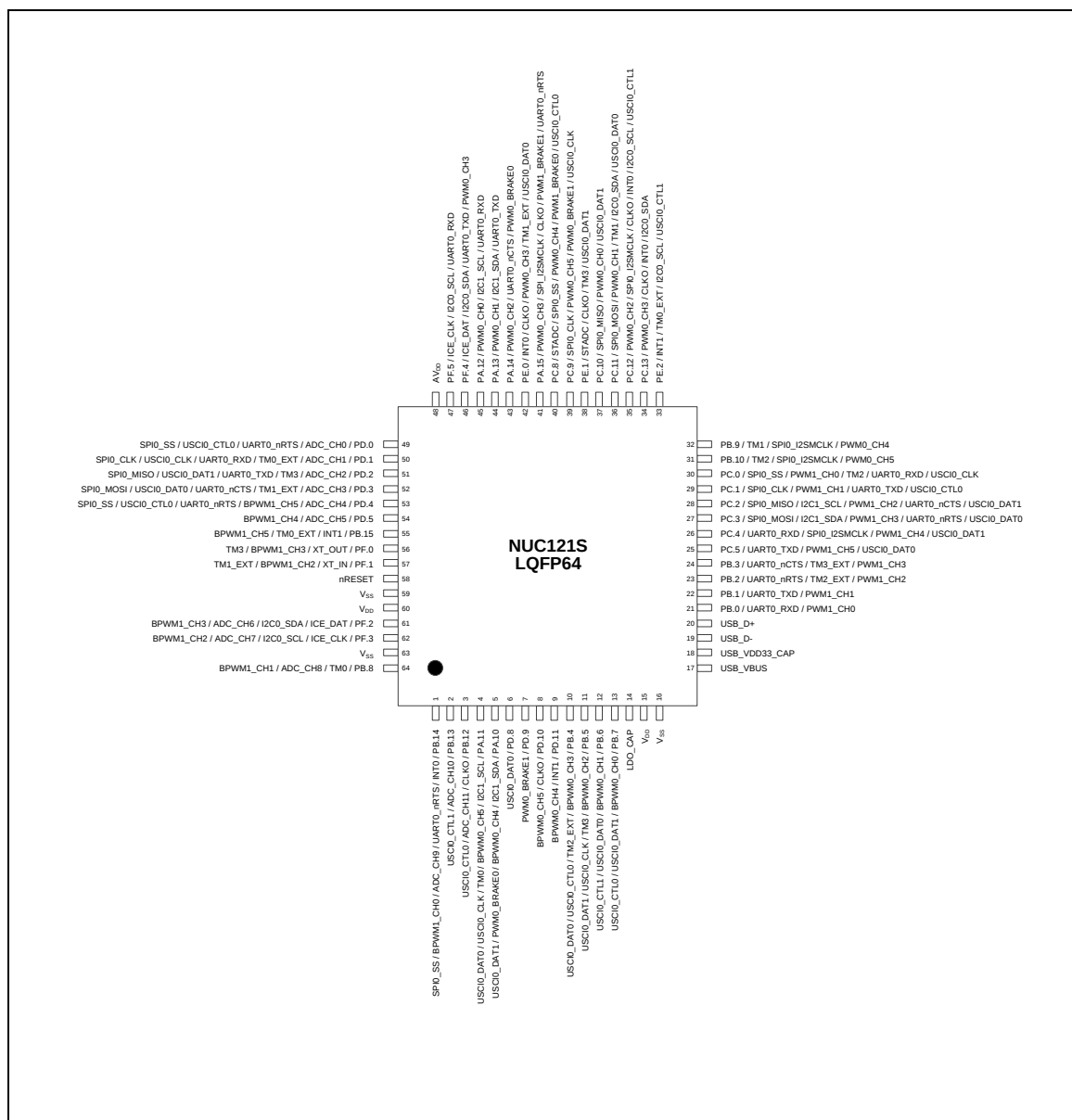


Figure 4.2-6 NuMicro® NUC121 LQFP 64-Pin Function Diagram

#### 4.2.7 NuMicro® NUC125 QFN 33-Pin Diagram

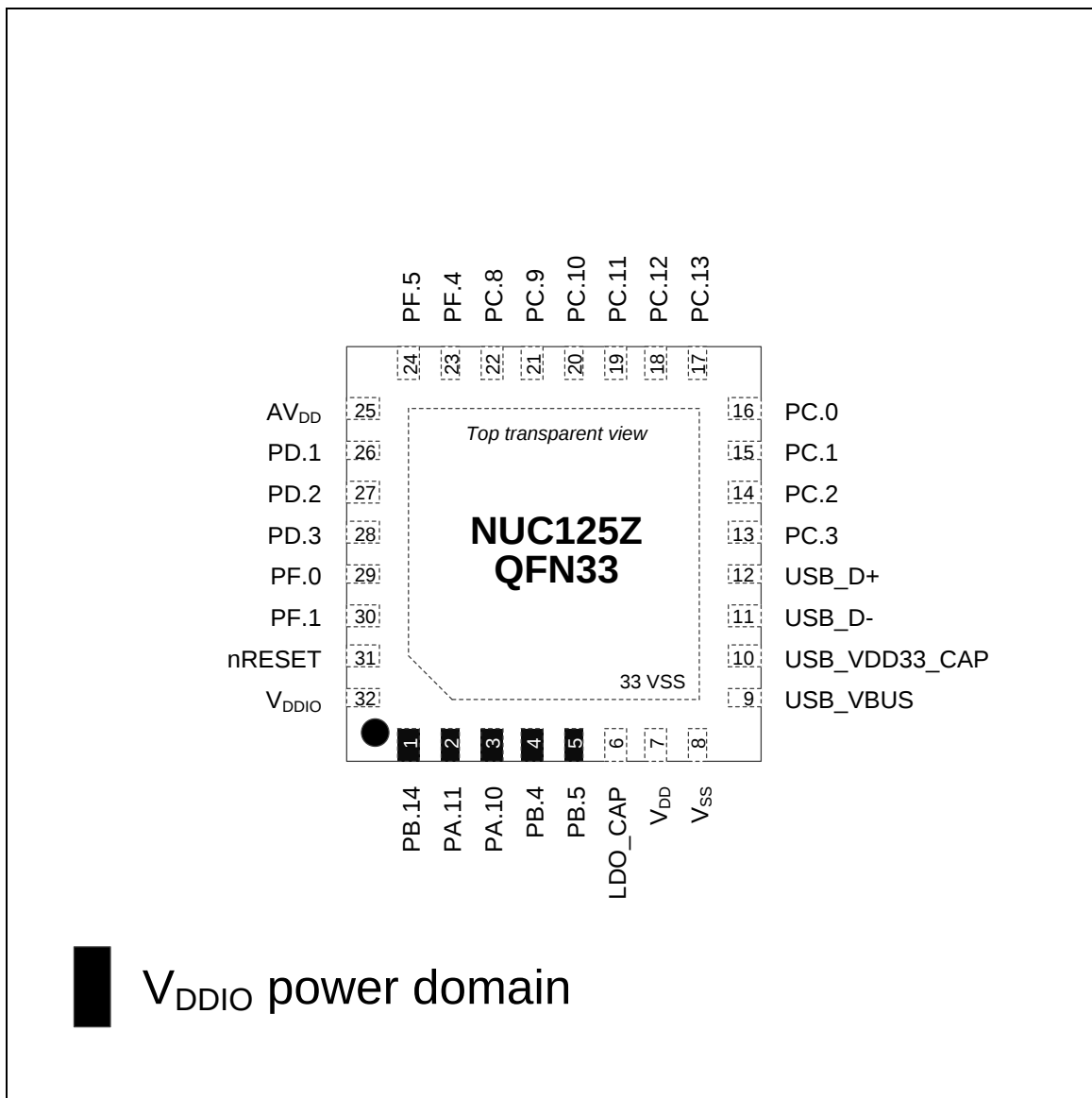


Figure 4.2-7 NuMicro® NUC125 QFN 33-Pin Diagram

#### 4.2.8 NuMicro® NUC125 QFN 33-Pin Function Diagram

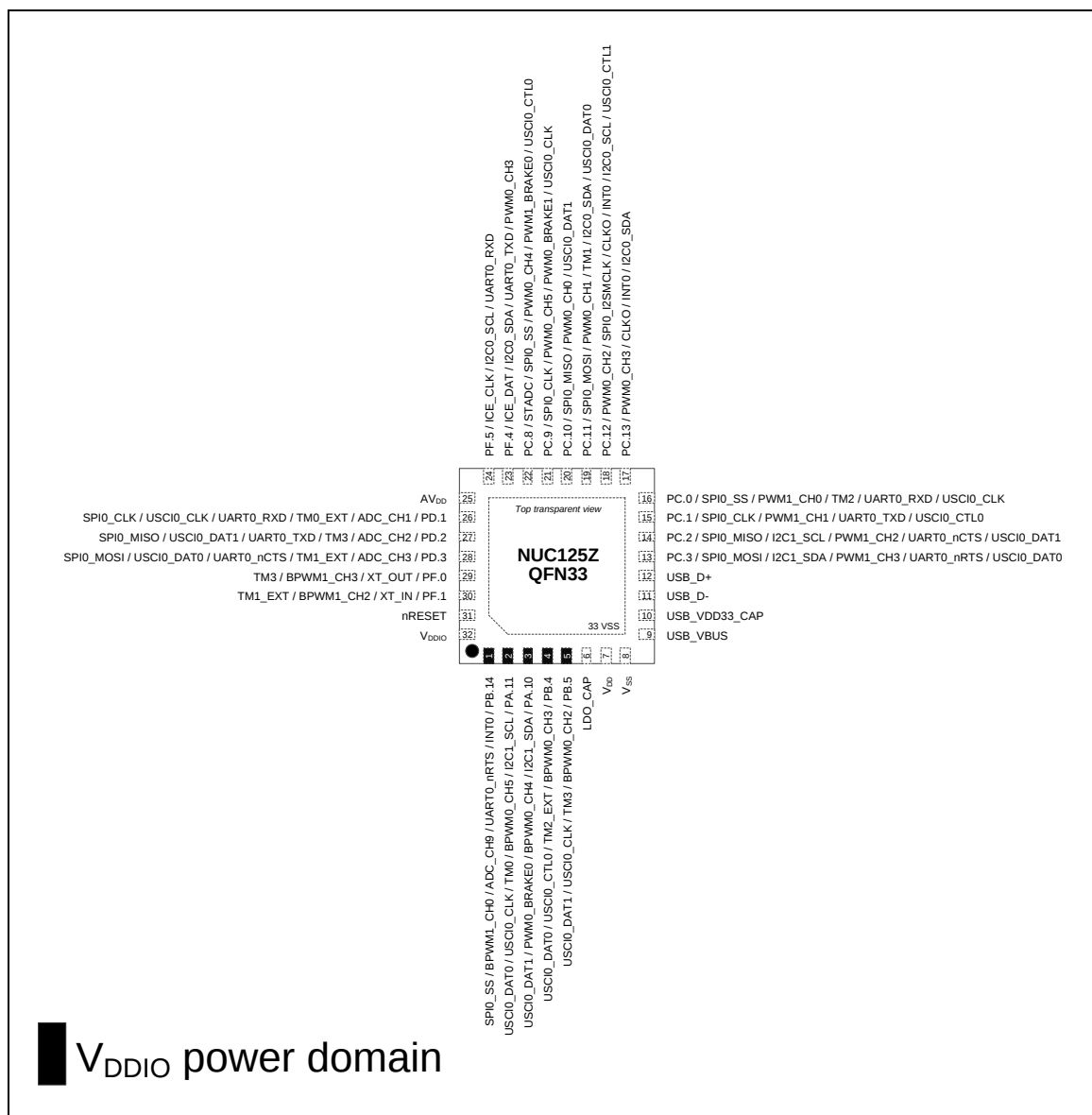


Figure 4.2-8 NuMicro® NUC125 QFN 33-Pin Function Diagram

#### 4.2.9 NuMicro® NUC125 LQFP 48-Pin Diagram

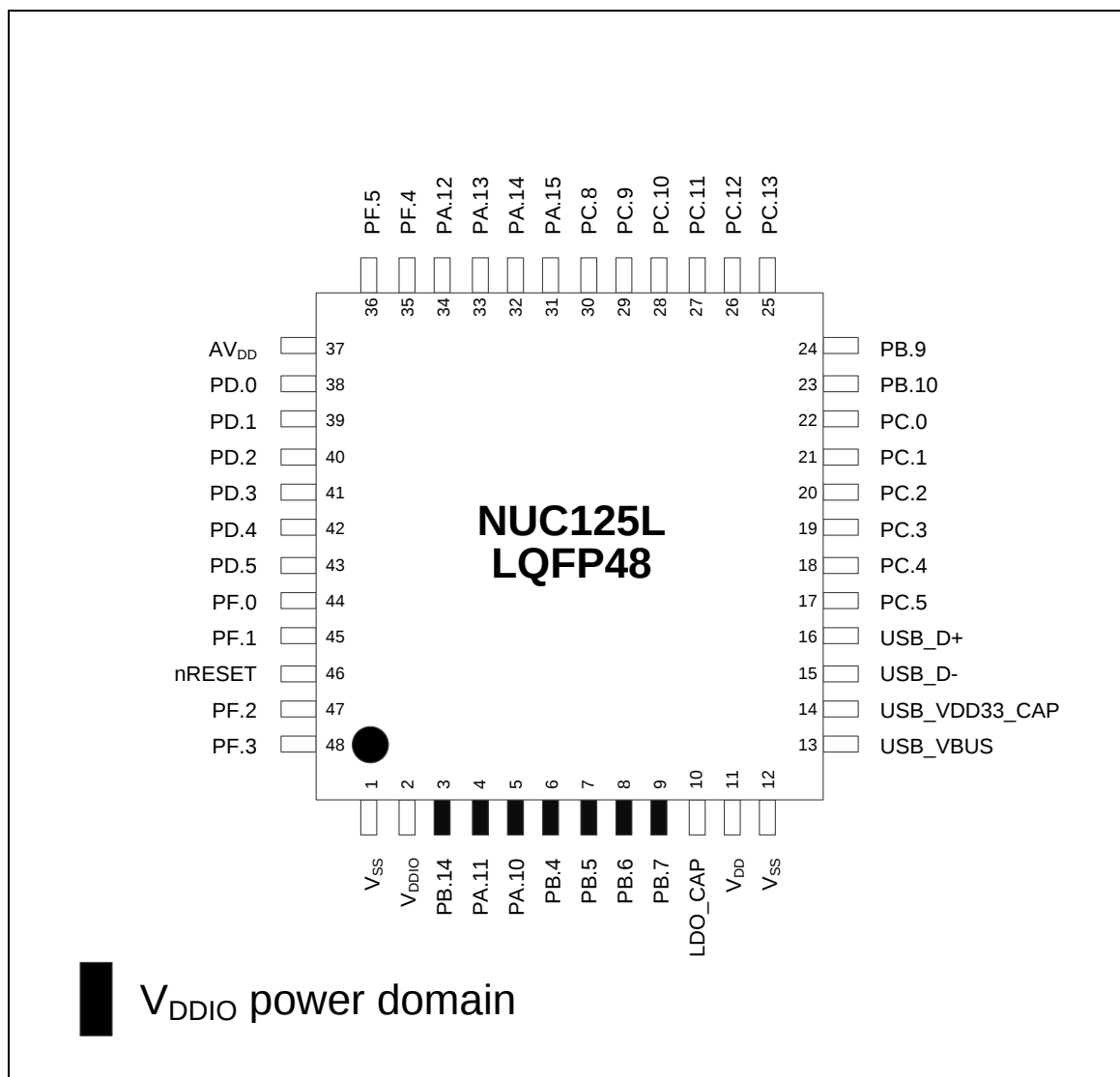


Figure 4.2-9 NuMicro® NUC125 LQFP 48-Pin Diagram

#### 4.2.10 NuMicro® NUC125 LQFP 48-Pin Function Diagram

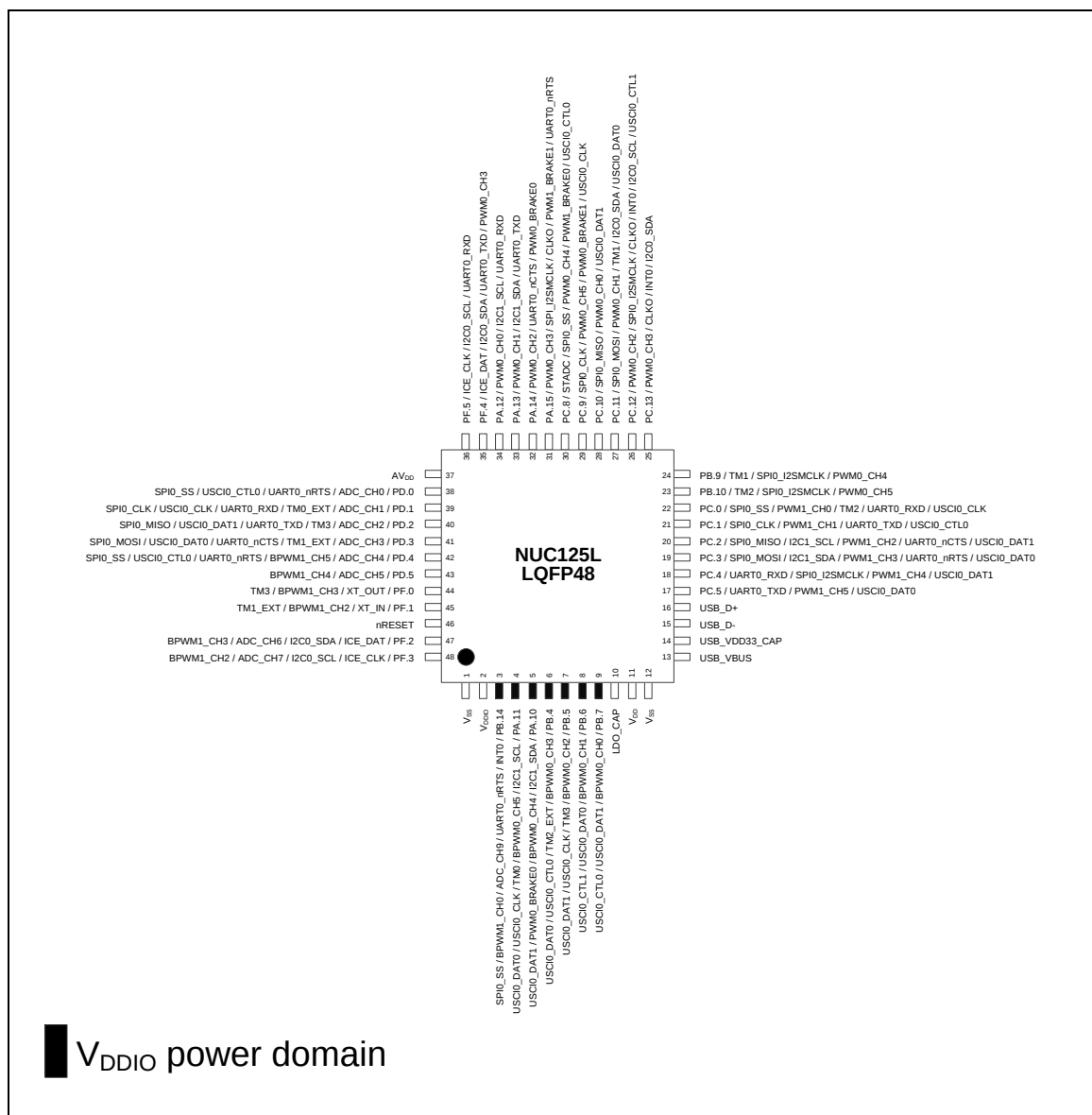


Figure 4.2-10 NuMicro® NUC125 LQFP 48-Pin Function Diagram

#### 4.2.11 NuMicro® NUC125 LQFP 64-Pin Diagram

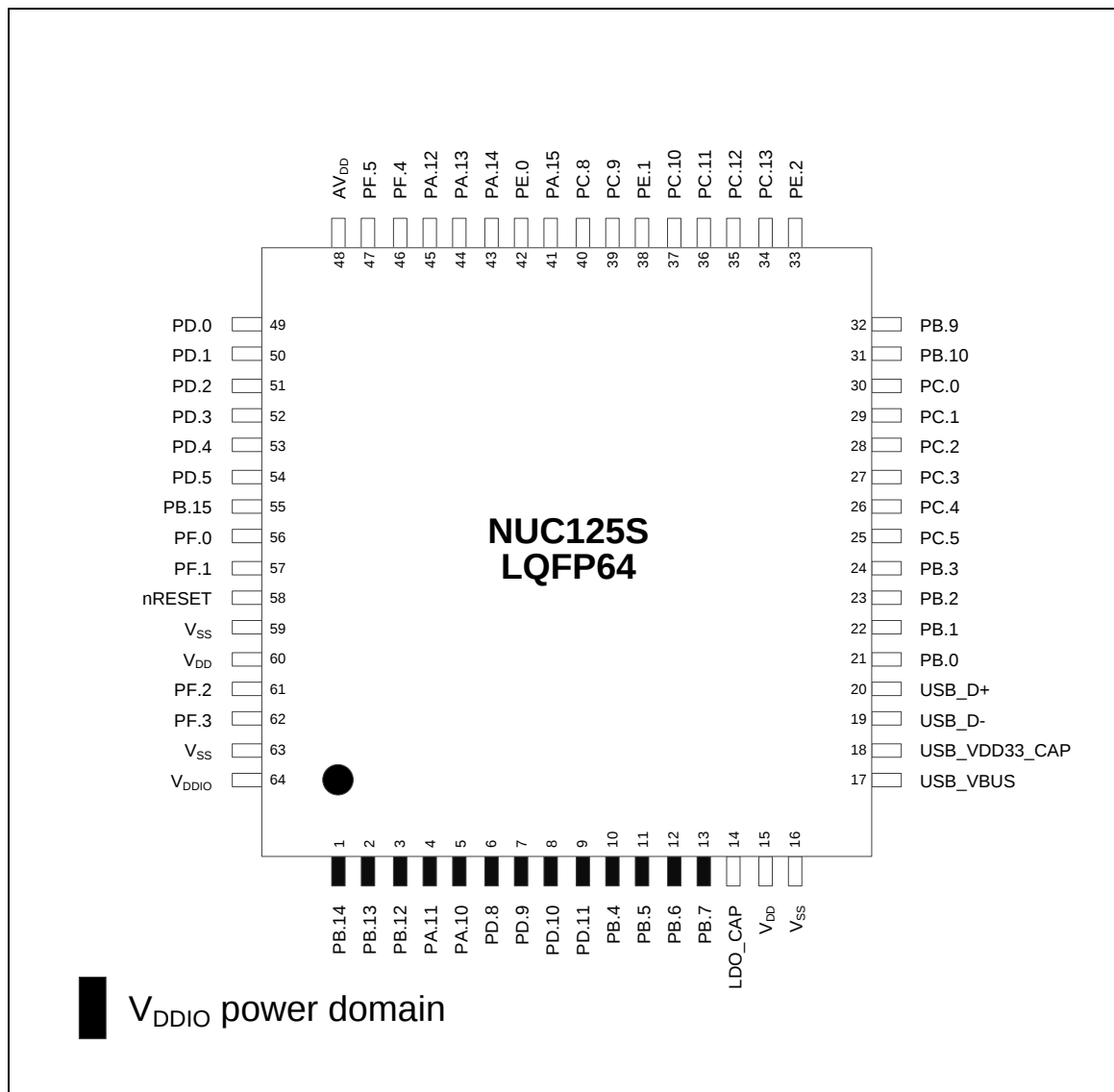


Figure 4.2-11 NuMicro® NUC125 LQFP 64-Pin Diagram

## 4.2.12 NuMicro® NUC125 LQFP 64-Pin Function Diagram

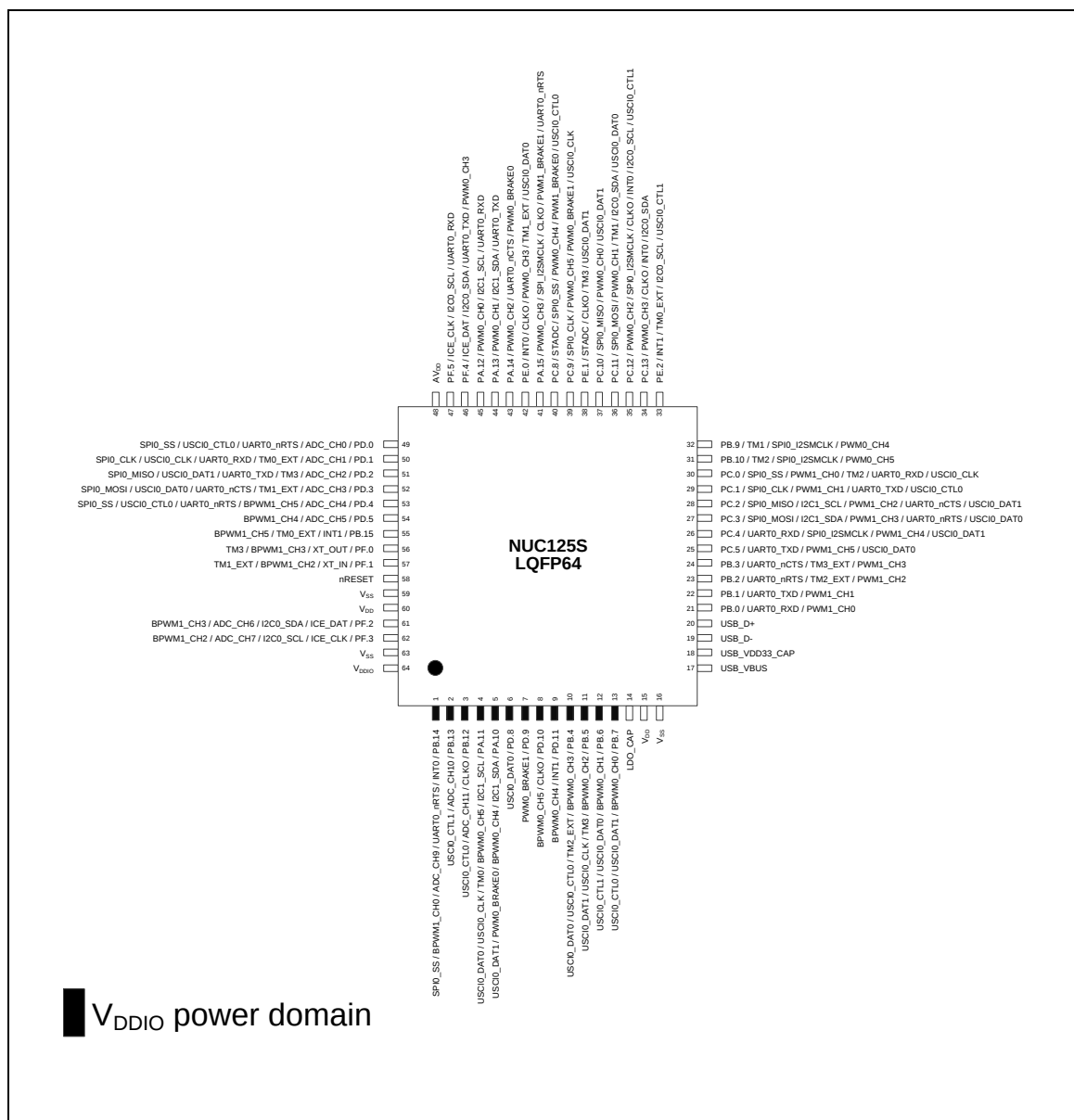


Figure 4.2-12 NuMicro® NUC125 LQFP 64-Pin Function Diagram

## 4.3 Pin Description

### 4.3.1 NUC121 USB Series QFN33 Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GPx\_MFPL and SYS\_GPx\_MFPH)

PA.10 MFP5 means SYS\_GPA\_MFPH[11:8]=0x5.

PC.0 MFP0 means SYS\_GPC\_MFPL[3:0]=0x0.

| Pin No. | Pin Name    | Type | MFP* | Description                                |
|---------|-------------|------|------|--------------------------------------------|
| 1       | PB.14       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | INT0        | I    | MFP1 | External interrupt0 input pin.             |
|         | UART0_nRTS  | O    | MFP2 | Request to Send output pin for UART0.      |
|         | ADC_CH9     | A    | MFP3 | ADC channel 9 analog input.                |
|         | BPWM1_CH0   | I/O  | MFP4 | BPWM1 channel 0 output/capture input.      |
|         | SPI0_SS     | I/O  | MFP7 | SPI0 slave select pin.                     |
| 2       | PA.11       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | I2C1_SCL    | I/O  | MFP1 | I <sup>2</sup> C1 clock pin.               |
|         | BPWM0_CH5   | I/O  | MFP4 | BPWM0 channel 5 output/capture input.      |
|         | TM0         | I/O  | MFP5 | Timer0event counter input / toggle output  |
|         | USCI0_CLK   | I/O  | MFP6 | USCI0 clock pin.                           |
|         | USCI0_DAT0  | I/O  | MFP7 | USCI0 DAT0 pin.                            |
| 3       | PA.10       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | I2C1_SDA    | I/O  | MFP1 | I <sup>2</sup> C1 data input/output pin.   |
|         | BPWM0_CH4   | I/O  | MFP4 | BPWM0 channel 4 output/capture input.      |
|         | PWM0_BRAKE0 | I    | MFP5 | Brake input pin 0 of PWM0.                 |
|         | USCI0_DAT1  | I/O  | MFP6 | USCI0 DAT1 pin.                            |
| 4       | PB.4        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | BPWM0_CH3   | I/O  | MFP4 | BPWM0 channel 3 output/capture input.      |
|         | TM2_EXT     | I    | MFP5 | Timer2 external counter input              |
|         | USCI0_CTL0  | I/O  | MFP6 | USCI0 CTL0 pin.                            |
|         | USCI0_DAT0  | I/O  | MFP7 | USCI0 DAT0 pin.                            |
| 5       | PB.5        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | BPWM0_CH2   | I/O  | MFP4 | BPWM0 channel 2 output/capture input.      |
|         | TM3         | I/O  | MFP5 | Timer3 event counter input / toggle output |
|         | USCI0_CLK   | I/O  | MFP6 | USCI0 clock pin.                           |
|         | USCI0_DAT1  | I/O  | MFP7 | USCI0 DAT1 pin.                            |

| Pin No. | Pin Name        | Type | MFP* | Description                                                                      |
|---------|-----------------|------|------|----------------------------------------------------------------------------------|
| 6       | LDO_CAP         | A    | MFP0 | LDO output pin.                                                                  |
| 7       | V <sub>DD</sub> | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |
| 8       | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                  |
| 9       | USB_VBUS        | A    | MFP0 | Power supply from USB host or HUB.                                               |
| 10      | USB_VDD33_CAP   | A    | MFP0 | Internal power regulator output 3.3V decoupling pin.                             |
| 11      | USB_D-          | I    | MFP0 | USB differential signal D-.                                                      |
| 12      | USB_D+          | I    | MFP0 | USB differential signal D+.                                                      |
| 13      | PC.3            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | SPI0_MOSI       | I/O  | MFP1 | SPI0 MOSI (Master Out, Slave In) pin.                                            |
|         | I2C1_SDA        | I/O  | MFP3 | I <sup>2</sup> C1 data input/output pin.                                         |
|         | PWM1_CH3        | I/O  | MFP4 | PWM1 channel3 output/capture input.                                              |
|         | UART0_nRTS      | O    | MFP6 | Request to Send output pin for UART0.                                            |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                                                  |
| 14      | PC.2            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | SPI0_MISO       | I/O  | MFP1 | SPI0 MISO (Master In, Slave Out) pin.                                            |
|         | I2C1_SCL        | I/O  | MFP3 | I <sup>2</sup> C1 clock pin.                                                     |
|         | PWM1_CH2        | I/O  | MFP4 | PWM1 channel2 output/capture input.                                              |
|         | UART0_nCTS      | I    | MFP6 | Clear to Send input pin for UART0.                                               |
|         | USCI0_DAT1      | I/O  | MFP7 | USCI0 DAT1 pin.                                                                  |
| 15      | PC.1            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | SPI0_CLK        | I/O  | MFP1 | SPI0 serial clock pin.                                                           |
|         | PWM1_CH1        | I/O  | MFP4 | PWM1 channel1 output/capture input.                                              |
|         | UART0_TXD       | O    | MFP6 | Data transmitter output pin for UART0.                                           |
|         | USCI0_CTL0      | I/O  | MFP7 | USCI0 CTL0 pin                                                                   |
| 16      | PC.0            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | SPI0_SS         | I/O  | MFP1 | SPI0 slave select pin.                                                           |
|         | PWM1_CH0        | I/O  | MFP4 | PWM1 channel0 output/capture input.                                              |
|         | TM2             | I/O  | MFP5 | Timer2 event counter input / toggle output                                       |
|         | UART0_RXD       | I    | MFP6 | Data receiver input pin for UART0.                                               |
|         | USCI0_CLK       | I/O  | MFP7 | USCI0 clock pin.                                                                 |
| 17      | PC.13           | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | PWM0_CH3        | I/O  | MFP2 | PWM0 channel3 output/capture input.                                              |
|         | CLKO            | O    | MFP3 | Clock Out                                                                        |

| Pin No. | Pin Name     | Type | MFP* | Description                                |
|---------|--------------|------|------|--------------------------------------------|
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SDA     | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
| 18      | PC.12        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2     | I/O  | MFP2 | PWM0 channel2 output/capture input.        |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | CLKO         | O    | MFP4 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SCL     | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |
|         | USCI0_CTL1   | I/O  | MFP7 | USCI0 CTL1 pin.                            |
| 19      | PC.11        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MOSI    | I/O  | MFP3 | SPI0 MOSI (Master Out, Slave In) pin.      |
|         | PWM0_CH1     | I/O  | MFP4 | PWM0 channel1 output/capture input.        |
|         | TM1          | I/O  | MFP5 | Timer1 event counter input / toggle output |
|         | I2C0_SDA     | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
|         | USCI0_DAT0   | I/O  | MFP7 | USCI0 DAT0 pin.                            |
| 20      | PC.10        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MISO    | I/O  | MFP3 | SPI0 MISO (Master In, Slave Out) pin.      |
|         | PWM0_CH0     | I/O  | MFP4 | PWM0 channel0 output/capture input.        |
|         | USCI0_DAT1   | I/O  | MFP7 | USCI0 DAT1 pin.                            |
| 21      | PC.9         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK     | I/O  | MFP3 | SPI0 serial clock pin.                     |
|         | PWM0_CH5     | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
|         | PWM0_BRAKE1  | I    | MFP5 | Brake input pin 1 of PWM0.                 |
|         | USCI0_CLK    | I/O  | MFP7 | USCI0 clock pin                            |
| 22      | PC.8         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC        | I    | MFP2 | ADC external trigger input.                |
|         | SPI0_SS      | I/O  | MFP3 | SPI0 slave select pin.                     |
|         | PWM0_CH4     | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
|         | PWM1_BRAKE0  | I    | MFP5 | Brake input pin 0 of PWM1.                 |
|         | USCI0_CTL0   | I/O  | MFP7 | USCI0 CTL0 pin                             |
| 23      | PF.4         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ICE_DAT      | I/O  | MFP1 | Serial wired debugger data pin             |
|         | I2C0_SDA     | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.   |

| Pin No. | Pin Name         | Type | MFP* | Description                                                                  |
|---------|------------------|------|------|------------------------------------------------------------------------------|
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.                                       |
|         | PWM0_CH3         | I/O  | MFP4 | PWM0 channel3 output/capture input.                                          |
| 24      | PF.5             | I/O  | MFP0 | General purpose digital I/O pin.                                             |
|         | ICE_CLK          | I    | MFP1 | Serial wired debugger clock pin                                              |
|         | I2C0_SCL         | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.                                                 |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.                                           |
| 25      | AV <sub>DD</sub> | A    | MFP0 | Power supply for internal analog circuit.                                    |
| 26      | PD.1             | I/O  | MFP0 | General purpose digital I/O pin.                                             |
|         | ADC_CH1          | A    | MFP3 | ADC channel 1 analog input.                                                  |
|         | TM0_EXT          | I    | MFP4 | Timer0 external counter input                                                |
|         | UART0_RXD        | I    | MFP5 | Data receiver input pin for UART0.                                           |
|         | USC10_CLK        | I/O  | MFP6 | USC10 clock pin.                                                             |
|         | SPI0_CLK         | I/O  | MFP7 | SPI0 serial clock pin.                                                       |
| 27      | PD.2             | I/O  | MFP0 | General purpose digital I/O pin.                                             |
|         | ADC_CH2          | A    | MFP3 | ADC channel 2 analog input.                                                  |
|         | TM3              | I/O  | MFP4 | Timer3 event counter input / toggle output                                   |
|         | UART0_TXD        | O    | MFP5 | Data transmitter output pin for UART0.                                       |
|         | USC10_DAT1       | I/O  | MFP6 | USC10 DAT1 pin.                                                              |
|         | SPI0_MISO        | I/O  | MFP7 | SPI0 MISO (Master In, Slave Out) pin.                                        |
| 28      | PD.3             | I/O  | MFP0 | General purpose digital I/O pin.                                             |
|         | ADC_CH3          | A    | MFP3 | ADC channel 3 analog input.                                                  |
|         | TM1_EXT          | I    | MFP4 | Timer1 external counter input                                                |
|         | UART0_nCTS       | I    | MFP5 | Clear to Send input pin for UART0.                                           |
|         | USC10_DAT0       | I/O  | MFP6 | USC10 DAT0 pin.                                                              |
|         | SPI0_MOSI        | I/O  | MFP7 | SPI0 MOSI (Master Out, Slave In) pin.                                        |
| 29      | PF.0             | I/O  | MFP0 | General purpose digital I/O pin.                                             |
|         | XT_OUT           | O    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal output pin. |
|         | BPWM1_CH3        | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                        |
|         | TM3              | I/O  | MFP5 | Timer3 event counter input / toggle output                                   |
| 30      | PF.1             | I/O  | MFP0 | General purpose digital I/O pin.                                             |
|         | XT_IN            | I    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal input pin.  |
|         | BPWM1_CH2        | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                        |

| Pin No. | Pin Name        | Type | MFP* | Description                                                                                          |
|---------|-----------------|------|------|------------------------------------------------------------------------------------------------------|
|         | TM1_EXT         | I    | MFP5 | Timer1 external counter input                                                                        |
| 31      | nRESET          | I    | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 32      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                                      |
| 33      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                                      |

Table 4.3-1 NUC121 USB Series QFN33 Pin Description

### 4.3.2 NUC121 USB Series LQFP48 Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GPx\_MFPL and SYS\_GPx\_MFPH)

PA.10 MFP5 means SYS\_GPA\_MFPH[11:8]=0x5.

PC.0 MFP0 means SYS\_GPC\_MFPL[3:0]=0x0..

| Pin No. | Pin Name        | Type | MFP* | Description                               |
|---------|-----------------|------|------|-------------------------------------------|
| 1       | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.           |
| 2       | PB.8            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | TM0             | I/O  | MFP1 | Timer0event counter input / toggle output |
|         | ADC_CH8         | A    | MFP3 | ADC channel 8 analog input.               |
|         | BPWM1_CH1       | I/O  | MFP4 | BPWM1 channel 1 output/capture input.     |
| 3       | PB.14           | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | INT0            | I    | MFP1 | External interrupt0 input pin.            |
|         | UART0_nRTS      | O    | MFP2 | Request to Send output pin for UART0.     |
|         | ADC_CH9         | A    | MFP3 | ADC channel 9 analog input.               |
|         | BPWM1_CH0       | I/O  | MFP4 | BPWM1 channel 0 output/capture input.     |
|         | SPI0_SS         | I/O  | MFP7 | SPI0 slave select pin.                    |
| 4       | PA.11           | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | I2C1_SCL        | I/O  | MFP1 | I <sup>2</sup> C1 clock pin.              |
|         | BPWM0_CH5       | I/O  | MFP4 | BPWM0 channel 5 output/capture input.     |
|         | TM0             | I/O  | MFP5 | Timer0event counter input / toggle output |
|         | USC10_CLK       | I/O  | MFP6 | USC10 clock pin.                          |
|         | USC10_DAT0      | I/O  | MFP7 | USC10 DAT0 pin.                           |
| 5       | PA.10           | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | I2C1_SDA        | I/O  | MFP1 | I <sup>2</sup> C1 data input/output pin.  |
|         | BPWM0_CH4       | I/O  | MFP4 | BPWM0 channel 4 output/capture input.     |
|         | PWM0_BRAKE0     | I    | MFP5 | Brake input pin 0 of PWM0.                |
|         | USC10_DAT1      | I/O  | MFP6 | USC10 DAT1 pin.                           |
| 6       | PB.4            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | BPWM0_CH3       | I/O  | MFP4 | BPWM0 channel 3 output/capture input.     |
|         | TM2_EXT         | I    | MFP5 | Timer2 external counter input             |
|         | USC10_CTL0      | I/O  | MFP6 | USC10 CTL0 pin.                           |
|         | USC10_DAT0      | I/O  | MFP7 | USC10 DAT0 pin.                           |
| 7       | PB.5            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | BPWM0_CH2       | I/O  | MFP4 | BPWM0 channel 2 output/capture input.     |

| Pin No. | Pin Name        | Type | MFP* | Description                                                                      |
|---------|-----------------|------|------|----------------------------------------------------------------------------------|
|         | TM3             | I/O  | MFP5 | Timer3 event counter input / toggle output                                       |
|         | USCI0_CLK       | I/O  | MFP6 | USCI0 clock pin.                                                                 |
|         | USCI0_DAT1      | I/O  | MFP7 | USCI0 DAT1 pin.                                                                  |
| 8       | PB.6            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH1       | I/O  | MFP4 | BPWM0 channel 1 output/capture input.                                            |
|         | USCI0_DAT0      | I/O  | MFP6 | USCI0 DAT0 pin.                                                                  |
|         | USCI0_CTL1      | I/O  | MFP7 | USCI0 CTL1 pin.                                                                  |
| 9       | PB.7            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH0       | I/O  | MFP4 | BPWM0 channel 0 output/capture input.                                            |
|         | USCI0_DAT1      | I/O  | MFP6 | USCI0 DAT1 pin.                                                                  |
|         | USCI0_CTL0      | I/O  | MFP7 | USCI0 CTL0 pin.                                                                  |
| 10      | LDO_CAP         | A    | MFP0 | LDO output pin.                                                                  |
| 11      | V <sub>DD</sub> | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |
| 12      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                  |
| 13      | USB_VBUS        | A    | MFP0 | Power supply from USB host or HUB.                                               |
| 14      | USB_VDD33_CAP   | A    | MFP0 | Internal power regulator output 3.3V decoupling pin.                             |
| 15      | USB_D-          | I    | MFP0 | USB differential signal D-.                                                      |
| 16      | USB_D+          | I    | MFP0 | USB differential signal D+.                                                      |
| 17      | PC.5            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | UART0_TXD       | O    | MFP2 | Data transmitter output pin for UART0.                                           |
|         | PWM1_CH5        | I/O  | MFP4 | PWM1 channel5 output/capture input.                                              |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                                                  |
| 18      | PC.4            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | UART0_RXD       | I    | MFP2 | Data receiver input pin for UART0.                                               |
|         | SPI0_I2SMCLK    | O    | MFP3 | I2S0 master clock output pin.                                                    |
|         | PWM1_CH4        | I/O  | MFP4 | PWM1 channel4 output/capture input.                                              |
|         | USCI0_DAT1      | I/O  | MFP7 | USCI0 DAT1 pin.                                                                  |
| 19      | PC.3            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | SPI0_MOSI       | I/O  | MFP1 | SPI0 MOSI (Master Out, Slave In) pin.                                            |
|         | I2C1_SDA        | I/O  | MFP3 | I <sup>2</sup> C1 data input/output pin.                                         |
|         | PWM1_CH3        | I/O  | MFP4 | PWM1 channel3 output/capture input.                                              |
|         | UART0_nRTS      | O    | MFP6 | Request to Send output pin for UART0.                                            |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                                                  |

| Pin No. | Pin Name     | Type | MFP* | Description                                |
|---------|--------------|------|------|--------------------------------------------|
| 20      | PC.2         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MISO    | I/O  | MFP1 | SPI0 MISO (Master In, Slave Out) pin.      |
|         | I2C1_SCL     | I/O  | MFP3 | I <sup>2</sup> C1 clock pin.               |
|         | PWM1_CH2     | I/O  | MFP4 | PWM1 channel2 output/capture input.        |
|         | UART0_nCTS   | I    | MFP6 | Clear to Send input pin for UART0.         |
|         | USC10_DAT1   | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 21      | PC.1         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK     | I/O  | MFP1 | SPI0 serial clock pin.                     |
|         | PWM1_CH1     | I/O  | MFP4 | PWM1 channel1 output/capture input.        |
|         | UART0_TXD    | O    | MFP6 | Data transmitter output pin for UART0.     |
|         | USC10_CTL0   | I/O  | MFP7 | USC10 CTL0 pin                             |
| 22      | PC.0         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_SS      | I/O  | MFP1 | SPI0 slave select pin.                     |
|         | PWM1_CH0     | I/O  | MFP4 | PWM1 channel0 output/capture input.        |
|         | TM2          | I/O  | MFP5 | Timer2 event counter input / toggle output |
|         | UART0_RXD    | I    | MFP6 | Data receiver input pin for UART0.         |
|         | USC10_CLK    | I/O  | MFP7 | USC10 clock pin.                           |
| 23      | PB.10        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM2          | I/O  | MFP1 | Timer2 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH5     | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
| 24      | PB.9         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM1          | I/O  | MFP1 | Timer1 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH4     | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
| 25      | PC.13        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3     | I/O  | MFP2 | PWM0 channel3 output/capture input.        |
|         | CLKO         | O    | MFP3 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SDA     | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
| 26      | PC.12        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2     | I/O  | MFP2 | PWM0 channel2 output/capture input.        |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |

| Pin No. | Pin Name    | Type | MFP* | Description                                |
|---------|-------------|------|------|--------------------------------------------|
|         | CLKO        | O    | MFP4 | Clock Out                                  |
|         | INT0        | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SCL    | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |
|         | USC10_CTL1  | I/O  | MFP7 | USC10 CTL1 pin.                            |
| 27      | PC.11       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MOSI   | I/O  | MFP3 | SPI0 MOSI (Master Out, Slave In) pin.      |
|         | PWM0_CH1    | I/O  | MFP4 | PWM0 channel1 output/capture input.        |
|         | TM1         | I/O  | MFP5 | Timer1 event counter input / toggle output |
|         | I2C0_SDA    | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
|         | USC10_DAT0  | I/O  | MFP7 | USC10 DAT0 pin.                            |
| 28      | PC.10       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MISO   | I/O  | MFP3 | SPI0 MISO (Master In, Slave Out) pin.      |
|         | PWM0_CH0    | I/O  | MFP4 | PWM0 channel0 output/capture input.        |
|         | USC10_DAT1  | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 29      | PC.9        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK    | I/O  | MFP3 | SPI0 serial clock pin.                     |
|         | PWM0_CH5    | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
|         | PWM0_BRAKE1 | I    | MFP5 | Brake input pin 1 of PWM0.                 |
|         | USC10_CLK   | I/O  | MFP7 | USC10 clock pin                            |
| 30      | PC.8        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC       | I    | MFP2 | ADC external trigger input.                |
|         | SPI0_SS     | I/O  | MFP3 | SPI0 slave select pin.                     |
|         | PWM0_CH4    | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
|         | PWM1_BRAKE0 | I    | MFP5 | Brake input pin 0 of PWM1.                 |
|         | USC10_CTL0  | I/O  | MFP7 | USC10 CTL0 pin                             |
| 31      | PA.15       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3    | I/O  | MFP1 | PWM0 channel3 output/capture input.        |
|         | SPI_I2SMCLK | O    | MFP2 | I2S0 master clock output pin.              |
|         | CLKO        | O    | MFP3 | Clock Out                                  |
|         | PWM1_BRAKE1 | I    | MFP4 | Brake input pin 1 of PWM1.                 |
|         | UART0_nRTS  | O    | MFP5 | Request to Send output pin for UART0.      |
| 32      | PA.14       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2    | I/O  | MFP1 | PWM0 channel2 output/capture input.        |

| Pin No. | Pin Name         | Type | MFP* | Description                               |
|---------|------------------|------|------|-------------------------------------------|
|         | UART0_nCTS       | I    | MFP3 | Clear to Send input pin for UART0.        |
|         | PWM0_BRAKE0      | I    | MFP4 | Brake input pin 0 of PWM0.                |
| 33      | PA.13            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH1         | I/O  | MFP1 | PWM0 channel1 output/capture input.       |
|         | I2C1_SDA         | I/O  | MFP2 | I <sup>2</sup> C1 data input/output pin.  |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.    |
| 34      | PA.12            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH0         | I/O  | MFP1 | PWM0 channel0 output/capture input.       |
|         | I2C1_SCL         | I/O  | MFP2 | I <sup>2</sup> C1 clock pin.              |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.        |
| 35      | PF.4             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ICE_DAT          | I/O  | MFP1 | Serial wired debugger data pin            |
|         | I2C0_SDA         | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.  |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.    |
|         | PWM0_CH3         | I/O  | MFP4 | PWM0 channel3 output/capture input.       |
| 36      | PF.5             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ICE_CLK          | I    | MFP1 | Serial wired debugger clock pin           |
|         | I2C0_SCL         | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.              |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.        |
| 37      | AV <sub>DD</sub> | A    | MFP0 | Power supply for internal analog circuit. |
| 38      | PD.0             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ADC_CH0          | A    | MFP3 | ADC channel 0 analog input.               |
|         | UART0_nRTS       | O    | MFP5 | Request to Send output pin for UART0.     |
|         | USC10_CTL0       | I/O  | MFP6 | USC10 CTL0 pin.                           |
|         | SPI0_SS          | I/O  | MFP7 | SPI0 slave select pin.                    |
| 39      | PD.1             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ADC_CH1          | A    | MFP3 | ADC channel 1 analog input.               |
|         | TM0_EXT          | I    | MFP4 | Timer0 external counter input             |
|         | UART0_RXD        | I    | MFP5 | Data receiver input pin for UART0.        |
|         | USC10_CLK        | I/O  | MFP6 | USC10 clock pin.                          |
|         | SPI0_CLK         | I/O  | MFP7 | SPI0 serial clock pin.                    |
| 40      | PD.2             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ADC_CH2          | A    | MFP3 | ADC channel 2 analog input.               |

| Pin No. | Pin Name   | Type | MFP* | Description                                                                                          |
|---------|------------|------|------|------------------------------------------------------------------------------------------------------|
|         | TM3        | I/O  | MFP4 | Timer3 event counter input / toggle output                                                           |
|         | UART0_TXD  | O    | MFP5 | Data transmitter output pin for UART0.                                                               |
|         | USC10_DAT1 | I/O  | MFP6 | USC10 DAT1 pin.                                                                                      |
|         | SPI0_MISO  | I/O  | MFP7 | SPI0 MISO (Master In, Slave Out) pin.                                                                |
| 41      | PD.3       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH3    | A    | MFP3 | ADC channel 3 analog input.                                                                          |
|         | TM1_EXT    | I    | MFP4 | Timer1 external counter input                                                                        |
|         | UART0_nCTS | I    | MFP5 | Clear to Send input pin for UART0.                                                                   |
|         | USC10_DAT0 | I/O  | MFP6 | USC10 DAT0 pin.                                                                                      |
|         | SPI0_MOSI  | I/O  | MFP7 | SPI0 MOSI (Master Out, Slave In) pin.                                                                |
| 42      | PD.4       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH4    | A    | MFP2 | ADC channel 4 analog input.                                                                          |
|         | BPWM1_CH5  | I/O  | MFP4 | BPWM1 channel 5 output/capture input.                                                                |
|         | UART0_nRTS | O    | MFP5 | Request to Send output pin for UART0.                                                                |
|         | USC10_CTL0 | I/O  | MFP6 | USC10 CTL0 pin.                                                                                      |
|         | SPI0_SS    | I/O  | MFP7 | SPI0 slave select pin.                                                                               |
| 43      | PD.5       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH5    | A    | MFP2 | ADC channel 5 analog input.                                                                          |
|         | BPWM1_CH4  | I/O  | MFP4 | BPWM1 channel 4 output/capture input.                                                                |
| 44      | PF.0       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | XT_OUT     | O    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal output pin.                         |
|         | BPWM1_CH3  | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                |
|         | TM3        | I/O  | MFP5 | Timer3 event counter input / toggle output                                                           |
| 45      | PF.1       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | XT_IN      | I    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal input pin.                          |
|         | BPWM1_CH2  | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                                                |
|         | TM1_EXT    | I    | MFP5 | Timer1 external counter input                                                                        |
| 46      | nRESET     | I    | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 47      | PF.2       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ICE_DAT    | I/O  | MFP1 | Serial wired debugger data pin                                                                       |
|         | I2C0_SDA   | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.                                                             |
|         | ADC_CH6    | A    | MFP3 | ADC channel 6 analog input.                                                                          |

| Pin No. | Pin Name  | Type | MFP* | Description                           |
|---------|-----------|------|------|---------------------------------------|
|         | BPWM1_CH3 | I/O  | MFP4 | BPWM1 channel 3 output/capture input. |
| 48      | PF.3      | I/O  | MFP0 | General purpose digital I/O pin.      |
|         | ICE_CLK   | I    | MFP1 | Serial wired debugger clock pin       |
|         | I2C0_SCL  | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.          |
|         | ADC_CH7   | A    | MFP3 | ADC channel 7 analog input.           |
|         | BPWM1_CH2 | I/O  | MFP4 | BPWM1 channel 2 output/capture input. |

Table 4.3-2 NUC121 USB Series LQFP48 Pin Description

### 4.3.3 NUC121 USB Series LQFP64 Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GPx\_MFPL and SYS\_GPx\_MFPH)

PA.10 MFP5 means SYS\_GPA\_MFPH[11:8]=0x5.

PC.0 MFP0 means SYS\_GPC\_MFPL[3:0]=0x0.

| Pin No. | Pin Name    | Type | MFP* | Description                               |
|---------|-------------|------|------|-------------------------------------------|
| 1       | PB.14       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | INT0        | I    | MFP1 | External interrupt0 input pin.            |
|         | UART0_nRTS  | O    | MFP2 | Request to Send output pin for UART0.     |
|         | ADC_CH9     | A    | MFP3 | ADC channel 9 analog input.               |
|         | BPWM1_CH0   | I/O  | MFP4 | BPWM1 channel 0 output/capture input.     |
|         | SPI0_SS     | I/O  | MFP7 | SPI0 slave select pin.                    |
| 2       | PB.13       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ADC_CH10    | A    | MFP3 | ADC channel 10 analog input.              |
|         | USC10_CTL1  | I/O  | MFP6 | USC10 CTL1 pin.                           |
| 3       | PB.12       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | CLKO        | O    | MFP2 | Clock Out                                 |
|         | ADC_CH11    | A    | MFP3 | ADC channel 11 analog input.              |
|         | USC10_CTL0  | I/O  | MFP6 | USC10 CTL0 pin.                           |
| 4       | PA.11       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | I2C1_SCL    | I/O  | MFP1 | I <sup>2</sup> C1 clock pin.              |
|         | BPWM0_CH5   | I/O  | MFP4 | BPWM0 channel 5 output/capture input.     |
|         | TM0         | I/O  | MFP5 | Timer0event counter input / toggle output |
|         | USC10_CLK   | I/O  | MFP6 | USC10 clock pin.                          |
|         | USC10_DAT0  | I/O  | MFP7 | USC10 DAT0 pin.                           |
| 5       | PA.10       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | I2C1_SDA    | I/O  | MFP1 | I <sup>2</sup> C1 data input/output pin.  |
|         | BPWM0_CH4   | I/O  | MFP4 | BPWM0 channel 4 output/capture input.     |
|         | PWM0_BRAKE0 | I    | MFP5 | Brake input pin 0 of PWM0.                |
|         | USC10_DAT1  | I/O  | MFP6 | USC10 DAT1 pin.                           |
| 6       | PD.8        | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | USC10_DAT0  | I/O  | MFP6 | USC10 DAT0 pin.                           |
| 7       | PD.9        | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_BRAKE1 | I    | MFP5 | Brake input pin 1 of PWM0.                |
| 8       | PD.10       | I/O  | MFP0 | General purpose digital I/O pin.          |

| Pin No. | Pin Name        | Type | MFP* | Description                                                                      |
|---------|-----------------|------|------|----------------------------------------------------------------------------------|
|         | CLKO            | O    | MFP1 | Clock Out                                                                        |
|         | BPWM0_CH5       | I/O  | MFP4 | BPWM0 channel 5 output/capture input.                                            |
| 9       | PD.11           | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | INT1            | I    | MFP1 | External interrupt1 input pin.                                                   |
|         | BPWM0_CH4       | I/O  | MFP4 | BPWM0 channel 4 output/capture input.                                            |
| 10      | PB.4            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH3       | I/O  | MFP4 | BPWM0 channel 3 output/capture input.                                            |
|         | TM2_EXT         | I    | MFP5 | Timer2 external counter input                                                    |
|         | USC10_CTL0      | I/O  | MFP6 | USC10 CTL0 pin.                                                                  |
|         | USC10_DAT0      | I/O  | MFP7 | USC10 DAT0 pin.                                                                  |
| 11      | PB.5            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH2       | I/O  | MFP4 | BPWM0 channel 2 output/capture input.                                            |
|         | TM3             | I/O  | MFP5 | Timer3 event counter input / toggle output                                       |
|         | USC10_CLK       | I/O  | MFP6 | USC10 clock pin.                                                                 |
|         | USC10_DAT1      | I/O  | MFP7 | USC10 DAT1 pin.                                                                  |
| 12      | PB.6            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH1       | I/O  | MFP4 | BPWM0 channel 1 output/capture input.                                            |
|         | USC10_DAT0      | I/O  | MFP6 | USC10 DAT0 pin.                                                                  |
|         | USC10_CTL1      | I/O  | MFP7 | USC10 CTL1 pin.                                                                  |
| 13      | PB.7            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH0       | I/O  | MFP4 | BPWM0 channel 0 output/capture input.                                            |
|         | USC10_DAT1      | I/O  | MFP6 | USC10 DAT1 pin.                                                                  |
|         | USC10_CTL0      | I/O  | MFP7 | USC10 CTL0 pin.                                                                  |
| 14      | LDO_CAP         | A    | MFP0 | LDO output pin.                                                                  |
| 15      | V <sub>DD</sub> | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |
| 16      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                  |
| 17      | USB_VBUS        | A    | MFP0 | Power supply from USB host or HUB.                                               |
| 18      | USB_VDD33_CAP   | A    | MFP0 | Internal power regulator output 3.3V decoupling pin.                             |
| 19      | USB_D-          | I    | MFP0 | USB differential signal D-.                                                      |
| 20      | USB_D+          | I    | MFP0 | USB differential signal D+.                                                      |
| 21      | PB.0            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | UART0_RXD       | I    | MFP1 | Data receiver input pin for UART0.                                               |
|         | PWM1_CH0        | I/O  | MFP4 | PWM1 channel0 output/capture input.                                              |

| Pin No. | Pin Name     | Type | MFP* | Description                              |
|---------|--------------|------|------|------------------------------------------|
| 22      | PB.1         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_TXD    | O    | MFP1 | Data transmitter output pin for UART0.   |
|         | PWM1_CH1     | I/O  | MFP4 | PWM1 channel1 output/capture input.      |
| 23      | PB.2         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_nRTS   | O    | MFP1 | Request to Send output pin for UART0.    |
|         | TM2_EXT      | I    | MFP2 | Timer2 external counter input            |
|         | PWM1_CH2     | I/O  | MFP4 | PWM1 channel2 output/capture input.      |
| 24      | PB.3         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_nCTS   | I    | MFP1 | Clear to Send input pin for UART0.       |
|         | TM3_EXT      | I    | MFP2 | Timer3 external counter input            |
|         | PWM1_CH3     | I/O  | MFP4 | PWM1 channel3 output/capture input.      |
| 25      | PC.5         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_TXD    | O    | MFP2 | Data transmitter output pin for UART0.   |
|         | PWM1_CH5     | I/O  | MFP4 | PWM1 channel5 output/capture input.      |
|         | USC10_DAT0   | I/O  | MFP7 | USC10 DAT0 pin.                          |
| 26      | PC.4         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_RXD    | I    | MFP2 | Data receiver input pin for UART0.       |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.            |
|         | PWM1_CH4     | I/O  | MFP4 | PWM1 channel4 output/capture input.      |
|         | USC10_DAT1   | I/O  | MFP7 | USC10 DAT1 pin.                          |
| 27      | PC.3         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | SPI0_MOSI    | I/O  | MFP1 | SPI0 MOSI (Master Out, Slave In) pin.    |
|         | I2C1_SDA     | I/O  | MFP3 | I <sup>2</sup> C1 data input/output pin. |
|         | PWM1_CH3     | I/O  | MFP4 | PWM1 channel3 output/capture input.      |
|         | UART0_nRTS   | O    | MFP6 | Request to Send output pin for UART0.    |
|         | USC10_DAT0   | I/O  | MFP7 | USC10 DAT0 pin.                          |
| 28      | PC.2         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | SPI0_MISO    | I/O  | MFP1 | SPI0 MISO (Master In, Slave Out) pin.    |
|         | I2C1_SCL     | I/O  | MFP3 | I <sup>2</sup> C1 clock pin.             |
|         | PWM1_CH2     | I/O  | MFP4 | PWM1 channel2 output/capture input.      |
|         | UART0_nCTS   | I    | MFP6 | Clear to Send input pin for UART0.       |
|         | USC10_DAT1   | I/O  | MFP7 | USC10 DAT1 pin.                          |
| 29      | PC.1         | I/O  | MFP0 | General purpose digital I/O pin.         |

| Pin No. | Pin Name     | Type | MFP* | Description                                |
|---------|--------------|------|------|--------------------------------------------|
|         | SPI0_CLK     | I/O  | MFP1 | SPI0 serial clock pin.                     |
|         | PWM1_CH1     | I/O  | MFP4 | PWM1 channel1 output/capture input.        |
|         | UART0_TXD    | O    | MFP6 | Data transmitter output pin for UART0.     |
|         | USC0_CTL0    | I/O  | MFP7 | USC0 CTL0 pin                              |
| 30      | PC.0         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_SS      | I/O  | MFP1 | SPI0 slave select pin.                     |
|         | PWM1_CH0     | I/O  | MFP4 | PWM1 channel0 output/capture input.        |
|         | TM2          | I/O  | MFP5 | Timer2 event counter input / toggle output |
|         | UART0_RXD    | I    | MFP6 | Data receiver input pin for UART0.         |
|         | USC0_CLK     | I/O  | MFP7 | USC0 clock pin.                            |
| 31      | PB.10        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM2          | I/O  | MFP1 | Timer2 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH5     | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
| 32      | PB.9         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM1          | I/O  | MFP1 | Timer1 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH4     | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
| 33      | PE.2         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | INT1         | I    | MFP1 | External interrupt1 input pin.             |
|         | TM0_EXT      | I    | MFP5 | Timer0 external counter input              |
|         | I2C0_SCL     | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |
|         | USC0_CTL1    | I/O  | MFP7 | USC0 CTL1 pin.                             |
| 34      | PC.13        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3     | I/O  | MFP2 | PWM0 channel3 output/capture input.        |
|         | CLKO         | O    | MFP3 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SDA     | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
| 35      | PC.12        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2     | I/O  | MFP2 | PWM0 channel2 output/capture input.        |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | CLKO         | O    | MFP4 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |

| Pin No. | Pin Name    | Type | MFP* | Description                                |
|---------|-------------|------|------|--------------------------------------------|
|         | I2C0_SCL    | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |
|         | USC10_CTL1  | I/O  | MFP7 | USC10 CTL1 pin.                            |
| 36      | PC.11       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MOSI   | I/O  | MFP3 | SPI0 MOSI (Master Out, Slave In) pin.      |
|         | PWM0_CH1    | I/O  | MFP4 | PWM0 channel1 output/capture input.        |
|         | TM1         | I/O  | MFP5 | Timer1 event counter input / toggle output |
|         | I2C0_SDA    | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
|         | USC10_DAT0  | I/O  | MFP7 | USC10 DAT0 pin.                            |
| 37      | PC.10       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MISO   | I/O  | MFP3 | SPI0 MISO (Master In, Slave Out) pin.      |
|         | PWM0_CH0    | I/O  | MFP4 | PWM0 channel0 output/capture input.        |
|         | USC10_DAT1  | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 38      | PE.1        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC       | I    | MFP2 | ADC external trigger input.                |
|         | CLKO        | O    | MFP3 | Clock Out                                  |
|         | TM3         | I/O  | MFP5 | Timer3 event counter input / toggle output |
|         | USC10_DAT1  | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 39      | PC.9        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK    | I/O  | MFP3 | SPI0 serial clock pin.                     |
|         | PWM0_CH5    | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
|         | PWM0_BRAKE1 | I    | MFP5 | Brake input pin 1 of PWM0.                 |
|         | USC10_CLK   | I/O  | MFP7 | USC10 clock pin                            |
| 40      | PC.8        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC       | I    | MFP2 | ADC external trigger input.                |
|         | SPI0_SS     | I/O  | MFP3 | SPI0 slave select pin.                     |
|         | PWM0_CH4    | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
|         | PWM1_BRAKE0 | I    | MFP5 | Brake input pin 0 of PWM1.                 |
|         | USC10_CTL0  | I/O  | MFP7 | USC10 CTL0 pin                             |
| 41      | PA.15       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3    | I/O  | MFP1 | PWM0 channel3 output/capture input.        |
|         | SPI_I2SMCLK | O    | MFP2 | I2S0 master clock output pin.              |
|         | CLKO        | O    | MFP3 | Clock Out                                  |
|         | PWM1_BRAKE1 | I    | MFP4 | Brake input pin 1 of PWM1.                 |

| Pin No. | Pin Name         | Type | MFP* | Description                               |
|---------|------------------|------|------|-------------------------------------------|
|         | UART0_nRTS       | O    | MFP5 | Request to Send output pin for UART0.     |
| 42      | PE.0             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | INT0             | I    | MFP1 | External interrupt0 input pin.            |
|         | CLKO             | O    | MFP3 | Clock Out                                 |
|         | PWM0_CH3         | I/O  | MFP4 | PWM0 channel3 output/capture input.       |
|         | TM1_EXT          | I    | MFP5 | Timer1 external counter input             |
|         | USC10_DAT0       | I/O  | MFP7 | USC10 DAT0 pin.                           |
| 43      | PA.14            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH2         | I/O  | MFP1 | PWM0 channel2 output/capture input.       |
|         | UART0_nCTS       | I    | MFP3 | Clear to Send input pin for UART0.        |
|         | PWM0_BRAKE0      | I    | MFP4 | Brake input pin 0 of PWM0.                |
| 44      | PA.13            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH1         | I/O  | MFP1 | PWM0 channel1 output/capture input.       |
|         | I2C1_SDA         | I/O  | MFP2 | I <sup>2</sup> C1 data input/output pin.  |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.    |
| 45      | PA.12            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH0         | I/O  | MFP1 | PWM0 channel0 output/capture input.       |
|         | I2C1_SCL         | I/O  | MFP2 | I <sup>2</sup> C1 clock pin.              |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.        |
| 46      | PF.4             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ICE_DAT          | I/O  | MFP1 | Serial wired debugger data pin            |
|         | I2C0_SDA         | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.  |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.    |
|         | PWM0_CH3         | I/O  | MFP4 | PWM0 channel3 output/capture input.       |
| 47      | PF.5             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ICE_CLK          | I    | MFP1 | Serial wired debugger clock pin           |
|         | I2C0_SCL         | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.              |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.        |
| 48      | AV <sub>DD</sub> | A    | MFP0 | Power supply for internal analog circuit. |
| 49      | PD.0             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ADC_CH0          | A    | MFP3 | ADC channel 0 analog input.               |
|         | UART0_nRTS       | O    | MFP5 | Request to Send output pin for UART0.     |
|         | USC10_CTL0       | I/O  | MFP6 | USC10 CTL0 pin.                           |

| Pin No. | Pin Name   | Type | MFP* | Description                                |
|---------|------------|------|------|--------------------------------------------|
|         | SPI0_SS    | I/O  | MFP7 | SPI0 slave select pin.                     |
| 50      | PD.1       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH1    | A    | MFP3 | ADC channel 1 analog input.                |
|         | TM0_EXT    | I    | MFP4 | Timer0 external counter input              |
|         | UART0_RXD  | I    | MFP5 | Data receiver input pin for UART0.         |
|         | USC10_CLK  | I/O  | MFP6 | USC10 clock pin.                           |
|         | SPI0_CLK   | I/O  | MFP7 | SPI0 serial clock pin.                     |
| 51      | PD.2       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH2    | A    | MFP3 | ADC channel 2 analog input.                |
|         | TM3        | I/O  | MFP4 | Timer3 event counter input / toggle output |
|         | UART0_TXD  | O    | MFP5 | Data transmitter output pin for UART0.     |
|         | USC10_DAT1 | I/O  | MFP6 | USC10 DAT1 pin.                            |
|         | SPI0_MISO  | I/O  | MFP7 | SPI0 MISO (Master In, Slave Out) pin.      |
| 52      | PD.3       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH3    | A    | MFP3 | ADC channel 3 analog input.                |
|         | TM1_EXT    | I    | MFP4 | Timer1 external counter input              |
|         | UART0_nCTS | I    | MFP5 | Clear to Send input pin for UART0.         |
|         | USC10_DAT0 | I/O  | MFP6 | USC10 DAT0 pin.                            |
|         | SPI0_MOSI  | I/O  | MFP7 | SPI0 MOSI (Master Out, Slave In) pin.      |
| 53      | PD.4       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH4    | A    | MFP2 | ADC channel 4 analog input.                |
|         | BPWM1_CH5  | I/O  | MFP4 | BPWM1 channel 5 output/capture input.      |
|         | UART0_nRTS | O    | MFP5 | Request to Send output pin for UART0.      |
|         | USC10_CTL0 | I/O  | MFP6 | USC10 CTL0 pin.                            |
|         | SPI0_SS    | I/O  | MFP7 | SPI0 slave select pin.                     |
| 54      | PD.5       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH5    | A    | MFP2 | ADC channel 5 analog input.                |
|         | BPWM1_CH4  | I/O  | MFP4 | BPWM1 channel 4 output/capture input.      |
| 55      | PB.15      | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | INT1       | I    | MFP1 | External interrupt1 input pin.             |
|         | TM0_EXT    | I    | MFP2 | Timer0 external counter input              |
|         | BPWM1_CH5  | I/O  | MFP4 | BPWM1 channel 5 output/capture input.      |
| 56      | PF.0       | I/O  | MFP0 | General purpose digital I/O pin.           |

| Pin No. | Pin Name        | Type | MFP* | Description                                                                                          |
|---------|-----------------|------|------|------------------------------------------------------------------------------------------------------|
|         | XT_OUT          | O    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal output pin.                         |
|         | BPWM1_CH3       | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                |
|         | TM3             | I/O  | MFP5 | Timer3 event counter input / toggle output                                                           |
| 57      | PF.1            | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | XT_IN           | I    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal input pin.                          |
|         | BPWM1_CH2       | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                                                |
|         | TM1_EXT         | I    | MFP5 | Timer1 external counter input                                                                        |
| 58      | nRESET          | I    | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 59      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                                      |
| 60      | V <sub>DD</sub> | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function.                     |
| 61      | PF.2            | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ICE_DAT         | I/O  | MFP1 | Serial wired debugger data pin                                                                       |
|         | I2C0_SDA        | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.                                                             |
|         | ADC_CH6         | A    | MFP3 | ADC channel 6 analog input.                                                                          |
|         | BPWM1_CH3       | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                |
| 62      | PF.3            | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ICE_CLK         | I    | MFP1 | Serial wired debugger clock pin                                                                      |
|         | I2C0_SCL        | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.                                                                         |
|         | ADC_CH7         | A    | MFP3 | ADC channel 7 analog input.                                                                          |
|         | BPWM1_CH2       | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                                                |
| 63      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                                      |
| 64      | PB.8            | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | TM0             | I/O  | MFP1 | Timer0event counter input / toggle output                                                            |
|         | ADC_CH8         | A    | MFP3 | ADC channel 8 analog input.                                                                          |
|         | BPWM1_CH1       | I/O  | MFP4 | BPWM1 channel 1 output/capture input.                                                                |

Table 4.3-3 NUC121 USB Series LQFP64 Pin Description

#### 4.3.4 NUC125 USB Series QFN33 Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GPx\_MFPL and SYS\_GPx\_MFPH)

PA.10 MFP5 means SYS\_GPA\_MFPH[11:8]=0x5.

PC.0 MFP0 means SYS\_GPC\_MFPL[3:0]=0x0.

| Pin No. | Pin Name        | Type | MFP* | Description                                                                      |
|---------|-----------------|------|------|----------------------------------------------------------------------------------|
| 1       | PB.14           | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | INT0            | I    | MFP1 | External interrupt0 input pin.                                                   |
|         | UART0_nRTS      | O    | MFP2 | Request to Send output pin for UART0.                                            |
|         | ADC_CH9         | A    | MFP3 | ADC channel 9 analog input.                                                      |
|         | BPWM1_CH0       | I/O  | MFP4 | BPWM1 channel 0 output/capture input.                                            |
|         | SPI0_SS         | I/O  | MFP7 | SPI0 slave select pin.                                                           |
| 2       | PA.11           | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | I2C1_SCL        | I/O  | MFP1 | I <sup>2</sup> C1 clock pin.                                                     |
|         | BPWM0_CH5       | I/O  | MFP4 | BPWM0 channel 5 output/capture input.                                            |
|         | TM0             | I/O  | MFP5 | Timer0event counter input / toggle output                                        |
|         | USCI0_CLK       | I/O  | MFP6 | USCI0 clock pin.                                                                 |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                                                  |
| 3       | PA.10           | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | I2C1_SDA        | I/O  | MFP1 | I <sup>2</sup> C1 data input/output pin.                                         |
|         | BPWM0_CH4       | I/O  | MFP4 | BPWM0 channel 4 output/capture input.                                            |
|         | PWM0_BRAKE0     | I    | MFP5 | Brake input pin 0 of PWM0.                                                       |
|         | USCI0_DAT1      | I/O  | MFP6 | USCI0 DAT1 pin.                                                                  |
| 4       | PB.4            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH3       | I/O  | MFP4 | BPWM0 channel 3 output/capture input.                                            |
|         | TM2_EXT         | I    | MFP5 | Timer2 external counter input                                                    |
|         | USCI0_CTL0      | I/O  | MFP6 | USCI0 CTL0 pin.                                                                  |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                                                  |
| 5       | PB.5            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH2       | I/O  | MFP4 | BPWM0 channel 2 output/capture input.                                            |
|         | TM3             | I/O  | MFP5 | Timer3 event counter input / toggle output                                       |
|         | USCI0_CLK       | I/O  | MFP6 | USCI0 clock pin.                                                                 |
|         | USCI0_DAT1      | I/O  | MFP7 | USCI0 DAT1 pin.                                                                  |
| 6       | LDO_CAP         | A    | MFP0 | LDO output pin.                                                                  |
| 7       | V <sub>DD</sub> | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |

| Pin No. | Pin Name        | Type | MFP* | Description                                          |
|---------|-----------------|------|------|------------------------------------------------------|
| 8       | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                      |
| 9       | USB_VBUS        | A    | MFP0 | Power supply from USB host or HUB.                   |
| 10      | USB_VDD33_CAP   | A    | MFP0 | Internal power regulator output 3.3V decoupling pin. |
| 11      | USB_D-          | I    | MFP0 | USB differential signal D-.                          |
| 12      | USB_D+          | I    | MFP0 | USB differential signal D+.                          |
| 13      | PC.3            | I/O  | MFP0 | General purpose digital I/O pin.                     |
|         | SPI0_MOSI       | I/O  | MFP1 | SPI0 MOSI (Master Out, Slave In) pin.                |
|         | I2C1_SDA        | I/O  | MFP3 | I <sup>2</sup> C1 data input/output pin.             |
|         | PWM1_CH3        | I/O  | MFP4 | PWM1 channel3 output/capture input.                  |
|         | UART0_nRTS      | O    | MFP6 | Request to Send output pin for UART0.                |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                      |
| 14      | PC.2            | I/O  | MFP0 | General purpose digital I/O pin.                     |
|         | SPI0_MISO       | I/O  | MFP1 | SPI0 MISO (Master In, Slave Out) pin.                |
|         | I2C1_SCL        | I/O  | MFP3 | I <sup>2</sup> C1 clock pin.                         |
|         | PWM1_CH2        | I/O  | MFP4 | PWM1 channel2 output/capture input.                  |
|         | UART0_nCTS      | I    | MFP6 | Clear to Send input pin for UART0.                   |
|         | USCI0_DAT1      | I/O  | MFP7 | USCI0 DAT1 pin.                                      |
| 15      | PC.1            | I/O  | MFP0 | General purpose digital I/O pin.                     |
|         | SPI0_CLK        | I/O  | MFP1 | SPI0 serial clock pin.                               |
|         | PWM1_CH1        | I/O  | MFP4 | PWM1 channel1 output/capture input.                  |
|         | UART0_TXD       | O    | MFP6 | Data transmitter output pin for UART0.               |
|         | USCI0_CTL0      | I/O  | MFP7 | USCI0 CTL0 pin                                       |
| 16      | PC.0            | I/O  | MFP0 | General purpose digital I/O pin.                     |
|         | SPI0_SS         | I/O  | MFP1 | SPI0 slave select pin.                               |
|         | PWM1_CH0        | I/O  | MFP4 | PWM1 channel0 output/capture input.                  |
|         | TM2             | I/O  | MFP5 | Timer2 event counter input / toggle output           |
|         | UART0_RXD       | I    | MFP6 | Data receiver input pin for UART0.                   |
|         | USCI0_CLK       | I/O  | MFP7 | USCI0 clock pin.                                     |
| 17      | PC.13           | I/O  | MFP0 | General purpose digital I/O pin.                     |
|         | PWM0_CH3        | I/O  | MFP2 | PWM0 channel3 output/capture input.                  |
|         | CLKO            | O    | MFP3 | Clock Out                                            |
|         | INT0            | I    | MFP5 | External interrupt0 input pin.                       |
|         | I2C0_SDA        | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.             |

| Pin No. | Pin Name     | Type | MFP* | Description                                |
|---------|--------------|------|------|--------------------------------------------|
| 18      | PC.12        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2     | I/O  | MFP2 | PWM0 channel2 output/capture input.        |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | CLKO         | O    | MFP4 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SCL     | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |
|         | USCI0_CTL1   | I/O  | MFP7 | USCI0 CTL1 pin.                            |
| 19      | PC.11        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MOSI    | I/O  | MFP3 | SPI0 MOSI (Master Out, Slave In) pin.      |
|         | PWM0_CH1     | I/O  | MFP4 | PWM0 channel1 output/capture input.        |
|         | TM1          | I/O  | MFP5 | Timer1 event counter input / toggle output |
|         | I2C0_SDA     | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
|         | USCI0_DAT0   | I/O  | MFP7 | USCI0 DAT0 pin.                            |
| 20      | PC.10        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MISO    | I/O  | MFP3 | SPI0 MISO (Master In, Slave Out) pin.      |
|         | PWM0_CH0     | I/O  | MFP4 | PWM0 channel0 output/capture input.        |
|         | USCI0_DAT1   | I/O  | MFP7 | USCI0 DAT1 pin.                            |
| 21      | PC.9         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK     | I/O  | MFP3 | SPI0 serial clock pin.                     |
|         | PWM0_CH5     | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
|         | PWM0_BRAKE1  | I    | MFP5 | Brake input pin 1 of PWM0.                 |
|         | USCI0_CLK    | I/O  | MFP7 | USCI0 clock pin                            |
| 22      | PC.8         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC        | I    | MFP2 | ADC external trigger input.                |
|         | SPI0_SS      | I/O  | MFP3 | SPI0 slave select pin.                     |
|         | PWM0_CH4     | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
|         | PWM1_BRAKE0  | I    | MFP5 | Brake input pin 0 of PWM1.                 |
|         | USCI0_CTL0   | I/O  | MFP7 | USCI0 CTL0 pin                             |
| 23      | PF.4         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ICE_DAT      | I/O  | MFP1 | Serial wired debugger data pin             |
|         | I2C0_SDA     | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.   |
|         | UART0_TXD    | O    | MFP3 | Data transmitter output pin for UART0.     |
|         | PWM0_CH3     | I/O  | MFP4 | PWM0 channel3 output/capture input.        |

| Pin No. | Pin Name         | Type | MFP* | Description                                                                                          |
|---------|------------------|------|------|------------------------------------------------------------------------------------------------------|
| 24      | PF.5             | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ICE_CLK          | I    | MFP1 | Serial wired debugger clock pin                                                                      |
|         | I2C0_SCL         | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.                                                                         |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.                                                                   |
| 25      | AV <sub>DD</sub> | A    | MFP0 | Power supply for internal analog circuit.                                                            |
| 26      | PD.1             | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH1          | A    | MFP3 | ADC channel 1 analog input.                                                                          |
|         | TM0_EXT          | I    | MFP4 | Timer0 external counter input                                                                        |
|         | UART0_RXD        | I    | MFP5 | Data receiver input pin for UART0.                                                                   |
|         | USC10_CLK        | I/O  | MFP6 | USC10 clock pin.                                                                                     |
|         | SPI0_CLK         | I/O  | MFP7 | SPI0 serial clock pin.                                                                               |
| 27      | PD.2             | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH2          | A    | MFP3 | ADC channel 2 analog input.                                                                          |
|         | TM3              | I/O  | MFP4 | Timer3 event counter input / toggle output                                                           |
|         | UART0_TXD        | O    | MFP5 | Data transmitter output pin for UART0.                                                               |
|         | USC10_DAT1       | I/O  | MFP6 | USC10 DAT1 pin.                                                                                      |
|         | SPI0_MISO        | I/O  | MFP7 | SPI0 MISO (Master In, Slave Out) pin.                                                                |
| 28      | PD.3             | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH3          | A    | MFP3 | ADC channel 3 analog input.                                                                          |
|         | TM1_EXT          | I    | MFP4 | Timer1 external counter input                                                                        |
|         | UART0_nCTS       | I    | MFP5 | Clear to Send input pin for UART0.                                                                   |
|         | USC10_DAT0       | I/O  | MFP6 | USC10 DAT0 pin.                                                                                      |
|         | SPI0_MOSI        | I/O  | MFP7 | SPI0 MOSI (Master Out, Slave In) pin.                                                                |
| 29      | PF.0             | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | XT_OUT           | O    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal output pin.                         |
|         | BPWM1_CH3        | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                |
|         | TM3              | I/O  | MFP5 | Timer3 event counter input / toggle output                                                           |
| 30      | PF.1             | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | XT_IN            | I    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal input pin.                          |
|         | BPWM1_CH2        | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                                                |
|         | TM1_EXT          | I    | MFP5 | Timer1 external counter input                                                                        |
| 31      | nRESET           | I    | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |

| Pin No. | Pin Name          | Type | MFP* | Description                                          |
|---------|-------------------|------|------|------------------------------------------------------|
| 32      | V <sub>DDIO</sub> | A    | MFP0 | Power supply for PB.14, PA.11, PA.10, PB.4 and PB.5. |
| 33      | V <sub>SS</sub>   | A    | MFP0 | Ground pin for digital circuit.                      |

Table 4.3-4 NUC125 USB Series QFN33 Pin Description

### 4.3.5 NUC125 USB Series LQFP48 Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GPx\_MFPL and SYS\_GPx\_MFPH)

PA.10 MFP5 means SYS\_GPA\_MFPH[11:8]=0x5.

PC.0 MFP0 means SYS\_GPC\_MFPL[3:0]=0x0..

| Pin No. | Pin Name          | Type | MFP* | Description                                                      |
|---------|-------------------|------|------|------------------------------------------------------------------|
| 1       | V <sub>SS</sub>   | A    | MFP0 | Ground pin for digital circuit.                                  |
| 2       | V <sub>DDIO</sub> | A    | MFP0 | Power supply for PB.14, PA.11, PA.10, PB.4, PB.5, PB.6 and PB.7. |
| 3       | PB.14             | I/O  | MFP0 | General purpose digital I/O pin.                                 |
|         | INT0              | I    | MFP1 | External interrupt0 input pin.                                   |
|         | UART0_nRTS        | O    | MFP2 | Request to Send output pin for UART0.                            |
|         | ADC_CH9           | A    | MFP3 | ADC channel 9 analog input.                                      |
|         | BPWM1_CH0         | I/O  | MFP4 | BPWM1 channel 0 output/capture input.                            |
|         | SPI0_SS           | I/O  | MFP7 | SPI0 slave select pin.                                           |
| 4       | PA.11             | I/O  | MFP0 | General purpose digital I/O pin.                                 |
|         | I2C1_SCL          | I/O  | MFP1 | I <sup>2</sup> C1 clock pin.                                     |
|         | BPWM0_CH5         | I/O  | MFP4 | BPWM0 channel 5 output/capture input.                            |
|         | TM0               | I/O  | MFP5 | Timer0event counter input / toggle output                        |
|         | USC10_CLK         | I/O  | MFP6 | USC10 clock pin.                                                 |
|         | USC10_DAT0        | I/O  | MFP7 | USC10 DAT0 pin.                                                  |
| 5       | PA.10             | I/O  | MFP0 | General purpose digital I/O pin.                                 |
|         | I2C1_SDA          | I/O  | MFP1 | I <sup>2</sup> C1 data input/output pin.                         |
|         | BPWM0_CH4         | I/O  | MFP4 | BPWM0 channel 4 output/capture input.                            |
|         | PWM0_BRAKE0       | I    | MFP5 | Brake input pin 0 of PWM0.                                       |
|         | USC10_DAT1        | I/O  | MFP6 | USC10 DAT1 pin.                                                  |
| 6       | PB.4              | I/O  | MFP0 | General purpose digital I/O pin.                                 |
|         | BPWM0_CH3         | I/O  | MFP4 | BPWM0 channel 3 output/capture input.                            |
|         | TM2_EXT           | I    | MFP5 | Timer2 external counter input                                    |
|         | USC10_CTL0        | I/O  | MFP6 | USC10 CTL0 pin.                                                  |
|         | USC10_DAT0        | I/O  | MFP7 | USC10 DAT0 pin.                                                  |
| 7       | PB.5              | I/O  | MFP0 | General purpose digital I/O pin.                                 |
|         | BPWM0_CH2         | I/O  | MFP4 | BPWM0 channel 2 output/capture input.                            |
|         | TM3               | I/O  | MFP5 | Timer3 event counter input / toggle output                       |
|         | USC10_CLK         | I/O  | MFP6 | USC10 clock pin.                                                 |
|         | USC10_DAT1        | I/O  | MFP7 | USC10 DAT1 pin.                                                  |

| Pin No. | Pin Name        | Type | MFP* | Description                                                                      |
|---------|-----------------|------|------|----------------------------------------------------------------------------------|
| 8       | PB.6            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH1       | I/O  | MFP4 | BPWM0 channel 1 output/capture input.                                            |
|         | USCI0_DAT0      | I/O  | MFP6 | USCI0 DAT0 pin.                                                                  |
|         | USCI0_CTL1      | I/O  | MFP7 | USCI0 CTL1 pin.                                                                  |
| 9       | PB.7            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH0       | I/O  | MFP4 | BPWM0 channel 0 output/capture input.                                            |
|         | USCI0_DAT1      | I/O  | MFP6 | USCI0 DAT1 pin.                                                                  |
|         | USCI0_CTL0      | I/O  | MFP7 | USCI0 CTL0 pin.                                                                  |
| 10      | LDO_CAP         | A    | MFP0 | LDO output pin.                                                                  |
| 11      | V <sub>DD</sub> | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |
| 12      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                  |
| 13      | USB_VBUS        | A    | MFP0 | Power supply from USB host or HUB.                                               |
| 14      | USB_VDD33_CAP   | A    | MFP0 | Internal power regulator output 3.3V decoupling pin.                             |
| 15      | USB_D-          | I    | MFP0 | USB differential signal D-.                                                      |
| 16      | USB_D+          | I    | MFP0 | USB differential signal D+.                                                      |
| 17      | PC.5            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | UART0_TXD       | O    | MFP2 | Data transmitter output pin for UART0.                                           |
|         | PWM1_CH5        | I/O  | MFP4 | PWM1 channel5 output/capture input.                                              |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                                                  |
| 18      | PC.4            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | UART0_RXD       | I    | MFP2 | Data receiver input pin for UART0.                                               |
|         | SPI0_I2SMCLK    | O    | MFP3 | I2S0 master clock output pin.                                                    |
|         | PWM1_CH4        | I/O  | MFP4 | PWM1 channel4 output/capture input.                                              |
|         | USCI0_DAT1      | I/O  | MFP7 | USCI0 DAT1 pin.                                                                  |
| 19      | PC.3            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | SPI0_MOSI       | I/O  | MFP1 | SPI0 MOSI (Master Out, Slave In) pin.                                            |
|         | I2C1_SDA        | I/O  | MFP3 | I <sup>2</sup> C1 data input/output pin.                                         |
|         | PWM1_CH3        | I/O  | MFP4 | PWM1 channel3 output/capture input.                                              |
|         | UART0_nRTS      | O    | MFP6 | Request to Send output pin for UART0.                                            |
|         | USCI0_DAT0      | I/O  | MFP7 | USCI0 DAT0 pin.                                                                  |
| 20      | PC.2            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | SPI0_MISO       | I/O  | MFP1 | SPI0 MISO (Master In, Slave Out) pin.                                            |
|         | I2C1_SCL        | I/O  | MFP3 | I <sup>2</sup> C1 clock pin.                                                     |

| Pin No. | Pin Name     | Type | MFP* | Description                                |
|---------|--------------|------|------|--------------------------------------------|
|         | PWM1_CH2     | I/O  | MFP4 | PWM1 channel2 output/capture input.        |
|         | UART0_nCTS   | I    | MFP6 | Clear to Send input pin for UART0.         |
|         | USC10_DAT1   | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 21      | PC.1         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK     | I/O  | MFP1 | SPI0 serial clock pin.                     |
|         | PWM1_CH1     | I/O  | MFP4 | PWM1 channel1 output/capture input.        |
|         | UART0_TXD    | O    | MFP6 | Data transmitter output pin for UART0.     |
|         | USC10_CTL0   | I/O  | MFP7 | USC10 CTL0 pin                             |
| 22      | PC.0         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_SS      | I/O  | MFP1 | SPI0 slave select pin.                     |
|         | PWM1_CH0     | I/O  | MFP4 | PWM1 channel0 output/capture input.        |
|         | TM2          | I/O  | MFP5 | Timer2 event counter input / toggle output |
|         | UART0_RXD    | I    | MFP6 | Data receiver input pin for UART0.         |
|         | USC10_CLK    | I/O  | MFP7 | USC10 clock pin.                           |
| 23      | PB.10        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM2          | I/O  | MFP1 | Timer2 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH5     | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
| 24      | PB.9         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM1          | I/O  | MFP1 | Timer1 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH4     | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
| 25      | PC.13        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3     | I/O  | MFP2 | PWM0 channel3 output/capture input.        |
|         | CLKO         | O    | MFP3 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SDA     | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
| 26      | PC.12        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2     | I/O  | MFP2 | PWM0 channel2 output/capture input.        |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | CLKO         | O    | MFP4 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SCL     | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |

| Pin No. | Pin Name    | Type | MFP* | Description                                |
|---------|-------------|------|------|--------------------------------------------|
|         | USC10_CTL1  | I/O  | MFP7 | USC10 CTL1 pin.                            |
| 27      | PC.11       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MOSI   | I/O  | MFP3 | SPI0 MOSI (Master Out, Slave In) pin.      |
|         | PWM0_CH1    | I/O  | MFP4 | PWM0 channel1 output/capture input.        |
|         | TM1         | I/O  | MFP5 | Timer1 event counter input / toggle output |
|         | I2C0_SDA    | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
|         | USC10_DAT0  | I/O  | MFP7 | USC10 DAT0 pin.                            |
| 28      | PC.10       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MISO   | I/O  | MFP3 | SPI0 MISO (Master In, Slave Out) pin.      |
|         | PWM0_CH0    | I/O  | MFP4 | PWM0 channel0 output/capture input.        |
|         | USC10_DAT1  | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 29      | PC.9        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK    | I/O  | MFP3 | SPI0 serial clock pin.                     |
|         | PWM0_CH5    | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
|         | PWM0_BRAKE1 | I    | MFP5 | Brake input pin 1 of PWM0.                 |
|         | USC10_CLK   | I/O  | MFP7 | USC10 clock pin                            |
| 30      | PC.8        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC       | I    | MFP2 | ADC external trigger input.                |
|         | SPI0_SS     | I/O  | MFP3 | SPI0 slave select pin.                     |
|         | PWM0_CH4    | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
|         | PWM1_BRAKE0 | I    | MFP5 | Brake input pin 0 of PWM1.                 |
|         | USC10_CTL0  | I/O  | MFP7 | USC10 CTL0 pin                             |
| 31      | PA.15       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3    | I/O  | MFP1 | PWM0 channel3 output/capture input.        |
|         | SPI_I2SMCLK | O    | MFP2 | I2S0 master clock output pin.              |
|         | CLKO        | O    | MFP3 | Clock Out                                  |
|         | PWM1_BRAKE1 | I    | MFP4 | Brake input pin 1 of PWM1.                 |
|         | UART0_nRTS  | O    | MFP5 | Request to Send output pin for UART0.      |
| 32      | PA.14       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2    | I/O  | MFP1 | PWM0 channel2 output/capture input.        |
|         | UART0_nCTS  | I    | MFP3 | Clear to Send input pin for UART0.         |
|         | PWM0_BRAKE0 | I    | MFP4 | Brake input pin 0 of PWM0.                 |
| 33      | PA.13       | I/O  | MFP0 | General purpose digital I/O pin.           |

| Pin No. | Pin Name         | Type | MFP* | Description                                |
|---------|------------------|------|------|--------------------------------------------|
|         | PWM0_CH1         | I/O  | MFP1 | PWM0 channel1 output/capture input.        |
|         | I2C1_SDA         | I/O  | MFP2 | I <sup>2</sup> C1 data input/output pin.   |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.     |
| 34      | PA.12            | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH0         | I/O  | MFP1 | PWM0 channel0 output/capture input.        |
|         | I2C1_SCL         | I/O  | MFP2 | I <sup>2</sup> C1 clock pin.               |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.         |
| 35      | PF.4             | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ICE_DAT          | I/O  | MFP1 | Serial wired debugger data pin             |
|         | I2C0_SDA         | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.   |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.     |
|         | PWM0_CH3         | I/O  | MFP4 | PWM0 channel3 output/capture input.        |
| 36      | PF.5             | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ICE_CLK          | I    | MFP1 | Serial wired debugger clock pin            |
|         | I2C0_SCL         | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.               |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.         |
| 37      | AV <sub>DD</sub> | A    | MFP0 | Power supply for internal analog circuit.  |
| 38      | PD.0             | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH0          | A    | MFP3 | ADC channel 0 analog input.                |
|         | UART0_nRTS       | O    | MFP5 | Request to Send output pin for UART0.      |
|         | USCI0_CTL0       | I/O  | MFP6 | USCI0 CTL0 pin.                            |
|         | SPI0_SS          | I/O  | MFP7 | SPI0 slave select pin.                     |
| 39      | PD.1             | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH1          | A    | MFP3 | ADC channel 1 analog input.                |
|         | TM0_EXT          | I    | MFP4 | Timer0 external counter input              |
|         | UART0_RXD        | I    | MFP5 | Data receiver input pin for UART0.         |
|         | USCI0_CLK        | I/O  | MFP6 | USCI0 clock pin.                           |
|         | SPI0_CLK         | I/O  | MFP7 | SPI0 serial clock pin.                     |
| 40      | PD.2             | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH2          | A    | MFP3 | ADC channel 2 analog input.                |
|         | TM3              | I/O  | MFP4 | Timer3 event counter input / toggle output |
|         | UART0_TXD        | O    | MFP5 | Data transmitter output pin for UART0.     |
|         | USCI0_DAT1       | I/O  | MFP6 | USCI0 DAT1 pin.                            |

| Pin No. | Pin Name   | Type | MFP* | Description                                                                                          |
|---------|------------|------|------|------------------------------------------------------------------------------------------------------|
|         | SPI0_MISO  | I/O  | MFP7 | SPI0 MISO (Master In, Slave Out) pin.                                                                |
| 41      | PD.3       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH3    | A    | MFP3 | ADC channel 3 analog input.                                                                          |
|         | TM1_EXT    | I    | MFP4 | Timer1 external counter input                                                                        |
|         | UART0_nCTS | I    | MFP5 | Clear to Send input pin for UART0.                                                                   |
|         | USC0_DAT0  | I/O  | MFP6 | USC0 DAT0 pin.                                                                                       |
|         | SPI0_MOSI  | I/O  | MFP7 | SPI0 MOSI (Master Out, Slave In) pin.                                                                |
| 42      | PD.4       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH4    | A    | MFP2 | ADC channel 4 analog input.                                                                          |
|         | BPWM1_CH5  | I/O  | MFP4 | BPWM1 channel 5 output/capture input.                                                                |
|         | UART0_nRTS | O    | MFP5 | Request to Send output pin for UART0.                                                                |
|         | USC0_CTL0  | I/O  | MFP6 | USC0 CTL0 pin.                                                                                       |
|         | SPI0_SS    | I/O  | MFP7 | SPI0 slave select pin.                                                                               |
| 43      | PD.5       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ADC_CH5    | A    | MFP2 | ADC channel 5 analog input.                                                                          |
|         | BPWM1_CH4  | I/O  | MFP4 | BPWM1 channel 4 output/capture input.                                                                |
| 44      | PF.0       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | XT_OUT     | O    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal output pin.                         |
|         | BPWM1_CH3  | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                |
|         | TM3        | I/O  | MFP5 | Timer3 event counter input / toggle output                                                           |
| 45      | PF.1       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | XT_IN      | I    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal input pin.                          |
|         | BPWM1_CH2  | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                                                |
|         | TM1_EXT    | I    | MFP5 | Timer1 external counter input                                                                        |
| 46      | nRESET     | I    | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 47      | PF.2       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ICE_DAT    | I/O  | MFP1 | Serial wired debugger data pin                                                                       |
|         | I2C0_SDA   | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.                                                             |
|         | ADC_CH6    | A    | MFP3 | ADC channel 6 analog input.                                                                          |
|         | BPWM1_CH3  | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                |
| 48      | PF.3       | I/O  | MFP0 | General purpose digital I/O pin.                                                                     |
|         | ICE_CLK    | I    | MFP1 | Serial wired debugger clock pin                                                                      |

| Pin No. | Pin Name  | Type | MFP* | Description                           |
|---------|-----------|------|------|---------------------------------------|
|         | I2C0_SCL  | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.          |
|         | ADC_CH7   | A    | MFP3 | ADC channel 7 analog input.           |
|         | BPWM1_CH2 | I/O  | MFP4 | BPWM1 channel 2 output/capture input. |

Table 4.3-5 NUC125 USB Series LQFP48 Pin Description

### 4.3.6 NUC125 USB Series LQFP64 Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GPx\_MFPL and SYS\_GPx\_MFPH)

PA.10 MFP5 means SYS\_GPA\_MFPH[11:8]=0x5.

PC.0 MFP0 means SYS\_GPC\_MFPL[3:0]=0x0.

| Pin No. | Pin Name    | Type | MFP* | Description                               |
|---------|-------------|------|------|-------------------------------------------|
| 1       | PB.14       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | INT0        | I    | MFP1 | External interrupt0 input pin.            |
|         | UART0_nRTS  | O    | MFP2 | Request to Send output pin for UART0.     |
|         | ADC_CH9     | A    | MFP3 | ADC channel 9 analog input.               |
|         | BPWM1_CH0   | I/O  | MFP4 | BPWM1 channel 0 output/capture input.     |
|         | SPI0_SS     | I/O  | MFP7 | SPI0 slave select pin.                    |
| 2       | PB.13       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ADC_CH10    | A    | MFP3 | ADC channel 10 analog input.              |
|         | USC10_CTL1  | I/O  | MFP6 | USC10 CTL1 pin.                           |
| 3       | PB.12       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | CLKO        | O    | MFP2 | Clock Out                                 |
|         | ADC_CH11    | A    | MFP3 | ADC channel 11 analog input.              |
|         | USC10_CTL0  | I/O  | MFP6 | USC10 CTL0 pin.                           |
| 4       | PA.11       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | I2C1_SCL    | I/O  | MFP1 | I <sup>2</sup> C1 clock pin.              |
|         | BPWM0_CH5   | I/O  | MFP4 | BPWM0 channel 5 output/capture input.     |
|         | TM0         | I/O  | MFP5 | Timer0event counter input / toggle output |
|         | USC10_CLK   | I/O  | MFP6 | USC10 clock pin.                          |
|         | USC10_DAT0  | I/O  | MFP7 | USC10 DAT0 pin.                           |
| 5       | PA.10       | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | I2C1_SDA    | I/O  | MFP1 | I <sup>2</sup> C1 data input/output pin.  |
|         | BPWM0_CH4   | I/O  | MFP4 | BPWM0 channel 4 output/capture input.     |
|         | PWM0_BRAKE0 | I    | MFP5 | Brake input pin 0 of PWM0.                |
|         | USC10_DAT1  | I/O  | MFP6 | USC10 DAT1 pin.                           |
| 6       | PD.8        | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | USC10_DAT0  | I/O  | MFP6 | USC10 DAT0 pin.                           |
| 7       | PD.9        | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_BRAKE1 | I    | MFP5 | Brake input pin 1 of PWM0.                |
| 8       | PD.10       | I/O  | MFP0 | General purpose digital I/O pin.          |

| Pin No. | Pin Name        | Type | MFP* | Description                                                                      |
|---------|-----------------|------|------|----------------------------------------------------------------------------------|
|         | CLKO            | O    | MFP1 | Clock Out                                                                        |
|         | BPWM0_CH5       | I/O  | MFP4 | BPWM0 channel 5 output/capture input.                                            |
| 9       | PD.11           | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | INT1            | I    | MFP1 | External interrupt1 input pin.                                                   |
|         | BPWM0_CH4       | I/O  | MFP4 | BPWM0 channel 4 output/capture input.                                            |
| 10      | PB.4            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH3       | I/O  | MFP4 | BPWM0 channel 3 output/capture input.                                            |
|         | TM2_EXT         | I    | MFP5 | Timer2 external counter input                                                    |
|         | USC10_CTL0      | I/O  | MFP6 | USC10 CTL0 pin.                                                                  |
|         | USC10_DAT0      | I/O  | MFP7 | USC10 DAT0 pin.                                                                  |
| 11      | PB.5            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH2       | I/O  | MFP4 | BPWM0 channel 2 output/capture input.                                            |
|         | TM3             | I/O  | MFP5 | Timer3 event counter input / toggle output                                       |
|         | USC10_CLK       | I/O  | MFP6 | USC10 clock pin.                                                                 |
|         | USC10_DAT1      | I/O  | MFP7 | USC10 DAT1 pin.                                                                  |
| 12      | PB.6            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH1       | I/O  | MFP4 | BPWM0 channel 1 output/capture input.                                            |
|         | USC10_DAT0      | I/O  | MFP6 | USC10 DAT0 pin.                                                                  |
|         | USC10_CTL1      | I/O  | MFP7 | USC10 CTL1 pin.                                                                  |
| 13      | PB.7            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | BPWM0_CH0       | I/O  | MFP4 | BPWM0 channel 0 output/capture input.                                            |
|         | USC10_DAT1      | I/O  | MFP6 | USC10 DAT1 pin.                                                                  |
|         | USC10_CTL0      | I/O  | MFP7 | USC10 CTL0 pin.                                                                  |
| 14      | LDO_CAP         | A    | MFP0 | LDO output pin.                                                                  |
| 15      | V <sub>DD</sub> | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function. |
| 16      | V <sub>SS</sub> | A    | MFP0 | Ground pin for digital circuit.                                                  |
| 17      | USB_VBUS        | A    | MFP0 | Power supply from USB host or HUB.                                               |
| 18      | USB_VDD33_CAP   | A    | MFP0 | Internal power regulator output 3.3V decoupling pin.                             |
| 19      | USB_D-          | I    | MFP0 | USB differential signal D-.                                                      |
| 20      | USB_D+          | I    | MFP0 | USB differential signal D+.                                                      |
| 21      | PB.0            | I/O  | MFP0 | General purpose digital I/O pin.                                                 |
|         | UART0_RXD       | I    | MFP1 | Data receiver input pin for UART0.                                               |
|         | PWM1_CH0        | I/O  | MFP4 | PWM1 channel0 output/capture input.                                              |

| Pin No. | Pin Name     | Type | MFP* | Description                              |
|---------|--------------|------|------|------------------------------------------|
| 22      | PB.1         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_TXD    | O    | MFP1 | Data transmitter output pin for UART0.   |
|         | PWM1_CH1     | I/O  | MFP4 | PWM1 channel1 output/capture input.      |
| 23      | PB.2         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_nRTS   | O    | MFP1 | Request to Send output pin for UART0.    |
|         | TM2_EXT      | I    | MFP2 | Timer2 external counter input            |
|         | PWM1_CH2     | I/O  | MFP4 | PWM1 channel2 output/capture input.      |
| 24      | PB.3         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_nCTS   | I    | MFP1 | Clear to Send input pin for UART0.       |
|         | TM3_EXT      | I    | MFP2 | Timer3 external counter input            |
|         | PWM1_CH3     | I/O  | MFP4 | PWM1 channel3 output/capture input.      |
| 25      | PC.5         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_TXD    | O    | MFP2 | Data transmitter output pin for UART0.   |
|         | PWM1_CH5     | I/O  | MFP4 | PWM1 channel5 output/capture input.      |
|         | USC10_DAT0   | I/O  | MFP7 | USC10 DAT0 pin.                          |
| 26      | PC.4         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | UART0_RXD    | I    | MFP2 | Data receiver input pin for UART0.       |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.            |
|         | PWM1_CH4     | I/O  | MFP4 | PWM1 channel4 output/capture input.      |
|         | USC10_DAT1   | I/O  | MFP7 | USC10 DAT1 pin.                          |
| 27      | PC.3         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | SPI0_MOSI    | I/O  | MFP1 | SPI0 MOSI (Master Out, Slave In) pin.    |
|         | I2C1_SDA     | I/O  | MFP3 | I <sup>2</sup> C1 data input/output pin. |
|         | PWM1_CH3     | I/O  | MFP4 | PWM1 channel3 output/capture input.      |
|         | UART0_nRTS   | O    | MFP6 | Request to Send output pin for UART0.    |
|         | USC10_DAT0   | I/O  | MFP7 | USC10 DAT0 pin.                          |
| 28      | PC.2         | I/O  | MFP0 | General purpose digital I/O pin.         |
|         | SPI0_MISO    | I/O  | MFP1 | SPI0 MISO (Master In, Slave Out) pin.    |
|         | I2C1_SCL     | I/O  | MFP3 | I <sup>2</sup> C1 clock pin.             |
|         | PWM1_CH2     | I/O  | MFP4 | PWM1 channel2 output/capture input.      |
|         | UART0_nCTS   | I    | MFP6 | Clear to Send input pin for UART0.       |
|         | USC10_DAT1   | I/O  | MFP7 | USC10 DAT1 pin.                          |
| 29      | PC.1         | I/O  | MFP0 | General purpose digital I/O pin.         |

| Pin No. | Pin Name     | Type | MFP* | Description                                |
|---------|--------------|------|------|--------------------------------------------|
|         | SPI0_CLK     | I/O  | MFP1 | SPI0 serial clock pin.                     |
|         | PWM1_CH1     | I/O  | MFP4 | PWM1 channel1 output/capture input.        |
|         | UART0_TXD    | O    | MFP6 | Data transmitter output pin for UART0.     |
|         | USC10_CTL0   | I/O  | MFP7 | USC10 CTL0 pin                             |
| 30      | PC.0         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_SS      | I/O  | MFP1 | SPI0 slave select pin.                     |
|         | PWM1_CH0     | I/O  | MFP4 | PWM1 channel0 output/capture input.        |
|         | TM2          | I/O  | MFP5 | Timer2 event counter input / toggle output |
|         | UART0_RXD    | I    | MFP6 | Data receiver input pin for UART0.         |
|         | USC10_CLK    | I/O  | MFP7 | USC10 clock pin.                           |
| 31      | PB.10        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM2          | I/O  | MFP1 | Timer2 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH5     | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
| 32      | PB.9         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | TM1          | I/O  | MFP1 | Timer1 event counter input / toggle output |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | PWM0_CH4     | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
| 33      | PE.2         | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | INT1         | I    | MFP1 | External interrupt1 input pin.             |
|         | TM0_EXT      | I    | MFP5 | Timer0 external counter input              |
|         | I2C0_SCL     | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |
|         | USC10_CTL1   | I/O  | MFP7 | USC10 CTL1 pin.                            |
| 34      | PC.13        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3     | I/O  | MFP2 | PWM0 channel3 output/capture input.        |
|         | CLKO         | O    | MFP3 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |
|         | I2C0_SDA     | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
| 35      | PC.12        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH2     | I/O  | MFP2 | PWM0 channel2 output/capture input.        |
|         | SPI0_I2SMCLK | O    | MFP3 | I2S0 master clock output pin.              |
|         | CLKO         | O    | MFP4 | Clock Out                                  |
|         | INT0         | I    | MFP5 | External interrupt0 input pin.             |

| Pin No. | Pin Name    | Type | MFP* | Description                                |
|---------|-------------|------|------|--------------------------------------------|
|         | I2C0_SCL    | I/O  | MFP6 | I <sup>2</sup> C0 clock pin.               |
|         | USC10_CTL1  | I/O  | MFP7 | USC10 CTL1 pin.                            |
| 36      | PC.11       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MOSI   | I/O  | MFP3 | SPI0 MOSI (Master Out, Slave In) pin.      |
|         | PWM0_CH1    | I/O  | MFP4 | PWM0 channel1 output/capture input.        |
|         | TM1         | I/O  | MFP5 | Timer1 event counter input / toggle output |
|         | I2C0_SDA    | I/O  | MFP6 | I <sup>2</sup> C0 data input/output pin.   |
|         | USC10_DAT0  | I/O  | MFP7 | USC10 DAT0 pin.                            |
| 37      | PC.10       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_MISO   | I/O  | MFP3 | SPI0 MISO (Master In, Slave Out) pin.      |
|         | PWM0_CH0    | I/O  | MFP4 | PWM0 channel0 output/capture input.        |
|         | USC10_DAT1  | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 38      | PE.1        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC       | I    | MFP2 | ADC external trigger input.                |
|         | CLKO        | O    | MFP3 | Clock Out                                  |
|         | TM3         | I/O  | MFP5 | Timer3 event counter input / toggle output |
|         | USC10_DAT1  | I/O  | MFP7 | USC10 DAT1 pin.                            |
| 39      | PC.9        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | SPI0_CLK    | I/O  | MFP3 | SPI0 serial clock pin.                     |
|         | PWM0_CH5    | I/O  | MFP4 | PWM0 channel5 output/capture input.        |
|         | PWM0_BRAKE1 | I    | MFP5 | Brake input pin 1 of PWM0.                 |
|         | USC10_CLK   | I/O  | MFP7 | USC10 clock pin                            |
| 40      | PC.8        | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | STADC       | I    | MFP2 | ADC external trigger input.                |
|         | SPI0_SS     | I/O  | MFP3 | SPI0 slave select pin.                     |
|         | PWM0_CH4    | I/O  | MFP4 | PWM0 channel4 output/capture input.        |
|         | PWM1_BRAKE0 | I    | MFP5 | Brake input pin 0 of PWM1.                 |
|         | USC10_CTL0  | I/O  | MFP7 | USC10 CTL0 pin                             |
| 41      | PA.15       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | PWM0_CH3    | I/O  | MFP1 | PWM0 channel3 output/capture input.        |
|         | SPI_I2SMCLK | O    | MFP2 | I2S0 master clock output pin.              |
|         | CLKO        | O    | MFP3 | Clock Out                                  |
|         | PWM1_BRAKE1 | I    | MFP4 | Brake input pin 1 of PWM1.                 |

| Pin No. | Pin Name         | Type | MFP* | Description                               |
|---------|------------------|------|------|-------------------------------------------|
|         | UART0_nRTS       | O    | MFP5 | Request to Send output pin for UART0.     |
| 42      | PE.0             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | INT0             | I    | MFP1 | External interrupt0 input pin.            |
|         | CLKO             | O    | MFP3 | Clock Out                                 |
|         | PWM0_CH3         | I/O  | MFP4 | PWM0 channel3 output/capture input.       |
|         | TM1_EXT          | I    | MFP5 | Timer1 external counter input             |
|         | USCI0_DAT0       | I/O  | MFP7 | USCI0 DAT0 pin.                           |
| 43      | PA.14            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH2         | I/O  | MFP1 | PWM0 channel2 output/capture input.       |
|         | UART0_nCTS       | I    | MFP3 | Clear to Send input pin for UART0.        |
|         | PWM0_BRAKE0      | I    | MFP4 | Brake input pin 0 of PWM0.                |
| 44      | PA.13            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH1         | I/O  | MFP1 | PWM0 channel1 output/capture input.       |
|         | I2C1_SDA         | I/O  | MFP2 | I <sup>2</sup> C1 data input/output pin.  |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.    |
| 45      | PA.12            | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | PWM0_CH0         | I/O  | MFP1 | PWM0 channel0 output/capture input.       |
|         | I2C1_SCL         | I/O  | MFP2 | I <sup>2</sup> C1 clock pin.              |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.        |
| 46      | PF.4             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ICE_DAT          | I/O  | MFP1 | Serial wired debugger data pin            |
|         | I2C0_SDA         | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.  |
|         | UART0_TXD        | O    | MFP3 | Data transmitter output pin for UART0.    |
|         | PWM0_CH3         | I/O  | MFP4 | PWM0 channel3 output/capture input.       |
| 47      | PF.5             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ICE_CLK          | I    | MFP1 | Serial wired debugger clock pin           |
|         | I2C0_SCL         | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.              |
|         | UART0_RXD        | I    | MFP3 | Data receiver input pin for UART0.        |
| 48      | AV <sub>DD</sub> | A    | MFP0 | Power supply for internal analog circuit. |
| 49      | PD.0             | I/O  | MFP0 | General purpose digital I/O pin.          |
|         | ADC_CH0          | A    | MFP3 | ADC channel 0 analog input.               |
|         | UART0_nRTS       | O    | MFP5 | Request to Send output pin for UART0.     |
|         | USCI0_CTL0       | I/O  | MFP6 | USCI0 CTL0 pin.                           |

| Pin No. | Pin Name   | Type | MFP* | Description                                |
|---------|------------|------|------|--------------------------------------------|
|         | SPI0_SS    | I/O  | MFP7 | SPI0 slave select pin.                     |
| 50      | PD.1       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH1    | A    | MFP3 | ADC channel 1 analog input.                |
|         | TM0_EXT    | I    | MFP4 | Timer0 external counter input              |
|         | UART0_RXD  | I    | MFP5 | Data receiver input pin for UART0.         |
|         | USC10_CLK  | I/O  | MFP6 | USC10 clock pin.                           |
|         | SPI0_CLK   | I/O  | MFP7 | SPI0 serial clock pin.                     |
| 51      | PD.2       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH2    | A    | MFP3 | ADC channel 2 analog input.                |
|         | TM3        | I/O  | MFP4 | Timer3 event counter input / toggle output |
|         | UART0_TXD  | O    | MFP5 | Data transmitter output pin for UART0.     |
|         | USC10_DAT1 | I/O  | MFP6 | USC10 DAT1 pin.                            |
|         | SPI0_MISO  | I/O  | MFP7 | SPI0 MISO (Master In, Slave Out) pin.      |
| 52      | PD.3       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH3    | A    | MFP3 | ADC channel 3 analog input.                |
|         | TM1_EXT    | I    | MFP4 | Timer1 external counter input              |
|         | UART0_nCTS | I    | MFP5 | Clear to Send input pin for UART0.         |
|         | USC10_DAT0 | I/O  | MFP6 | USC10 DAT0 pin.                            |
|         | SPI0_MOSI  | I/O  | MFP7 | SPI0 MOSI (Master Out, Slave In) pin.      |
| 53      | PD.4       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH4    | A    | MFP2 | ADC channel 4 analog input.                |
|         | BPWM1_CH5  | I/O  | MFP4 | BPWM1 channel 5 output/capture input.      |
|         | UART0_nRTS | O    | MFP5 | Request to Send output pin for UART0.      |
|         | USC10_CTL0 | I/O  | MFP6 | USC10 CTL0 pin.                            |
|         | SPI0_SS    | I/O  | MFP7 | SPI0 slave select pin.                     |
| 54      | PD.5       | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | ADC_CH5    | A    | MFP2 | ADC channel 5 analog input.                |
|         | BPWM1_CH4  | I/O  | MFP4 | BPWM1 channel 4 output/capture input.      |
| 55      | PB.15      | I/O  | MFP0 | General purpose digital I/O pin.           |
|         | INT1       | I    | MFP1 | External interrupt1 input pin.             |
|         | TM0_EXT    | I    | MFP2 | Timer0 external counter input              |
|         | BPWM1_CH5  | I/O  | MFP4 | BPWM1 channel 5 output/capture input.      |
| 56      | PF.0       | I/O  | MFP0 | General purpose digital I/O pin.           |

| Pin No. | Pin Name          | Type | MFP* | Description                                                                                              |
|---------|-------------------|------|------|----------------------------------------------------------------------------------------------------------|
|         | XT_OUT            | O    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal output pin.                             |
|         | BPWM1_CH3         | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                    |
|         | TM3               | I/O  | MFP5 | Timer3 event counter input / toggle output                                                               |
| 57      | PF.1              | I/O  | MFP0 | General purpose digital I/O pin.                                                                         |
|         | XT_IN             | I    | MFP1 | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal input pin.                              |
|         | BPWM1_CH2         | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                                                    |
|         | TM1_EXT           | I    | MFP5 | Timer1 external counter input                                                                            |
| 58      | nRESET            | I    | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.     |
| 59      | V <sub>SS</sub>   | A    | MFP0 | Ground pin for digital circuit.                                                                          |
| 60      | V <sub>DD</sub>   | A    | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital function.                         |
| 61      | PF.2              | I/O  | MFP0 | General purpose digital I/O pin.                                                                         |
|         | ICE_DAT           | I/O  | MFP1 | Serial wired debugger data pin                                                                           |
|         | I2C0_SDA          | I/O  | MFP2 | I <sup>2</sup> C0 data input/output pin.                                                                 |
|         | ADC_CH6           | A    | MFP3 | ADC channel 6 analog input.                                                                              |
|         | BPWM1_CH3         | I/O  | MFP4 | BPWM1 channel 3 output/capture input.                                                                    |
| 62      | PF.3              | I/O  | MFP0 | General purpose digital I/O pin.                                                                         |
|         | ICE_CLK           | I    | MFP1 | Serial wired debugger clock pin                                                                          |
|         | I2C0_SCL          | I/O  | MFP2 | I <sup>2</sup> C0 clock pin.                                                                             |
|         | ADC_CH7           | A    | MFP3 | ADC channel 7 analog input.                                                                              |
|         | BPWM1_CH2         | I/O  | MFP4 | BPWM1 channel 2 output/capture input.                                                                    |
| 63      | V <sub>SS</sub>   | A    | MFP0 | Ground pin for digital circuit.                                                                          |
| 64      | V <sub>DDIO</sub> | A    | MFP0 | Power supply for PB.14, PB.13, PB.12, PA.11, PA.10, PD.8, PD.9, PD.10, PD.11, PB.4, PB.5, PB.6 and PB.7. |

Table 4.3-6 NUC125 USB Series LQFP64 Pin Description

### 4.3.7 GPIO Multi-function Pin Summary

MFP\* = Multi-function pin. (Refer to section SYS\_GP<sub>x</sub>\_MFPL and SYS\_GP<sub>x</sub>\_MFP<sub>H</sub>)

PA.10 MFP5 means SYS\_GPA\_MFPH[11:8]=0x5.

PC.0 MFP0 means SYS\_GPC\_MFPL[3:0]=0x0.

| Group | Pin Name  | GPIO  | MFP* | Type | Description                 |
|-------|-----------|-------|------|------|-----------------------------|
| ADC0  | ADC0_CH0  | PD.0  | MFP3 | A    | ADC0 analog input.          |
|       | ADC0_CH1  | PD.1  | MFP3 | A    | ADC1 analog input.          |
|       | ADC0_CH2  | PD.2  | MFP3 | A    | ADC2 analog input.          |
|       | ADC0_CH3  | PD.3  | MFP3 | A    | ADC3 analog input.          |
|       | ADC0_CH4  | PD.4  | MFP2 | A    | ADC4 analog input.          |
|       | ADC0_CH5  | PD.5  | MFP2 | A    | ADC5 analog input.          |
|       | ADC0_CH6  | PF.2  | MFP3 | A    | ADC6 analog input.          |
|       | ADC0_CH7  | PF.3  | MFP3 | A    | ADC7 analog input.          |
|       | ADC0_CH8  | PB.8  | MFP3 | A    | ADC8 analog input.          |
|       | ADC0_CH9  | PB.14 | MFP3 | A    | ADC9 analog input.          |
|       | ADC0_CH10 | PB.13 | MFP3 | A    | ADC10 analog input.         |
|       | ADC0_CH11 | PB.12 | MFP3 | A    | ADC11 analog input.         |
|       | STADC     | PC.8  | MFP2 | I    | ADC external trigger input. |
|       | STADC     | PE.1  | MFP2 | I    | ADC external trigger input  |
| BPWM0 | BPWM0_CH0 | PB.7  | MFP4 | I/O  | BPWM0 output/capture input. |
|       | BPWM0_CH1 | PB.6  | MFP4 | I/O  | BPWM0 output/capture input. |
|       | BPWM0_CH2 | PB.5  | MFP4 | I/O  | BPWM0 output/capture input. |
|       | BPWM0_CH3 | PB.4  | MFP4 | I/O  | BPWM0 output/capture input. |
|       | BPWM0_CH4 | PA.10 | MFP4 | I/O  | BPWM0 output/capture input. |
|       | BPWM0_CH4 | PD.11 | MFP4 | I/O  | BPWM0 output/capture input. |
|       | BPWM0_CH5 | PA.11 | MFP4 | I/O  | BPWM0 output/capture input. |
|       | BPWM0_CH5 | PD.10 | MFP4 | I/O  | BPWM0 output/capture input. |
| BPWM1 | BPWM1_CH0 | PB.14 | MFP4 | I/O  | BPWM1 output/capture input. |
|       | BPWM1_CH1 | PB.8  | MFP4 | I/O  | BPWM1 output/capture input. |
|       | BPWM1_CH2 | PF.1  | MFP4 | I/O  | BPWM1 output/capture input. |
|       | BPWM1_CH2 | PF.3  | MFP4 | I/O  | BPWM1 output/capture input. |
|       | BPWM1_CH3 | PF.0  | MFP4 | I/O  | BPWM1 output/capture input. |
|       | BPWM1_CH3 | PF.2  | MFP4 | I/O  | BPWM1 output/capture input. |
|       | BPWM1_CH4 | PD.5  | MFP4 | I/O  | BPWM1 output/capture input. |

| Group | Pin Name    | GPIO  | MFP* | Type | Description                      |
|-------|-------------|-------|------|------|----------------------------------|
|       | BPWM1_CH5   | PB.15 | MFP4 | I/O  | BPWM1 output/capture input.      |
|       | BPWM1_CH5   | PD.4  | MFP4 | I/O  | BPWM1 output/capture input.      |
| CLKO  | CLKO        | PA.15 | MFP3 | O    | Clock Out.                       |
|       | CLKO        | PB.12 | MFP2 | O    | Clock Out.                       |
|       | CLKO        | PC.12 | MFP4 | O    | Clock Out.                       |
|       | CLKO        | PC.13 | MFP3 | O    | Clock Out.                       |
|       | CLKO        | PD.10 | MFP1 | O    | Clock Out.                       |
|       | CLKO        | PE.0  | MFP3 | O    | Clock Out.                       |
|       | CLKO        | PE.1  | MFP3 | O    | Clock Out.                       |
| I2C0  | I2C0_SCL    | PC.12 | MFP6 | I/O  | I2C0 clock pin.                  |
|       | I2C0_SCL    | PE.2  | MFP6 | I/O  | I2C0 clock pin.                  |
|       | I2C0_SCL    | PF.3  | MFP2 | I/O  | I2C0 clock pin.                  |
|       | I2C0_SCL    | PF.5  | MFP2 | I/O  | I2C0 clock pin.                  |
|       | I2C0_SDA    | PC.11 | MFP6 | I/O  | I2C0 data input/output pin.      |
|       | I2C0_SDA    | PC.13 | MFP6 | I/O  | I2C0 data input/output pin.      |
|       | I2C0_SDA    | PF.2  | MFP2 | I/O  | I2C0 data input/output pin.      |
|       | I2C0_SDA    | PF.4  | MFP2 | I/O  | I2C0 data input/output pin.      |
| I2C1  | I2C1_SCL    | PA.11 | MFP1 | I/O  | I2C1 clock pin.                  |
|       | I2C1_SCL    | PA.12 | MFP2 | I/O  | I2C1 clock pin.                  |
|       | I2C1_SCL    | PC.2  | MFP3 | I/O  | I2C1 clock pin.                  |
|       | I2C1_SDA    | PA.10 | MFP1 | I/O  | I2C1 data input/output pin.      |
|       | I2C1_SDA    | PA.13 | MFP2 | I/O  | I2C1 data input/output pin.      |
|       | I2C1_SDA    | PC.3  | MFP3 | I/O  | I2C1 data input/output pin.      |
| ICE   | ICE_CLK     | PF.5  | MFP1 | I    | Serial wired debugger clock pin. |
|       | ICE_DAT     | PF.4  | MFP1 | I/O  | Serial wired debugger data pin.  |
| INT0  | INT0        | PB.14 | MFP1 | I    | External interrupt0 input pin.   |
|       | INT0        | PC.12 | MFP5 | I    | External interrupt0 input pin.   |
|       | INT0        | PC.13 | MFP5 | I    | External interrupt0 input pin.   |
|       | INT0        | PE.0  | MFP1 | I    | External interrupt0 input pin.   |
| INT1  | INT1        | PB.15 | MFP1 | I    | External interrupt1 input pin.   |
|       | INT1        | PD.11 | MFP1 | I    | External interrupt1 input pin.   |
|       | INT1        | PE.2  | MFP1 | I    | External interrupt1 input pin.   |
| PWM0  | PWM0_BRAKE0 | PA.10 | MFP5 | I    | PWM0 brake input 0.              |

| Group | Pin Name    | GPIO  | MFP* | Type | Description                               |
|-------|-------------|-------|------|------|-------------------------------------------|
|       | PWM0_BRAKE0 | PA.14 | MFP4 | I    | PWM0 brake input 0.                       |
|       | PWM0_BRAKE1 | PC.9  | MFP5 | I    | PWM0 brake input 1.                       |
|       | PWM0_BRAKE1 | PD.9  | MFP5 | I    | PWM0 brake input 1.                       |
|       | PWM0_CH0    | PA.12 | MFP1 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH0    | PC.10 | MFP4 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH1    | PA.13 | MFP1 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH1    | PC.11 | MFP4 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH2    | PA.14 | MFP1 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH2    | PC.12 | MFP2 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH3    | PA.15 | MFP1 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH3    | PC.13 | MFP2 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH3    | PE.0  | MFP4 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH3    | PF.4  | MFP4 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH4    | PB.9  | MFP4 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH4    | PC.8  | MFP4 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH5    | PB.10 | MFP4 | I/O  | PWM0 output/capture input.                |
|       | PWM0_CH5    | PC.9  | MFP4 | I/O  | PWM0 output/capture input.                |
| PWM1  | PWM1_BRAKE0 | PC.8  | MFP4 | I    | PWM1 brake input 0.                       |
|       | PWM1_BRAKE1 | PA.15 | MFP4 | I    | PWM1 brake input 1.                       |
|       | PWM1_CH0    | PB.0  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH0    | PC.0  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH1    | PB.1  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH1    | PC.1  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH2    | PB.2  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH2    | PC.2  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH3    | PB.3  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH3    | PC.3  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH4    | PC.4  | MFP4 | I/O  | PWM1 output/capture input.                |
|       | PWM1_CH5    | PC.5  | MFP4 | I/O  | PWM1 output/capture input.                |
| SPI0  | SPI0_CLK    | PC.1  | MFP1 | I/O  | SPI0 serial clock pin.                    |
|       | SPI0_CLK    | PC.9  | MFP3 | I/O  | SPI0 serial clock pin.                    |
|       | SPI0_CLK    | PD.1  | MFP7 | I/O  | SPI0 serial clock pin.                    |
|       | SPI0_MISO0  | PC.2  | MFP1 | I/O  | SPI0 1st MISO (Master In, Slave Out) pin. |

| Group | Pin Name     | GPIO  | MFP* | Type | Description                                 |
|-------|--------------|-------|------|------|---------------------------------------------|
|       | SPI0_MISO0   | PC.10 | MFP3 | I/O  | SPI0 1st MISO (Master In, Slave Out) pin.   |
|       | SPI0_MISO0   | PD.2  | MFP7 | I/O  | SPI0 1st MISO (Master In, Slave Out) pin.   |
|       | SPI0_MOSI0   | PC.3  | MFP1 | I/O  | SPI0 1st MOSI (Master Out, Slave In) pin.   |
|       | SPI0_MOSI0   | PC.11 | MFP3 | I/O  | SPI0 1st MOSI (Master Out, Slave In) pin.   |
|       | SPI0_MOSI0   | PD.3  | MFP7 | I/O  | SPI0 1st MOSI (Master Out, Slave In) pin.   |
|       | SPI0_SS      | PB.14 | MFP7 | I/O  | SPI0 slave select pin.                      |
|       | SPI0_SS      | PC.0  | MFP1 | I/O  | SPI0 slave select pin.                      |
|       | SPI0_SS      | PC.8  | MFP3 | I/O  | SPI0 slave select pin.                      |
|       | SPI0_SS      | PD.0  | MFP7 | I/O  | SPI0 slave select pin.                      |
|       | SPI0_SS      | PD.4  | MFP7 | I/O  | SPI0 slave select pin.                      |
|       | SPI0_I2SMCLK | PA.15 | MFP2 | O    | I2S0 master clock output pin.               |
|       | SPI0_I2SMCLK | PB.9  | MFP3 | O    | I2S0 master clock output pin.               |
|       | SPI0_I2SMCLK | PB.10 | MFP3 | O    | I2S0 master clock output pin.               |
|       | SPI0_I2SMCLK | PC.4  | MFP3 | O    | I2S0 master clock output pin.               |
|       | SPI0_I2SMCLK | PC.12 | MFP3 | O    | I2S0 master clock output pin.               |
| TM0   | TM0          | PA.11 | MFP5 | I/O  | Timer0 event counter input / toggle output. |
|       | TM0          | PB.8  | MFP1 | I/O  | Timer0 event counter input / toggle output. |
|       | TM0_EXT      | PB.15 | MFP2 | I    | Timer0 external counter input.              |
|       | TM0_EXT      | PD.1  | MFP4 | I    | Timer0 external counter input.              |
|       | TM0_EXT      | PE.2  | MFP5 | I    | Timer0 external counter input.              |
| TM1   | TM1          | PB.9  | MFP5 | I/O  | Timer1 event counter input / toggle output. |
|       | TM1          | PC.11 | MFP1 | I/O  | Timer1 event counter input / toggle output. |
|       | TM1_EXT      | PD.3  | MFP4 | I    | Timer1 external counter input.              |
|       | TM1_EXT      | PF.1  | MFP5 | I    | Timer1 external counter input.              |
|       | TM1_EXT      | PE.3  | MFP5 | I    | Timer1 external counter input.              |
| TM2   | TM2          | PB.10 | MFP1 | I/O  | Timer2 event counter input / toggle output. |
|       | TM2          | PC.0  | MFP5 | I/O  | Timer2 event counter input / toggle output. |
|       | TM2_EXT      | PB.2  | MFP2 | I    | Timer2 external counter input.              |
|       | TM2_EXT      | PB.4  | MFP5 | I    | Timer2 external counter input.              |
| TM3   | TM3          | PB.5  | MFP5 | I/O  | Timer3 event counter input / toggle output. |
|       | TM3          | PD.2  | MFP4 | I/O  | Timer3 event counter input / toggle output. |
|       | TM3          | PE.1  | MFP5 | I/O  | Timer3 event counter input / toggle output. |
|       | TM3          | PF.0  | MFP5 | I/O  | Timer3 event counter input / toggle output. |

| Group | Pin Name   | GPIO  | MFP* | Type | Description                            |
|-------|------------|-------|------|------|----------------------------------------|
|       | TM3_EXT    | PB.3  | MFP2 | I    | Timer3 external counter input.         |
| UART0 | UART0_RXD  | PA12  | MFP3 | I    | Data receiver input pin for UART0.     |
|       | UART0_RXD  | PB.0  | MFP1 | I    | Data receiver input pin for UART0.     |
|       | UART0_RXD  | PC.0  | MFP6 | I    | Data receiver input pin for UART0.     |
|       | UART0_RXD  | PC.4  | MFP2 | I    | Data receiver input pin for UART0.     |
|       | UART0_RXD  | PD.1  | MFP5 | I    | Data receiver input pin for UART0.     |
|       | UART0_RXD  | PF.5  | MFP3 | I    | Data receiver input pin for UART0.     |
|       | UART0_TXD  | PA.13 | MFP3 | O    | Data transmitter output pin for UART0. |
|       | UART0_TXD  | PB.1  | MFP1 | O    | Data transmitter output pin for UART0. |
|       | UART0_TXD  | PC.1  | MFP6 | O    | Data transmitter output pin for UART0. |
|       | UART0_TXD  | PC.5  | MFP2 | O    | Data transmitter output pin for UART0. |
|       | UART0_TXD  | PD.2  | MFP5 | O    | Data transmitter output pin for UART0. |
|       | UART0_TXD  | PF.4  | MFP3 | O    | Data transmitter output pin for UART0. |
|       | UART0_nCTS | PA.14 | MFP3 | I    | Clear to Send input pin for UART0.     |
|       | UART0_nCTS | PB.3  | MFP1 | I    | Clear to Send input pin for UART0.     |
|       | UART0_nCTS | PC.2  | MFP6 | I    | Clear to Send input pin for UART0.     |
|       | UART0_nCTS | PD.3  | MFP5 | I    | Clear to Send input pin for UART0.     |
|       | UART0_nRTS | PA.15 | MFP5 | O    | Request to Send output pin for UART0.  |
|       | UART0_nRTS | PB.2  | MFP1 | O    | Request to Send output pin for UART0.  |
|       | UART0_nRTS | PB.14 | MFP2 | O    | Request to Send output pin for UART0.  |
|       | UART0_nRTS | PC.3  | MFP6 | O    | Request to Send output pin for UART0.  |
|       | UART0_nRTS | PD.0  | MFP5 | O    | Request to Send output pin for UART0.  |
|       | UART0_nRTS | PD.4  | MFP5 | O    | Request to Send output pin for UART0.  |
| USC10 | USC10_CLK  | PC.0  | MFP7 | I/O  | USC10 clock pin.                       |
|       | USC10_CLK  | PC.9  | MFP7 | I/O  | USC10 clock pin.                       |
|       | USC10_CLK  | PD.1  | MFP6 | I/O  | USC10 clock pin.                       |
|       | USC10_CTL0 | PB.4  | MFP6 | I/O  | USC10 CTL0 pin.                        |
|       | USC10_CTL0 | PB.7  | MFP7 | I/O  | USC10 CTL0 pin.                        |
|       | USC10_CTL0 | PB.12 | MFP6 | I/O  | USC10 CTL0 pin.                        |
|       | USC10_CTL0 | PC.1  | MFP7 | I/O  | USC10 CTL0 pin.                        |
|       | USC10_CTL0 | PC.8  | MFP7 | I/O  | USC10 CTL0 pin.                        |
|       | USC10_CTL0 | PD.0  | MFP6 | I/O  | USC10 CTL0 pin.                        |
|       | USC10_CTL0 | PD.4  | MFP6 | I/O  | USC10 CTL0 pin.                        |

| Group | Pin Name   | GPIO  | MFP* | Type | Description                                                                  |
|-------|------------|-------|------|------|------------------------------------------------------------------------------|
|       | USCI0_CTL1 | PB6   | MFP7 | I/O  | USCI0 CTL1 pin.                                                              |
|       | USCI0_CTL1 | PB.13 | MFP6 | I/O  | USCI0 CTL1 pin.                                                              |
|       | USCI0_CTL1 | PC.12 | MFP7 | I/O  | USCI0 CTL1 pin.                                                              |
|       | USCI0_CTL1 | PE.2  | MFP7 | I/O  | USCI0 CTL1 pin.                                                              |
|       | USCI0_DAT0 | PA.11 | MFP7 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PB4   | MFP7 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PB.6  | MFP6 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PC.3  | MFP7 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PC.5  | MFP7 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PC.11 | MFP7 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PD.3  | MFP6 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PD.8  | MFP6 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT0 | PE.0  | MFP7 | I/O  | USCI0 DAT0 pin.                                                              |
|       | USCI0_DAT1 | PA.10 | MFP6 | I/O  | USCI0 DAT1 pin.                                                              |
|       | USCI0_DAT1 | PB.5  | MFP7 | I/O  | USCI0 DAT1 pin.                                                              |
|       | USCI0_DAT1 | PB.7  | MFP6 | I/O  | USCI0 DAT1 pin.                                                              |
|       | USCI0_DAT1 | PC.2  | MFP7 | I/O  | USCI0 DAT1 pin.                                                              |
|       | USCI0_DAT1 | PC.4  | MFP7 | I/O  | USCI0 DAT1 pin.                                                              |
|       | USCI0_DAT1 | PC.10 | MFP7 | I/O  | USCI0 DAT1 pin.                                                              |
|       | USCI0_DAT1 | PD.2  | MFP6 | I/O  | USCI0 DAT1 pin.                                                              |
|       | USCI0_DAT1 | PE.1  | MFP7 | I/O  | USCI0 DAT1 pin.                                                              |
| XT    | XT_IN      | PF.1  | MFP1 | I    | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal input pin.  |
|       | XT_OUT     | PF.0  | MFP1 | O    | External 4~24 MHz (high speed) or 32.768 kHz (low speed) crystal output pin. |

Table 4.3-7 NUC121/125 GPIO Multi-function Table

## 5 BLOCK DIAGRAM

### 5.1 NuMicro® NUC121/125 Block Diagram

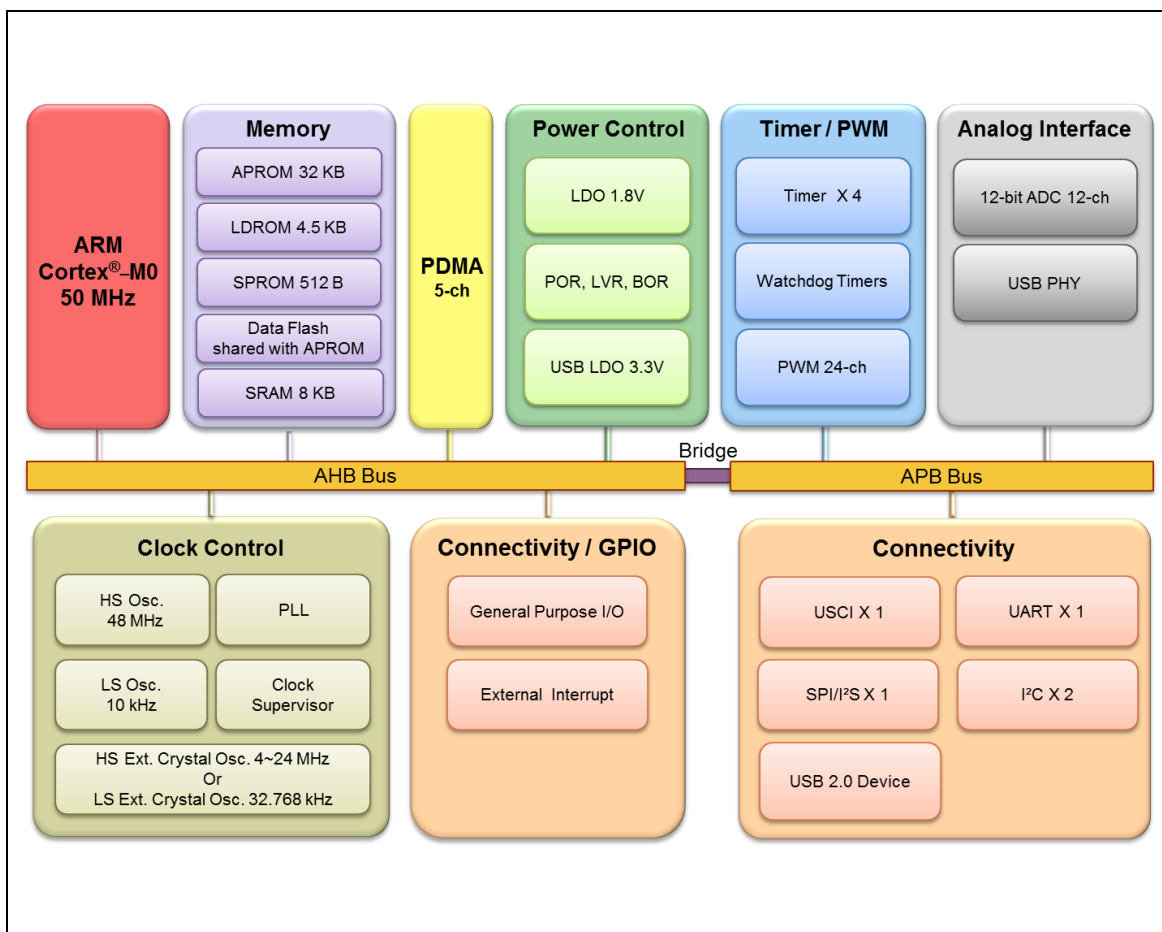


Figure 5.1-1 NuMicro® NUC121/125 Block Diagram

## 6 FUNCTIONAL DESCRIPTION

### 6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M0 is a processor with the same capability as the Cortex®-M0 processor and includes floating point arithmetic functionality. The NuMicro® NUC121/125 series is embedded with Cortex®-M0 processor. Throughout this document, the name Cortex®-M0 refers to both Cortex®-M0 and Cortex®-M0 processors. Figure 6.1-1 shows the functional controller of the processor.

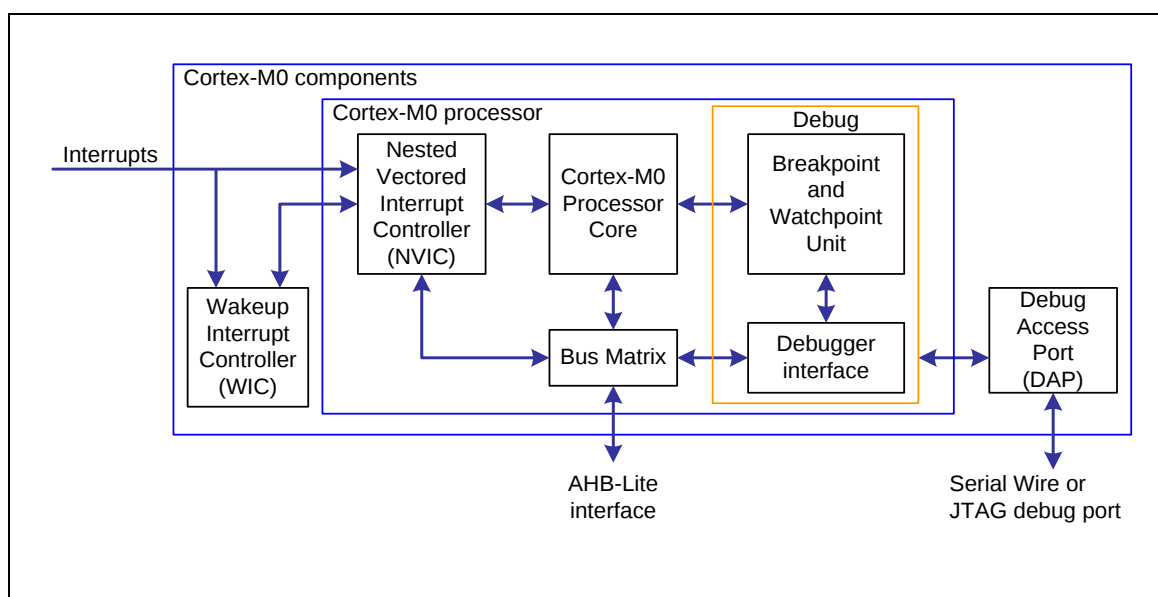


Figure 6.1-1 Cortex®-M0 Block Diagram

The implemented device provides:

- ◆ A low gate count processor:
- ◆ ARMv6-M Thumb® instruction set
- ◆ Thumb-2 technology
- ◆ ARMv6-M compliant 24-bit SysTick timer
- ◆ A 32-bit hardware multiplier
- ◆ System interface supported with little-endian data accesses
- ◆ Ability to have deterministic, fixed-latency, interrupt handling
- ◆ Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling

- ◆ C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
- ◆ Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC:
  - ◆ 32 external interrupt inputs, each with four levels of priority
  - ◆ Dedicated Non-maskable Interrupt (NMI) input
  - ◆ Supports for both level-sensitive and pulse-sensitive interrupt lines
  - ◆ Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug Support:
  - ◆ Four hardware breakpoints
  - ◆ Two watchpoints
  - ◆ Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - ◆ Single step and vector catch capabilities
- Bus interfaces:
  - ◆ Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - ◆ Single 32-bit slave port that supports the DAP (Debug Access Port)

## 6.2 System Manager

### 6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- Power Modes and Wake-up Sources
- System Power Distribution
- SRAM Memory Organization
- System Control Register for Part Number ID, Chip Reset and Multi-function Pin Control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

### 6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS\_RSTSTS register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS\_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS\_IPRST0[1])

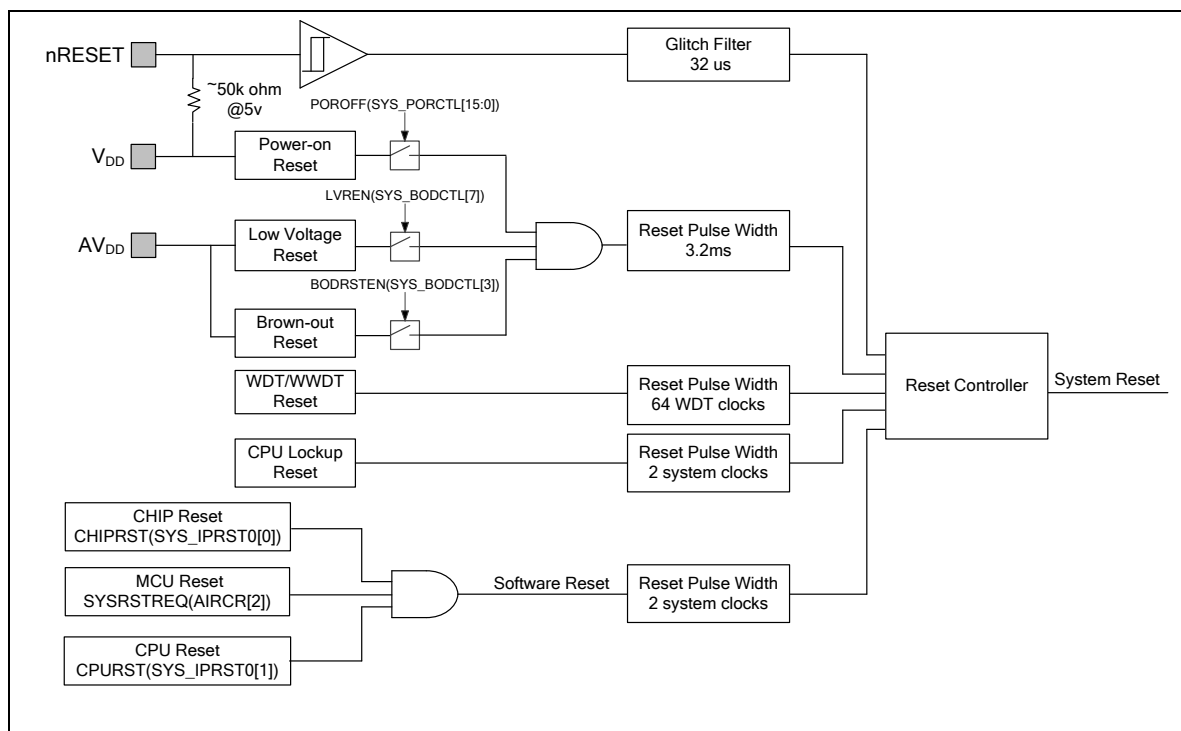


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro<sup>®</sup> family. In general, CPU reset is used to reset Cortex-M0 only; the other reset sources will reset Cortex-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

| Reset Sources Register               | POR                 | NRESET              | WDT                 | LVR                 | BOD                 | Lockup              | CHIP                | MCU                 | CPU       |
|--------------------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|-----------|
| <b>SYS_RSTSTS</b>                    | 0x001               | Bit 1 = 1           | Bit 2 = 1           | Bit 3 = 1           | Bit 4 = 1           | Bit 8 = 1           | Bit 0 = 1           | Bit 5 = 1           | Bit 7 = 1 |
| <b>CHIPRST</b><br>(SYS_IPRST0[0])    | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>BODEN</b><br>(SYS_BODCTL[0])      | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | -                   | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | -         |
| <b>BODVL</b><br>(SYS_BODCTL[2:1])    |                     |                     |                     |                     |                     |                     |                     |                     |           |
| <b>BODRSTEN</b><br>(SYS_BODCTL[3])   |                     |                     |                     |                     |                     |                     |                     |                     |           |
| <b>HXTEN</b><br>(CLK_PWRCTL[0])      | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | -         |
| <b>LXTEN</b><br>(CLK_PWRCTL[1])      | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>WDTCKEN</b><br>(CLK_APBCLK0[0])   | 0x1                 | -                   | 0x1                 | -                   | -                   | -                   | 0x1                 | -                   | -         |
| <b>HCLKSEL</b><br>(CLK_CLKSEL0[2:0]) | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | -         |
| <b>WDTSEL</b><br>(CLK_CLKSEL1[1:0])  | 0x3                 | 0x3                 | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>HXTSTB</b><br>(CLK_STATUS[0])     | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>LXTSTB</b><br>(CLK_STATUS[1])     | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>PLLSTB</b><br>(CLK_STATUS[2])     | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>HIRCSTB</b><br>(CLK_STATUS[4])    | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>CLKSFAIL</b><br>(CLK_STATUS[7])   | 0x0                 | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| <b>RSTEN</b><br>(WDT_CTL[1])         | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | -                   | Reload from CONFIG0 | -                   | -         |
| <b>WDTEN</b><br>(WDT_CTL[7])         |                     |                     |                     |                     |                     |                     |                     |                     |           |
| <b>WDT_CTL</b>                       | 0x0700              | 0x0700              | 0x0700              | 0x0700              | 0x0700              | -                   | 0x0700              | -                   | -         |

|                                                                    |                              |                              |                              |                              |                              |   |                              |   |   |
|--------------------------------------------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|---|------------------------------|---|---|
| except bit 1 and bit 7.                                            |                              |                              |                              |                              |                              |   |                              |   |   |
| WDT_ALTCTL                                                         | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | - | 0x0000                       | - | - |
| WWDT_RLDCNT                                                        | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | - | 0x0000                       | - | - |
| WWDT_CTL                                                           | 0x3F0800                     | 0x3F0800                     | 0x3F0800                     | 0x3F0800                     | 0x3F0800                     | - | 0x3F0800                     | - | - |
| WWDT_STATUS                                                        | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | - | 0x0000                       | - | - |
| WWDT_CNT                                                           | 0x3F                         | 0x3F                         | 0x3F                         | 0x3F                         | 0x3F                         | - | 0x3F                         | - | - |
| BS<br>(FMC_ISPCTL[1])                                              | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | - | Reload<br>from<br>CONFIG0    | - | - |
| BL<br>(FMC_ISPCTL[16])                                             |                              |                              |                              |                              |                              |   |                              |   |   |
| FMC_DFBA                                                           | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | - | Reload<br>from<br>CONFIG1    | - | - |
| CBS<br>(FMC_ISPSTS[2:1])                                           | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | - | Reload<br>from<br>CONFIG0    | - | - |
| VECMAP<br>(FMC_ISPSTS[23:9])                                       | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | - | Reload<br>base on<br>CONFIG0 | - | - |
| Other Peripheral<br>Registers                                      | Reset Value                  |                              |                              |                              |                              |   |                              |   | - |
| FMC Registers                                                      | Reset Value                  |                              |                              |                              |                              |   |                              |   |   |
| Note: '-' means that the value of register keeps original setting. |                              |                              |                              |                              |                              |   |                              |   |   |

Table 6.2-1 Reset Value of Registers

### 6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than  $0.2 V_{DD}$  and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above  $0.7 V_{DD}$  and the state keeps longer than 32 us (glitch filter). The PINRF(SYS\_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

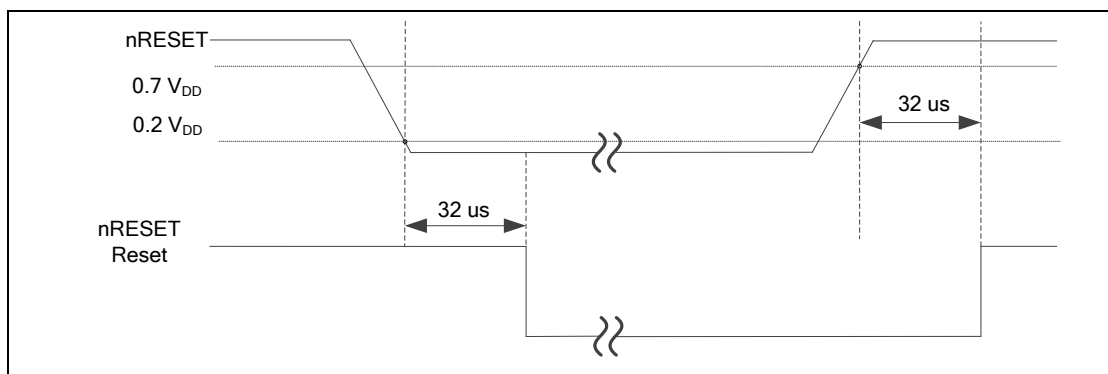


Figure 6.2-2 nRESET Reset Waveform

#### 6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS\_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS\_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

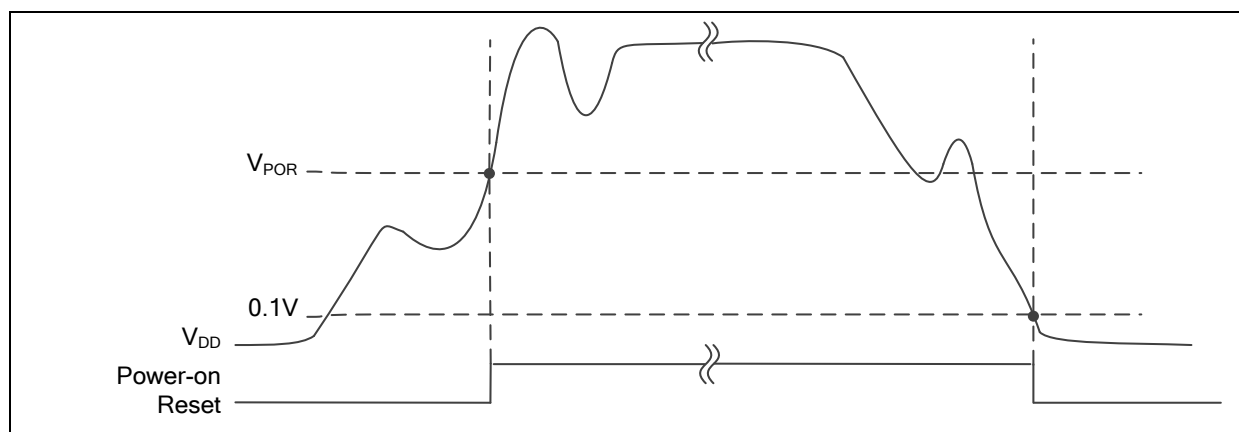


Figure 6.2-3 Power-on Reset (POR) Waveform

#### 6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS\_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect  $AV_{DD}$  during system operation. When the  $AV_{DD}$  voltage is lower than  $V_{LVR}$  and the state keeps longer than De-glitch time set by LVRDGSEL (SYS\_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the  $AV_{DD}$  voltage rises above  $V_{LVR}$  and the state keeps longer than De-glitch time set by LVRDGSEL (SYS\_BODCTL[14:12]). The LVRF(SYS\_RSTSTS[3]) will be set to 1 if the previous reset source is LVR reset. The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

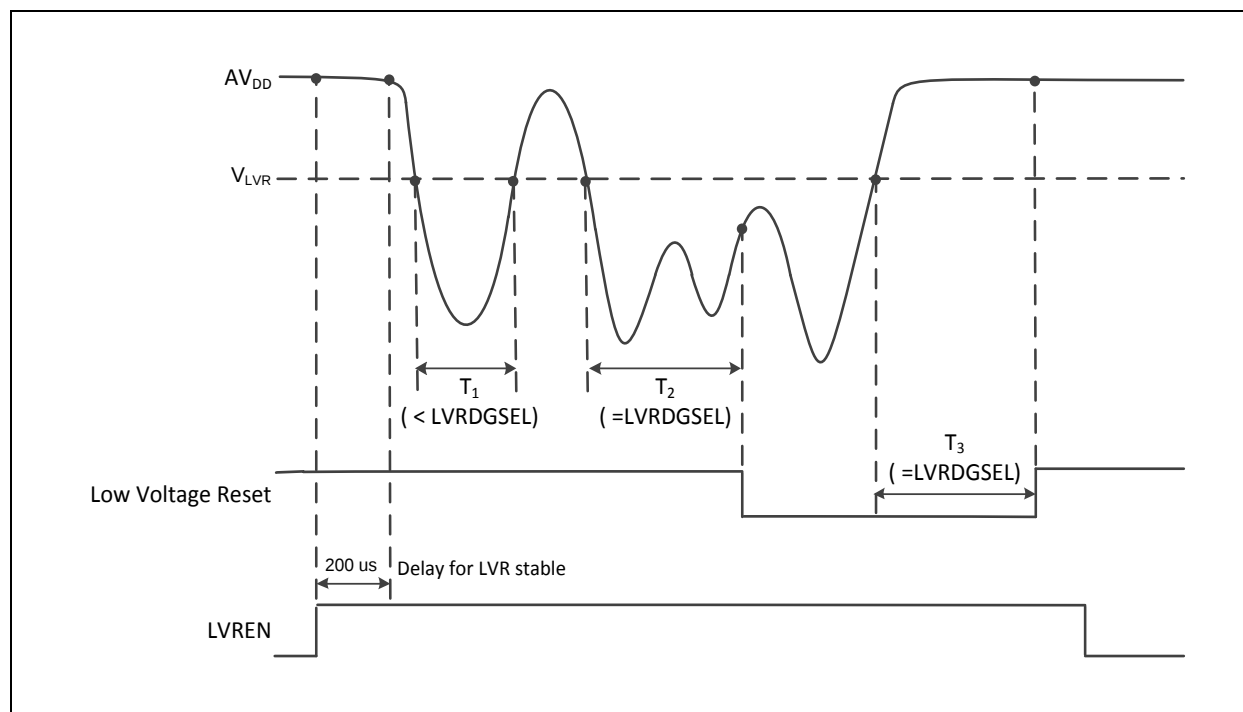


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

#### 6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS\_BODCTL[0]), Brown-Out Detector function will detect  $AV_{DD}$  during system operation. When the  $AV_{DD}$  voltage is lower than  $V_{BOD}$  which is decided by BOD\_EN (BODCR[0]) and BOD\_VL (BODCR[2:1]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS\_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the  $AV_{DD}$  voltage rises above  $V_{BOD}$  and the state keeps longer than De-glitch time set by BODDGSEL (SYS\_BODCTL[10:8]). The default value of BODEN, BODVL and BODRSTEN(SYS\_BODCTL[3]) is set by flash controller user configuration register CBODEN (CONFIG0 [23]), CBOV (CONFIG0 [22:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-Out Detector waveform.

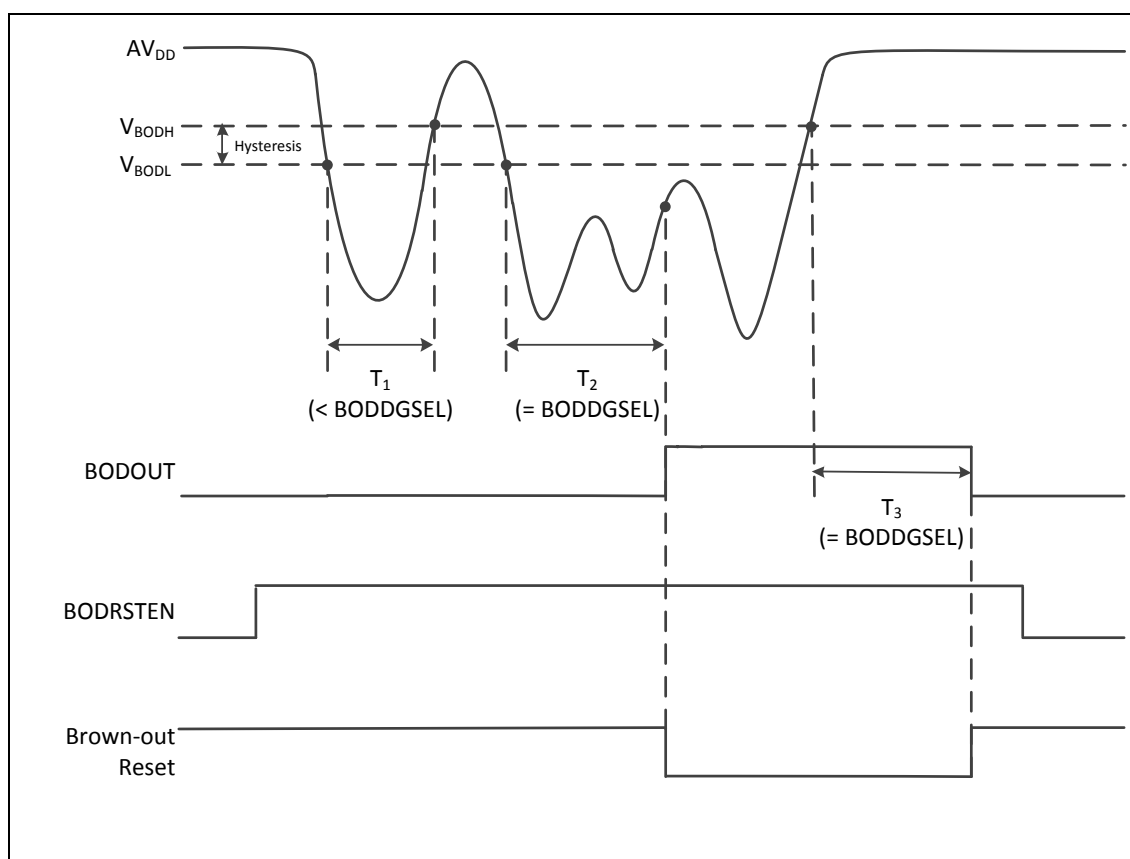


Figure 6.2-5 Brown-out Detector (BOD) Waveform

#### 6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS\_RSTSTS[2]).

#### 6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

#### 6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS\_IPRST0[1]) to 1 to assert the CPU Reset

signal.

The CHIP Reset is same with Power-On Reset. The CPU and all peripherals are reset and BS(FMC\_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS\_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC\_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

### 6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

| Power Mode       | Normal Mode                                        | Idle Mode                     | Power-Down Mode                                                                       |
|------------------|----------------------------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Definition       | CPU is in active state                             | CPU is in sleep state         | CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended. |
| Entry Condition  | Chip is in normal mode after system reset released | CPU executes WFI instruction. | CPU sets sleep mode enable and power down enable and executes WFI instruction.        |
| Wake-up Sources  | N/A                                                | All interrupts                | WDT, I <sup>2</sup> C, Timer, UART, BOD, GPIO, EINT, USCI and USBDM.                  |
| Available Clocks | All                                                | All except CPU clock          | LXT and LIRC                                                                          |
| After Wake-up    | N/A                                                | CPU back to normal mode       | CPU back to normal mode                                                               |

Table 6.2-2 Power Mode Difference Table

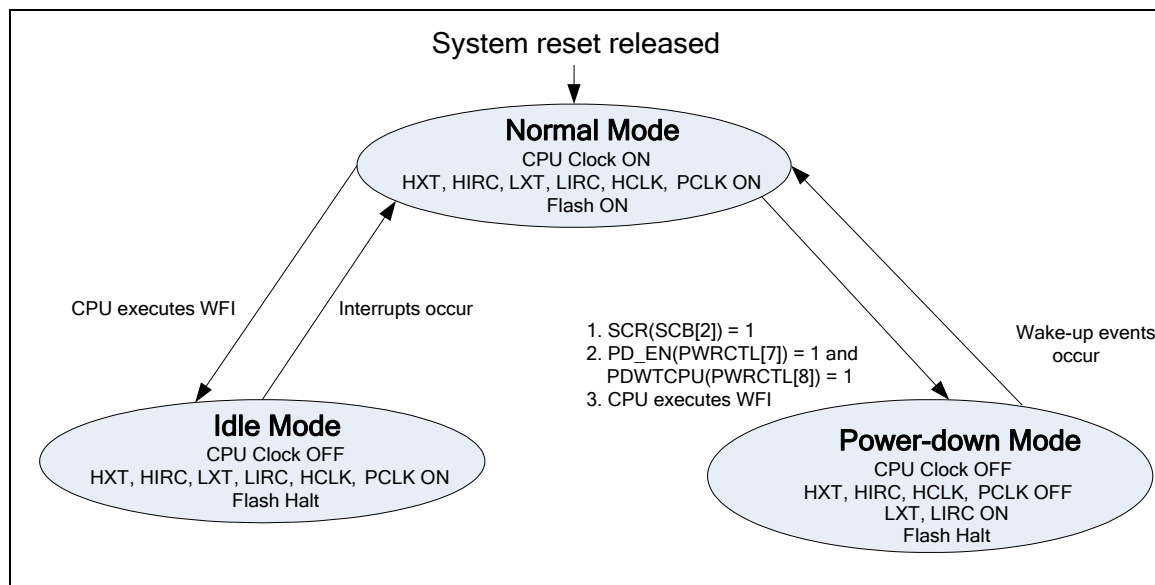


Figure 6.2-6 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in run mode.
2. LIRC (10 kHz OSC) ON or OFF depends on SW setting in run mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If UART clock source is selected as LXT and LXT is on.

|                      | Normal Mode | Idle Mode | Power-Down Mode     |
|----------------------|-------------|-----------|---------------------|
| HXT (4~24 MHz XTL)   | ON          | ON        | Halt                |
| HIRC (48 MHz OSC)    | ON          | ON        | Halt                |
| LXT (32768 Hz XTL)   | ON          | ON        | ON/OFF <sup>1</sup> |
| LIRC (10 kHz OSC)    | ON          | ON        | ON/OFF <sup>2</sup> |
| PLL                  | ON          | ON        | Halt                |
| LDO                  | ON          | ON        | ON                  |
| CPU                  | ON          | Halt      | Halt                |
| HCLK/PCLK            | ON          | ON        | Halt                |
| SRAM retention       | ON          | ON        | ON                  |
| FLASH                | ON          | ON        | Halt                |
| GPIO                 | ON          | ON        | Halt                |
| PDMA                 | ON          | ON        | Halt                |
| TIMER                | ON          | ON        | ON/OFF <sup>3</sup> |
| BPWM                 | ON          | ON        | Halt                |
| PWM                  | ON          | ON        | Halt                |
| WDT                  | ON          | ON        | ON/OFF <sup>4</sup> |
| WWDT                 | ON          | ON        | Halt                |
| USCI                 | ON          | ON        | Halt                |
| UART                 | ON          | ON        | ON/OFF <sup>5</sup> |
| I <sup>2</sup> C     | ON          | ON        | Halt                |
| SPI/I <sup>2</sup> S | ON          | ON        | Halt                |
| USBD                 | ON          | ON        | Halt                |
| ADC                  | ON          | ON        | Halt                |

Table 6.2-3 Clocks in Power Modes

#### Wake-up Sources in Power-down Mode:

WDT, I<sup>2</sup>C, Timer, UART, BOD, GPIO, EINT, USCI and USB

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

\*User needs to wait this condition before setting PD\_EN(PWRCTL[6]) and execute WFI to enter Power-down mode.

| Wake-Up Source   | Wake-Up Condition                      | System Can Enter Power-Down Mode Again Condition*                                    |
|------------------|----------------------------------------|--------------------------------------------------------------------------------------|
| BOD              | Brown-Out Detector Interrupt           | After software writes 1 to clear SYS_BODCTL[BODIF].                                  |
| GPIO             | GPIO Interrupt                         | After software write 1 to clear the INTSRC[n] bit.                                   |
| TIMER            | Timer Interrupt                        | After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]). |
| WDT              | WDT Interrupt                          | After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).                   |
| UART             | RX Data wake-up                        | After software writes 1 to clear DATWKIF (UARTx_INTSTS[17]).                         |
|                  | nCTS wake-up                           | After software writes 1 to clear CTSWKIF (UARTx_INTSTS[16]).                         |
| I <sup>2</sup> C | Falling edge in the I2C_SDA or I2C_CLK | After software writes 1 to clear WKIF( I2C_WKSTS[0]).                                |
| USCI             |                                        |                                                                                      |
| USB              | Remote Wake-up                         | After software writes 1 to clear BUSIF (USB_INTSTS[0]).                              |

Table 6.2-4 Condition of Entering Power-down Mode Again

## 6.2.4 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV<sub>DD</sub> and AV<sub>SS</sub> provides the power for analog components operation.
- Digital power from V<sub>DD</sub> and V<sub>SS</sub> supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- A dedicated power from V<sub>DDIO</sub> supplies the power for PA.10, PA.11, PB.4 ~ PB.7, PB.12 ~ PB.14 and PD.8 ~ 11 of NUC125.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AV<sub>DD</sub>) should be the same voltage level of the digital power (V<sub>DD</sub>). Figure 6.2-7 shows the power distribution of the NuMicro<sup>®</sup> NUC121 and NUC125.

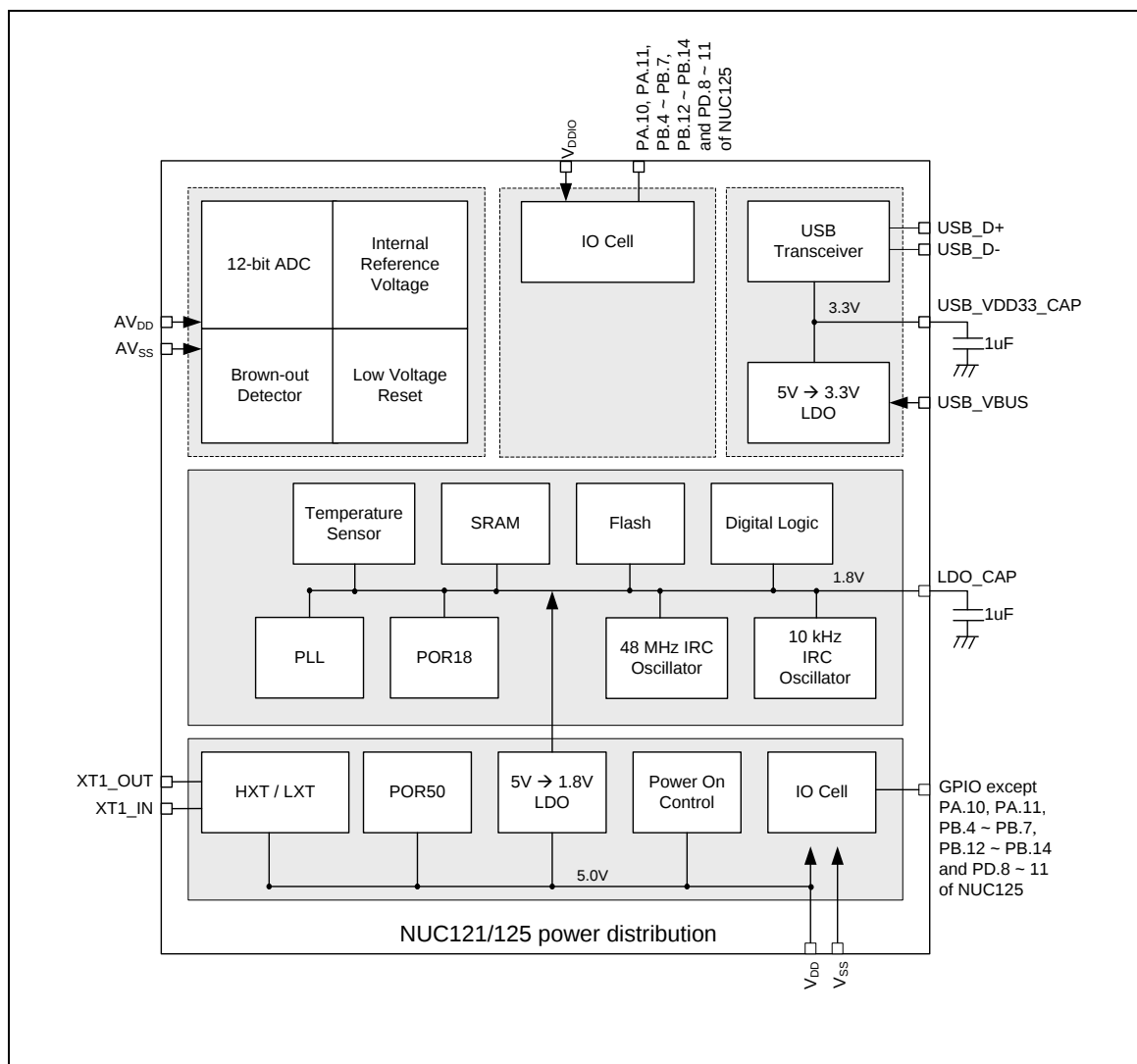


Figure 6.2-7 NuMicro® NUC121/125 Power Distribution Diagram

## 6.3 Clock Controller

### 6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK\_PWRCTL[7]) and Cortex<sup>®</sup>-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

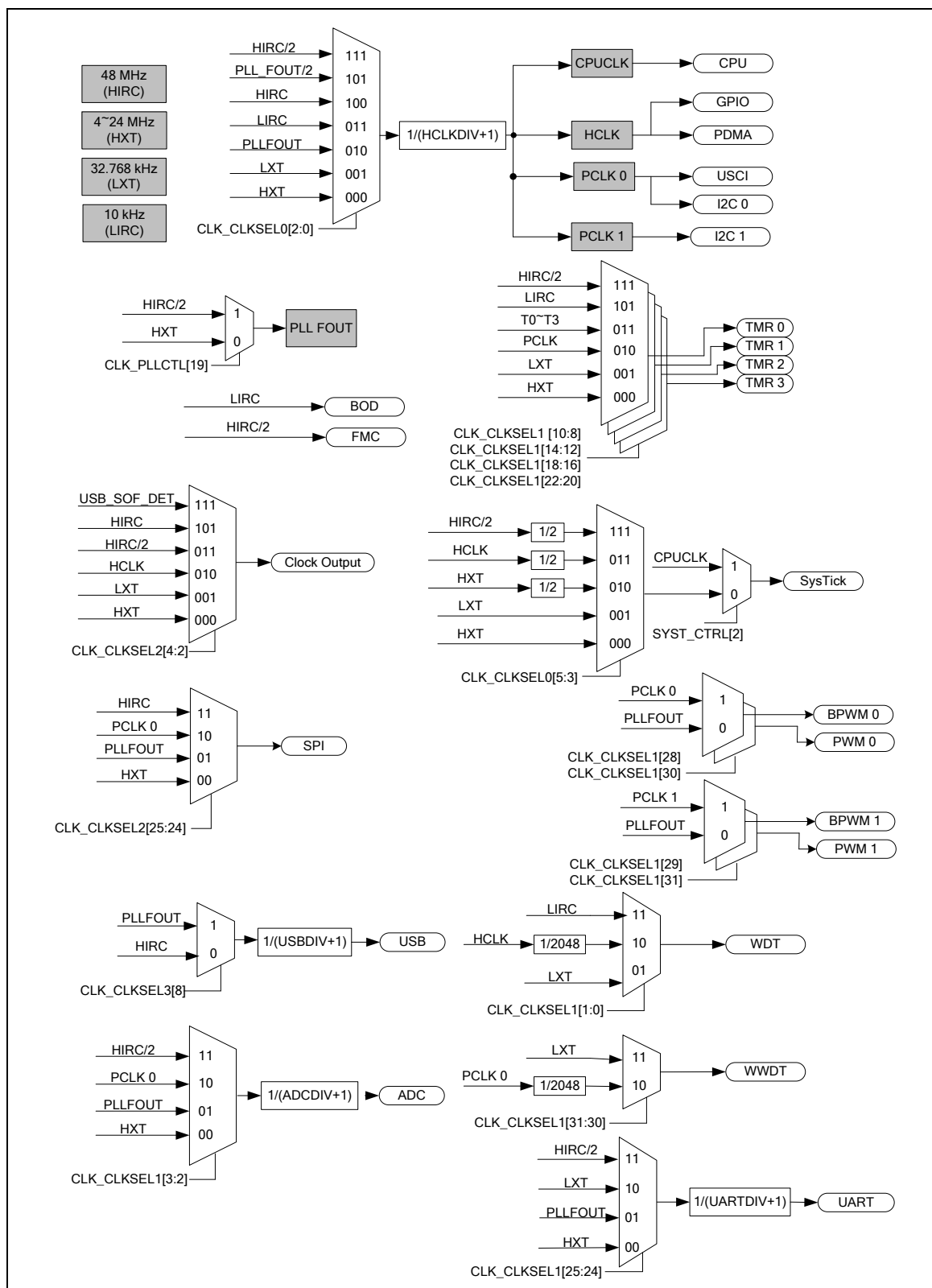


Figure 6.3-1 Clock Generator Global View Diagram

### 6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low-speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 24 MHz (Internal high speed oscillator, HIRC/2)
- 48 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index (HIRCSTB(CLK\_STATUS[4]), LIRCSTB(CLK\_STATUS[3]), PLLSTB(CLK\_STATUS[2]), HXTSTB(CLK\_STATUS[0]) and LXTSTB(CLK\_STATUS[1]) are set to 1 after stable counter value reach a define value as shown in the following table.

System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will auto clear when user disables the clock source (LIRCEN(CLK\_PWRCTL[3]), HIRCEN(CLK\_PWRCTL[2]), XTLEN(CLK\_PWRCTL[1:0]) and PD(CLK\_PLLCTL[16]). Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

| Clock Source | Clock Stable Count Value                                                                                                                                     | Clock Stable Time                                                         |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|
| HXT          | 4096 HXT clocks                                                                                                                                              | 341.33 uS for 12 Mhz                                                      |
| PLL          | It's based on the value of STBSEL (CLK_PLLCTL[23])<br>STBSEL = 0, stable count is 6144 PLL clocks.<br>STBSEL = 1, stable count is 12288 PLL clocks.(Default) | STBSEL = 0<br>122.88 uS for 50 Mhz<br>STBSEL = 1:<br>245.76 uS for 50 Mhz |
| HIRC         | 512 HIRC clocks                                                                                                                                              | 10.667 uS for 48Mhz                                                       |
| LIRC         | 1 LIRC clock                                                                                                                                                 | 100 uS for 10 kHz                                                         |
| LXT          | 8192 LXT clock                                                                                                                                               | 250 mS for 32 KHz                                                         |

Table 6.3-1 Clock Stable Count Value Table

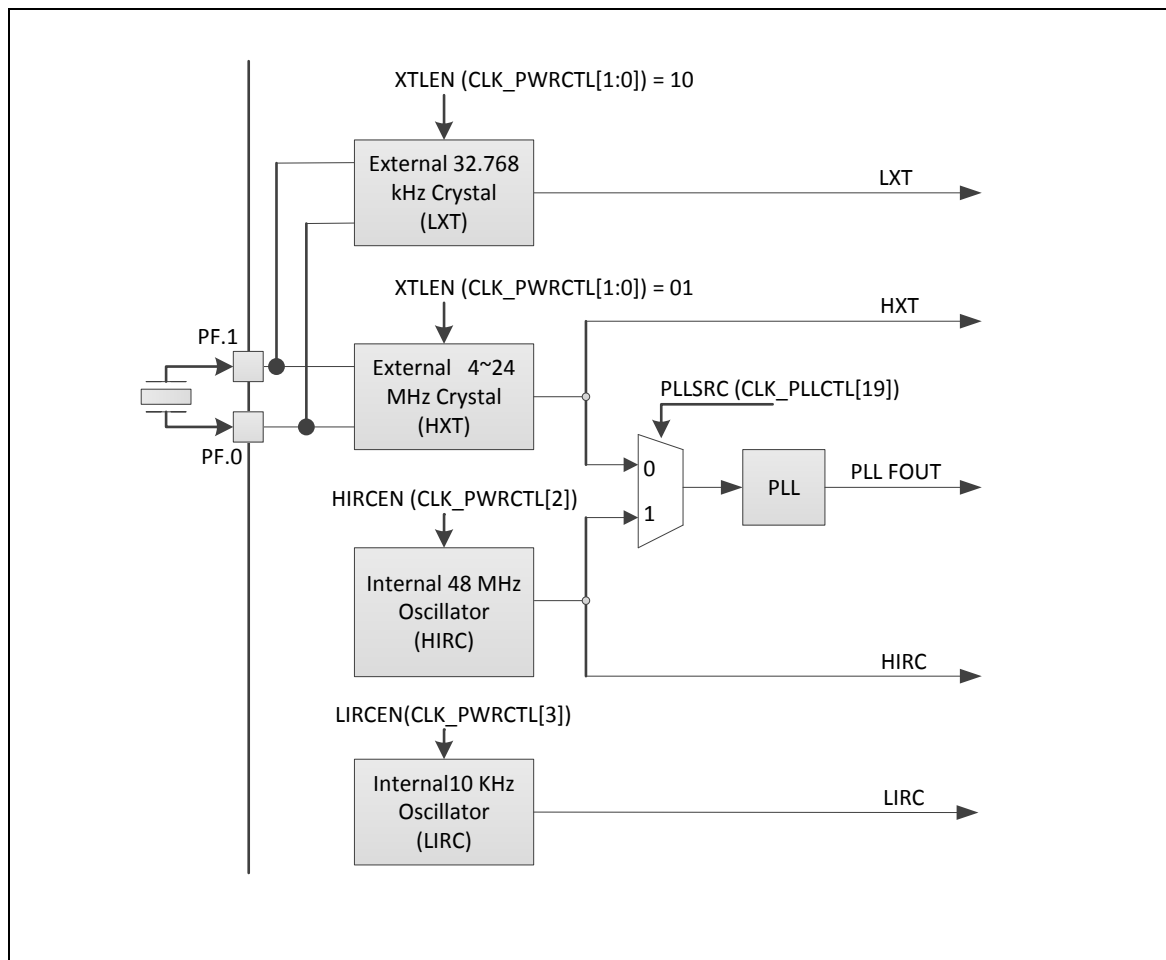


Figure 6.3-2 Clock Generator Block Diagram

### 6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK\_CLKSEL0 [2:0]). The block diagram is shown in Figure 6.3-3

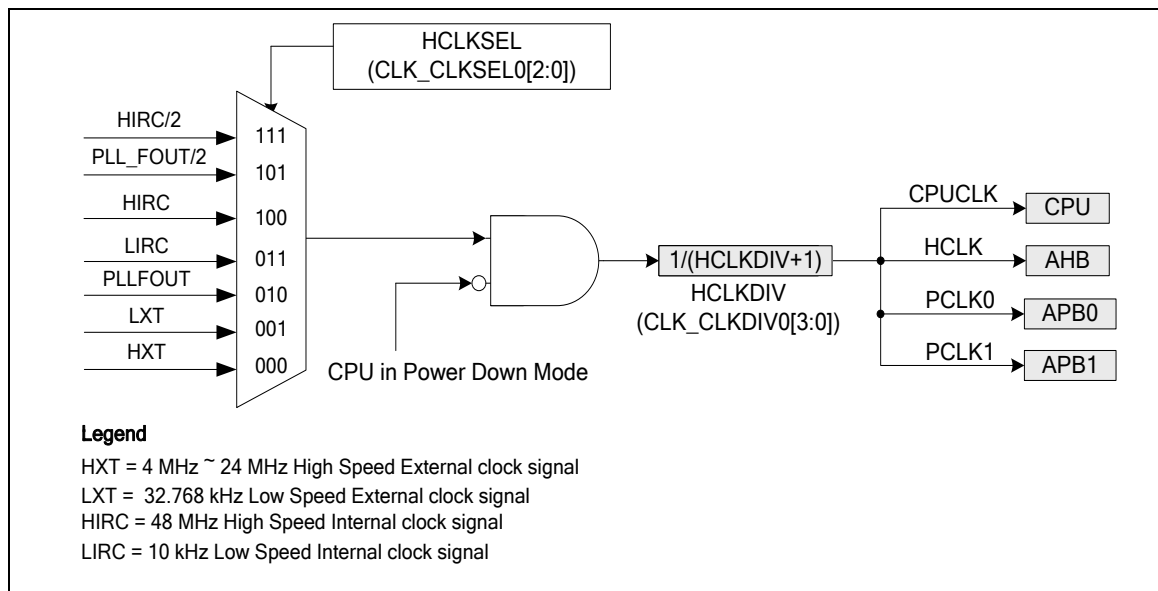


Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source if stop and they have individual enable and interrupt control. When HXT fail detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock fail detector is enabled, the system clock will auto switch to HIRC/2 (24 MHz) if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK\_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK\_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC/2 (24 MHz) procedure is shown in Figure 6.3-4

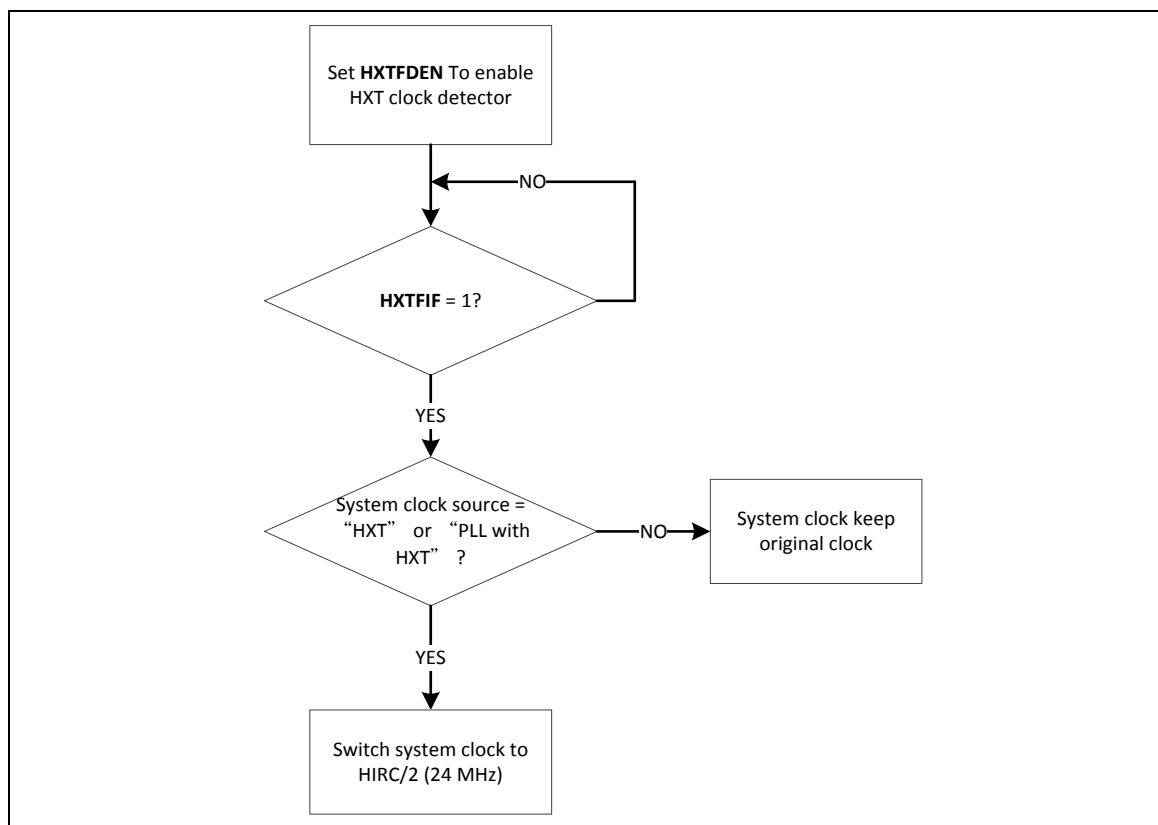


Figure 6.3-4 HXT Stop Protect Procedure

Except HXT fail(stop) detector, HXT also has a frequency detector to observe HXT clock frequency if normally and it also has individual enable(HXTFQDEN=CLK\_CLKDCTL[16]) and interrupt control (HXTFQIEN=CLK\_CLKDCTL[17]). When HXT frequency detector is enabled, the HIRC clock is enabled automatically. Otherwise, before HXT frequency detector is enabled, we need set the frequency detector upper boundary(UPERBD=CLK\_CDUPB[9:0]) and lower boundary (LOWERBD=CLK\_CDLOWB[9:0]).

If HXT clock frequency abnormally condition is detected, the HXTFQIF(CLK\_CLKDSTS[8]) is set to 1 and chip will enter interrupt if HXTFQIEN (CLK\_CLKDCTL[17]) is set to 1. Different with HXT fail(stop) detector, when HXT clock frequency abnormally condition is detected, the system clock will NOT auto switch to HIRC/2 (24 MHz) even though system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. The HXT frequency detector just reminds user HXT clock frequency abnormally through to observe HXTFQIF (CLK\_CLKDSTS[8]).

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST\_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK\_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5

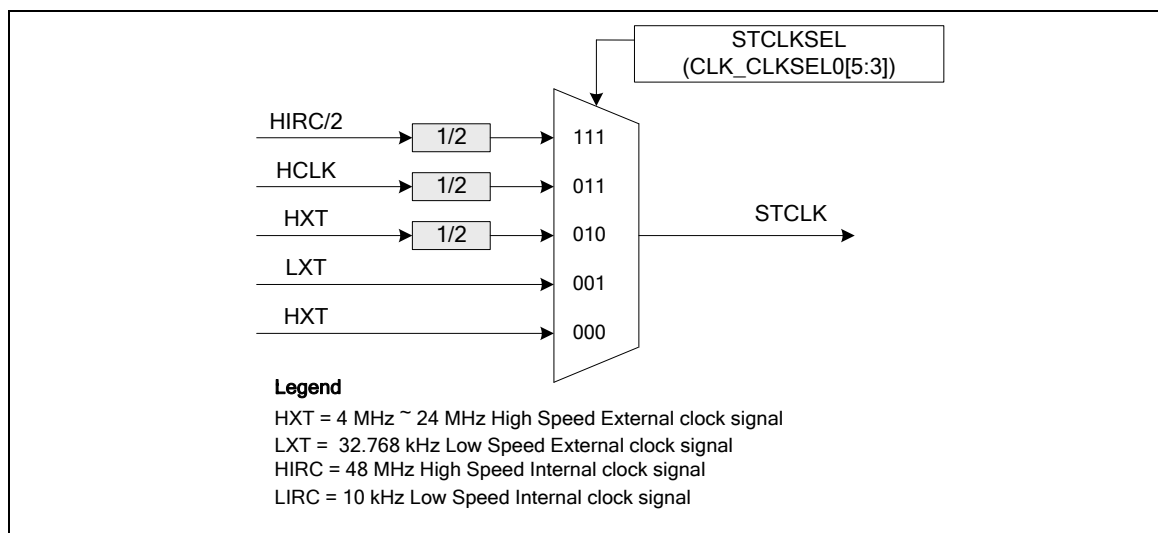


Figure 6.3-5 SysTick Clock Control Block Diagram

### 6.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting, which depends on the different peripheral.

### 6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources, and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For these clocks, which still keep active, are listed below:

- Clock Generator
  - ◆ 10 kHz internal low-speed RC oscillator (LIRC) clock
  - ◆ 32.768 kHz external low-speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

### 6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from  $F_{in}/2^1$  to  $F_{in}/2^{16}$  where  $F_{in}$  is input clock frequency to the clock divider.

The output formula is  $F_{out} = F_{in}/2^{(N+1)}$ , where  $F_{in}$  is the input clock frequency,  $F_{out}$  is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK\_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK\_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK\_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

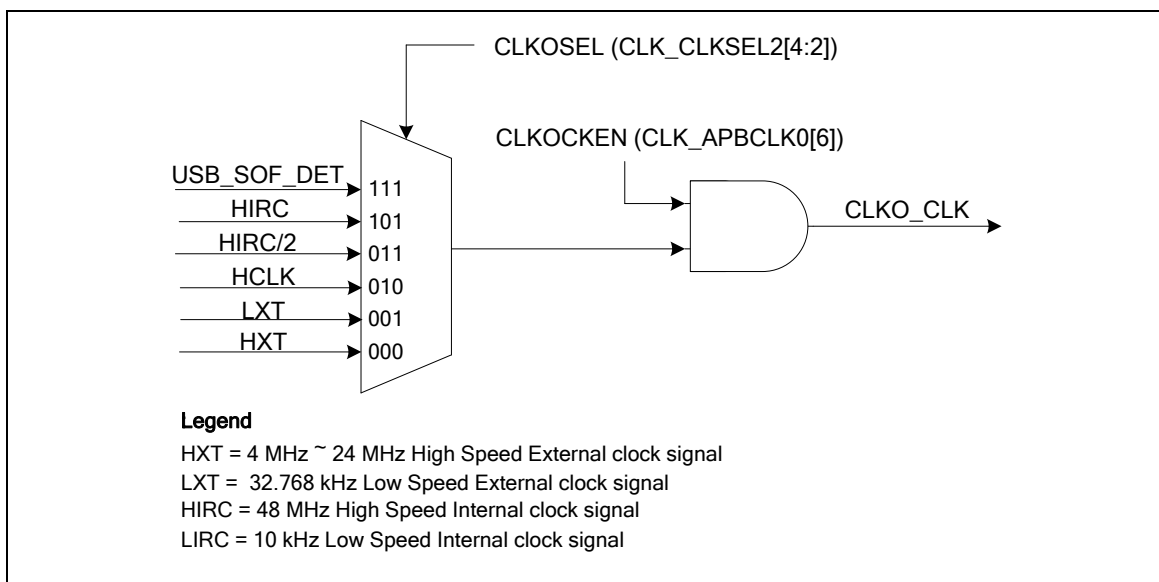


Figure 6.3-6 Clock Source of Clock Output

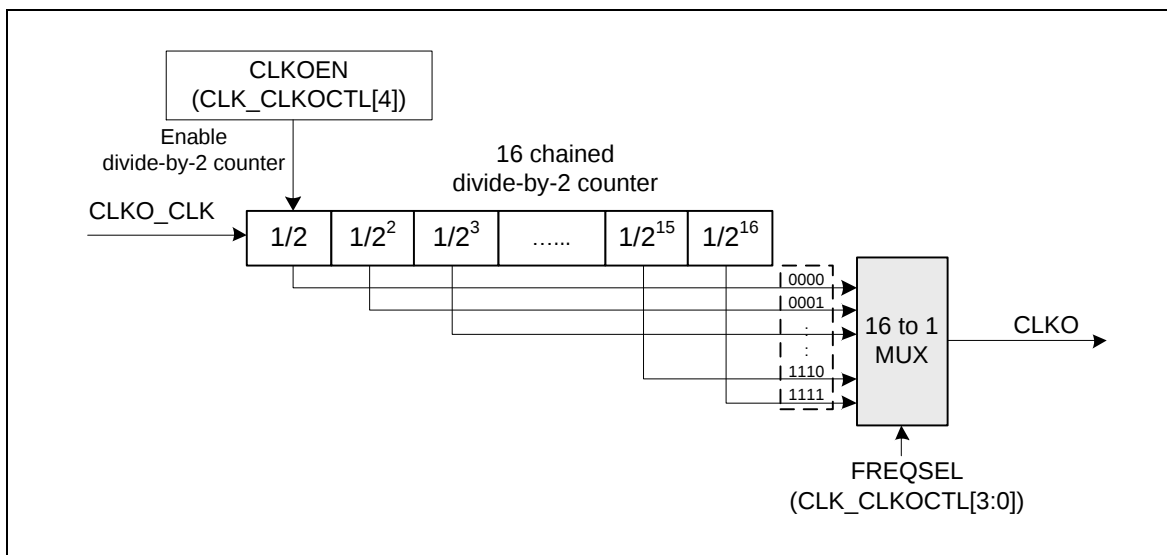


Figure 6.3-7 Clock Output Block Diagram

## 6.4 Flash Memory Controller (FMC)

### 6.4.1 Overview

The NUC121/125 series is equipped with 32 K-bytes on-chip embedded flash for application and Data Flash to store some application dependent data. A User Configuration block provides for system initialization. A 4.5 K-bytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 512 bytes security protection ROM (SPROM) can conceal user program. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

### 6.4.2 Features

- Supports 32 K-bytes application ROM (APROM).
- Supports 4.5 K-bytes loader ROM (LDROM).
- Supports configurable Data Flash size to share with APROM.
- Supports 512 bytes security protection ROM (SPROM) to conceal user program.
- Supports 12 bytes User Configuration block to control system initialization.
- Supports 512 bytes page erase for all embedded flash.
- Supports CRC-32 checksum calculation function (must be 512 bytes page alignment).
- Supports APROM, LDROM and embedded SRAM remap to system vector memory.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory.

## 6.5 General Purpose I/O (GPIO)

### 6.5.1 Overview

The NUC121/125 series has up to 52 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 52 pins are arranged in 6 ports named as PA, PB, PC, PD, PE and PF.

PA has 6 pins on port (PA.10 ~ PA.15).

PB has 15 pins on port (PB.0 ~ PB.15, exclude PB.11).

PC has 12 pins on port (PC.0 ~ PC.13, exclude PC.6, PC.7).

PD has 10 pins on port (PD.0 ~ PD.11, exclude PD.6, PD.7).

PE has 3 pins on port (PE.0 ~ PE.2).

PF has 6 pins on port (PF.0 ~ PF.5).

Each of the 52 pins is independent and has the corresponding register bits to control the pin mode function and data

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up resistor which is about 110 k $\Omega$  ~ 300 k $\Omega$  for V<sub>DD</sub> is from 5.0 V to 2.5 V.

### 6.5.2 Features

- Four I/O modes:
  - ◆ Quasi-bidirectional mode
  - ◆ Push-Pull Output mode
  - ◆ Open-Drain Output mode
  - ◆ Input mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Slew Rate I/O mode
- Supports High Drive Strength mode for Port C
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - ◆ CIOIN = 0, all GPIO pins in input mode after chip reset
  - ◆ CIOIN = 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

## 6.6 PDMA Controller (PDMA)

### 6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory. The PDMA supports time-out function for channel 0 and channel 1.

### 6.6.2 Features

- Supports 5 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, I<sup>2</sup>S, I<sup>2</sup>C, USCI, ADC, PWM and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function for channel 0 and channel 1

## 6.7 Timer Controller (TMR)

### 6.7.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

### 6.7.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx\_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx\_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, BPWM, PDMA, ADC and DAC function

## 6.8 Basic PWM Generator and Capture Timer (BPWM)

### 6.8.1 Overview

The NUC121/125 series provides two BPWM generators: BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

### 6.8.2 Features

#### 6.8.2.1 BPWM function features

- Supports maximum clock frequency up to 100 MHz
- Supports up to two BPWM modules, each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution BPWM counter, each module provides 1 BPWM counter
  - ◆ Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt on the following events:
  - ◆ BPWM counter match zero, period value or compared value
- Supports trigger ADC on the following events:
  - ◆ BPWM counter match zero, period value or compared value

#### 6.8.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising edge or falling edge or both edges capture condition
- Supports input rising/falling edge or both edges capture interrupt
- Supports rising/falling or both edges capture with counter reload option

## 6.9 PWM Generator and Capture Timer (PWM)

### 6.9.1 Overview

The NUC121/125 series provides two PWM generators — PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses the comparator compared with counter to generate events. These events are used to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, which have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask, tri-state output enable and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened.

### 6.9.2 Features

#### 6.9.2.1 PWM function features

- Supports maximum clock frequency up to 100 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - ◆ Dead-time insertion with 12-bit resolution
- Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter, each module provides 3 PWM counters
  - ◆ Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - ◆ Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
  - ◆ Noise filter for brake source from pin
  - ◆ Edge detect brake source to control brake state until brake interrupt cleared
  - ◆ Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - ◆ PWM counter match zero, period value or compared value
  - ◆ Brake condition happened
- Supports trigger ADC on the following events:
  - ◆ PWM counter match zero, period value or compared value

#### 6.9.2.2 *Capture Function Features*

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

## 6.10 Watchdog Timer (WDT)

### 6.10.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

### 6.10.2 Features

- 18-bit free running up counter for WDT time-out interval.
- Selectable time-out interval ( $2^4 \sim 2^{18}$ ) and the time-out interval is 1.6 ms ~ 26.214 s if WDT\_CLK = 10 kHz.
- System kept in reset state for a period of  $(1 / \text{WDT\_CLK}) * 63$ .
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT\_CLK reset delay period.
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register.
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT.

## 6.11 Window Watchdog Timer (WWDT)

### 6.11.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

### 6.11.2 Features

- 6-bit down counter value CNTDAT(WWDT\_CNT[5:0]) and maximum 6-bit compare value CMPDAT(WWDT\_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value PSCSEL(WWDT\_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode
- WWDT counter only can be reloaded within in valid window period to prevent system reset

## 6.12 USCI - Universal Serial Control Interface Controller

### 6.12.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I<sup>2</sup>C functional protocol.

### 6.12.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I<sup>2</sup>C

To increase readability, the registers of USCI have different alias names that depending on the selected protocol. For example, register USCI\_CTL has alias name *UUART\_CTL* for protocol UART, has alias name *USPI\_CTL* for protocol SPI, and has alias name *UI2C\_CTL* for protocol I<sup>2</sup>C.

## **6.13 USCI - UART Mode**

### **6.13.1 Overview**

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system by incoming data or nCTS.

### **6.13.2 Features**

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Supports 9-Bit Data Transfer (9-Bit RS-485)
- Supports baud rate detection by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

## 6.14 USCI - SPI Mode

### 6.14.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI\_CTL[2:0]) = 0x1.

This SPI protocol can operate as master or slave mode by setting the SLAVE (USPI\_PROTCTL[0]) to communicate with the off-chip SPI slave or master device. The application block diagrams in master and slave mode are shown below.

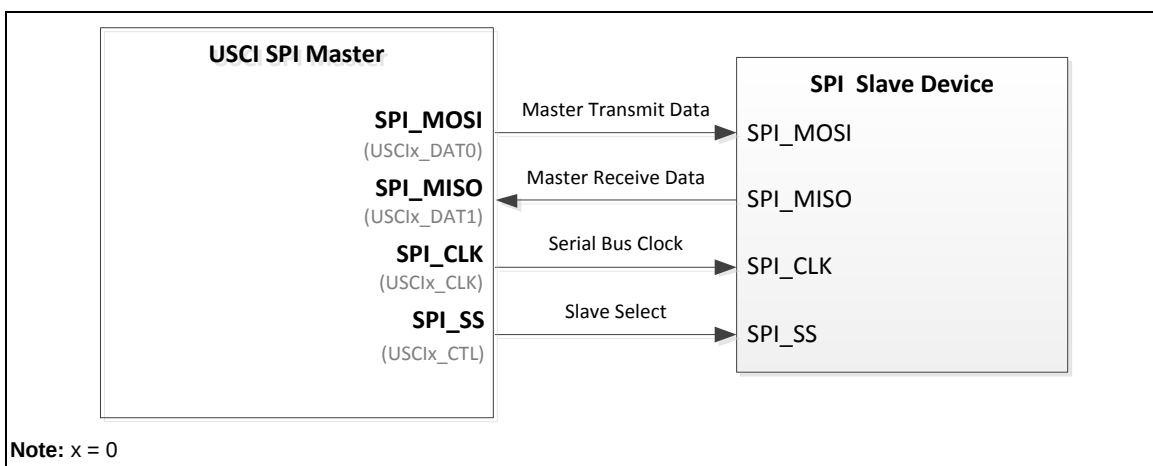


Figure 6.14-1 SPI Master Mode Application Block Diagram

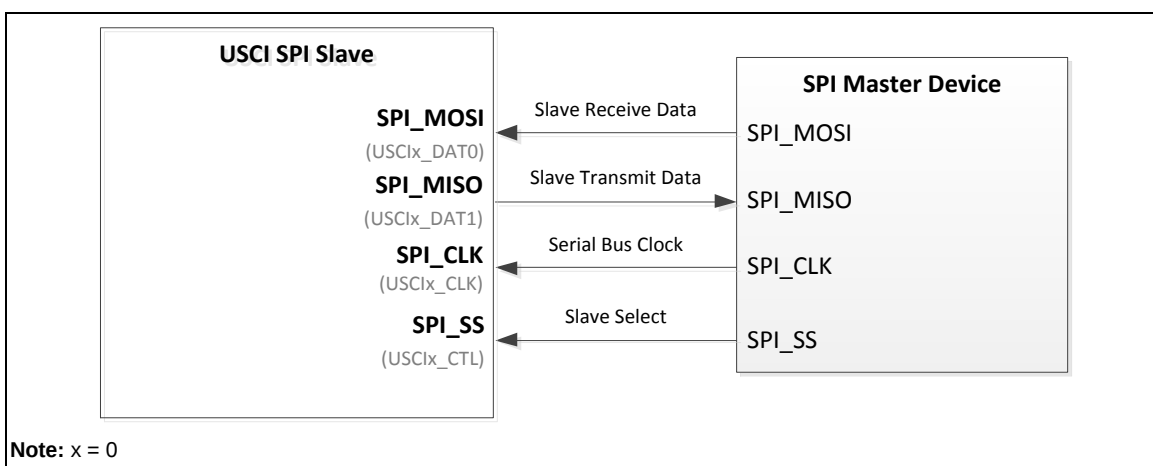


Figure 6.14-2 SPI Slave Mode Application Block Diagram

### 6.14.2 Features

- Supports master or slave mode operation (the maximum frequency for Master =  $f_{PCLK} / 2$ , for Slave <  $f_{PCLK} / 5$ )

- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports word suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

## 6.15 USCI - I<sup>2</sup>C Mode

### 6.15.1 Overview

On I<sup>2</sup>C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.15-1 for more detailed I<sup>2</sup>C BUS Timing.

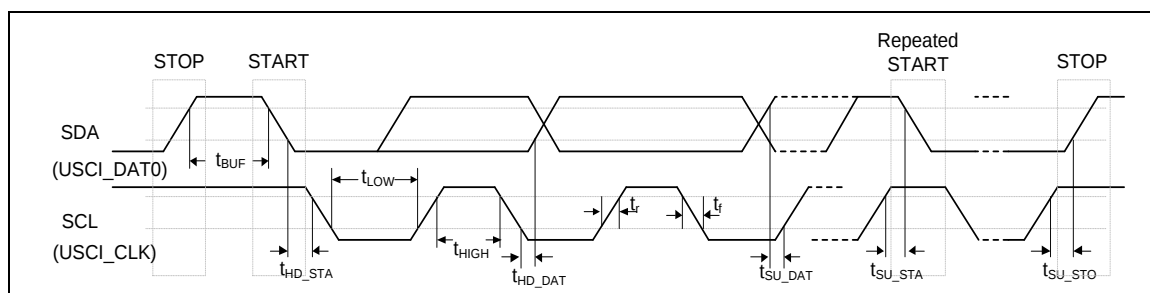


Figure 6.15-1 I<sup>2</sup>C Bus Timing

The device's on-chip I<sup>2</sup>C provides the serial interface that meets the I<sup>2</sup>C bus standard mode specification. The I<sup>2</sup>C port handles byte transfers autonomously. The I<sup>2</sup>C mode is selected by FUNMODE (UI2C\_CTL [2:0]) = 100b. When enable this port, the USCI interfaces to the I<sup>2</sup>C bus via two pins: SDA and SCL. When I/O pins are used as I<sup>2</sup>C ports, user must set the pins function to I<sup>2</sup>C in advance.

**Note:** Pull-up resistor is needed for I<sup>2</sup>C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I<sup>2</sup>C operation mode .

### 6.15.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

## 6.16 UART Interface Controller (UART)

### 6.16.1 Overview

The NUC121/125 series provides one channel of Universal Asynchronous Receiver/Transmitters (UART). UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and RS-485 function modes and auto-baud rate measuring function.

### 6.16.2 Features

- Full-duplex asynchronous communications
- Supports maximum clock frequency up to 10 Mbps
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART\_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - ◆ Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - ◆ Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - ◆ Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - ◆ Supports for 3/16 bit duration for normal mode
- Supports LIN function mode
  - ◆ Supports LIN master/slave mode
  - ◆ Supports programmable break generation function for transmitter
  - ◆ Supports break detection function for receiver
- Supports RS-485 function mode
  - ◆ Supports RS-485 9-bit mode
  - ◆ Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction

- Supports PDMA transfer function

## 6.17 I<sup>2</sup>C Serial Interface Controller (I<sup>2</sup>C)

### 6.17.1 Overview

I<sup>2</sup>C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I<sup>2</sup>C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I<sup>2</sup>C controllers which support Power-down wake-up function.

### 6.17.2 Features

The I<sup>2</sup>C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I<sup>2</sup>C bus include:

- Supports up to two I<sup>2</sup>C ports
- Supports speed up to 1Mbps
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I<sup>2</sup>C interrupt if the I<sup>2</sup>C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable

## 6.18 Serial Peripheral Interface (SPI)

### 6.18.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NUC121/125 series contains one SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI controller can be configured as a master or a slave device.

This controller also supports the PDMA function to access the data buffer. The SPI controller also supports I<sup>2</sup>S mode to connect external audio CODEC.

### 6.18.2 Features

- SPI Mode
  - ◆ One set of SPI controller
  - ◆ Supports Master or Slave mode operation
  - ◆ Configurable bit length of a transaction word from 8 to 32-bit
  - ◆ Provides separate 4-level depth transmit and receive FIFO buffers
  - ◆ Supports MSB first or LSB first transfer sequence
  - ◆ Supports Byte Reorder function
  - ◆ Supports PDMA transfer
  - ◆ Supports one data channel half-duplex transfer
  - ◆ Support receive-only mode
- I<sup>2</sup>S Mode
  - ◆ Supports Master or Slave
  - ◆ Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - ◆ Provides separate 4-level depth transmit and receive FIFO buffers
  - ◆ Supports monaural and stereo audio data
  - ◆ Supports PCM mode A, PCM mode B, I<sup>2</sup>S and MSB justified data format
  - ◆ Supports PDMA transfer

## 6.19 USB Device Controller (USBD)

### 6.19.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types. It implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 768 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD\_BUFSEGN, n=0~7).

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of "Endpoint Control" is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are five different interrupt events in this controller. They are the SOF event, no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD\_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD\_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD\_SE0), the USB controller will force the output of USB\_D+ and USB\_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1*.

### 6.19.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (NEVWK, VBUSDET, USB, BUS and SOF)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 768 bytes buffer size
- Provides remote wake-up capability
- Start of Frame (SOF) locked clock pulse generation
- Supports USB 2.0 Link Power Management

## 6.20 Analog-to-Digital Converter (ADC)

### 6.20.1 Overview

The NUC121/125 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 14 input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/PC.8), timer0~3 overflow pulse trigger and PWM trigger.

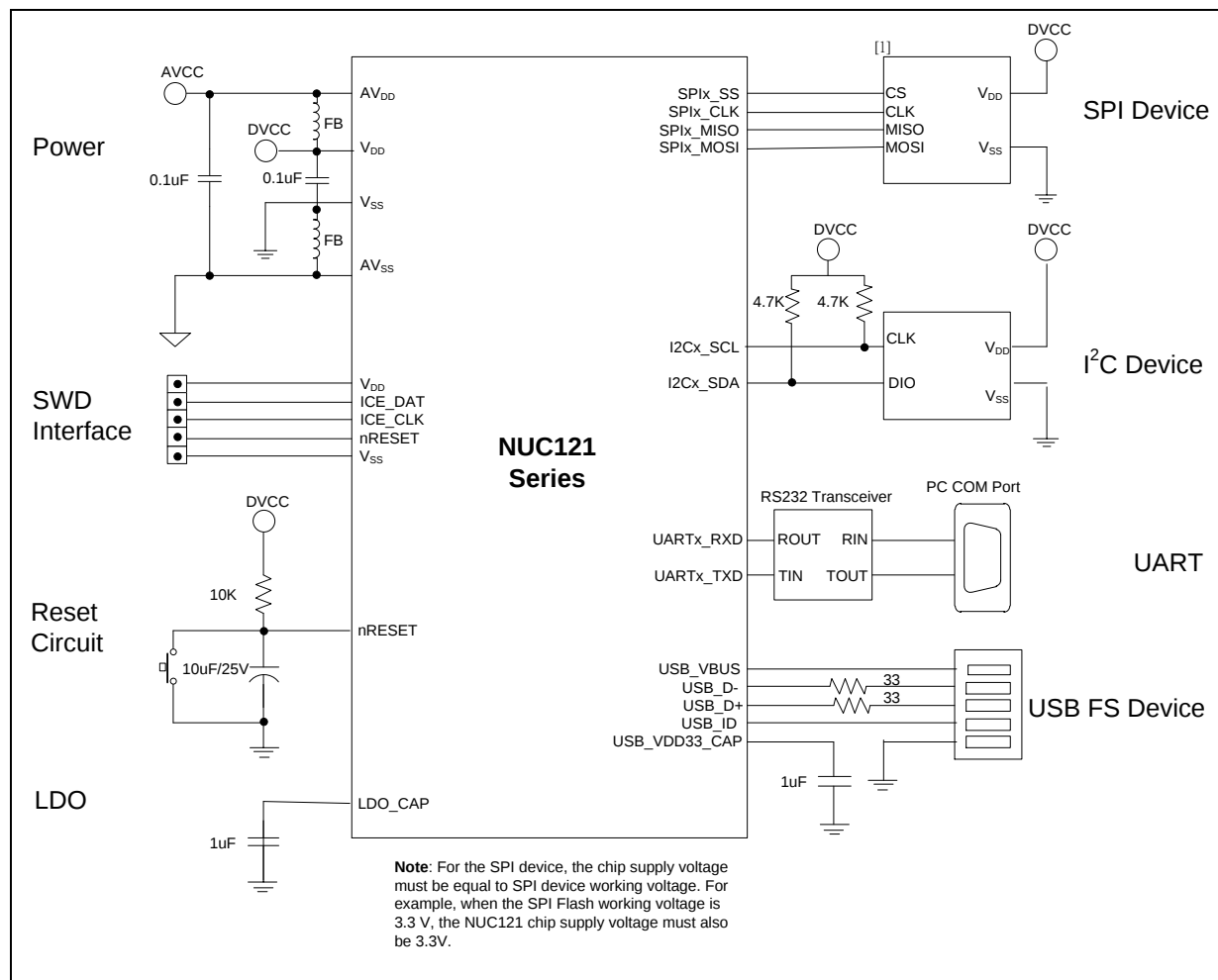
### 6.20.2 Features

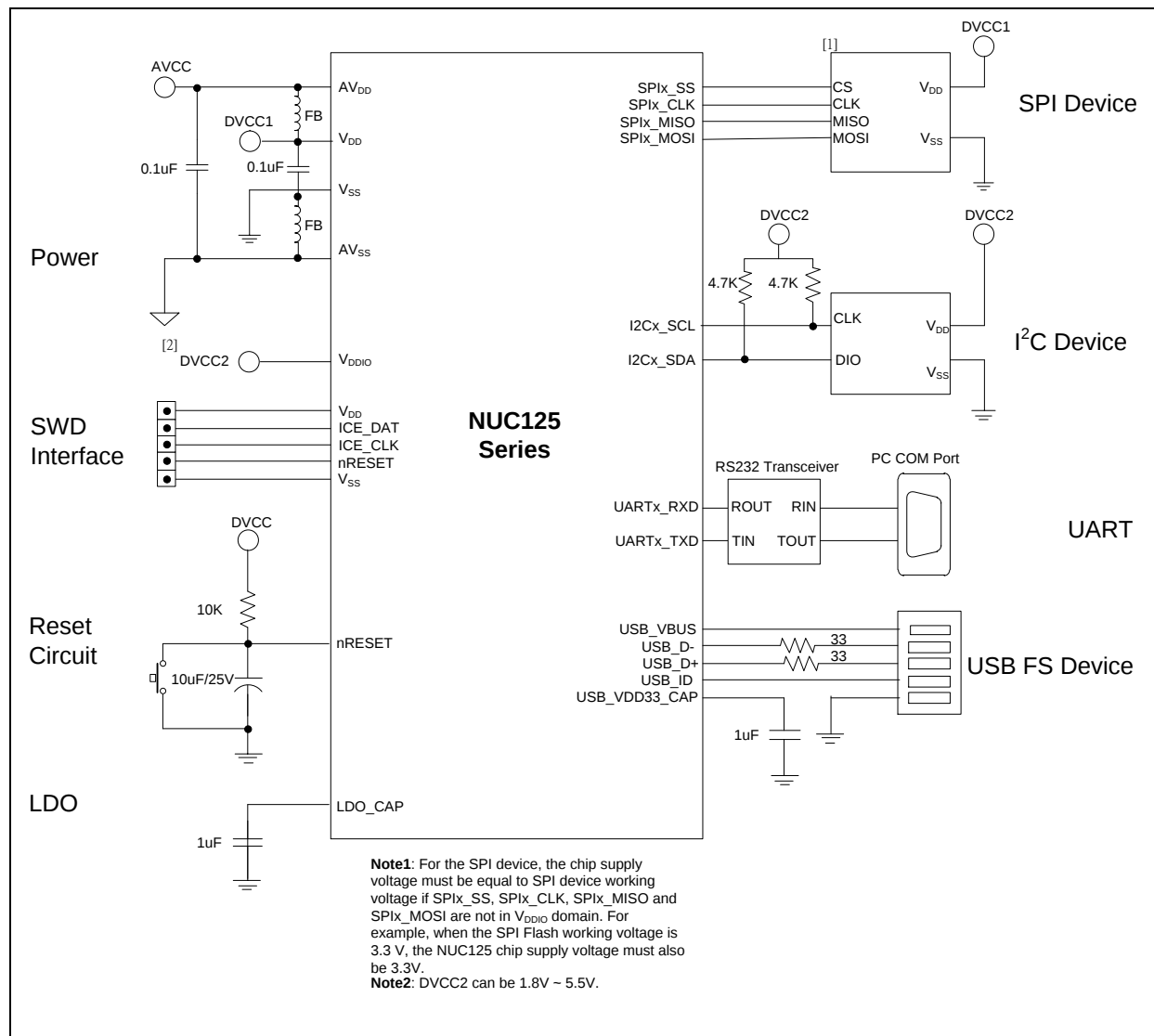
- Analog input voltage range: 0 ~  $AV_{DD}$ .
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 12 single-end analog input channels or 6 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 800k SPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - ◆ Single mode: A/D conversion is performed one time on a specified channel.
  - ◆ Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - ◆ Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - ◆ Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - ◆ Software Write 1 to ADST bit
  - ◆ External pin (STADC)
  - ◆ Timer 0~3 overflow pulse trigger
  - ◆ PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Two internal channels which are band-gap voltage (VBG) and temperature sensor (VTEMP).
- Supports PDMA transfer mode.

**Note 1:** ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

**Note 2:** If the internal channel (VTEMP) is selected to convert, the sampling rate needs to be less than 300k SPS for accurate result.

## 7 APPLICATION CIRCUIT





## 8 ELECTRICAL CHARACTERISTICS

### 8.1 Absolute Maximum Ratings

| SYMBOL                                    | PARAMETER       | MIN            | MAX            | UNIT |
|-------------------------------------------|-----------------|----------------|----------------|------|
| DC Power Supply                           | $V_{DD}-V_{SS}$ | -0.3           | +7.0           | V    |
| Input Voltage                             | $V_{IN}$        | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | V    |
| Input Voltage on $V_{DDIO}$               | $V_{DDIO}$      | +1.8           | +5.5           | V    |
| Oscillator Frequency                      | $1/t_{CLCL}$    | 4              | 24             | MHz  |
| Operating Temperature                     | $T_A$           | -40            | +105           | °C   |
| Storage Temperature                       | $T_{ST}$        | -55            | +150           | °C   |
| Maximum Current into $V_{DD}$             | $I_{DD}$        | -              | 120            | mA   |
| Maximum Current out of $V_{SS}$           | $I_{SS}$        | -              | 120            | mA   |
| Maximum Current sunk by a I/O Pin         | $I_{IO}$        | -              | 35             | mA   |
| Maximum Current Sourced by a I/O Pin      |                 | -              | 35             | mA   |
| Maximum Current Sunk by Total I/O Pins    |                 | -              | 100            | mA   |
| Maximum Current Sourced by Total I/O Pins |                 | -              | 100            | mA   |

**Note:** Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the life and reliability of the device.

## 8.2 DC Electrical Characteristics

( $V_{DD}-V_{SS} = 2.5 \sim 5.5V$ ,  $T_A = 25^\circ C$ ,  $F_{OSC} = 50$  MHz unless otherwise specified.)

| PARAMETER                                                                                   | SYM.                | SPECIFICATIONS |      |       |      | TEST CONDITIONS                                            |        |        |     |                    |
|---------------------------------------------------------------------------------------------|---------------------|----------------|------|-------|------|------------------------------------------------------------|--------|--------|-----|--------------------|
|                                                                                             |                     | MIN.           | TYP. | MAX.  | UNIT |                                                            |        |        |     |                    |
| Operation Voltage                                                                           | $V_{DD} - V_{SS}$   | 2.5            | -    | 5.5   | V    | $V_{DD} = 2.5 \sim 5.5V$ up to 50 MHz                      |        |        |     |                    |
| Power supply for PB.14, PA.11, PA.10, PB.4 and PB.5                                         | $V_{DDIO} - V_{SS}$ | 1.8            | -    | 5.5   | V    |                                                            |        |        |     |                    |
| Power Ground                                                                                | $V_{SS} - AV_{SS}$  | -0.05          | -    | +0.05 | V    |                                                            |        |        |     |                    |
| LDO Output Voltage                                                                          | $V_{LDO}$           | 1.62           | 1.8  | 1.98  | V    | MCU operating in Run, Idle or Power-down mode              |        |        |     |                    |
|                                                                                             | $C_{LDO}$           | 1              | -    | 1     | uF   | Connect to LDO_CAP pin                                     |        |        |     |                    |
| Band-gap Voltage                                                                            | $V_{BG}$            | -              | 1.21 | -     | V    | $V_{DD} = 2.5 V \sim 5.5 V$ , $T_A = -40 \sim 105^\circ C$ |        |        |     |                    |
| Allowed voltage difference for $V_{DD}$ and $AV_{DD}$                                       | $V_{DD} - AV_{DD}$  | -0.3           | -    | +0.3  | V    |                                                            |        |        |     |                    |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD1}$           | -              | 20.4 | -     | mA   | $V_{DD}$                                                   | HXT    | HIRC   | PLL | All digital module |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | X                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD2}$           | -              | 9.5  | -     | mA   | 3.0 V                                                      | 12 MHz | X      | V   | X                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | X                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD3}$           | -              | 20.0 | -     | mA   | $V_{DD}$                                                   | HXT    | HIRC   | PLL | All digital module |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | X      | 48 MHz | V   | X                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | X      | 48 MHz | V   | V                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD4}$           | -              | 11.5 | -     | mA   | 3.0 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | X      | 48 MHz | V   | X                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD5}$           | -              | 24.6 | -     | mA   | $V_{DD}$                                                   | HXT    | HIRC   | PLL | All digital module |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | X      | 48 MHz | V   | X                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | X      | 48 MHz | V   | V                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD6}$           | -              | 24.1 | -     | mA   | 3.0 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | X      | 48 MHz | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | X      | 48 MHz | V   | X                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD7}$           | -              | 11.4 | -     | mA   | $V_{DD}$                                                   | HXT    | HIRC   | PLL | All digital module |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | X                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD8}$           | -              | 19.5 | -     | mA   | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | X                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD9}$           | -              | 8.8  | -     | mA   | $V_{DD}$                                                   | HXT    | HIRC   | PLL | All digital module |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | X                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD10}$          | -              | 20.0 | -     | mA   | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | X                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD11}$          | -              | 9.1  | -     | mA   | $V_{DD}$                                                   | HXT    | HIRC   | PLL | All digital module |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | X                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD12}$          | -              | 20.0 | -     | mA   | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 3.0 V                                                      | 12 MHz | X      | V   | X                  |
| Operating Current Normal Run Mode HCLK =48 MHz while(1){executed from flash $V_{LDO}=1.8 V$ | $I_{DD13}$          | -              | 20.0 | -     | mA   | $V_{DD}$                                                   | HXT    | HIRC   | PLL | All digital module |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | X                  |
|                                                                                             |                     |                |      |       |      | 5.5 V                                                      | 12 MHz | X      | V   | V                  |

| PARAMETER                                                                                                          | SYM.              | SPECIFICATIONS |      |      |      | TEST CONDITIONS |        |          |     |                       |
|--------------------------------------------------------------------------------------------------------------------|-------------------|----------------|------|------|------|-----------------|--------|----------|-----|-----------------------|
|                                                                                                                    |                   | MIN.           | TYP. | MAX. | UNIT |                 |        |          |     |                       |
| Normal Run Mode<br>HCLK =48 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V                      |                   |                |      |      |      | 5.5 V           | X      | 48 MHz   | X   | V                     |
|                                                                                                                    | I <sub>DD14</sub> | -              | 8.5  | -    | mA   | 5.5 V           | X      | 48 MHz   | X   | X                     |
|                                                                                                                    | I <sub>DD15</sub> | -              | 19.5 | -    | mA   | 3.0 V           | X      | 48 MHz   | X   | V                     |
|                                                                                                                    | I <sub>DD16</sub> | -              | 8.4  | -    | mA   | 3.0 V           | X      | 48 MHz   | X   | X                     |
| Operating Current<br>Normal Run Mode<br>HCLK =24 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>DD17</sub> | -              | 9.7  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                                    |                   |                |      |      |      | 5.5 V           | 24 MHz | X        | X   | V                     |
|                                                                                                                    | I <sub>DD18</sub> | -              | 4.4  | -    | mA   | 5.5 V           | 24 MHz | X        | X   | X                     |
|                                                                                                                    | I <sub>DD19</sub> | -              | 9.5  | -    | mA   | 3.0 V           | 24 MHz | X        | X   | V                     |
|                                                                                                                    | I <sub>DD20</sub> | -              | 4.2  | -    | mA   | 3.0 V           | 24 MHz | X        | X   | X                     |
| Operating Current<br>Normal Run Mode<br>HCLK =24 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>DD21</sub> | -              | 11.1 | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                                    |                   |                |      |      |      | 5.5 V           | X      | 48/2 MHz | X   | V                     |
|                                                                                                                    | I <sub>DD22</sub> | -              | 5.2  | -    | mA   | 5.5 V           | X      | 48/2 MHz | X   | X                     |
|                                                                                                                    | I <sub>DD23</sub> | -              | 10.9 | -    | mA   | 3.0 V           | X      | 48/2 MHz | X   | V                     |
|                                                                                                                    | I <sub>DD24</sub> | -              | 5.1  | -    | mA   | 3.0 V           | X      | 48/2 MHz | X   | X                     |
| Operating Current<br>Normal Run Mode<br>HCLK =16 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>DD25</sub> | -              | 6.4  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                                    |                   |                |      |      |      | 5.5 V           | 16 MHz | X        | X   | V                     |
|                                                                                                                    | I <sub>DD26</sub> | -              | 3.1  | -    | mA   | 5.5 V           | 16 MHz | X        | X   | X                     |
|                                                                                                                    | I <sub>DD27</sub> | -              | 6.3  | -    | mA   | 3.0 V           | 16 MHz | X        | X   | V                     |
|                                                                                                                    | I <sub>DD28</sub> | -              | 3.0  | -    | mA   | 3.0 V           | 16 MHz | X        | X   | X                     |
| Operating Current<br>Normal Run Mode<br>HCLK =16 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>DD29</sub> | -              | 8.3  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                                    |                   |                |      |      |      | 5.5 V           | X      | 48/3 MHz | X   | V                     |
|                                                                                                                    | I <sub>DD30</sub> | -              | 4.2  | -    | mA   | 5.5 V           | X      | 48/3 MHz | X   | X                     |
|                                                                                                                    | I <sub>DD31</sub> | -              | 8.1  | -    | mA   | 3.0 V           | X      | 48/3 MHz | X   | V                     |
|                                                                                                                    | I <sub>DD32</sub> | -              | 4.1  | -    | mA   | 3.0 V           | X      | 48/3 MHz | X   | X                     |
| Operating Current<br>Normal Run Mode<br>HCLK =12 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>DD33</sub> | -              | 4.9  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                                    |                   |                |      |      |      | 5.5 V           | 12 MHz | X        | X   | V                     |
|                                                                                                                    | I <sub>DD34</sub> | -              | 2.2  | -    | mA   | 5.5 V           | 12 MHz | X        | X   | X                     |
|                                                                                                                    | I <sub>DD35</sub> | -              | 4.7  | -    | mA   | 3.0 V           | 12 MHz | X        | X   | V                     |
|                                                                                                                    | I <sub>DD36</sub> | -              | 2.1  | -    | mA   | 3.0 V           | 12 MHz | X        | X   | X                     |
| Operating Current<br>Normal Run Mode                                                                               | I <sub>DD37</sub> | -              | 6.8  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |

| PARAMETER                                                                                                              | SYM.               | SPECIFICATIONS |      |      |      | TEST CONDITIONS |            |           |     |                       |
|------------------------------------------------------------------------------------------------------------------------|--------------------|----------------|------|------|------|-----------------|------------|-----------|-----|-----------------------|
|                                                                                                                        |                    | MIN.           | TYP. | MAX. | UNIT |                 |            |           |     |                       |
| HCLK =12 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V                                             |                    |                |      |      |      | 5.5 V           | X          | 48/4 MHz  | X   | V                     |
|                                                                                                                        | I <sub>DD38</sub>  | -              | 3.7  | -    | mA   | 5.5 V           | X          | 48/4 MHz  | X   | X                     |
|                                                                                                                        | I <sub>DD39</sub>  | -              | 6.6  | -    | mA   | 3.0 V           | X          | 48/4 MHz  | X   | V                     |
|                                                                                                                        | I <sub>DD40</sub>  | -              | 3.6  | -    | mA   | 3.0 V           | X          | 48/4 MHz  | X   | X                     |
| Operating Current<br>Normal Run Mode<br>HCLK =4 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V      | I <sub>DD41</sub>  | -              | 1.8  | -    | mA   | V <sub>DD</sub> | HXT        | HIRC      | PLL | All digital<br>module |
|                                                                                                                        |                    |                |      |      |      | 5.5 V           | 4 MHz      | X         | X   | V                     |
|                                                                                                                        | I <sub>DD42</sub>  | -              | 0.9  | -    | mA   | 5.5 V           | 4 MHz      | X         | X   | X                     |
|                                                                                                                        | I <sub>DD43</sub>  | -              | 1.7  | -    | mA   | 3.0 V           | 4 MHz      | X         | X   | V                     |
| Operating Current<br>Normal Run Mode<br>HCLK =4 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V      | I <sub>DD45</sub>  | -              | 3.9  | -    | mA   | V <sub>DD</sub> | HXT        | HIRC      | PLL | All digital<br>module |
|                                                                                                                        |                    |                |      |      |      | 5.5 V           | X          | 48/12 MHz | X   | V                     |
|                                                                                                                        | I <sub>DD46</sub>  | -              | 2.5  | -    | mA   | 5.5 V           | X          | 48/12 MHz | X   | X                     |
|                                                                                                                        | I <sub>DD47</sub>  | -              | 3.9  | -    | mA   | 3.0 V           | X          | 48/12 MHz | X   | V                     |
| Operating Current<br>Normal Run Mode<br>HCLK =32.768 kHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>DD49</sub>  | -              | 120  | -    | uA   | V <sub>DD</sub> | LXT        | LIRC      | PLL | All digital<br>module |
|                                                                                                                        |                    |                |      |      |      | 5.5 V           | 32.768 kHz | X         | X   | V                     |
|                                                                                                                        | I <sub>DD50</sub>  | -              | 113  | -    | uA   | 5.5 V           | 32.768 kHz | X         | X   | X                     |
|                                                                                                                        | I <sub>DD51</sub>  | -              | 105  | -    | uA   | 3.0 V           | 32.768 kHz | X         | X   | V                     |
| Operating Current<br>Normal Run Mode<br>HCLK =10 kHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V     | I <sub>DD53</sub>  | -              | 111  | -    | uA   | V <sub>DD</sub> | LXT        | LIRC      | PLL | All digital<br>module |
|                                                                                                                        |                    |                |      |      |      | 5.5 V           | X          | 10 kHz    | X   | V                     |
|                                                                                                                        | I <sub>DD54</sub>  | -              | 109  | -    | uA   | 5.5 V           | X          | 10 kHz    | X   | X                     |
|                                                                                                                        | I <sub>DD55</sub>  | -              | 96   | -    | uA   | 3.0 V           | X          | 10 kHz    | X   | V                     |
| Operating Current<br>Idle Mode<br>HCLK =50 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V           | I <sub>IDLE1</sub> | -              | 15.2 | -    | mA   | V <sub>DD</sub> | HXT        | HIRC      | PLL | All digital<br>module |
|                                                                                                                        |                    |                |      |      |      | 5.5 V           | 12 MHz     | X         | V   | V                     |
|                                                                                                                        | I <sub>IDLE2</sub> | -              | 4.4  | -    | mA   | 5.5 V           | 12 MHz     | X         | V   | X                     |
|                                                                                                                        | I <sub>IDLE3</sub> | -              | 14.9 | -    | mA   | 3.0 V           | 12 MHz     | X         | V   | V                     |
| Operating Current<br>Idle Mode                                                                                         | I <sub>IDLE4</sub> | -              | 4.3  | -    | mA   | 3.0 V           | 12 MHz     | X         | V   | X                     |
|                                                                                                                        |                    |                |      |      |      | V <sub>DD</sub> | HXT        | HIRC      | PLL | All digital<br>module |
| Operating Current<br>Idle Mode                                                                                         | I <sub>IDLE5</sub> | -              | 19.3 | -    | mA   | V <sub>DD</sub> | HXT        | HIRC      | PLL | All digital<br>module |

| PARAMETER                                                                                                    | SYM.                | SPECIFICATIONS |      |      |      | TEST CONDITIONS |        |          |     |                       |
|--------------------------------------------------------------------------------------------------------------|---------------------|----------------|------|------|------|-----------------|--------|----------|-----|-----------------------|
|                                                                                                              |                     | MIN.           | TYP. | MAX. | UNIT |                 |        |          |     |                       |
| HCLK =50 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V                                   |                     |                |      |      |      | 5.5 V           | X      | 48 MHz   | V   | V                     |
|                                                                                                              | I <sub>IDLE6</sub>  | -              | 6.8  | -    | mA   | 5.5 V           | X      | 48 MHz   | V   | X                     |
|                                                                                                              | I <sub>IDLE7</sub>  | -              | 19.1 | -    | mA   | 3.0 V           | X      | 48 MHz   | V   | V                     |
|                                                                                                              | I <sub>IDLE8</sub>  | -              | 6.8  | -    | mA   | 3.0 V           | X      | 48 MHz   | V   | X                     |
| Operating Current<br>Idle Mode<br>HCLK =48 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>IDLE9</sub>  | -              | 14.7 | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                              |                     |                |      |      |      | 5.5 V           | 12 MHz | X        | V   | V                     |
|                                                                                                              | I <sub>IDLE10</sub> | -              | 4.3  | -    | mA   | 5.5 V           | 12 MHz | X        | V   | X                     |
|                                                                                                              | I <sub>IDLE11</sub> | -              | 14.3 | -    | mA   | 3.0 V           | 12 MHz | X        | V   | V                     |
| Operating Current<br>Idle Mode<br>HCLK =48 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>IDLE12</sub> | -              | 4.1  | -    | mA   | 3.0 V           | 12 MHz | X        | V   | X                     |
|                                                                                                              |                     |                |      |      |      |                 |        |          |     |                       |
|                                                                                                              | I <sub>IDLE13</sub> | -              | 14.5 | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                              |                     |                |      |      |      | 5.5 V           | X      | 48 MHz   | X   | V                     |
| Operating Current<br>Idle Mode<br>HCLK =48 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>IDLE14</sub> | -              | 3.7  | -    | mA   | 5.5 V           | X      | 48 MHz   | X   | X                     |
|                                                                                                              | I <sub>IDLE15</sub> | -              | 14.2 | -    | mA   | 3.0 V           | X      | 48 MHz   | X   | V                     |
|                                                                                                              | I <sub>IDLE16</sub> | -              | 3.6  | -    | mA   | 3.0 V           | X      | 48 MHz   | X   | X                     |
|                                                                                                              |                     |                |      |      |      |                 |        |          |     |                       |
| Operating Current<br>Idle Mode<br>HCLK =24 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>IDLE17</sub> | -              | 7.2  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                              |                     |                |      |      |      | 5.5 V           | 24 MHz | X        | X   | V                     |
|                                                                                                              | I <sub>IDLE18</sub> | -              | 2.0  | -    | mA   | 5.5 V           | 24 MHz | X        | X   | X                     |
|                                                                                                              | I <sub>IDLE19</sub> | -              | 7.0  | -    | mA   | 3.0 V           | 24 MHz | X        | X   | V                     |
| Operating Current<br>Idle Mode<br>HCLK =24 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>IDLE20</sub> | -              | 1.8  | -    | mA   | 3.0 V           | 24 MHz | X        | X   | X                     |
|                                                                                                              |                     |                |      |      |      |                 |        |          |     |                       |
|                                                                                                              | I <sub>IDLE21</sub> | -              | 8.3  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                              |                     |                |      |      |      | 5.5 V           | X      | 48/2 MHz | X   | V                     |
| Operating Current<br>Idle Mode<br>HCLK =24 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>IDLE22</sub> | -              | 2.8  | -    | mA   | 5.5 V           | X      | 48/2 MHz | X   | X                     |
|                                                                                                              | I <sub>IDLE23</sub> | -              | 8.1  | -    | mA   | 3.0 V           | X      | 48/2 MHz | X   | V                     |
|                                                                                                              | I <sub>IDLE24</sub> | -              | 2.75 | -    | mA   | 3.0 V           | X      | 48/2 MHz | X   | X                     |
|                                                                                                              |                     |                |      |      |      |                 |        |          |     |                       |
| Operating Current<br>Idle Mode<br>HCLK =16 MHz<br>while(1){executed<br>from flash<br>V <sub>LDO</sub> =1.8 V | I <sub>IDLE25</sub> | -              | 4.7  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                              |                     |                |      |      |      | 5.5 V           | 16 MHz | X        | X   | V                     |
|                                                                                                              | I <sub>IDLE26</sub> | -              | 1.3  | -    | mA   | 5.5 V           | 16 MHz | X        | X   | X                     |
|                                                                                                              | I <sub>IDLE27</sub> | -              | 4.6  | -    | mA   | 3.0 V           | 16 MHz | X        | X   | V                     |
| Operating Current<br>Idle Mode<br>HCLK =16 MHz                                                               | I <sub>IDLE28</sub> | -              | 1.2  | -    | mA   | 3.0 V           | 16 MHz | X        | X   | X                     |
|                                                                                                              |                     |                |      |      |      |                 |        |          |     |                       |
| Operating Current<br>Idle Mode<br>HCLK =16 MHz                                                               | I <sub>IDLE29</sub> | -              | 6.3  | -    | mA   | V <sub>DD</sub> | HXT    | HIRC     | PLL | All digital<br>module |
|                                                                                                              |                     |                |      |      |      | 5.5 V           | X      | 48/3 MHz | X   | V                     |

| PARAMETER                                                                                                 | SYM.         | SPECIFICATIONS |      |      |      | TEST CONDITIONS |            |           |     |                    |
|-----------------------------------------------------------------------------------------------------------|--------------|----------------|------|------|------|-----------------|------------|-----------|-----|--------------------|
|                                                                                                           |              | MIN.           | TYP. | MAX. | UNIT |                 |            |           |     |                    |
| while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$                                                    | $I_{IDLE30}$ | -              | 2.6  | -    | mA   | 5.5 V           | X          | 48/3 MHz  | X   | X                  |
|                                                                                                           | $I_{IDLE31}$ | -              | 6.1  | -    | mA   | 3.0 V           | X          | 48/3 MHz  | X   | V                  |
|                                                                                                           | $I_{IDLE32}$ | -              | 2.5  | -    | mA   | 3.0 V           | X          | 48/3 MHz  | X   | X                  |
| Operating Current Idle Mode<br>HCLK =12 MHz<br>while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$     | $I_{IDLE33}$ | -              | 3.6  | -    | mA   | $V_{DD}$        | HXT        | HIRC      | PLL | All digital module |
|                                                                                                           |              |                |      |      |      | 5.5 V           | 12 MHz     | X         | X   | V                  |
|                                                                                                           | $I_{IDLE34}$ | -              | 1.0  | -    | mA   | 5.5 V           | 12 MHz     | X         | X   | X                  |
|                                                                                                           | $I_{IDLE35}$ | -              | 3.5  | -    | mA   | 3.0 V           | 12 MHz     | X         | X   | V                  |
| Operating Current Idle Mode<br>HCLK =12 MHz<br>while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$     | $I_{IDLE37}$ | -              | 5.2  | -    | mA   | $V_{DD}$        | HXT        | HIRC      | PLL | All digital module |
|                                                                                                           |              |                |      |      |      | 5.5 V           | X          | 48/4 MHz  | X   | V                  |
|                                                                                                           | $I_{IDLE38}$ | -              | 2.4  | -    | mA   | 5.5 V           | X          | 48/4 MHz  | X   | X                  |
|                                                                                                           | $I_{IDLE39}$ | -              | 5.1  | -    | mA   | 3.0 V           | X          | 48/4 MHz  | X   | V                  |
| Operating Current Idle Mode<br>HCLK =12 MHz<br>while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$     | $I_{IDLE40}$ | -              | 2.4  | -    | mA   | 3.0 V           | X          | 48/4 MHz  | X   | X                  |
|                                                                                                           |              |                |      |      |      | 3.0 V           | X          | 48/4 MHz  | X   | X                  |
|                                                                                                           | $I_{IDLE41}$ | -              | 1.35 | -    | mA   | $V_{DD}$        | HXT        | HIRC      | PLL | All digital module |
|                                                                                                           |              |                |      |      |      | 5.5 V           | 4 MHz      | X         | X   | V                  |
| Operating Current Idle Mode<br>HCLK =4 MHz<br>while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$      | $I_{IDLE42}$ | -              | 0.48 | -    | mA   | 5.5 V           | 4 MHz      | X         | X   | X                  |
|                                                                                                           | $I_{IDLE43}$ | -              | 1.28 | -    | mA   | 3.0 V           | 4 MHz      | X         | X   | V                  |
|                                                                                                           | $I_{IDLE44}$ | -              | 0.43 | -    | mA   | 3.0 V           | 4 MHz      | X         | X   | X                  |
|                                                                                                           |              |                |      |      |      | 3.0 V           | 4 MHz      | X         | X   | X                  |
| Operating Current Idle Mode<br>HCLK =4 MHz<br>while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$      | $I_{IDLE45}$ | -              | 3.2  | -    | mA   | $V_{DD}$        | HXT        | HIRC      | PLL | All digital module |
|                                                                                                           |              |                |      |      |      | 5.5 V           | X          | 48/12 MHz | X   | V                  |
|                                                                                                           | $I_{IDLE46}$ | -              | 2.2  | -    | mA   | 5.5 V           | X          | 48/12 MHz | X   | X                  |
|                                                                                                           | $I_{IDLE47}$ | -              | 3.1  | -    | mA   | 3.0 V           | X          | 48/12 MHz | X   | V                  |
| Operating Current Idle Mode<br>HCLK =4 MHz<br>while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$      | $I_{IDLE48}$ | -              | 2.1  | -    | mA   | 3.0 V           | X          | 48/12 MHz | X   | X                  |
|                                                                                                           |              |                |      |      |      | 3.0 V           | X          | 48/12 MHz | X   | X                  |
|                                                                                                           | $I_{IDLE49}$ | -              | 116  | -    | uA   | $V_{DD}$        | LXT        | LIRC      | PLL | All digital module |
|                                                                                                           |              |                |      |      |      | 5.5 V           | 32.768 kHz | X         | X   | V                  |
| Operating Current Idle Mode<br>HCLK =32.768 kHz<br>while(1){executed from flash<br>$V_{LDO}=1.8\text{ V}$ | $I_{IDLE50}$ | -              | 110  | -    | uA   | 5.5 V           | 32.768 kHz | X         | X   | X                  |
|                                                                                                           | $I_{IDLE51}$ | -              | 101  | -    | uA   | 3.0 V           | 32.768 kHz | X         | X   | V                  |
|                                                                                                           | $I_{IDLE52}$ | -              | 95   | -    | uA   | 3.0 V           | 32.768 kHz | X         | X   | X                  |
|                                                                                                           |              |                |      |      |      | 3.0 V           | 32.768 kHz | X         | X   | X                  |
| Operating Current Idle Mode<br>HCLK =10 kHz<br>while(1){executed from flash                               | $I_{IDLE53}$ | -              | 109  | -    | uA   | $V_{DD}$        | LXT        | LIRC      | PLL | All digital module |
|                                                                                                           |              |                |      |      |      | 5.5 V           | X          | 10 kHz    | X   | V                  |
|                                                                                                           | $I_{IDLE54}$ | -              | 107  | -    | uA   | 5.5 V           | X          | 10 kHz    | X   | X                  |

| PARAMETER                                                    | SYM.         | SPECIFICATIONS |      |      |               | TEST CONDITIONS |          |            |     |               |
|--------------------------------------------------------------|--------------|----------------|------|------|---------------|-----------------|----------|------------|-----|---------------|
|                                                              |              | MIN.           | TYP. | MAX. | UNIT          |                 |          |            |     |               |
| $V_{LDO}=1.8\text{ V}$                                       | $I_{IDLE55}$ | -              | 95   | -    | $\mu\text{A}$ | 3.0 V           | X        | 10 kHz     | X   | V             |
|                                                              | $I_{IDLE56}$ | -              | 93   | -    | $\mu\text{A}$ | 3.0 V           | X        | 10 kHz     | X   | X             |
| Standby Current<br>Power-down Mode<br>$V_{LDO}=1.8\text{ V}$ | $I_{PWD1}$   | -              | 6.7  | -    | $\mu\text{A}$ | $V_{DD}$        | HXT/HIRC | LXT/LIRC   | PLL | RAM retention |
|                                                              |              |                |      |      |               | 5.5 V           | X        | LXT        | X   | V             |
|                                                              | $I_{PWD2}$   | -              | 6.8  | -    | $\mu\text{A}$ | 5.5 V           | X        | LIRC       | X   | V             |
|                                                              | $I_{PWD3}$   | -              | 7.4  | -    | $\mu\text{A}$ | 5.5 V           | X        | LXT & LIRC | X   | V             |
|                                                              | $I_{PWD4}$   | -              | 6.1  | -    | $\mu\text{A}$ | 5.5 V           | X        | X          | X   | V             |
|                                                              | $I_{PWD5}$   | -              | 5.7  | -    | $\mu\text{A}$ | 3.0 V           | X        | LXT        | X   | V             |
|                                                              | $I_{PWD6}$   | -              | 5.8  | -    | $\mu\text{A}$ | 3.0 V           | X        | LIRC       | X   | V             |
|                                                              | $I_{PWD7}$   | -              | 6.3  | -    | $\mu\text{A}$ | 3.0 V           | X        | LXT & LIRC | X   | V             |
|                                                              | $I_{PWD8}$   | -              | 5.1  | -    | $\mu\text{A}$ | 3.0 V           | X        | X          | X   | V             |

|                                                                           |           |      |      |                |                  |                                                                                         |
|---------------------------------------------------------------------------|-----------|------|------|----------------|------------------|-----------------------------------------------------------------------------------------|
| Input Current at $n\text{RESET}^{[1]}$                                    | $I_{IN}$  | -    | TBD  | -              | $\mu\text{A}$    | $V_{DD} = 3.3\text{V}, V_{IN} = 0.45\text{V}$                                           |
| Logic 0 Input Current (Quasi-bidirectional mode)                          | $I_{IL}$  | -    | -68  | -              | $\mu\text{A}$    | $V_{DD} = V_{DDIO} = 5.5\text{V}, V_{IN} = 0\text{V}$                                   |
| Logic 1 to 0 Transition Current (Quasi-bidirectional mode) <sup>[3]</sup> | $I_{TL}$  | -    | -600 | -              | $\mu\text{A}$    | $V_{DD} = V_{DDIO} = 5.5\text{V}, V_{IN} = 2.0\text{V}$                                 |
| Input Pull Up Resistor                                                    | $R_{IN}$  | -    | 79   | -              | $\text{K}\Omega$ | $V_{DD} = V_{DDIO} = 5.5\text{V}$                                                       |
|                                                                           |           | -    | 143  | -              | $\text{K}\Omega$ | $V_{DD} = V_{DDIO} = 3.3\text{V}$                                                       |
|                                                                           |           | -    | 428  | -              | $\text{K}\Omega$ | $V_{DD} = V_{DDIO} = 1.8\text{V}$                                                       |
| Input Leakage Current                                                     | $I_{LK}$  | -    | 0    | -              | $\mu\text{A}$    | $V_{DD} = V_{DDIO} = 5.5\text{V}, 0 < V_{IN} < V_{DD}$<br>Open-drain or input only mode |
| Input Low Voltage (TTL input)                                             | $V_{IL1}$ | -0.3 | -    | 0.8            | V                | $V_{DD} = V_{DDIO} = 4.5\text{ V}$                                                      |
|                                                                           |           | -0.3 | -    | 0.6            | V                | $V_{DD} = V_{DDIO} = 2.5\text{ V}$                                                      |
| Input Low Voltage (TTL input for $V_{DDIO}$ domain)                       | $V_{IL2}$ | -    | 0.58 | -              | V                | $V_{DD} = 2.5 \sim 5.5\text{ V}$<br>$V_{DDIO} = 1.8\text{ V}$                           |
| Input High Voltage (TTL input)                                            | $V_{IH1}$ | 2.0  | -    | $V_{DD} + 0.3$ | V                | $V_{DD} = V_{DDIO} = 5.5\text{V}$                                                       |
|                                                                           |           | 1.5  | -    | $V_{DD} + 0.3$ | V                | $V_{DD} = V_{DDIO} = 2.5\text{V}$                                                       |

|                                                                              |                  |                      |                    |                         |    |                                                                                 |
|------------------------------------------------------------------------------|------------------|----------------------|--------------------|-------------------------|----|---------------------------------------------------------------------------------|
| Input High Voltage<br>(TTL input for V <sub>DDIO</sub> domain)               | V <sub>IH2</sub> | -                    | 0.64               | -                       | V  | V <sub>DD</sub> = 2.5 ~ 5.5 V<br>V <sub>DDIO</sub> = 1.8 V                      |
| Input Low Voltage<br>(Schmitt input)                                         | V <sub>IL3</sub> | -0.3                 | -                  | 0.3V <sub>DD</sub>      | V  | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.5 ~ 5.5 V                               |
| Input Low Voltage<br>(Schmitt input for V <sub>DDIO</sub> domain)            | V <sub>IL4</sub> | -0.3                 | -                  | 0.3V <sub>DD</sub>      | V  | V <sub>DDIO</sub> = 1.8 ~ 5.5V                                                  |
| Input High Voltage<br>(Schmitt input)                                        | V <sub>IH3</sub> | 0.7V <sub>DD</sub>   | -                  | V <sub>DD</sub> + 0.3   | V  | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.5 ~ 5.5V                                |
| Input Low Voltage<br>(Schmitt input for V <sub>DDIO</sub> domain)            | V <sub>IH4</sub> | 0.7V <sub>DDIO</sub> | -                  | V <sub>DDIO</sub> + 0.3 | V  | V <sub>DDIO</sub> = 1.8 ~ 5.5V                                                  |
| Hysteresis voltage of<br>PA~PF (Schmitt input)                               | V <sub>HY</sub>  | -                    | 0.2V <sub>DD</sub> | -                       | V  |                                                                                 |
| Negative going<br>threshold<br>(Schmitt input),<br>nRESET                    | V <sub>IL5</sub> | -0.3                 | -                  | 0.2V <sub>DD</sub>      | V  |                                                                                 |
| Positive going<br>threshold<br>(Schmitt Input),<br>nRESET                    | V <sub>IH5</sub> | 0.8V <sub>DD</sub>   | -                  | V <sub>DD</sub> + 0.3   | V  |                                                                                 |
| Internal nRESET pin<br>pull up resistor                                      | R <sub>RST</sub> | -                    | 17                 | -                       | KΩ |                                                                                 |
| Source Current<br>(Quasi-bidirectional<br>Mode)                              | I <sub>SR1</sub> | -                    | -390               | -                       | uA | V <sub>DD</sub> = V <sub>DDIO</sub> = 4.5V, V <sub>S</sub> = 2.4V               |
|                                                                              | I <sub>SR2</sub> | -                    | -78                | -                       | uA | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.7V, V <sub>S</sub> = 2.2V               |
|                                                                              | I <sub>SR3</sub> | -                    | -71                | -                       | uA | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.5V, V <sub>S</sub> = 2.0V               |
| Source Current<br>(Quasi-bidirectional<br>Mode for V <sub>DDIO</sub> domain) | I <sub>SR4</sub> | -                    | 21.2               | -                       | uA | V <sub>DD</sub> = 2.5 ~ 5.5V<br>V <sub>DDIO</sub> = 1.8V, V <sub>S</sub> = 1.6V |
| Source Current<br>(Push-pull Mode)                                           | I <sub>SR5</sub> | -                    | -25                | -                       | mA | V <sub>DD</sub> = V <sub>DDIO</sub> = 4.5V, V <sub>S</sub> = 2.4V               |
|                                                                              | I <sub>SR6</sub> | -                    | -5                 | -                       | mA | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.7V, V <sub>S</sub> = 2.2V               |
|                                                                              | I <sub>SR7</sub> | -                    | -4                 | -                       | mA | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.5V, V <sub>S</sub> = 2.0V               |
| Source Current<br>(Push-pull Mode for<br>V <sub>DDIO</sub> domain)           | I <sub>SR8</sub> | -                    | 1.51               | -                       | mA | V <sub>DD</sub> = 2.5 ~ 5.5V<br>V <sub>DDIO</sub> = 1.8V, V <sub>S</sub> = 1.6V |
| Sink Current<br>(Quasi-bidirectional,<br>Open-Drain and Push-                | I <sub>SK1</sub> | -                    | 15                 | -                       | mA | V <sub>DD</sub> = V <sub>DDIO</sub> = 4.5V, V <sub>S</sub> = 0.45V              |
|                                                                              | I <sub>SK2</sub> | -                    | 10                 | -                       | mA | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.7V, V <sub>S</sub> = 0.45V              |

|                                                                                                             |                    |   |       |   |    |                                                                                 |
|-------------------------------------------------------------------------------------------------------------|--------------------|---|-------|---|----|---------------------------------------------------------------------------------|
| pull Mode)                                                                                                  | I <sub>SK3</sub>   | - | 9     | - | mA | V <sub>DD</sub> = V <sub>DDIO</sub> = 2.5V, V <sub>S</sub> = 0.45V              |
| Sink Current<br>(Quasi-bidirectional,<br>Open-Drain and Push-<br>pull Mode for V <sub>DDIO</sub><br>domain) | I <sub>SK4</sub>   | - | 6.51  | - | mA | V <sub>DD</sub> = 2.5 ~ 5.5V<br>V <sub>DDIO</sub> = 1.8V, V <sub>S</sub> = 1.6V |
| Higher GPIO Rising<br>Rate                                                                                  | HIORR <sub>1</sub> | - | 1.76  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 5.5V, without capacitor                   |
| Basic GPIO Rising<br>Rate                                                                                   | BIORR <sub>1</sub> | - | 3.12  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 5.5V, without capacitor                   |
| Higher GPIO Rising<br>Rate                                                                                  | HIORR <sub>2</sub> | - | 3.73  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V, without capacitor                   |
| Basic GPIO Rising<br>Rate                                                                                   | BIORR <sub>2</sub> | - | 5.97  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V, without capacitor                   |
| Higher GPIO Rising<br>Rate<br>(for V <sub>DDIO</sub> domain)                                                | HIORR <sub>3</sub> | - | 25    | - | ns | V <sub>DD</sub> = 2.5 ~ 5.5V, V <sub>DDIO</sub> = 1.8V, without<br>capacitor    |
| Basic GPIO Rising<br>Rate<br>(for V <sub>DDIO</sub> domain)                                                 | BIORR <sub>3</sub> | - | 27    | - | ns | V <sub>DD</sub> = 2.5 ~ 5.5V, V <sub>DDIO</sub> = 1.8V, without<br>capacitor    |
| Higher GPIO Falling<br>Rate                                                                                 | HIOFR <sub>1</sub> | - | 1.53  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 5.5V, without capacitor                   |
| Basic GPIO Falling<br>Rate                                                                                  | BIOFR <sub>1</sub> | - | 3.02  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 5.5V, without capacitor                   |
| Higher GPIO Falling<br>Rate                                                                                 | HIOFR <sub>2</sub> | - | 2.84  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V, without capacitor                   |
| Basic GPIO Falling<br>Rate                                                                                  | BIOFR <sub>2</sub> | - | 6.08  | - | ns | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V, without capacitor                   |
| Higher GPIO Falling<br>Rate<br>(for V <sub>DDIO</sub> domain)                                               | HIOFR <sub>3</sub> | - | 8.69  | - | ns | V <sub>DD</sub> = 2.5 ~ 5.5V, V <sub>DDIO</sub> = 1.8V, without<br>capacitor    |
| Basic GPIO Falling<br>Rate<br>(for V <sub>DDIO</sub> domain)                                                | BIOFR <sub>3</sub> | - | 20.28 | - | ns | V <sub>DD</sub> = 2.5 ~ 5.5V, V <sub>DDIO</sub> = 1.8V, without<br>capacitor    |

**Note:**

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. All pins can source a transition current when they are externally driven from 1 to 0. In the condition of V<sub>DD</sub> = 5.5V, the transition current reaches its maximum value when V<sub>IN</sub> approximates to 2V.
4. For ensuring power stability, a 1uF must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.

## 8.3 AC Electrical Characteristics

### 8.3.1 External 4~24 MHz High Speed Crystal (HXT) Input Clock

| PARAMETER          | SYM.       | SPECIFICATIONS |      |             |      | TEST CONDITION |
|--------------------|------------|----------------|------|-------------|------|----------------|
|                    |            | MIN.           | TYP. | MAX.        | UNIT |                |
| Clock High Time    | $t_{CHCX}$ | 10             | -    | -           | nS   |                |
| Clock Low Time     | $t_{CLCX}$ | 10             | -    | -           | nS   |                |
| Clock Rise Time    | $t_{CLCH}$ | 2              | -    | 15          | nS   |                |
| Clock Fall Time    | $t_{CHCL}$ | 2              | -    | 15          | nS   |                |
| Input High Voltage | $V_{IH}$   | $0.7V_{DD}$    | -    | $V_{DD}$    | V    |                |
| Input Low Voltage  | $V_{IL}$   | 0              | -    | $0.3V_{DD}$ | V    |                |

Note: Duty cycle is 50%.

### 8.3.2 External 4~24 MHz High Speed Crystal (HXT) Oscillator

| PARAMETER            | SYM.      | SPECIFICATIONS |      |      |      | TEST CONDITION           |
|----------------------|-----------|----------------|------|------|------|--------------------------|
|                      |           | MIN.           | TYP. | MAX. | UNIT |                          |
| Oscillator frequency | $f_{HXT}$ | 4              | -    | 24   | MHz  | $V_{DD} = 2.5 \sim 5.5V$ |
| Temperature          | $T_{HXT}$ | -40            | -    | +105 | °C   |                          |
| Operating current    | $I_{HXT}$ | -              | 0.74 | -    | mA   | $V_{DD} = 5.5V @ 12MHz$  |
|                      |           | -              | 0.61 | -    | mA   | $V_{DD} = 3.3V @ 12MHz$  |

#### 8.3.2.1 Typical Crystal Application Circuits

| CRYSTAL       | C1   | C2   | R1      |
|---------------|------|------|---------|
| 4MHz ~ 24 MHz | 20pF | 20pF | without |

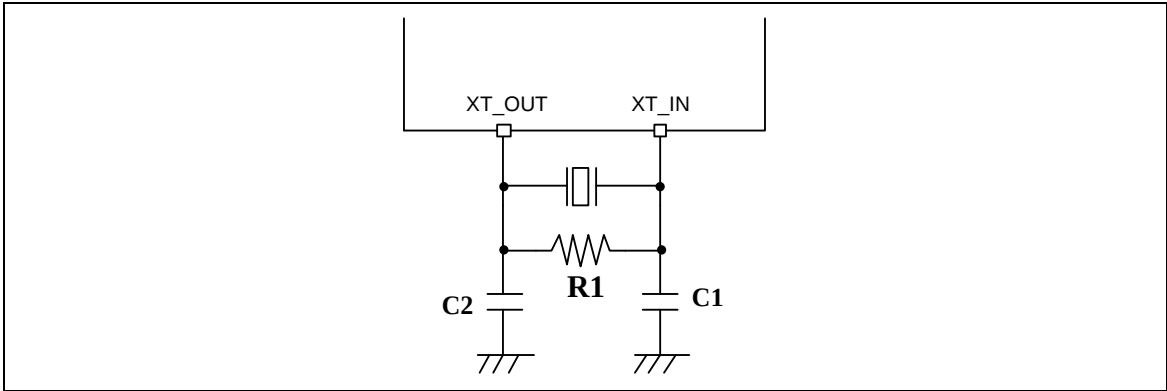


Figure 8.3-1 Typical Crystal Application Circuit

8.3.3 External 32.768 kHz Low Speed Crystal (LXT) Input Clock

| PARAMETER                        | SYM.                | SPECIFICATIONS     |      |                    |      | TEST CONDITION |
|----------------------------------|---------------------|--------------------|------|--------------------|------|----------------|
|                                  |                     | MIN.               | TYP. | MAX.               | UNIT |                |
| Clock High Time                  | t <sub>CHCX</sub>   | TBD                | -    | -                  | nS   |                |
| Clock Low Time                   | t <sub>CLCX</sub>   | TBD                | -    | -                  | nS   |                |
| Clock Rise Time                  | t <sub>CLCH</sub>   | TBD                | -    | TBD                | nS   |                |
| Clock Fall Time                  | t <sub>CHCL</sub>   | TBD                | -    | TBD                | nS   |                |
| LXT Input Pin Input High Voltage | Xin_V <sub>IH</sub> | 0.7V <sub>DD</sub> | -    | V <sub>DD</sub>    | V    |                |
| LXT Input Pin Input Low Voltage  | Xin_V <sub>IL</sub> | 0                  | -    | 0.3V <sub>DD</sub> | V    |                |

Note: Duty cycle is 50%.

8.3.4 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

| PARAMETER | SYM. | SPECIFICATIONS |      |      |      | TEST CONDITION |
|-----------|------|----------------|------|------|------|----------------|
|           |      | MIN.           | TYP. | MAX. | UNIT |                |

| PARAMETER            | SYM.      | SPECIFICATIONS |        |      |      | TEST CONDITION           |
|----------------------|-----------|----------------|--------|------|------|--------------------------|
|                      |           | MIN.           | TYP.   | MAX. | UNIT |                          |
| Oscillator frequency | $f_{LXT}$ | -              | 32.768 | -    | kHz  | $V_{DD} = 2.5 \sim 5.5V$ |
| Temperature          | $T_{LXT}$ | -40            | -      | +105 | °C   |                          |
| Operating current    | $I_{LXT}$ |                | 1.15   |      | μA   | $V_{DD} = 5.5V$          |
|                      |           | -              | 0.58   | -    | μA   | $V_{DD} = 3.3V$          |

#### 8.3.4.1 Typical Crystal Application Circuits

| CRYSTAL    | C3   | C4   | R2      |
|------------|------|------|---------|
| 32.768 kHz | 20pF | 20pF | without |

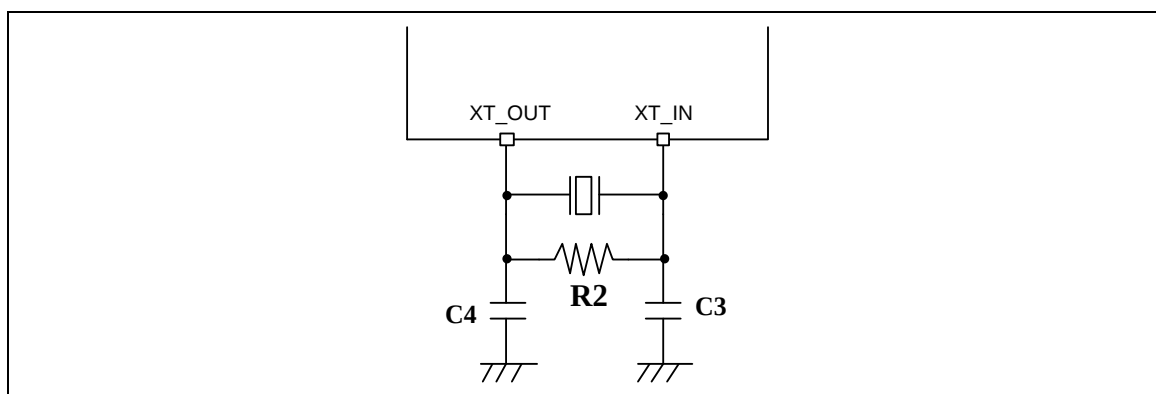


Figure 8.3-2 Typical Crystal Application Circuit

#### 8.3.4.2 Internal 48 MHz High Speed RC Oscillator (HIRC)

| PARAMETER                                | SYM.             | SPECIFICATIONS |      |       |      | TEST CONDITION                                                                                                                      |
|------------------------------------------|------------------|----------------|------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------|
|                                          |                  | MIN.           | TYP. | MAX.  | UNIT |                                                                                                                                     |
| Supply voltage <sup>[1]</sup>            | V <sub>HRC</sub> | 1.62           | 1.8  | 1.98  | V    |                                                                                                                                     |
| Center Frequency                         | f <sub>HRC</sub> | -              | 48   | -     | MHz  | T <sub>A</sub> = 25°C, V <sub>DD</sub> = 3.3V                                                                                       |
| Calibrated Internal Oscillator Frequency |                  | -2             | -    | +2    | %    | -40°C ~ +105°C,<br>V <sub>DD</sub> = 2.5 ~ 5.5V                                                                                     |
|                                          |                  | -0.25          | -    | +0.25 | %    | -40°C ~ +105 °C,<br>V <sub>DD</sub> = 2.5 ~ 5.5V<br><br>Enable 32.768K crystal oscillator or USB SOF, and set SYS_IRCTCTL[1:0]="10" |

| PARAMETER         | SYM.      | SPECIFICATIONS |      |      |         | TEST CONDITION   |
|-------------------|-----------|----------------|------|------|---------|------------------|
|                   |           | MIN.           | TYP. | MAX. | UNIT    |                  |
| Operating current | $I_{HRC}$ | -              | 431  | -    | $\mu A$ | $V_{DD} = 5.5 V$ |
|                   |           | -              | 430  | -    | $\mu A$ | $V_{DD} = 3.3 V$ |

#### 8.3.4.3 Internal 10 kHz Low Speed RC Oscillator (LIRC)

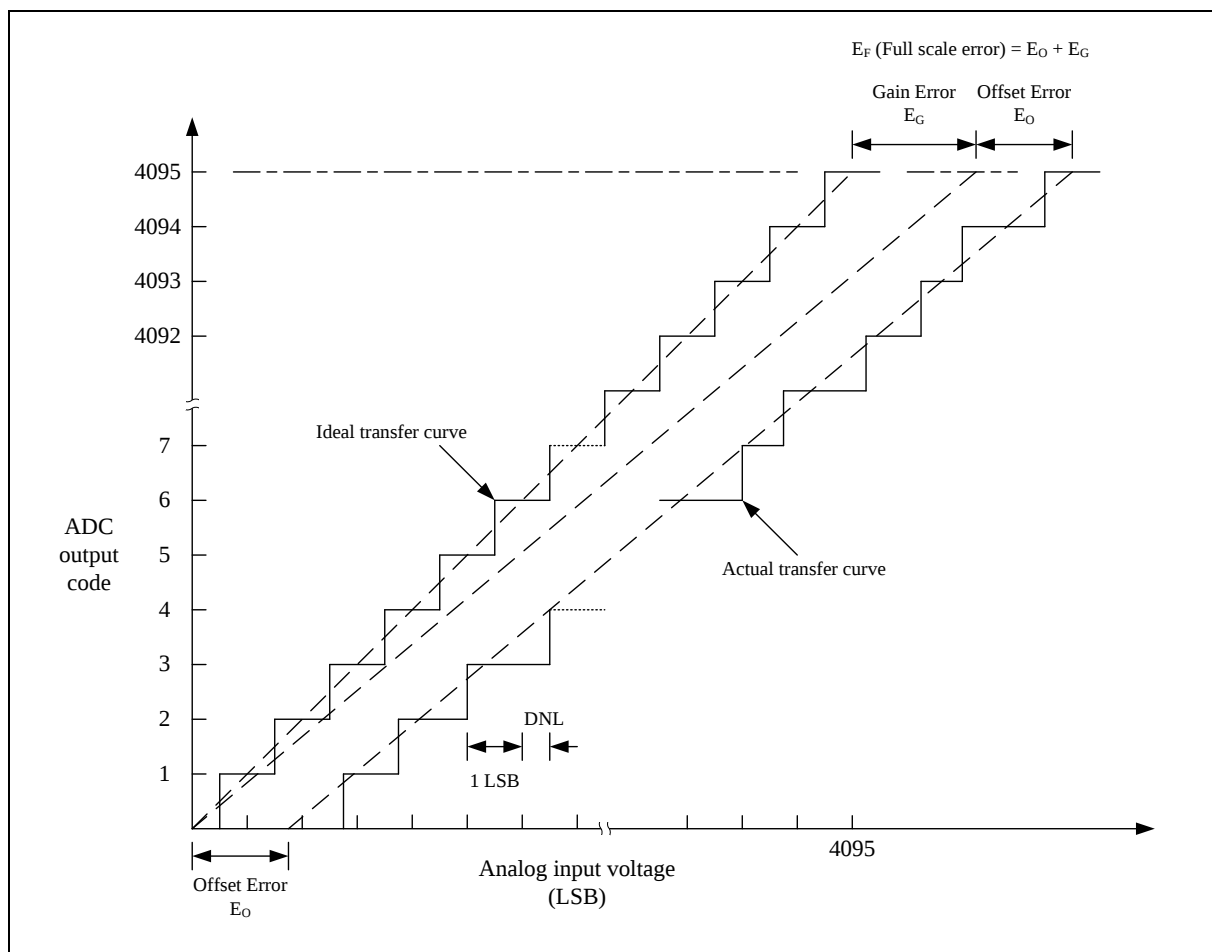
| PARAMETER                                | SYM.             | SPECIFICATIONS |      |      |      | TEST CONDITION                                  |
|------------------------------------------|------------------|----------------|------|------|------|-------------------------------------------------|
|                                          |                  | MIN.           | TYP. | MAX. | UNIT |                                                 |
| Supply voltage <sup>[1]</sup>            | V <sub>LRC</sub> | 1.62           | 1.8  | 1.98 | V    |                                                 |
| Center Frequency                         | F <sub>LRC</sub> | -              | 10   | -    | kHz  | 25°C, V <sub>DD</sub> = 3.3V                    |
| Calibrated Internal Oscillator Frequency |                  | -30            | -    | +30  | %    | 25 °C,<br>V <sub>DD</sub> = 2.5 ~ 5.5V          |
|                                          |                  | -50            | -    | +50  | %    | -40°C ~+105 °C,<br>V <sub>DD</sub> = 2.5 ~ 5.5V |
| Operating current                        | I <sub>LRC</sub> | -              | 0.74 | -    | μA   | V <sub>DD</sub> = 5.5V                          |
|                                          |                  |                | 0.66 |      | μA   | V <sub>DD</sub> = 3.3V                          |

**Note:** Internal oscillator operation voltage comes from LDO.

## 8.4 Analog Characteristics

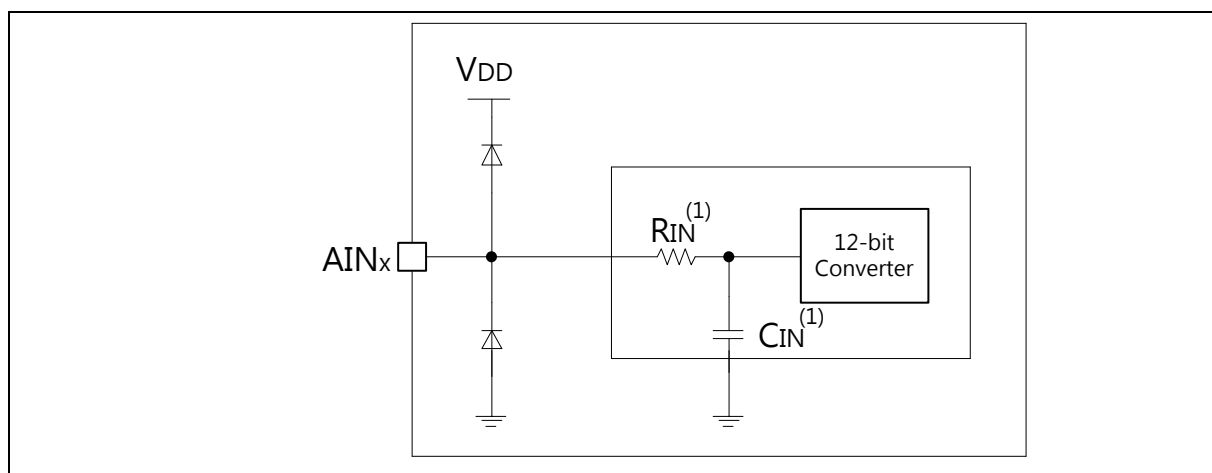
### 8.4.1 12-bit ADC

| PARAMETER                                         | SYM.         | SPECIFICATIONS |           |           |             | TEST CONDITION                                                |
|---------------------------------------------------|--------------|----------------|-----------|-----------|-------------|---------------------------------------------------------------|
|                                                   |              | MIN.           | TYP.      | MAX.      | UNIT        |                                                               |
| Operating voltage                                 | $AV_{DD}$    | 3.0            | -         | 5.5       | V           | $AV_{DD} = V_{DD}$                                            |
| Operating current ( $AV_{DD}$ current)            | $I_{ADC1}$   | -              | 2.72      | -         | mA          | $AV_{DD} = V_{DD} = 4.5V$<br>ADC Clock Rate = 16 MHz          |
| (Enable ADC and disable all other analog modules) | $I_{ADC2}$   |                |           |           | $\mu A$     | $AV_{DD} = V_{DD} = 2.5V$<br>ADC Clock Rate = 6 MHz           |
| Resolution                                        | $R_{ADC}$    | -              | -         | 12        | Bit         |                                                               |
| Reference voltage                                 | $V_{REF}$    | -              | $AV_{DD}$ | -         | V           | $AV_{DD} = 5V$                                                |
| ADC input voltage                                 | $V_{IN}$     | 0              | -         | $AV_{DD}$ | V           |                                                               |
| ADC Clock frequency                               | $F_{ADC}$    | -              | -         | 16        | MHz         | $AV_{DD} = 5V$                                                |
|                                                   |              | -              | -         | 8         | MHz         | $AV_{DD} = 3V$                                                |
| Acquisition Time (Sample Stage)                   | $T_{ACQ}$    | 2              | 7         | 21        | $1/F_{ADC}$ | Default: 7 ( $1/F_{ADC}$ )                                    |
| Conversion time                                   | $T_{CONV}$   | 15             | 20        | 34        | $1/F_{ADC}$ | $T_{CONV} = T_{ACQ} + 13$<br>Default: 20 ( $1/F_{ADC}$ )      |
| Conversion Rate<br>( $F_{ADC}/T_{CONV}$ )         | $F_{SPS}$    | -              | -         | 800       | kSPS        | $AV_{DD} = 5V$<br>$T_{CONV} = 20$ clock<br>$F_{ADC} = 16$ MHz |
|                                                   |              | -              | -         | 300       | kSPS        | $AV_{DD} = 3V$<br>$T_{CONV} = 20$ clock<br>$F_{ADC} = 6$ MHz  |
| Integral Non-Linearity Error                      | INL          | +1.6           | -         | +2.1      | LSB         |                                                               |
| Differential Non-Linearity                        | DNL          | -1             | -         | -1.5      | LSB         |                                                               |
| Gain error                                        | $E_G$        | -3.4           | -         | -4.7      | LSB         |                                                               |
| Offset error                                      | $E_{OFFSET}$ | +2.2           | -         | +3.6      | LSB         |                                                               |
| Absolute error                                    | $E_{ABS}$    | +3.1           | -         | +4.7      | LSB         |                                                               |
| Internal Capacitance                              | $C_{IN}$     | -              | 3.2       | -         | pF          |                                                               |
| Input Load                                        | $R_{IN}$     | -              | 6         | -         | k $\Omega$  |                                                               |
| Monotonic                                         | -            | Guaranteed     |           |           | -           |                                                               |



**Note:** The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

Typical connection diagram using the ADC



**Note:**  $GND < AIN_x < V_{DD}$

### 8.4.2 LDO

| Symbol           | Parameter       | Min  | Typ | Max  | Unit | Test Condition |
|------------------|-----------------|------|-----|------|------|----------------|
| V <sub>DD</sub>  | DC Power Supply | 2.5  | -   | 5.5  | V    |                |
| V <sub>LDO</sub> | Output Voltage  | 1.62 | 1.8 | 1.98 | V    |                |
| T <sub>A</sub>   | Temperature     | -40  | 25  | +105 | °C   |                |

**Note 1:** It is recommended a 0.1μF bypass capacitor is connected between V<sub>DD</sub> and the closest V<sub>SS</sub> pin of the device.

**Note 2:** For ensuring power stability, a 1μF Capacitor must be connected between LDO\_CAP pin and the closest V<sub>SS</sub> pin of the device.

### 8.4.3 Low-Voltage Reset

| Symbol                 | Parameter         | Min | Typ | Max  | Unit | Test Condition          |
|------------------------|-------------------|-----|-----|------|------|-------------------------|
| AV <sub>DD</sub>       | Supply Voltage    | 0   | -   | 5.5  | V    |                         |
| T <sub>A</sub>         | Temperature       | -40 | -   | +105 | °C   | -                       |
| I <sub>LVR</sub>       | Quiescent Current | -   | 1.1 | -    | uA   | AV <sub>DD</sub> = 5.5V |
| V <sub>POR</sub>       | Threshold Voltage | 2.1 | 2.2 | 2.3  | V    | T <sub>A</sub> = 85°C   |
|                        |                   | 2.0 | 2.1 | 2.2  | V    | T <sub>A</sub> = 25°C   |
|                        |                   | 1.9 | 2.0 | 2.1  | V    | T <sub>A</sub> = -40°C  |
| T <sub>LVR_Start</sub> | Start-up Time     | -   | 129 | -    | uS   |                         |

### 8.4.4 Brown-out Detector

| Symbol           | Parameter                           | Min  | Typ | Max  | Unit | Test Condition          |
|------------------|-------------------------------------|------|-----|------|------|-------------------------|
| AV <sub>DD</sub> | Supply Voltage                      | 0    | -   | 5.5  | V    | -                       |
| T <sub>A</sub>   | Temperature                         | -40  | -   | +105 | °C   | -                       |
| I <sub>BOD</sub> | Quiescent Current                   | -    | 81  | -    | μA   | AV <sub>DD</sub> = 5.5V |
| VBOD             | Brown-out Voltage<br>(Falling edge) | 4.3  | 4.5 | 4.7  | V    | BODVL [1:0] = 11        |
|                  |                                     | 3.5  | 3.7 | 3.9  | V    | BODVL [1:0] = 10        |
|                  |                                     | 2.55 | 2.7 | 2.85 | V    | BODVL [1:0] = 01        |
|                  |                                     | 2.05 | 2.2 | 2.35 | V    | BODVL [1:0] = 00        |
| VBOD             | Brown-out Voltage                   | 4.3  | 4.6 | 4.7  | V    | BODVL [1:0] = 11        |

|                        |               |     |      |     |    |                  |
|------------------------|---------------|-----|------|-----|----|------------------|
|                        | (Rising edge) | 3.6 | 3.8  | 4.0 | V  | BODVL [1:0] = 10 |
|                        |               | 2.6 | 2.75 | 2.9 | V  | BODVL [1:0] = 01 |
|                        |               | 2.1 | 2.25 | 2.4 | V  | BODVL [1:0] = 00 |
| T <sub>BOD_Start</sub> | Start-up Time | -   | 1060 | -   | uS |                  |

#### 8.4.5 Power-on Reset

| Symbol           | Parameter                 | Min | Typ  | Max  | Unit | Test Condition |
|------------------|---------------------------|-----|------|------|------|----------------|
| T <sub>A</sub>   | Temperature               | -40 | -    | +105 | °C   | -              |
| V <sub>POR</sub> | Threshold Voltage         | 1.5 | 2    | 2.2  | V    | -              |
| V <sub>HYS</sub> | Power Drop Detect Voltage |     | 1.78 |      | V    |                |

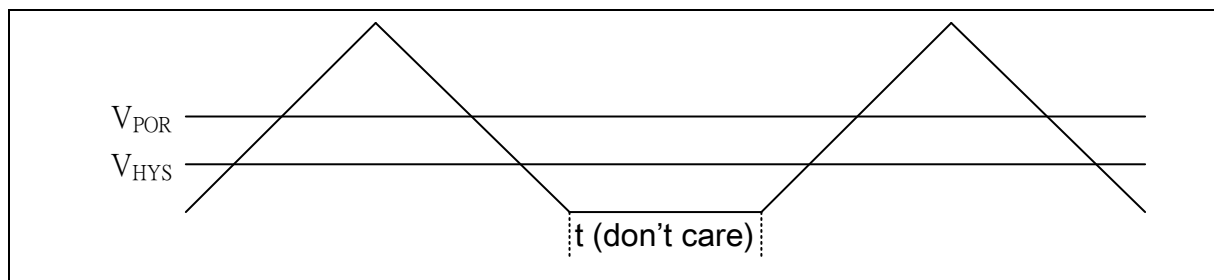


Figure 8.4-1 Power-up Ramp Condition

#### 8.4.6 Temperature Sensor

| PARAMETER             | SYM.              | SPECIFICATIONS |       |       |       | TEST CONDITION<br>(supply voltage = 3V) |
|-----------------------|-------------------|----------------|-------|-------|-------|-----------------------------------------|
|                       |                   | MIN.           | TYP.  | MAX.  | UNIT  |                                         |
| Detection Temperature | T <sub>DET</sub>  | -40            | -     | +105  | °C    |                                         |
| Operating current     | I <sub>TEMP</sub> | 6.4            | -     | 10.5  | μA    |                                         |
| Gain                  | V <sub>TG</sub>   | -1.8           | -1.76 | -1.73 | mV/°C |                                         |
| Offset                | V <sub>TO</sub>   | -              | 725   | -     | mV    | Temperature at 0 °C                     |

**Note 1:** Internal operation voltage comes from LDO.

**Note 2:** The temperature sensor formula for the output voltage (Vtemp) is as below equation.

$$V_{temp} \text{ (mV)} = \text{Gain (mV/°C)} \times \text{Temperature (°C)} + \text{Offset (mV)}$$

## 8.4.7 USB PHY

### 8.4.7.1 Low-full-Speed DC Electrical Specifications

| Symbol    | Parameter                                          | Min.  | Typ. | Max.  | Unit       | Test Conditions         |
|-----------|----------------------------------------------------|-------|------|-------|------------|-------------------------|
| $V_{IH}$  | Input High (driven)                                | 2.0   | -    | -     | V          | -                       |
| $V_{IL}$  | Input Low                                          | -     | -    | 0.8   | V          | -                       |
| $V_{DI}$  | Differential Input Sensitivity                     | 0.2   | -    | -     | V          | PADP-PADM               |
| $V_{CM}$  | Differential Common-mode Range                     | 0.8   | -    | 2.5   | V          | Includes $V_{DI}$ range |
| $V_{SE}$  | Single-ended Receiver Threshold                    | 0.8   | -    | 2.0   | V          | -                       |
|           | Receiver Hysteresis                                | -     | 200  | -     | mV         | -                       |
| $V_{OL}$  | Output Low (driven)                                | 0     | -    | 0.3   | V          | -                       |
| $V_{OH}$  | Output High (driven)                               | 2.8   | -    | 3.6   | V          | -                       |
| $V_{CRS}$ | Output Signal Cross Voltage                        | 1.3   | -    | 2.0   | V          | -                       |
| $R_{PU}$  | Pull-up Resistor                                   | 1.425 | -    | 1.575 | k $\Omega$ | -                       |
| $R_{PD}$  | Pull-down Resistor                                 | 14.25 | -    | 15.75 | k $\Omega$ | -                       |
| $V_{TRM}$ | TERMINATION Voltage for Uptream port pull up (RPU) | 3.0   | -    | 3.6   | V          | -                       |
| $Z_{DRV}$ | Driver Output Resistance                           | -     | 10   | -     | $\Omega$   | Steady state drive*     |
| $C_{IN}$  | Transceiver Capacitance                            | -     | -    | 20    | pF         | Pin to GND              |

\*Driver output resistance doesn't include series resistor resistance.

### 8.4.7.2 USB Full-Speed Driver Electrical Characteristics

| Symbol     | Parameter                   | Min. | Typ. | Max.   | Unit | Test Conditions          |
|------------|-----------------------------|------|------|--------|------|--------------------------|
| $T_{FR}$   | Rise Time                   | 4    | -    | 20     | ns   | $C_L=50p$                |
| $T_{FF}$   | Fall Time                   | 4    | -    | 20     | ns   | $C_L=50p$                |
| $T_{FRFF}$ | Rise and Fall Time Matching | 90   | -    | 111.11 | %    | $T_{FRFF}=T_{FR}/T_{FF}$ |

### 8.4.7.3 USB LDO Specification

| Symbol     | Parameter                   | Min. | Typ. | Max. | Unit    | Test Conditions |
|------------|-----------------------------|------|------|------|---------|-----------------|
| $V_{BUS}$  | $V_{BUS}$ Pin Input Voltage | 4.0  | 5.0  | 5.5  | V       | -               |
| $V_{DD33}$ | LDO Output Voltage          | 3.0  | 3.3  | 3.6  | V       | -               |
| $C_{bp}$   | External Bypass Capacitor   | -    | 1.0  | -    | $\mu F$ | -               |

## 8.5 Flash DC Electrical Characteris

| Symbol          | Parameter       | Min    | Typ | Max  | Unit                  | Test Condition             |
|-----------------|-----------------|--------|-----|------|-----------------------|----------------------------|
| $V_{FLA}^{[1]}$ | Supply Voltage  | 1.62   | 1.8 | 1.98 | V                     | $T_A = 25^{\circ}\text{C}$ |
| $N_{ENDUR}$     | Endurance       | 20,000 | -   | -    | cycles <sup>[2]</sup> |                            |
| $T_{RET}$       | Data Retention  | 100    | -   | -    | year                  |                            |
| $T_{ERASE}$     | Page Erase Time | 20     | -   | 40   | mS                    |                            |
| $T_{MER}$       | Mass Erase Time | 20     | -   | 40   | mS                    |                            |
| $T_{PROG}$      | Program Time    | 20     | -   | 40   | uS                    |                            |
| $I_{DD1}$       | Read Current    | -      | -   | TBD  | mA                    |                            |
| $I_{DD2}$       | Program Current | -      | -   | TBD  | mA                    |                            |
| $I_{DD3}$       | Erase Current   | -      | -   | TBD  | uA                    |                            |

**Note 1:**  $V_{FLA}$  is source from chip LDO output voltage.

**Note 2:** Number of program/erase cycles.

**Note 3:** This table is guaranteed by design, not test in production.

## 8.6 I<sup>2</sup>C Dynamic Characteristics

| Symbol         | Parameter                           | Standard Mode <sup>[1][2]</sup> |                     | Fast Mode <sup>[1][2]</sup> |                    | Unit |
|----------------|-------------------------------------|---------------------------------|---------------------|-----------------------------|--------------------|------|
|                |                                     | Min.                            | Max.                | Min.                        | Max.               |      |
| $t_{LOW}$      | SCL low period                      | 4.7                             | -                   | 1.2                         | -                  | μs   |
| $t_{HIGH}$     | SCL high period                     | 4                               | -                   | 0.6                         | -                  | μs   |
| $t_{SU, STA}$  | Repeated START condition setup time | 4.7                             | -                   | 1.2                         | -                  | μs   |
| $t_{HD, STA}$  | START condition hold time           | 4                               | -                   | 0.6                         | -                  | μs   |
| $t_{SU, STO}$  | STOP condition setup time           | 4                               | -                   | 0.6                         | -                  | μs   |
| $t_{BUF}$      | Bus free time                       | 4.7 <sup>[3]</sup>              | -                   | 1.2 <sup>[3]</sup>          | -                  | μs   |
| $t_{SU, DAT}$  | Data setup time                     | 250                             | -                   | 100                         | -                  | ns   |
| $t_{HD, DAT}$  | Data hold time                      | 0 <sup>[4]</sup>                | 3.45 <sup>[5]</sup> | 0 <sup>[4]</sup>            | 0.8 <sup>[5]</sup> | μs   |
| $t_r$          | SCL/SDA rise time                   | -                               | 1000                | 20+0.1C <sub>b</sub>        | 300                | ns   |
| $t_f$          | SCL/SDA fall time                   | -                               | 300                 | -                           | 300                | ns   |
| C <sub>b</sub> | Capacitive load for each bus line   | -                               | 400                 | -                           | 400                | pF   |

### Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I<sup>2</sup>C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I<sup>2</sup>C frequency.
3. I<sup>2</sup>C controller must be retrigged immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

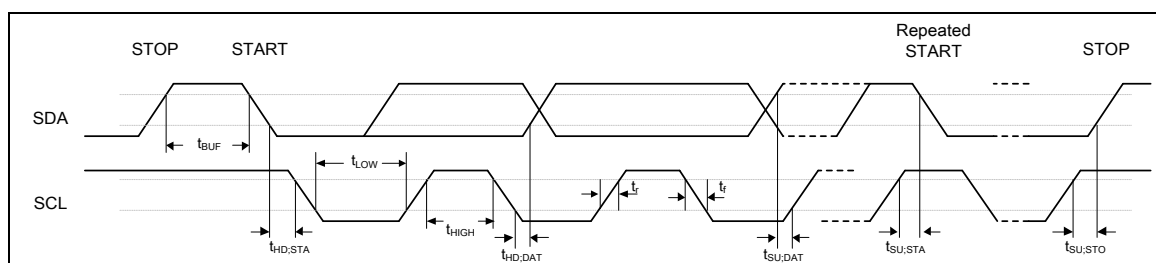


Figure 8.6-1 I<sup>2</sup>C Timing Diagram

## 8.7 SPI Dynamic Characteristics

### 8.7.1 Dynamic Characteristics of Data Input and Output Pin

| SYMBOL                                                             | PARAMETER              | MIN. | TYP. | MAX. | UNIT |
|--------------------------------------------------------------------|------------------------|------|------|------|------|
| <b>SPI MASTER MODE (VDD = 4.5 V~5.5V, 30 PF LOADING CAPACITOR)</b> |                        |      |      |      |      |
| $t_{DS}$                                                           | Data setup time        | 4    | 2    | -    | ns   |
| $t_{DH}$                                                           | Data hold time         | 0    | -    | -    | ns   |
| $t_V$                                                              | Data output valid time | -    | 7    | 11   | ns   |
| <b>SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)</b>  |                        |      |      |      |      |
| $t_{DS}$                                                           | Data setup time        | 5    | 3    | -    | ns   |
| $t_{DH}$                                                           | Data hold time         | 0    | -    | -    | ns   |
| $t_V$                                                              | Data output valid time | -    | 13   | 18   | ns   |

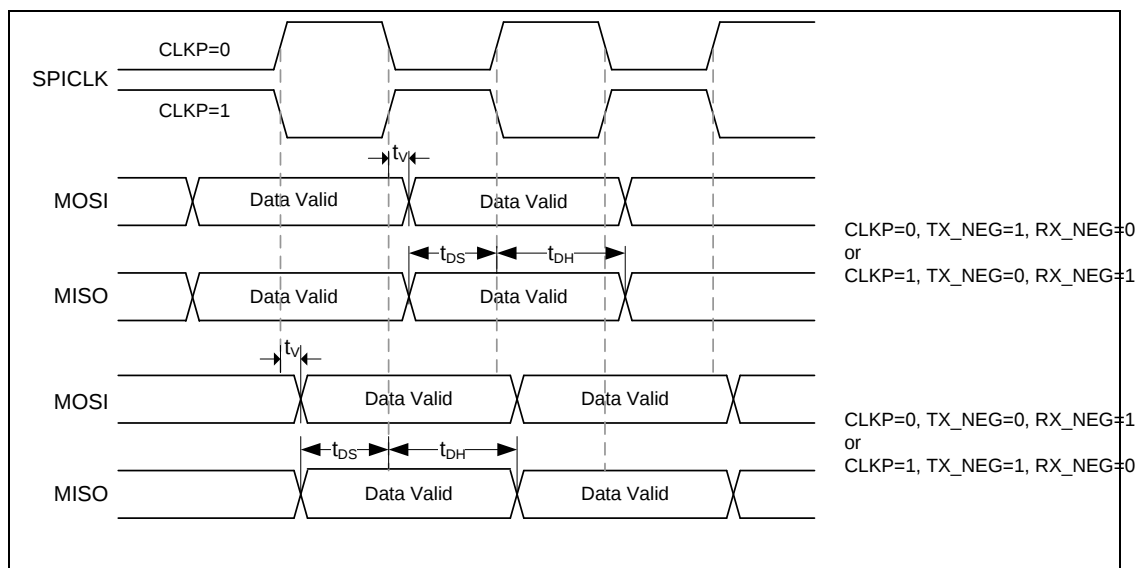


Figure 8.7-1 SPI Master Mode Timing Diagram

| SYMBOL                                                               | PARAMETER              | MIN.               | TYP.                | MAX.                | UNIT |
|----------------------------------------------------------------------|------------------------|--------------------|---------------------|---------------------|------|
| <b>SPI SLAVE MODE (VDD = 4.5 V~5.5V, 30 PF LOADING CAPACITOR)</b>    |                        |                    |                     |                     |      |
| $t_{DS}$                                                             | Data setup time        | 0                  | -                   | -                   | ns   |
| $t_{DH}$                                                             | Data hold time         | $2 \cdot PCLK + 4$ | -                   | -                   | ns   |
| $t_V$                                                                | Data output valid time | -                  | $2 \cdot PCLK + 11$ | $2 \cdot PCLK + 19$ | ns   |
| <b>SPI SLAVE MODE (VDD = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)</b> |                        |                    |                     |                     |      |

|          |                        |                    |                     |                     |    |
|----------|------------------------|--------------------|---------------------|---------------------|----|
| $t_{DS}$ | Data setup time        | 0                  | -                   | -                   | ns |
| $t_{DH}$ | Data hold time         | $2 \cdot PCLK + 6$ | -                   | -                   | ns |
| $t_V$    | Data output valid time | -                  | $2 \cdot PCLK + 19$ | $2 \cdot PCLK + 25$ | ns |

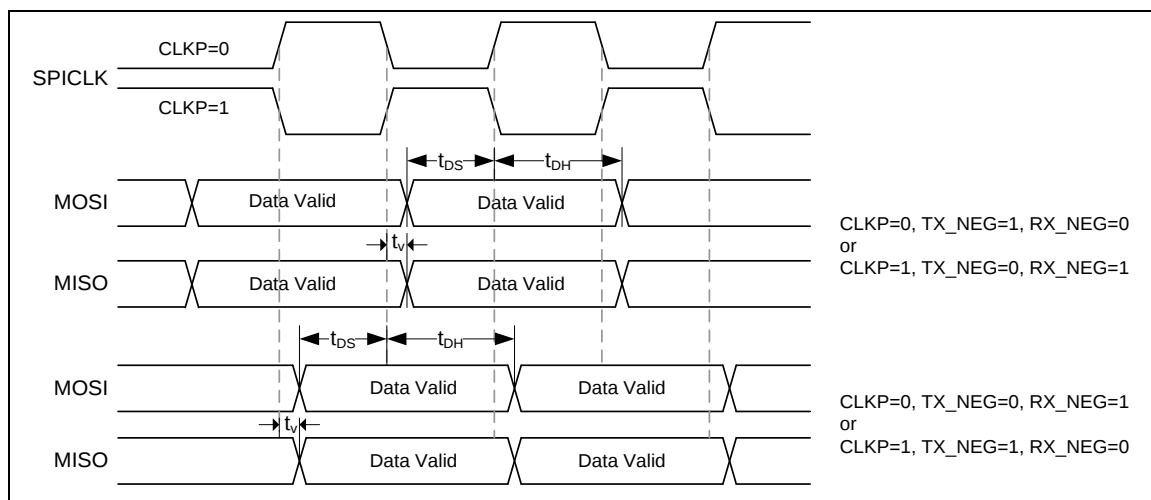
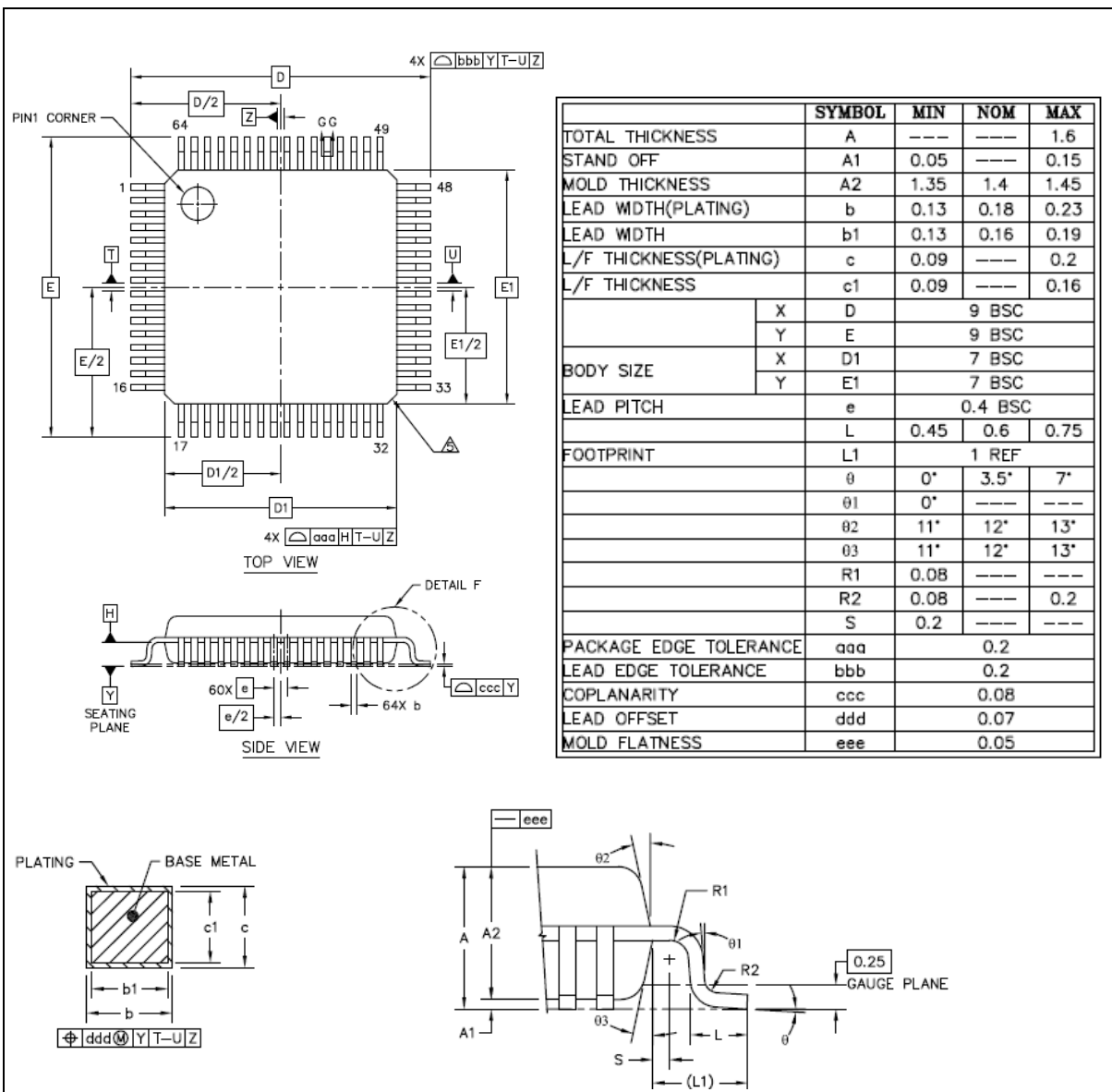


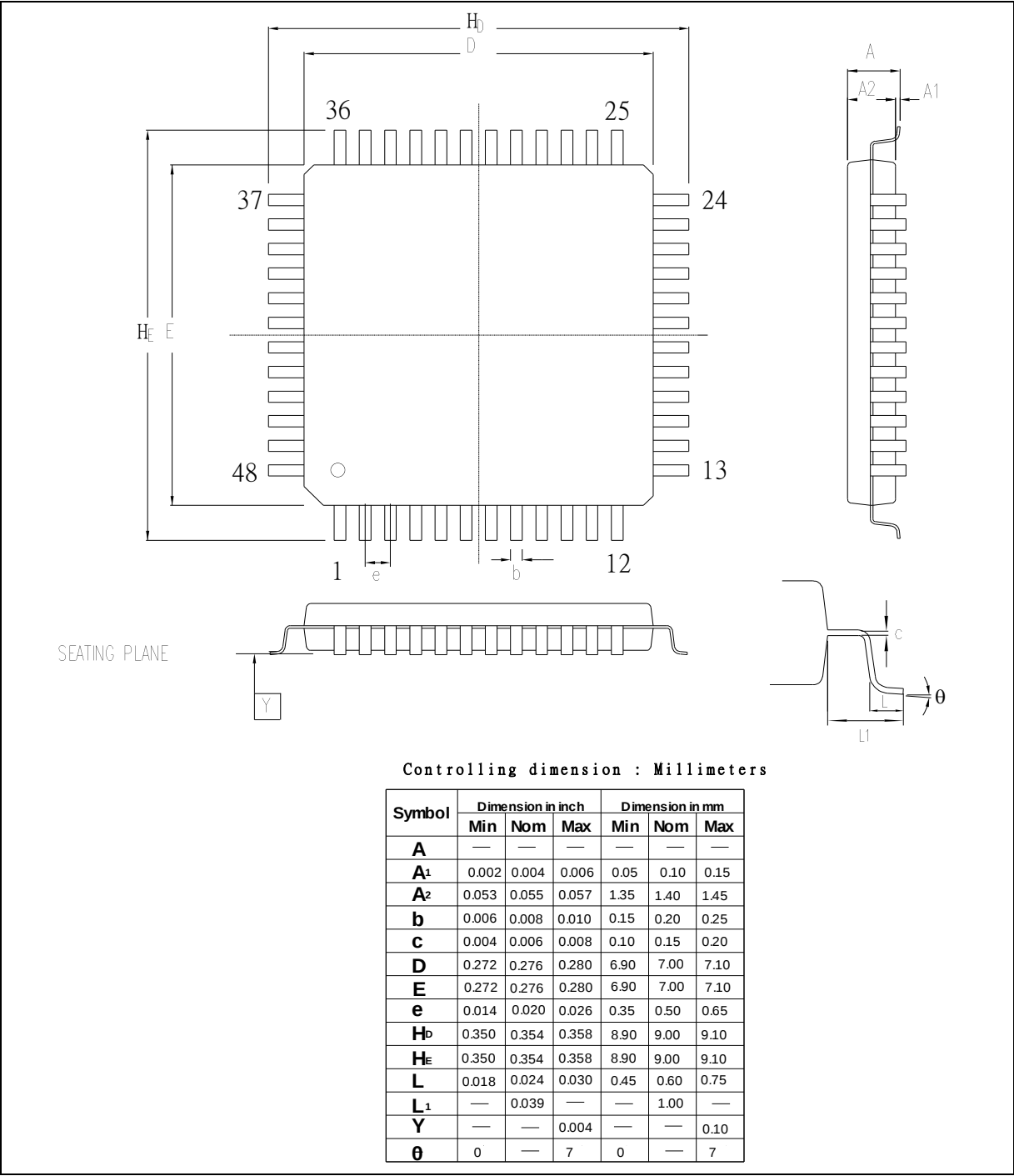
Figure 8.7-2 SPI Slave Mode Timing Diagram

## 9 PACKAGE DIMENSIONS

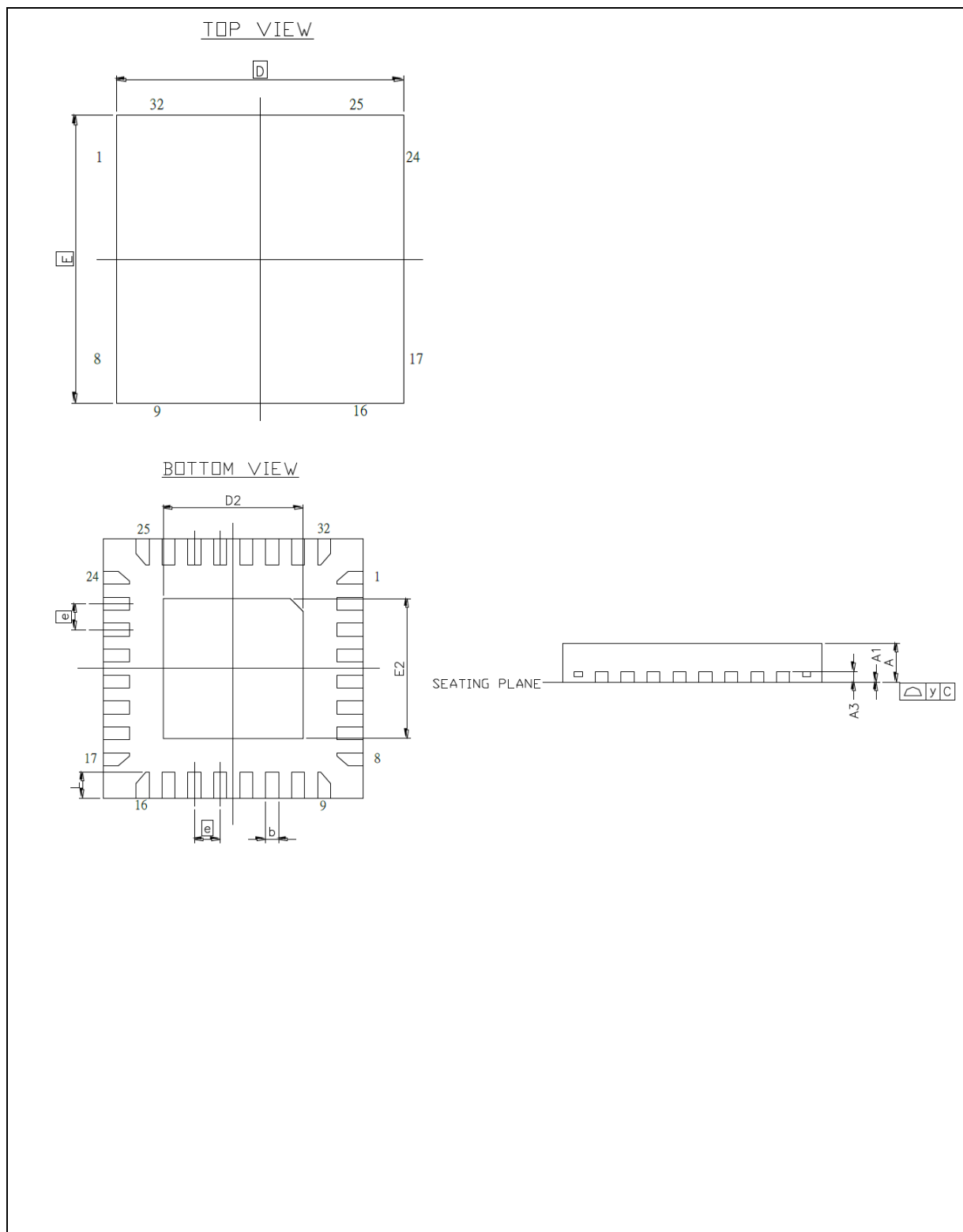
### 9.1 LQFP 64S (7x7x1.4 mm)



9.2 LQFP 48L (7x7x1.4 mm)



### 9.3 QFN 33Z (5x5x0.8 mm)



| SYMBOL | DIMENSION<br>(MM) |      |      | DIMENSION<br>(INCH) |        |        |
|--------|-------------------|------|------|---------------------|--------|--------|
|        | MIN.              | NOM. | MAX. | MIN.                | NOM.   | MAX.   |
| A      | 0.70              | 0.75 | 0.80 | 0.0275              | 0.0295 | 0.0315 |
| A1     | 0                 | 0.02 | 0.05 | 0                   | 0.001  | 0.002  |
| A3     | 0.20 REF          |      |      | 0.008 REF           |        |        |
| b      | 0.18              | 0.25 | 0.30 | 0.007               | 0.010  | 0.012  |
| D      | 5.00 BSC          |      |      | 0.197 BSC           |        |        |
| E      | 5.00 BSC          |      |      | 0.197 BSC           |        |        |
| e      | 0.50 BSC          |      |      | 0.0197 BSC          |        |        |
| L      | 0.30              | 0.40 | 0.50 | 0.012               | 0.016  | 0.020  |
| y      | 0.10              |      |      | 0.0039              |        |        |
| D2     | 3.20              | 3.40 | 3.60 | 0.124               | 0.138  | 0.142  |
| E2     | 3.20              | 3.40 | 3.60 | 0.124               | 0.138  | 0.142  |

**10 REVISION HISTORY**

| Revision | Date       | Description         |
|----------|------------|---------------------|
| 1.00     | 2017.02.15 | Preliminary version |

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