NuMicro® Family

Arm® Cortex®-M23-based Microcontroller

NUC1263 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro NUC1263 series 32-bit microcontroller is based on Arm Cortex-M23 core for Armv8-M architecture with LED Light Strip Interface (LLSI) and USB2.0 full-speed device using built-in 48 MHz oscillator to support the communication with PC and Mobile accessories. It runs up to 72 MHz and features 64 Kbytes of Flash, 20 Kbytes of SRAM, 2.5V ~ 5.5V wide operating voltage, and -40°C ~ +105°C operating temperature.

The NUC1263 series has 6 channels of LED Light Strip Interface (LLSI) which is easy to control the LED light strip, up to 24 channels of high-speed PWM with clock frequency up to 144 MHz for precision control.

The NUC1263 series supports USB 2.0 full-speed device interfaces without external crystal oscillators, and USB commands can be used for light control. In addition, the NUC1263 series has a built-in 2 Kbytes of SPROM (Security Protection ROM), which provides an independent security encryption area to protect the intellectual property rights of developers. The NUC1263 series can be widely used in industrial control, lighting control, keyboard/mouse, and home appliances related applications.

The NUC1263 series is equipped with plenty of peripherals supporting up to 6 channels of LED Light Strip Interface (LLSI), up to 24 channels of 16-bit PWM, up to 2 channels I3C and USB 2.0 full-speed devices without external crystal oscillators. The NUC1263 series also equipped with Timers, Watchdog Timers, up to 10 channels of PDMA, 3 sets of UART, 3 sets of I²C, 3 sets of SPI/ I²S, making it highly suitable for connecting comprehensive external modules. It also integrates high performance analog circuit, such as 16 channels of 12-bit 800 kSPS ADC, and supports high anti-interference capability 8 kV ESD (HBM)/ 4.4 kV EFT (LQFP64) and 4 kV ESD (HBM)/ 4.4 kV EFT (QFN33).

Supported packages include QFN33 (5 mm x 5 mm), QFN48 (7 mm x 7 mm), LQFP48 (7 mm x 7 mm), and LQFP64 (7 mm x 7 mm), which are pin-compatible to other Nuvoton series to make the system design and parts change on functional enhancement easily.

Nuvoton NuMaker-NUC1263SD evaluation board and Nu-Link debugger are powerful tools for product evaluation and development. It supports IDEs provided by third parties, such as Keil MDK, IAR EWARM and NuEclipse IDE with GNU GCC compiler.

1.1 Key Feature and Application

Product Line	USB	UART	I²C	I3C	SPI/I²S	PWM	LED Lighting Strip Interface (LLSI)	PDMA	GPIO	DAC	ACMP	ADC
NUC1263	2.0 FS Device	3	3	2	3	24	6	10	49	4	4	16

Table 1.1-1 Key Features Support Table

The NUC1263 series is suitable for a wide range of applications such as:

- Industrial Control
- Lighting Control
- Keyboard/Mouse
- Home Appliance
- Amusement Device
- Home Automation
- Security Alarm System
- Portable Data Collector

- USB to SPI Device
- PWM Control
- LED Control

2 FEATURES

Core and System	
Arm Cortex-M23 without TrustZone	• Arm Cortex-M23 core, running up to 72 MHz • Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • DSP extension 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access
Brown-out Detector (BOD)	• Four-level BOD with brown-out interrupt and reset option
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Flash	• 64 Kbytes on-chip Application ROM (APROM) • Embedded with 4 Kbytes cache, with performance at zero wait cycle in continuous address read access • 4 Kbytes on-chip Flash for user program loader (LDROM) • All on-chip Flash support 2 Kbytes page erase • Fast Flash programming verification with CRC-32 • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• 20 Kbytes on-chip SRAM • Supports byte-, half-word- and word-access • PDMA operation

Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value • Supports order reverse setting and one's complement setting for input data and CRC checksum • Supports 8/16/32-bit of data width • Supports using PDMA to write data to perform CRC operation
Peripheral DMA (PDMA)	• Up to 10 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather Transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Supports Fixed-priority and Round-robin priority modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC) trimmed to 0.25% accuracy that can optionally be used as a system clock and for crystal-less USB • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 144 MHz on-chip PLL, sourced from HIRC or HXT, allowing CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Timers	
32-bit Timer	• Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle-output and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter

	• Supports chip wake-up function, if a timer interrupt signal is generated
Basic PWM (BPWM)	• Four 16-bit counters with 12-bit clock prescale for twenty-four 144 MHz PWM output channel • Up to 24 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 3 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger ADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• One set of 12-bit, 18-ch 800 KSPS SAR ADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed • One internal channel for band-gap VBG input • Supports external V_{REF} pin or internal reference voltage • Conversion can be triggered by software, external pin, Timer 0~3 overflow pulse or BPWM • Configurable ADC sampling time • PDMA operation
Digital-to-Analog Converter (DAC)	• Up to four sets of 8-bit, 200 KSPS voltage type DAC without buffer • Conversion can be triggered by the software, Timer0~3, external pin • PDMA operation

Analog Comparator (ACMP)	• Up to four rail-to-rail Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports I/O pins, band-gap, DAC, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 0mV, 20mV and 40mV • Supports offset calibration

Internal reference voltage	• One Internal reference voltage with 2.048V, 2.560V, 3.072V, 4.096V
	• Can be configured to supply a reference voltage to the following:
	  • ADC reference Voltage
	  • DAC reference Voltage
	  • Comparator negative input

Temperature Sensor	• Built-in calibrated temperature sensor • Supported temperature range: –40 to 105 °C • Precision: ±2 °C
Communication Interfaces	
Low-power UART	• Low-power UARTs with up to 7.2 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600 bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function

		• Supports PDMA operation
I²C		• Up to three sets of I²C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) and High speed mode (Up to 3.4Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation • Supports setup/hold time programmable
I3CS		• Supports up to two I3C ports • Supports Slave mode only • Supports 7-bit addressing mode • Static or Dynamic Slave Device support • Built-in Hardware Dynamic Address Allocation support (ENTDAA/SETDASA) • Built-in CCC transfer handler • Auto Hot-Join request generation support • In-Band Interrupt request generation support • Adaptive mode of operation between I²C and I3C depending on I3C bus traffic • Built-in S0-S5 Error Handling • Supports Power-down wake-up function • Supports PDMA mode for data transfer • Supports SDR mode, data rates up to 12.5 Mbps • Supports HDR-DDR mode, data rates up to 25 Mbps
SPI/I²S		• Up to three sets of SPI/ I²S controller with Master/Slave mode • Provides separate 4-level of 32-bit (or 8-level of 16-bit) depth transmit and receive FIFO buffers
	SPI	
		• Master mode up to 24 MHz (V_{DD} = 1.8 ~5.5V) • Slave mode up to 11.5 MHz (V_{DD} = 1.8 ~5.5V) • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence

	• Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Support receive-only mode • PDMA operation **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports high drive and high sink current I/O • Supports software selectable slew rate control • Configurable I/O mode of all pins after reset default to Quasi-bidirection mode or input mode
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports suspend function when no bus activity exists for 3 ms • 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types • 1 Kbytes configurable RAM for endpoint buffer • Remote wake-up capability • Start of Frame (SOF) locked clock pulse generation for crystal-less feature • Supports Link Power Management (LPM) • Supports Battery charging 1.2 (BC1.2)

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

QFN33	QFN48	LQFP48	LQFP64
NUC1263ZD4CE	NUC1263ND4CE	NUC1263LD4CE	NUC1263SD4CE

3.2 NUC1263 Series Naming Rule

NUC	1263	S	D	4	C	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
Cortex-M23	1263: USB	Z: QFN33 (5x5 mm) N: QFN48 (7x7 mm) L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm)	D: 64 KB	4: 20 KB		E: -40 ˚C ~ 105 ˚C

3.3 NUC1263 Series Selection Guide

PART NUMBER		NUC1263ZD4CE	NUC1263ND4CE	NUC1263LD4CE	NUC1263SD4CE
Flash (KB)		64			
SRAM (KB)		20			
LDROM (KB)		4			
PLL (MHz)		144			
HXT		√			
LXT		√			
I/O		22	36	36	49
32-bit Timer		4			
BPWM		24			
WDT/WWDT		√			
Connectivity	UART	3			
	SPI /I^2S	3			
	I^2C	3			
	I3C	1 (1V, JESD300-5)		2	
12-bit ADC		16			
ACMP		4			
DAC		4			
USB 2.0 FS Device		-		√	
LLSI		6			
PDMA		10			
Internal V_{REF}		√			
Package		QFN33	QFN48	LQFP48	LQFP64

4 PIN CONFIGURATION

Users can find pin configuration information in the Multi-function Pin Diagram section or by using NuTool - PinConfig. The NuTool - PinConfig contains all Nuvoton NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 Pin Diagram

NuMicro NUC1263 LQFP64 Pin Diagram

Corresponding Part Number: NUC1263SD4CE

4.1.1.1

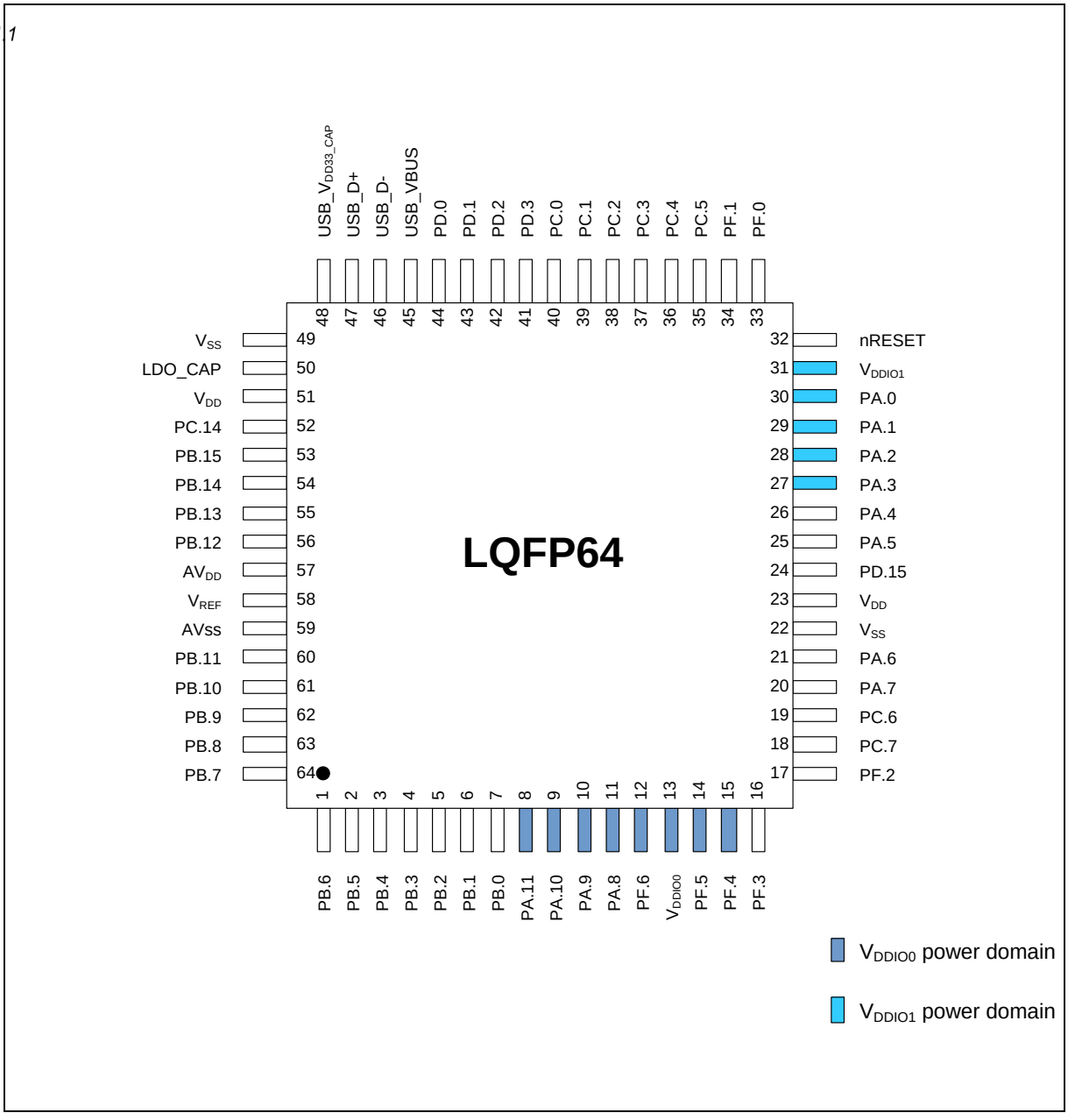


Figure 4.1-1 NuMicro NUC1263 LQFP 64-pin Diagram

NuMicro NUC1263 LQFP48 Pin Diagram

Corresponding Part Number: NUC1263LD4CE

4.1.1.2

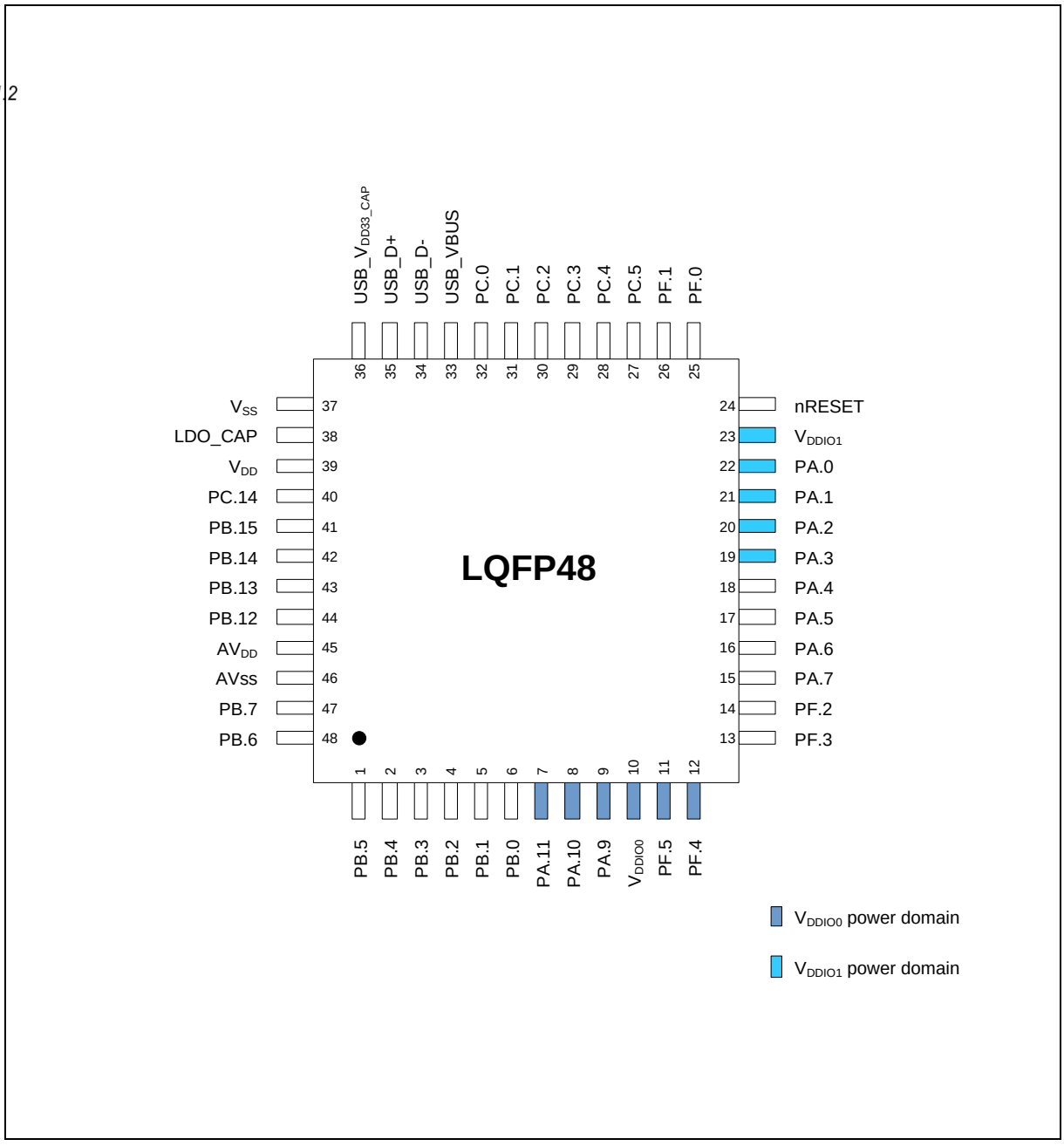


Figure 4.1-2 NuMicro NUC1263 LQFP 48-pin Diagram

NuMicro NUC1263 QFN48 Pin Diagram

Corresponding Part Number: NUC1263ND4CE

4.1.1.3

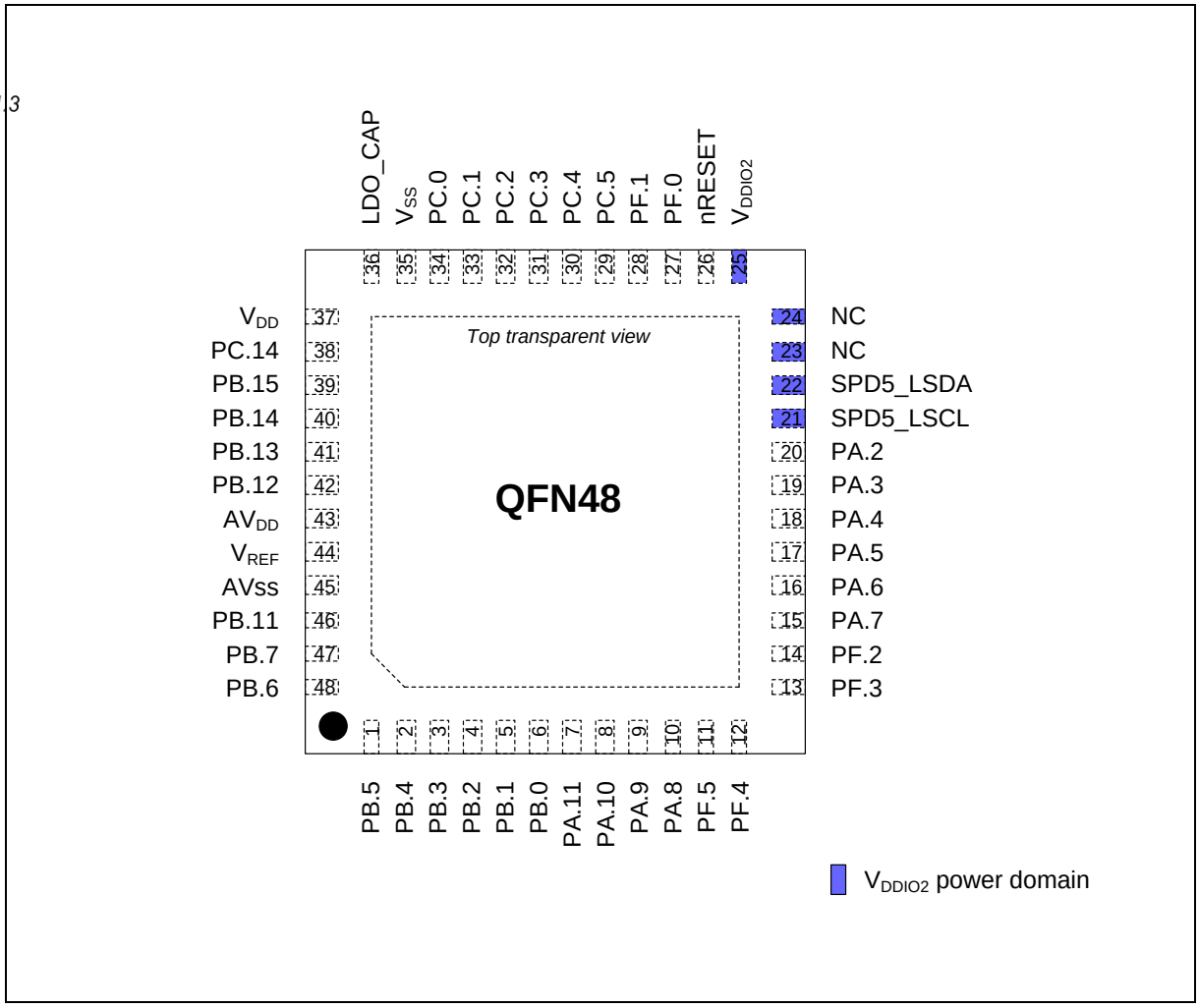


Figure 4.1-3 NuMicro NUC1263 QFN 48-pin Diagram

NuMicro NUC1263 QFN33 Pin Diagram

Corresponding Part Number: NUC1263ZD4CE

4.1.1.4

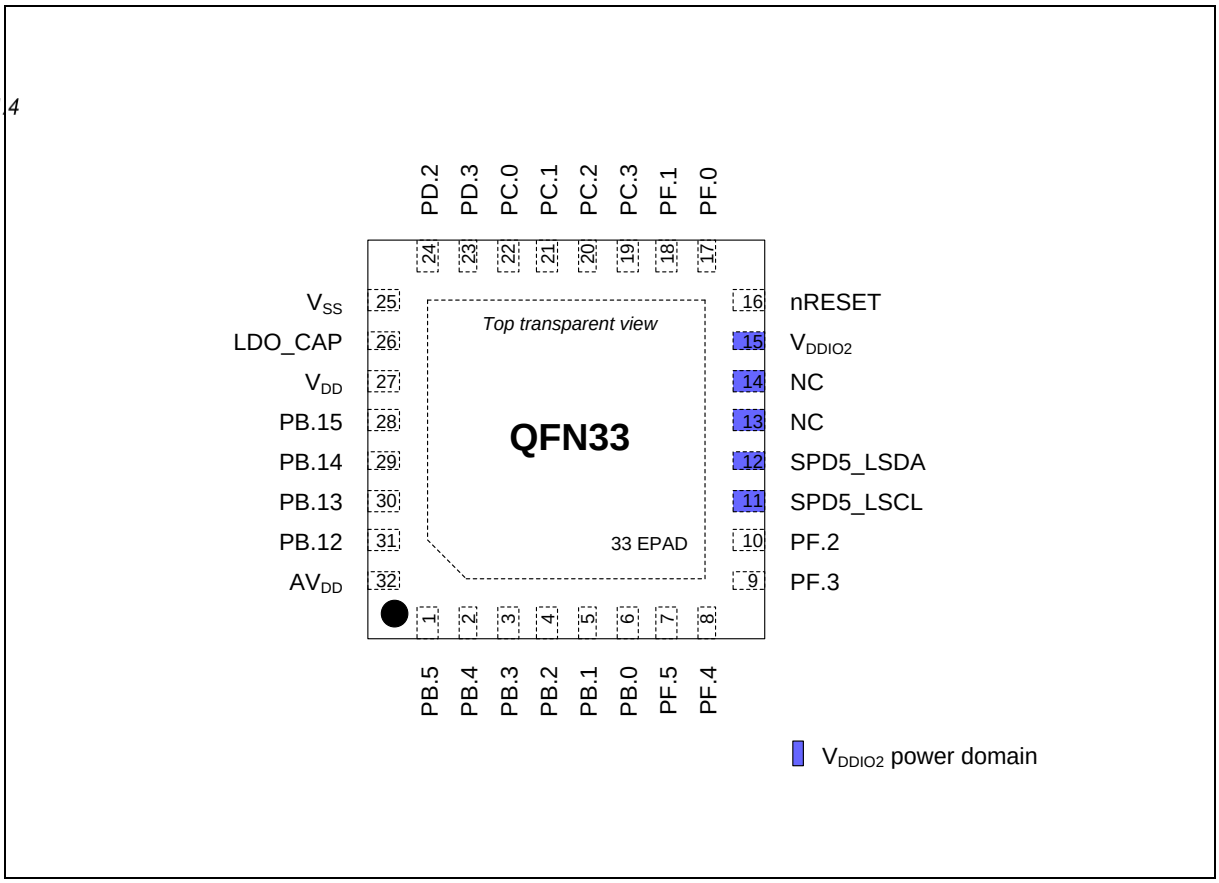


Figure 4.1-4 NuMicro NUC1263 QFN 33-pin Diagram

4.1.2 Multi-function Pin Diagram

NuMicro NUC1263 LQFP64 Pin Multi-function Pin Diagram

Corresponding Part Number: NUC1263SD4CE

4.1.2.1

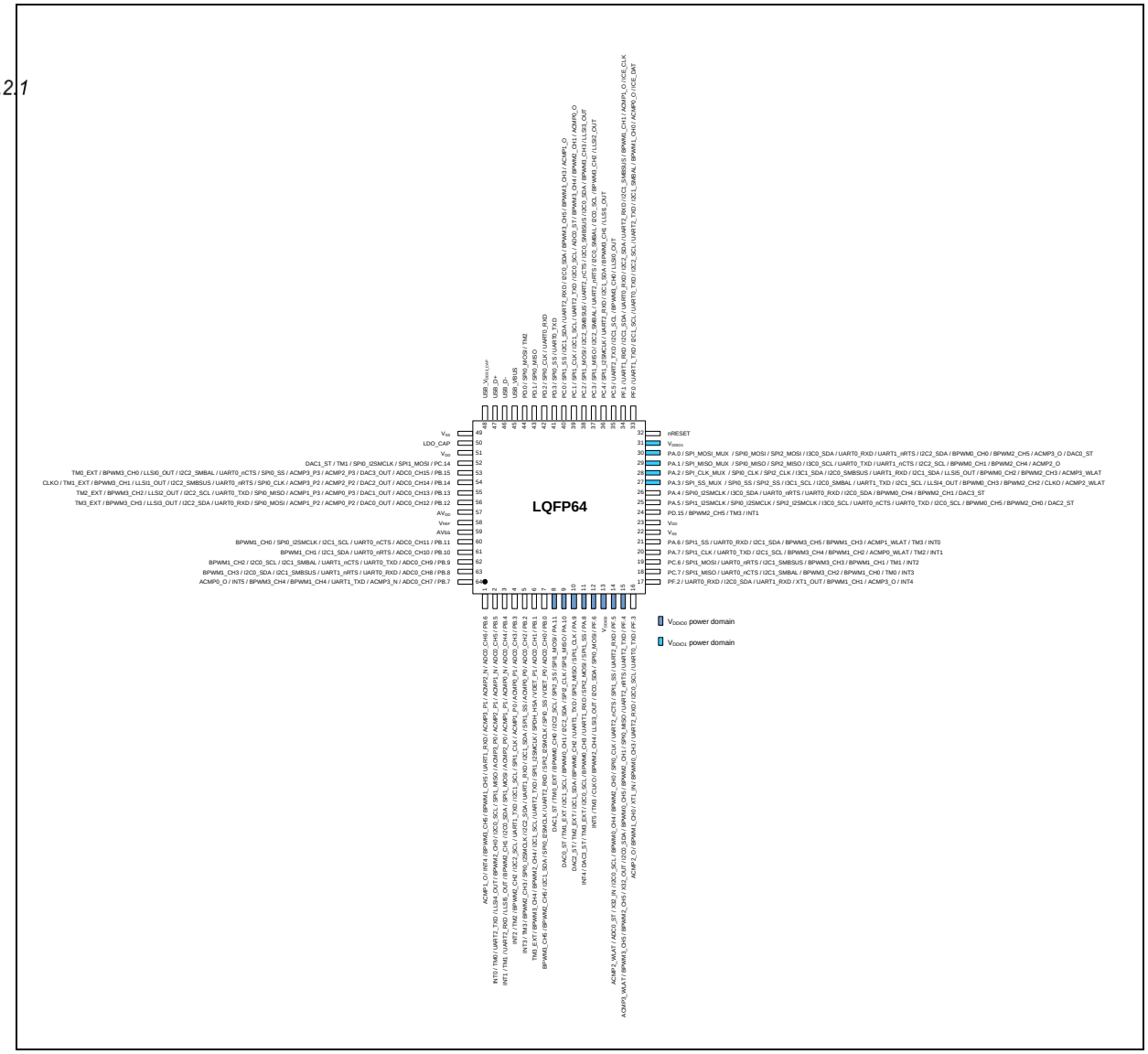


Figure 4.1-5 NuMicro NUC1263 LQFP 64-pin Multi-function Pin Diagram

NuMicro NUC1263 LQFP48 Pin Multi-function Pin Diagram

Corresponding Part Number: NUC1263LD4CE

4.1.2.2

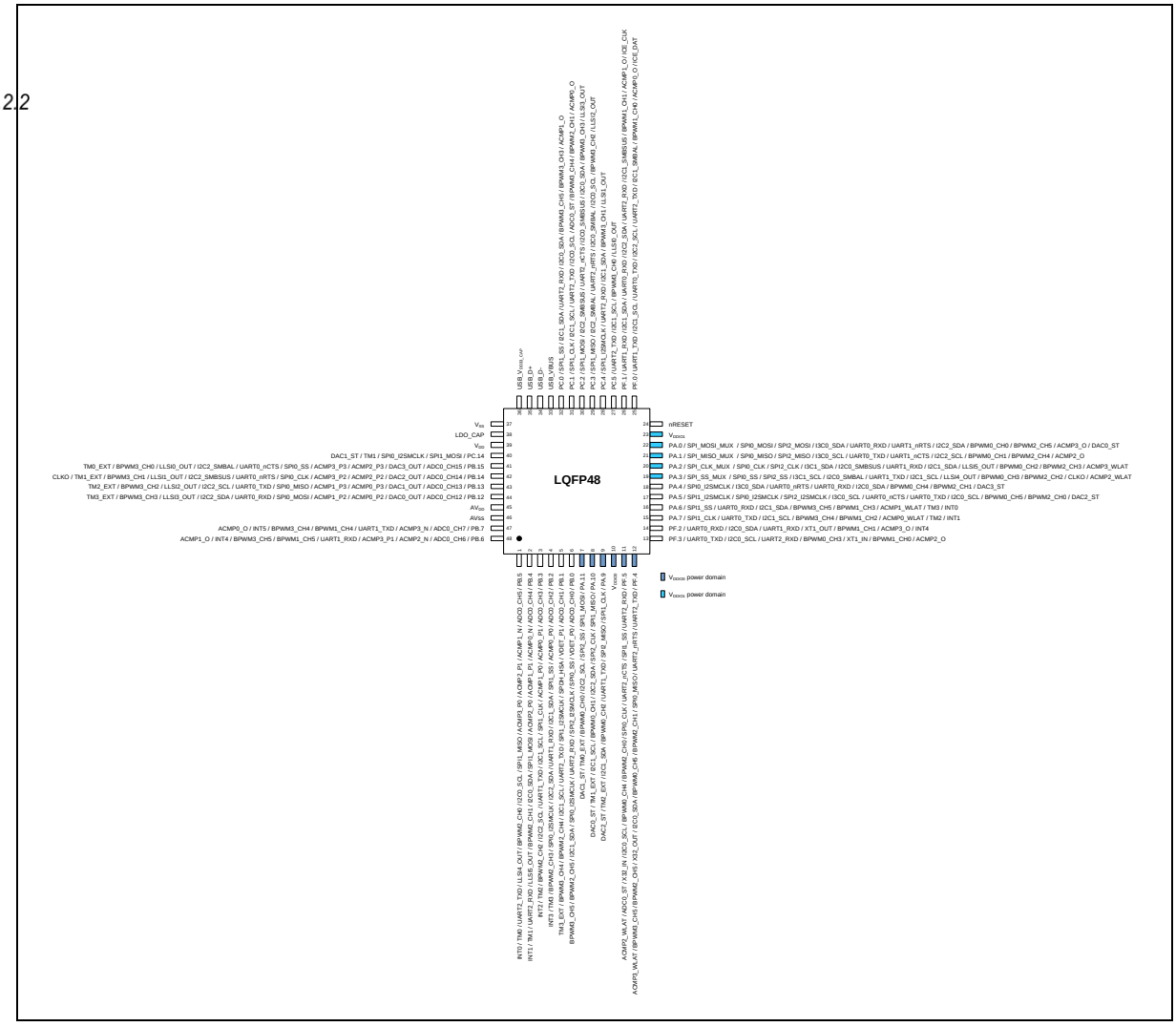


Figure 4.1-6 NuMicro NUC1263 LQFP 48-pin Multi-function Pin Diagram

NuMicro NUC1263 QFN48 Pin Multi-function Pin Diagram

Corresponding Part Number: NUC1263ND4CE

4.1.2.3

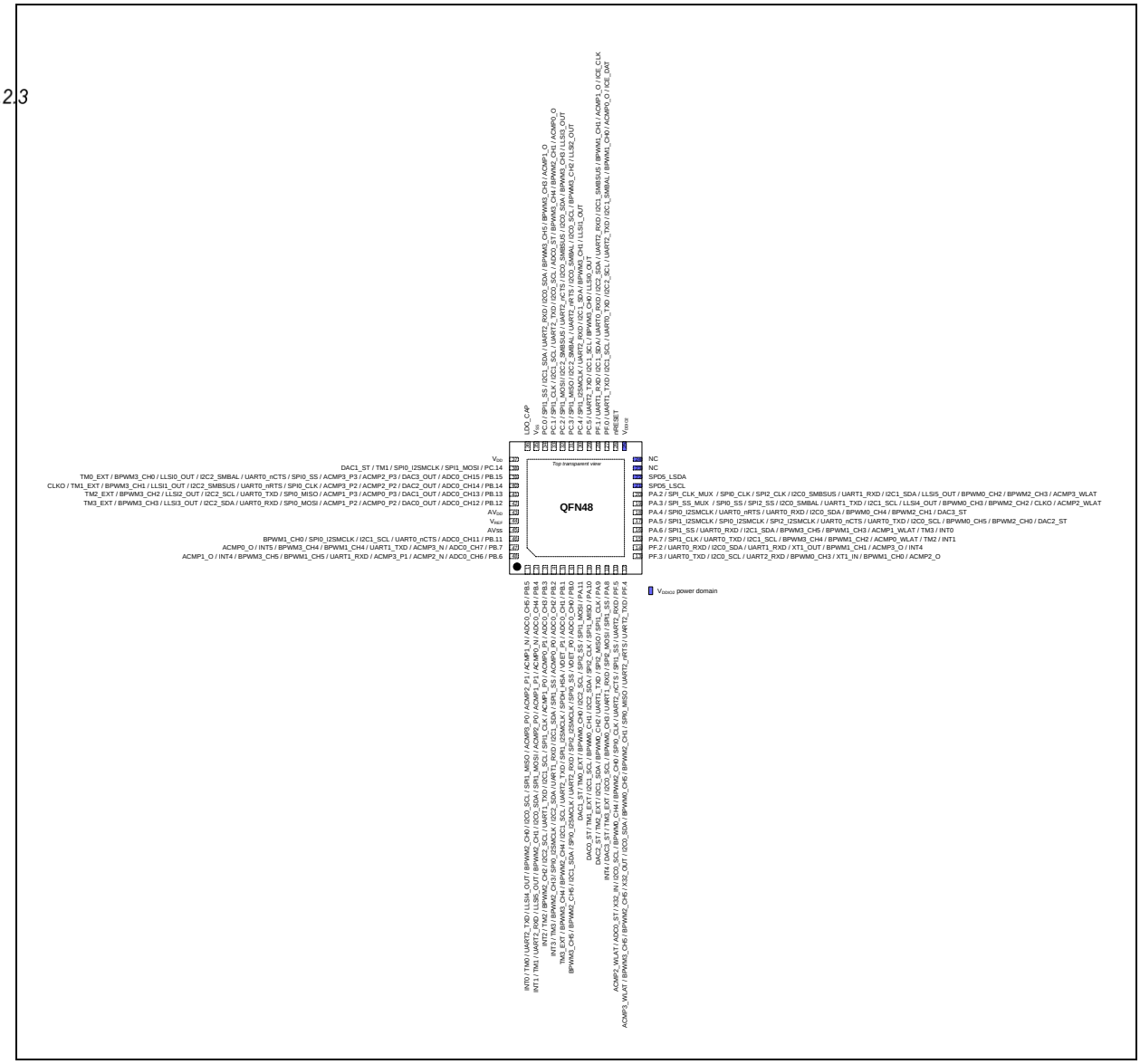


Figure 4.1-7 NuMicro NUC1263 QFN 48-pin Multi-function Pin Diagram

NuMicro NUC1263 QFN33 Pin Multi-function Pin Diagram

Corresponding Part Number: NUC1263ZD4CE

4.1.2.4

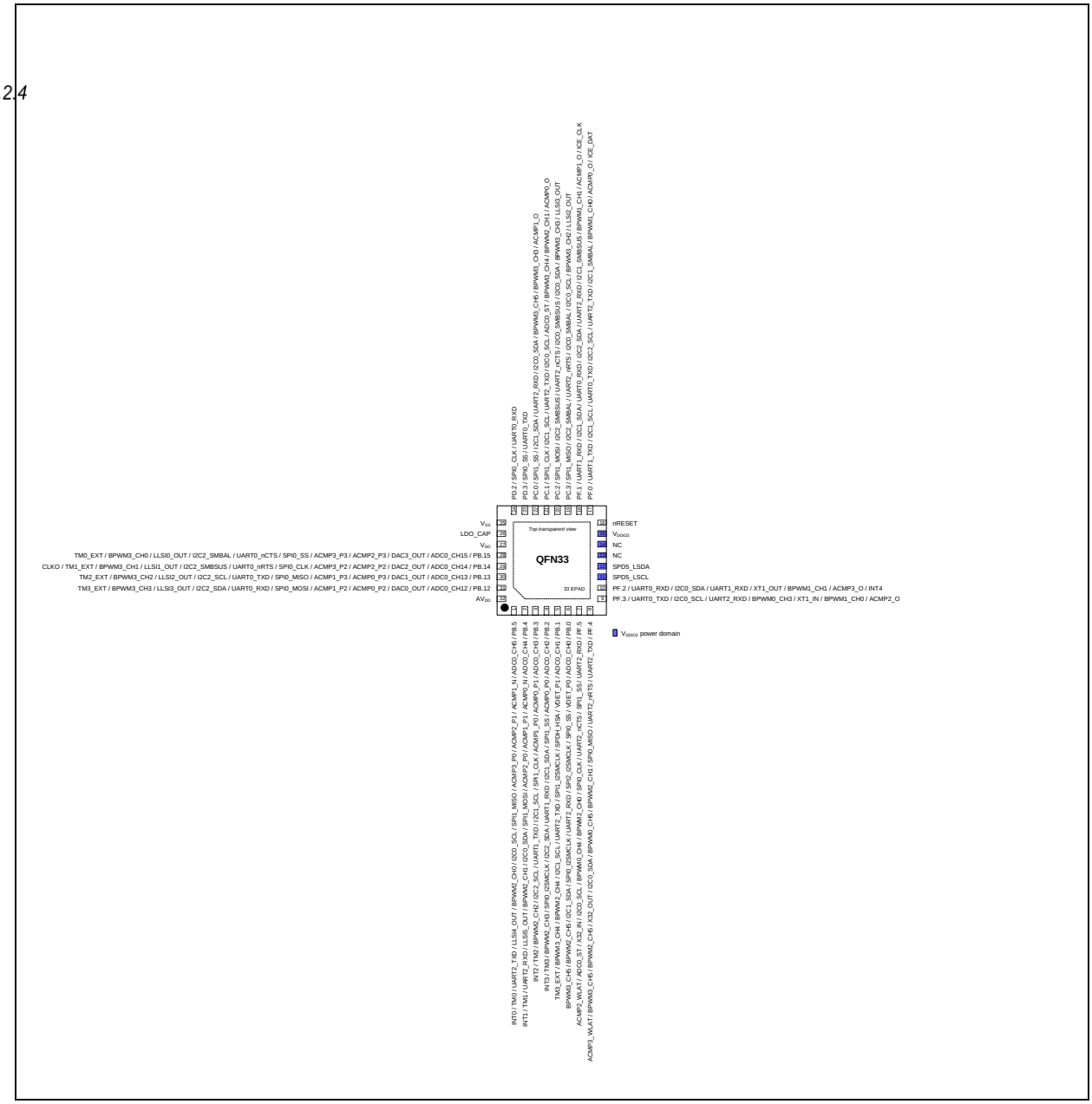


Figure 4.1-8 NuMicro NUC1263 QFN 33-pin Multi-function Pin Diagram

4.2 Pin Mapping

Different part number with same package might has different function. Please refer to the selection guide in section 3.3, Pin Configuration in section 4.1 or NuTool - PinConfig.

Corresponding Part Number: NUC1263ZD4CE, NUC1263ND4CE, NUC1263LD4CE, NUC1263SD4CE

	NUC1263			
Pin Name	33 Pin	48 Pin	48 Pin	64 Pin
PB.5	1	1	1	2
PB.4	2	2	2	3
PB.3	3	3	3	4
PB.2	4	4	4	5
PB.1	5	5	5	6
PB.0	6	6	6	7
PA.11		7	7	8
PA.10		8	8	9
PA.9		9	9	10
PA.8		10		11
PF.6				12
V_{DDIO0}			10	13
PF.5	7	11	11	14
PF.4	8	12	12	15
PF.3	9	13	13	16
PF.2	10	14	14	17
PC.7				18
PC.6				19
PA.7		15	15	20
PA.6		16	16	21
V_{SS}				22
V_{DD}				23
PD.15				24
PA.5		17	17	25
PA.4		18	18	26
PA.3		19	19	27
PA.2		20	20	28
PA.1			21	29

PA.0			22	30
V_{DDIO1}			23	31
NC	13	23		
NC	14	24		
SPD5_LSCL	11	21		
SPD5_LSDA	12	22		
V_{DDIO2}	15	25		
nRESET	16	26	24	32
PF.0	17	27	25	33
PF.1	18	28	26	34
PC.5		29	27	35
PC.4		30	28	36
PC.3	19	31	29	37
PC.2	20	32	30	38
PC.1	21	33	31	39
PC.0	22	34	32	40
PD.3	23			41
PD.2	24			42
PD.1				43
PD.0				44
USB_VBUS			33	45
USB_D-			34	46
USB_D+			35	47
USB_VDD33_CAP			36	48
V_{SS}	25	35	37	49
LDO_CAP	26	36	38	50
V_{DD}	27	37	39	51
PC.14		38	40	52
PB.15	28	39	41	53
PB.14	29	40	42	54
PB.13	30	41	43	55
PB.12	31	42	44	56
AV_{DD}	32	43	45	57
V_{REF}		44		58
AV_{SS}		45	46	59

PB.11		46		60
PB.10				61
PB.9				62
PB.8				63
PB.7		47	47	64
PB.6		48	48	1
V_{SS}	33			

4.3 Pin Functional Description

4.3.1 Multi-function Summary Table

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
ACMP2	ACMP2_N	A	Analog comparator 2 negative input pin.
	ACMP2_O	O	Analog comparator 2 output pin.
	ACMP2_P0	A	Analog comparator 2 positive input 0 pin.
	ACMP2_P1	A	Analog comparator 2 positive input 1 pin.
	ACMP2_P2	A	Analog comparator 2 positive input 2 pin.
	ACMP2_P3	A	Analog comparator 2 positive input 3 pin.
	ACMP2_WLAT	I	Analog comparator 2 window latch input pin
ACMP3	ACMP3_N	A	Analog comparator 3 negative input pin.
	ACMP3_O	O	Analog comparator 3 output pin.
	ACMP3_P0	A	Analog comparator 3 positive input 0 pin.
	ACMP3_P1	A	Analog comparator 3 positive input 1 pin.
	ACMP3_P2	A	Analog comparator 3 positive input 2 pin.
	ACMP3_P3	A	Analog comparator 3 positive input 3 pin.
	ACMP3_WLAT	I	Analog comparator 3 window latch input pin
ADC0	ADC0_CH0	A	ADC0 channel 0 analog input.
	ADC0_CH1	A	ADC0 channel 1 analog input.
	ADC0_CH2	A	ADC0 channel 2 analog input.

Group	Pin Name	Type	Description
	ADC0_CH3	A	ADC0 channel 3 analog input.
	ADC0_CH4	A	ADC0 channel 4 analog input.
	ADC0_CH5	A	ADC0 channel 5 analog input.
	ADC0_CH6	A	ADC0 channel 6 analog input.
	ADC0_CH7	A	ADC0 channel 7 analog input.
	ADC0_CH8	A	ADC0 channel 8 analog input.
	ADC0_CH9	A	ADC0 channel 9 analog input.
	ADC0_CH10	A	ADC0 channel 10 analog input.
	ADC0_CH11	A	ADC0 channel 11 analog input.
	ADC0_CH12	A	ADC0 channel 12 analog input.
	ADC0_CH13	A	ADC0 channel 13 analog input.
	ADC0_CH14	A	ADC0 channel 14 analog input.
	ADC0_CH15	A	ADC0 channel 15 analog input.
	ADC0_ST	I	ADC0 external trigger input pin.
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
BPWM2	BPWM2_CH0	I/O	BPWM2 channel 0 output/capture input.
	BPWM2_CH1	I/O	BPWM2 channel 1 output/capture input.
	BPWM2_CH2	I/O	BPWM2 channel 2 output/capture input.
	BPWM2_CH3	I/O	BPWM2 channel 3 output/capture input.
	BPWM2_CH4	I/O	BPWM2 channel 4 output/capture input.
	BPWM2_CH5	I/O	BPWM2 channel 5 output/capture input.
BPWM3	BPWM3_CH0	I/O	BPWM3 channel 0 output/capture input.
	BPWM3_CH1	I/O	BPWM3 channel 1 output/capture input.

Group	Pin Name	Type	Description
	BPWM3_CH2	I/O	BPWM3 channel 2 output/capture input.
	BPWM3_CH3	I/O	BPWM3 channel 3 output/capture input.
	BPWM3_CH4	I/O	BPWM3 channel 4 output/capture input.
	BPWM3_CH5	I/O	BPWM3 channel 5 output/capture input.
CLKO	CLKO	O	Clock Out
DAC0	DAC0_OUT	A	DAC0 channel analog output.
	DAC0_ST	I	DAC0 external trigger input.
DAC1	DAC1_OUT	A	DAC1 channel analog output.
	DAC1_ST	I	DAC1 external trigger input.
DAC2	DAC2_OUT	A	DAC2 channel analog output.
	DAC2_ST	I	DAC2 external trigger input.
DAC3	DAC3_OUT	A	DAC3 channel analog output.
	DAC3_ST	I	DAC3 external trigger input.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
	I2C1_SMBAL	O	I2C1 SMBus SMBALTER pin
	I2C1_SMBSUS	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C2	I2C2_SCL	I/O	I2C2 clock pin.
	I2C2_SDA	I/O	I2C2 data input/output pin.
	I2C2_SMBAL	O	I2C2 SMBus SMBALTER pin
	I2C2_SMBSUS	O	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
I3C0	I3C0_SCL	I/O	I3C0 clock pin.
	I3C0_SDA	I/O	I3C0 data input/output pin.
I3C1	I3C1_SCL	I/O	I3C1 clock pin.
	I3C1_SDA	I/O	I3C1 data input/output pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.

Group	Pin Name	Type	Description
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
LLSI0	LLSI0_OUT	O	LED Lighting Strip Interface 0 output pin.
LLSI1	LLSI1_OUT	O	LED Lighting Strip Interface 1 output pin.
LLSI2	LLSI2_OUT	O	LED Lighting Strip Interface 2 output pin.
LLSI3	LLSI3_OUT	O	LED Lighting Strip Interface 3 output pin.
LLSI4	LLSI4_OUT	O	LED Lighting Strip Interface 4 output pin.
LLSI5	LLSI5_OUT	O	LED Lighting Strip Interface 5 output pin.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I^2S master clock output pin
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_I2SMCLK	I/O	SPI1 I^2S master clock output pin
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
SPI2	SPI2_CLK	I/O	SPI2 serial clock pin.
	SPI2_I2SMCLK	I/O	SPI2 I^2S master clock output pin
	SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin.
	SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin.
	SPI2_SS	I/O	SPI2 slave select pin.
SPI	SPI_CLK_MUX	I/O	External SPI serial clock pin for SPI mux.
	SPI_MISO_MUX	I/O	SPI_ MISOM (Master In, Slave Out) pin.
	SPI_MOSI_MUX	I/O	SPI_ MOSIM (Master Out, Slave In) pin.
	SPI_SS_MUX	I/O	SPI_ slave select M pin.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.

Group	Pin Name	Type	Description
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
VDET	VDET_P0	A	Voltage detector positive input 0 pin.
	VDET_P1	A	Voltage detector positive input 1 pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
USB	USB_D+	A	USB differential signal D+.
	USB_D-	A	USB differential signal D-.
	USB_VBUS	P	Power supply from USB host or HUB.
	USB_VDD33_CAP	A	Internal power regulator output 3.3V decoupling pin. **Note:** This pin needs to be connected with a 1uF capacitor.
SPD5	SPD5_LSCL	I/O	SPD5 hub local bus clock pin.
	SPD5_LSDA	I/O	SPD5 hub local bus data input/output pin.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. **Note:** This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.

Group	Pin Name	Type	Description
	V_{DDIO0}	P	Power supply for VDDIO0 domain I/O ports
	V_{DDIO1}	P	Power supply for VDDIO1 domain I/O ports
	V_{DDIO2}	P	Power supply for VDDIO2 domain I/O ports
	V_{REF}	A	ADC reference voltage input. **Note:** This pin needs to be connected with a 1uF capacitor.
	V_{SS}	P	Ground pin for digital circuit.
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

4.3.2 Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	SPI_MOSI_MUX	I/O	MFP2	SPI_ MOSIM (Master Out, Slave In) pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	SPI2_MOSI	I/O	MFP5	SPI2 MOSI (Master Out, Slave In) pin.
	I3C0_SDA	I/O	MFP6	I3C0 data input/output pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
	BPWM2_CH5	I/O	MFP13	BPWM2 channel 5 output/capture input.
	ACMP3_O	O	MFP14	Analog comparator 3 output pin.
	DAC0_ST	I	MFP15	DAC0 external trigger input.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	SPI_MISO_MUX	I/O	MFP2	SPI_ MISOM (Master In, Slave Out) pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	SPI2_MISO	I/O	MFP5	SPI2 MISO (Master In, Slave Out) pin.
	I3C0_SCL	I/O	MFP6	I3C0 clock pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	I2C2_SCL	I/O	MFP9	I2C2 clock pin.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
	BPWM2_CH4	I/O	MFP13	BPWM2 channel 4 output/capture input.
	ACMP2_O	O	MFP15	Analog comparator 2 output pin.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SPI_CLK_MUX	I/O	MFP2	External SPI serial clock pin for SPI mux.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	SPI2_CLK	I/O	MFP5	SPI2 serial clock pin.
	I3C1_SDA	I/O	MFP6	I3C1 data input/output pin.
	I2C0_SMBSUS	O	MFP7	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	LLSI5_OUT	O	MFP10	LED Lighting Strip Interface 5 output pin.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.

	Pin Name	Type	MFP	Description
	BPWM2_CH3	I/O	MFP13	BPWM2 channel 3 output/capture input.
	ACMP3_WLAT	I	MFP15	Analog comparator 3 window latch input pin
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SPI_SS_MUX	I/O	MFP2	SPI_ slave select M pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	SPI2_SS	I/O	MFP5	SPI2 slave select pin.
	I3C1_SCL	I/O	MFP6	I3C1 clock pin.
	I2C0_SMBAL	O	MFP7	I2C0 SMBus SMBALTER pin
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	LLSI4_OUT	O	MFP10	LED Lighting Strip Interface 4 output pin.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	BPWM2_CH2	I/O	MFP13	BPWM2 channel 2 output/capture input.
	CLKO	O	MFP14	Clock Out
	ACMP2_WLAT	I	MFP15	Analog comparator 2 window latch input pin
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	I3C0_SDA	I/O	MFP6	I3C0 data input/output pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	UART0_RXD	I	MFP8	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
	BPWM2_CH1	I/O	MFP13	BPWM2 channel 1 output/capture input.
	DAC3_ST	I	MFP15	DAC3 external trigger input.
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	SPI1_I2SMCLK	I/O	MFP2	SPI1 I^2S master clock output pin
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	SPI2_I2SMCLK	I/O	MFP5	SPI2 I^2S master clock output pin
	I3C0_SCL	I/O	MFP6	I3C0 clock pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
	BPWM2_CH0	I/O	MFP13	BPWM2 channel 0 output/capture input.

	Pin Name	Type	MFP	Description
	DAC2_ST	I	MFP15	DAC2 external trigger input.
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP2	SPI1 slave select pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
	BPWM3_CH5	I/O	MFP11	BPWM3 channel 5 output/capture input.
	BPWM1_CH3	I/O	MFP12	BPWM1 channel 3 output/capture input.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	BPWM3_CH4	I/O	MFP11	BPWM3 channel 4 output/capture input.
	BPWM1_CH2	I/O	MFP12	BPWM1 channel 2 output/capture input.
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP3	SPI1 slave select pin.
	SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
	I2C0_SCL	I/O	MFP10	I2C0 clock pin.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
	DAC3_ST	I	MFP14	DAC3 external trigger input.
	INT4	I	MFP15	External interrupt 4 input pin.
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
	SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin.
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
	BPWM0_CH2	I/O	MFP9	BPWM0 channel 2 output/capture input.
	I2C1_SDA	I/O	MFP10	I2C1 data input/output pin.

	Pin Name	Type	MFP	Description
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
	DAC2_ST	I	MFP14	DAC2 external trigger input.
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
	SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
	I2C2_SDA	I/O	MFP7	I2C2 data input/output pin.
	BPWM0_CH1	I/O	MFP9	BPWM0 channel 1 output/capture input.
	I2C1_SCL	I/O	MFP10	I2C1 clock pin.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	DAC0_ST	I	MFP14	DAC0 external trigger input.
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin.
	SPI2_SS	I/O	MFP4	SPI2 slave select pin.
	I2C2_SCL	I/O	MFP7	I2C2 clock pin.
	BPWM0_CH0	I/O	MFP9	BPWM0 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
	DAC1_ST	I	MFP14	DAC1 external trigger input.
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
	VDET_P0	A	MFP1	Voltage detector positive input 0 pin.
	SPI0_SS	I/O	MFP3	SPI0 slave select pin.
	SPI2_I2SMCLK	I/O	MFP4	SPI2 I^2S master clock output pin
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	SPI0_I2SMCLK	I/O	MFP8	SPI0 I^2S master clock output pin
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	BPWM2_CH5	I/O	MFP11	BPWM2 channel 5 output/capture input.
	BPWM3_CH5	I/O	MFP12	BPWM3 channel 5 output/capture input.
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
	VDET_P1	A	MFP1	Voltage detector positive input 1 pin.
	SPI1_I2SMCLK	I/O	MFP2	SPI1 I^2S master clock output pin
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	BPWM2_CH4	I/O	MFP11	BPWM2 channel 4 output/capture input.

	Pin Name	Type	MFP	Description
	BPWM3_CH4	I/O	MFP12	BPWM3 channel 4 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
	SPI1_SS	I/O	MFP2	SPI1 slave select pin.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	I2C2_SDA	I/O	MFP7	I2C2 data input/output pin.
	SPI0_I2SMCLK	I/O	MFP8	SPI0 I^2S master clock output pin
	BPWM2_CH3	I/O	MFP11	BPWM2 channel 3 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
	ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	I2C2_SCL	I/O	MFP7	I2C2 clock pin.
	BPWM2_CH2	I/O	MFP11	BPWM2 channel 2 output/capture input.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
	ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
	ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
	ACMP2_P0	A	MFP1	Analog comparator 2 positive input 0 pin.
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
	BPWM2_CH1	I/O	MFP11	BPWM2 channel 1 output/capture input.
	LLSI5_OUT	O	MFP12	LED Lighting Strip Interface 5 output pin.
	UART2_RXD	I	MFP13	UART2 data receiver input pin.

	Pin Name	Type	MFP	Description
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
	ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
	ACMP2_P1	A	MFP1	Analog comparator 2 positive input 1 pin.
	ACMP3_P0	A	MFP1	Analog comparator 3 positive input 0 pin.
	SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
	I2C0_SCL	I/O	MFP6	I2C0 clock pin.
	BPWM2_CH0	I/O	MFP11	BPWM2 channel 0 output/capture input.
	LLSI4_OUT	O	MFP12	LED Lighting Strip Interface 4 output pin.
	UART2_TXD	O	MFP13	UART2 data transmitter output pin.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
	ACMP2_N	A	MFP1	Analog comparator 2 negative input pin.
	ACMP3_P1	A	MFP1	Analog comparator 3 positive input 1 pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	BPWM1_CH5	I/O	MFP10	BPWM1 channel 5 output/capture input.
	BPWM3_CH5	I/O	MFP12	BPWM3 channel 5 output/capture input.
	INT4	I	MFP13	External interrupt 4 input pin.
	ACMP1_O	O	MFP15	Analog comparator 1 output pin.
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
	ACMP3_N	A	MFP1	Analog comparator 3 negative input pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	BPWM1_CH4	I/O	MFP10	BPWM1 channel 4 output/capture input.
	BPWM3_CH4	I/O	MFP12	BPWM3 channel 4 output/capture input.
	INT5	I	MFP13	External interrupt 5 input pin.
	ACMP0_O	O	MFP15	Analog comparator 0 output pin.
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH8	A	MFP1	ADC0 channel 8 analog input.
	UART0_RXD	I	MFP5	UART0 data receiver input pin.

	Pin Name	Type	MFP	Description
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.
	I2C1_SMBSUS	O	MFP7	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	BPWM1_CH3	I/O	MFP10	BPWM1 channel 3 output/capture input.
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH9	A	MFP1	ADC0 channel 9 analog input.
	UART0_TXD	O	MFP5	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
	I2C1_SMBAL	O	MFP7	I2C1 SMBus SMBALTER pin
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	BPWM1_CH2	I/O	MFP10	BPWM1 channel 2 output/capture input.
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
	UART0_nRTS	O	MFP5	UART0 request to Send output pin.
	I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
	BPWM1_CH1	I/O	MFP10	BPWM1 channel 1 output/capture input.
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
	UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
	I2C1_SCL	I/O	MFP7	I2C1 clock pin.
	SPI0_I2SMCLK	I/O	MFP9	SPI0 I^2S master clock output pin
	BPWM1_CH0	I/O	MFP10	BPWM1 channel 0 output/capture input.
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
	DAC0_OUT	A	MFP1	DAC0 channel analog output.
	ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
	ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART0_RXD	I	MFP6	UART0 data receiver input pin.
	I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
	LLSI3_OUT	O	MFP10	LED Lighting Strip Interface 3 output pin.
	BPWM3_CH3	I/O	MFP11	BPWM3 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
	DAC1_OUT	A	MFP1	DAC1 channel analog output.
	ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
	ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART0_TXD	O	MFP6	UART0 data transmitter output pin.
	I2C2_SCL	I/O	MFP8	I2C2 clock pin.
	LLSI2_OUT	O	MFP10	LED Lighting Strip Interface 2 output pin.
	BPWM3_CH2	I/O	MFP11	BPWM3 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PB.14	PB.14	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
	DAC2_OUT	A	MFP1	DAC2 channel analog output.
	ACMP2_P2	A	MFP1	Analog comparator 2 positive input 2 pin.
	ACMP3_P2	A	MFP1	Analog comparator 3 positive input 2 pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART0_nRTS	O	MFP6	UART0 request to Send output pin.
	I2C2_SMBSUS	O	MFP8	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
	LLSI1_OUT	O	MFP10	LED Lighting Strip Interface 1 output pin.
	BPWM3_CH1	I/O	MFP11	BPWM3 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP14	Clock Out
PB.15	PB.15	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
	DAC3_OUT	A	MFP1	DAC3 channel analog output.
	ACMP2_P3	A	MFP1	Analog comparator 2 positive input 3 pin.
	ACMP3_P3	A	MFP1	Analog comparator 3 positive input 3 pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
	I2C2_SMBAL	O	MFP8	I2C2 SMBus SMBALTER pin
	LLSI0_OUT	O	MFP10	LED Lighting Strip Interface 0 output pin.
	BPWM3_CH0	I/O	MFP11	BPWM3 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	SPI1_SS	I/O	MFP2	SPI1 slave select pin.
	I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	BPWM3_CH5	I/O	MFP12	BPWM3 channel 5 output/capture input.
	BPWM3_CH3	I/O	MFP13	BPWM3 channel 3 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
	I2C1_SCL	I/O	MFP7	I2C1 clock pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	ADC0_ST	I	MFP11	ADC0 external trigger input pin.
	BPWM3_CH4	I/O	MFP12	BPWM3 channel 4 output/capture input.
	BPWM2_CH1	I/O	MFP13	BPWM2 channel 1 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
	I2C2_SMBSUS	O	MFP7	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
	UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
	I2C0_SMBSUS	O	MFP9	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C0_SDA	I/O	MFP10	I2C0 data input/output pin.
	BPWM3_CH3	I/O	MFP12	BPWM3 channel 3 output/capture input.
	LLSI3_OUT	O	MFP15	LED Lighting Strip Interface 3 output pin.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
	I2C2_SMBAL	O	MFP7	I2C2 SMBus SMBALTER pin
	UART2_nRTS	O	MFP8	UART2 request to Send output pin.
	I2C0_SMBAL	O	MFP9	I2C0 SMBus SMBALTER pin
	I2C0_SCL	I/O	MFP10	I2C0 clock pin.
	BPWM3_CH2	I/O	MFP12	BPWM3 channel 2 output/capture input.
	LLSI2_OUT	O	MFP15	LED Lighting Strip Interface 2 output pin.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	SPI1_I2SMCLK	I/O	MFP2	SPI1 I^2S master clock output pin

	Pin Name	Type	MFP	Description
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	BPWM3_CH1	I/O	MFP12	BPWM3 channel 1 output/capture input.
	LLSI1_OUT	O	MFP15	LED Lighting Strip Interface 1 output pin.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	BPWM3_CH0	I/O	MFP12	BPWM3 channel 0 output/capture input.
	LLSI0_OUT	O	MFP15	LED Lighting Strip Interface 0 output pin.
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP4	SPI1 MOSI (Master Out, Slave In) pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	BPWM3_CH3	I/O	MFP11	BPWM3 channel 3 output/capture input.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP4	SPI1 MISO (Master In, Slave Out) pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin
	BPWM3_CH2	I/O	MFP11	BPWM3 channel 2 output/capture input.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PC.14	PC.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
	DAC1_ST	I	MFP15	DAC1 external trigger input.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART0_TXD	O	MFP9	UART0 data transmitter output pin.
PD.15	PD.15	I/O	MFP0	General purpose digital I/O pin.
	BPWM2_CH5	I/O	MFP12	BPWM2 channel 5 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
	UART0_TXD	O	MFP4	UART0 data transmitter output pin.
	I2C2_SCL	I/O	MFP7	I2C2 clock pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C1_SMBAL	O	MFP9	I2C1 SMBus SMBALTER pin
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	ACMP0_O	O	MFP13	Analog comparator 0 output pin.
	ICE_DAT	I/O	MFP14	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
	UART0_RXD	I	MFP4	UART0 data receiver input pin.
	I2C2_SDA	I/O	MFP7	I2C2 data input/output pin.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C1_SMBSUS	O	MFP9	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	ACMP1_O	O	MFP13	Analog comparator 1 output pin.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.

	Pin Name	Type	MFP	Description
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	XT1_OUT	O	MFP10	External 4~24 MHz (high speed) crystal output pin.
	BPWM1_CH1	I/O	MFP11	BPWM1 channel 1 output/capture input.
	ACMP3_O	O	MFP13	Analog comparator 3 output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
	XT1_IN	I	MFP10	External 4~24 MHz (high speed) crystal input pin.
	BPWM1_CH0	I/O	MFP11	BPWM1 channel 0 output/capture input.
	ACMP2_O	O	MFP13	Analog comparator 2 output pin.
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	UART2_nRTS	O	MFP4	UART2 request to Send output pin.
	SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin.
	BPWM2_CH1	I/O	MFP7	BPWM2 channel 1 output/capture input.
	BPWM0_CH5	I/O	MFP8	BPWM0 channel 5 output/capture input.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	X32_OUT	O	MFP10	External 32.768 kHz crystal output pin.
	BPWM2_CH5	I/O	MFP11	BPWM2 channel 5 output/capture input.
	BPWM3_CH5	I/O	MFP12	BPWM3 channel 5 output/capture input.
	ACMP3_WLAT	I	MFP13	Analog comparator 3 window latch input pin
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	SPI1_SS	I/O	MFP3	SPI1 slave select pin.
	UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
	SPI0_CLK	I/O	MFP5	SPI0 serial clock pin.
	BPWM2_CH0	I/O	MFP7	BPWM2 channel 0 output/capture input.
	BPWM0_CH4	I/O	MFP8	BPWM0 channel 4 output/capture input.

	Pin Name	Type	MFP	Description
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	X32_IN	I	MFP10	External 32.768 kHz crystal input pin.
	ADC0_ST	I	MFP11	ADC0 external trigger input pin.
	ACMP2_WLAT	I	MFP13	Analog comparator 2 window latch input pin
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MFP10	I2C0 data input/output pin.
	LLSI3_OUT	O	MFP11	LED Lighting Strip Interface 3 output pin.
	BPWM2_CH4	I/O	MFP12	BPWM2 channel 4 output/capture input.
	CLKO	O	MFP13	Clock Out
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT5	I	MFP15	External interrupt 5 input pin.

Table 4.3-1 NUC1263 GPIO Multi-function Table

5 BLOCK DIAGRAM

5.1 NUC1263 Series Block Diagram

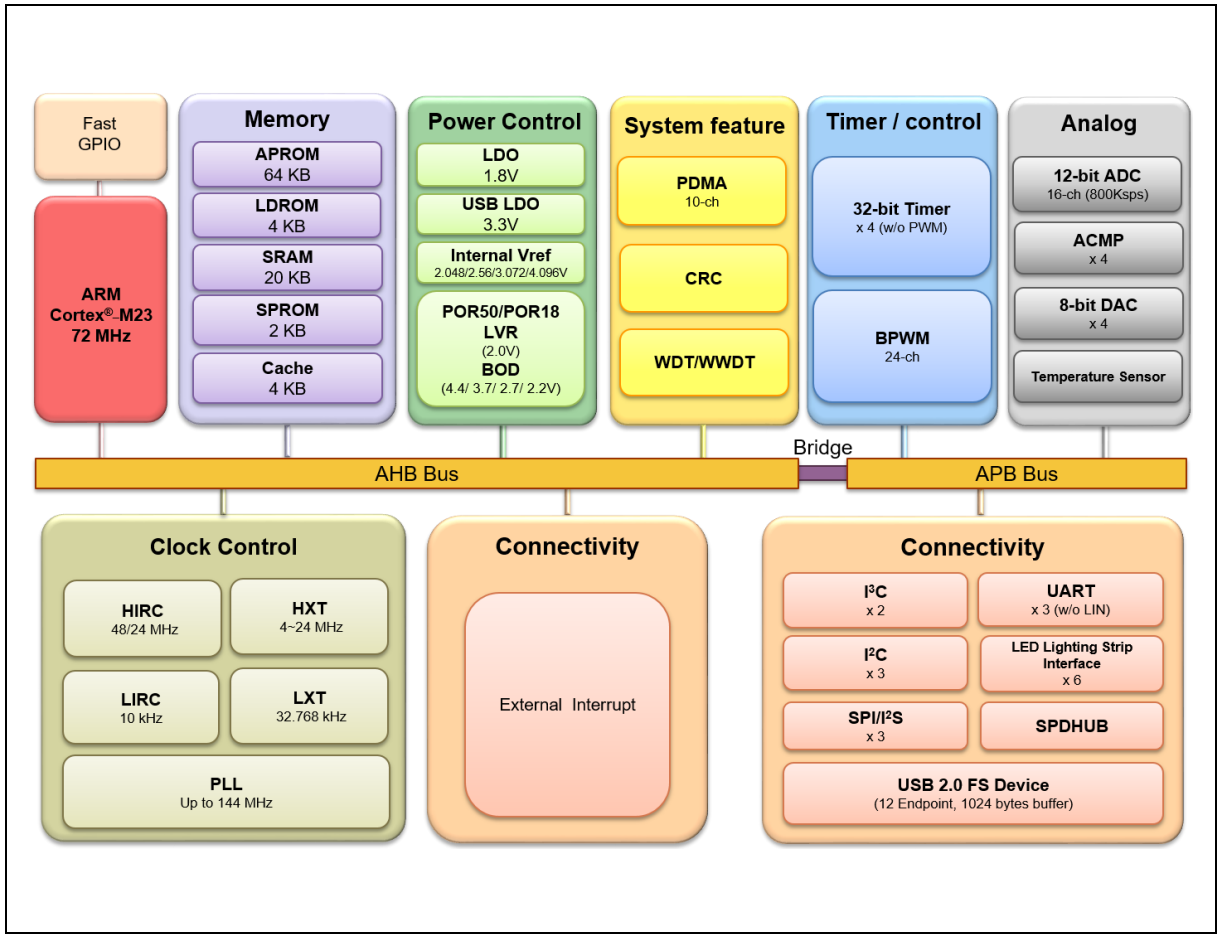


Figure 5.1-1 NuMicro NUC1263 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm Cortex-M23 Core

The Cortex-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm TrustZone technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. The NuMicro NUC1263 is embedded with Cortex-M23 processor. Figure 4.1-1 shows the functional controller of the processor.

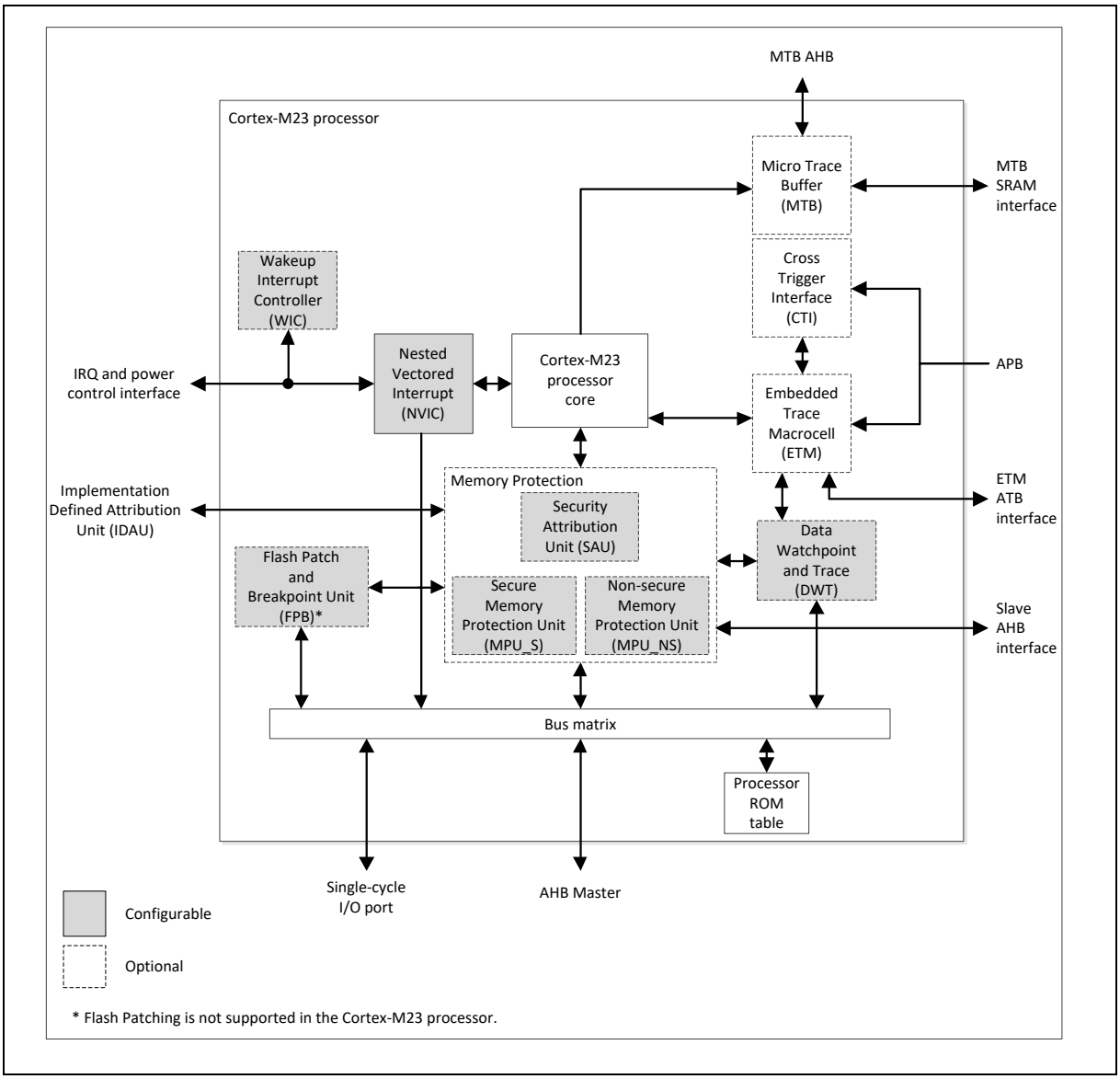


Figure 6.1-1 Cortex-M23 Block Diagram

Cortex-M23 processor features:

- Armv8-M Baseline architecture.
- Armv8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.

- Support for single-cycle I/O access.
- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex-M23 core only by writing 1 to CPURST (SYS_IPRST0[1])

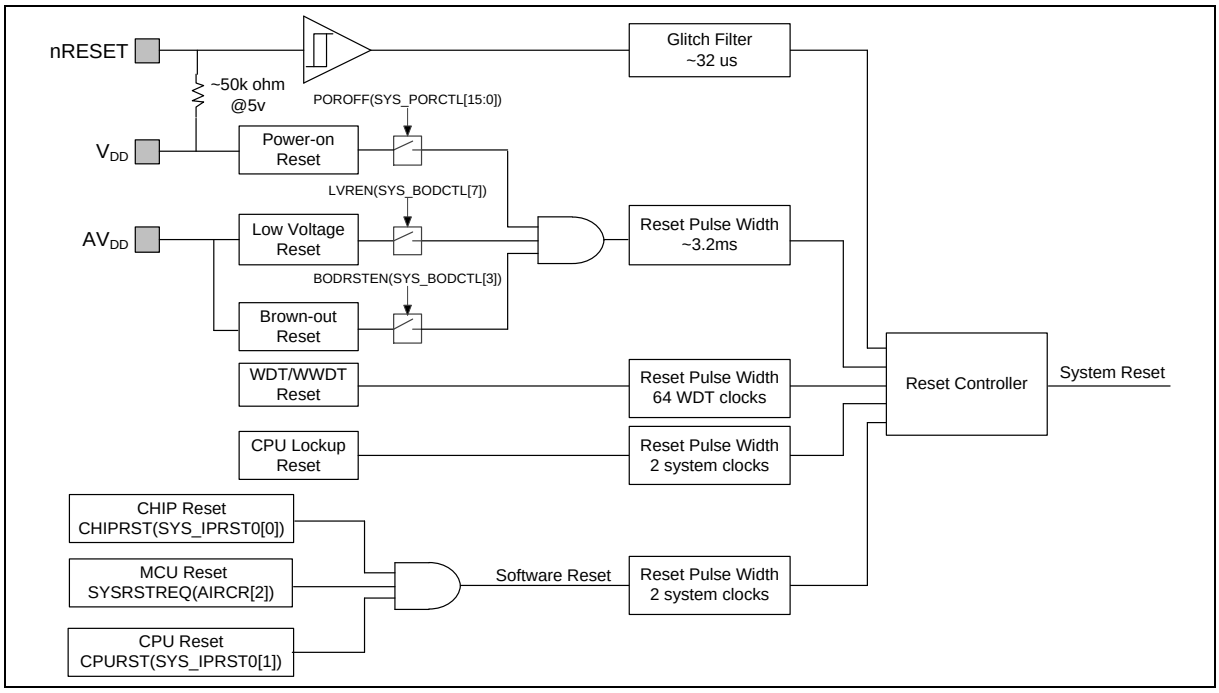


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro family. In general, CPU reset is used to reset Cortex-M23 only; the other reset sources will reset Cortex-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	0x01	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x7	0x7	0x7	0x7	0x7	0x7	0x7	0x7	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
Other Peripheral Registers	Reset Value								-
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than V_{ILR} and the state keeps longer than t_{FR} (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above V_{IHR} and the state keeps longer than t_{FR} (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

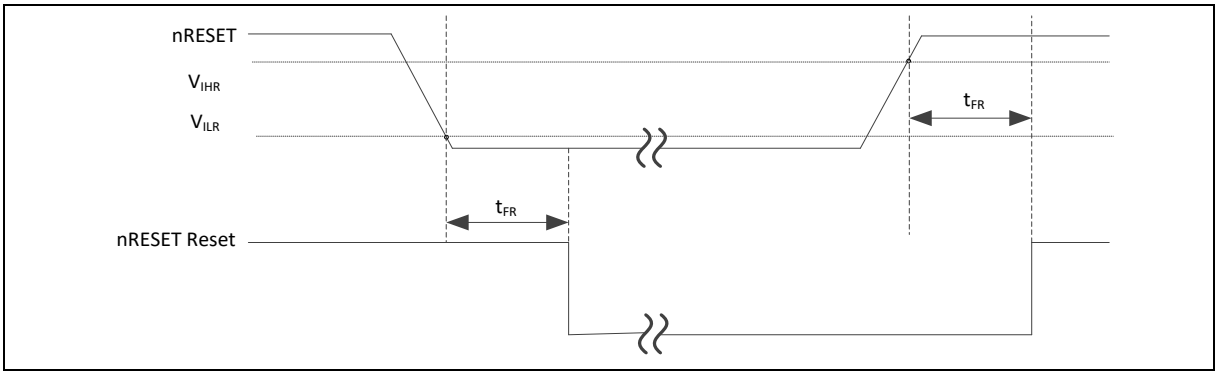


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

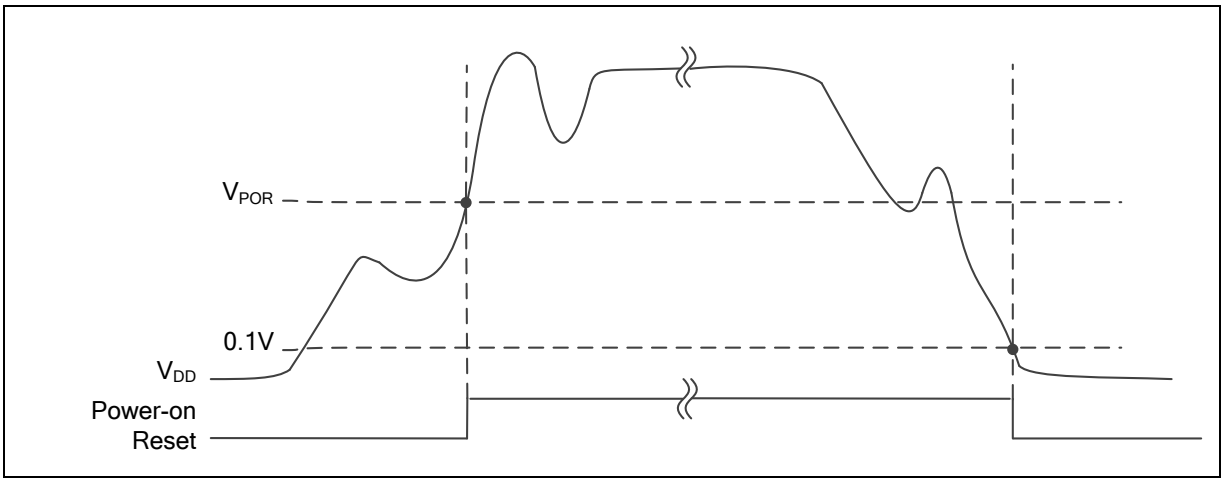


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

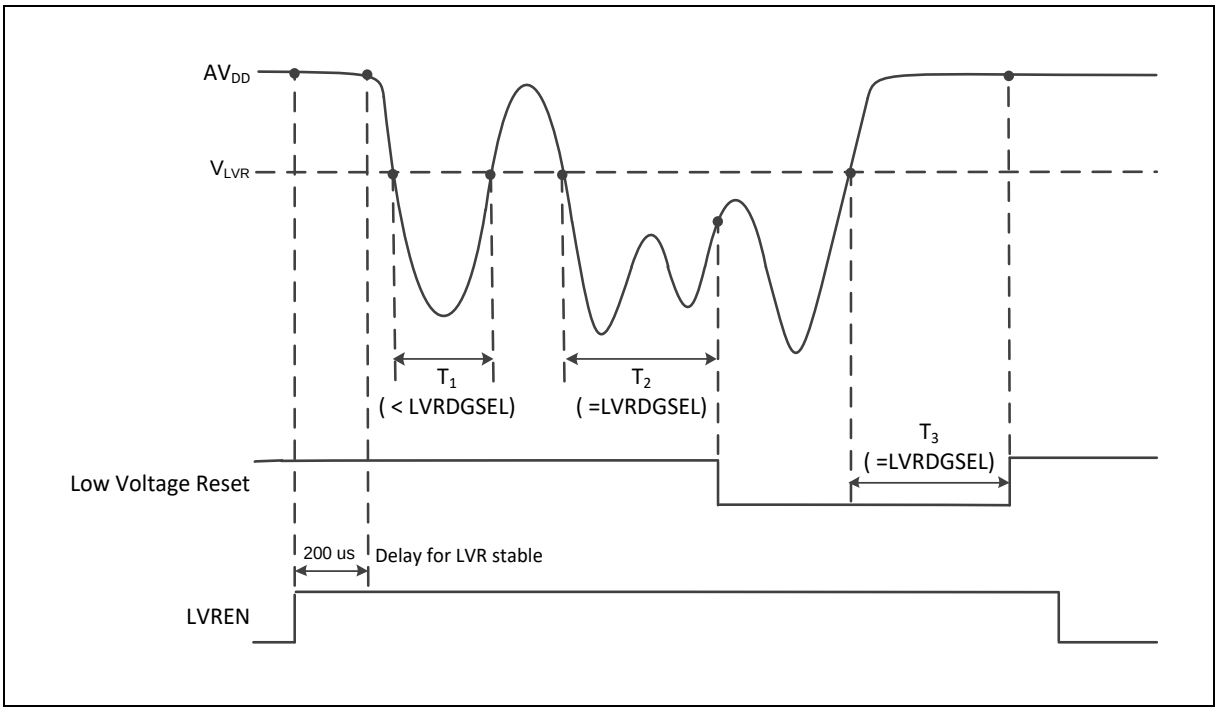


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN (SYS_BODCTL[0]) and BODVL (SYS_BODCTL[2:1]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]). The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [23]), CBOV (CONFIG0 [22:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

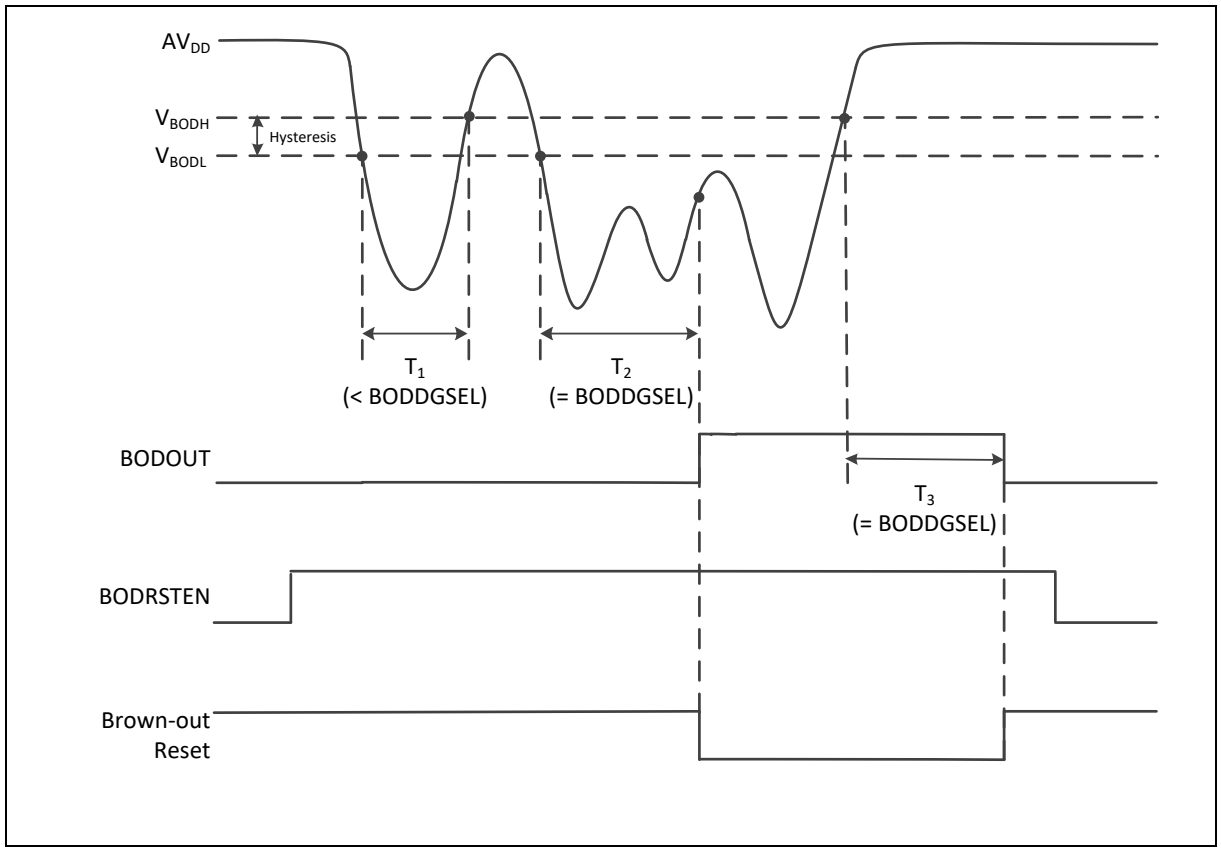


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be

reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD, GPIO, EINT, USBD, VDET, ACMP and I3CS.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table

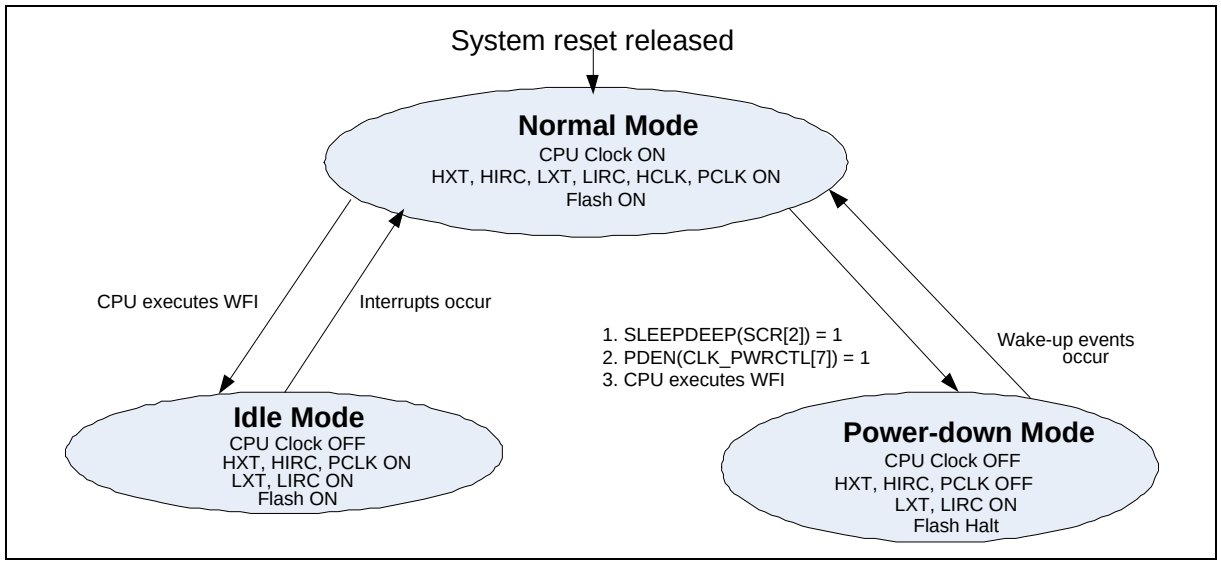


Figure 6.2-6 NuMicro NUC1263 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (10 kHz OSC) ON or OFF depends on SOFTWARE setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC/LXT and LIRC/LXT is on.
5. If UART clock source is selected as LXT and LXT is on.
6. FMC clock source ON or OFF depends on SOFTWARE setting in idle mode.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~24 MHz XTL)	ON	ON	Halt
HIRC (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON/OFF[6]	Halt
TIMER	ON	ON	ON/OFF[3]
WDT	ON	ON	ON/OFF[4]
UART	ON	ON	ON/OFF[5]
Others	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, BOD, VDET, GPIO, USBD, ACMP and I3CS.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
VDET	Voltage Detector Interrupt	After software writes 1 to clear VDETIF (SYS_BODCTL[19]).
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
UART	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
I²C	Address match wake-up	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
I3CS	Address match wake-up	The detailed wakeup limitation please refer to I3CS section.
ACMP	Comparator Power-Down Wake-Up Interrupt	After software writes 1 to clear WKIF0 (ACMP01_STATUS[8]), WKIF1 (ACMP01_STATUS[9]), WKIF0 (ACMP23_STATUS[8]) and WKIF1 (ACMP23_STATUS[9]),
USBD	1.Remote wake-up 2.Plug in wake-up	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).

Table 6.2-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Distribution

In this chip, power distribution is divided into six segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.
- I/O power from V_{DDIO0} supplies the power for PA.8 ~ PA.11 and PF.4 ~ PF.6
- I/O power from V_{DDIO1} supplies the power for PA.0 ~ PA.3
- I/O power from V_{DDIO2} supplies the power for SPDH_LSCL and SPDH_LSDA

The outputs of internal voltage regulators, LDO and USB_VDD33, require an external capacitor which

should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-7 shows the NUC1263 series power distribution.

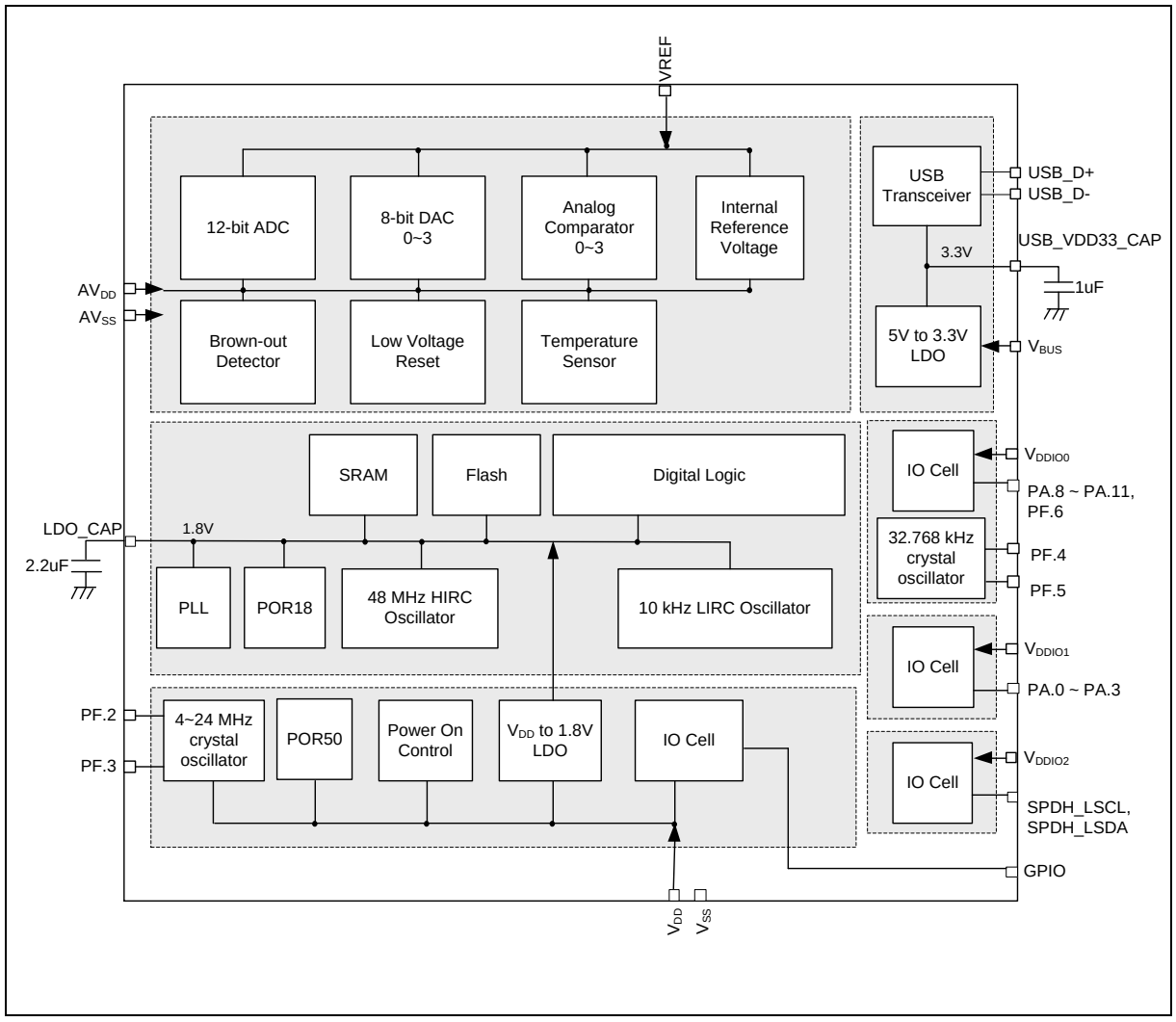


Figure 6.2-7 NuMicro NUC1263 Power Distribution Diagram

6.2.5 System Memory Map

This chip provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. This chip only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	Flash Memory Space (64 KB)
0x0001_0000 – 0x1FFF_FFFF	Reserved	Reserved
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20 Kbytes)
0x2000_5000 – 0x3FFF_FFFF	Reserved	Reserved
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_7FFF	Reserved	Reserved
0x5001_8000 – 0x5001_FFFF	CRC_BA	CRC Generator Registers
Peripheral Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	Reserved	Reserved
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I2C0 Interface Control Registers
0x4002_4000 – 0x4002_7FFF	I2C2_BA	I2C2 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	BPWM0_BA	BPWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	BPWM2_BA	BPWM2 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4005_4000 – 0x4005_41FF	LLSI0_BA	LLSI0 Control Registers
0x4005_4200 – 0x4005_43FF	LLSI2_BA	LLSI2 Control Registers
0x4005_4400 – 0x4005_45FF	LLSI4_BA	LLSI4 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x4007_0000 – 0x4007_3FFF	I3CS0_BA	I3CS0 Interface Control Registers

0x4008_0000 – 0x4008_3FFF	UART2_BA	UART2 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x400F_0000 – 0x400F_3FFF	DAC_BA	DAC Control Registers
0x4010_0000 – 0x4010_3FFF	Reserved	Reserved
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4014_0000 – 0x4014_3FFF	BPWM1_BA	BPWM1 Control Registers
0x4014_4000 – 0x4014_7FFF	BPWM3_BA	BPWM3 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_41FF	LLSI1_BA	LLSI1 Control Registers
0x4015_4200 – 0x4015_43FF	LLSI3_BA	LLSI3 Control Registers
0x4015_4400 – 0x4015_45FF	LLSI5_BA	LLSI5 Control Registers
0x4017_0000 – 0x4017_3FFF	I3CS1_BA	I3CS1 Interface Control Registers
0x401D_0000 – 0x401D_3FFF	ACMP23_BA	Analog Comparator 2/3 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-5 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Organization

This chip supports embedded SRAM with total 20 Kbytes size in one bank.

- Supports total 20 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

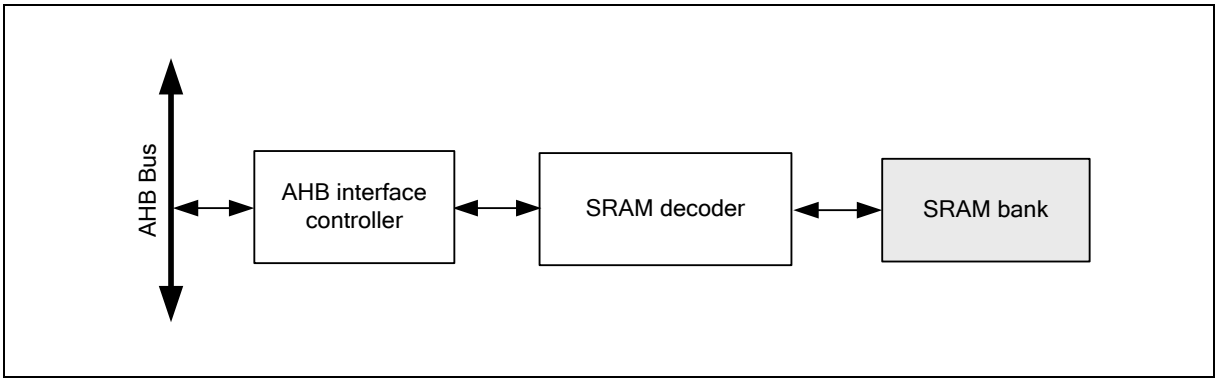


Figure 6.2-8 SRAM Block Diagram

Figure 6.2-9 shows the NUC1263 series SRAM organization. There is one SRAM bank in this chip and addressed to 20 Kbytes. The address space is from 0x2000_0000 to 0x2000_4FFF. The address between 0x2000_5000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

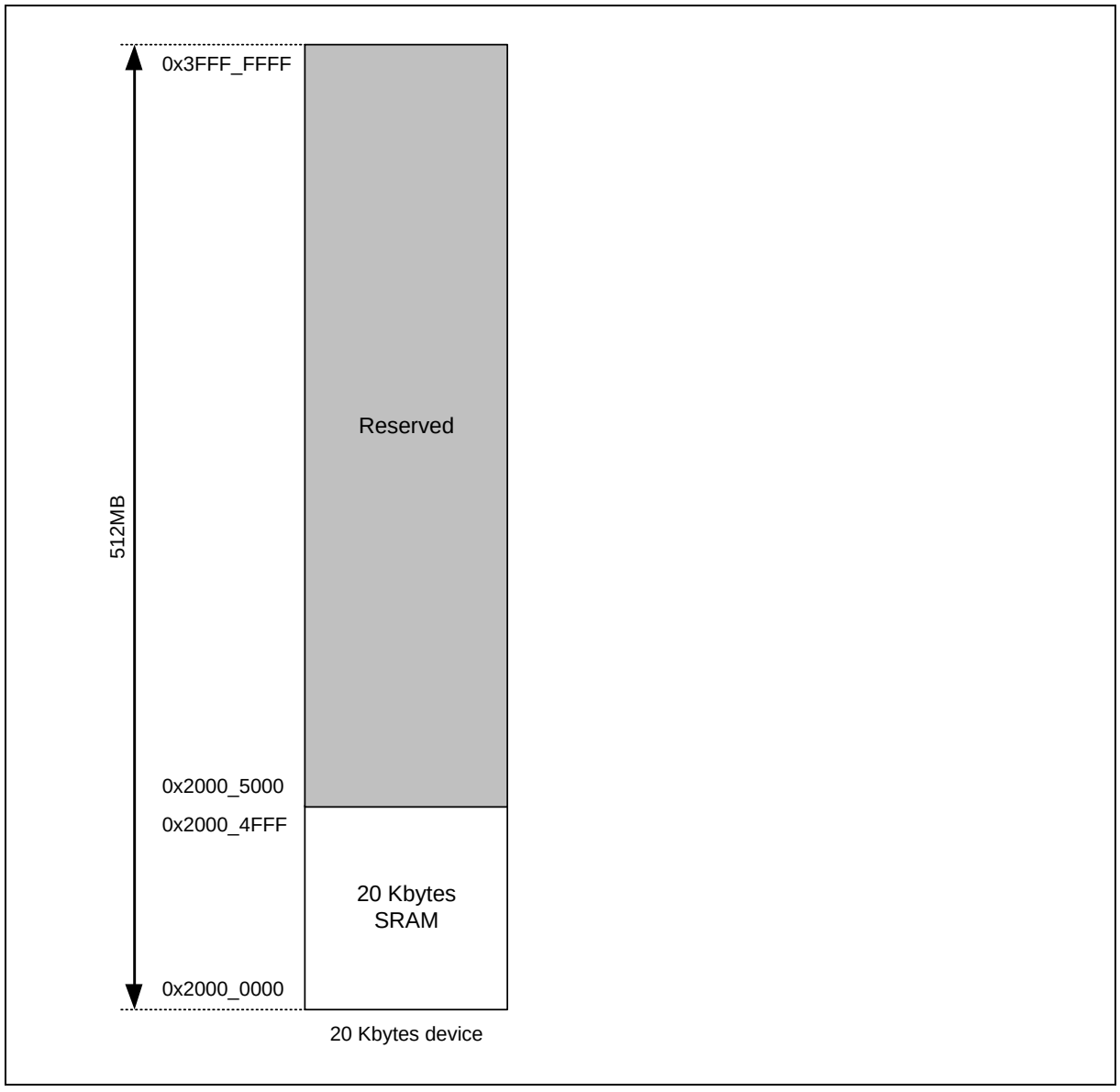


Figure 6.2-9 SRAM Memory Organization

6.2.7 Temperature Sensor

This chip is equipped with an on-chip temperature sensor. Temperature sensor control registers are located in SYS_TSCTL and SYS_TSDATA.

User should set both TSEN(SYS_TSCTL[0]) and TSBGEN(SYS_TSCTL[1]) bits to 1 to enable the temperature sensor. User needs to wait 200us for temperatre sensor to be stable, and then set TSST(SYS_TSCTL[2]) bit to 1 to start temperature sensor conversion.

After temperature sensor conversion is finished, TSEOC(SYS_TSDATA[0]) bit will be set to 1 automatically, and TSDATA(SYS_TSDATA[27:16]) will present the temperature sensor data. Figure 6.2-10 shows the timing waveform of temperature sensor conversion.

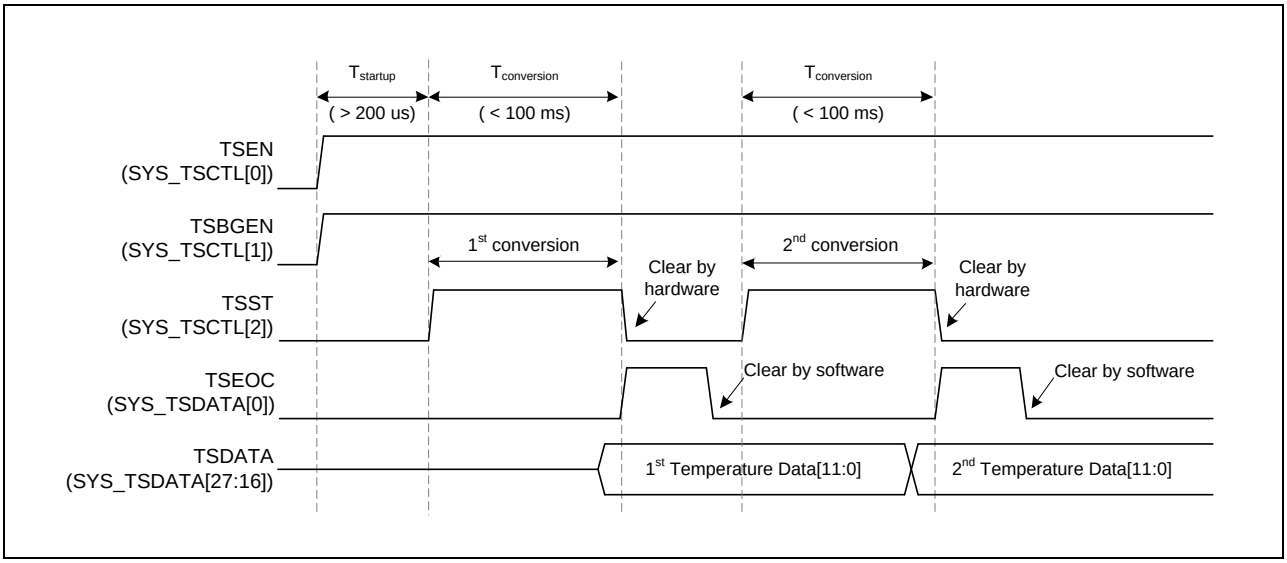


Figure 6.2-10 Temperature Sensor Conversion Waveform

Table 6.2-6 is a reference table for the relationship between temperature and TSDATA. Negative temperature is represented in TSDATA(SYS_TSDATA[27:16]) by two's complement format, and per LSB difference is equivalent to 0.0625 ° C.

Temperature (°C)	Temperature Data (TSDATA)
128	0x7FF
127.9375	0x7FF
100	0x640
80	0x500
75	0x4B0
50	0x320
25	0x190
0.25	0x004
0	0x000
-0.25	0xFFC
-25	0xE70

-55	0xC90

Table 6.2-6 Temperature Data Truth Table

6.2.8 Register Lock

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x5000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check the protection disable bit at address 0x5000_0100 bit0, 1 is protection disable, and 0 is protection enable. Then user can update the target protected register value and then write any data to the address “0x5000_0100” to enable register protection.

6.2.9 Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 48 MHz clock. In such case, if users do not want to use PLL as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL [1:0] trim frequency selection) to “01”, set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “0”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

Another example is that the system needs an accurate 48 MHz clock for USB application. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL [10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL [1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

HIRC trim can only work properly when the clock sources are stable. When the RC clock or the reference clock is not stable or the system goes into power down, HIRC trim needs to wait until the clock is stable or system wakes up, and then it can be enabled or will get a clock error flag.

6.2.10 Internal V_{REF}

This chip supports internal V_{REF} function, depend on setting of VREFCTL(SYS_VREFCTL[4:0]) to generate different reference voltage for ADC/DAC/ACMP. User has to enable PRELOADEN (SYS_VREFCTL[6]) to fit the Tstable when VREFCTL(SYS_VREFCTL[4:0]) change setting (except set to 00000) to make sure that V_{REF} works well. Tstable depends on different situations has different requirement, please refer to the relative Datasheet.

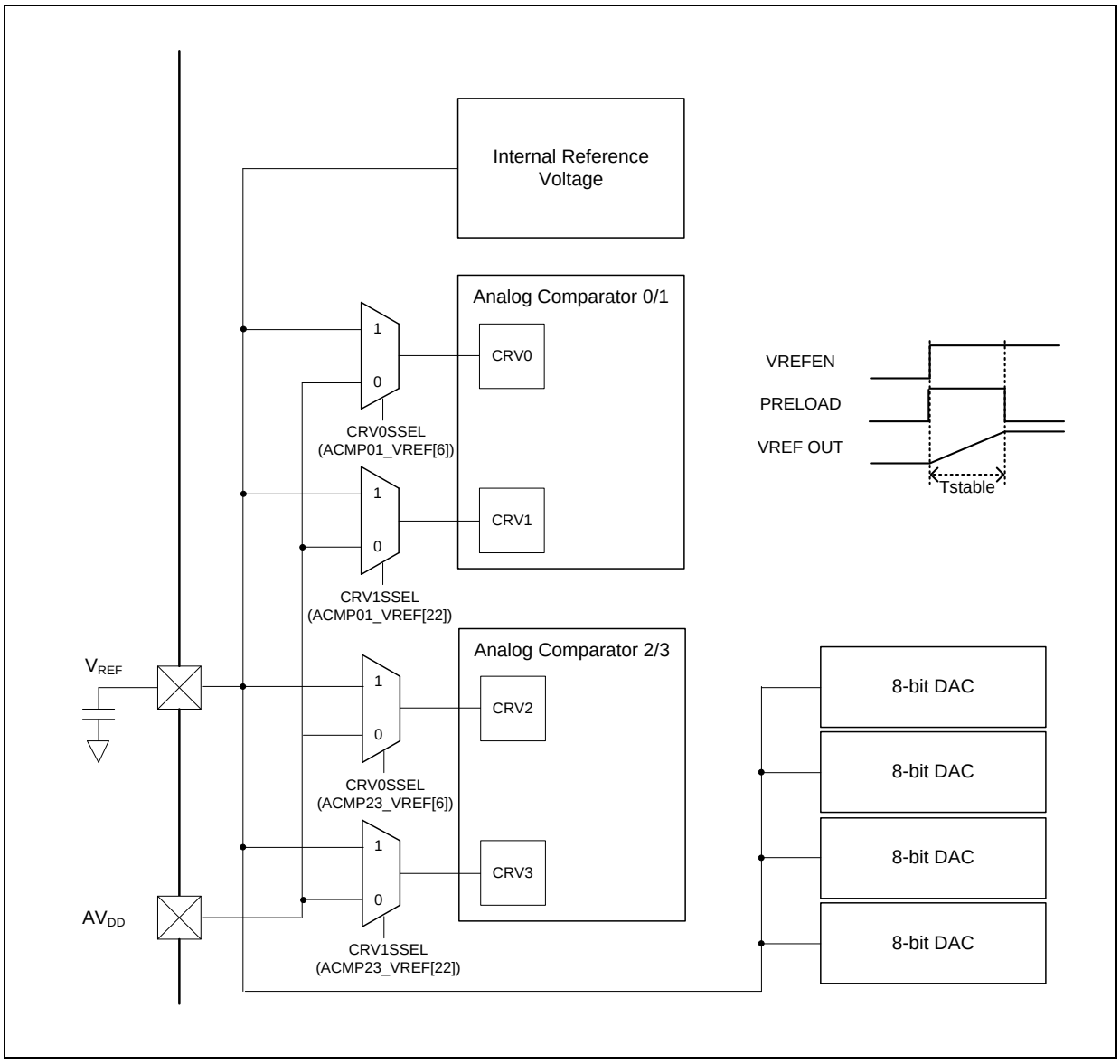


Figure 6.2-11 NuMicro NUC1263 V_{REF} Diagram

6.2.11 UART1_TXD Modulation with BPWM

This chip supports UART1_TXD to modulate with BPWM channel. User can set MODPWMSEL(SYS_MODCTL[6:4]) to choose which BPWM0 channel to modulate with UART1_TXD and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART1_TXD before modulating with BPWM.

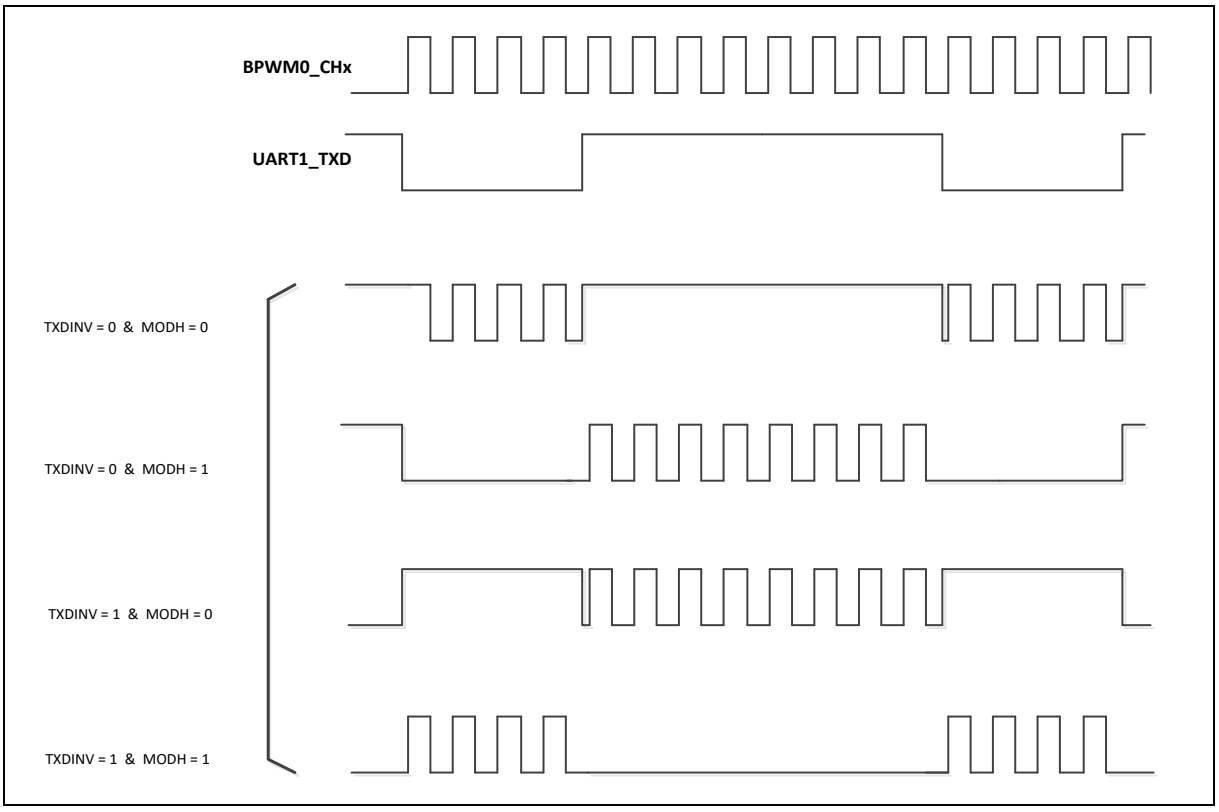


Figure 6.2-12 UART1_TXD Modulated with BPWM Channel

6.2.12 Voltage Detector (VDET)

This chip supports low power comparator to detect external voltage. User can control Band-gap active interval and comparator active interval to achieve low power detection purpose. There is no debounce function in Power-down mode since no HCLK is available in Power-down mode.

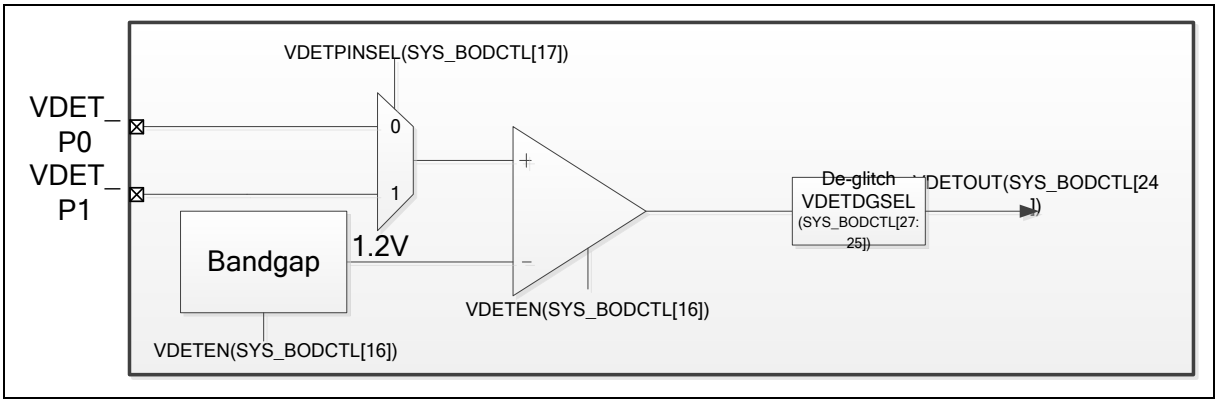


Figure 6.2-13 VDET Block Diagram

6.2.13 SPI Mux for SPI1 Master and External SPI Master

This chip supports an internal multiplexer on SPI1 master output to switch between SPI1 master signals and an external feed-through SPI master signals into one set of SPI pins to access a SPI slave. User can set the multi-function pin to SPI_SS_MUX, SPI_CLK_MUX, SPI_MISO_MUX, and SPI_MOSI_MUX to activate this function. Before enabling SPI multiplexor function, SPI1 master occupys SPI1 related pins. After enabling SPI multiplexer function, SPI_SS_MUX pin decides which SPI master can traverse through the multiplexer to access the target SPI slave. When SPI_SS_MUX is low, the multiplexor chooses external SPI master; on the contrary, when SPI_SS_MUX is high, the multiplexor chooses SPI1 master. User can also set MUXSWEN (SYS_SPIMUX[0]) to enable software control method. After MUXSWEN is set, SPI_SS_MUX can no longer control the multiplexer; instead, the multiplexer is controlled by MUXSWSEL (SYS_SPIMUX[1]) setting.

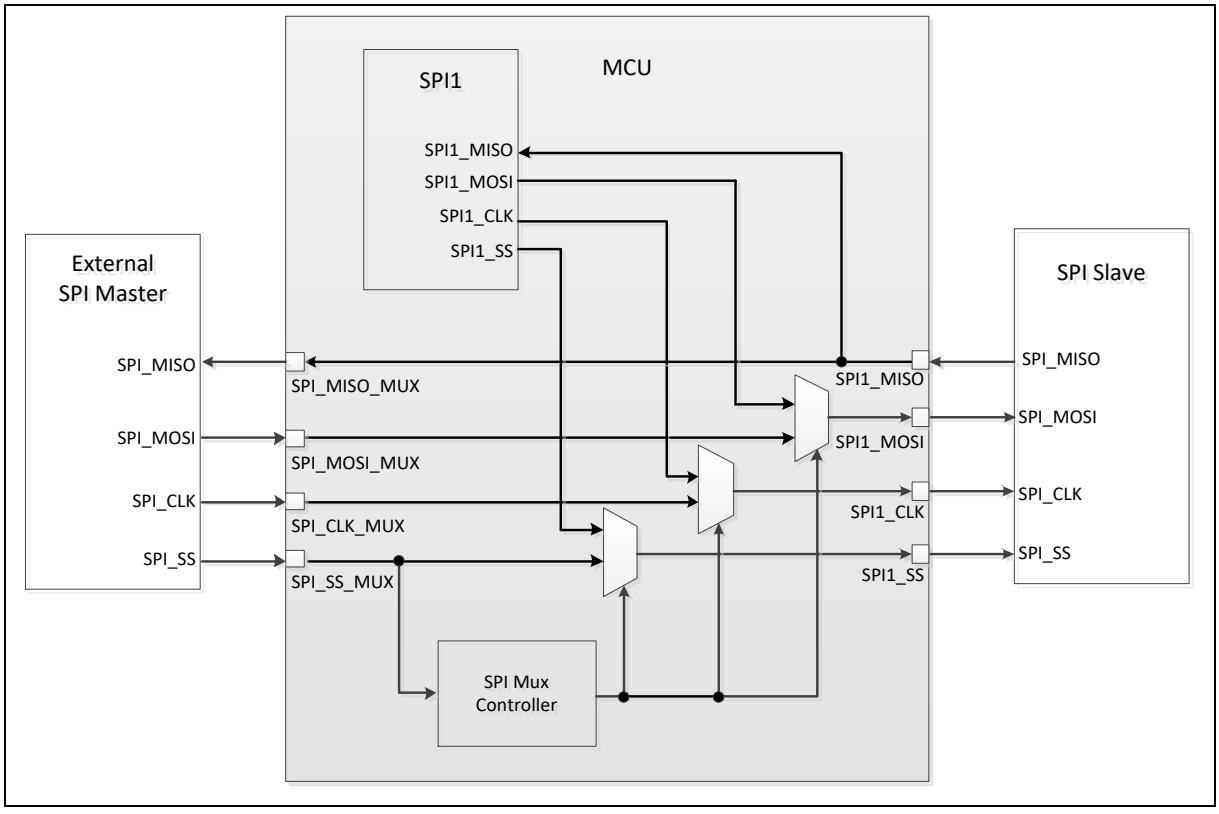


Figure 6.2-14 SPI Mux Diagram

6.2.14 System Timer (SysTick)

The Cortex-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm Cortex-M23 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

6.2.15 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-50 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.

6.2.15.1

- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

Exception Model and System Interrupt Map

Table 6.2-7 lists the exception model supported by the NUC1263 series. Software can set 4 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0x00" and the lowest priority is denoted as "0xC0" (The 6-LSB always 0). The default priority of all the user-configurable interrupts is "0x00". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

When any interrupts is accepted, the processor will automatically fetch the starting address of the

interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80.

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Reserved	4~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Reserved	12~13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ49)	16 ~ 65	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-7 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BOD_INT	Brown-out low voltage detected interrupt
17	1	WDT_INT	Watchdog Timer interrupt
18	2	EINT024	External interrupt from INT0/INT2/INT4 pin
19	3	EINT135	External interrupt from INT1/INT3/INT5 pin
20	4	GPAB_INT	External signal interrupt from PA[11:0]/PB[15:0]
21	5	GPCDF_INT	External interrupt from PC[7:0]/PC[14]/PD[3:0]/PD[15]/PF[6:0
22	6	BPWM0_INT	BPWM0 interrupt
23	7	BPWM1_INT	BPWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART0_INT	UART0 interrupt
29	13	UART1_INT	UART1 interrupt

30	14	SPI0_INT	SPI0 interrupt
31	15	SPI1_INT	SPI1 interrupt
32	16	BPWM2_INT	BPWM2 interrupt
33	17	BPWM3_INT	BPWM3 interrupt
34	18	I2C0_INT	I2C0 interrupt
35	19	I2C1_INT	I2C1 interrupt
36	20	I2C2_INT	I2C2 interrupt
37	21		Reserved
38	22		Reserved
39	23	USBD_INT	USB Device interrupt
40	24		Reserved
41	25	ACMP01_INT	ACMP01 interrupt
42	26	PDMA_INT	PDMA interrupt
43	27		Reserved
44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from Power-down state
45	29	ADC_INT	ADC interrupt
46	30	CLKDIRC_INT	Clock fail detect and IRC TRIM interrupt
47	31		Reserved
48	32	LLSI0_INT	LED Lighting Strip Interface 0 interrupt
49	33	LLSI1_INT	LED Lighting Strip Interface 1 interrupt
50	34	LLSI2_INT	LED Lighting Strip Interface 2 interrupt
51	35	LLSI3_INT	LED Lighting Strip Interface 3 interrupt
52	36	LLSI4_INT	LED Lighting Strip Interface 4 interrupt
53	37	LLSI5_INT	LED Lighting Strip Interface 5 interrupt
54	38		Reserved
55	39		Reserved
56	40		Reserved
57	41		Reserved
58	42	SPI2_INT	SPI2 interrupt
59	43	UART2_INT	UART2 interrupt
60	44	I3CS0_INT	I3CS0 interrupt
61	45	I3CS1_INT	I3CS1 interrupt
62	46	DAC_INT	DAC interrupt
63	47	ACMP23_INT	ACMP23 interrupt
64	48	TS_INT	Temperature sensor interrupt

Table 6.2-8 Interrupt Number Table

Operation Description

6.2.15.2

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in the next section.

NVIC Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address: **NVIC_BA = 0xE000_E100**				
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000
NVIC_ISER1	NVIC_BA+0x004	R/W	IRQ32 ~ IRQ49 Set-enable Control Register	0x0000_0000
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000
NVIC_ICER1	NVIC_BA+0x084	R/W	IRQ32 ~ IRQ49 Clear-enable Control Register	0x0000_0000
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ32 ~ IRQ49 Set-pending Control Register	0x0000_0000
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ32 ~ IRQ49 Clear-pending Control Register	0x0000_0000
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ32 ~ IRQ49 Active Bit Register	0x0000_0000
NVIC_IPRn **n=0,1..15**	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ49 Priority Control Register	0x0000_0000

6.2.15.3

IRQ0 ~ IRQ31 Set-enable Control Register (NVIC_ISER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER1 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ31 ~ IRQ49 Set-enable Control Register (NVIC_ISER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER1	NVIC_BA+0x004	R/W	IRQ32 ~ IRQ49 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER1 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Clear-enable Control Register (NVIC_ICER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER1 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ32 ~ IRQ49 Clear-enable Control Register (NVIC_ICER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER1	NVIC_BA+0x084	R/W	IRQ32 ~ IRQ49 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER2 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR1 registers force interrupts into the pending state, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ32 ~ IRQ49 Set-pending Control Register (NVIC_ISPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ32 ~ IRQ49 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR1 registers force interrupts into the pending state, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR1 registers remove the pending state from interrupts, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ32 ~ IRQ49 Clear-pending Control Register (NVIC_ICPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ32 ~ IRQ49 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR1 registers remove the pending state from interrupts, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR1 registers indicate which interrupts are active. 0 = interrupt not active. 1 = interrupt active.

IRQ32 ~ IRQ49 Active Bit Register (NVIC_IABR1)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ32 ~ IRQ49 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR1 registers indicate which interrupts are active. 0 = interrupt not active. 1 = interrupt active.

IRQ0 ~ IRQ49 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn **n=0,1..15**	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ49 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_4n_2		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_4n_1		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4n_0		**Reserved**					

Bits	Description	
[31:30]	**PRI_4n_3**	**Priority of IRQ_4n+3** “0” denotes the highest priority and “3” denotes the lowest priority
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_4n_2**	**Priority of IRQ_4n+2** “0” denotes the highest priority and “3” denotes the lowest priority
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_4n_1**	**Priority of IRQ_4n+1** “0” denotes the highest priority and “3” denotes the lowest priority
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_4n_0**	**Priority of IRQ_4n+0** “0” denotes the highest priority and “3” denotes the lowest priority
[5:0]	**Reserved**	Reserved.

6.2.16 System Control

The Cortex-M23 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex-M23 interrupt priority and Cortex-M23 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm Cortex-M23 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M23 core executes the WFI instruction. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

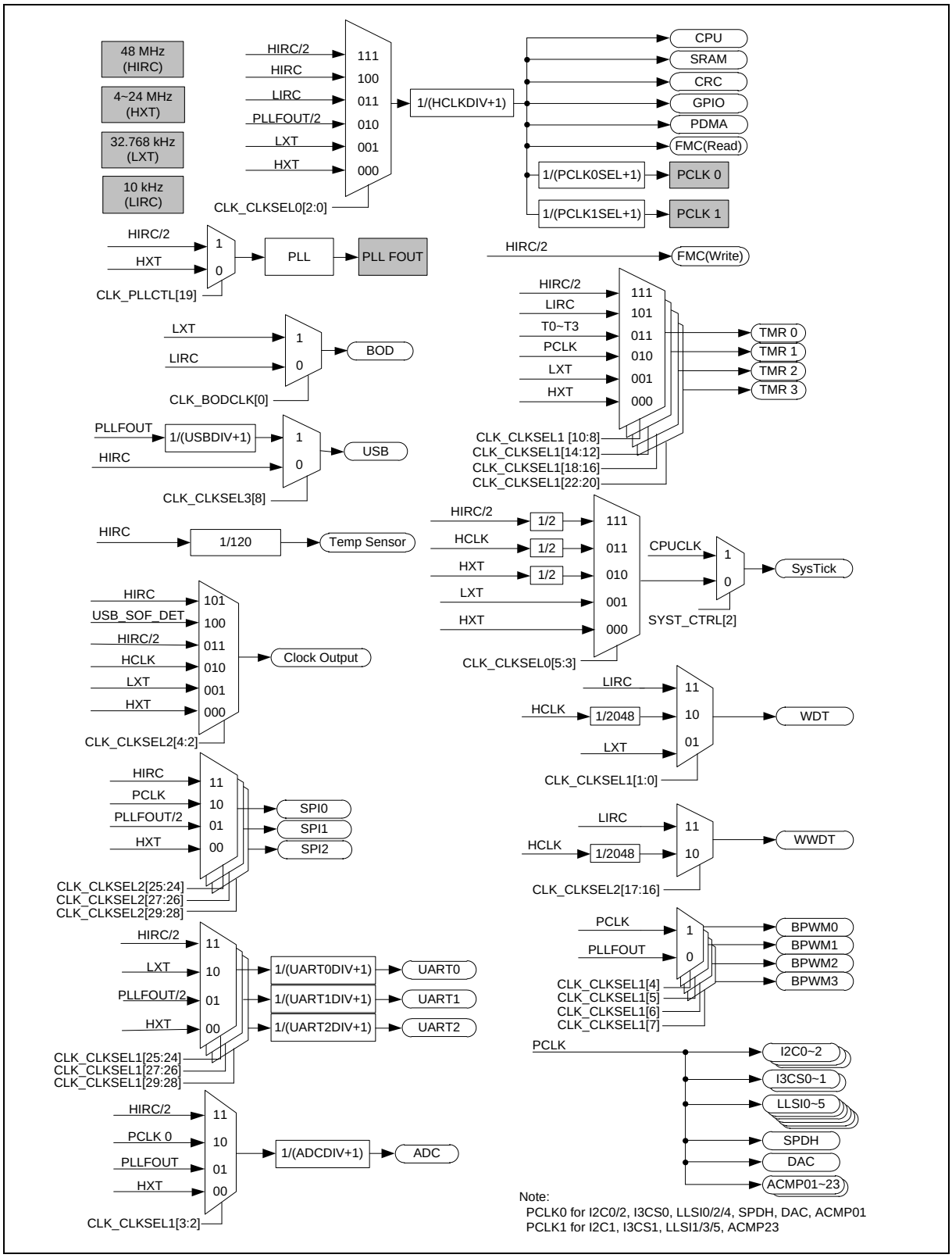


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

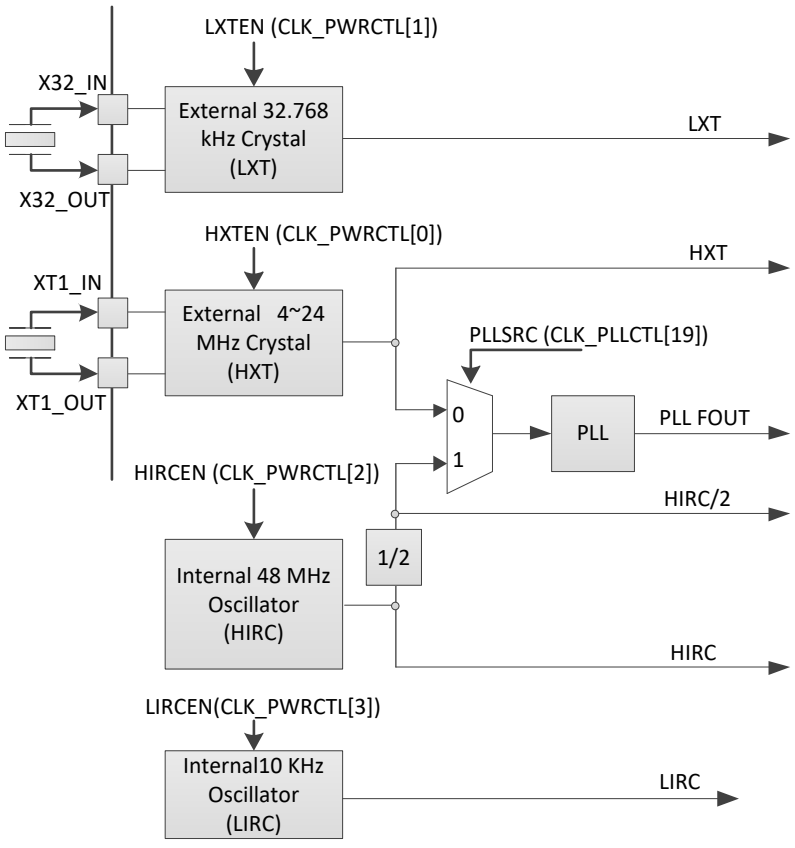
The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low-speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator divided by 2 (HIRC/2)
- 48 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter starts counting and correlated clock stable index (HIRCSTB(CLK_STATUS[4]), LIRCSTB(CLK_STATUS[3]), PLLSTB(CLK_STATUS[2]), LXTSTB(CLK_STATUS[1]) and HXTSTB(CLK_STATUS[0]) are set to 1 after stable counter value reaches a define value as shown in Table 6.3-1. System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will automatically cleared when user disables the clock source (LIRCEN(CLK_PWRCTL[3]), HIRCEN(CLK_PWRCTL[2]), HXTEN(CLK_PWRCTL[0]), PD(CLK_PLLCTL[16]) and LXTEN(CLK_PWRCTL[1])). Besides, the clock stable index of HXT, HIRC and PLL will be automatically cleared when chip enters power-down and clock stable counter will re-count after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clock	341.33 uS for 12 MHz
PLL	It's based on the value of STBSEL (CLK_PLLCTL[23]) STBSEL = 0, stable count is 6144 clocks of PLL clock source. STBSEL = 1, stable count is 12288 clocks of PLL clock source. (Default)	STBSEL = 0, 512 uS for 12 MHz STBSEL = 1, 1024 uS for 12 MHz
HIRC	512 HIRC clock	10.67 uS for 48 MHz
LIRC	1 LIRC clock	100 uS for 10 kHz
LXT	16384 LXT clock	500mS for 32.768 kHz

Table 6.3-1 Clock Stable Count Value Table

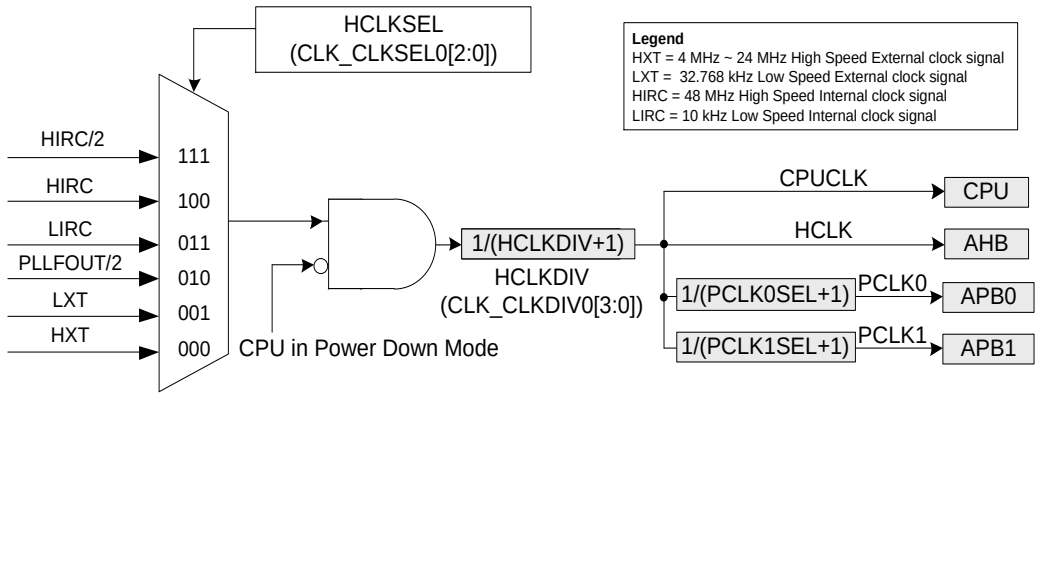


Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 6 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0 [2:0]). The block diagram is shown in Figure 6.3-3.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will automatically switch to HIRC/2 if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. HXT clock source stable flag, HXTSTB (CLK_STATUS[0]), will be cleared if HXT stops when using HXT fail detector function. User can try to recover HXT by disabling HXT and enabling HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recovered to oscillate after re-enable action and user can switch system clock to HXT again.

When LXT clock detector is enabled, the system clock will automatically switch to LIRC if LXT clock stops being detected on the following condition: system clock source comes from LXT. If LXT clock stop condition is detected, the LXTFIF (CLK_CLKDSTS[1]) is set to 1 and chip will enter interrupt if LXTFIE (CLK_CLKDCTL[5]) is set to 1. LXT clock source stable flag, LXTSTB (CLK_STATUS[1]), will be cleared if LXT stops when using LXT fail detector function. User can try to recover LXT by disabling LXT and enabling LXT again to check if the clock stable bit is set to 1 or not. If LXT clock stable bit is set to 1, it means LXT is recovered to oscillate after re-enable action and user can switch system clock to LXT again.

The HXT clock stop detect and system clock switch to HIRC/2 procedure is shown in Figure 6.3-4.

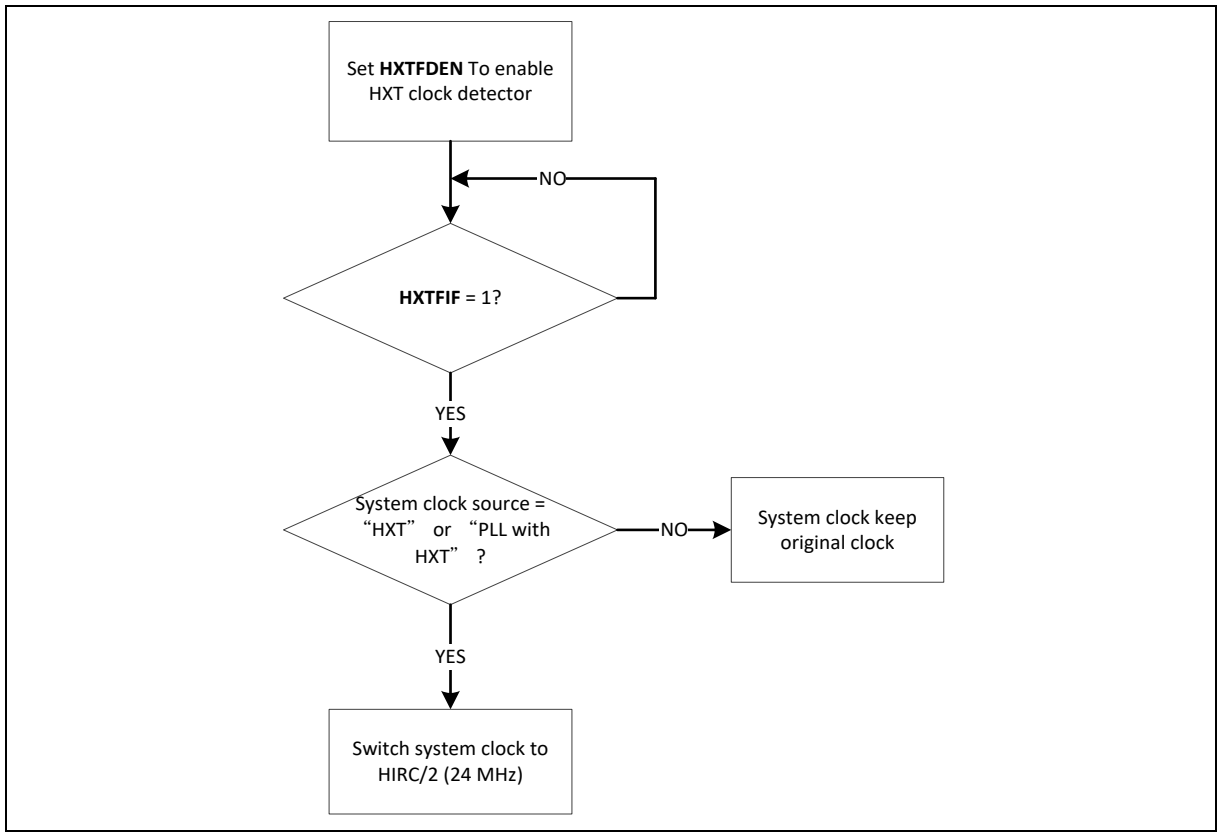


Figure 6.3-4 HXT Stop Protect Procedure

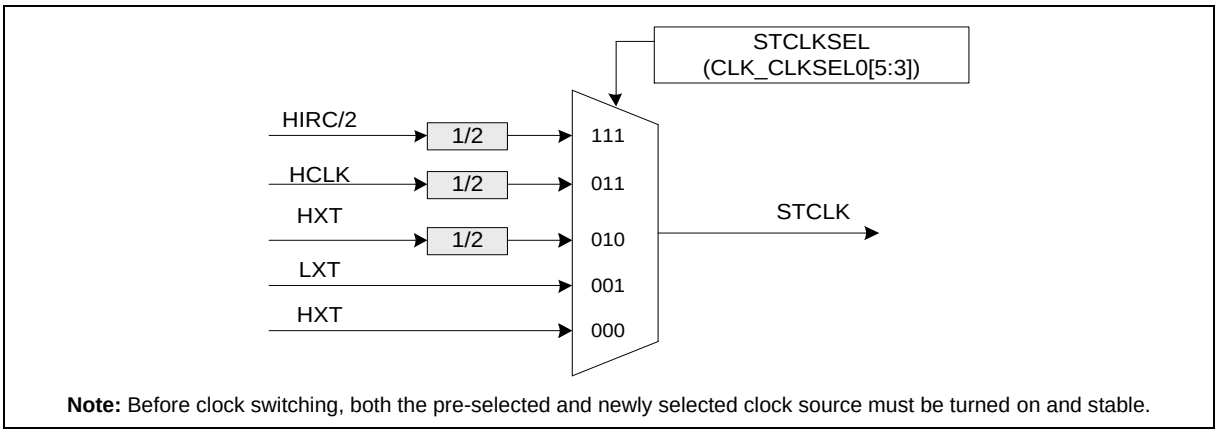
Besides, user can also monitor HXT CLK frequency range by HIRC clock. User can set UPERBD (CLK_CDUPB[9:0]) and LOWERBD (CLK_CDLOWB[9:0]) to decide monitoring frequency window. If target clock speed is greater than UPERBD or less than LOWERBD, the HXT Clock Frequency Range Detector Interrupt Flag HXTFQIF(CLK_CLKDSTS[8]) will be set to 1.

The formula of UPERBD and LOWERBD is listed below.

HIRC_period* 1024 < HXT_period* UPERBD

HIRC_period* 1024 > HXT_period* LOWERBD

The clock source of SysTick in Cortex-M23 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 description in Register Description section.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources, and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low-speed RC oscillator (LIRC) clock
  - 32.768 kHz external low-speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

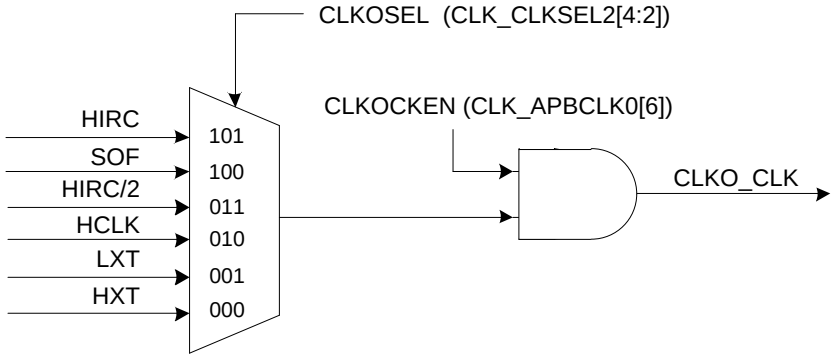
This device is equipped with a power-of-2 frequency divider composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

If DIVI1EN(CLK_CLKOCTL[5]) is set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The clock output clock will be output to CLKO pin directly.

When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-6 Clock Source of Clock Output

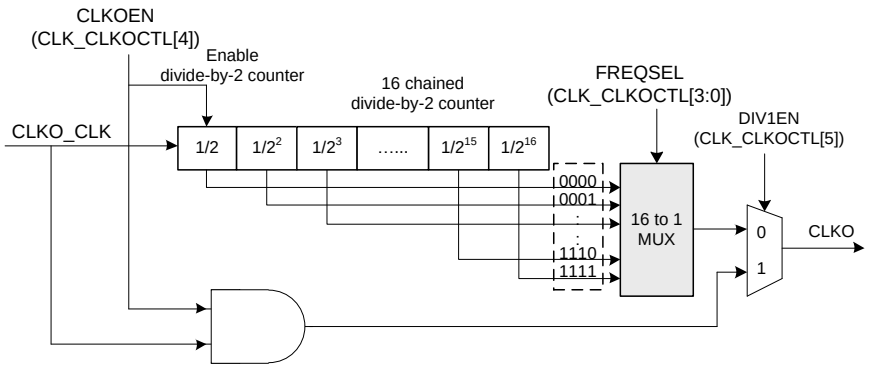


Figure 6.3-7 Clock Output Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

This chip is equipped with 64 Kbytes on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. An User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 2 Kbytes security protection ROM (SPROM) can conceal user program. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded Flash updated.

6.4.2 Features

- Supports 64 Kbytes application ROM (APROM).
- Supports 4 Kbytes loader ROM (LDROM).
- Supports 2 Kbytes security protection ROM (SPROM) to conceal user program.
- Supports Data Flash with configurable memory size.
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 2 Kbytes page erase for all embedded Flash.
- Supports 32-bit/64-bit and multi-word Flash programming function.
- Supports CRC-32 checksum calculation function.
- Supports Flash all one verification function.
- Supports embedded SRAM remap to system vector memory.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.
- Supports cache memory to improve Flash access performance and reduce power consumption.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 49 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 49 pins are arranged in 5 ports named as PA, PB, PC, PD, and PF. PA has 12 pins on port. PB has 16 pins on port. PC has 9 pins on port. PD has 5 pins on port. PF has 7 pins on port. Each of the 49 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]).

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in input tri-state mode after chip reset
  - CIOIN = 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- Supports independent pull-up control
- Enabling the pin interrupt function will also enable the wake-up function

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 10 channels and each channel can perform transfer between memory and peripherals or between memory and memory. The PDMA supports time-out function for channel 0 and channel 1.

6.6.2 Features

- Supports 10 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI/I^2S, UART, I^2C, I3CS, ADC, DAC, LLSI and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function for channel0 and channel 1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports internal capture triggered while LIRC transition
- Internal capture triggered source from ACMP output.
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger ADC, DAC, PDMA, BPWM function
- Supports Inter-Timer trigger mode

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- Supports 18-bit free running up counter
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK is 10 kHz
- Supports selectable WDT reset delay period between WDT time-out event to WDT reset system event, and it includes 1026, 130, 18 or 3 * WDT_CLK delay period
- System kept in reset state about 63 * WDT_CLK period time after system reset event occurred
- Supports to force WDT function enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset while WWDT counter is not reloaded within a specified window period when application program runs to uncontrollable status by any unpredictable condition.

6.9.2 Features

- Supports 6-bit down counter value CNTDAT (WWDT_CNT[5:0]) and maximum 6-bit compare value CMPDAT (WWDT_CTL[21:16]) to adjust the WWDT compare time-out window period flexibly
- Supports PSCSEL (WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode
- WWDT counter only can be reloaded within the valid window period to prevent system reset

6.10 Basic PWM Generator and Capture Timer (BPWM)

6.10.1 Overview

The chip provides four BPWM generators — BPWM0, BPWM1, BPWM2 and BPWM3. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.10.2 Features

6.10.2.1 BPWM Function Features

- Supports maximum clock frequency up to 144 MHz frequency
- Supports up to four BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up-down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger ADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.10.2.2 Capture Function Features

- Supports up to 24 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.11 UART Interface Controller (UART)

6.11.1 Overview

This chip provides three channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports nine types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR and RS-485 function modes and auto-baud rate measuring function.

6.11.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. This chip contains up to three sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device.

This controller also supports the PDMA function to access the data buffer. The SPI controller also support I^2S mode to connect external audio CODEC.

6.12.2 Features

- SPI Mode
  - Up to three sets of SPI controllers
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports PDMA transfer

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are three sets of I²C controllers that support Power-down wake-up function.

6.13.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to three I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

6.14 I3C Slave Serial Interface Controller (I3CS)

6.14.1 Overview

I3C is a two-wire bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The Improved Inter Integrated Circuit (I3C) is part of a group of communication protocols defined by the MIPI Alliance. This specification is developed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.

The I3CS controller meets the requirement of I3C protocol and I^2C protocol as specified by the MIPI I3C Specification v1.0.

6.14.2 Features

The I3C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I3CS controller include:

- Supports up to two I3C ports
- Supports Slave mode only
- Supports 7-bit addressing mode
- Static or Dynamic Slave Device support
- Built-in Hardware Dynamic Address Allocation support (ENTDAA/SETDASA)
- Built-in CCC transfer handler
- Auto Hot-Join request generation support
- In-Band Interrupt request generation support
- Adaptive mode of operation between I^2C and I3C depending on I3C bus traffic
- Built-in S0-S5 Error Handling
- Supports Power-down wake-up function
- Supports PDMA mode for data transfer
- Supports SDR mode, data rates up to 12.5 Mbps
- Supports HDR-DDR mode, data rates up to 25 Mbps

6.15 USB 2.0 Full-Speed Device Controller (USBD)

6.15.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver with BC1.2 in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are six different interrupt events in this controller. They are no-event-wake-up, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, etc., BUS events, such as suspend and resume, etc., SOF events, start of frame at every 1ms and BC12 events, such as V_{BUS} attach in VBUSOK state. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurred, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurred in this endpoint.

A software-disconnect function is supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, the host will enumerate the USB device again.

Battery Charging 1.2 protocol is also supported in this USB controller. It executes V_{BUS} detect, DCD detect, PD (primary detect) and SD (secondary detect) through BCDC register. Status in BCDC will tell users what port is connected.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.15.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 6 different interrupt events (SOF, NEVWK, VBUSDET, USB , BUS and BC12)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3ms
- Supports USB 2.0 Link Power Management (LPM)
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbytes buffer size
- Provides remote wake-up capability
- Supports Battery charging 1.2 (BC12) with interrupt event (BCD)

6.16 CRC Controller (CRC)

6.16.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.16.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to program DATA (CRC_DAT[31:0]) to perform CRC operation

6.17 LED Light Strip Interface (LLSI)

6.17.1 Overview

The LLSI is a RGB LED strip controller that can convert the RGB data for hundreds of LEDs per strip into T0 and T1 code output. There are six sets of LLSI that can be used.

6.17.2 Features

- 6 sets of LLSI channels with IDLE polarity control
- Each LLSI has 4x32-bit TX FIFO
- Configurable transfer period and frame reset length
- Configurable T0H and T1H duty cycle
- Supports RGB and GRB output format
- Supports Software mode and PDMA base mode transfer

6.18 Analog-to-Digital Converter (ADC)

6.18.1 Overview

This chip contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with eight input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin STADC (PC.1/PF.5), timer0~3 overflow pulse trigger and BPWM trigger.

6.18.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog input channels or differential analog input channels
- Maximum ADC peripheral clock frequency is 20 MHz
- Up to 800 KSPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - BPWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- One internal channel for band-gap voltage (V_{BG}).
- Supports PDMA transfer mode.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300 KSPS.

6.19 Digital to Analog Converter (DAC)

6.19.1 Overview

The DAC module is a 8-bit, voltage output digital-to-analog converter. It can be configured to used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.19.2 Features

- Analog output voltage range: 0~AV_{DD}.
- Supports 8-bit output mode.
- Rail to rail settle time 5us.
- Supports up to one 8-bit 200 KSPS voltage type DAC without buffer.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin and AV_{DD}.
- Supports software and hardware trigger, including Timer0~3, and external trigger pin to start DAC conversion.
- Supports PDMA mode.

6.20 Analog Comparator Controller (ACMP)

6.20.1 Overview

The chip provides two ACMP controllers, each controller supports 2 comparators. Controller ACMP01 supports ACMP0 and ACMP1; controller ACMP23 supports ACMP2 and ACMP3. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.20.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to four rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 20mV, 40mV
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Supports Comparator Reference Voltage (CRV0)
    - Internal band-gap voltage (V_{BG})
    - DAC0 output (DAC0_OUT)
- ACMP1 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Supports Comparator Reference Voltage (CRV1)
    - Internal band-gap voltage (V_{BG})
    - DAC1 output (DAC1_OUT)
- ACMP2 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP2_P0, ACMP2_P1, ACMP2_P2, or ACMP2_P3
  - 4 negative sources:
    - ACMP2_N
    - Supports Comparator Reference Voltage (CRV2)
    - Internal band-gap voltage (V_{BG})
    - DAC2 output (DAC2_OUT)

- ACMP3 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP3_P0, ACMP3_P1, ACMP3_P2, or ACMP3_P3
  - 4 negative sources:
    - ACMP3_N
    - Supports Comparator Reference Voltage (CRV3)
    - Internal band-gap voltage (V_{BG})
    - DAC3 output (DAC3_OUT)
- Shares one ACMP interrupt vector for two comparators, ACMP01_INT is for ACMP0 and ACMP1, ACMP23_INT is for ACMP2 and ACMP3
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports window compare mode and window latch mode
- Supports offset calibration

6.21 Peripherals Interconnection

6.21.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast response.

6.21.2 Peripherals Interconnect Matrix Table

Please refer to the relative Technical Reference Manual for detailed functional description about the peripherals interconnection.

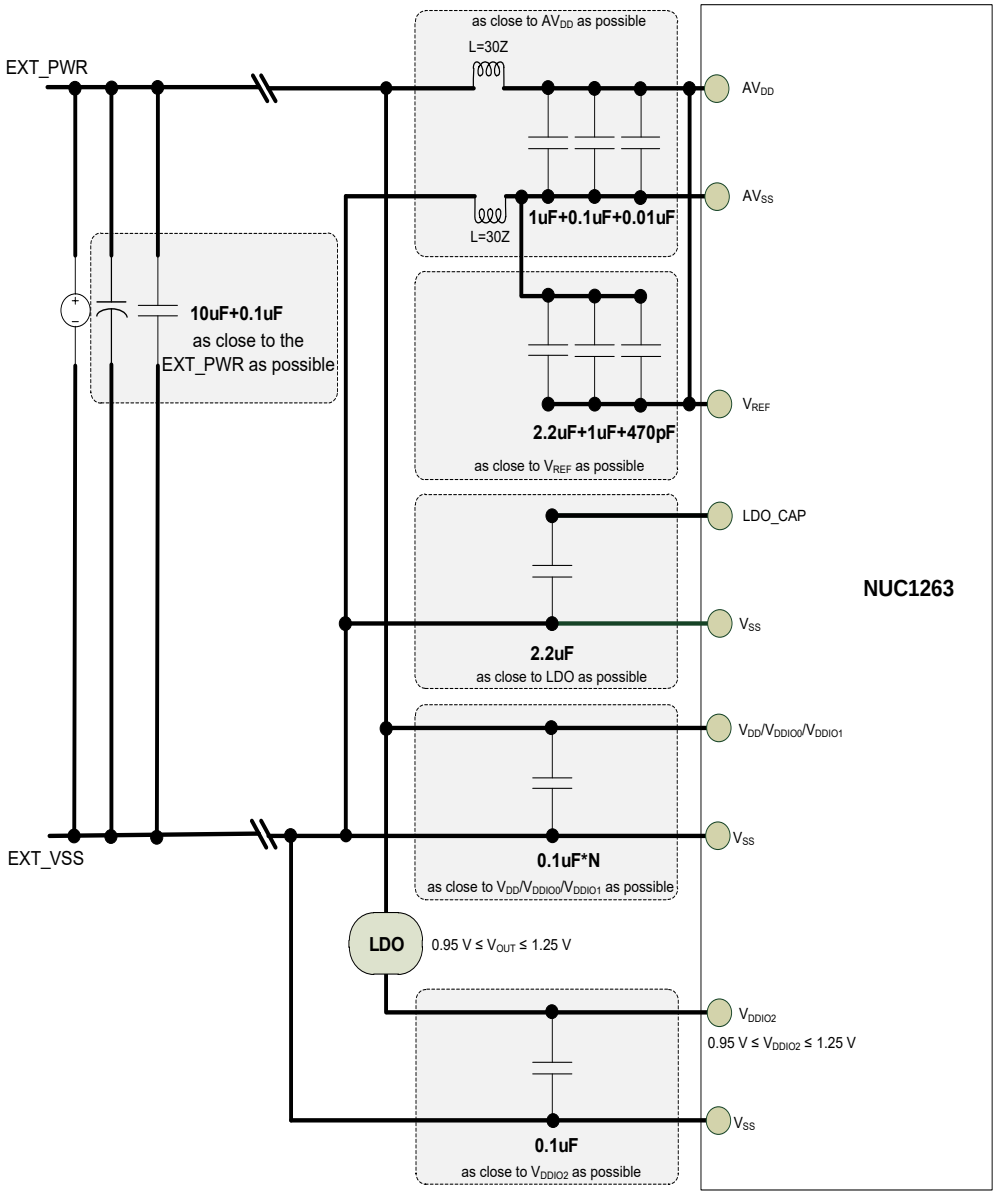
Source	Destination				
	ADC	DAC	HIRC TRIM	BPWM	Timer
LIRC	-	-	-	-	√
BPWM	√	-	-	-	-
LXT			√		
Timer	√	√		√	√
USBD			√		

Table 6.21-1 Peripherals Interconnect Matrix Table

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme

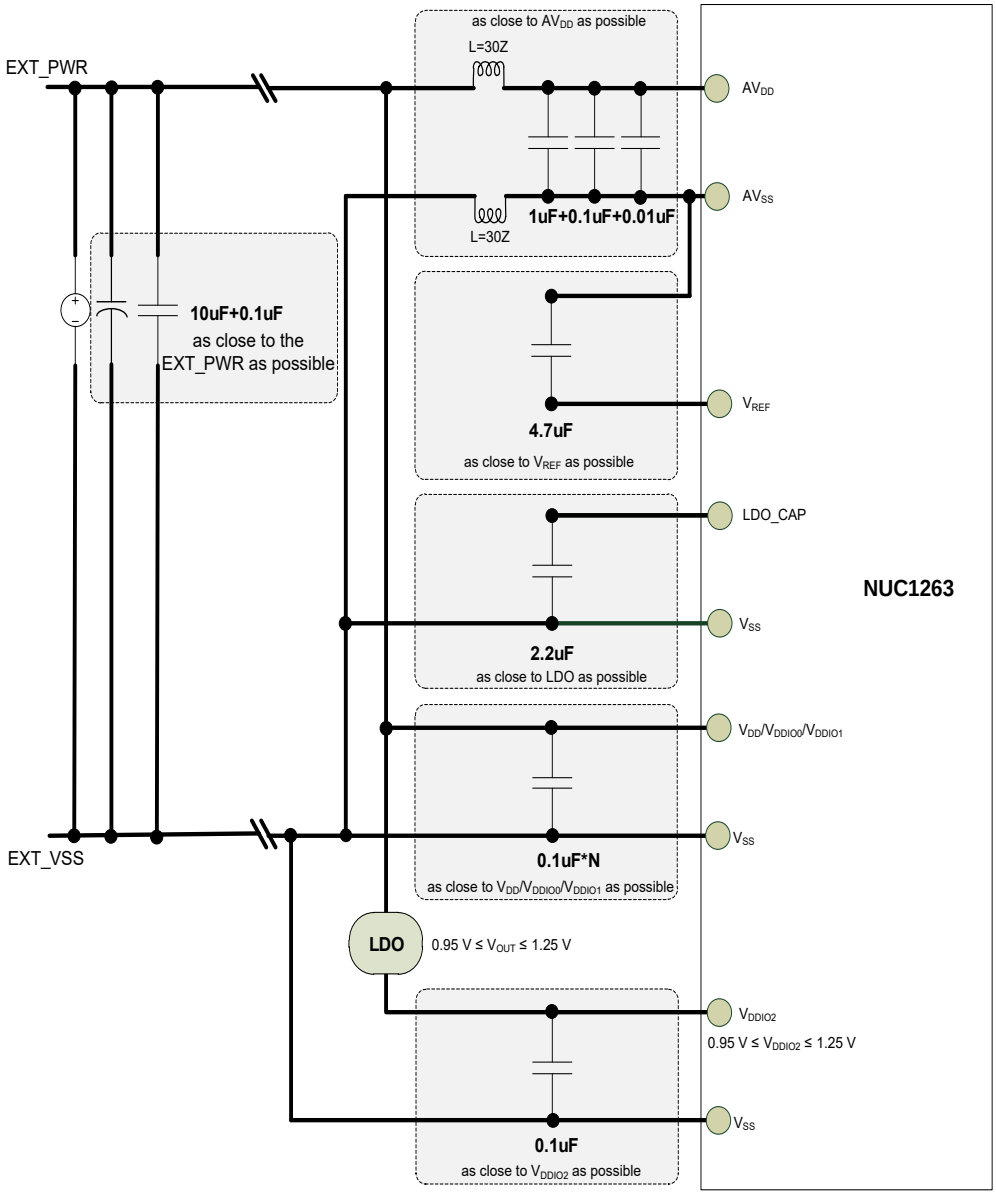
7.1.1 VREF Connects to AVDD



Note: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

Figure 7.1-1 Power supply scheme

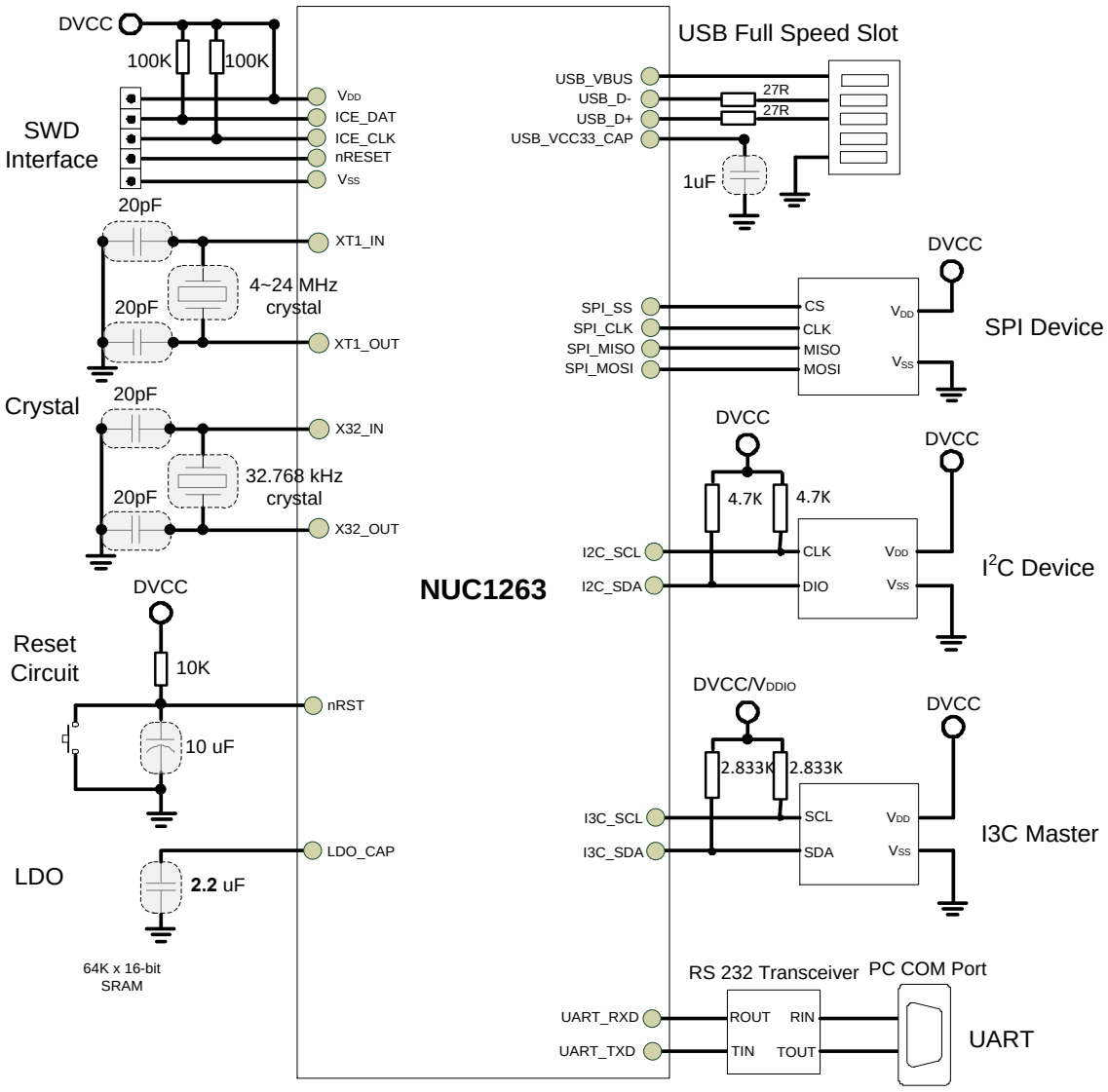
7.1.2 VREF Floating



Note: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

Figure 7.1-2 Power supply scheme

7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 3: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

Note 4: It is recommended to use 2.833 kΩ pull-up resistor on the SDA and SCL pins of the I3C master.

Figure 7.2-1 Peripheral application scheme

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
V_{DDIO0}-V_{SS}[*1]	V_{DDIO0} Power Supply	-0.3	6.5	V
V_{DDIO1}-V_{SS}[*1]	V_{DDIO1} Power Supply	-0.3	6.5	V
V_{DDIO2}-V_{SS}[*1]	V_{DDIO2} Power Supply	-0.3	1.25	V
V_{BUS}-V_{SS}[*1]	V_{BUS} Power Supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{DD} - AV_{DD} \rvert$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\lvert V_{SS} - AV_{SS} \rvert$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	V_{DD} + 0.3	V

Notes:

1. All main power (V_{DD}, V_{DDIO0}, V_{DDIO1}, V_{DDIO2}, AV_{DD}, V_{REF}, V_{BUS}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD} [*1]	Maximum current into V_{DD}	-	200	mA
I_{DDIO0}	Maximum Current into V_{DDIO0}	-	50	
I_{DDIO1}	Maximum Current into V_{DDIO1}	-	50	
I_{DDIO2}	Maximum Current into V_{DDIO2}	-	50	
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins [*2]	-	100	
	Maximum current sourced by total I/O Pins [*2]	-	100	
I_{IO}	Maximum current sunk by a I/O Pin for I3C	-	3	
	Maximum current sourced by a I/O Pin for I3C	-	3	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA}) = T_C + (P_D \times \theta_{JC})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- θ_{JC} = thermal resistance junction-case (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 48-pin QFN(7x7 mm)	-	30.9	-	℃/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	℃/Watt
θ_{JC}[*1]	Thermal resistance junction-case 48-pin QFN(7x7 mm)	-	TBD	-	℃/Watt
	Thermal resistance junction-case 64-pin LQFP(7x7 mm)	-	TBD	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8K	-	+8K	V
V_{HBM}[*1]	Electrostatic discharge,human body mode For I3C pins	-4K	-	+4K	
V_{CDM}[*2]	Electrostatic discharge,charge device model	-750	-	+750	
V_{MM}[*]	Electrostatic discharge,machine model	-300	-	+300	
LU[*3]	Pin current for latch-up[*3]	-100	-	+100	mA
V_{EFT}[*4]	Fast transient voltage burst	-4.4	-	+4.4	kV
V_{SYSESD}	System electrostatic discharge (contact mode)	-1.6	-	+1.6	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.
5. Determinded according to IEC 61000-4-6 standard and the performance class is class A.

Table 8.1-4 EMC characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
33-pin QFN(5x5 mm) [*1]	MSL 3
48-pin QFN(7x7 mm) [*1]	MSL 3
48-pin LQFP(7x7 mm) [*1]	MSL 3
64-pin LQFP(7x7 mm) [*1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

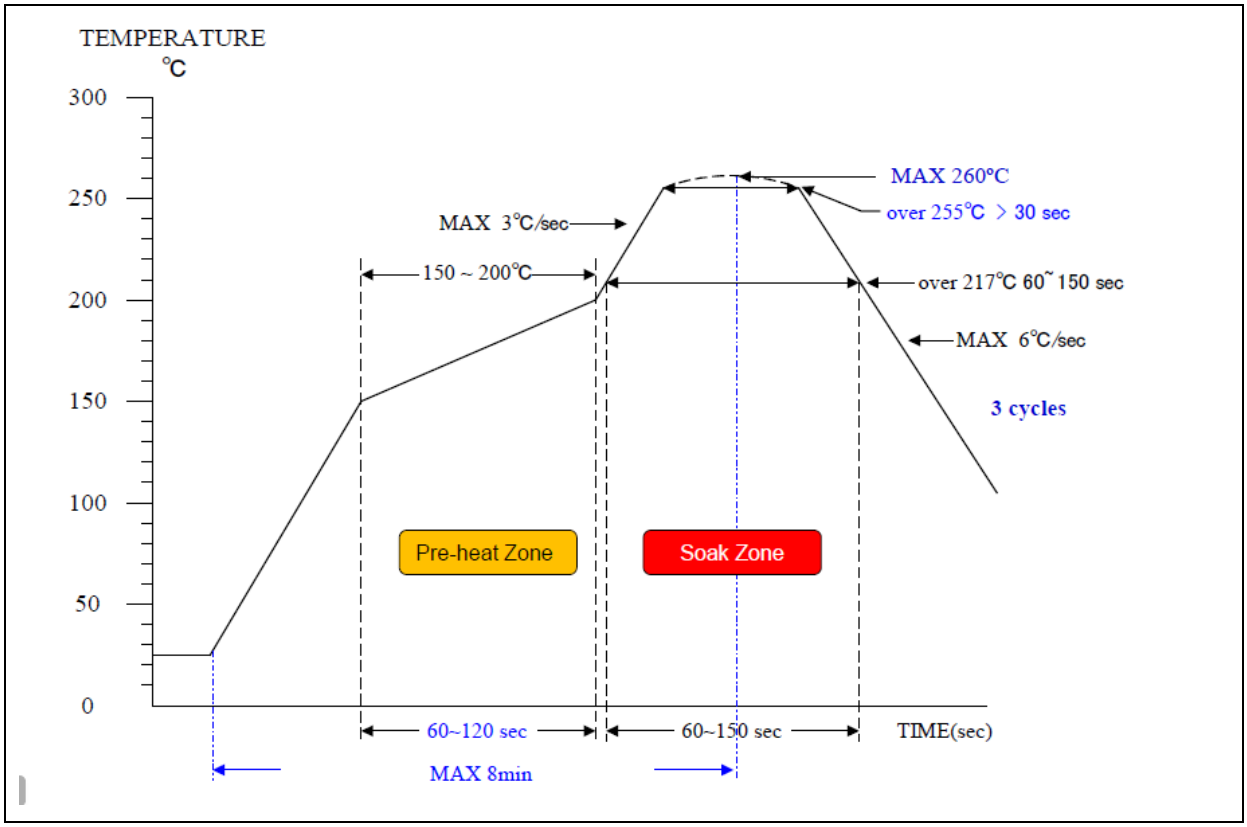


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1.Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.5 ~ 5.5V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	72	MHz	
V_{DD}	Operation voltage	2.5	-	5.5	V	
V_{DDIO0}	V_{DDIO} Operation voltage	1.8	-	5.5		
V_{DDIO1}	V_{DDIO} Operation voltage	1.8	-	5.5		
V_{DDIO2}	V_{DDIO} Operation voltage	0.95	-	1.25		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				Except ADC, ACMP, TempSensor and DAC[*4]
V_{REF}	Analog reference voltage	2.5	-	AV_{DD}		Except ADC[*4]
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}	Band-gap voltage	1.10	1.21	1.30	mV	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	100	-	-	µS	
C_{LDO}[*2]	LDO output capacitor	2.2			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	100		mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	3.96	-	µC	V_{DD} = 1.8 V, T_A = 25 °C

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production.
4. The specific operation voltage range of analog peripheral is listed in section 8.5.

Table 8.2-1 General operating conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = max.VDD V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 2.5 ~ 5.5 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO0} = V_{DDIO1}, V_{DDIO2}$ = 1.2 V
- When the peripherals are enabled, HCLK is the system clock and $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	HCLK	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_OP}	Normal run mode, executed from Flash, all peripherals disable HIRC, PLL, HXT or or LIRC clock	PLL (HIRC)	72 MHz	19.63	20.60	21.63	22.42	mA
		HIRC	48 MHz	11.27	11.82	12.63	13.33	
		HXT	24 MHz	8.41	9.95	10.70	11.36	
		HIRC/4	12 MHz	4.20	4.43	5.01	5.61	
		HIRC/12	4 MHz	2.61	2.77	3.29	3.88	
		HIRC/24	2 MHz	2.15	2.28	2.79	3.38	
		LXT	32.768 kHz	0.11	0.15	0.63	1.21	
		LIRC	10 kHz	0.12	0.15	0.63	1.22	
	Normal run mode, executed from Flash, all peripherals enable HIRC, PLL, HXT or LIRC clock	PLL (HIRC)	72 MHz	41.17	43.37	45.25	46.35	
		HIRC	48 MHz	25.44	26.80	28.25	29.19	
		HXT	24 MHz	15.29	17.16	18.24	19.07	
		HIRC/4	12 MHz	8.42	8.90	9.70	10.38	
		HIRC/12	4 MHz	4.63	4.91	5.53	6.15	
		HIRC/24	2 MHz	3.61	3.83	4.41	5.02	
		LXT	32.768 kHz	0.12	0.16	0.64	1.22	
		LIRC	10 kHz	0.12	0.15	0.64	1.23	

Notes:

1. When analog peripheral blocks such as POR, LVR, USB, ADC, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current consumption in Normal Run mode

Symbol	Conditions	HCLK	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable HIRC, PLL, HXT or LIRC clock	PLL (HIRC)	72 MHz	8.10	8.60	9.31	9.97	mA
		HIRC48	48 MHz	3.56	3.80	4.39	4.99	
		HXT	24 MHz	4.61	6.04	6.69	7.30	
		HIRC/4	12 MHz	2.28	2.42	2.94	3.54	
		HIRC/12	4 MHz	1.97	2.10	2.60	3.20	
		HIRC/24	2 MHz	1.83	1.95	2.45	3.04	
		LXT	32.768 kHz	0.10	0.13	0.62	1.19	
		LIRC	10 kHz	0.10	0.13	0.61	1.19	
	Idle mode, all peripherals enable HIRC, PLL, HXT or LIRC clock	PLL (HIRC)	72 MHz	30.58	32.44	34.10	35.11	
		HIRC48	48 MHz	18.20	19.34	20.59	21.45	
		HXT	24 MHz	11.93	13.71	14.69	15.47	
		HIRC/4	12 MHz	6.26	6.65	7.37	8.03	
		HIRC/12	4 MHz	3.60	3.82	4.41	5.02	
		HIRC/24	2 MHz	2.87	3.05	3.60	4.19	
		LXT	32.768 kHz	0.11	0.14	0.63	1.21	
		LIRC	10 kHz	0.10	0.13	0.62	1.20	

Notes:

1. When analog peripheral blocks such as USB, ADC, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 10 kHz	Typ[*2]	Max[*3][*4]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	14	33	487	1043	µA
	Power-down mode, all peripherals disable	-	V	15	34	488	1047	
	Power-down mode, all peripherals disable	V	-	17	36	491	1051	
	Power-down mode, all peripherals disable	V	V	17	37	493	1054	
	Power-down mode, all peripherals disable Except WDT/Timer	-	V	15	34	491	1053	
	Power-down mode, all peripherals disable Except WDT/Timer/UART	V	-	18	38	495	1059	
	Power-down mode, all peripherals disable Except WDT/Timer/UART	V	V	19	39	497	1062	

Notes:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L7 gain level.
2. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as USB, ADC and are ON, an additional power consumption should be considered.
5. LCD COM/SEG is set to 1/8 duty, 1/4 bias, 64 Hz frame rate, all pixels active, type B waveform, no LCD panel loading.

Table 8.3-3 Chip Current Consumption in Power-down mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = V_{DDIO0} = V_{DDIO1} = 5 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1}$ = f_{HCLK}
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on based on default clock source selection.

Peripheral	I_{DD}[*1]	Unit
PDMA	621	uA
ISP	~0	
CRC	61	
FMCIDLE	1430	
GPA	244	
GPB	318	
GPC	177	
GPD	108	
GPF	173	
WDT	447	
TMR0	581	
TMR1	560	
TMR2	531	
TMR3	530	
CLKO	58	
I2C0	344	
I2C1	296	
I2C2	364	
SPI0	873	
SPI1	829	
SPI2	820	
UART0	775	
UART1	772	
UART2	1064	
BPWM0	461	
BPWM1	391	
BPWM2	462	

BPWM3	411	
I3C0	1444	
I3C1	1380	
USBD	878	
ADC	747	
DAC	450	
ACMP01	721	
ACMP23	676	
LLSI0	537	
LLSI1	481	
LLSI2	525	
LLSI3	495	
LLSI4	558	
LLSI5	467	

Notes:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the USB is turned on, add an additional power consumption per USB for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}[*1]	Wakeup from IDLE mode	-	4	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal Power-down mode running in flash	-	31	
	Wakeup from normal Power-down mode running in RAM	-	31	
t_{ET_IDLE}[*1]	Enter to IDLE mode	-	10	cycles
t_{ET_NPD}[*1]	Enter to normal Power-down mode	-	1.35	

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-5 Low-power mode wakeup timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	+0	mA	Injected current on nReset pins
		-0	+0		Injected current on PF2~PF5 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O current injection characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	$0.3*V_{DD}$	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 2.5 V
V_{IH}	Input high voltage (Schmitt trigger)	$0.7*V_{DD}$	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		1.2	-	V_{DD}		V_{DD} = 2.5 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1	-	1		$V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	66.96	78.5	249	kΩ	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O input characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2] [*3]	Source current for quasi-bidirectional mode and high level	-	-109.7	-	µA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-	-67.4	-	µA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-	-61.4	-	µA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-	-7.8	-	mA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-	-4.7	-	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-	-4.3	-	mA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
	PA0~PA3,PA8~PA11 PF4~PF6 Source current for push-pull mode and high level	-	-12.18	-	mA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-	-7.47	-	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-	-6.81	-	mA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2] [*4]	Sink current for push-pull mode and low level	-	13.8	-	mA	V_{DD} = 4.5 V V_{IN}= 0.4 V
		-	8.5	-	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		-	7.8	-	mA	V_{DD} = 2.5 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.
3. The range of output high level voltage (V_{OH}) is from V_{DD}-0.4 to V_{DD} based on minimum value of source current (I_{SR}).
4. The range of output low level voltage (V_{OL}) is from 0 to 0.4 based on minimum value of sink current (I_{SK}).

Table 8.3-8 I/O output characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	$0.3*V_{DD}$	V	
V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	35.36	42.2	125.1	kΩ	V_{DD}=2.5V ~ 5.5V
t_{RP}[*1]	Minimum nRESET pulse width		32	-	µS	Normal run and Idle mode
			179	-		Power-down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

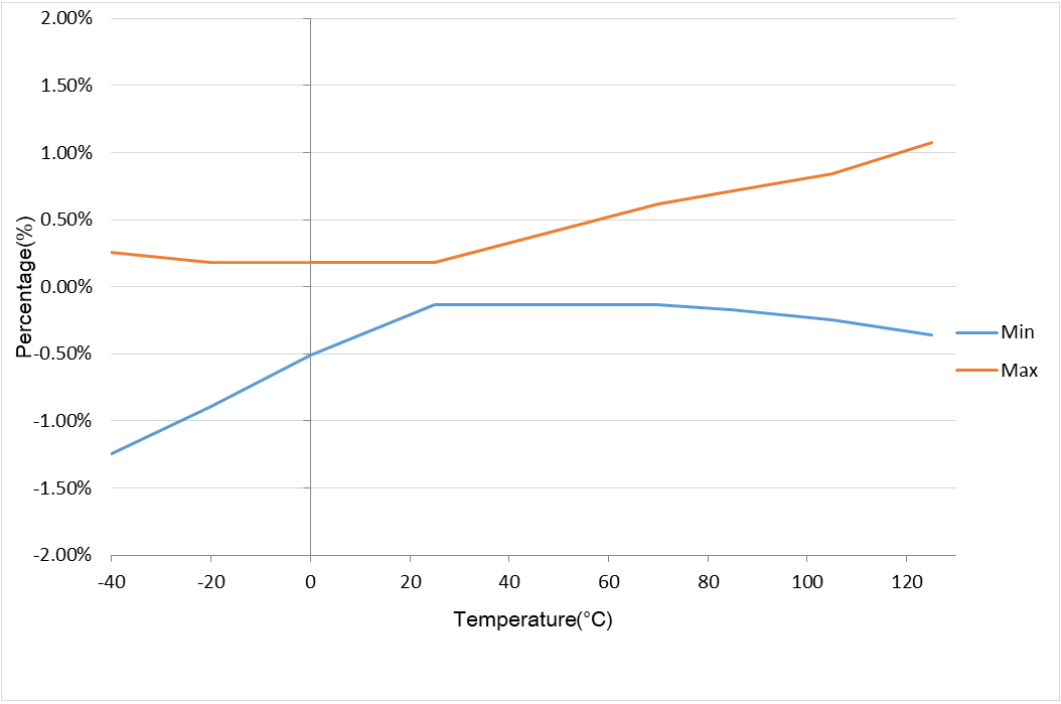
The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operating voltage	2.5	-	5.5	V	
f_{HIRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[*1]	-	2[*1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V
		-0.25	-	+0.25	%	T_A = -40°C ~ +105°C, V_{DD} = 2.5 ~ 5.5V Auto trimmed by LXT
I_{HIRC}[*1]	Operating current	-	500	-	μA	
T_S[*2]	Stable time	-	-	5	μS	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V

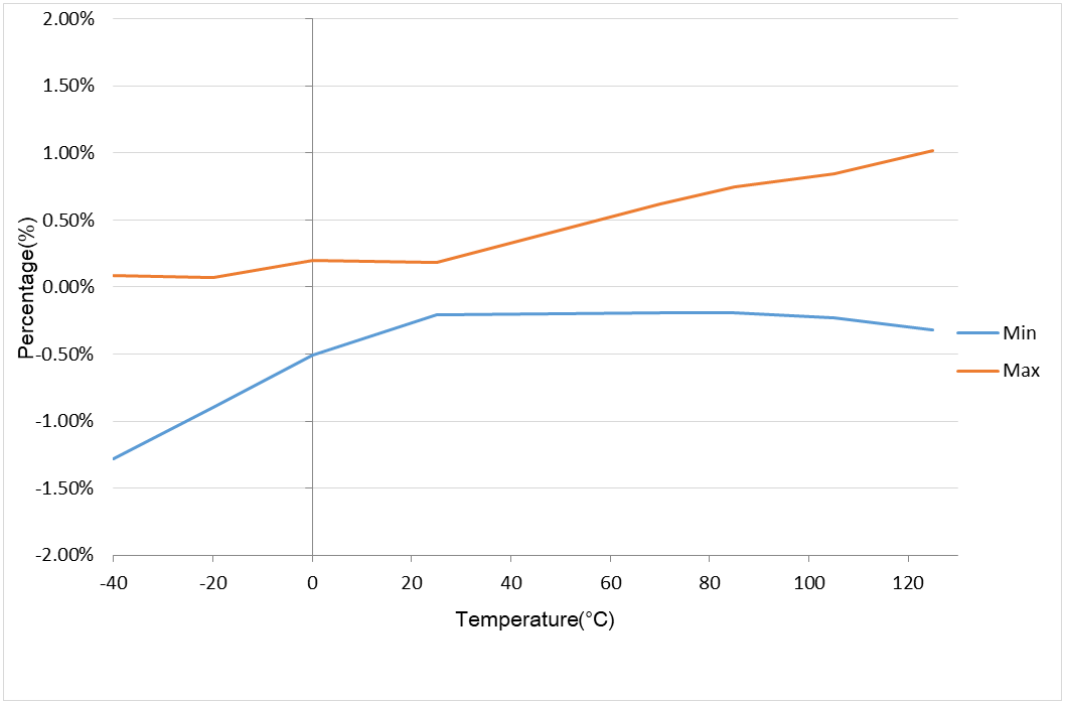
Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



(a) Test condition: V_{DD}=3.6 V, Temp = -40~125°C



(b) Test condition: V_{DD}=2.5 V, Temp = -40~125°C

Note:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-1.

Figure 8.4-1 HIRC vs. Temperature

8.4.2 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operating voltage	2.5	-	5.5	V	
F_{LIRC} [*2]	Oscillator frequnecy	-	10	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-40	-	40	%	T_A=-40~105°C V_{DD}=2.5V~5.5V Without software calibration
I_{LIRC}	Operating current			1.4	μA	V_{DD} = 3.3V
T_S [*3]	Stable time	-	100		μS	T_A=-40~105°C V_{DD}=2.5V~5.5V

Notes:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-2 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.3 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
R_f	Internal feedback resister	-	250	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption (Crystal type)	-	0.3	1	mA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	1	4		12 MHz, Gain = L1, C_L = 12.5 pF
		-	1.5	6.7		16 MHz, Gain = L2, C_L = 12.5 pF
		-	2.2	9		24 MHz, Gain = L3, C_L = 12.5 pF
I_{HXT}	Current consumption (Resonator type)	-	0.45	2	mA	4 MHz, Gain = L0, C_L = 30 pF
		-	0.8	3.2		12 MHz, Gain = L1, C_L = 20 pF
		-	1.5	8		16 MHz, Gain = L2, C_L = 10 pF
		-	2	9		24 MHz, Gain = L3, C_L = 10 pF
T_S	Stable time (Crystal type)	-	4.5	8.5	mS	4 MHz, Gain = L0, C_L = 12.5 pF
		-	3	3.5		12 MHz, Gain = L1, C_L = 12.5 pF
		-	2.5	2.8		16 MHz, Gain = L2, C_L = 12.5 pF
		--	1.5	2		24 MHz, Gain = L3, C_L = 12.5 pF
T_S	Stable time (Resonator type)	-	1.04	1.1	mS	4 MHz, Gain = L0, C_L = 30 pF
		-	0.35	0.4		12 MHz, Gain = L1, C_L = 20 pF
		-	0.26	0.3		16 MHz, Gain = L2, C_L = 10 pF
		--	0.21	0.25		24 MHz, Gain = L3, C_L = 10 pF
Du_{HXT}	Duty cycle	40	-	70	%	
V_{PP}	Swing Amplitude	0.3*V_{DD}	50	70	V	

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
Notes: 1. Guaranteed by characterization, not tested in production.						

Table 8.4-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR) (Crystal type)	-	-	150	Ω	Crystal at 4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	120		Crystal at 12 MHz, C_L = 12.5 pF, Gain = L1
		-	-	100		Crystal at 16 MHz, C_L = 12.5 pF, Gain = L2
		-	-	80		Crystal at 24 MHz, C_L = 12.5 pF, Gain = L3
	Equivalent series resisotr(ESR) (Resonator type)	-	-	40		Ceramic Resonator at 4 MHz, C_L = 30 pF, Gain = L0
		-	-	20		Ceramic Resonator at 12 MHz, C_L = 20 pF, Gain = L1
		-	-	60		Ceramic Resonator at 16 MHz, C_L = 10 pF, Gain = L2
		-	-	60		Ceramic Resonator at 24 MHz, C_L = 10 pF, Gain = L3

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

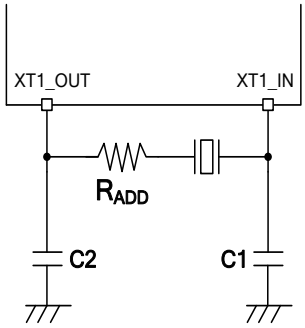


Table 8.4-4 External 4~24 MHz High Speed Crystal Characteristics

8.4.3.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

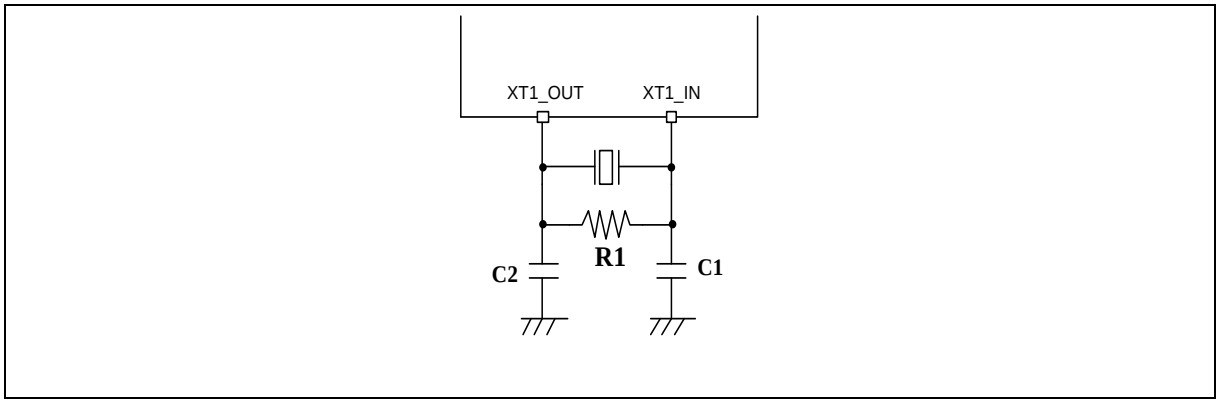
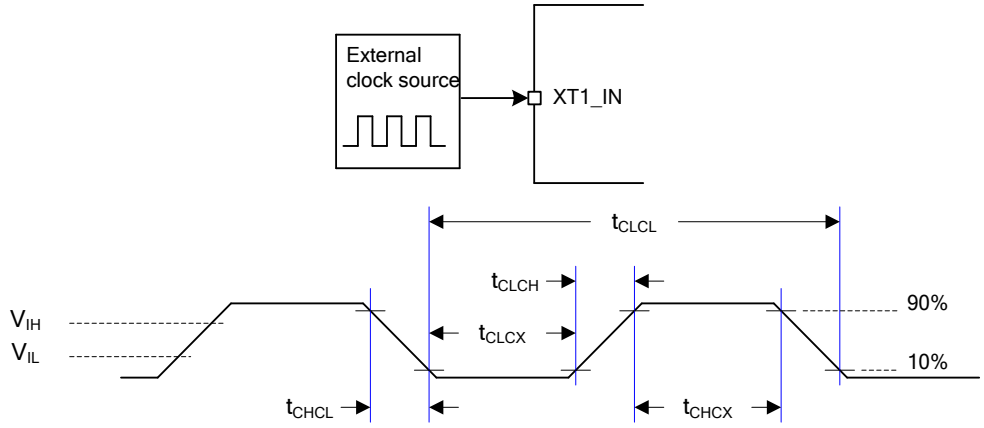


Figure 8.4-2 Typical Crystal Application Circuit

8.4.4 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	The XT1_IN is set as schmitt trigger input mode.
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	The XT1_IN is set as schmitt trigger input mode.



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~24 MHz High Speed Clock Input Signal

8.4.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	6	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	600	4400	nA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L0
		-	750	4600		ESR=35 kΩ, C_L = 12.5 pF, Gain = L1
		-	800	4800		ESR=35 kΩ, C_L = 12.5 pF, Gain = L2
		-	950	5200		ESR=70 kΩ, C_L = 12.5 pF, Gain = L3
		-	1050	5400		ESR=70 kΩ, C_L = 12.5 pF, Gain = L4
		-	1400	5600		ESR=70 kΩ, C_L = 12.5 pF, Gain = L5
		-	1600	6000		ESR=90 kΩ, C_L = 12.5 pF, Gain = L6
		-	1900	6600		ESR=90 kΩ, C_L = 12.5 pF, Gain = L7
Ts_{LXT}	Stable time	-	1	-	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	0.35	0.5	-	V	

Notes:
1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	90	kΩ	Crystal @32.768 kHz

Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics

8.4.5.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

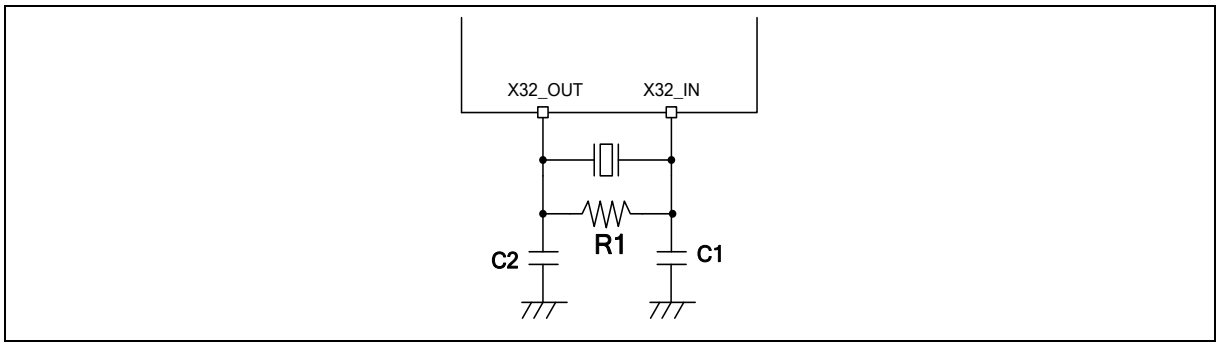
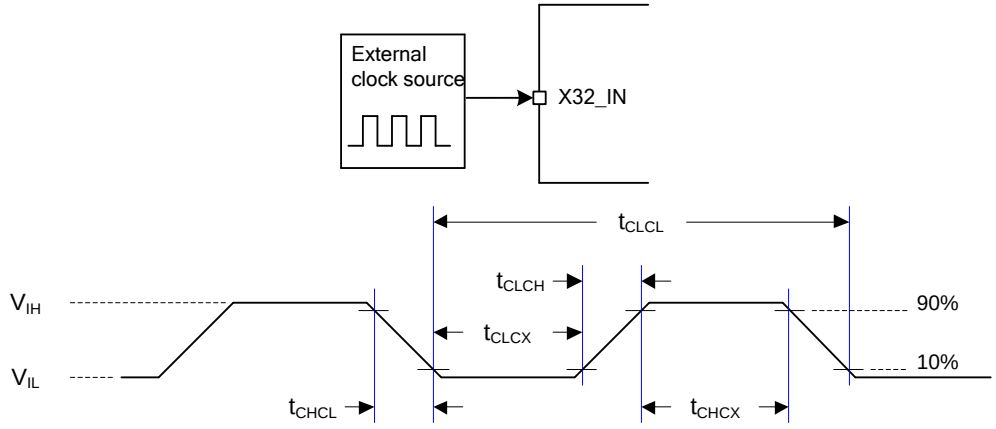


Figure 8.4-3 Typical 32.768 kHz Crystal Application Circuit

8.4.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
V_{IH}	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	The X32_IN is set as schmitt trigger input mode.
V_{IL}	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	The X32_IN is set as schmitt trigger input mode.



Notes:

1.Guaranteed by design, not tested in production

Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal

8.4.7 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	16	-	144	MHz	
f_{PLL_REF}	PLL reference clock	4	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	200	-	480	MHz	
T_L	PLL locking time	-	-	500	µS	
Jitter[*2]	Cycle-to-cycle Jitter	500	-	-	pS	
I_{DD}	Power consumption	-	-	16	mA	VDD=5.5V @ f_{PLL_VCO} = 288 MHz

Notes:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-9 PLL Characteristics

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(I/O)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	7.0	-	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		5.2	-		C_L = 10 pF, V_{DD} >= 4.5 V
		12.0	-		C_L = 30 pF, V_{DD} >= 2.7 V
		9.2	-		C_L = 10 pF, V_{DD} >= 2.7 V
		13.0	-		C_L = 30 pF, V_{DD} >= 2.5 V
		10.0	-		C_L = 10 pF, V_{DD} >= 2.5 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	4.3	-		C_L = 30 pF, V_{DD} >= 4.5 V
		3.0	-		C_L = 10 pF, V_{DD} >= 4.5 V
		6.4	-		C_L = 30 pF, V_{DD} >= 2.7 V
		4.6	-		C_L = 10 pF, V_{DD} >= 2.7 V
		7.0	-		C_L = 30 pF, V_{DD} >= 2.5 V
		4.9	-		C_L = 10 pF, V_{DD} >= 2.5 V
$t_{r(I/O)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	6.1	-	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		4.2	-		C_L = 10 pF, V_{DD} >= 4.5 V
		10.3	-		C_L = 30 pF, V_{DD} >= 2.7 V
		6.9	-		C_L = 10 pF, V_{DD} >= 2.7 V
		11.6	-		C_L = 30 pF, V_{DD} >= 2.5 V
		7.6	-		C_L = 10 pF, V_{DD} >= 2.5 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	4.7	-	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		2.9	-		C_L = 10 pF, V_{DD} >= 4.5 V
		7.9	-		C_L = 30 pF, V_{DD} >= 2.7 V
		4.7	-		C_L = 10 pF, V_{DD} >= 2.7 V
		8.5	-		C_L = 30 pF, V_{DD} >= 2.5 V
		5.2	-		C_L = 10 pF, V_{DD} >= 2.5 V
$f_{max(I/O)out}$[*3]	I/O maximum frequency	51.2	-	MHz	C_L = 30 pF, V_{DD} >= 4.5 V

	(Normal Slew Rate)	72.0	-		C_L = 10 pF, V_{DD} >= 4.5 V
		30.2	-		C_L = 30 pF, V_{DD} >= 2.7 V
		41.6	-		C_L = 10 pF, V_{DD} >= 2.7 V
		27.3	-		C_L = 30 pF, V_{DD} >= 2.5 V
		38.2	-		C_L = 10 pF, V_{DD} >= 2.5 V
	I/O maximum frequency (High Slew Rate)	74.8	-	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		115.2	-		C_L = 10 pF, V_{DD} >= 4.5 V
		46.7	-		C_L = 30 pF, V_{DD} >= 2.7 V
		72.6	-		C_L = 10 pF, V_{DD} >= 2.7 V
		43.2	-		C_L = 30 pF, V_{DD} >= 2.5 V
		67.2	-		C_L = 10 pF, V_{DD} >= 2.5 V
I_{DIO}[*4]	I/O dynamic current consumption	2.8	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 24 MHz
		1.2	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 24 MHz
		0.7	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 6 MHz

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-10 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	2.5	3.3	5.5	V	
V_{LDO}	Output voltage	-	1.8	-	V	
T_A	Temperature	-40	-	105	°C	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. F or ensuring power stability, a 2.2μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.
3. V_{LDO} is only used to supply internal power.

Table 8.5-1 LDO characteristics

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	-	5.5	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	-	0.7	1.65		V_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	90	150		AV_{DD} = 5.5V, Normal mode
		-	0.5	1.5		AV_{DD} = 5.5V, Low Power mode
V_{POR}	POR reset voltage	1.13	1.75	2.5	V	
	POR Hysteresis	0.1	0.24	-		
V_{LVR}	LVR reset voltage	1.5	2.0	2.4		
V_{BOD}	BOD brown-out detect voltage (Rising edge)	2.15	2.3	2.45		BODVL = 0
		2.65	2.8	2.95		BODVL = 1
		3.65	3.8	3.95		BODVL = 2
		4.35	4.5	4.65		BODVL = 3
	BOD brown-out detect voltage (Falling edge)	2.1	2.2	2.3		BODVL = 0
		2.6	2.7	2.8		BODVL = 1
		3.6	3.7	3.8		BODVL = 2
		4.3	4.4	4.5		BODVL = 3
V_{HYSn}	BOD Hysteresis	50	100	150	mV	
T_{LVR_SU}[*1]	LVR startup time	-	150	250	μS	-
T_{LVR_RE}[*1]	LVR respond time	-	90	100		-
T_{BOD_SU}[*1]	BOD startup time	-	1000	1200		-

T_{BOD_RE}[*1]	BOD respond time	-	60	100		Normal mode
		-	-	15000		Low Power mode
R_VDD_R[*1]	V_{DD} rise time rate	10	-	-	µS/V	POR Enabled
R_VDD_F[*1]	V_{DD} fall time rate	10000	-	-		POR Enabled
		2000	-	-		LVR Enabled
		500	-	-		BOD 2.2V Enabled, Normal mode
		150	-	-		BOD 2.7V Enabled, Normal mode
		60	-	-		BOD 3.7 Enabled, Normal mode
		40	-	-		BOD 4.5V Enabled, Normal mode
		75			mS/V	BOD 2.2V Enabled, Low Power mode
		25				BOD 2.7V Enabled, Low Power mode
		9				BOD 3.7 Enabled, Low Power mode
		6				BOD 4.5V Enabled, Low Power mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-2 Reset and Power Control Unit

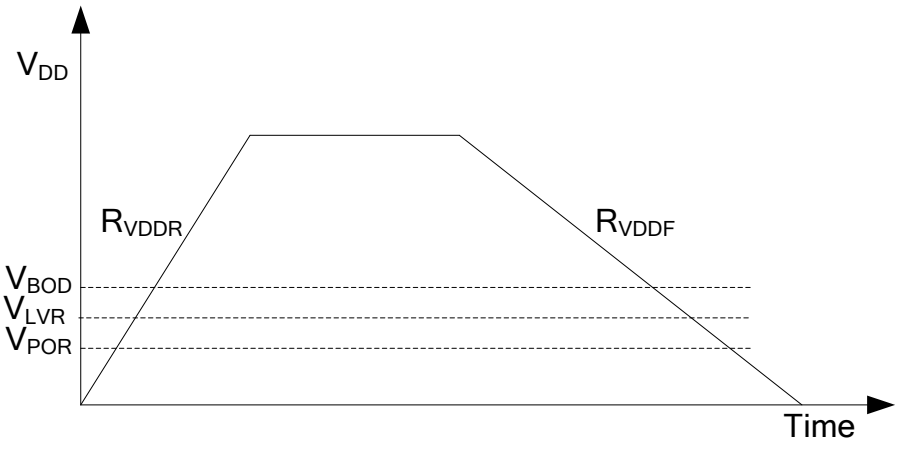


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

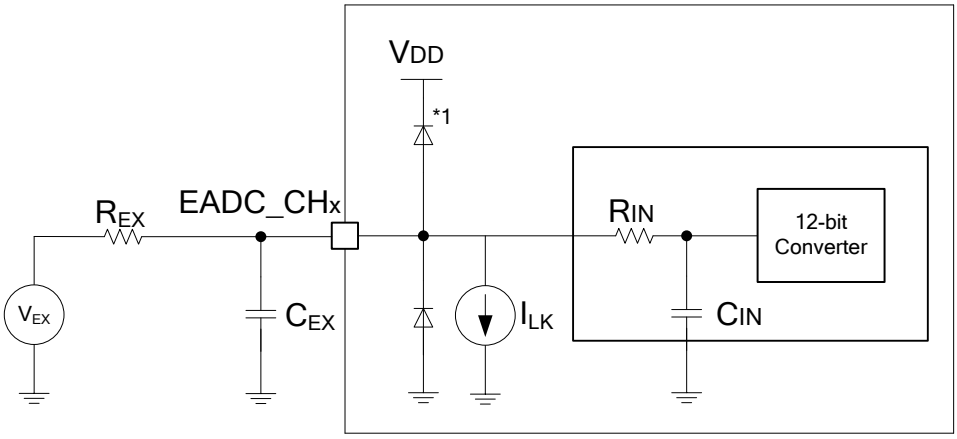
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	3.0	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	3.0	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	-	4	mA	$AV_{DD} = V_{DD} = V_{REF}$ = 5 V F_{ADC} = 16 MHz $T_{CONV} = 16 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	16	MHz	
T_{SMP}	Sampling Time	4	-	11	$1/F_{ADC}$	T_{SMP} = (SMPTSEL(ADC_ADCR[18:16]) + 4) * T_{ADC}
T_{CONV}	Conversion time	16	-	23	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 12 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	222	-	800	KSPS	FSPS = FADC / TCONV 800ksps = 16M/20, 222ksps = 4M/18
T_{EN}	Enable to ready time	5	-	-	µS	
INL[*1]	Integral Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD}$,
DNL[*1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$,
E_G[*1]	Gain error	-4	-2	+4	LSB	$V_{REF} = AV_{DD}$,
E_O[*1]$_T$	Offset error	-4	2	+4	LSB	$V_{REF} = AV_{DD}$,
E_A[*1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
ENOB[*1]	Effective number of bits	-	9.75	-	bits	F_{ADC} = 16 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	60.5	-	dB	
SNR[*1]	Signal-to-noise ratio	-	62.6	-		
THD[*1]	Total harmonic distortion	-	-64	-		
C_{IN}[*1]	Internal Capacitance	-	3.85	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	1.36	kΩ	
R_{EX}[*1]	External input impedance	-	-	30	kΩ	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

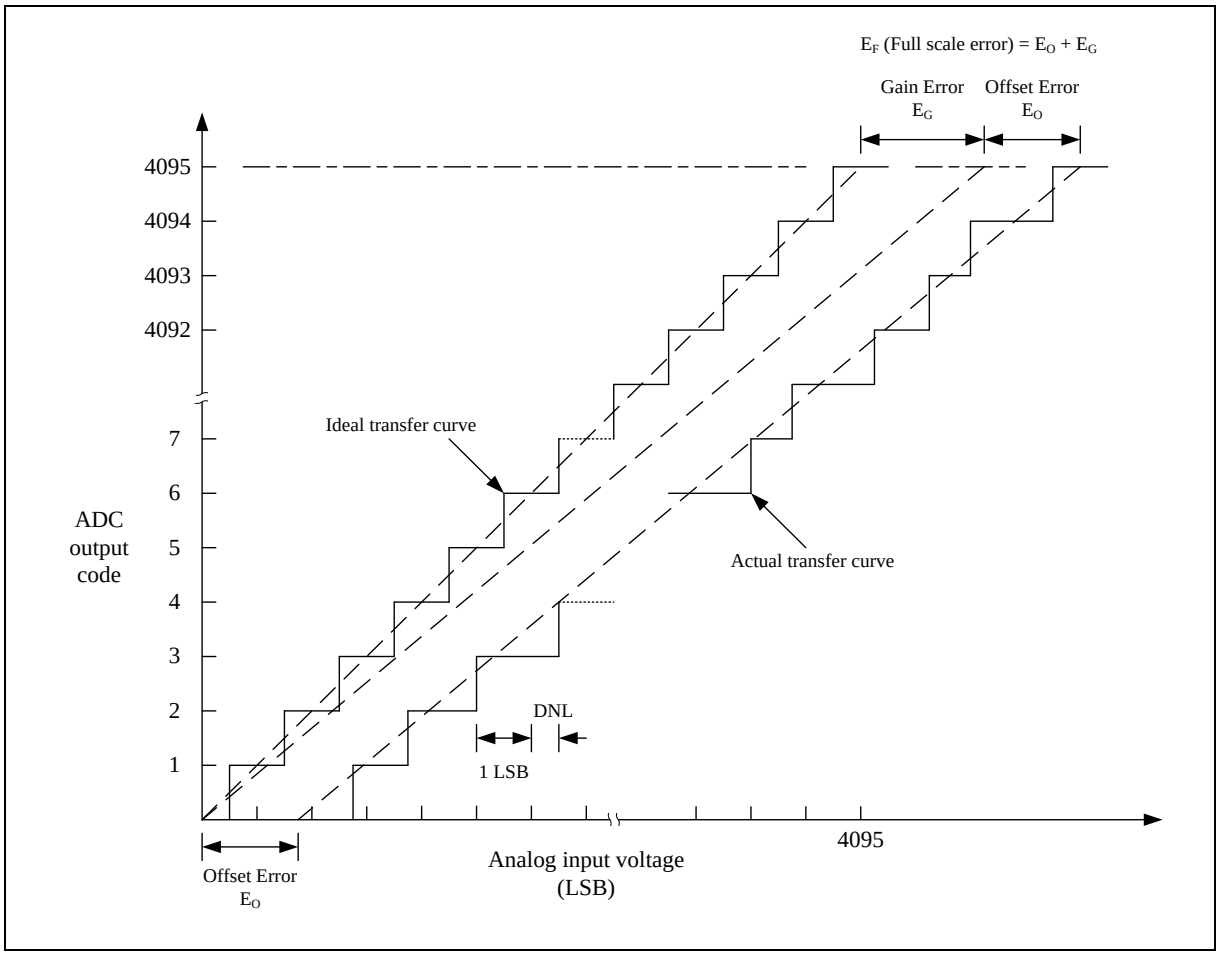
Table 8.5-3 ADC Characteristics



Notes:

1. The internal ESD diode doesn't be supported between IO and VDD at 5V tolerence IO pin.

Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Digital to Analog Converter (DAC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Analog supply voltage	2.5	-	5.5	V	
N_R	Resolution		8		bit	
V_{REF}	Reference supply voltage	2.5	-	AV_{DD}	V	$V_{REF} \le AV_{DD}$
DNL[*2]	Differential non-linearity error	-	±0.4	-	LSB	No Loading
INL[*2]	Integral non-linearity error	-	±0.5	-	LSB	No Loading
OE[*2]	Offset Error	-	±0.5	-	LSB	No Loading
GE[*2]	Gain Error	-	±0.5	-	LSB	No Loading
AE[*2]	Absolute Error	-	-	±1	LSB	No Loading
		-	-	±2	LSB	$AV_{DD} = V_{REF}$ = 3.072 ~ 5.5V and R_{LOAD} = 4M ohm
		-	-	±3	LSB	$AV_{DD} = V_{REF}$ = 3.072 ~ 5.5V and R_{LOAD} = 2M ohm
-	Monotonic		8-bit guaranteed		-	
V_O[*1]	Output Voltage	1*LSB	-	V_{REF} - 1*LSB	V	
R_{LOAD}[*2] [*3]	Resistive load	5	-	-	kΩ	
R_O[*2]	Output impedance	-	6.4	-	kΩ	
C_{LOAD}[*2] [*4]	Capacitive load	-	-	35	pF	-
I_{DAC_AVDD}[*2]	DAC operating current on AV_{DD} supply	-	10	-	μA	AV_{DD} = 5.5V, no load
I_{DAC_VREF}[*2]	DAC operating current on V_{REF} supply	-	-	1000	μA	AV_{DD} = 5.5V, no load
T_B[*2]	Settling Time	-	4	4.5	μS	Full scale: for a 8-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \le$ 35pF, No R_{LOAD}

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

Table 8.5-4 DAC Characteristics

8.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	2.5	-	5.5	V	$V_{DD} = AV_{DD}$
T_A	Temperature	-40	-	105	℃	
I_{ACMP}[*2]	ACMP operating current	-	75	150	μA	
V_{CM}[*2]	Input common mode voltage range	0	1/2 AV_{DD}	AV_{DD}		
V_{DI}[*2]	Differential input voltage sensitivity	30	-	-	mV	(20mV+10mV offset)
V_{offset}[*2]	Input offset voltage	-	±10	±20	mV	
V_{hys}[*2]	Hysteresis window	-	0	-	mV	HYSSEL = 000
		10	20	40		HYSSEL = 010
		20	40	70		HYSSEL = 100
A_v[*1]	DC voltage Gain	43	70	-	dB	
T_d[*2]	Propagation delay	-	120	200	nS	
T_{Setup}[*2]	Setup time	-	-	5	μS	
A_{CRV}[*2]	CRV output voltage	-1.6	-	1.6	%	AV_{DD} x (CRVCTL/63)
I_{DD_CRV}[*2]	Operating current	-	50	100	μA	

Notes:

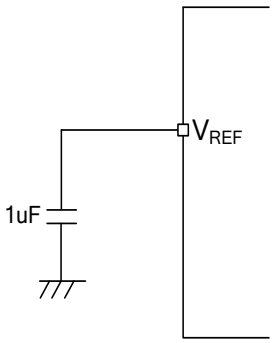
1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-5 ACMP Characteristics

8.5.6 Internal Voltage Reference

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{REF_INT}	Internal reference voltage	2.01728	2.048	2.07872	V	AV_{DD} >= 2.5 V, 0°C~85°C
		2.00704	2.048	2.08896		AV_{DD} >= 2.5 V, -40°C~105°C
		2.5216	2.560	2.5984		AV_{DD} >= 2.9 V, 0°C~85°C
		2.5088	2.560	2.6112		AV_{DD} >= 2.9 V, -40°C~105°C
		3.02592	3.072	3.11808		AV_{DD} >= 3.4 V, 0°C~85°C
		3.01056	3.072	3.13344		AV_{DD} >= 3.4 V, -40°C~105°C
		4.03456	4.096	4.15744		AV_{DD} >= 4.5 V, 0°C~85°C
		4.01408	4.096	4.17792		AV_{DD} >= 4.5 V, -40°C~105°C
T_s[*1]	Stable time	-	-	0.8	mS	C_L = 2.2 uF, V_{REF} initial=0V, Preload is enabled.
		-	-	7	mS	C_L = 2.2 uF, V_{REF} initial= max.VDD V, Preload is enabled.
		-	-	4	mS	C_L = 4.7 uF, V_{REF} initial=0V, Preload is enabled.
		-	-	15	mS	C_L = 4.7 uF, V_{REF} initial=max.VDD V, Preload is enabled.
I_{VREF_INT}[*1]	V_{REF_INT} operating current	-	0.25	0.5	mA	
Note: Guaranteed by characterization, not tested in production.						

Table 8.5-6 Internal V_{REF} Characteristics



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.7 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog supply voltage	2.7		5	V	
T_{TEMP_ERR}	Temperature Deviation	-	±0.5	±1.0	°C	+75℃ to + 95℃
		-	±1.0	±2.0	°C	+40℃ to + 105℃
		-	±2.0	±3.0	°C	-40℃ to + 105℃
I_{TEMP}	Temperature Sensor operating current	-	200	-	μA	
	Long-term stability and drift		1.2		°C	168 hours at 125℃

Note:

1. Guaranteed by characterization, not tested in production

Table 8.5-7 Temperture Sensor Characteristics

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	27	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	15		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	13		2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	4.1	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	4.1	nS	2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	4.1	nS	V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
Note: Guaranteed by design.						

Table 8.6-1 SPI Master Mode Characteristics

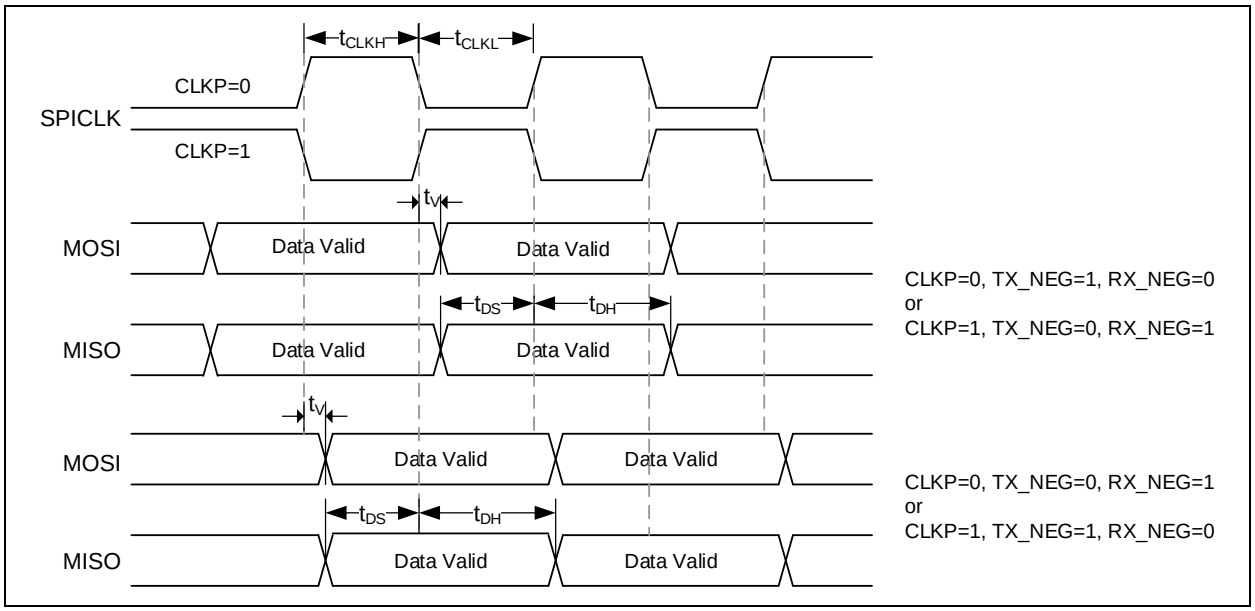


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	12.8	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	9		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	8.3		2.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		2.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	1.5	-	-	nS	
t_{DH}	Data input hold time	3.5	-	-	nS	
t_V	Data output valid time	-	-	39	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	55		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	60		2.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
Note: Guaranteed by design.						

Table 8.6-2 SPI Slave Mode Characteristics

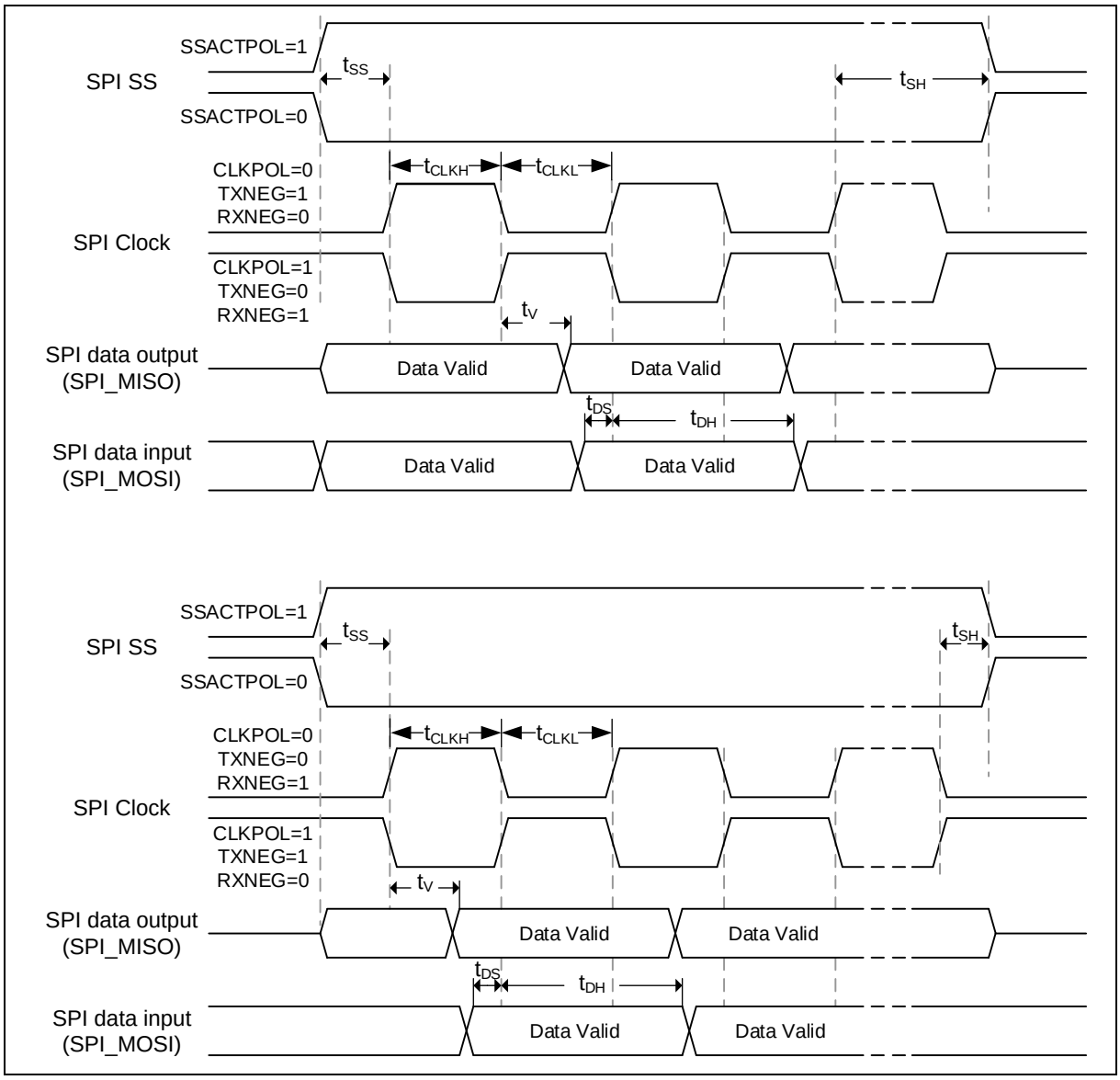


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	80	-	nS	Master f_{PCLK} = 48 MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I²S clock low time	80	-		
$t_{v(WS)}$	WS valid time	2	6		Master mode
$t_{h(WS)}$	WS hold time	2	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	nS	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	25		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I2S Characteristics

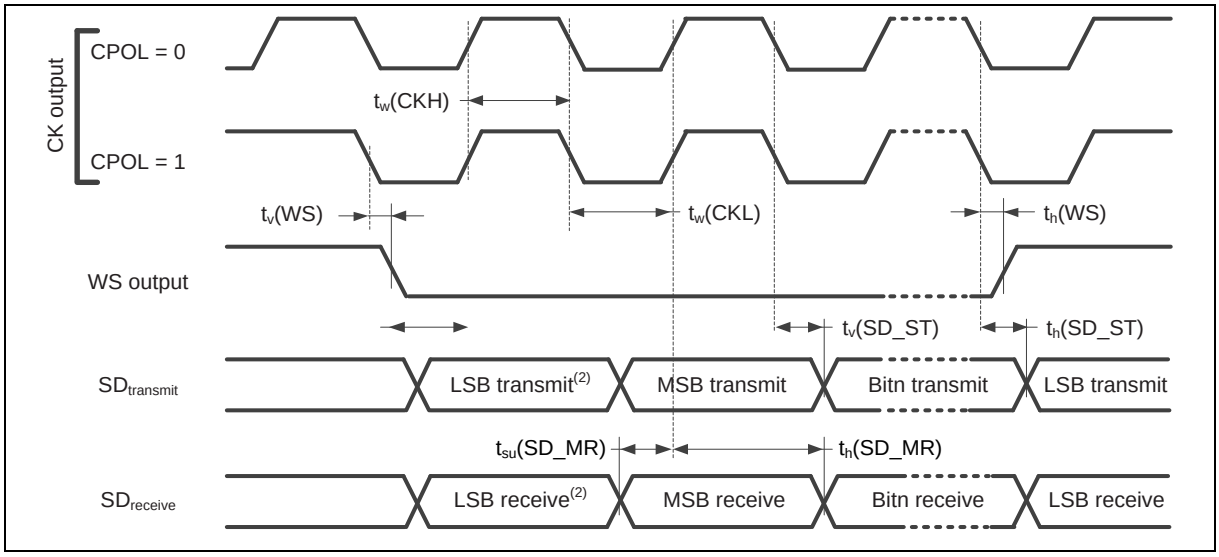


Figure 8.6-3 I2S Master Mode Timing Diagram

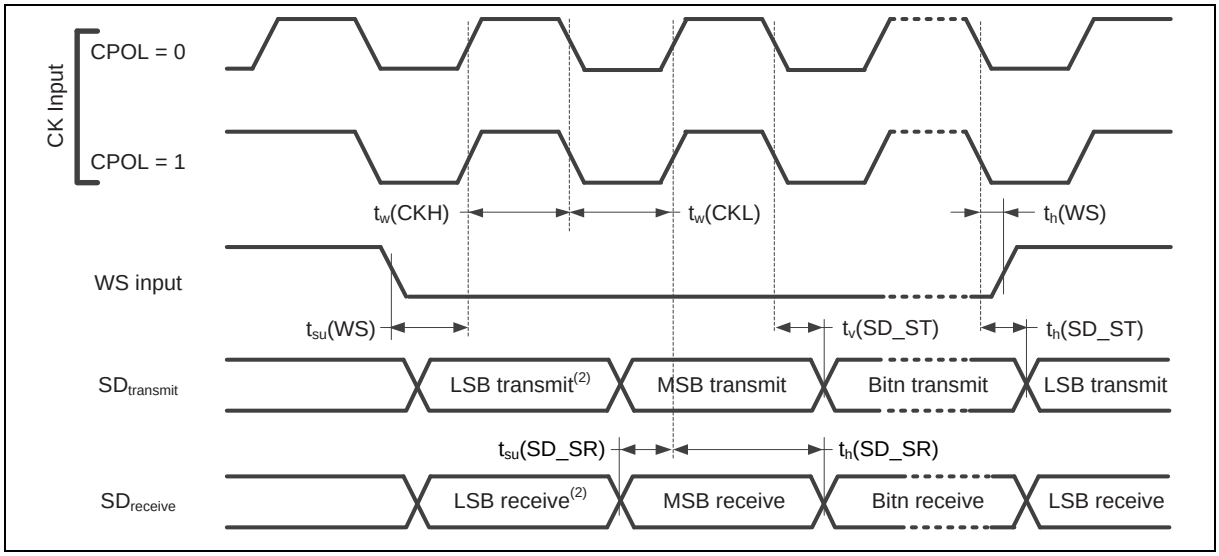


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	µS
t_{HIGH}	SCL high period	4	-	0.6	-	µS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	µS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C Characteristics

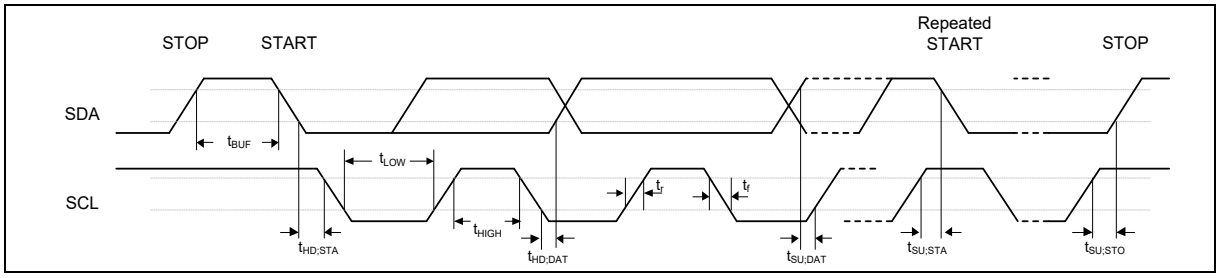


Figure 8.6-5 I²C Timing Diagram

8.6.4 USB Characteristics

8.6.4.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	4.4	-	5.25	V	
VDD_{33}[*2]	USB Internal power regulator output	3.0	3.3	3.6	V	
V_{IH}	Input high (driven)	2.0	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.2	-	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2.0	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up resistor	1.19	-	1.9	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3.0	-	3.6	V	
Z_{DRV}[*3]	Driver output resistance	-	10	-	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Notes:

1. Guaranteed by characterization result, not tested in production.
2. To ensure stability, an external 1 μF output capacitor, 1uF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 44Ω).

Table 8.6-5 USB Full-Speed Characteristics

8.6.4.2 USB Full-Speed PHY characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	nS	C_L=50 pF
T_{FF}	fall time	4	-	20	nS	C_L=50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-6 USB Full-Speed PHY Characteristics

8.6.5 SPD5 I3C Dynamic Characteristics

Symbol	Parameter	I²C Mode (Open Drain)		I3C Basic (Push-Pull)		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency	0.01	1	0	12.5	MHz
t_{HIGH}	Clock pulse width high time	260	-	35	-	nS
t_{LOW}	Clock pulse width low time	500	-	35	-	nS
$t_{TIMEOUT}$	Detect clock low time	10	50	10	50	mS
t_R	SDA rise time	-	120	-	5	nS
t_F	SDA fall time	-	120	-	5	nS
$t_{SU:DAT}$	Data in setup time	50	-	4	-	nS
$t_{HD:DI}$	Data in hold time	0	-	3	-	nS
$t_{SU:STA}$	Start condition setup time	260	-	14	-	nS
$t_{HD:STA}$	Start condition hold time	260	-	28	-	nS
$t_{SU:STO}$	Stop condition setup time	260	-	14	-	nS
t_{BUF}	Time between Stop Condition and next Start Condition	500	-	500	-	nS
t_W	Write time	-	72.98	-	72.98	µS
t_{INIT}	Time from power on to first command	-	10	-	10	mS
t_{RST}	Device reinitialization time	-	5.84	-	5.84	mS
Note: f_{HCLK} = 72 MHz						

Table 8.6-7 SPD5 I3C Dynamic Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	-	1.8	-	V	T_A = 25°C
T_{ERASE}	Page erase time	-	25.6	-	mS	
T_{PROG}	Program time	-	72	-	µS	
I_{DD1}	Read current	-	9.5	-	mA	
I_{DD2}	Program current	-	10	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Cycling Endurance	20,000	-	-	cycles[2]	
T_{RET}	Data retention	10	-	-	year	20 kcycle[2], T_J = 85°C
		100	-	-	year	20 kcycle[2], T_J = 25°C

Notes:

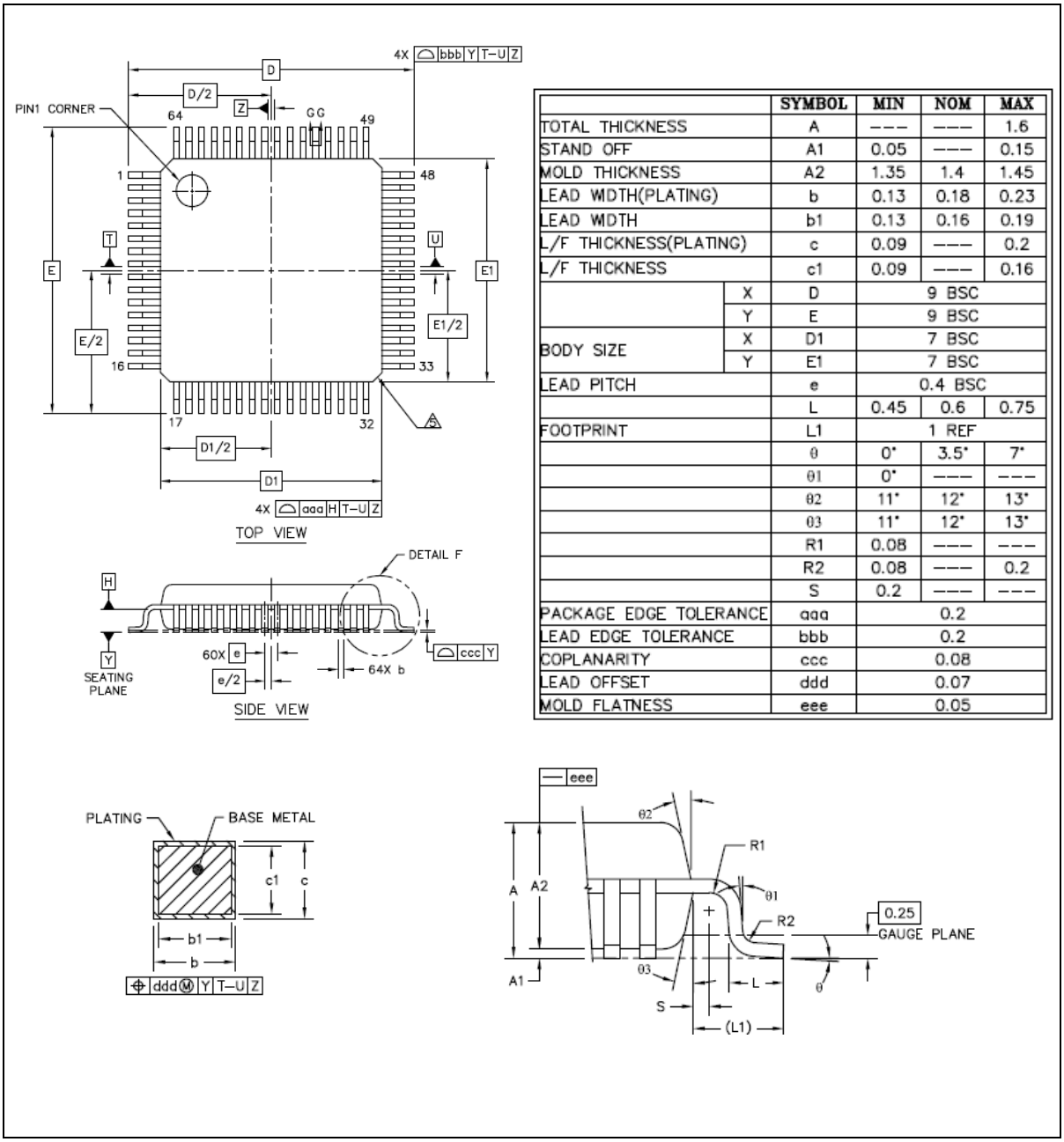
1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The Flash data can only be programmed once at the same address after Flash erase.
3. Guaranteed by design.

Table 8.7-1 Flash DC Electrical Characteristics

9 PACKAGE DIMENSIONS

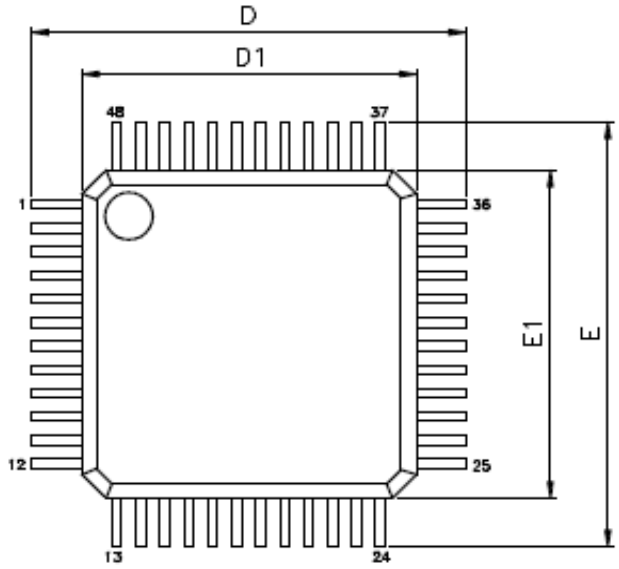
Package is Halogen-free, RoHS-compliant and TSCA-compliant.

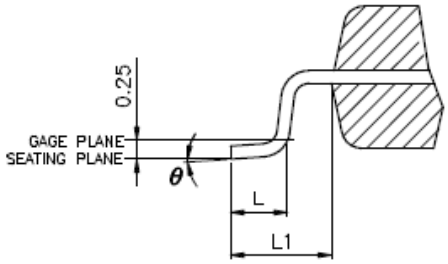
9.1 LQFP 64L (7x7x1.4 mm footprint 2.0 mm)

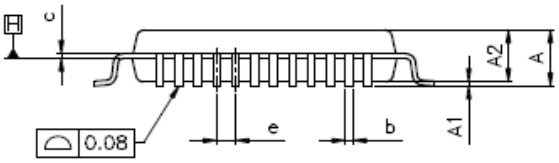


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

9.2 LQFP 48L (7x7x1.4 mm footprint 2.0 mm)



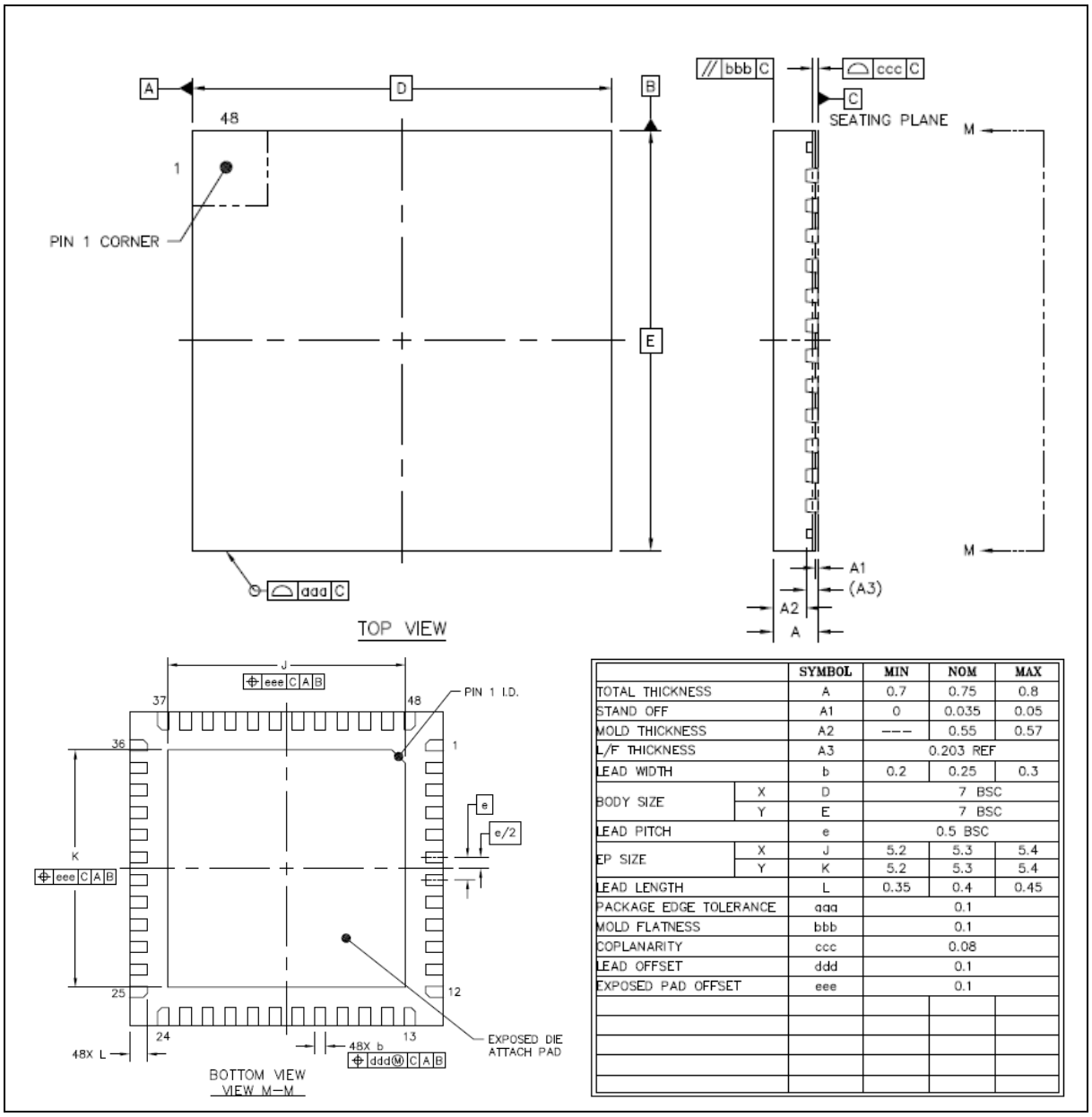




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

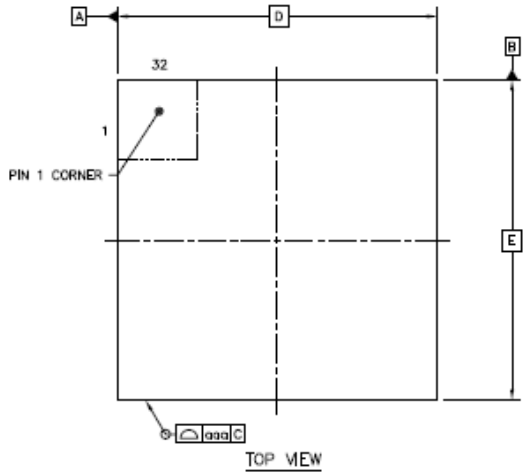
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	--	--
θ	0°	3.5°	7°
θ1	0°	--	--
θ2	11°	12°	13°
θ3	11°	12°	13°

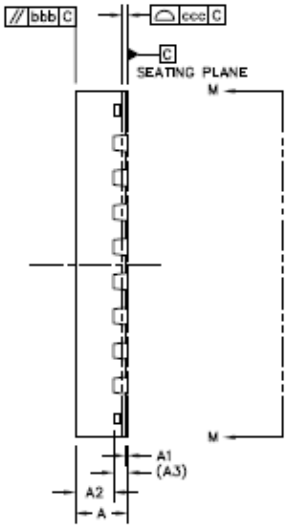
9.3 QFN 48L (7x7x0.8 mm)



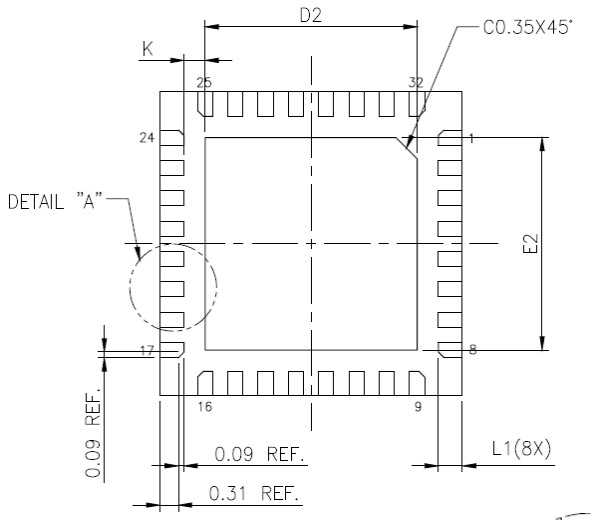
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

9.4 QFN 33L (5x5x0.8 mm)

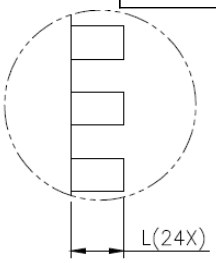




mm



SYMBOLS	Min	Nom	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A3		0.2 REF	
b	0.18	0.25	0.3
D		5.0 BSC	
E		5.0 BSC	
e		0.5 BSC	
D2	3.45	3.5	3.55
E2	3.45	3.5	3.55
L	0.35	0.4	0.45
L1	0.33	0.4	0.43
K	0.2	-	-



DETAIL "A"

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital

SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2023.06.06	1.00	Initial version.
2023.11.14	1.01	Updated the part number NUC1263ZD4AE/NUC1263ND4AE/NUC1263LD4AE/NUC1263SD4AE to NUC1263ZD4CE/NUC1263ND4CE/NUC1263LD4CE/NUC1263SD4CE in section 3.1 to 3.3 and section 4.1 to 4.2.

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.