NUF6106FCT1

6 Channel EMI Pi-Filter Array with ESD Protection

This device is a 6 channel EMI filter array for data lines. Greater than −20 dB attenuation is obtained at frequencies from 800 MHz to 2.2 GHz. It also offers ESD protection − clamping transients from static discharges to protect delicate data line circuitry.

Features

- EMI Filtering and ESD Protection for Data Lines
- Integration of 30 Discretes Offers Cost and Space Savings
- Exceeds IEC61000−4−2 (Level 4) Specifications
- Low Profile Flip−Chip Packaging
- MSL 1

Typical Applications

- EMI Filtering and ESD Protection for Data Lines
- Cell Phones
- Handheld Portables
- Notebook Computers
- MP3 Players

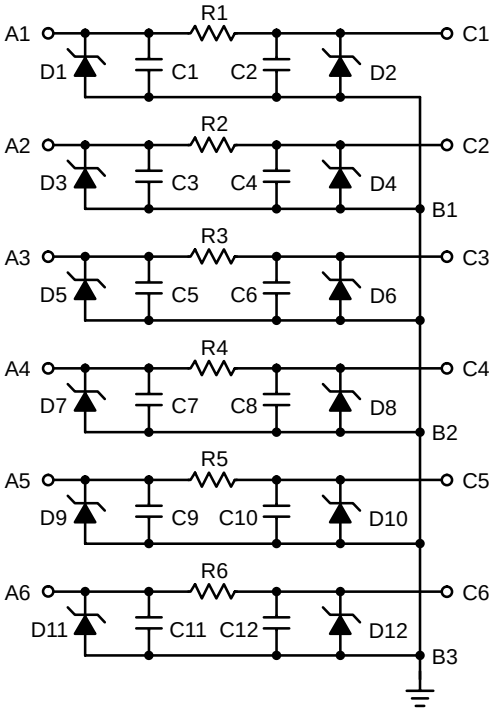
MAXIMUM RATINGS (T_A = 25°C)

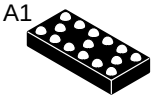
Rating	Symbol	Value	Unit
ESD Discharge IEC61000−4−2, − Contact Discharge Human Body Model Machine Model	V_{PP}	 8.0 16 1.6	kV
DC Power per Resistor	P_R	100	mW
DC Power per Package	P_T	600	mW
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_{op}	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ON Semiconductor®

http://onsemi.com

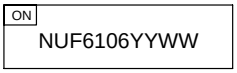
CIRCUIT DESCRIPTION





FLIP−CHIP
CASE 499D
PLASTIC

DEVICE MARKING



NUF6106= Specific Device Code
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NUF6106FCT1	Flip−Chip	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{BR}	I_Z = 10 mA	6.0	7.0	8.0	V
I_R	V_{RM} = 3.3 V per line	−	−	0.1	μA
$R_{I/O}$	I_R = 20 mA	80	100	120	Ω
C_{line}	V_R = 2.5 V, f = 1 MHz (Note 1)	−	21	23	pF

1. Measured from Input/Output Pins to Ground

TYPICAL PERFORMANCE CURVES

(T_A = 25°C unless otherwise specified)

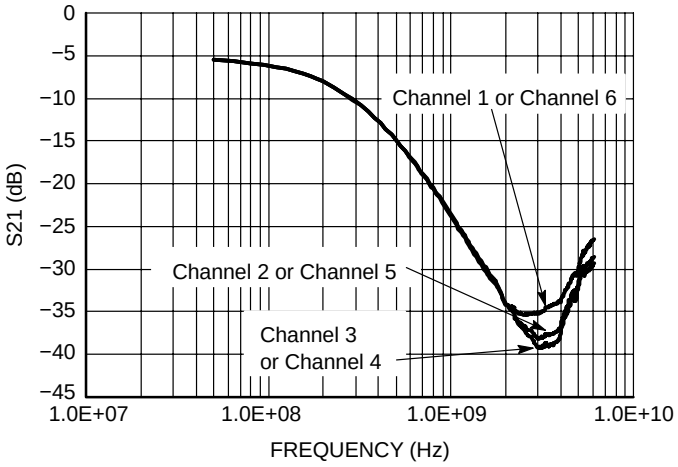


Figure 1. Insertion Loss Characteristics (S21 Measurement)

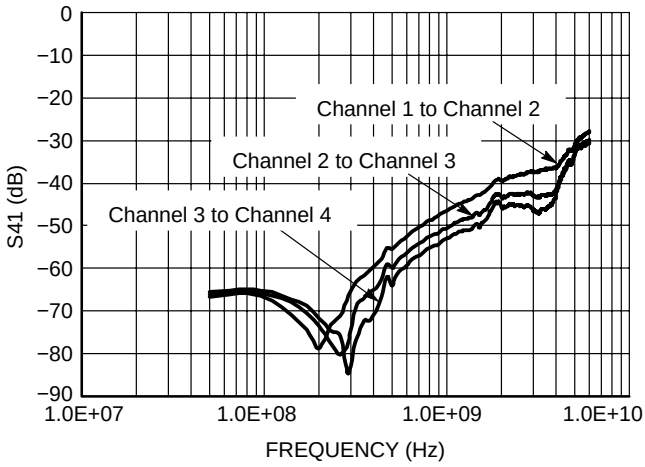


Figure 2. Analog Crosstalk Curve (S41 Measurement)

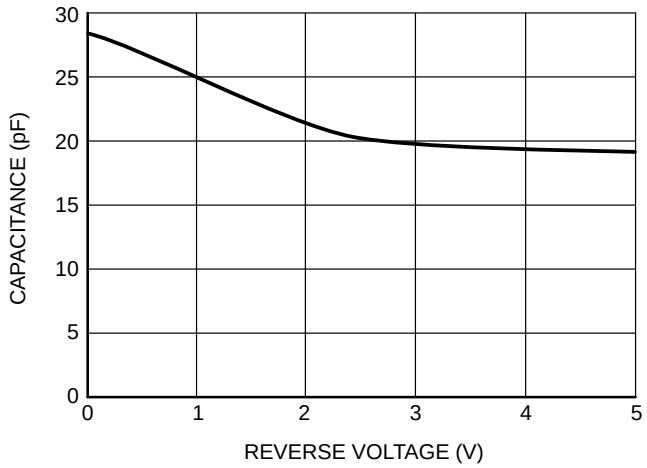


Figure 3. Typical Line Capacitance vs. Reverse Bias Voltage

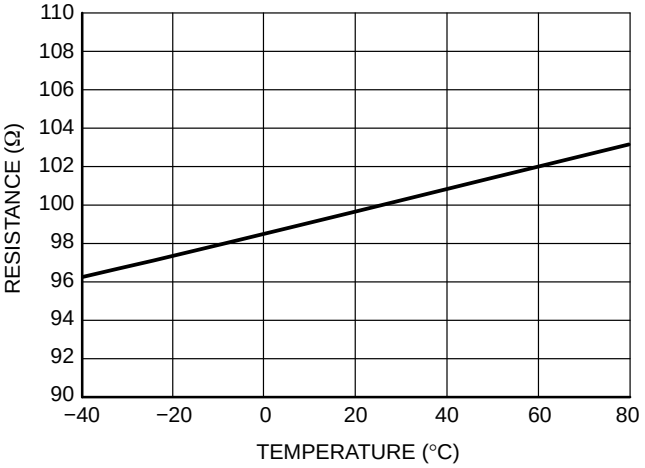


Figure 4. Typical Resistance Over Temperature

Printed Circuit Board Recommendations

Parameter	500 μm Pitch 300 μm Solder Ball
PCB Pad Size	250 μm +25 −0
Pad Shape	Round
Pad Type	NSMD
Solder Mask Opening	350 μm ±25
Solder Stencil Thickness	125 μm
Stencil Aperture	250 x 250 μm sq.
Solder Flux Ratio	50/50
Solder Paste Type	No Clean Type 3 or Finer
Trace Finish	OSP Cu
Trace Width	150 μm Max

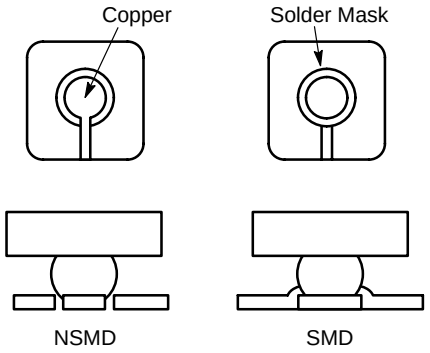


Figure 5. Solder Mask versus Non−Solder Mask Definition

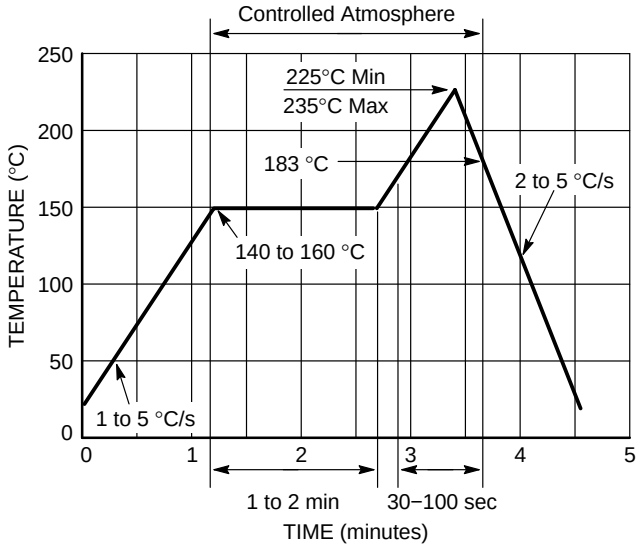
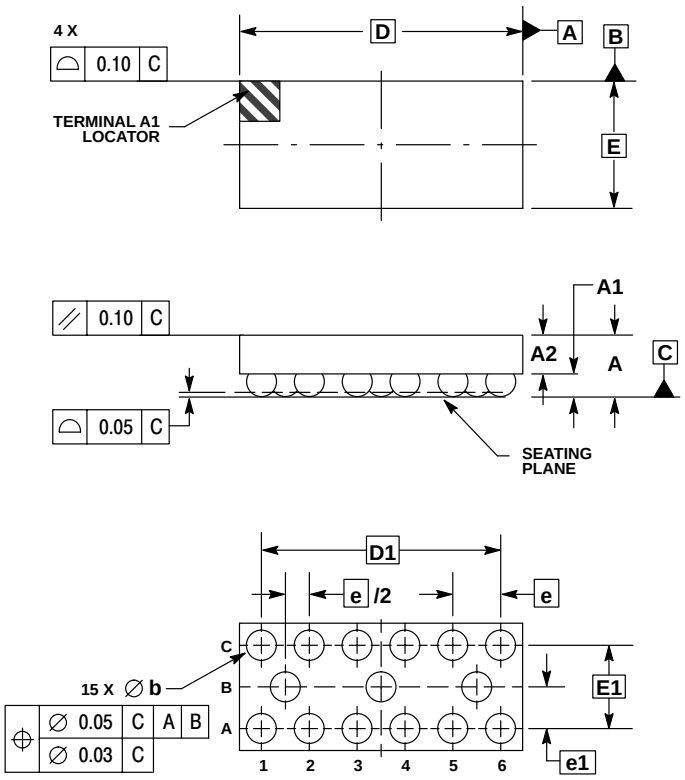


Figure 6. Solder Reflow Profile

NUF6106FCT1

PACKAGE DIMENSIONS

15 PIN FLIP−CHIP CSP
CASE 499D−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.700
A1	0.210	0.270
A2	0.380	0.430
D	2.960 BSC	
E	1.330 BSC	
b	0.290	0.340
e	0.500 BSC	
e1	0.435 BSC	
D1	2.500 BSC	
E1	0.870 BSC	

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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