

# NUP2201MR6

## Low Capacitance TSOP-6 Diode-TVS Array for High Speed Data Lines Protection

The NUP2201MR6 transient voltage suppressor is designed to protect high speed data lines from ESD, EFT, and lightning.

### Features:

- Low Capacitance (3 pF Maximum Between I/O Lines)
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (ESD) 15 kV (air) 8 kV (contact)  
IEC 61000-4-4 (EFT) 40 A (5/50 ns)  
IEC 61000-4-5 (lightning) 23 A (8/20  $\mu$ s)
- UL Flammability Rating of 94 V-0

### Typical Applications:

- High Speed Communication Line Protection
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI)
- Monitors and Flat Panel Displays
- Pb-Free Package is Available

www.DataSheet4U.com

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 $\mu$ S @ $T_A = 25^\circ\text{C}$ (Note 1)	$P_{pk}$	500	W
Operating Junction Temperature Range	$T_J$	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature - Maximum (10 Seconds)	$T_L$	235	$^\circ\text{C}$
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Air (ESD) IEC 61000-4-2 Contact (ESD)	ESD	16000 400 20000 20000	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Non-repetitive current pulse per Figure 1 (Pin 5 to Pin 2)

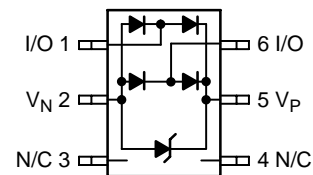


ON Semiconductor®

http://onsemi.com

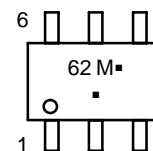
## TSOP-6 LOW CAPACITANCE DIODE TVS ARRAY 500 WATTS PEAK POWER 6 VOLTS

### PIN CONFIGURATION AND SCHEMATIC



TSOP-6  
CASE 318G  
PLASTIC

### MARKING DIAGRAM



62 = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NUP2201MR6T1	TSOP-6	3000/Tape & Reel
NUP2201MR6T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NUP2201MR6

## ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	(Note 2)			5.0	V
Breakdown Voltage	$V_{BR}$	$I_T=1\text{ mA}$ , (Note 3)	6.0			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5\text{ V}$			5.0	$\mu\text{A}$
Clamping Voltage	$V_C$	$I_{PP} = 5\text{ A}$ (Note 4)			12.5	V
Clamping Voltage	$V_C$	$I_{PP} = 8\text{ A}$ (Note 4)			20	V
Maximum Peak Pulse Current	$I_{PP}$	8x20 $\mu\text{s}$ Waveform			25	A
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f=1\text{ MHz}$ between I/O Pins and GND		3.0	5.0	pF
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f=1\text{ MHz}$ between I/O Pins		1.5	3.0	pF

- TVS devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
- $V_{BR}$  is measured at pulse test current  $I_T$ .
- Non-repetitive current pulse per Figure 1 (Pin 5 to Pin 2)

## TYPICAL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

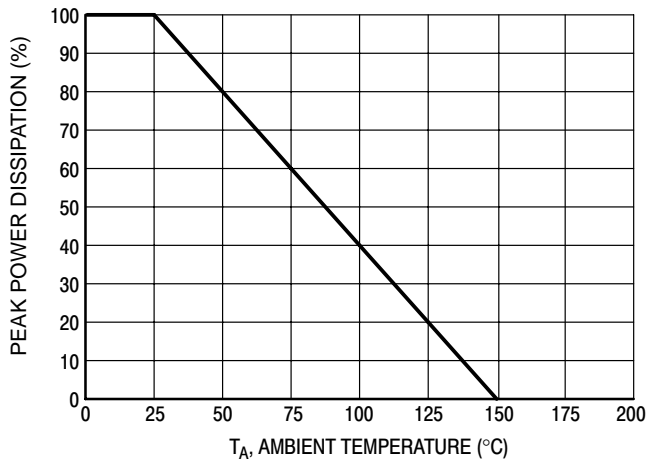


Figure 1. Pulse Derating Curve

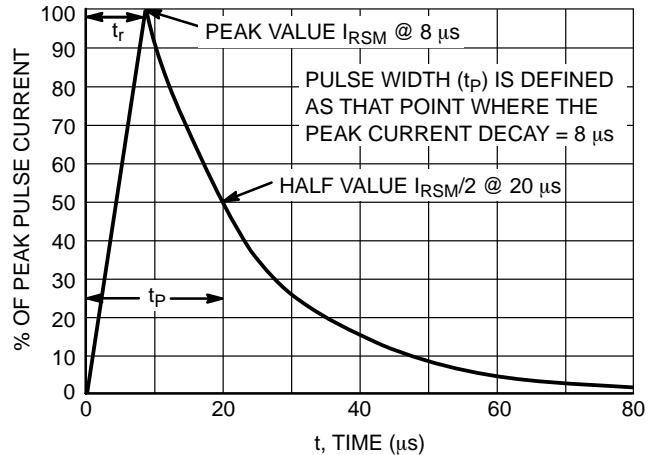


Figure 2.  $8 \times 20\ \mu\text{s}$  Pulse Waveform

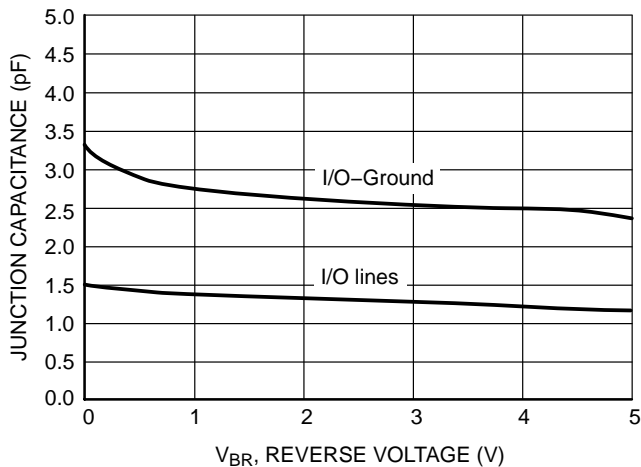


Figure 3. Junction Capacitance vs Reverse Voltage

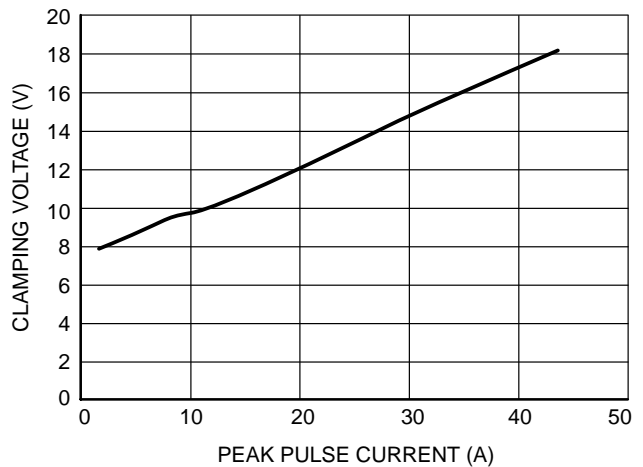


Figure 4. Clamping Voltage vs. Peak Pulse Current ( $8 \times 20\ \mu\text{s}$  Waveform)

# NUP2201MR6

## APPLICATIONS INFORMATION

The NUP2201MR6 is a low capacitance TVS diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used on high speed I/O data lines. The integrated design of the NUP2201MR6 offers surge rated, low capacitance steering diodes and a TVS diode integrated in a single package (TSOP-6). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The TVS device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

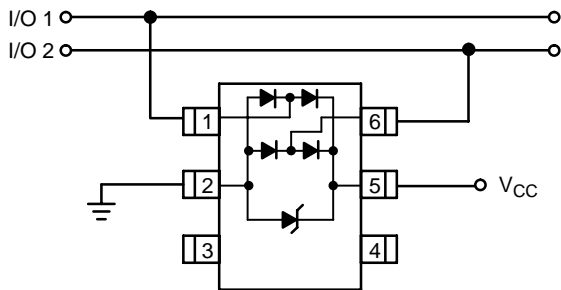
### NUP2201MR6 Configuration Options

The NUP2201MR6 is able to protect two data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage ( $V_f$  or  $V_{cc}+V_f$ ). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1 and 6. The negative reference is connected at pin 2. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductance.

#### Option 1

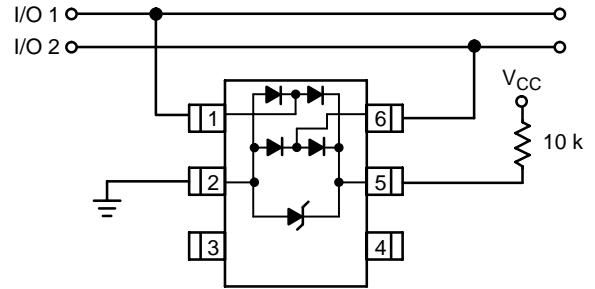
Protection of two data lines and the power supply using  $V_{cc}$  as reference.



For this configuration, connect pin 5 directly to the positive supply rail ( $V_{cc}$ ), the data lines are referenced to the supply voltage. The internal TVS diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

#### Option 2

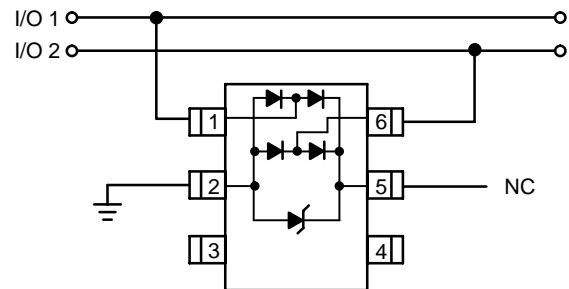
Protection of two data lines with bias and power supply isolation resistor.



The NUP2201MR6 can be isolated from the power supply by connecting a series resistor between pin 5 and  $V_{cc}$ . A 10 kΩ resistor is recommended for this application. This will maintain bias on the internal TVS and steering diodes, reducing their capacitance.

#### Option 3

Protection of two data lines using the internal TVS diode as reference.

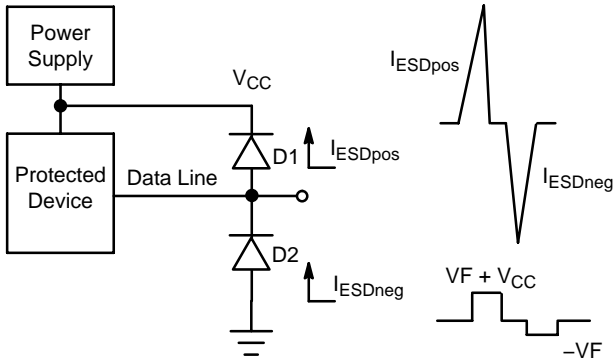


In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal TVS can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the TVS plus one diode drop ( $V_c = V_f + V_{TVS}$ ).

### ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion. Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:

# NUP2201MR6



Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

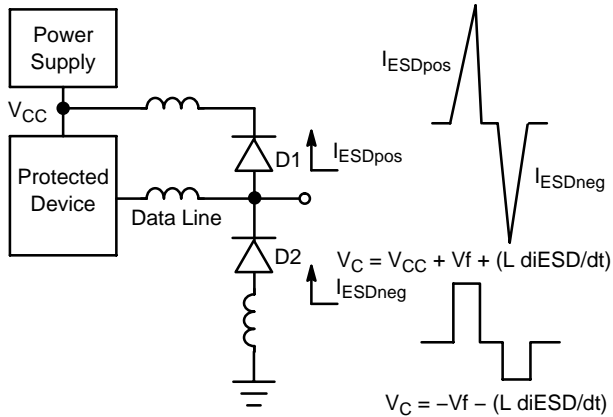
For positive pulse conditions:

$$V_c = V_{CC} + V_{fD1}$$

For negative pulse conditions:

$$V_c = -V_{fD2}$$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.



An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$$V_c = V_{CC} + V_f + (L \frac{di_{ESD}}{dt})$$

For negative pulse conditions:

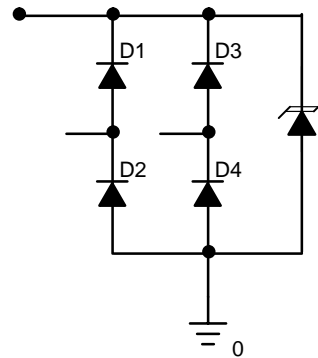
$$V_c = -V_f - (L \frac{di_{ESD}}{dt})$$

As shown in the formulas, the clamping voltage ( $V_c$ ) not only depends on the  $V_f$  of the steering diodes but also on the  $L \frac{di_{ESD}}{dt}$  factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic

inductance will provide significant benefits in transient immunity.

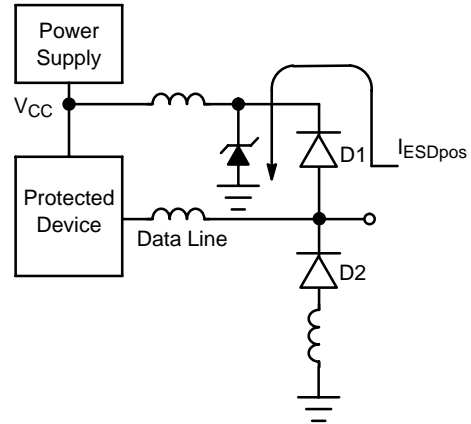
Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP2201MR6 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a TVS diode within a network of steering diodes.



NUP2201MR6 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the TVS diode as shown below.



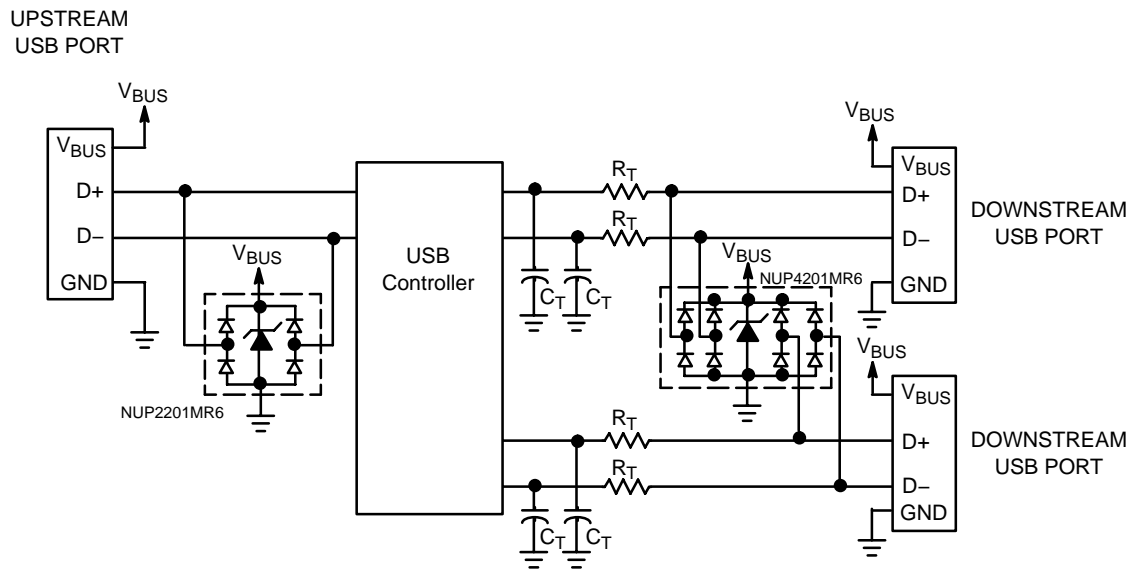
The resulting clamping voltage on the protected IC will be:

$$V_c = V_f + V_{TVS}$$

The clamping voltage of the TVS diode is provided in Figure 4 and depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

# NUP2201MR6

## TYPICAL APPLICATIONS

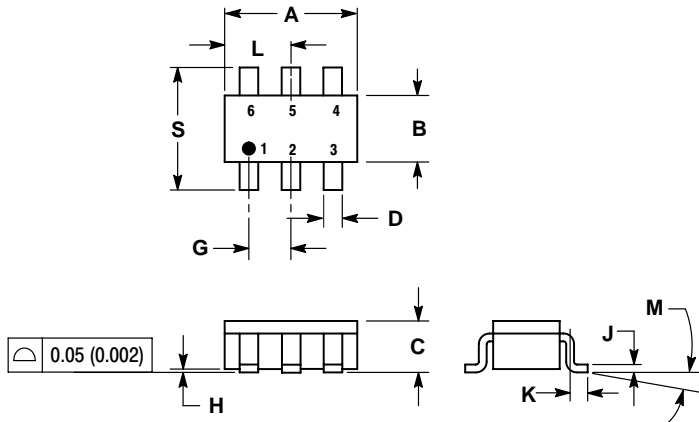


ESD Protection for USB Port

# NUP2201MR6

## PACKAGE DIMENSIONS

TSOP-6  
CASE 318G-02  
ISSUE K



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

### SOLDERING FOOTPRINT\*

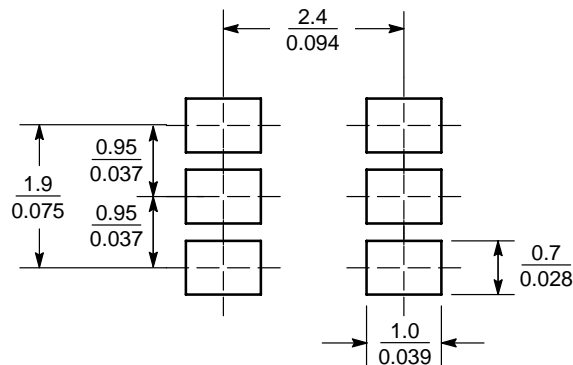


Figure 5. TSOP-6

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.