

# NUS3046MN

## Overvoltage Protection IC with Integrated MOSFET

This device represents a new level of safety and integration by combining the NCP346 overvoltage protection circuit (OVP) with a 30 V P-channel power MOSFET. This IC is specifically designed to protect sensitive electronic circuitry from overvoltage transients and power supply faults. During such hazardous events, the IC quickly disconnects the input supply from the load, thus protecting the load before any damage can occur.

The OVP IC is optimized for applications that use an external AC-DC adapter or a car accessory charger to power a portable product or recharge its internal batteries. It has a nominal overvoltage threshold of 5.5 V which makes it ideal for single cell Li-Ion as well as 3/4 cell NiCD/NiMH applications.

### Features

- Overvoltage Turn-Off Time of Less Than 1.0  $\mu$ s
- Accurate Voltage Threshold of 5.5 V, Nominal
- Control Input Compatible with 1.8 V Logic Levels
- -30 V Integrated P-Channel Power MOSFET
- Low  $R_{DS(on)}$  = 66 m $\Omega$  @ -4.5 V
- Low Profile 3.3 x 3.3 mm DFN Package Suitable for Portable Applications
- Maximum Solder Reflow temperature @ 260°C
- This is a Pb-Free Device

### Benefits

- Provide Battery Protection
- Integrated Solution Offers Cost and Space Savings
- Integrated Solution Improves System Reliability

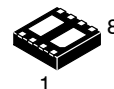
### Applications

- Portable Computers and PDAs
- Cell Phones and Handheld Products
- Digital Cameras



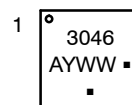
ON Semiconductor®

<http://onsemi.com>



DFN8  
CASE 506AL

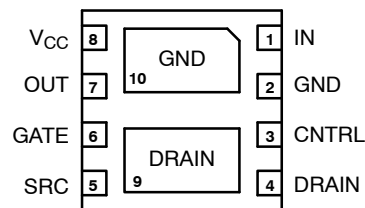
### MARKING DIAGRAM



3046 = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENT



(Bottom View)

### ORDERING INFORMATION

Device	Package	Shipping†
NUS3046MNT1G	DFN8 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NUS3046MN

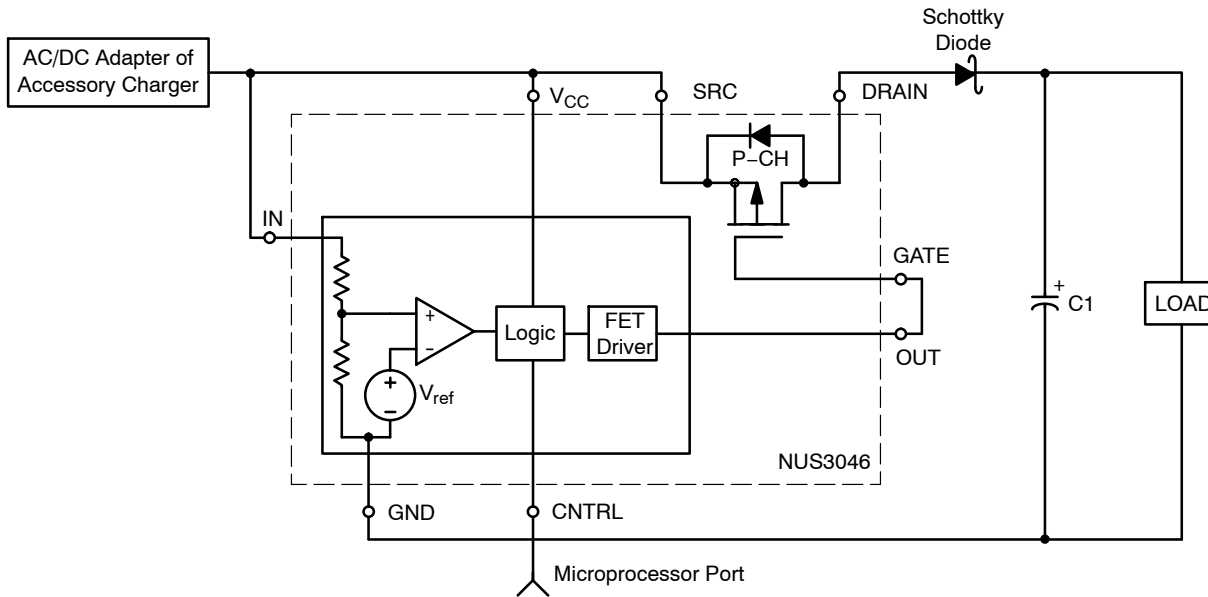


Figure 1. Simplified Schematic

## PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	IN	This pin senses an external voltage point. If the voltage on this input rises above the overvoltage threshold ( $V_{TH}$ ), the OUT pin will be driven to within 1.0 V of $V_{CC}$ , thus disconnecting the P-channel power MOSFET. The nominal threshold level is 5.5 V and this threshold level can be increased with the addition of an external resistor between IN and $V_{CC}$ .
2, 10	GND	Circuit Ground
3	CNTRL	This logic signal is used to control the state of OUT and turn-on/off the P-channel power MOSFET. A logic High results in the OUT signal being driven to within 1.0 V of $V_{CC}$ which disconnects the FET. If this pin is not used, the input should be connected to ground.
4, 9	DRAIN	Drain pin of the P-channel power MOSFET
5	SRC	Source pin of the P-channel power MOSFET
6	GATE	Gate pin of the P-channel power MOSFET
7	OUT	This signal drives the gate of a P-channel MOSFET. It is controlled by the voltage level on IN or the logic state of the CNTRL input. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of $V_{CC}$ in less than 1.0 $\mu$ sec provided that gate and stray capacitance is less than 12 nF.
8	$V_{CC}$	Positive Voltage supply. P-channel power MOSFET is guaranteed to be in ON state as long as $V_{CC}$ remains above 2.5 V and below the overvoltage threshold.

## OVERVOLTAGE PROTECTION CIRCUIT TRUTH TABLE

IN	CNTRL	OUT
$<V_{th}$	L	GND
$<V_{th}$	H	$V_{CC}$
$>V_{th}$	L	$V_{CC}$
$>V_{th}$	H	$V_{CC}$

# NUS3046MN

## MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise stated)

Rating	Pin	Symbol	Min	Max	Unit
OUT Voltage to GND	7	$V_O$	-0.3	30	V
Input and CNTRL Pin Voltage to GND	1 3	$V_{\text{input}}$ $V_{\text{CNTRL}}$	-0.3 -0.3	30 13	V
$V_{CC}$ Maximum Range	8	$V_{CC(\text{max})}$	-0.3	30	V
Maximum Power Dissipation (Note 1)	-	$P_D$	-	1.0	W
Thermal Resistance Junction-to-Air (Note 1)	-	$R_{\theta JA}$	-	108.6 104.3	$^\circ\text{C/W}$
		OVP IC P-Channel FET	- -		
Junction Temperature	-	$T_J$	-	150	$^\circ\text{C}$
Operating Ambient Temperature	-	$T_A$	-40	85	$^\circ\text{C}$
$V_{\text{CNTRL}}$ Operating Voltage	3	-	0	5.0	V
Storage Temperature Range	-	$T_{\text{stg}}$	-65	150	$^\circ\text{C}$
ESD Performance (HBM) (Note 2)	1, 2, 3, 7, 8, 10	-	2.5	-	kV
Drain-to-Source Voltage		$V_{DSS}$		-30	V
Gate-to-Source Voltage		$V_{GS}$	-20	20	V
Continuous Drain Current, Steady State, $T_A = 25^\circ\text{C}$ (Note 1)		$I_D$		-1.2	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Human body model (HBM): MIL STD 883C Method 3015-7, (R = 1500  $\Omega$ , C = 100 pF, F = 3 pulses delay 1 s).

# NUS3046MN

## OVERVOLTAGE PROTECTION IC ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 6.0\text{ V}$ , unless otherwise specified)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
$V_{CC}$ Operating Voltage Range	$V_{CC(\text{opt})}$	8	2.5 <sup>(+3)</sup>	-	25	V
Supply Current ( $I_{CC} + I_{\text{Input}}$ ; $V_{CC} = 5.0\text{ V}$ Steady State)	$I_{\text{supply}}$	1, 8	-	0.75	1.2	mA
Input Threshold ( $V_{\text{Input}}$ connected to $V_{CC}$ ; $V_{\text{Input}}$ increasing)	$V_{\text{Th}}$	1	5.3	5.5	5.7	V
Input Hysteresis ( $V_{\text{Input}}$ connected to $V_{CC}$ ; $V_{\text{Input}}$ decreasing)	$V_{\text{Hyst}}$	1	20	50	200	mV
Input Impedance (Input = $V_{\text{Th}}$ )	$R_{\text{in}}$	1	30	60	100	k $\Omega$
CNTRL Voltage High ( $V_{CC} = V_{\text{in}} = 4.0\text{ V}$ )	$V_{\text{ih}}$	3	1.5	-	-	V
CNTRL Voltage Low ( $V_{CC} = V_{\text{in}} = 4.0\text{ V}$ )	$V_{\text{il}}$	3	-	-	0.5	V
CNTRL Current High ( $V_{\text{ihCNTRL}} = 5.0\text{ V}$ , $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ )	$I_{\text{ih}}$	3	-	95	200	$\mu\text{A}$
CNTRL Current Low ( $V_{\text{ilCNTRL}} = 0.5\text{ V}$ , $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ )	$I_{\text{il}}$	3	-	10	20	$\mu\text{A}$
Output Sink Current ( $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ ; $V_{\text{OUT}} = 1.0\text{ V}$ )	$I_{\text{Sink}}$	7	4	10	16	$\mu\text{A}$
Output Voltage High ( $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ ; CNTRL = 0 V, $I_{\text{Source}} = 10\text{ mA}$ ) Output Voltage High ( $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ ; CNTRL = 0 V, $I_{\text{Source}} = 0.25\text{ mA}$ ) Output Voltage High ( $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ ; CNTRL = 0 V, $I_{\text{Source}} = 0\text{ mA}$ )	$V_{\text{oh}}$	7	$V_{CC} - 1.0$ $V_{CC} - 0.25$ $V_{CC} - 0.1$	-	-	V
Output Voltage Low ( $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ ; $I_{\text{Sink}} = 0\text{ mA}$ ; CNTRL = 0 V)	$V_{\text{ol}}$	7	-	-	0.1	V
Turn ON Delay – Input (Note 3) ( $V_{\text{Input}}$ connected to $V_{CC}$ ; $V_{\text{Input}}$ step down signal from 6.0 to 5.0 V; measured to 50% point of OUT)	$T_{\text{ON IN}}$	7	-	1.8	-	ms
Turn OFF Delay – Input ( $V_{\text{Input}}$ connected to $V_{CC}$ ; CNTRL = 0 V; $V_{\text{Input}}$ stepup signal from 5.0 to 6.0 V; $C_L = 12\text{ nF}$ ; Output > $V_{CC} - 1.0\text{ V}$ )	$T_{\text{OFF IN}}$	7	-	0.5	1.0	$\mu\text{s}$
Turn ON Delay – CNTRL ( $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ ; CNTRL step down signal from 2.0 to 0.5 V; measured to 50% point of OUT) (Note 3)	$T_{\text{ON CT}}$	7	-	10	-	$\mu\text{s}$
Turn OFF Delay – CNTRL ( $V_{CC} = V_{\text{in}} = 5.0\text{ V}$ ; CNTRL step up signal from 0.5 to 2.0 V; $C_L = 12\text{ nF}$ ; Output > $V_{CC} - 1.0\text{ V}$ )	$T_{\text{OFF CT}}$	7	-	0.6	1.0	$\mu\text{s}$

3. Guaranteed by design.

## P-CHANNEL MOSFET ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
Drain to Source On Resistance $V_{\text{GS}} = -4.5\text{ V}$ , $I_{\text{D}} = -600\text{ mA}$ $V_{\text{GS}} = -4.5\text{ V}$ , $I_{\text{D}} = -1.0\text{ A}$	$R_{\text{DS(on)}}$		66 66	110 110	m $\Omega$
Zero Gate Voltage Drain Current $V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = -24\text{ V}$	$I_{\text{DSS}}$			-1.0	$\mu\text{A}$
Turn On Delay (Note 4) $V_{\text{GS}} = -4.5\text{ V}$ , $I_{\text{D}} = -1.0\text{ A}$ , $R_{\text{G}} = 6.0\text{ }\Omega$ , $V_{\text{DS}} = -15\text{ V}$	$t_{\text{d(on)}}$		11		ns
Turn Off Delay (Note 4) $V_{\text{GS}} = -4.5\text{ V}$ , $I_{\text{D}} = -1.0\text{ A}$ , $R_{\text{G}} = 6.0\text{ }\Omega$ , $V_{\text{DS}} = -15\text{ V}$	$t_{\text{d(off)}}$		28		ns
Input Capacitance (Note 3) $V_{\text{GS}} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ , $V_{\text{DS}} = -15\text{ V}$	$C_{\text{in}}$		750		pF
Gate to Source Leakage Current $V_{\text{GS}} = \pm 20\text{ V}$ , $V_{\text{DS}} = 0\text{ V}$	$I_{\text{GSS}}$		$\pm 10$		nA
Drain to Source Breakdown Voltage $V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = -250\text{ }\mu\text{A}$	$V_{\text{(BR)DSS}}$	30			V
Gate Threshold Voltage $V_{\text{GS}} = V_{\text{DS}}$ , $I_{\text{D}} = -250\text{ }\mu\text{A}$	$V_{\text{(GS)th}}$	-3.0		-1.0	V

4. Switching characteristics are independent of operating junction temperature.

**Normal Operation**

Figure 1 illustrates a typical configuration. The external adapter provides power to the protection system so the circuitry is only active when the adapter is connected. The OVP monitors the voltage from the charger and if the voltage exceeds the overvoltage threshold,  $V_{th}$ , the OUT signal drives the gate of the MOSFET to within 1.0 V of  $V_{CC}$ , thus turning off the FET and disconnecting the source from the load. The nominal time it takes to drive the gate to this state is 400 nsec (1.0  $\mu$ sec maximum for gate capacitance of < 12 nF). The CNTRL input can be used to interrupt charging and allow the microcontroller to measure the cell voltage under a normal condition to get a more accurate measure of the battery voltage. Once the overvoltage is removed, the MOSFET will be turned on again.

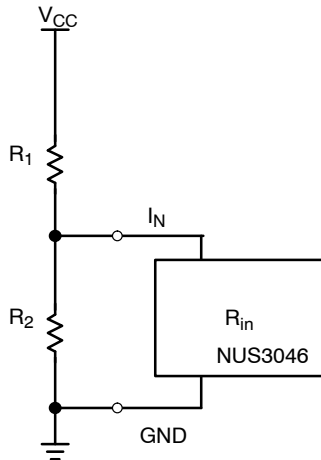
There are two events that will cause the OVP to turn off the MOSFET.

- Voltage on IN Rises Above the Overvoltage Detection Threshold
- CNTRL Input is Driven to a Logic HIGH

**Adjusting the Overvoltage Detection Point with External Resistors**

The separate IN and  $V_{CC}$  pins allow the user to adjust the overvoltage threshold,  $V_{th}$ , upwards by adding a resistor divider with the tap at the IN pin. However, the input impedance  $R_{in}$  does play a significant role in the calculation since it is several 10's of  $k\Omega$  ( $R_{in} = 54 k\Omega$  typical). The following equation shows the effects of  $R_{in}$ .

$$V_{CC} = V_x(1 + R_1/(R_2//R_{in})) \tag{eq. 1}$$



**Figure 2. Voltage divider input to adjust overvoltage detection point**

which equates to:

$$V_{CC} = V_x(1 + R_1/R_2 + R_1/R_{in}) \tag{eq. 2}$$

So, as  $R_{in}$  approaches infinity:

$$V_{CC} = V_x(1 + R_1/R_2) \tag{eq. 3}$$

This shows that  $R_{in}$  shifts the  $V_{th}$  detection point in accordance to the ratio of  $R_1 / R_{in}$ . However, if  $R_1 \ll R_{in}$ , this shift can be minimized. The following steps show this procedure.

**Designing around the Maximum Voltage Rating Requirements,  $V(V_{CC}, IN)$**

The maximum breakdown voltage between pins  $V_{CC}$  and IN is 15 V. Therefore, care must be taken that the design does not exceed this voltage. Normally, the designer shorts  $V_{CC}$  to IN,  $V(V_{CC}, IN)$  is shorted to 0 V, so there is no issue. However, one must take care when adjusting the overvoltage threshold.

In Figure 2, the  $R_1$  resistor of the voltage divider divides the  $V(V_{CC}, IN)$  voltage to a given voltage threshold equal to:

$$V(V_{CC}, IN) = V_{CC} * (R_1/(R_1 + (R_2//R_{in}))) \tag{eq. 4}$$

$V(V_{CC}, IN)$  worst case equals 15 V, and  $V_{CC}$  worst case equals 30 V, therefore, one must ensure that:

$$R_1/(R_1 + (R_2//R_{in})) < 0.5 \tag{eq. 5}$$

Where  $0.5 = V(V_{CC}, IN)_{max}/V_{CCmax}$

Therefore, the overvoltage threshold should be adjusted to voltage levels that are less than 15 V. If greater thresholds are desired, ON Semiconductor offers the NCP3045 which can withstand those voltages.

**Design Steps for Adjusting the Overvoltage Threshold**

1..Use Typical  $R_{in}$ , and  $V_{th}$  Values from the Electrical Specifications

2..Minimize  $R_{in}$  Effect by Selecting  $R_1 \ll R_{in}$  since:

$$VOV = V_{th}(1 + R_1/R_2 + R_1/R_{in}). \quad (\text{eq. 6})$$

3..Let  $X = R_{in} / R_1 = 100$ .

4..Identify Required Nominal Overvoltage Threshold.

5..Calculate nominal  $R_1$  and  $R_2$  from Nominal Values:

$$R_1 = R_{in}/X \quad (\text{eq. 7})$$

$$R_2 = \frac{R_1}{(VOV/V_{th} - R_1/R_{in} - 1)} \quad (\text{eq. 8})$$

6..Pick Standard Resistor Values as Close as Possible to these Values

7..Use min/max Data and Resistor Tolerances to

Determine Overvoltage Detection Tolerance:

$$VOV_{min} = V_{thmin}(1 + R_{1min}/R_{2max} + R_{1min}/R_{inmax}) \quad (\text{eq. 9})$$

$$VOV_{typ} = V_{thtyp}(1 + R_{1typ}/R_{2typ} + R_{1typ}/R_{intyp}) \quad (\text{eq. 10})$$

$$VOV_{max} = V_{thmax}(1 + R_{1min}/R_{2max} + R_{1max}/R_{inmin}) \quad (\text{eq. 11})$$

The specification takes into account the hysteresis of the comparator, so the minimum input threshold voltage ( $V_{th}$ ) is the falling voltage detection point and the maximum is the rising voltage detection point. One should design the input supply such that its maximum supply voltage in normal operation is less than the minimum desired overvoltage threshold.

8..Use worst case resistor tolerances to determine the maximum  $V(V_{CC}, IN)$

$$V(V_{CC}, IN)_{min} = V_{CCmax} * (R_{1min}/(R_{1min} + R_{2max})) \quad (\text{eq. 12})$$

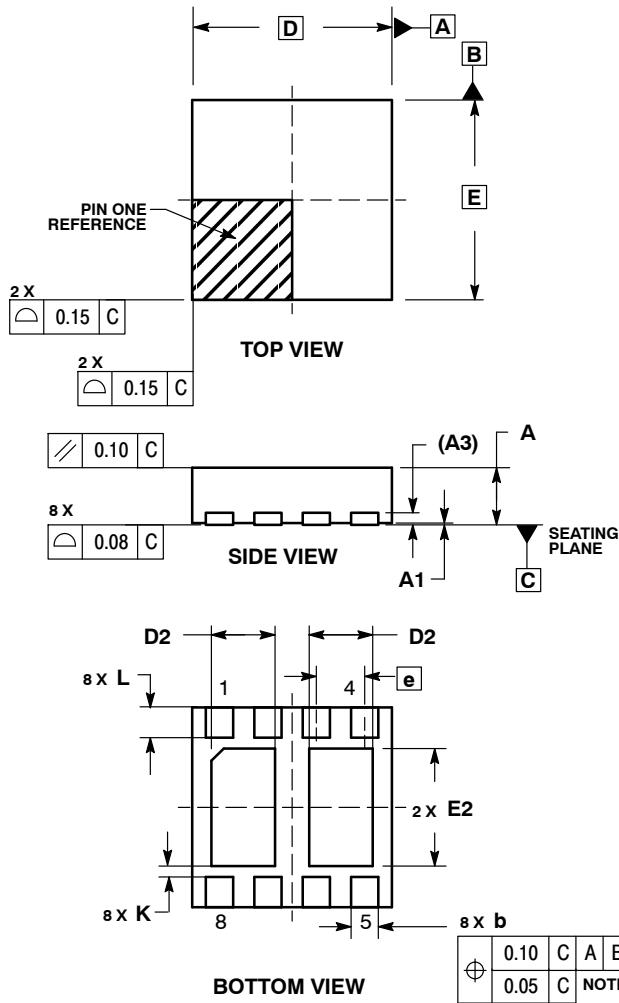
$$V(V_{CC}, IN)_{typ} = V_{CCmax} * (R_{1typ}/(R_{1typ} + R_{2typ})) \quad (\text{eq. 13})$$

$$V(V_{CC}, IN)_{max} = V_{CCmax} * (R_{1max}/(R_{1max} + R_{2min})) \quad (\text{eq. 14})$$

# NUS3046MN

## PACKAGE DIMENSIONS

DFN8  
CASE 506AL-01  
ISSUE A



**NOTES:**

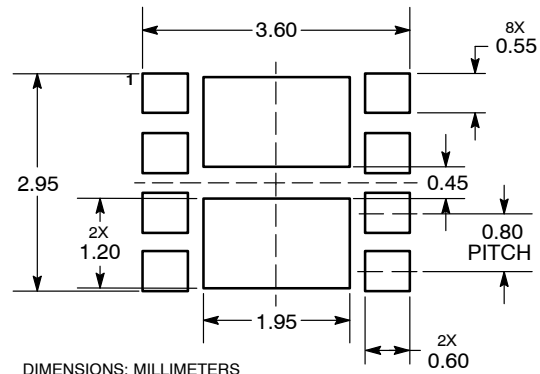
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.35	0.40	0.45
D	3.30 BSC		
D2	0.95	1.05	1.15
E	3.30 BSC		
E2	1.80	1.90	2.00
e	0.80 BSC		
K	0.21	---	---
L	0.30	0.40	0.50

**STYLE 1:**

1. PIN 1. IN
2. GND
3. CNTRL
4. DRAIN
5. SOURCE
6. GATE
7. OUT
8. VCC

**SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative