TITLE ：NV156FHM-N4H

Final Product Specification

Rev.0

(DELL DPN : 0JMJGH)

BOE Optoelectronics Technology Co., Ltd

REVISION HISTORY

( )Preliminary Specification

(√)Final Specification

Revision No.	Page	Description of Changes	Date	Prepared
P0	All	Initial Release	2018.03.15	Li Bing
P1	P26/P29~P34	Label and EDID change to X10	2018.08.09	Yang Zainian
P2	P26/P29~P34	Label and EDID change to X20	2018.12.06	Yang Zainian
0	P26/P29~P34	Label and EDID change to A00	2018.12.19	Yang Zainian

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Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NV156FHM-N4H is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.6 inch diagonally measured active area with Full-HD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 262k(6bit) colors and color gamut 45%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.2 interface compatible.

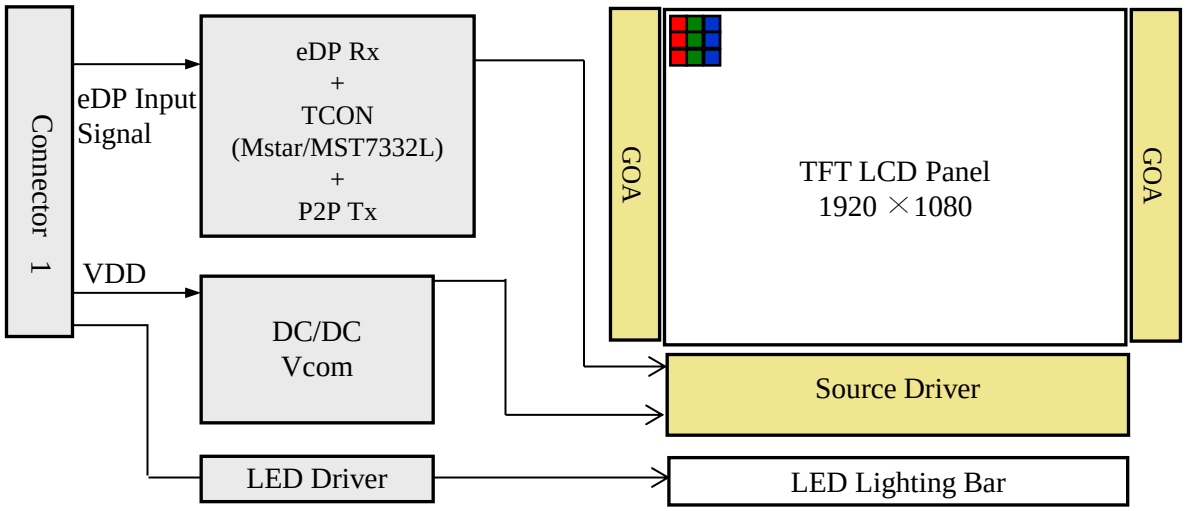


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 262k(6bit) color depth, color gamut 45%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip

1.3 Application

● Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV156FHM-N4H. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.16(H) ×193.59(V)	mm	
Number of pixels	1920 (H) ×1080 (V)	pixels	
Pixel pitch	179.25(H) ×179.25(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	262k(6bit)		
Color gamut	45%		NTSC
Display mode	Normally Black		
Dimensional outline	350.66±0.3(H)×205.69±0.3(V)×1.6 Max for FPC(V)×3.0±0.15(W/O PCB) 350.66±0.3(H)×205.69±0.3(V)×1.6 Max for FPC(V)×5.4(Max)(W PCB)	mm	
Weight	380 (max)	g	
Surface treatment	AG		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P_D : 0.88	W	@Mosaic
	P_{BL} : 2.6	W	Max
	P_{Total} : 3.48	W	@Mosaic

Notes : 1. LED Lighting Bar (40*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2˚C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	˚C	Note 2
Storage Temperature	T_{ST}	-20	+60	˚C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
90 % RH Max. (40 ˚C ≥ Ta) Maximum wet - bulb temperature at 39 ˚C or less. (Ta > 40 ˚C) No condensation.

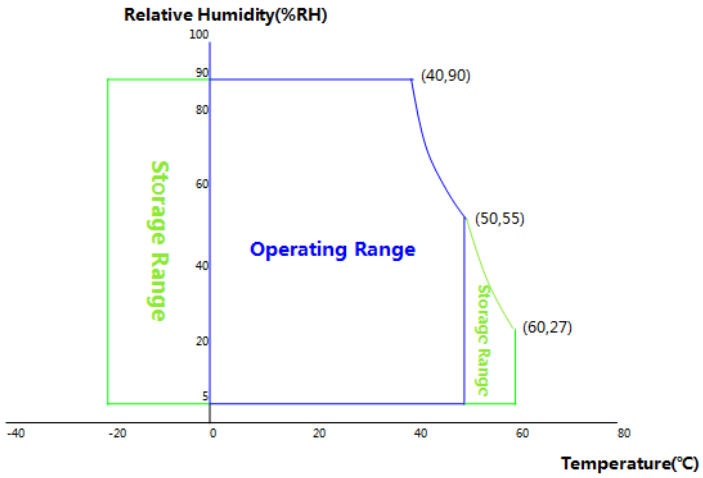


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

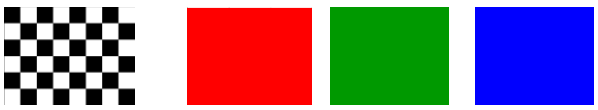
3.1 Electrical Specifications

< Table 3. Electrical Specifications > Ta=25+/-2˚C

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V_{RF}	-10%*V_{DD}	-	10%*V_{DD}	V	Note4
CABC Control Level	High Level	2.0	2.5	3.6	V	
	Low Level	0	-	0.6	V	
BIST Control Level	High Level	2.0	2.5	3.6	V	
	Low Level	0	-	0.6	V	
Power Supply Current	I_{DD}	-	267	485	mA	Note 1
Power Supply Inrush Current	Inrush	-	-	2.0	A	Note3
Power Consumption	P_D	-	0.88	1.6	W	Note 1
	P_{BL}	-	-	2.6	W	Note 2
	P_{total}	-	3.48	4.2	W	Note 1

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 ˚C.
   a) Typ : Mosaic pattern 8*8
   b) Max : R/G/B patterns



(a) (b)

Figure 3. Power Measure Patterns

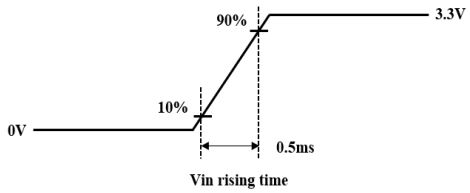


Figure 4. Inrush Measure Condition

2. Calculated value for reference (V_{LED} × I_{LED})
3. Measure condition (Figure 4)
4. Input voltage range:3.0~3.6V.Test condition: Oscilloscope bandwidth 20MHz, AC coupling.

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2˚C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	2.9	V	
LED Forward Current		I_F	-	19	-	mA	
LED Power Consumption		P_{LED}	-	-	2.6	W	Note 1
LED Life-Time		N/A	15,000	-	-	Hour	I_F = 19mA
Power Supply Voltage for LED Driver		V_{LED}	5	12	21	V	
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	2.0	A	Note 3
EN Control Level	Backlight On		2.0	-	5	V	
	Backlight Off		0	-	0.6	V	
PWM Control Level	High Level		2.0	-	3.6	V	
	Low Level		0	-	0.6	V	
PWM Control Frequency		F_{PWM}	200	-	2,000	Hz	
Duty Ratio			5	-	100	%	

Notes :

1. Power supply voltage12V for LED driver.
   Calculator value for reference IF × VF ×40 /driver efficiency = PLED
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5)

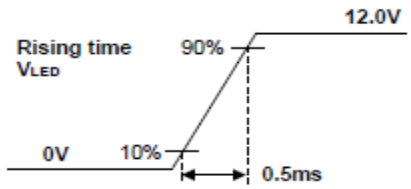


Figure 5. Inrush Measure Condition

3.3 LED Structure

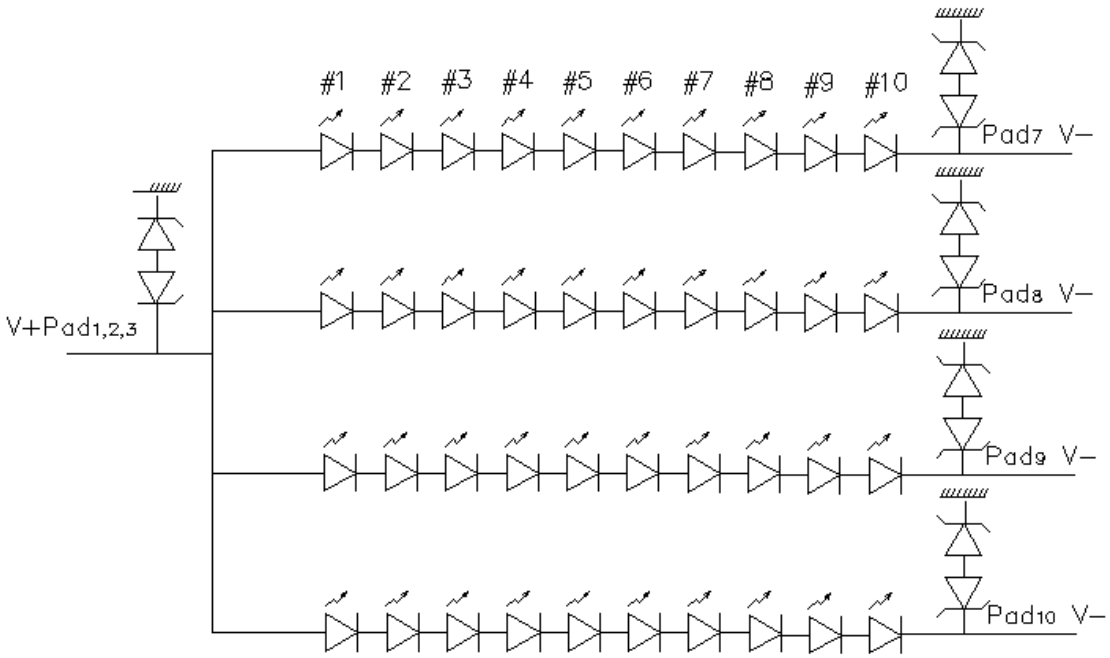


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	-	85	-	Deg.	Note 1
		Θ_9		-	85	-	Deg.	
	Vertical	Θ_{12}		-	85	-	Deg.	
		Θ_6		-	85	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	600	700			Note 2
Luminance of White	5 Points	Y_w	Θ = 0° I_{LED} = 19mA	187	220	-	cd/m²	Note 3
White Luminance Uniformity	5 Points	ΔY5		80	-	-		Note 4
	13 Points	ΔY13		65	-	-		
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	Θ = 0°	Typ.-0.03	0.585	Typ.+0.03		
		R_y			0.364			
	Green	G_x			0.350			
		G_y			0.568			
	Blue	B_x			0.163			
		B_y			0.124			
Color Gamut				43	45	-	%	
Response Time (Rising + Falling)		T_{RT}	Ta= 25℃ Θ = 0°	-	30	35	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

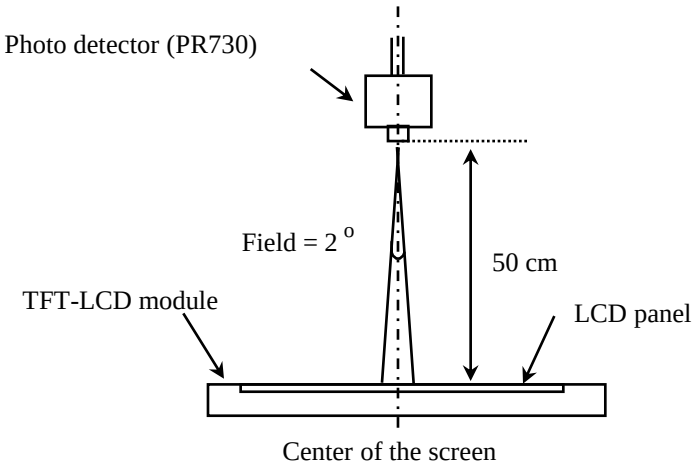
4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r, and 90% to 10% is T_f.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

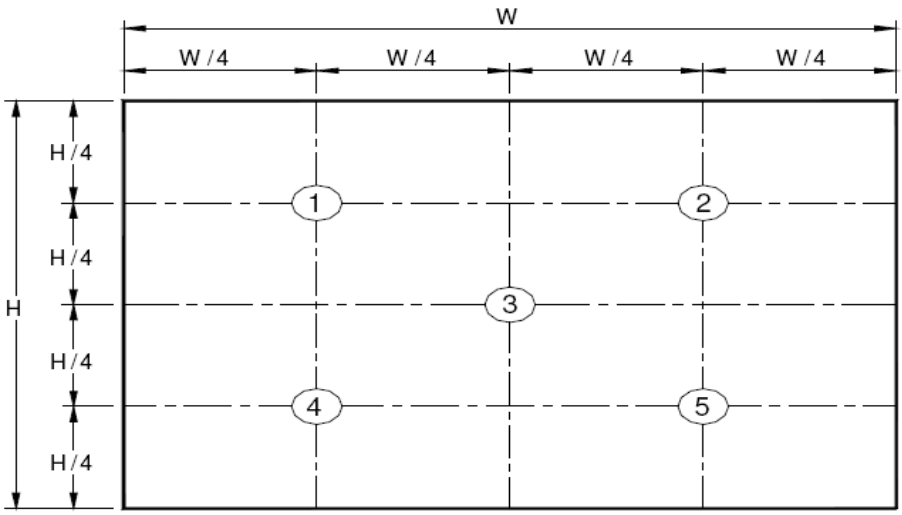


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

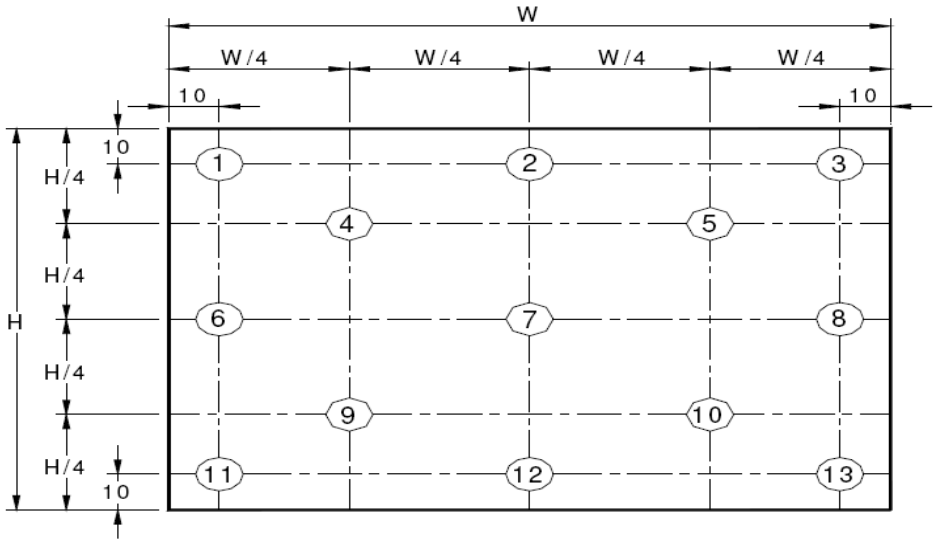


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

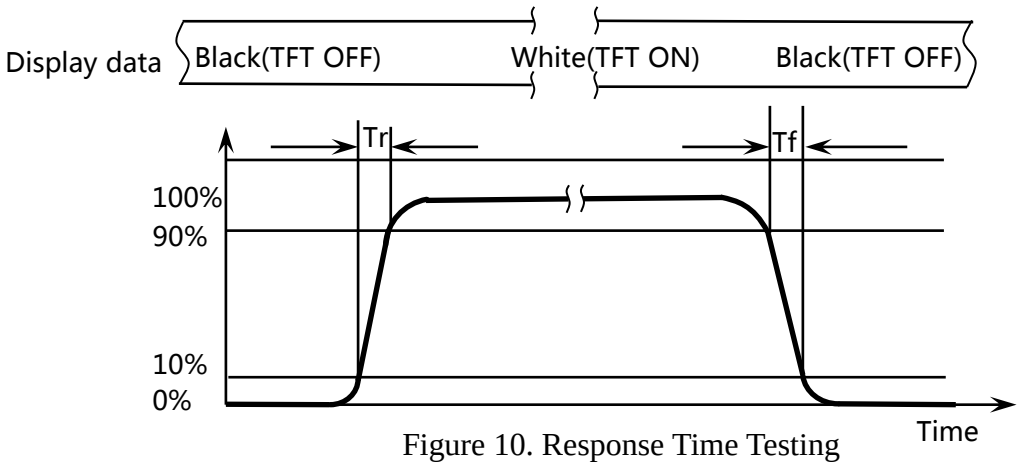
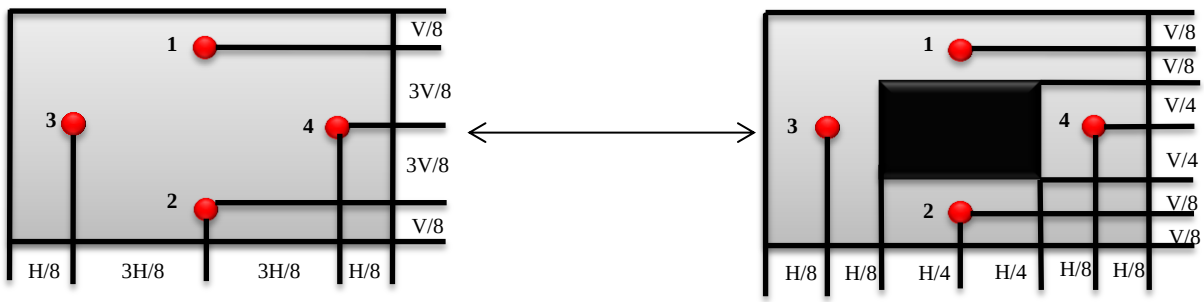


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tf: The luminance to change from 90% to 10% ,Tr: The luminance to change from 10% to 90% .

The test system : PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

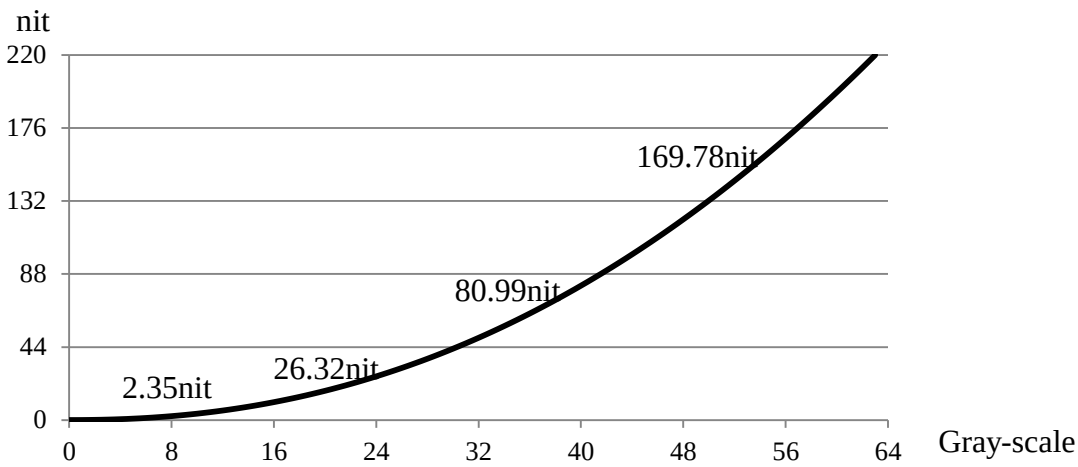


Figure 12. Brightness and Gray-scale Contrast

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is STM MSAK24025P30 or Compatible.
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	CABC_EN	CABC_Function Reserved
2	H_GND	Ground
3	LANE1_N	eDP RX channel 1 negative
4	LANE1_P	eDP RX channel 1 positive
5	H_GND	Ground
6	LANE0_N	eDP RX Channel 0 Negative
7	LANE0_P	eDP RX Channel 0 Positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH Positive
10	AUX_CH_N	eDP AUX CH Negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel Self Test Enable
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect Output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-21V
27	BL_POWER	LED Power Supply 5V-21V
28	BL_POWER	LED Power Supply 5V-21V
29	BL_POWER	LED Power Supply 5V-21V
30	NC	No Connection

5.2 eDP Interface

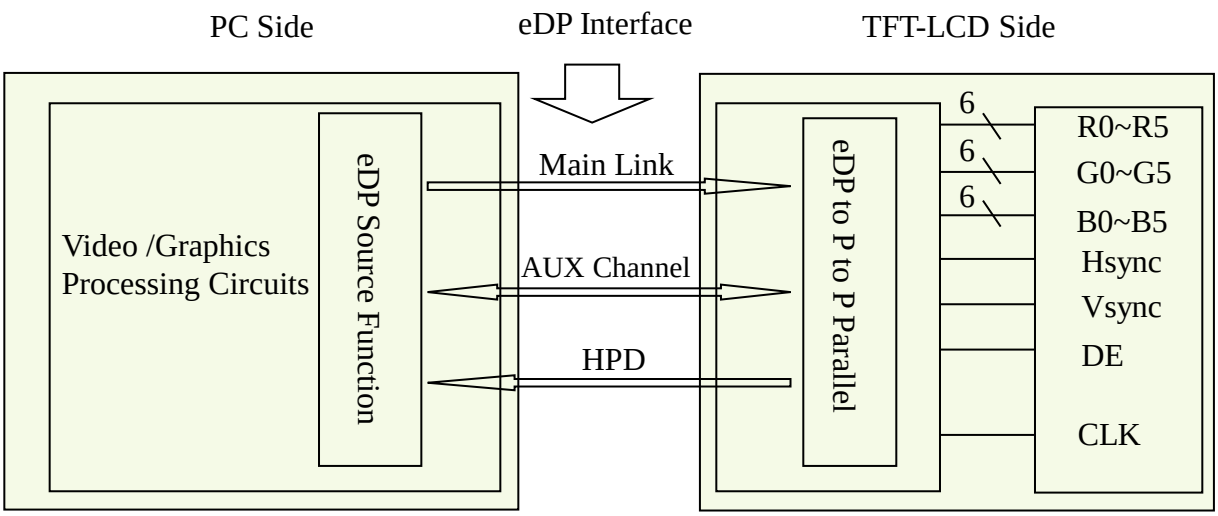


Figure 13. eDP Interface Architecture

Note:
Transmitter : Parade DP501 or equivalent.
Transmitter is not contained in module.

5.3 Data Input Format

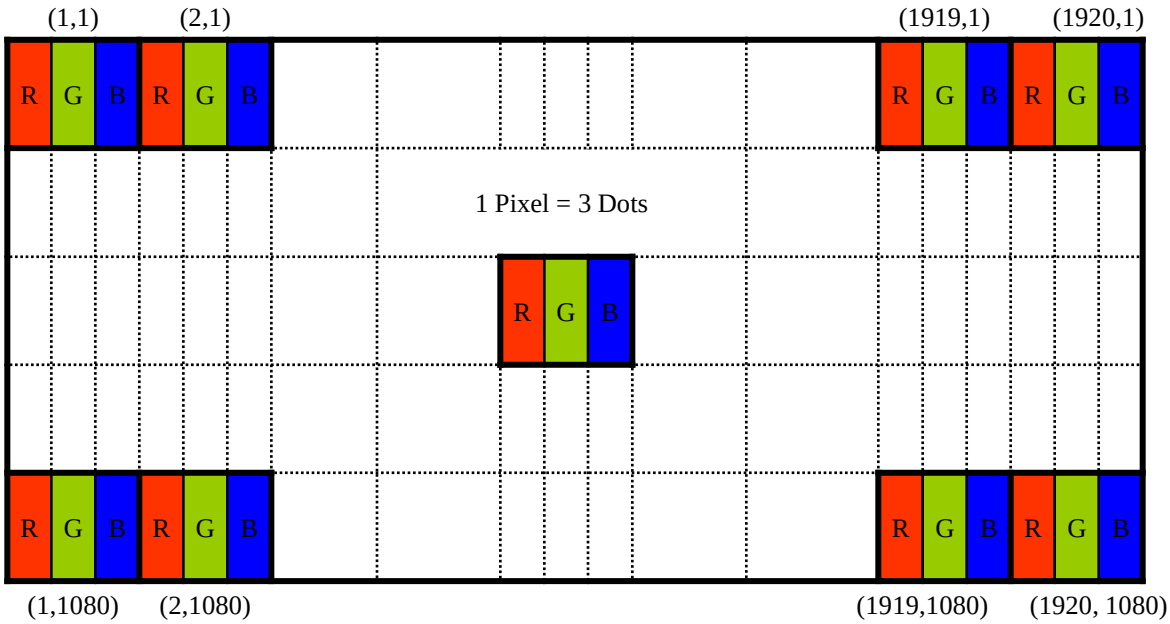


Figure 14. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: STM MSK24022P10 or Compatible.

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	NC	No Connection
2	Vout	LED anode connection	7	LED	LED cathode connection
3	Vout	LED anode connection	8	LED	LED cathode connection
4	NC	No Connection	9	LED	LED cathode connection
5	GND	Ground	10	LED	LED cathode connection

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV156FHM-N4H Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	145.1	152.5	156.6	MHz
Frame Period		Tv	1120	1140	1160	lines
			-	60	-	Hz
			-	16.7	-	ms
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	2160	2230	2250	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	0	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	100	-	1320	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	120	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	60	ps	

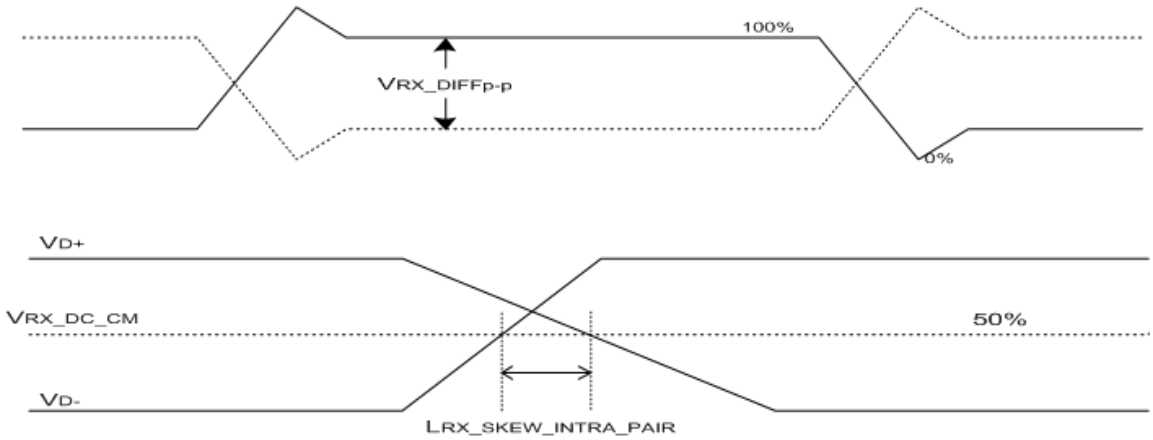


Figure 15. $V_{RX-DIFFp-p}$ & $L_{RX\_SKEW\_INTRA\_PAIR}$

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 10. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																	
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△				↑						↑						↑		
	▽				↓						↓						↓		
	Brighter	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	△				↑						↑						↑		
	▽				↓						↓						↓		
	Brighter	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	△				↑						↓						↑		
	▽				↓						↓						↓		
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	△				↑						↑						↑		
	▽				↓						↓						↓		
	Brighter	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
	▽	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

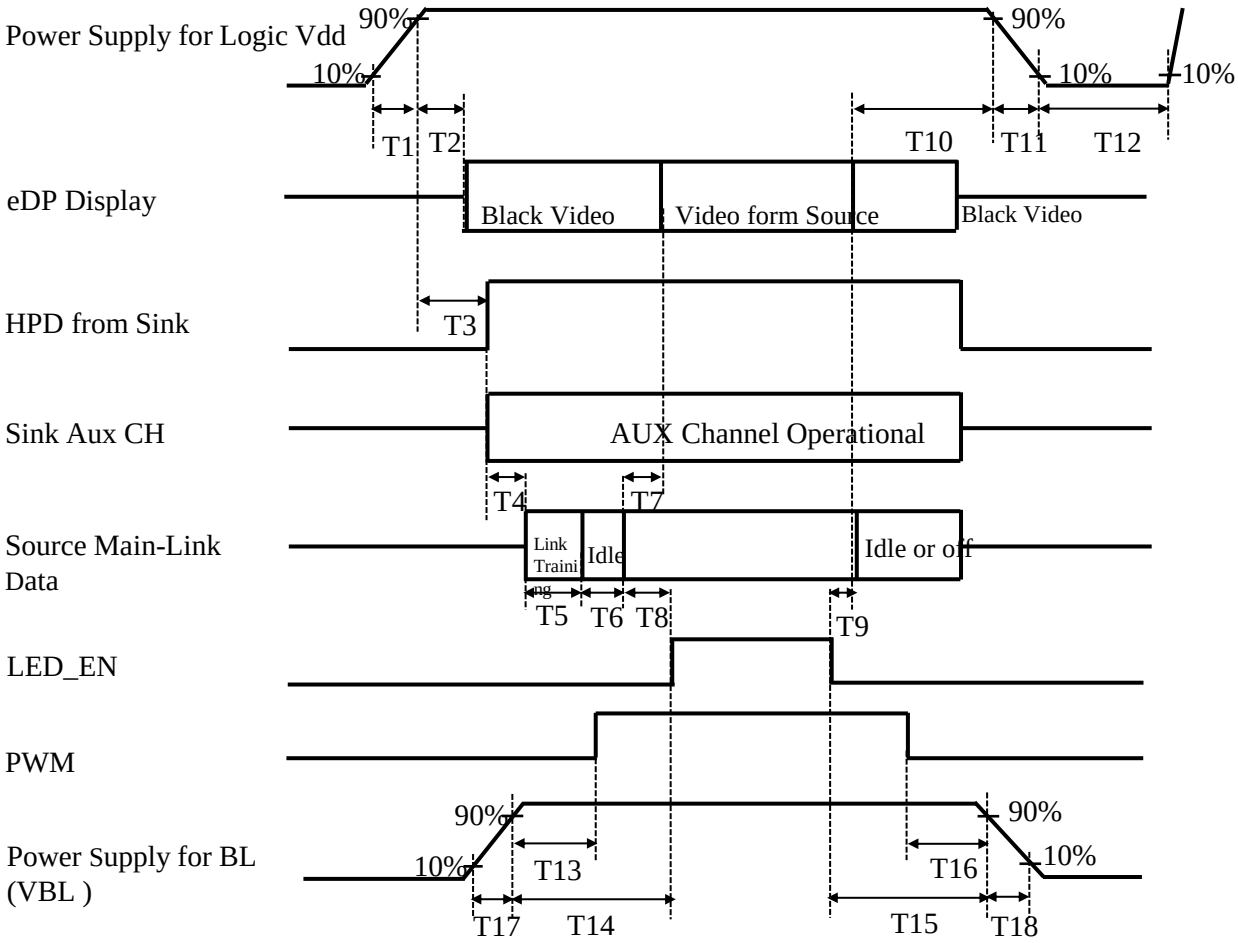


Figure 16. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T3+T4+T5+T6+T8>200ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 0ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 11. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM or Compatible
Type/ Part Number	MSAK24025P30 or Compatible
Mating Housing/ Part Number	I-PEX 20454-030T or Compatible

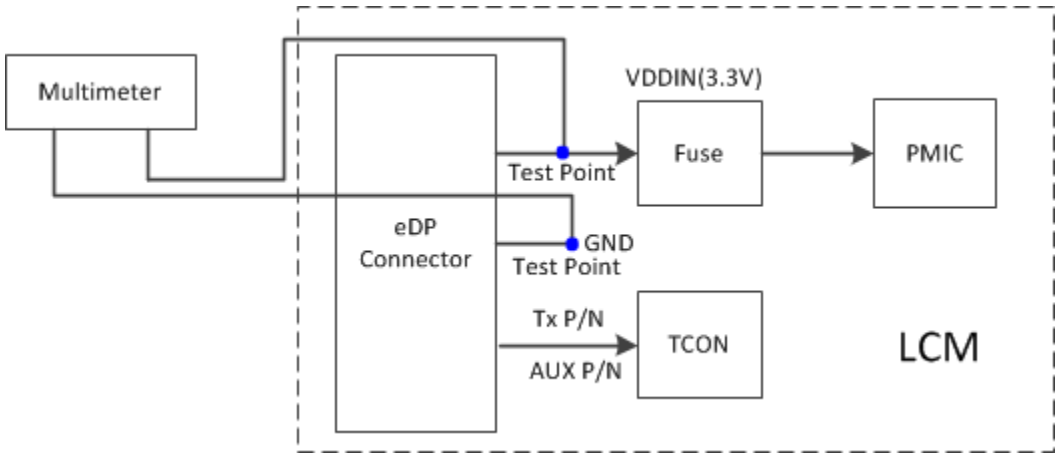
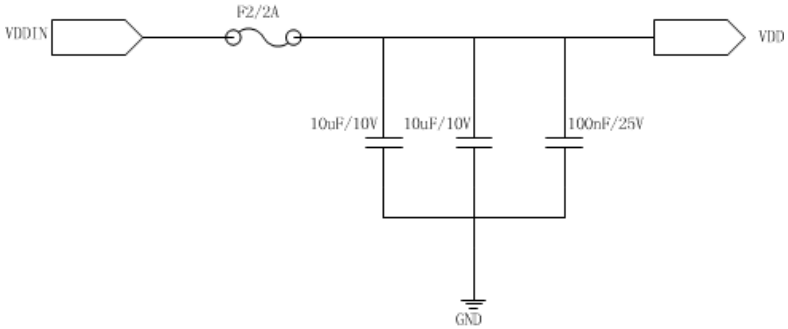


Figure 17. RC Loading test schematic diagram



Item	RC Loading	
JMJGH	R	C
	27.87kΩ	16.5uF

Figure 18. VCC Loop R/C Loading Parameter

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NV156FHM-N4H.
Other parameters are shown in Table 12.

<Table 12. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.16 (H) ×193.59 (V)	mm
Number of pixels	1920 (H) X 1080 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	179.25 (H) X 179.25 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	262K(6bit)	
Display mode	Normally Black	
Dimensional outline	350.66±0.3(H)×205.69±0.3(V)×1.6 Max for FPC(V)×3.0±0.15(W/O PCB) 350.66±0.3(H)×205.69±0.3(V)×1.6 Max for FPC(V)×5.4(Max)(W PCB)	mm
Weight	380(Max)	g

10.2 Mounting

See Figure 23.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 13. Reliability Test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 60˚C , 60%RH, 240 hrs
2	Low temperature storage test	Ta = -20˚C , 240 hrs
3	High temperature & high humidity operation test	Ta = 50˚C , 80%RH, 240 hrs
4	High temperature operation test	Ta = 50˚C , 60%RH, 240 hrs
5	Low temperature operation test	Ta = 0˚C , 240 hrs
6	Thermal shock	Ta = -20 ˚C ↔ 60 ˚C (0.5 hr), 60%±3%RH, 100 cycle
7	Vibration test (non-operating)	Ta = 25˚C , 60%RH, 1.5G, 10~500Hz, Sine X,Y, Z / Sweep rate : 1 hour
8	Shock test (non-operating)	Ta = 25˚C , 60%RH, 220G, Half Sine Wave 2msec±X,±Y,±Z Once for each direction
9	Electro-static discharge test (Operating)	Air : 150 pF, 330Ω, ±15 KV Contact : 150 pF, 330Ω, ±8 KV Ta = 25˚C , 60%RH,

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

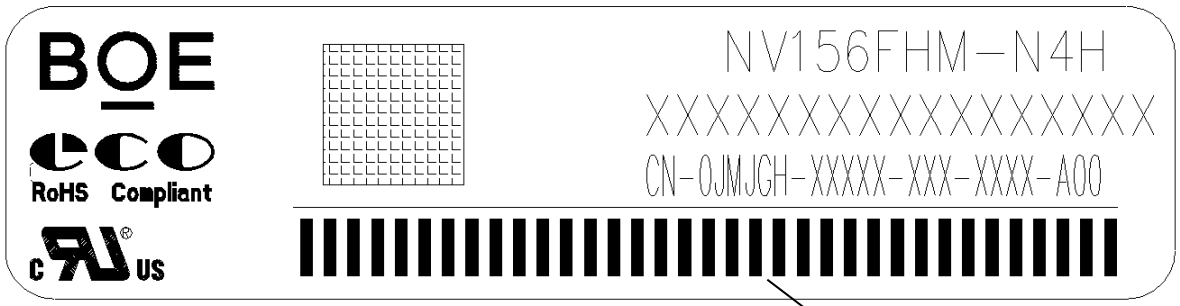


Figure 19. Product Label

Module ID Naming Rule:

<Table 14. Module ID Naming Rule>

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	B	9	A	F	1	7	8	8	D	3	8	0	0	0	0	6	8
Description	Product Name		Product Grade	B8	Year		Month	Model Extension Code (Last 4 Digits of FG CODE)				Serial No. 00001-ZZZZZZ					

(2) High voltage caution label

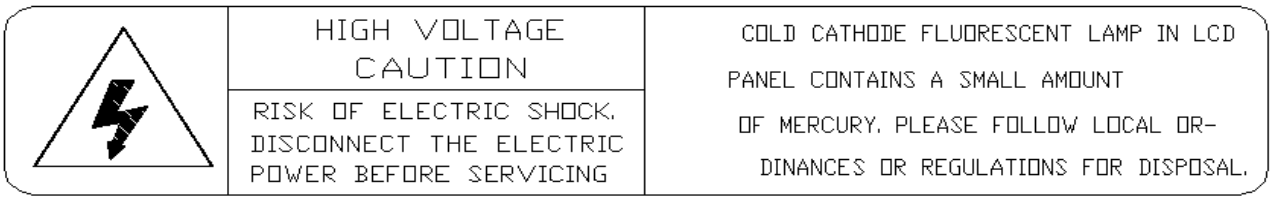


Figure 20. High Voltage Caution Label

(3) Box Label

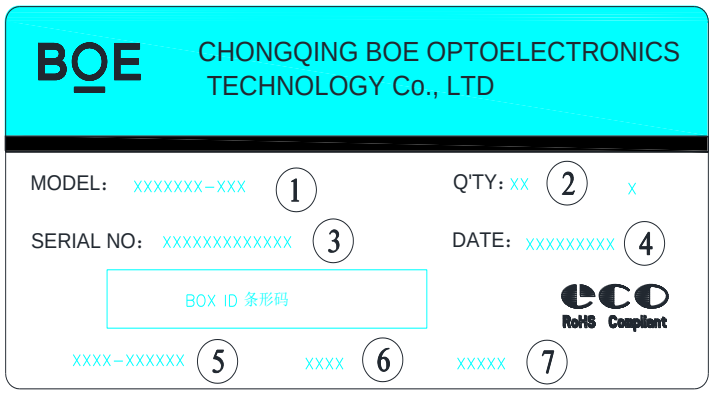


Figure 21. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code after four
7. The supplier code

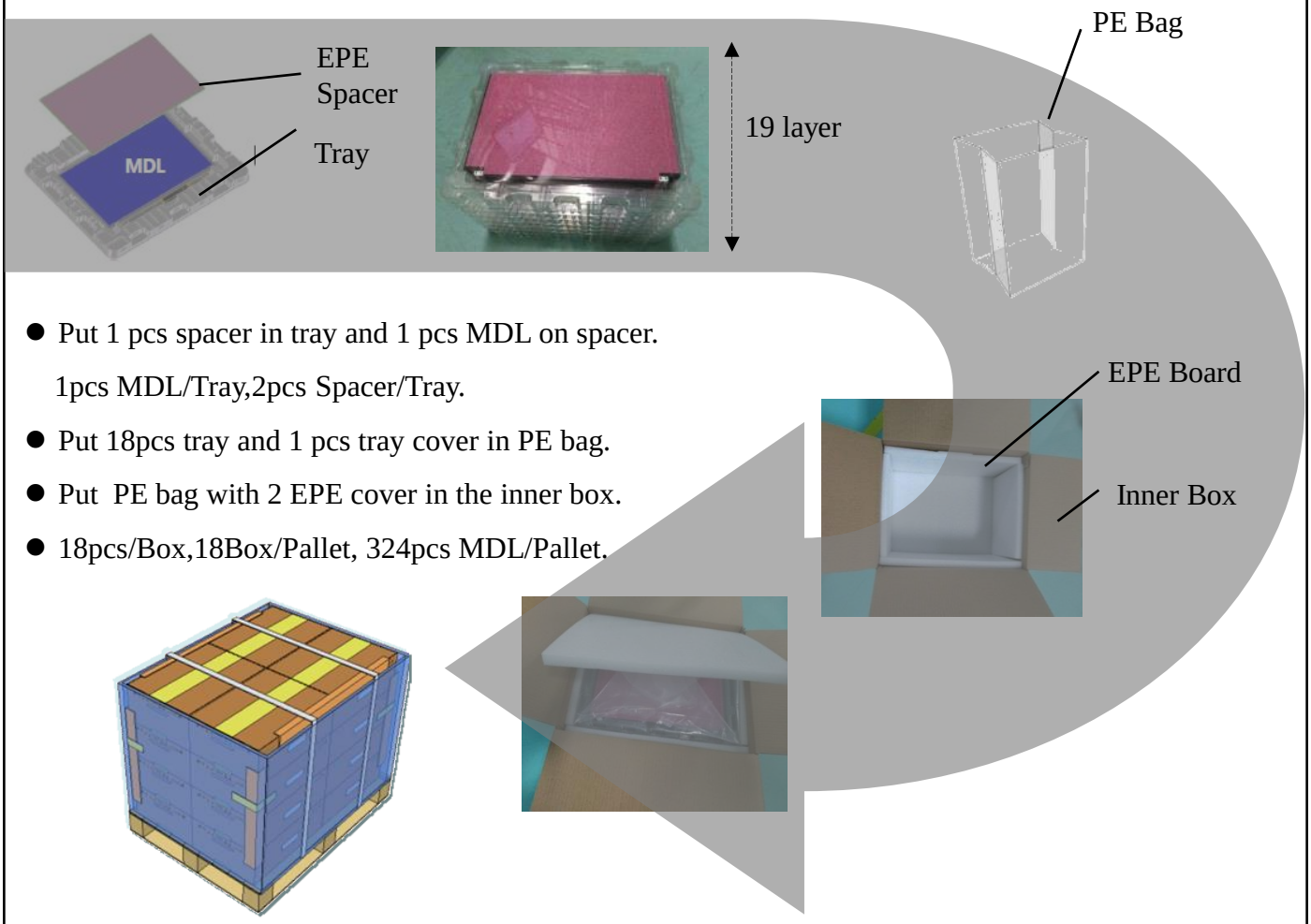
Total Size:100×50mm

<Table 15. Box Label Naming Rule >

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B8	Year		Month	Revision	BOX Serial Number				

14.0 PACKING INFORMATION

14.1 Packing Order



- Put 1 pcs spacer in tray and 1 pcs MDL on spacer.
  1pcs MDL/Tray,2pcs Spacer/Tray.
- Put 18pcs tray and 1 pcs tray cover in PE bag.
- Put PE bag with 2 EPE cover in the inner box.
- 18pcs/Box,18Box/Pallet, 324pcs MDL/Pallet.

Figure 22. Packing Order

14.2 Notes

- Box dimension: 480mm*350mm*285mm
- Package quantity in one box: 18pcs
- Total weight: 12.17kg/Box

15.0 MECHANICAL OUTLINE DIMENSION

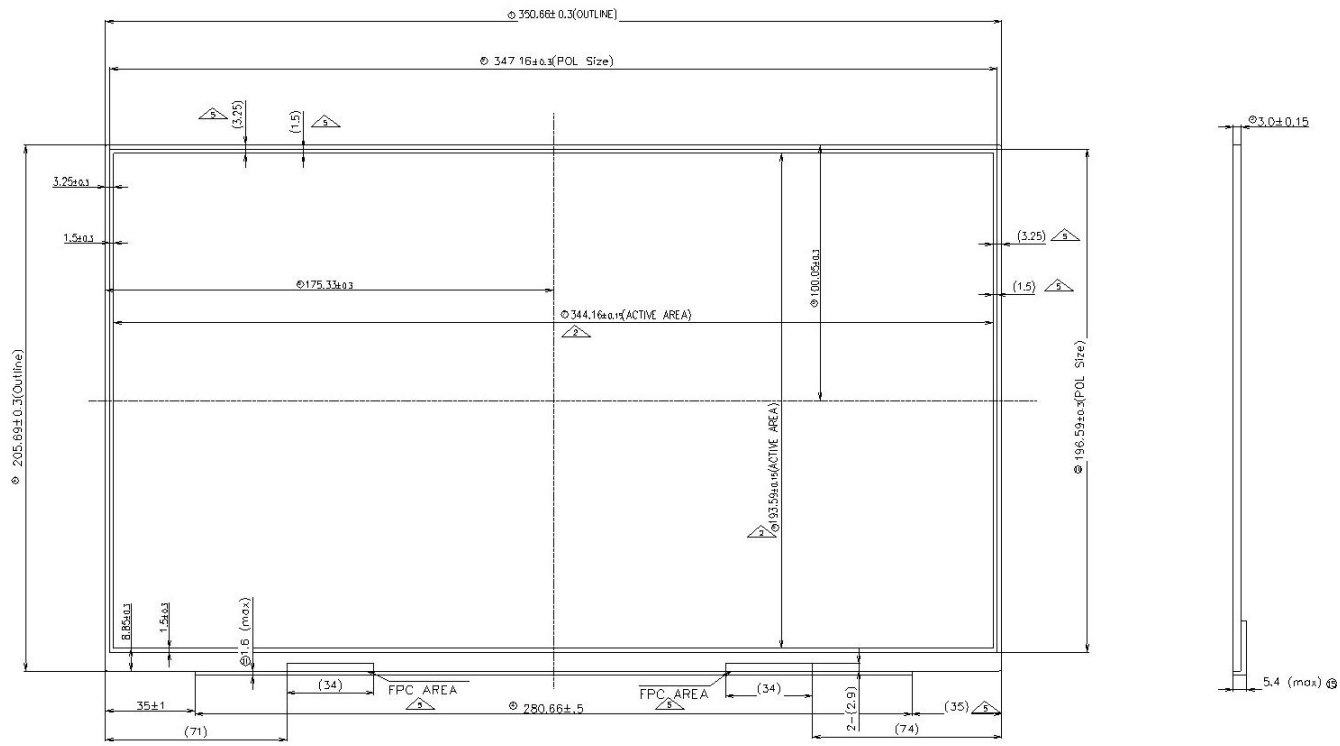


Figure 23. TFT-LCD Module Outline Dimension (Front View)

Note:

1.PCB side is lower than top polarizer and other PCB component is l ower than top polarizer

2.Warps and deformation are 0≤d≤0.5mm.

3.Top POL is the highest surface.

4.No light leakage from all 4 corners of LCM.

5.Critical sizes :①-⑮

CPK controlled sizes :①②③④ ⑪

6.Sizes measured by Vernier caliper :①②③④ ⑮

Sizes measured by 3D : ⑤⑥⑨⑩⑪ ⑫ ⑬

Sizes measured by thickness gauge : ⑭

7. Cell Tape arch height :Y direction ≤0.8mm

Z direction (behind) ≤1.5mm

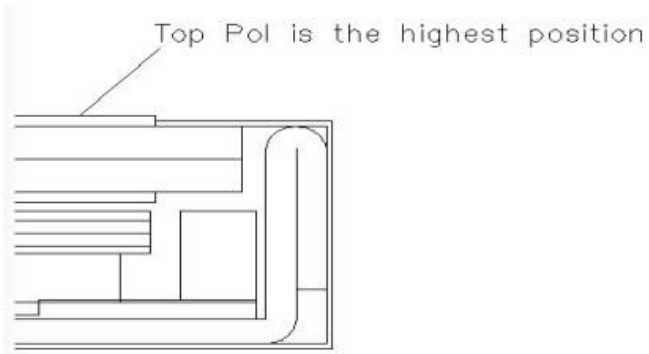


Figure 24. Highest Point Position

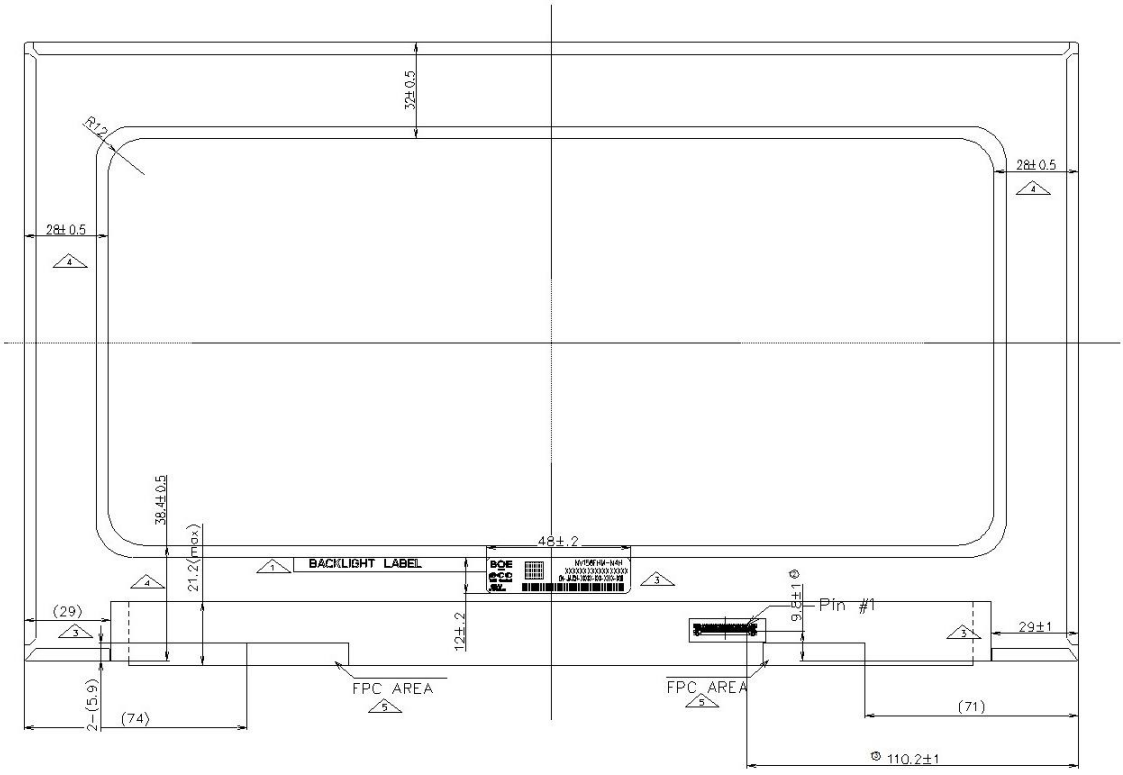


Figure 25. TFT-LCD Module Outline Dimensions (Rear view)

Note:
1.PCB side is lower than top polarizer and other PCB component is lower than top polarizer
2.Warps and deformation are 0≤d≤0.5mm.
3.Top POL is the highest surface.
4.No light leakage from all 4 corners of LCM.
5.Critical sizes :①-⑮
CPK controlled sizes :①②③④ ⑪
6.Sizes measured by Vernier caliper :①②③④ ⑮
Sizes measured by 3D : ⑤⑥⑨⑩⑪ ⑫ ⑬
Sizes measured by thickness gauge : ⑭
7. Cell Tape arch height :Y direction ≤0.8mm
Z direction (behind) ≤1.5mm

16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0	-	0	EDID Header
01		FF	255	-	255	
02		FF	255	-	255	
03		FF	255	-	255	
04		FF	255	-	255	
05		FF	255	-	255	
06		FF	255	-	255	
07		00	0	-	0	
08	ID Manufacturer Name	09	9	-	BOE	ID = BOE
09		E5	229	-		
0A	ID Product Code	D5	213	-	2005	ID = 2005
0B		07	7	-		
0C	32-bit serial No.	00	0	-	0	-
0D		00	0	-	0	
0E		00	0	-	0	
0F		00	0	-	0	
10	Week of manufacture	01	1	-	1	
11	Year of Manufacture	1C	28	-	2018	Manufactured in 2018
12	EDID Structure Ver.	01	1	-	1	EDID Ver 1.0
13	EDID revision #	04	4	-	4	EDID Rev. 0.4
14	Video input definition	95	149	-	-	Refer to right table
15	Max H image size	22	34	-	34	34 cm (Approx)
16	Max V image size	13	19	_	19	19 cm (Approx)
17	Display Gamma	78	120	_	2.2	Gamma curve = 2.2
18	Feature support	02	2	-	-	Refer to right table
19	Red/Green low bits	C9	201	_	-	Red / Green Low Bits
1A	Blue/White low bits	A0	160	_	-	Blue / White Low Bits
1B	Red x high bits	95	149	599	0.585	Red (x) = 10010101 (0.585)
1C	Red y high bits	5D	93	372	0.364	Red (y) = 01011101 (0.364)
1D	Green x high bits	59	89	358	0.350	Green (x) = 01011001 (0.35)
1E	Green y high bits	91	145	581	0.568	Green (y) = 10010001 (0.568)
1F	Blue x high bits	29	41	166	0.163	Blue (x) = 00101001 (0.163)
20	BLue y high bits	1F	31	126	0.124	Blue (y) = 00011111 (0.124)
21	White x high bits	50	80	320	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	336	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0	-	-	Refer to right table
24	Established timing 2	00	0	-	-	
25	Established timing 3	00	0	-	-	

26	Standard timing #1	01	1	-	-	Not Used
27		01	1	-	-	
28	Standard timing #2	01	1	-	-	Not Used
29		01	1	-	-	
2A	Standard timing #3	01	1	-	-	Not Used
2B		01	1	-	-	
2C	Standard timing #4	01	1	-	-	Not Used
2D		01	1	-	-	
2E	Standard timing #5	01	1	-	-	Not Used
2F		01	1	-	-	
30	Standard timing #6	01	1	_	_	Not Used
31		01	1	_	_	
32	Standard timing #7	01	1	-	-	Not Used
33		01	1	-	-	
34	Standard timing #8	01	1	-	-	Not Used
35		01	1	-	-	
36	Detailed timing/monitor descriptor #1	95	149	-	152.5	152.532MHz Main clock
37		3B	59	-		
38		80	128	-	1920	Hor Active = 1920
39		36	54	-	310	Hor Blanking = 310
3A		71	113	-	-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		38	56	-	1080	Ver Active = 1080
3C		3C	60	_	60	Ver Blanking = 60
3D		40	64	_	-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48	-	48	Hor Sync Offset = 48
3F		20	32	_	32	H Sync Pulse Width = 32
40		36	54	-	3	V sync Offset = 3 line
41		00	0	-	6	V Sync Pulse width : 6 line
42		58	88	-	344	Horizontal Image Size = 344 mm (Low 8 bits)
43		C2	194	-	194	Vertical Image Size = 194 mm (Low 8 bits)
44		10	16	_	-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0	_	0	Hor Border (pixels)
46		00	0	-	0	Vertical Border (Lines)
47		1A	26	-	-	Refer to right table

48	Detailed timing/monitor descriptor #2	FD	253	-	117.7	117.7344MHz Main clock
49		2D	45	-		
4A		80	128	-	1920	Hor Active = 1920
4B		0E	14	-	270	Hor Blanking = 270
4C		71	113	-	-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		38	56	-	1080	Ver Active = 1080
4E		28	40	-	40	Ver Blanking = 40
4F		40	64	-	-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50		30	48	-	48	Hor Sync Offset = 48
51		20	32	-	32	H Sync Pulse Width = 32
52		36	54	_	3	V sync Offset = 3 line
53		00	0	_	6	V Sync Pulse width : 6 line
54		58	88	-	344	Horizontal Image Size = 344 mm (Low 8 bits)
55		C2	194	-	194	Vertical Image Size = 194 mm (Low 8 bits)
56		10	16	-	-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0	-	0	Hor Border (pixels)
58		00	0	-	0	Vertical Border (Lines)
59		1A	26	-	-	Refer to right above table
5A	Detailed timing/monitor descriptor #3	00	0	-	-	ASCII Data Sting Tag
5B		00	0	-	-	
5C		00	0	-	-	
5D		FE	254	-	-	
5E		00	0	_	-	
5F		4A	74	_	J	Dell P/N:JMJGH
60		4D	77	-	M	
61		4A	74	_	J	
62		47	71	-	G	
63		48	72	-	H	
64		80	128	-	10000000	EDID Revison:A00
65		4E	78	-	N	BOE PN
66		56	86	_	V	
67		31	49	_	1	
68		35	53	-	5	
69		4E	78	-	N	
6A		34	52	-	4	
6B		48	72	-	H	

6C	Detailed timing/monitor descriptor #4	00	0	-	-	Flag
6D		00	0	-	-	
6E		00	0	-	-	
6F		00	0	-	-	Data Type Tag: Manufacturer Specified Data 00
70		00	0	-	-	Flag
71		00	0	-	-	6-bit Color Depth & no FRC
72		41	65	-	-	WLED & singal light bar & one light bar
73		21	33	-	-	Frame rate 40Hz~65Hz
74		96	150	-	-	Light Controller:PWM & Max. Luminance220
75		00	0	-	-	Front Surface:Anti-Glare & RGB v-stripe
76		10	16	-	-	with DBC
77		00	0	-	-	no Motion Blur & no Active Gamma
78		00	0	-	-	no Wireless Enhancement & no In-Cell Scanner
79		0A	10	-	-	2 Lane edp
7A		01	1	-	-	Built-In Self Test
7B		0A	10	-	-	Format： terminate with ASCII code 0Ah and pad field with ASCII code 20h
7C		20	32	-	-	
7D		20	32	-	-	
7E	Extension flag	00	0	-	1	0 ：1個EDID；N-1：N个EDID
7F	Checksum	6E	110	110	-	