EEPROM Serial 8/16-Kb SPI - Automotive Grade 1 in Wettable Flank UDFN8 Package

NV25080MUW, NV25160MUW

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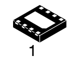
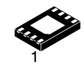




UDFN8 (2x2) (Wettable Flank) MUW2 SUFFIX CASE 517AW	UDFN8 (2x3) (Wettable Flank) MUW3 SUFFIX CASE 517DH

Description

The NV25080/25160 are EEPROM Serial 8/16−Kb SPI − Automotive Grade 1 devices internally organized as 1024x8/2048x8 bits. They feature a 32−byte page write buffer and support the Serial Peripheral Interface (SPI) protocol. The device is enabled through a Chip Select ($\overline{CS}$) input. In addition, the required bus signals are a clock input (SCK), data input (SI) and data output (SO) lines. The $\overline{HOLD}$ input may be used to pause any serial communication with the NV25080/25160 device. These devices feature software and hardware write protection, including partial as well as full array protection.

Features

- Automotive AEC−Q100 Grade 1 (−40°C to +125°C) Qualified
- 10 MHz SPI Compatible
- 1.8 V to 5.5 V Supply Voltage Range
- SPI Modes (0,0) & (1,1)
- 32−byte Page Write Buffer
- Self−timed Write Cycle
- Hardware and Software Protection
- Block Write Protection
  − Protect 1/4, 1/2 or Entire EEPROM Array
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8−Pad Wettable Flank UDFN8 Packages
- These Devices are Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

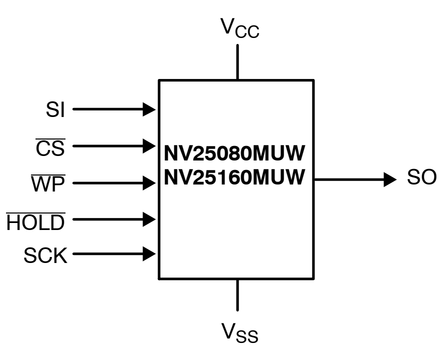
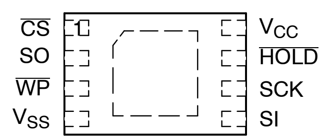


Figure 1. Functional Symbol

PIN CONFIGURATIONS



UDFN8 (MUW2, MUW3)
(Top View)

PIN FUNCTION

Pin Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock
$\overline{HOLD}$	Hold Transmission Input
V_{CC}	Power Supply

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Unit
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Unit
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C.

Table 3. DC OPERATING CHARACTERISTICS (V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Unit
I_{CCR}	Supply Current (Read Mode)	Read, V_{CC} = 5.5 V, 5 MHz, SO open		2	mA
I_{CCW}	Supply Current (Write Mode)	Write, V_{CC} = 5.5 V, 5 MHz, SO open		3	mA
I_{SB1}	Standby Current	V_{IN} = GND or V_{CC}, $\overline{CS}$ = V_{CC}, $\overline{WP}$ = V_{CC}, V_{CC} = 5.5 V		2	μA
I_{SB2}	Standby Current	V_{IN} = GND or V_{CC}, $\overline{CS}$ = V_{CC}, $\overline{WP}$ = GND, V_{CC} = 5.5 V		5	μA
I_L	Input Leakage Current	V_{IN} = GND or V_{CC}	−2	2	μA
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{CC}, V_{OUT} = GND or V_{CC}	−1	2	μA
V_{IL1}	Input Low Voltage	$V_{CC} \geq 2.5$ V	−0.5	0.3 V_{CC}	V
V_{IH1}	Input High Voltage	$V_{CC} \geq 2.5$ V	0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL2}	Input Low Voltage	$V_{CC} < 2.5$ V	−0.5	0.2 V_{CC}	V
V_{IH2}	Input High Voltage	$V_{CC} < 2.5$ V	0.8 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	I_{OL} = 3.0 mA		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	V_{CC} − 0.8 V		V

Table 4. PIN CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V) (Note 2)

Symbol	Test	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitance (SO)	V_{OUT} = 0 V			8	pF
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	V_{IN} = 0 V			8	pF

Table 5. AC CHARACTERISTICS (T_A = −40°C to +125°C) (Note 4)

Symbol	Parameter	V_{CC} = 1.8 V – 5.5 V		V_{CC} = 2.5 V – 5.5 V		Unit
		Min	Max	Min	Max	
f_{SCK}	Clock Frequency	DC	5	DC	10	MHz
t_{SU}	Data Setup Time	20		10		ns
t_H	Data Hold Time	20		10		ns
t_{WH}	SCK High Time	75		40		ns
t_{WL}	SCK Low Time	75		40		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z		50		25	ns
t_{RI} (Note 5)	Input Rise Time		2		2	μs
t_{FI} (Note 5)	Input Fall Time		2		2	μs
t_{HD}	$\overline{HOLD}$ Setup Time	0		0		ns
t_{CD}	$\overline{HOLD}$ Hold Time	10		10		ns
t_V	Output Valid from Clock Low		80		35	ns
t_{HO}	Output Hold Time	0		0		ns
t_{DIS}	Output Disable Time		50		20	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		100		25	ns
t_{CS}	$\overline{CS}$ High Time	80		40		ns
t_{CSS}	$\overline{CS}$ Setup Time	60		30		ns
t_{CSH}	$\overline{CS}$ Hold Time	60		30		ns
t_{CNS}	$\overline{CS}$ Inactive Setup Time	60		20		ns
t_{CNH}	$\overline{CS}$ Inactive Hold Time	60		20		ns
t_{WPS}	$\overline{WP}$ Setup Time	10		10		ns
t_{WPH}	$\overline{WP}$ Hold Time	15		15		ns
t_{WC} (Note 6)	Write Cycle Time		5		5	ms

4. AC Test Conditions:
   Input Pulse Voltages: 0.3 V_{CC} to 0.7 V_{CC} at V_{CC} = 2.5 V – 5.5 V and 0.2 V_{CC} to 0.8 V at V_{CC} = 1.8 V – 2.5 V.
   Input rise and fall times: ≤ 10 ns
   Input and output reference voltages: 0.5 V_{CC}
   Output load: current source $I_{OL\ max}/I_{OH\ max}$; C_L = 30 pF
5. This parameter is tested initially and after a design or process change that affects the parameter.
6. t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

Table 6. POWER−UP TIMING (Notes 5, 7)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Power−up to Read Operation	0.1	1	ms
t_{PUW}	Power−up to Write Operation	0.1	1	ms

7. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Pin Description

SI: The serial data input pin accepts op−codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.

SO: The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.

SCK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and NV25080/160.

$\overline{CS}$: The chip select input pin is used to enable/disable the NV25080/160. When $\overline{CS}$ is high, the SO output is tri−stated (high impedance) and the device is in Standby Mode (unless an internal write operation is in progress). *Every communication session between host and NV25080/160 must be preceded by a high to low transition and concluded with a low to high transition of the $\overline{CS}$ input.*

$\overline{WP}$: The write protect input pin will allow all write operations to the device when held high. When $\overline{WP}$ pin is tied low and the WPEN bit in the Status Register (refer to Status Register description, later in this Data Sheet) is set to "1", writing to the Status Register is disabled.

$\overline{HOLD}$: The $\overline{HOLD}$ input pin is used to pause transmission between host and NV25080/160, without having to retransmit the entire sequence at a later time. To pause, $\overline{HOLD}$ must be taken low and to resume it must be taken back high, with the SCK input low during both transitions. When not used for pausing, the $\overline{HOLD}$ input should be tied to V_{CC}, either directly or through a resistor.

Functional Description

The NV25080/160 devices support the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8−bit instruction register. The instruction set and associated op−codes are listed in Table 7.

Reading data stored in the NV25080/160 is accomplished by simply providing the READ command and an address. Writing to the NV25080/160, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the $\overline{CS}$ input pin, the NV25080/160 will accept any one of the six instruction op−codes listed in Table 7 and will ignore all other possible 8−bit combinations. The communication protocol follows the timing from Figure 2.

Table 7. INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

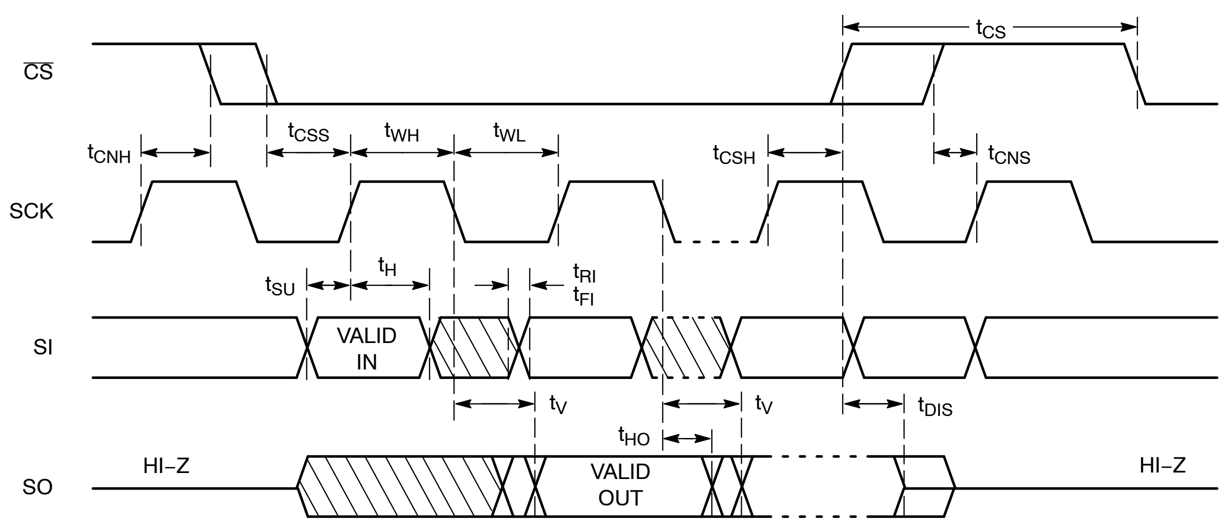


Figure 2. Synchronous Data Timing

Status Register

The Status Register, as shown in Table 8, contains a number of status and control bits.

The $\overline{RDY}$ (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The WEL (Write Enable Latch) bit is set/reset by the WREN/WRDI commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.

The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non−volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 9. The protected blocks then become read−only.

Table 8. STATUS REGISTER

7	6	5	4	3	2	1	0
WPEN	0	0	0	BP1	BP0	WEL	$\overline{\text{RDY}}$

Table 9. BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	**BP0**		
0	0	None	No Protection
0	1	25080: 0300−03FF 25160: 0600−07FF	Quarter Array Protection
1	0	25080: 0200−03FF 25160: 0400−07FF	Half Array Protection
1	1	25080: 0000−03FF 25160: 0000−07FF	Full Array Protection

Table 10. WRITE PROTECT CONDITIONS

WPEN	$\overline{\text{WP}}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

WRITE OPERATIONS

The NV25080/160 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable

The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the NV25080/160. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 3. The WREN instruction must be sent prior to any WRITE or WRSR instruction.

The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 4. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

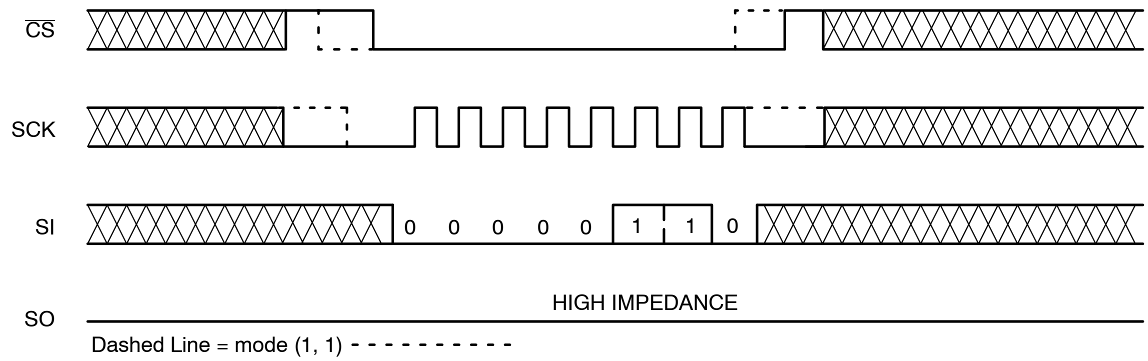


Figure 3. WREN Timing

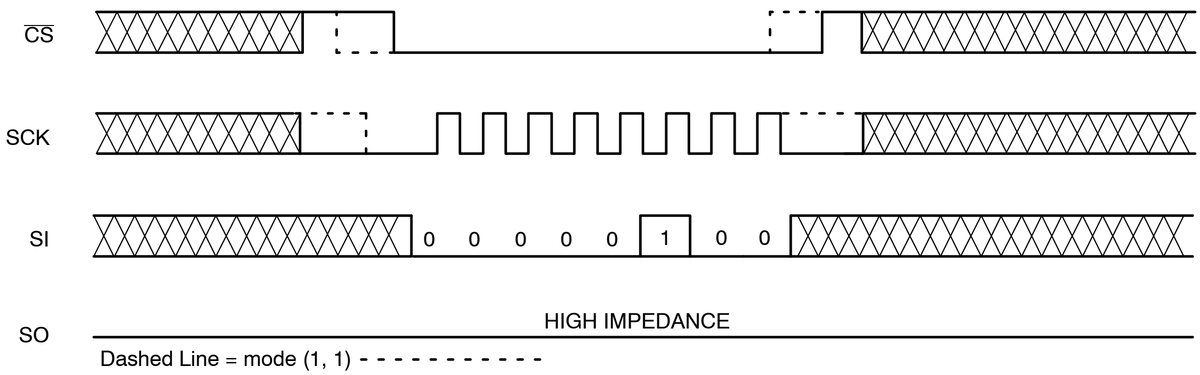


Figure 4. WRDI Timing

Byte Write

Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16−bit address and data as shown in Figure 5. Only 10 significant address bits are used by the NV25080 and 11 by the NV25160. The rest are don't care bits, as shown in Table 11. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{RDY}$ bit will indicate if the internal write cycle is in progress ($\overline{RDY}$ high), or the device is ready to accept commands ($\overline{RDY}$ low).

Page Write

After sending the first data byte to the NV25080/160, the host may continue sending data, up to a total of 32 bytes, according to timing shown in Figure 6. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will "roll over" to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the NV25080/160 is automatically returned to the write disable state.

Table 11. BYTE ADDRESS

Device	Address Significant Bits	Address Don't Care Bits	# Address Clock Pulse
NV25080	A9 – A0	A15 – A10	16
NV25160	A10 – A0	A15 – A11	16

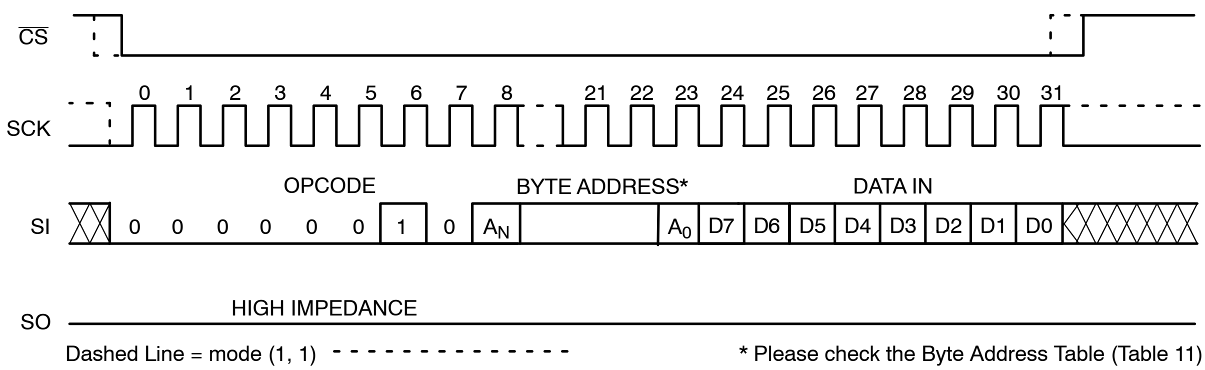


Figure 5. Byte WRITE Timing

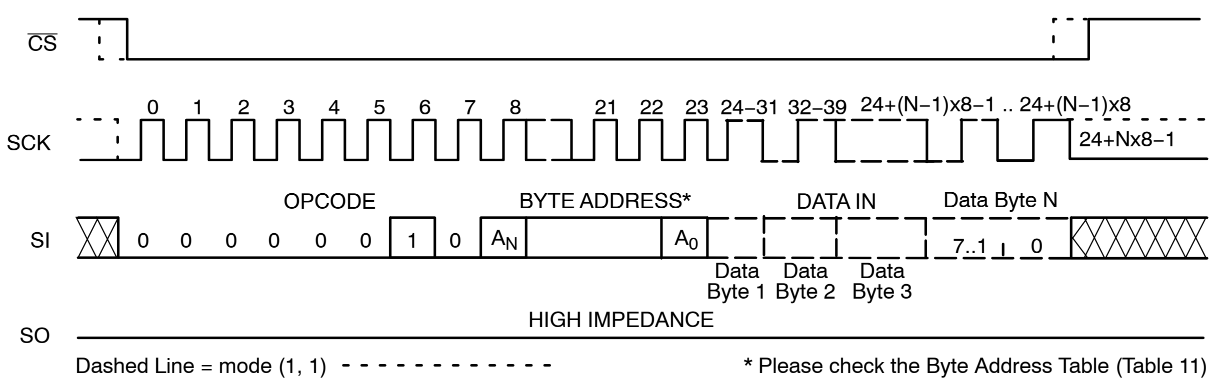


Figure 6. Page WRITE Timing

Write Status Register

The Status Register is written by sending a WRSR instruction according to timing shown in Figure 7. Only bits 2, 3 and 7 can be written using the WRSR command.

Write Protection

The Write Protect ($\overline{WP}$) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When $\overline{WP}$ is low and the WPEN bit is set to “1”, write operations to the Status Register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the Status Register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to “0”. The $\overline{WP}$ input timing is shown in Figure 8.

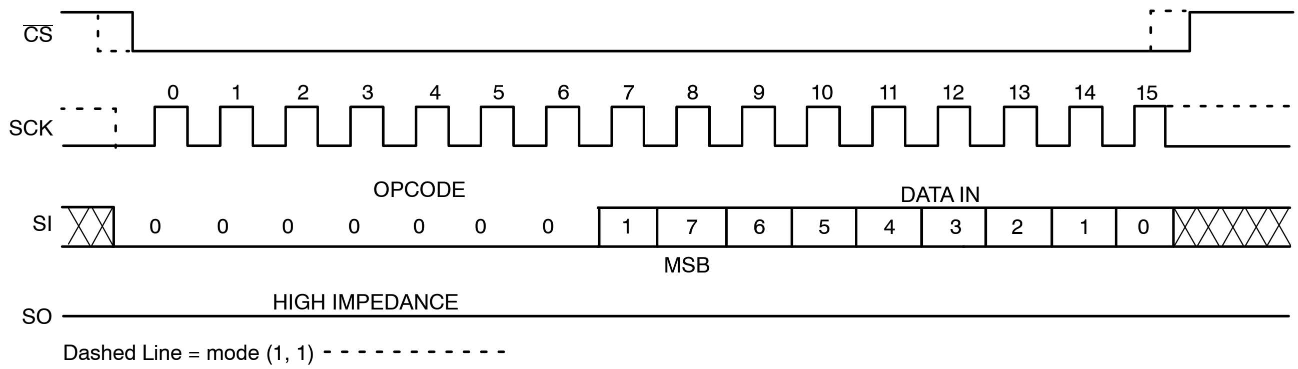


Figure 7. WRSR Timing

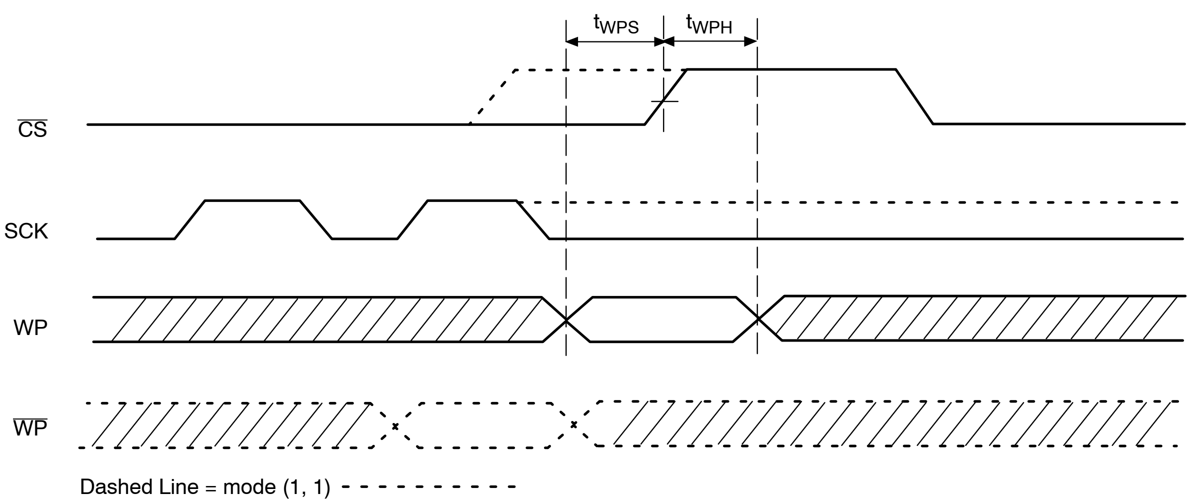


Figure 8. $\overline{WP}$ Timing

READ OPERATIONS

Read from Memory Array

To read from memory, the host sends a READ instruction followed by a 16−bit address (see Table 11 for the number of significant address bits).

After receiving the last address bit, the NV25080/160 will respond by shifting out data on the SO pin (as shown in Figure 9). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Read Status Register

To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the NV25080/160 will shift out the contents of the status register on the SO pin (Figure 10). The status register may be read at any time, including during an internal write cycle. While the internal write cycle is in progress, the RDSR command will output the full content of the status register. For easy detection of the internal write cycle completion, both during writing to the memory array and to the status register, we recommend sampling the RDY bit only through the polling routine. After detecting the RDY bit “0”, the next RDSR instruction will always output the expected content of the status register.

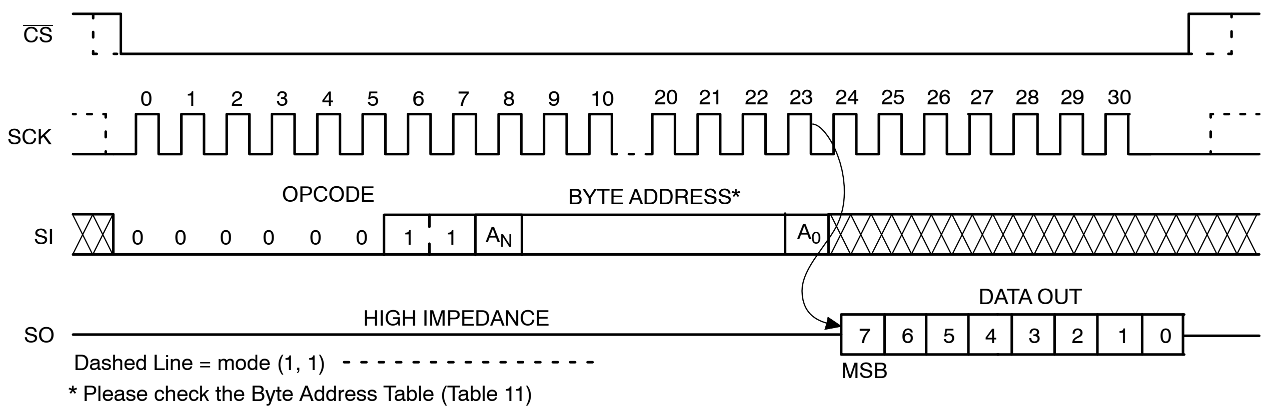


Figure 9. READ Timing

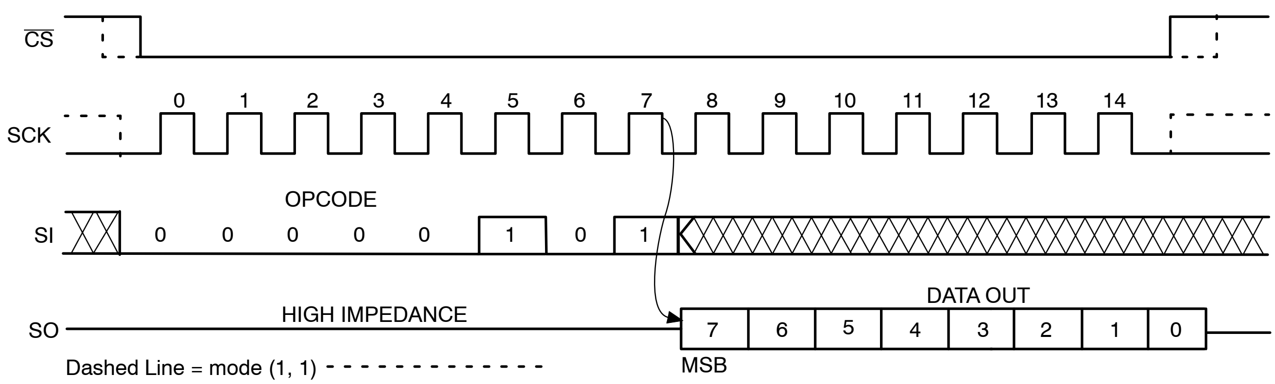


Figure 10. RDSR Timing

Hold Operation

The $\overline{HOLD}$ input can be used to pause communication between host and NV25080/160. To pause, $\overline{HOLD}$ must be taken low while SCK is low (Figure 11). During the hold condition the device must remain selected ($\overline{CS}$ low). During the pause, the data output pin (SO) is tri−stated (high impedance) and SI transitions are ignored. To resume communication, $\overline{HOLD}$ must be taken high while SCK is low.

Design Considerations

The NV25080/160 devices incorporate Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR behavior protects the device against 'brown−out' failure following a temporary loss of power.

The NV25080/160 device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior to any writes to the device.

After power up, the $\overline{CS}$ pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The $\overline{CS}$ input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op−code will be ignored and the serial output pin (SO) will remain in the high impedance state.

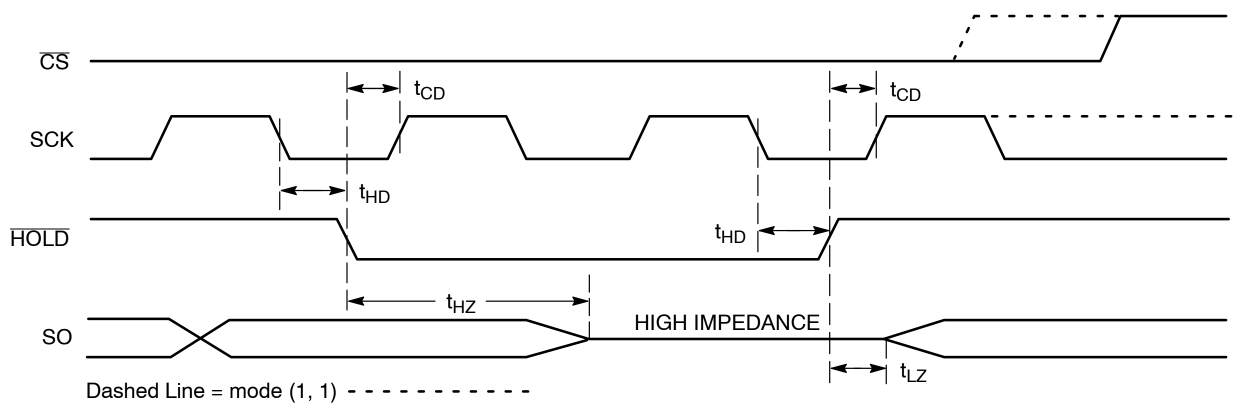


Figure 11. $\overline{HOLD}$ Timing

ORDERING INFORMATION (Notes 8 and 9)

Device Order Number	Specific Device Marking	Temperature Range	Package Type	Shipping†
NV25080MUW2VTAG	D3	−40°C to +125°C	UDFN8 (2x2) (Wettable Flank) (Pb−Free)	3000 / Tape & Reel
NV25080MUW3VTBG	S3W	−40°C to +125°C	UDFN8 (2x3) (Wettable Flank) (Pb−Free)	3000 / Tape & Reel
NV25160MUW3VTBG	S4W	−40°C to +125°C	UDFN8 (2x3) (Wettable Flank) (Pb−Free)	3000 / Tape & Reel

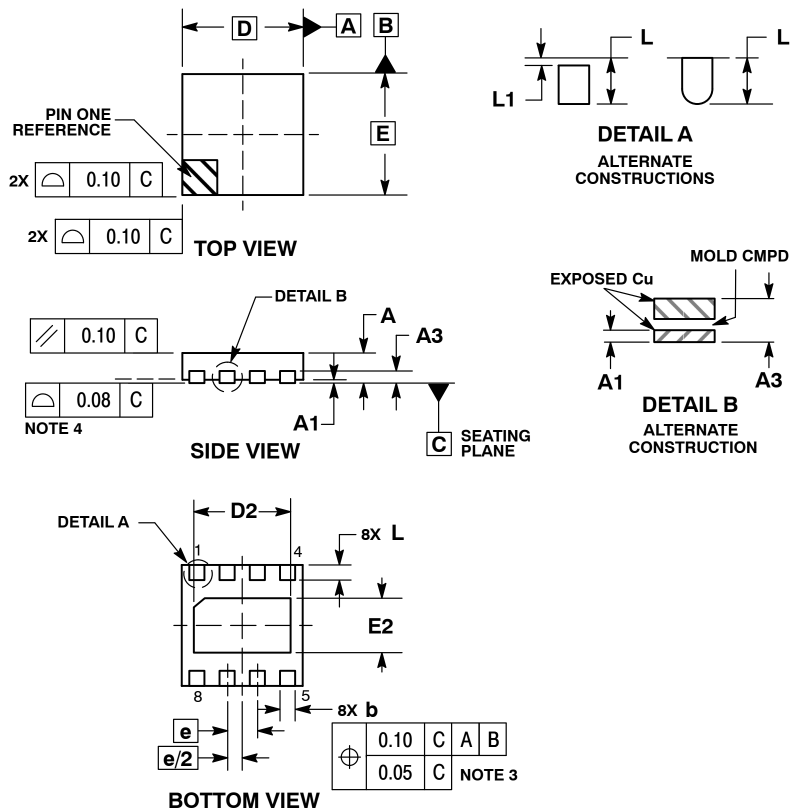
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. All packages are RoHS−compliant (Pb−Free, Halogen−free).
9. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

SCALE 2:1

UDFN8, 2x2
CASE 517AW
ISSUE A

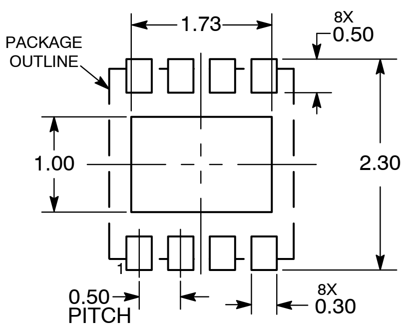
DATE 13 NOV 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.18	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
L	0.20	0.45
L1	---	0.15

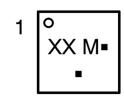
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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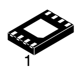
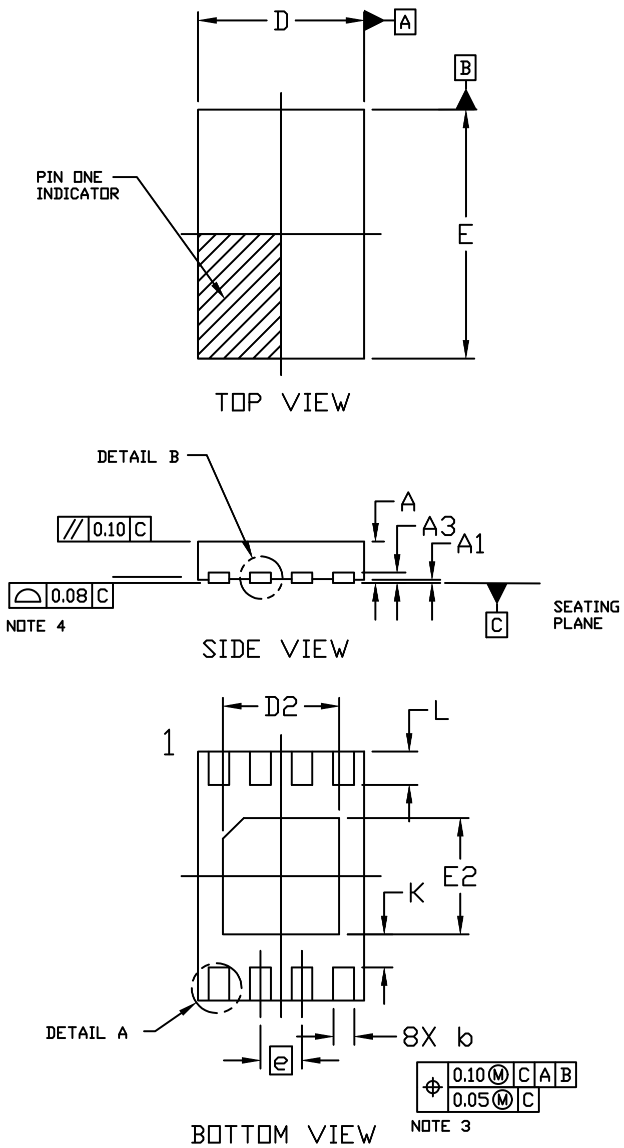
DESCRIPTION:	**UDFN8, 2X2**	**PAGE 1 OF 1**



SCALE 2:1

UDFN8 2x3, 0.5P
CASE 517DH
ISSUE A

DATE 10 DEC 2020



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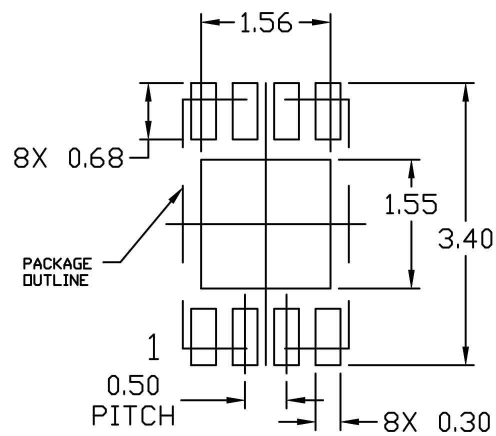
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

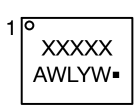
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.30	1.40	1.50
e	0.50 BSC		
K	0.40 REF		
L	0.30	0.40	0.50



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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