DATA SHEET

NV3029G-01

240RGB x 320dot, 262,144-color
TFT Controller Driver with Internal RAM

Version 0.1
Nov.30, 2015

Contents

1. Introduction

NV3029G-01 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

NV3029G-01 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

NV3029G-01 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. NV3029G-01 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the NV3029G-01 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

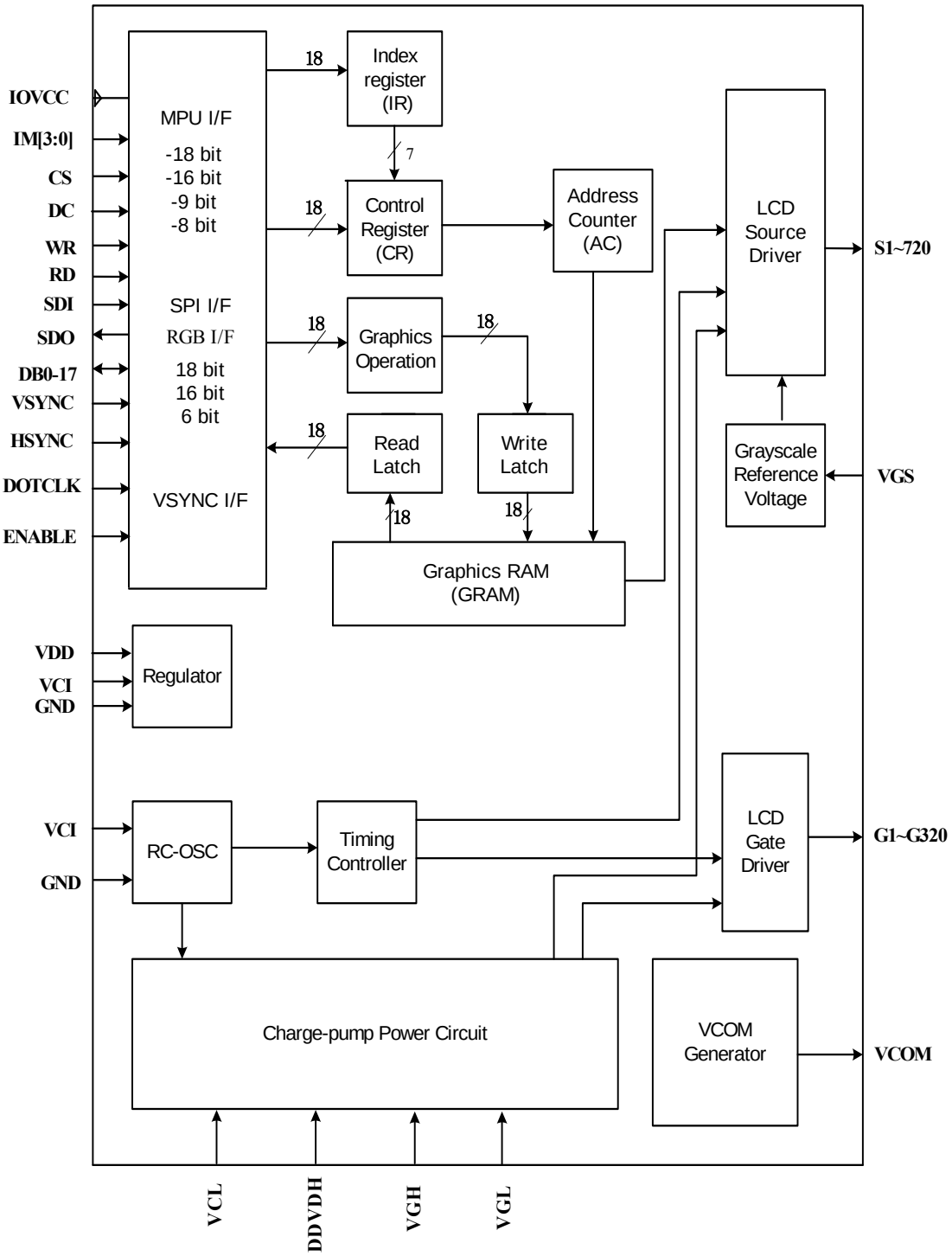
- One-chip controller driver for 240RGB x 320-dot graphics display in 262,144 colors on TFT panel
- One-chip solution for a-Si TFT panel
- System interface
  - High-speed interface via 8-, 9-, 16-, 18-bit parallel ports
  - Clock synchropadus serial interface
- Moving picture display interface
  - RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 6-, 16-, 18-bit ports
- Window address function to specify a rectangular area in the internal RAM to write data
  - Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
- Color display control functions
  - correction function to display in 262k colors
  - 1-line unit vertical scroll function
- Low –power consumption architecture (allowing direct input of interface I/O power supply)
  - 8-color display function
  - Input power supply voltages: IOVcc = 1.65V ~ 3.6 V (interface I/O power supply)

  Vci = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)

  (Vci-VCL ≤ 6.0V)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/Vcom power supply: DDVDH-AGND = 4.5V ~ 6.0V
  - Gate drive power supply: VGH-VGL ≤ 28.0V
  - Vcom drive (Vcom power supply): VcomH = 2.5V ~(DDVDH-0.5)V

    VcomL = (VCL+0.5)V ~ GND
- Internal liquid crystal drive circuit: 720-channel source output and 320-channel gate output
- N-line-inversion liquid crystal drive to invert polarity of liquid crystal in a cycle of arbitrary line period
- Internal oscillator, Hardware and software Reset
- TFT storage capacitor: Cst only
- Only need one external capacitor(VGL storage capacitor)

3. Block Diagram



Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

4. Pin Function

Power supply		
Signal	Connect to	Function
IOVCC	I/O voltage	Low voltage power supply for interface logic circuits (1.65~3.3V), IOVCC <= VCI
VDD3-P	LED driver Power	Power supply for LED driver interface (1.65~3.3V). If LED driver is not used, fix this pin at IOVCC.
VCI	Analog Power	High voltage power supply for analog circuit blocks. Connect to an external power supply of 2.5V ~ 3.3V.
VDD	Regulated Voltage	Digital circuit power pad.
GND	Logic Ground	System ground level for logic blocks.
GNDA	Analog Ground	System ground level for analog circuit blocks. Connect to GND on the FPC to prevent noise.

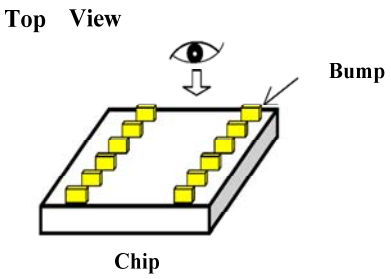
Test pins		
Signal	I/O	Function
DUMMYR1 DUMMYR2	I	Dummy pin. Leave these pads open.
TMODE[3:0]	-	Dummy pin. Leave these pads open.
TMUX[2:0]	-	Dummy pin. Leave these pads open.
EXCLK	-	Dummy pin. Leave these pads open.
DB[23:18]	-	Dummy pin. Leave these pads open.
VCIR_EXIN	-	Dummy pin. Leave these pads open.
DUMMY	-	Dummy pin. Leave these pads open.
EXTC	-	Dummy pin. Leave these pads open.

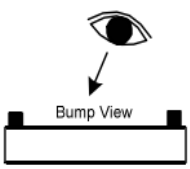
<table>
<tr><th colspan="3">Interface logic pins</th></tr>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>Select the MPU system interface mode.
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MPU interface Mode</th><th colspan="2">DB pins</th></tr>
<tr><th>Register</th><th>Gram</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>i80-system
8 bit interface I</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>i80-system
16-bit interface I</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system
9-bit interface I</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system
18-bit interface I</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data Serial interface I
2 data lane serial interface</td><td colspan="2">SDA: in/out</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data Serial interface I</td><td colspan="2">SDA: in/out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>i80-system
16-bit interface II</td><td>DB[8:1]</td><td>DB[8:1],
DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>i80-system
8 bit interface II</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system
18-bit interface II</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system
9-bit interface II</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data Serial interface II</td><td colspan="2">SDI: in
SDO: out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data Serial interface II</td><td colspan="2">SDI: in
SDO: out</td></tr>
</table>
If pad not used, please fix this pin to IOVCC or VSS level.</td></tr>
<tr><td>RESET</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>CS</td><td>I</td><td>A chip select signal.
Low: the NV3029G-01 is selected and accessible.
High: the NV3029G-01 is not selected and not accessible.</td></tr>
<tr><td>DC</td><td>I</td><td>This pin is used to select “Data or Command” in the parallel interface.
When DC = ’1’, data is selected.
When DC = ’0’, command is selected.
This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
If not used, this pin should be connected to IOVCC or VSS.</td></tr>
</table>

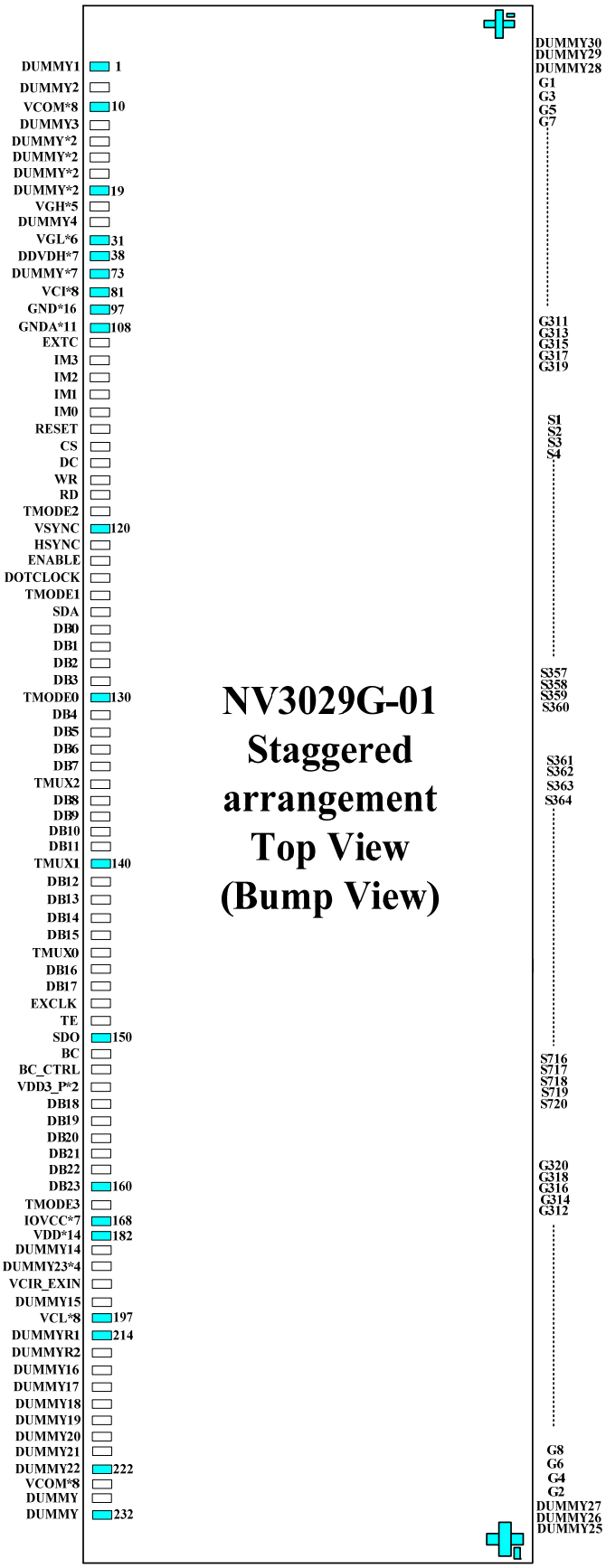
WR	I	A write strobe signal and enables an operation to write data when the signal is low. Fix to either IOVCC or GND level when not in use. SPI 4-line system (DC): Serves as command or parameter select. 2 data lane serial interface: rgb data
RD	I	A read strobe signal and enables an operation to read out data when the signal is low. Fix to either IOVCC or GND level when not in use.
SDI/SDA	I/O	SPI interface bi-directional pin.The data is latched on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.
SDO	O	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. If not used, open this pin.
TE	O	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, fix this pin at IOVCC or GND.
VSYNC	I	Vertical sync. Signal in RGB I/F mode. If not used, fix this pin at IOVCC or GND.
HSYNC	I	Horizontal sync. Signal in RGB I/F mode. If not used, fix this pin at IOVCC or GND.
ENABLE	I	Data enable signal in RGB I/F mode. If not used, fix this pin at IOVCC or GND.
DB0- DB17	I/O	18-bit parallel bi-directional data bus for MPU system interface and RGB interface mode. If not used, fix this pin at IOVCC or GND.

Driver input/output pins		
Signal	I/O	Function
S1 to S720	O	Source driver output pads.
G1 to G320	O	Gate driver output pads.
DDVDH	O	Generated power output PAD for source driver block.
VGH	O	Power supply for the gate driver.
VGL	O	Power supply for the gate driver. Connect this PAD to the capacitor for stabilization.
VCL	O	Power supply for generating VCOM low level.
VCOM	O	Power supply PAD for the TFT-display counter electrode. Charge recycling method is used with VCI and GND voltage. Connect this PAD to the TFT-display counter electrode.

5. Pad Arrangement







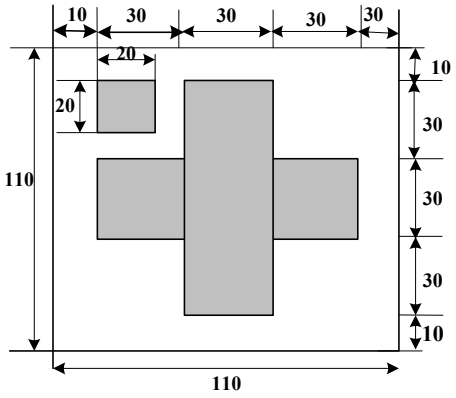
6. Chip Size

Item	PAD Pad.	Size		Unit
		X	Y	
Chip size	-	16320	626	um
PAD Pitch	Input Side	85/72.5/60		
	Output Side	14		
Bumped PAD Top Size	Input Side	40	50.5	
	Output Side	14	100	
Bumped PAD Height	Height In Wafer	9		
	Tolerance In Chip	Under 2		
	Dimple Height	Under 2		
Chip Thickness	-	280		

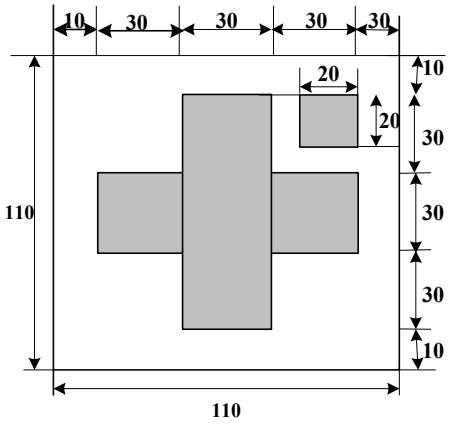
Note:
1. Scribe lane 60um included in this die size.
2. Wafer thickness can be varied with the customer's needs.

Alignment mark

Left COG Align key



Right COG Align key



unit:um

7. Pad Coordinates

NO.	Pad	X	Y
1	DUMMY1	-7292.5	-245.523
2	DUMMY2	-7232.5	-245.523
3	VCOM	-7172.5	-245.523
4	VCOM	-7112.5	-245.523
5	VCOM	-7052.5	-245.523
6	VCOM	-6992.5	-245.523
7	VCOM	-6932.5	-245.523
8	VCOM	-6872.5	-245.523
9	VCOM	-6812.5	-245.523
10	VCOM	-6752.5	-245.523
11	DUMMY3	-6692.5	-245.523
12	DUMMY	-6632.5	-245.523
13	DUMMY	-6572.5	-245.523
14	DUMMY	-6512.5	-245.523
15	DUMMY	-6452.5	-245.523
16	DUMMY	-6392.5	-245.523
17	DUMMY	-6332.5	-245.523
18	DUMMY	-6272.5	-245.523
19	DUMMY	-6212.5	-245.523
20	VGH	-6152.5	-245.523
21	VGH	-6092.5	-245.523
22	VGH	-6032.5	-245.523
23	VGH	-5972.5	-245.523
24	VGH	-5912.5	-245.523
25	DUMMY4	-5852.5	-245.523
26	VGL	-5792.5	-245.523
27	VGL	-5732.5	-245.523
28	VGL	-5672.5	-245.523
29	VGL	-5612.5	-245.523
30	VGL	-5552.5	-245.523
31	VGL	-5492.5	-245.523
32	DDVDH	-5432.5	-245.523
33	DDVDH	-5372.5	-245.523
34	DDVDH	-5312.5	-245.523
35	DDVDH	-5252.5	-245.523
36	DDVDH	-5192.5	-245.523
37	DDVDH	-5132.5	-245.523
38	DDVDH	-5072.5	-245.523
39	No pad		
40	No pad		
41	No pad		
42	No pad		
43	No pad		
44	No pad		
45	No pad		
46	No pad		
47	No pad		
48	No pad		
49	No pad		
50	No pad		

NO.	Pad	X	Y
51	No pad		
52	No pad		
53	No pad		
54	No pad		
55	No pad		
56	No pad		
57	No pad		
58	No pad		
59	No pad		
60	No pad		
61	No pad		
62	No pad		
63	No pad		
64	No pad		
65	No pad		
66	No pad		
67	DUMMY	-3332.5	-245.523
68	DUMMY	-3272.5	-245.523
69	DUMMY	-3212.5	-245.523
70	DUMMY	-3152.5	-245.523
71	DUMMY	-3092.5	-245.523
72	DUMMY	-3032.5	-245.523
73	DUMMY	-2972.5	-245.523
74	VCI	-2912.5	-245.523
75	VCI	-2852.5	-245.523
76	VCI	-2792.5	-245.523
77	VCI	-2732.5	-245.523
78	VCI	-2672.5	-245.523
79	VCI	-2612.5	-245.523
80	VCI	-2552.5	-245.523
81	VCI	-2492.5	-245.523
82	GND	-2432.5	-245.523
83	GND	-2372.5	-245.523
84	GND	-2312.5	-245.523
85	GND	-2252.5	-245.523
86	GND	-2192.5	-245.523
87	GND	-2132.5	-245.523
88	GND	-2072.5	-245.523
89	GND	-2012.5	-245.523
90	GND	-1952.5	-245.523
91	GND	-1892.5	-245.523
92	GND	-1832.5	-245.523
93	GND	-1772.5	-245.523
94	GND	-1712.5	-245.523
95	GND	-1652.5	-245.523
96	GND	-1592.5	-245.523
97	GND	-1532.5	-245.523
98	GNDA	-1472.5	-245.523
99	GNDA	-1412.5	-245.523
100	GNDA	-1352.5	-245.523

NO.	Pad	X	Y
101	GNDA	-1292.5	-245.523
102	GNDA	-1232.5	-245.523
103	GNDA	-1172.5	-245.523
104	GNDA	-1112.5	-245.523
105	GNDA	-1052.5	-245.523
106	GNDA	-992.5	-245.523
107	GNDA	-932.5	-245.523
108	GNDA	-872.5	-245.523
109	EXTC	-812.5	-245.523
110	IM3	-752.5	-245.523
111	IM2	-692.5	-245.523
112	IM1	-632.5	-245.523
113	IM0	-572.5	-245.523
114	RESET	-512.5	-245.523
115	CS	-452.5	-245.523
116	DC	-392.5	-245.523
117	WR	-332.5	-245.523
118	RD	-272.5	-245.523
119	TMODE2	-212.5	-245.523
120	VSYNC	-152.5	-245.523
121	HSYNC	-92.5	-245.523
122	ENABLE	-32.5	-245.523
123	DOTCLOCK	27.5	-245.523
124	TMODE1	87.5	-245.523
125	SDA	160	-245.523
126	DB0	245	-245.523
127	DB1	330	-245.523
128	DB2	415	-245.523
129	DB3	500	-245.523
130	TMODE0	572.5	-245.523
131	DB4	645	-245.523
132	DB5	730	-245.523
133	DB6	815	-245.523
134	DB7	900	-245.523
135	TMUX2	972.5	-245.523
136	DB8	1045	-245.523
137	DB9	1130	-245.523
138	DB10	1215	-245.523
139	DB11	1300	-245.523
140	TMUX1	1372.5	-245.523
141	DB12	1445	-245.523
142	DB13	1530	-245.523
143	DB14	1615	-245.523
144	DB15	1700	-245.523
145	TMUX0	1772.5	-245.523
146	DB16	1845	-245.523
147	DB17	1930	-245.523
148	EXCLK	2002.5	-245.523
149	TE	2075	-245.523
150	SDO	2160	-245.523

NO.	Pad	X	Y
151	BC	2245	-245.523
152	BC_CTRL	2330	-245.523
153	VDD3_P	2402.5	-245.523
154	VDD3_P	2462.5	-245.523
155	DB18	2535	-245.523
156	DB19	2620	-245.523
157	DB20	2705	-245.523
158	DB21	2790	-245.523
159	DB22	2875	-245.523
160	DB23	2960	-245.523
161	TMODE3	3032.5	-245.523
162	IOVCC	3092.5	-245.523
163	IOVCC	3152.5	-245.523
164	IOVCC	3212.5	-245.523
165	IOVCC	3272.5	-245.523
166	IOVCC	3332.5	-245.523
167	IOVCC	3392.5	-245.523
168	IOVCC	3452.5	-245.523
169	VDD	3512.5	-245.523
170	VDD	3572.5	-245.523
171	VDD	3632.5	-245.523
172	VDD	3692.5	-245.523
173	VDD	3752.5	-245.523
174	VDD	3812.5	-245.523
175	VDD	3872.5	-245.523
176	VDD	3932.5	-245.523
177	VDD	3992.5	-245.523
178	VDD	4052.5	-245.523
179	VDD	4112.5	-245.523
180	VDD	4172.5	-245.523
181	VDD	4232.5	-245.523
182	VDD	4292.5	-245.523
183	DUMMY14	4352.5	-245.523
184	DUMMY23	4412.5	-245.523
185	DUMMY23	4472.5	-245.523
186	DUMMY23	4532.5	-245.523
187	DUMMY23	4592.5	-245.523
188	VCIR_EXIN	4652.5	-245.523
189	DUMMY15	4712.5	-245.523
190	VCL	4772.5	-245.523
191	VCL	4832.5	-245.523
192	VCL	4892.5	-245.523
193	VCL	4952.5	-245.523
194	VCL	5012.5	-245.523
195	VCL	5072.5	-245.523
196	VCL	5132.5	-245.523
197	VCL	5192.5	-245.523
198	No pad		
199	No pad		
200	No pad		

NO.	Pad	X	Y
201	No pad		
202	No pad		
203	No pad		
204	No pad		
205	No pad		
206	No pad		
207	No pad		
208	No pad		
209	No pad		
210	No pad		
211	No pad		
212	No pad		
213	No pad		
214	DUMMYR1	6212.5	-245.523
215	DUMMYR2	6272.5	-245.523
216	DUMMY16	6332.5	-245.523
217	DUMMY17	6392.5	-245.523
218	DUMMY18	6452.5	-245.523
219	DUMMY19	6512.5	-245.523
220	DUMMY20	6572.5	-245.523
221	DUMMY21	6632.5	-245.523
222	DUMMY22	6692.5	-245.523
223	VCOM	6752.5	-245.523
224	VCOM	6812.5	-245.523
225	VCOM	6872.5	-245.523
226	VCOM	6932.5	-245.523
227	VCOM	6992.5	-245.523
228	VCOM	7052.5	-245.523
229	VCOM	7112.5	-245.523
230	VCOM	7172.5	-245.523
231	DUMMY	7232.5	-245.523
232	DUMMY	7292.5	-245.523
233	DUMMY25	7399	224
234	DUMMY26	7385	93
235	DUMMY27	7371	224
236	G2	7357	93
237	G4	7343	224
238	G6	7329	93
239	G8	7315	224
240	G10	7301	93
241	G12	7287	224
242	G14	7273	93
243	G16	7259	224
244	G18	7245	93
245	G20	7231	224
246	G22	7217	93
247	G24	7203	224
248	G26	7189	93
249	G28	7175	224
250	G30	7161	93

NO.	Pad	X	Y
251	G32	7147	224
252	G34	7133	93
253	G36	7119	224
254	G38	7105	93
255	G40	7091	224
256	G42	7077	93
257	G44	7063	224
258	G46	7049	93
259	G48	7035	224
260	G50	7021	93
261	G52	7007	224
262	G54	6993	93
263	G56	6979	224
264	G58	6965	93
265	G60	6951	224
266	G62	6937	93
267	G64	6923	224
268	G66	6909	93
269	G68	6895	224
270	G70	6881	93
271	G72	6867	224
272	G74	6853	93
273	G76	6839	224
274	G78	6825	93
275	G80	6811	224
276	G82	6797	93
277	G84	6783	224
278	G86	6769	93
279	G88	6755	224
280	G90	6741	93
281	G92	6727	224
282	G94	6713	93
283	G96	6699	224
284	G98	6685	93
285	G100	6671	224
286	G102	6657	93
287	G104	6643	224
288	G106	6629	93
289	G108	6615	224
290	G110	6601	93
291	G112	6587	224
292	G114	6573	93
293	G116	6559	224
294	G118	6545	93
295	G120	6531	224
296	G122	6517	93
297	G124	6503	224
298	G126	6489	93
299	G128	6475	224
300	G130	6461	93

NO.	Pad	X	Y
301	G132	6447	224
302	G134	6433	93
303	G136	6419	224
304	G138	6405	93
305	G140	6391	224
306	G142	6377	93
307	G144	6363	224
308	G146	6349	93
309	G148	6335	224
310	G150	6321	93
311	G152	6307	224
312	G154	6293	93
313	G156	6279	224
314	G158	6265	93
315	G160	6251	224
316	G162	6237	93
317	G164	6223	224
318	G166	6209	93
319	G168	6195	224
320	G170	6181	93
321	G172	6167	224
322	G174	6153	93
323	G176	6139	224
324	G178	6125	93
325	G180	6111	224
326	G182	6097	93
327	G184	6083	224
328	G186	6069	93
329	G188	6055	224
330	G190	6041	93
331	G192	6027	224
332	G194	6013	93
333	G196	5999	224
334	G198	5985	93
335	G200	5971	224
336	G202	5957	93
337	G204	5943	224
338	G206	5929	93
339	G208	5915	224
340	G210	5901	93
341	G212	5887	224
342	G214	5873	93
343	G216	5859	224
344	G218	5845	93
345	G220	5831	224
346	G222	5817	93
347	G224	5803	224
348	G226	5789	93
349	G228	5775	224
350	G230	5761	93

NO.	Pad	X	Y
351	G232	5747	224
352	G234	5733	93
353	G236	5719	224
354	G238	5705	93
355	G240	5691	224
356	G242	5677	93
357	G244	5663	224
358	G246	5649	93
359	G248	5635	224
360	G250	5621	93
361	G252	5607	224
362	G254	5593	93
363	G256	5579	224
364	G258	5565	93
365	G260	5551	224
366	G262	5537	93
367	G264	5523	224
368	G266	5509	93
369	G268	5495	224
370	G270	5481	93
371	G272	5467	224
372	G274	5453	93
373	G276	5439	224
374	G278	5425	93
375	G280	5411	224
376	G282	5397	93
377	G284	5383	224
378	G286	5369	93
379	G288	5355	224
380	G290	5341	93
381	G292	5327	224
382	G294	5313	93
383	G296	5299	224
384	G298	5285	93
385	G300	5271	224
386	G302	5257	93
387	G304	5243	224
388	G306	5229	93
389	G308	5215	224
390	G310	5201	93
391	G312	5187	224
392	G314	5173	93
393	G316	5159	224
394	G318	5145	93
395	G320	5131	224
396	S720	5075	93
397	S719	5061	224
398	S718	5047	93
399	S717	5033	224
400	S716	5019	93

NO.	Pad	X	Y
401	S715	5005	224
402	S714	4991	93
403	S713	4977	224
404	S712	4963	93
405	S711	4949	224
406	S710	4935	93
407	S709	4921	224
408	S708	4907	93
409	S707	4893	224
410	S706	4879	93
411	S705	4865	224
412	S704	4851	93
413	S703	4837	224
414	S702	4823	93
415	S701	4809	224
416	S700	4795	93
417	S699	4781	224
418	S698	4767	93
419	S697	4753	224
420	S696	4739	93
421	S695	4725	224
422	S694	4711	93
423	S693	4697	224
424	S692	4683	93
425	S691	4669	224
426	S690	4655	93
427	S689	4641	224
428	S688	4627	93
429	S687	4613	224
430	S686	4599	93
431	S685	4585	224
432	S684	4571	93
433	S683	4557	224
434	S682	4543	93
435	S681	4529	224
436	S680	4515	93
437	S679	4501	224
438	S678	4487	93
439	S677	4473	224
440	S676	4459	93
441	S675	4445	224
442	S674	4431	93
443	S673	4417	224
444	S672	4403	93
445	S671	4389	224
446	S670	4375	93
447	S669	4361	224
448	S668	4347	93
449	S667	4333	224
450	S666	4319	93

NO.	Pad	X	Y
451	S665	4305	224
452	S664	4291	93
453	S663	4277	224
454	S662	4263	93
455	S661	4249	224
456	S660	4235	93
457	S659	4221	224
458	S658	4207	93
459	S657	4193	224
460	S656	4179	93
461	S655	4165	224
462	S654	4151	93
463	S653	4137	224
464	S652	4123	93
465	S651	4109	224
466	S650	4095	93
467	S649	4081	224
468	S648	4067	93
469	S647	4053	224
470	S646	4039	93
471	S645	4025	224
472	S644	4011	93
473	S643	3997	224
474	S642	3983	93
475	S641	3969	224
476	S640	3955	93
477	S639	3941	224
478	S638	3927	93
479	S637	3913	224
480	S636	3899	93
481	S635	3885	224
482	S634	3871	93
483	S633	3857	224
484	S632	3843	93
485	S631	3829	224
486	S630	3815	93
487	S629	3801	224
488	S628	3787	93
489	S627	3773	224
490	S626	3759	93
491	S625	3745	224
492	S624	3731	93
493	S623	3717	224
494	S622	3703	93
495	S621	3689	224
496	S620	3675	93
497	S619	3661	224
498	S618	3647	93
499	S617	3633	224
500	S616	3619	93

NO.	Pad	X	Y
501	S615	3605	224
502	S614	3591	93
503	S613	3577	224
504	S612	3563	93
505	S611	3549	224
506	S610	3535	93
507	S609	3521	224
508	S608	3507	93
509	S607	3493	224
510	S606	3479	93
511	S605	3465	224
512	S604	3451	93
513	S603	3437	224
514	S602	3423	93
515	S601	3409	224
516	S600	3395	93
517	S599	3381	224
518	S598	3367	93
519	S597	3353	224
520	S596	3339	93
521	S595	3325	224
522	S594	3311	93
523	S593	3297	224
524	S592	3283	93
525	S591	3269	224
526	S590	3255	93
527	S589	3241	224
528	S588	3227	93
529	S587	3213	224
530	S586	3199	93
531	S585	3185	224
532	S584	3171	93
533	S583	3157	224
534	S582	3143	93
535	S581	3129	224
536	S580	3115	93
537	S579	3101	224
538	S578	3087	93
539	S577	3073	224
540	S576	3059	93
541	S575	3045	224
542	S574	3031	93
543	S573	3017	224
544	S572	3003	93
545	S571	2989	224
546	S570	2975	93
547	S569	2961	224
548	S568	2947	93
549	S567	2933	224
550	S566	2919	93

NO.	Pad	X	Y
551	S565	2905	224
552	S564	2891	93
553	S563	2877	224
554	S562	2863	93
555	S561	2849	224
556	S560	2835	93
557	S559	2821	224
558	S558	2807	93
559	S557	2793	224
560	S556	2779	93
561	S555	2765	224
562	S554	2751	93
563	S553	2737	224
564	S552	2723	93
565	S551	2709	224
566	S550	2695	93
567	S549	2681	224
568	S548	2667	93
569	S547	2653	224
570	S546	2639	93
571	S545	2625	224
572	S544	2611	93
573	S543	2597	224
574	S542	2583	93
575	S541	2569	224
576	S540	2555	93
577	S539	2541	224
578	S538	2527	93
579	S537	2513	224
580	S536	2499	93
581	S535	2485	224
582	S534	2471	93
583	S533	2457	224
584	S532	2443	93
585	S531	2429	224
586	S530	2415	93
587	S529	2401	224
588	S528	2387	93
589	S527	2373	224
590	S526	2359	93
591	S525	2345	224
592	S524	2331	93
593	S523	2317	224
594	S522	2303	93
595	S521	2289	224
596	S520	2275	93
597	S519	2261	224
598	S518	2247	93
599	S517	2233	224
600	S516	2219	93

NO.	Pad	X	Y
601	S515	2205	224
602	S514	2191	93
603	S513	2177	224
604	S512	2163	93
605	S511	2149	224
606	S510	2135	93
607	S509	2121	224
608	S508	2107	93
609	S507	2093	224
610	S506	2079	93
611	S505	2065	224
612	S504	2051	93
613	S503	2037	224
614	S502	2023	93
615	S501	2009	224
616	S500	1995	93
617	S499	1981	224
618	S498	1967	93
619	S497	1953	224
620	S496	1939	93
621	S495	1925	224
622	S494	1911	93
623	S493	1897	224
624	S492	1883	93
625	S491	1869	224
626	S490	1855	93
627	S489	1841	224
628	S488	1827	93
629	S487	1813	224
630	S486	1799	93
631	S485	1785	224
632	S484	1771	93
633	S483	1757	224
634	S482	1743	93
635	S481	1729	224
636	S480	1715	93
637	S479	1701	224
638	S478	1687	93
639	S477	1673	224
640	S476	1659	93
641	S475	1645	224
642	S474	1631	93
643	S473	1617	224
644	S472	1603	93
645	S471	1589	224
646	S470	1575	93
647	S469	1561	224
648	S468	1547	93
649	S467	1533	224
650	S466	1519	93

NO.	Pad	X	Y
651	S465	1505	224
652	S464	1491	93
653	S463	1477	224
654	S462	1463	93
655	S461	1449	224
656	S460	1435	93
657	S459	1421	224
658	S458	1407	93
659	S457	1393	224
660	S456	1379	93
661	S455	1365	224
662	S454	1351	93
663	S453	1337	224
664	S452	1323	93
665	S451	1309	224
666	S450	1295	93
667	S449	1281	224
668	S448	1267	93
669	S447	1253	224
670	S446	1239	93
671	S445	1225	224
672	S444	1211	93
673	S443	1197	224
674	S442	1183	93
675	S441	1169	224
676	S440	1155	93
677	S439	1141	224
678	S438	1127	93
679	S437	1113	224
680	S436	1099	93
681	S435	1085	224
682	S434	1071	93
683	S433	1057	224
684	S432	1043	93
685	S431	1029	224
686	S430	1015	93
687	S429	1001	224
688	S428	987	93
689	S427	973	224
690	S426	959	93
691	S425	945	224
692	S424	931	93
693	S423	917	224
694	S422	903	93
695	S421	889	224
696	S420	875	93
697	S419	861	224
698	S418	847	93
699	S417	833	224
700	S416	819	93

NO.	Pad	X	Y
701	S415	805	224
702	S414	791	93
703	S413	777	224
704	S412	763	93
705	S411	749	224
706	S410	735	93
707	S409	721	224
708	S408	707	93
709	S407	693	224
710	S406	679	93
711	S405	665	224
712	S404	651	93
713	S403	637	224
714	S402	623	93
715	S401	609	224
716	S400	595	93
717	S399	581	224
718	S398	567	93
719	S397	553	224
720	S396	539	93
721	S395	525	224
722	S394	511	93
723	S393	497	224
724	S392	483	93
725	S391	469	224
726	S390	455	93
727	S389	441	224
728	S388	427	93
729	S387	413	224
730	S386	399	93
731	S385	385	224
732	S384	371	93
733	S383	357	224
734	S382	343	93
735	S381	329	224
736	S380	315	93
737	S379	301	224
738	S378	287	93
739	S377	273	224
740	S376	259	93
741	S375	245	224
742	S374	231	93
743	S373	217	224
744	S372	203	93
745	S371	189	224
746	S370	175	93
747	S369	161	224
748	S368	147	93
749	S367	133	224
750	S366	119	93

NO.	Pad	X	Y
751	S365	105	224
752	S364	91	93
753	S363	77	224
754	S362	63	93
755	S361	49	224
756	S360	-49	93
757	S359	-63	224
758	S358	-77	93
759	S357	-91	224
760	S356	-105	93
761	S355	-119	224
762	S354	-133	93
763	S353	-147	224
764	S352	-161	93
765	S351	-175	224
766	S350	-189	93
767	S349	-203	224
768	S348	-217	93
769	S347	-231	224
770	S346	-245	93
771	S345	-259	224
772	S344	-273	93
773	S343	-287	224
774	S342	-301	93
775	S341	-315	224
776	S340	-329	93
777	S339	-343	224
778	S338	-357	93
779	S337	-371	224
780	S336	-385	93
781	S335	-399	224
782	S334	-413	93
783	S333	-427	224
784	S332	-441	93
785	S331	-455	224
786	S330	-469	93
787	S329	-483	224
788	S328	-497	93
789	S327	-511	224
790	S326	-525	93
791	S325	-539	224
792	S324	-553	93
793	S323	-567	224
794	S322	-581	93
795	S321	-595	224
796	S320	-609	93
797	S319	-623	224
798	S318	-637	93
799	S317	-651	224
800	S316	-665	93

NO.	Pad	X	Y
801	S315	-679	224
802	S314	-693	93
803	S313	-707	224
804	S312	-721	93
805	S311	-735	224
806	S310	-749	93
807	S309	-763	224
808	S308	-777	93
809	S307	-791	224
810	S306	-805	93
811	S305	-819	224
812	S304	-833	93
813	S303	-847	224
814	S302	-861	93
815	S301	-875	224
816	S300	-889	93
817	S299	-903	224
818	S298	-917	93
819	S297	-931	224
820	S296	-945	93
821	S295	-959	224
822	S294	-973	93
823	S293	-987	224
824	S292	-1001	93
825	S291	-1015	224
826	S290	-1029	93
827	S289	-1043	224
828	S288	-1057	93
829	S287	-1071	224
830	S286	-1085	93
831	S285	-1099	224
832	S284	-1113	93
833	S283	-1127	224
834	S282	-1141	93
835	S281	-1155	224
836	S280	-1169	93
837	S279	-1183	224
838	S278	-1197	93
839	S277	-1211	224
840	S276	-1225	93
841	S275	-1239	224
842	S274	-1253	93
843	S273	-1267	224
844	S272	-1281	93
845	S271	-1295	224
846	S270	-1309	93
847	S269	-1323	224
848	S268	-1337	93
849	S267	-1351	224
850	S266	-1365	93

NO.	Pad	X	Y
851	S265	-1379	224
852	S264	-1393	93
853	S263	-1407	224
854	S262	-1421	93
855	S261	-1435	224
856	S260	-1449	93
857	S259	-1463	224
858	S258	-1477	93
859	S257	-1491	224
860	S256	-1505	93
861	S255	-1519	224
862	S254	-1533	93
863	S253	-1547	224
864	S252	-1561	93
865	S251	-1575	224
866	S250	-1589	93
867	S249	-1603	224
868	S248	-1617	93
869	S247	-1631	224
870	S246	-1645	93
871	S245	-1659	224
872	S244	-1673	93
873	S243	-1687	224
874	S242	-1701	93
875	S241	-1715	224
876	S240	-1729	93
877	S239	-1743	224
878	S238	-1757	93
879	S237	-1771	224
880	S236	-1785	93
881	S235	-1799	224
882	S234	-1813	93
883	S233	-1827	224
884	S232	-1841	93
885	S231	-1855	224
886	S230	-1869	93
887	S229	-1883	224
888	S228	-1897	93
889	S227	-1911	224
890	S226	-1925	93
891	S225	-1939	224
892	S224	-1953	93
893	S223	-1967	224
894	S222	-1981	93
895	S221	-1995	224
896	S220	-2009	93
897	S219	-2023	224
898	S218	-2037	93
899	S217	-2051	224
900	S216	-2065	93

NO.	Pad	X	Y
901	S215	-2079	224
902	S214	-2093	93
903	S213	-2107	224
904	S212	-2121	93
905	S211	-2135	224
906	S210	-2149	93
907	S209	-2163	224
908	S208	-2177	93
909	S207	-2191	224
910	S206	-2205	93
911	S205	-2219	224
912	S204	-2233	93
913	S203	-2247	224
914	S202	-2261	93
915	S201	-2275	224
916	S200	-2289	93
917	S199	-2303	224
918	S198	-2317	93
919	S197	-2331	224
920	S196	-2345	93
921	S195	-2359	224
922	S194	-2373	93
923	S193	-2387	224
924	S192	-2401	93
925	S191	-2415	224
926	S190	-2429	93
927	S189	-2443	224
928	S188	-2457	93
929	S187	-2471	224
930	S186	-2485	93
931	S185	-2499	224
932	S184	-2513	93
933	S183	-2527	224
934	S182	-2541	93
935	S181	-2555	224
936	S180	-2569	93
937	S179	-2583	224
938	S178	-2597	93
939	S177	-2611	224
940	S176	-2625	93
941	S175	-2639	224
942	S174	-2653	93
943	S173	-2667	224
944	S172	-2681	93
945	S171	-2695	224
946	S170	-2709	93
947	S169	-2723	224
948	S168	-2737	93
949	S167	-2751	224
950	S166	-2765	93

NO.	Pad	X	Y
951	S165	-2779	224
952	S164	-2793	93
953	S163	-2807	224
954	S162	-2821	93
955	S161	-2835	224
956	S160	-2849	93
957	S159	-2863	224
958	S158	-2877	93
959	S157	-2891	224
960	S156	-2905	93
961	S155	-2919	224
962	S154	-2933	93
963	S153	-2947	224
964	S152	-2961	93
965	S151	-2975	224
966	S150	-2989	93
967	S149	-3003	224
968	S148	-3017	93
969	S147	-3031	224
970	S146	-3045	93
971	S145	-3059	224
972	S144	-3073	93
973	S143	-3087	224
974	S142	-3101	93
975	S141	-3115	224
976	S140	-3129	93
977	S139	-3143	224
978	S138	-3157	93
979	S137	-3171	224
980	S136	-3185	93
981	S135	-3199	224
982	S134	-3213	93
983	S133	-3227	224
984	S132	-3241	93
985	S131	-3255	224
986	S130	-3269	93
987	S129	-3283	224
988	S128	-3297	93
989	S127	-3311	224
990	S126	-3325	93
991	S125	-3339	224
992	S124	-3353	93
993	S123	-3367	224
994	S122	-3381	93
995	S121	-3395	224
996	S120	-3409	93
997	S119	-3423	224
998	S118	-3437	93
999	S117	-3451	224
1000	S116	-3465	93

NO.	Pad	X	Y
1001	S115	-3479	224
1002	S114	-3493	93
1003	S113	-3507	224
1004	S112	-3521	93
1005	S111	-3535	224
1006	S110	-3549	93
1007	S109	-3563	224
1008	S108	-3577	93
1009	S107	-3591	224
1010	S106	-3605	93
1011	S105	-3619	224
1012	S104	-3633	93
1013	S103	-3647	224
1014	S102	-3661	93
1015	S101	-3675	224
1016	S100	-3689	93
1017	S99	-3703	224
1018	S98	-3717	93
1019	S97	-3731	224
1020	S96	-3745	93
1021	S95	-3759	224
1022	S94	-3773	93
1023	S93	-3787	224
1024	S92	-3801	93
1025	S91	-3815	224
1026	S90	-3829	93
1027	S89	-3843	224
1028	S88	-3857	93
1029	S87	-3871	224
1030	S86	-3885	93
1031	S85	-3899	224
1032	S84	-3913	93
1033	S83	-3927	224
1034	S82	-3941	93
1035	S81	-3955	224
1036	S80	-3969	93
1037	S79	-3983	224
1038	S78	-3997	93
1039	S77	-4011	224
1040	S76	-4025	93
1041	S75	-4039	224
1042	S74	-4053	93
1043	S73	-4067	224
1044	S72	-4081	93
1045	S71	-4095	224
1046	S70	-4109	93
1047	S69	-4123	224
1048	S68	-4137	93
1049	S67	-4151	224
1050	S66	-4165	93

NO.	Pad	X	Y
1051	S65	-4179	224
1052	S64	-4193	93
1053	S63	-4207	224
1054	S62	-4221	93
1055	S61	-4235	224
1056	S60	-4249	93
1057	S59	-4263	224
1058	S58	-4277	93
1059	S57	-4291	224
1060	S56	-4305	93
1061	S55	-4319	224
1062	S54	-4333	93
1063	S53	-4347	224
1064	S52	-4361	93
1065	S51	-4375	224
1066	S50	-4389	93
1067	S49	-4403	224
1068	S48	-4417	93
1069	S47	-4431	224
1070	S46	-4445	93
1071	S45	-4459	224
1072	S44	-4473	93
1073	S43	-4487	224
1074	S42	-4501	93
1075	S41	-4515	224
1076	S40	-4529	93
1077	S39	-4543	224
1078	S38	-4557	93
1079	S37	-4571	224
1080	S36	-4585	93
1081	S35	-4599	224
1082	S34	-4613	93
1083	S33	-4627	224
1084	S32	-4641	93
1085	S31	-4655	224
1086	S30	-4669	93
1087	S29	-4683	224
1088	S28	-4697	93
1089	S27	-4711	224
1090	S26	-4725	93
1091	S25	-4739	224
1092	S24	-4753	93
1093	S23	-4767	224
1094	S22	-4781	93
1095	S21	-4795	224
1096	S20	-4809	93
1097	S19	-4823	224
1098	S18	-4837	93
1099	S17	-4851	224
1100	S16	-4865	93

NO.	Pad	X	Y
1101	S15	-4879	224
1102	S14	-4893	93
1103	S13	-4907	224
1104	S12	-4921	93
1105	S11	-4935	224
1106	S10	-4949	93
1107	S9	-4963	224
1108	S8	-4977	93
1109	S7	-4991	224
1110	S6	-5005	93
1111	S5	-5019	224
1112	S4	-5033	93
1113	S3	-5047	224
1114	S2	-5061	93
1115	S1	-5075	224
1116	G319	-5131	93
1117	G317	-5145	224
1118	G315	-5159	93
1119	G313	-5173	224
1120	G311	-5187	93
1121	G309	-5201	224
1122	G307	-5215	93
1123	G305	-5229	224
1124	G303	-5243	93
1125	G301	-5257	224
1126	G299	-5271	93
1127	G297	-5285	224
1128	G295	-5299	93
1129	G293	-5313	224
1130	G291	-5327	93
1131	G289	-5341	224
1132	G287	-5355	93
1133	G285	-5369	224
1134	G283	-5383	93
1135	G281	-5397	224
1136	G279	-5411	93
1137	G277	-5425	224
1138	G275	-5439	93
1139	G273	-5453	224
1140	G271	-5467	93
1141	G269	-5481	224
1142	G267	-5495	93
1143	G265	-5509	224
1144	G263	-5523	93
1145	G261	-5537	224
1146	G259	-5551	93
1147	G257	-5565	224
1148	G255	-5579	93
1149	G253	-5593	224
1150	G251	-5607	93

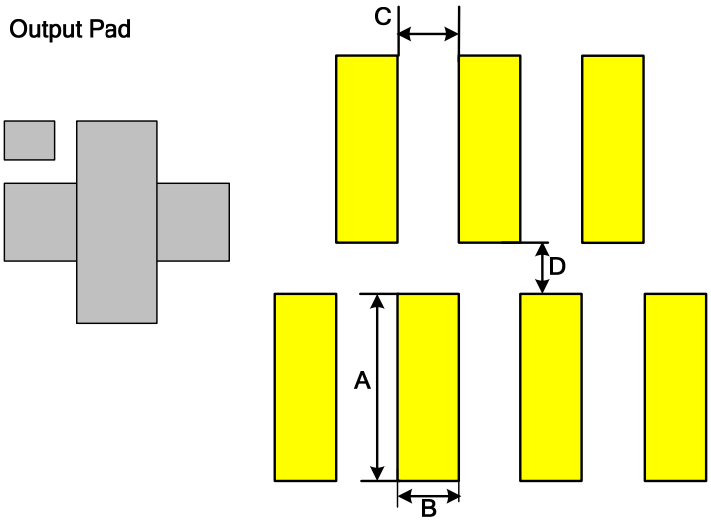
NO.	Pad	X	Y
1151	G249	-5621	224
1152	G247	-5635	93
1153	G245	-5649	224
1154	G243	-5663	93
1155	G241	-5677	224
1156	G239	-5691	93
1157	G237	-5705	224
1158	G235	-5719	93
1159	G233	-5733	224
1160	G231	-5747	93
1161	G229	-5761	224
1162	G227	-5775	93
1163	G225	-5789	224
1164	G223	-5803	93
1165	G221	-5817	224
1166	G219	-5831	93
1167	G217	-5845	224
1168	G215	-5859	93
1169	G213	-5873	224
1170	G211	-5887	93
1171	G209	-5901	224
1172	G207	-5915	93
1173	G205	-5929	224
1174	G203	-5943	93
1175	G201	-5957	224
1176	G199	-5971	93
1177	G197	-5985	224
1178	G195	-5999	93
1179	G193	-6013	224
1180	G191	-6027	93
1181	G189	-6041	224
1182	G187	-6055	93
1183	G185	-6069	224
1184	G183	-6083	93
1185	G181	-6097	224
1186	G179	-6111	93
1187	G177	-6125	224
1188	G175	-6139	93
1189	G173	-6153	224
1190	G171	-6167	93
1191	G169	-6181	224
1192	G167	-6195	93
1193	G165	-6209	224
1194	G163	-6223	93
1195	G161	-6237	224
1196	G159	-6251	93
1197	G157	-6265	224
1198	G155	-6279	93
1199	G153	-6293	224
1200	G151	-6307	93

NO.	Pad	X	Y
1201	G149	−6321	224
1202	G147	−6335	93
1203	G145	−6349	224
1204	G143	−6363	93
1205	G141	−6377	224
1206	G139	−6391	93
1207	G137	−6405	224
1208	G135	−6419	93
1209	G133	−6433	224
1210	G131	−6447	93
1211	G129	−6461	224
1212	G127	−6475	93
1213	G125	−6489	224
1214	G123	−6503	93
1215	G121	−6517	224
1216	G119	−6531	93
1217	G117	−6545	224
1218	G115	−6559	93
1219	G113	−6573	224
1220	G111	−6587	93
1221	G109	−6601	224
1222	G107	−6615	93
1223	G105	−6629	224
1224	G103	−6643	93
1225	G101	−6657	224
1226	G99	−6671	93
1227	G97	−6685	224
1228	G95	−6699	93
1229	G93	−6713	224
1230	G91	−6727	93
1231	G89	−6741	224
1232	G87	−6755	93
1233	G85	−6769	224
1234	G83	−6783	93
1235	G81	−6797	224
1236	G79	−6811	93
1237	G77	−6825	224
1238	G75	−6839	93
1239	G73	−6853	224
1240	G71	−6867	93
1241	G69	−6881	224
1242	G67	−6895	93
1243	G65	−6909	224
1244	G63	−6923	93
1245	G61	−6937	224
1246	G59	−6951	93
1247	G57	−6965	224
1248	G55	−6979	93
1249	G53	−6993	224
1250	G51	−7007	93

NO.	Pad	X	Y
1251	G49	−7021	224
1252	G47	−7035	93
1253	G45	−7049	224
1254	G43	−7063	93
1255	G41	−7077	224
1256	G39	−7091	93
1257	G37	−7105	224
1258	G35	−7119	93
1259	G33	−7133	224
1260	G31	−7147	93
1261	G29	−7161	224
1262	G27	−7175	93
1263	G25	−7189	224
1264	G23	−7203	93
1265	G21	−7217	224
1266	G19	−7231	93
1267	G17	−7245	224
1268	G15	−7259	93
1269	G13	−7273	224
1270	G11	−7287	93
1271	G9	−7301	224
1272	G7	−7315	93
1273	G5	−7329	224
1274	G3	−7343	93
1275	G1	−7357	224
1276	DUMMY28	−7371	93
1277	DUMMY29	−7385	224
1278	DUMMY30	−7399	93
	Left Mark	−7480	225
	Right Mark	7480	225

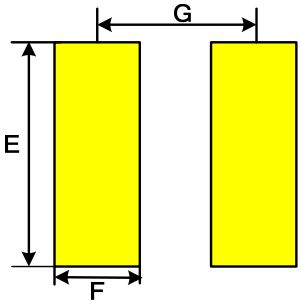
8. Bump Size

Output Pad



Symbol	Typical	Unit
A	100	um
B	14	
C	14	
D	31	

input Pad



Symbol	Typical	Unit
E	45.545	um
F	40	
G	85/72.5/60	

9. Command

9.1 Command list

Regulative commands

Command function	DC	W/R	D1 7-8	D7	D6	D5	D4	D3	D2	D1	D0	H/W default
No Operation	0	W	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	W	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification information	0	W	XX	0	0	0	0	0	1	0	0	04h
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	ID4[23：16]								00h
	1	R	XX	ID4[15：8]								30h
	1	R	XX	ID4[7：0]								33h
Read Display Status	0	W	XX	0	0	0	0	1	0	0	1	09h
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	boost_ status	madctl[7：2]						X	00h
	1	R	XX	X	color_mode[2:0]			idle	partial_mo de	sleep	normal_m ode	61h
	1	R	XX	scroll_ mode	X	inv_en	X	X	display_en	tear_en	gamset[2]	00h
	1	R	XX	gamset[1:0]		tear_m ode	X	X	X	X	X	00h
Read Display Power Mode	0	W	XX	0	0	0	0	1	0	1	0	0ah
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	boost_ status	idle	partial_ mode	sleep	normal _mode	display_en	X	X	08h
Read Display MADCTL	0	W	XX	0	0	0	0	1	0	1	1	0bh
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	madctl[7:0]								00h
Read Display Pixel Format	0	W	XX	0	0	0	0	1	1	0	0	0ch
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	rim	dpi[2:0]			X	dbi[2:0]			66h
Read Display Image Mode	0	W	XX	0	0	0	0	1	1	0	1	0dh
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	0	0	0	0	0	0	0	0	00h
Read Display Signal Mode	0	W	XX	0	0	0	0	1	1	1	0	0eh
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	te_on_ off	tear_m ode	rcm[2:0]			de_mode	X	X	3ch
Read Display self-Diagnostic Result	0	W	XX	0	0	0	0	1	1	1	1	0fh
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	reg_lo ad_det	func_de t	X	X	X	X	X	X	00h
Sleep In	0	W	XX	0	0	0	1	0	0	0	0	10h
Sleep Out	0	W	XX	0	0	0	1	0	0	0	1	11h
Partial Mode On	0	W	XX	0	0	0	1	0	0	1	0	12h
Normal Mode	0	W	XX	0	0	0	1	0	0	1	1	13h
Display Inversion Off	0	W	XX	0	0	1	0	0	0	0	0	20h
Display Inversion On	0	W	XX	0	0	1	0	0	0	0	1	21h
Display Off	0	W	XX	0	0	1	0	1	0	0	0	28h
Display On	0	W	XX	0	0	1	0	1	0	0	1	29h

Column Address	0	W	XX	0	0	1	0	1	0	1	0	2ah
	1	W	XX	caset_sc[15:8]								00h
	1	W	XX	caset_sc[7:0]								00h
	1	W	XX	caset_ec[15:8]								00h
	1	W	XX	caset_ec[7:0]								efh
Page Address	0	W	XX	0	0	1	0	1	0	1	1	2bh
	1	W	XX	paset_sp[15:8]								00h
	1	W	XX	paset_sp[7:0]								00h
	1	W	XX	paset_ep[15:8]								01h
	1	W	XX	paset_ep[7:0]								3fh
Memory Write	0	W	XX	0	0	1	0	1	1	0	0	2ch
	1	W	XX	D[7：0]								XX
Memory Read	0	W	XX	0	0	1	0	1	1	1	0	2eh
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	D[7：0]								XX
Partial Area	0	W	XX	0	0	1	1	0	0	0	0	30h
	1	W	XX	paset_sr[15:8]								00h
	1	W	XX	paset_sr[7:0]								00h
	1	W	XX	paset_er[15:8]								01h
	1	W	XX	paset_er[7:0]								3fh
Vertical Scrolling	0	W	XX	0	0	1	1	0	0	1	1	33h
	1	W	XX	vscrdef_tfa[15:8]								00h
	1	W	XX	vscrdef_tfa[7:0]								00h
	1	W	XX	vscrdef_vsa[15:8]								01h
	1	W	XX	vscrdef_vsa[7:0]								40h
	1	W	XX	vscrdef_bfa[15:8]								00h
	1	W	XX	vscrdef_bfa[7:0]								00h
Tear Effect Line Off	0	W	XX	0	0	1	1	0	1	0	0	34h
Tear Effect Line On	0	W	XX	0	0	1	1	0	1	0	1	35h
	1	W	XX	X	X	X	X	X	X	X	tear_en	00h
Memory Data Access Control	0	W	XX	0	0	1	1	0	1	1	0	36h
	1	W	XX	my	mx	mv	ml	bgr	mh	X	X	00h
Vertical Scroll Start address	0	W	XX	0	0	1	1	0	1	1	1	37h
	1	W	XX	vscrdef_vsp[15:8]								00h
	1	W	XX	vscrdef_vsp[7:0]								00h
Idle Mode Off	0	W	XX	0	0	1	1	1	0	0	0	38h
Idle Mode On	0	W	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	W	XX	0	0	1	1	1	0	1	0	3ah
	1	W	XX	X	dpi[2:0]			X	dbi[2:0]			66h
Write Memory Continue	0	W	XX	0	0	1	1	1	1	0	0	3ch
	1	W	XX	D[7：0]								XX
Read memory Continue	0	W	XX	0	0	1	1	1	1	1	0	3eh
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	D[7：0]								XX
Set Tear Scanline	0	W	XX	0	1	0	0	0	1	0	0	44h
	1	W	XX	X	X	X	X	X	X	X	sts[8]	00h
	1	W	XX	sts[7:0]								00h

Get Tear Scanline	0	W	XX	0	1	0	0	0	1	0	1	45h
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	X	X	X	X	X	X	gts[9:8]		00h
	1	R	XX	gts[7:0]								00h
Read IDD3	0	W	XX	1	1	0	1	0	0	1	1	d3h
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	idd3[23:16]								00h
	1	R	XX	idd3[15:8]								30h
	1	R	XX	idd3[7:0]								33h
Read ID1	0	W	XX	1	1	0	1	1	0	1	0	dah
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	id4[23:16]								00h
Read ID2	0	W	XX	1	1	0	1	1	0	1	1	dbh
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	id4[15:8]								30h
Read ID3	0	W	XX	1	1	0	1	1	1	0	0	dch
	1	R	XX	X	X	X	X	X	X	X	X	XX
	1	R	XX	id4[7:0]								33h

Extended commands（Set FDH register when accessing Extended commands）

Command function	DC	W/R	D 17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex default
Power Control 0	0	W	XX	0	1	1	0	0	0	0	0	60h
	1	W	XX	X	vrh[6:0]							10h
Power Control 1	0	W	XX	0	1	1	0	0	1	0	0	64h
	1	W	XX	x	x	ga_ap[1:0]		com_ap[1:0]		cmp_ap[1:0]		00h
Power Control 2	0	W	XX	0	1	1	0	0	1	0	1	65h
	1	W	XX	X	X	X	X	vreg_ap[1:0]		X	X	00h
Power Control 3	0	W	XX	0	1	1	0	0	1	1	0	66h
	1	W	XX	vram[1:0]		X	osc_trim[4:0]					90h
Power Control 4	0	W	XX	0	1	1	0	1	0	0	1	69h
	1	W	XX	X	X	dc_vghl[1:0]		dc_vcl[1:0]		dc_ddvdh[1:0]		1ah
Power Control 5	0	W	XX	0	1	1	0	1	0	1	0	6ah
	1	W	XX	src_str	com_ str	X	X	sap2[1:0]		sap[1:0]		00h
Power Control 6	0	W	XX	0	1	1	0	1	1	1	0	6eh
	1	W	XX	ddvdh_set[3:0]				x	x	x	x	84h
Power Control 7	0	W	XX	0	1	1	1	0	0	0	1	71h
	1	W	XX	x	vgh_set[2:0]			x	vgl_set[2:0]			52h
Vcom Control 1	0	W	XX	0	1	1	0	1	0	1	1	6bh
	1	W	XX	x	x	vcm[5:0]						31h
Vcom Control 2	0	W	XX	0	1	1	0	1	1	0	0	6ch
	1	W	XX	x	x	x	vdv[4:0]					18h
RGB Interface Control	0	W	XX	1	0	1	1	0	0	0	0	b0h
	1	W	XX	bypass _mode	rcm[1:0]		X	vspl	hspl	dpl	epl	40h
Frame Rate1	0	W	XX	1	0	1	1	0	0	0	1	b1h
	1	W	XX	X	X	X	X	X	X	Divi[1:0]		00h
	1	W	XX	X	X	X	rtni[4:0]					17h
Frame Rate2	0	W	XX	1	0	1	1	0	0	1	0	b2h
	1	W	XX	X	X	X	X	X	X	dive[1:0]		00h

Display Inversion	0	W	XX	1	0	1	1	0	1	0	0	b4h
	1	W	XX	X	X	X	X	X	nla	nlb	nlc	02h
Blanking Porch	0	W	XX	1	0	1	1	0	1	0	1	b5h
	1	W	XX	X	vfp[6:0]							02h
	1	W	XX	X	vbp[6:0]							02h
	1	W	XX	X	X	X	hfp[4:0]					0ah
	1	W	XX	X	X	X	hbp[4:0]					14h
Display Function	0	W	XX	1	0	1	1	0	1	1	0	b6h
	1	W	XX	X	X	X	X	ptg[1:0]		pts[1:0]		0ah
	1	W	XX	rev	gs	ss	sm	isc[3:0]				82h
	1	W	XX	X	X	nl[5:0]						27h
Entry Mode Set	0	W	XX	1	0	1	1	0	1	1	1	b7h
	1	W	XX	X	X	X	X	X	gon	dte	X	06h
gamma positive 1	0	W	XX	1	1	1	0	0	0	0	0	e0h
	1	W	XX	X	X	X	pkp0[4:0]					0bh
	1	W	XX	X	X	X	pkp1[4:0]					17h
	1	W	XX	X	X	X	pkp2[4:0]					06h
	1	W	XX	X	X	X	pkp3[4:0]					10h
	1	W	XX	X	X	X	pkp4[4:0]					05h
	1	W	XX	X	X	X	pkp5[4:0]					12h
	1	W	XX	X	X	X	pkp6[4:0]					0ah
Gamma Positive 2	0	W	XX	1	1	1	0	0	0	0	1	e1h
	1	W	XX	X	prp0[6:0]							1bh
	1	W	XX	X	prp1[6:0]							5ah
Gamma Positive 3	0	W	XX	1	1	1	0	0	0	1	0	e2h
	1	W	XX	X	X	vrp0[5:0]						0ah
	1	W	XX	X	X	vrp1[5:0]						2eh
	1	W	XX	X	X	vrp2[5:0]						27h
	1	W	XX	X	X	vrp3[5:0]						19h
	1	W	XX	X	X	vrp4[5:0]						18h
	1	W	XX	X	X	vrp5[5:0]						2bh
Gamma Negative 1	0	W	XX	1	1	1	0	0	0	1	1	e3h
	1	W	XX	X	X	X	pkn0[4:0]					0ch
	1	W	XX	X	X	X	pkn1[4:0]					19h
	1	W	XX	X	X	X	pkn2[4:0]					0fh
	1	W	XX	X	X	X	pkn3[4:0]					19h
	1	W	XX	X	X	X	pkn4[4:0]					08h
	1	W	XX	X	X	X	pkn5[4:0]					13h
	1	W	XX	X	X	X	pkn6[4:0]					13h
Gamma Negative 2	0	W	XX	1	1	1	0	0	1	1	1	e4h
	1	W	XX	X	prn0[6:0]							1bh
	1	W	XX	X	prn1[6:0]							5ah
Gamma Negative 3	0	W	XX	1	1	1	0	1	0	0	0	e5h
	1	W	XX	X	X	vrn0[5:0]						0ah
	1	W	XX	X	X	vrn1[5:0]						22h
	1	W	XX	X	X	vrn2[5:0]						20h
	1	W	XX	X	X	vrn3[5:0]						13h
	1	W	XX	X	X	vrn4[5:0]						0ch
	1	W	XX	X	X	vrn5[5:0]						2bh
Gate driver timing	0	W	XX	1	1	1	0	1	1	0	0	ech
	1	W	XX	nowe[3:0]				nowi[3:0]				33h
	1	W	XX	nowi_e[7:0]								16h
	1	W	XX	nowe_e[7:0]								16h

	1	W	XX	gcse[3:0]				gcsi[3:0]				44h
	1	W	XX	gcsi_e[7:0]								15h
	1	W	XX	gcse_e[7:0]								15h
Source, VCOM driver timing	0	W	XX	1	1	1	0	1	1	0	1	edh
	1	W	XX	vcsie	vcsiv[2:0]			scsie	scsiv[2:0]			bbh
	1	W	XX	vcsee	vcsev[2:0]			scsee	scsev[2:0]			bbh
	1	W	XX	X	mcpe[2:0]			X	mcpi[2:0]			00h
	1	W	XX	X	mspe[2:0]			X	mspi[2:0]			00h
	1	W	XX	X	lde[2:0]			X	ldi[2:0]			11h
	1	W	XX	X	com_cs_str_delay[2:0]			X	X	cs_delay[1:0]		21h
interface control	0	W	XX	1	1	1	1	0	1	1	0	f6h
	1	W	XX	my_eor	mx_eor	mv_eor	0	bgr_eor	0	0	we mode	01h
	1	W	XX	X	X	epf[1:0]		X	X	mdt[1:0]		10h
	1	W	XX	spi_2wire_mode	X	endian	X	dm[1:0]		rm	rim	00h
lcd ac drive control	0	W	XX	1	1	1	1	0	1	1	1	f7h
	1	W	XX	X	X	X	frc_en	X	X	nw[1:0]		10h
private access	0	W	XX	1	1	1	1	1	1	0	1	fdh
	1	W	XX	private_access[15:8]								00h
	1	W	XX	private_access[7:0]								00h

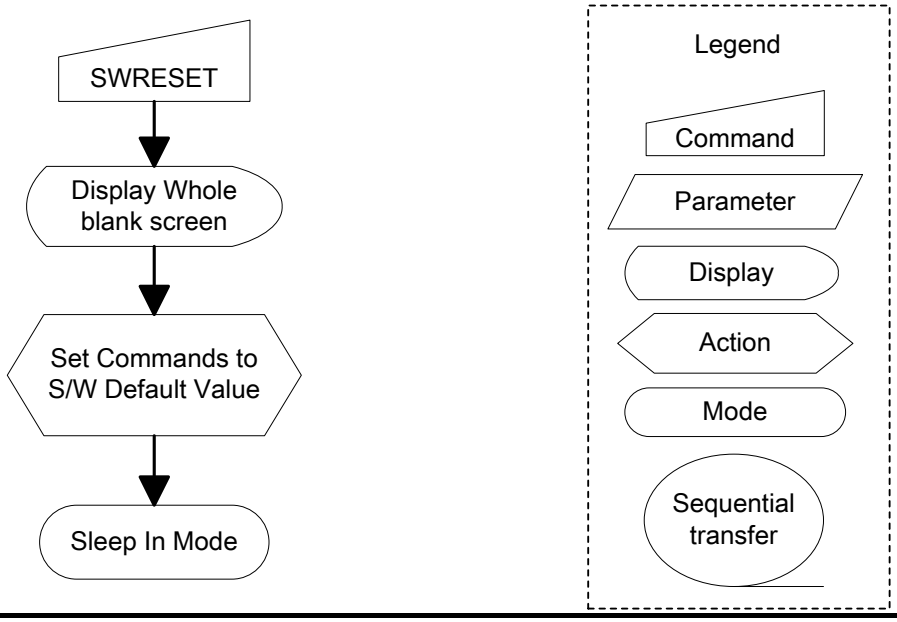
9.2 Command description

9.2.1 System interface command description

9.2.1.1 NOP (00h)

<table>
<tr><td>00h</td><td colspan="12">NOP （No Operation）</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Parameter</td><td colspan="12">No parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is empty command. It does not have any effect on the display module. However it can be used to terminate frame memory write as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.
X=Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep in or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
</table>

9.2.1.2 Software Reset (01h)

<table>
<tr><td>01h</td><td colspan="12">SWRESET(Software Reset)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01</td></tr>
<tr><td>Parameter</td><td colspan="13">No parameter</td></tr>
<tr><td>Description</td><td colspan="13">When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Note: The Frame Memory contents are unaffected by this command.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">It will be necessary to wait 5 msec before sending new command following software reset.The display module loads all display suppliers’ factory default values to the registers during this 5 msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120 msec before sending Sleep Out command. Software Reset Command cannot be sent during Sleep Out sequence.</td></tr>
<tr><td>Register availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="13"> 
</td></tr>
</table>

9.2.1.3 Read Display Identification Information (04h)

04h	RDDIDIF (Read Display Identification Information)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04
1st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	XX	ID4[23:16]								00
3rd parameter	1	↑	1	XX	ID4[15:8]								30
4th parameter	1	↑	1	XX	ID4[7:0]								33
Description	This read byte returns 24-bits display identification information. The 1st Parameter is dummy read. The 2nd Parameter identifies the LCD module's manufacture. The 3rd Parameter identifies the LCD module/driver version ID. The 4th Parameter identifies the LCD module/driver ID. X = Don't care.												
Restriction													

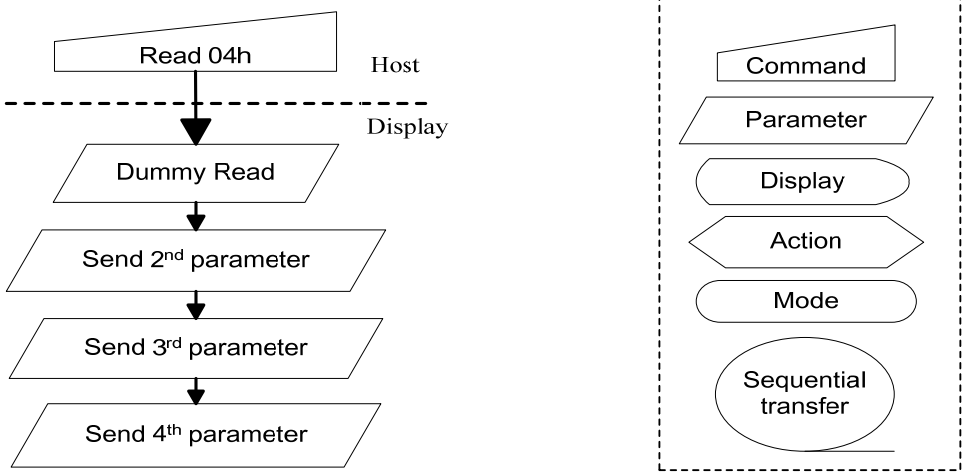
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	24'h003031
S/W Reset	24'h003031
H/W Reset	24'h003031

Flow Chart



9.2.1.4 Read Display Status (09h)

09h	RDDST (Read Display Status)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09
1st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	XX	boost_ status	Madctl[7:2]						X	00
3rd parameter	1	↑	1	XX	X	color_mode[2:0]			idle	partial_ mode	sleep	normal_ mode	61
4th parameter	1	↑	1	XX	scroll_ mode	X	inv_en	X	X	display_en	tear_en	gamset[2]	00
5th parameter	1	↑	1	XX	gamset[1:0]		tear_mode	X	X	X	X	X	00

Description

This command indicates the current status of the display as described in the table below:
（**the table 1**）

Bit	Description	Value	Comment
boost_status	Booster Voltage Status	0	Booster Off
		1	Booster On
Madctl [7...2]	Page Address Order	0	Top to Bottom (When MADCTL B7 = ‘0’)
		1	Bottom to Top (When MADCTL B7 = ‘1’)
	Column Address Order	0	Left to Right (When MADCTL B6 = ‘0’)
		1	Right to Left (When MADCTL B6 = ‘1’)
	Page/Column Order	0	Normal Mode (When MADCTL B5 = ‘0’)
		1	Reverse Mode (When MADCTL B5 = ‘1’)
	Line Address Order	0	LCD Refresh Top to Bottom (When MADCTL B4 = ‘0’)
		1	LCD Refresh Bottom to Top (When MADCTL B4 = ‘1’)
	RGB/BGR Order		RGB (When MADCTL B3 = ‘0’)
			BGR (When MADCTL B3 = ‘1’)
	-	0	Set to ‘0’
color_mode[2:0]	Interface Color Pixel Format Definition		Detailed in **the table 2**
idle	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
partial_mode	Partial Mode On/Off	0	Partial Mode Off
		1	Partial Mode On
sleep	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode.
Normal_mode	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
scroll_mode	Vertical Scrolling Status	0	Vertical Scrolling is Off
		1	Vertical Scrolling is On
inv_en	Inversion Status	0	Inversion is Off
		1	Inversion is On
display_en	Display On/Off	0	Display is Off
		1	Display is On
tear_en	Tearing Effect Line On/Off	0	Tearing Effect Line Off
		1	Tearing Effect Line On
tear_mode	Tearing Effect Output Line Mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking
D[4…0]	For Future Use	0	Set to ‘0’
Others	-	0	Set to ‘0’

Bits color_mode[2:0]: Interface Color Pixel Format Definition
（the table 2）

Interface Format	color_mode[2]	color_mode[1]	color_mode[0]
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
18 Bit/Pixel	1	1	1

Note:

1. For Bits Madctl [7:5], also refer to Section 10.2.3 MCU to Memory write/read direction.
2. For Bits Madctl [4:2] also refer to 9.2.1.27 Memory Access Control (36h).

X = Don't care.

Restriction

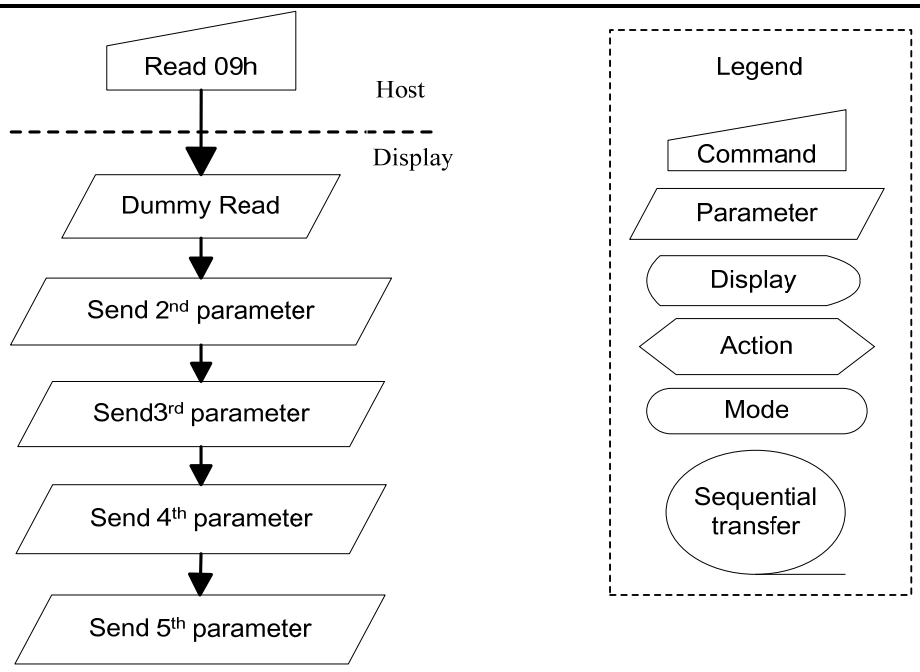
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart



9.2.1.5 Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0A
1st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	XX	boost_ status	idle	partial _mode	sleep	normal _mode	display _en	X	X	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Comment
boost_status	Booster Voltage Status	0	Booster Off or has a fault
		1	Booster On and working OK
idle	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
partial_mode	Partial Mode On/Off	0	Partial Mode Off
		1	Partial Mode On
sleep	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
normal_mode	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
display_en	Display On/Off	0	Display Off
		1	Display On
others	-	0	Set to '0'

X = Don't care.

Restriction

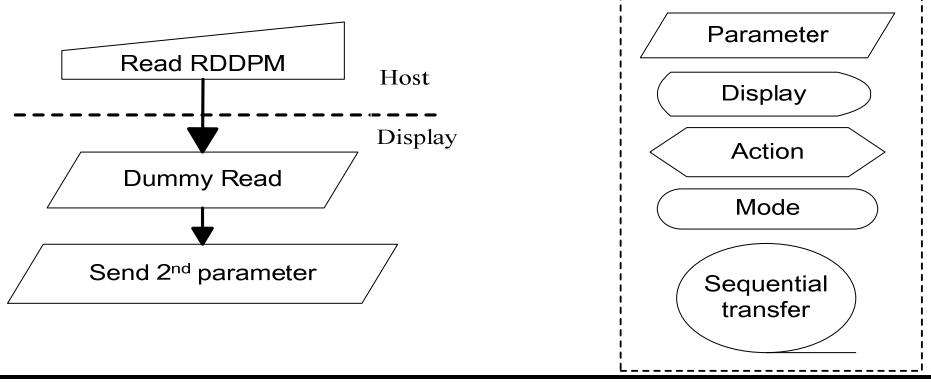
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep in or Booster Off	Yes

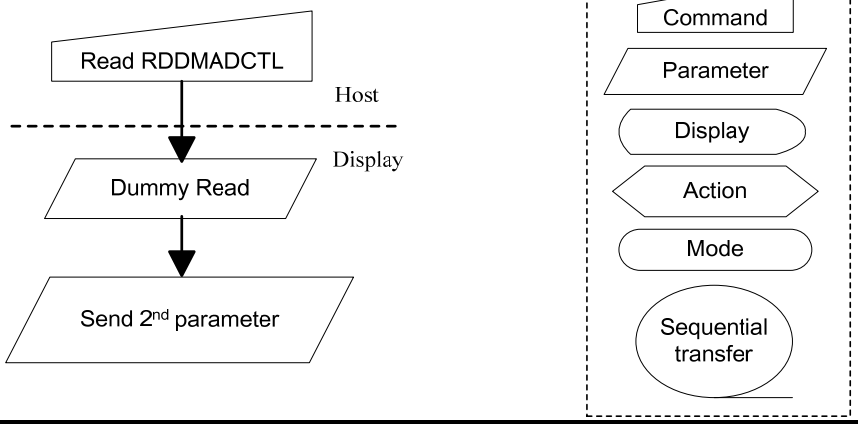
Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



9.2.1.6 Read Display Madctl (0Bh)

<table>
<tr><td>0Bh</td><td colspan="13">RDDMADCTL (Read Display MADCTL)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">madctl[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">Madctl[7]</td><td rowspan="2">Page Address Order</td><td>0</td><td>Top to Bottom (When MADCTL B7=’0’).</td></tr>
<tr><td>1</td><td>Bottom to Top (When MADCTL B7=’1’).</td></tr>
<tr><td rowspan="2">Madctl[6]</td><td rowspan="2">Column Address Order</td><td>0</td><td>Left to Right (When MADCTL B6=’0’)</td></tr>
<tr><td>1</td><td>Right to Left (when MADCTL B6=’1’</td></tr>
<tr><td rowspan="2">Madctl[5]</td><td rowspan="2">Page/Column Order</td><td>0</td><td>Normal Mode (When MADCTL B5=’0’).</td></tr>
<tr><td>1</td><td>Reverse Mode (When MADCTL B5=’1’)</td></tr>
<tr><td rowspan="2">Madctl[4]</td><td rowspan="2">Line Address Order</td><td>0</td><td>LCD Refresh Top to Bottom (When MADCTL B4=’0’)</td></tr>
<tr><td>1</td><td>LCD Refresh Bottom to Top (When MADCTL B4=’1’)</td></tr>
<tr><td rowspan="2">Madctl[3]</td><td rowspan="2">RGB/BGR Order</td><td>0</td><td>RGB (When MADCTL B3=’0’)</td></tr>
<tr><td>1</td><td>“1”: BGR (When MADCTL B3=’1’)</td></tr>
<tr><td>others</td><td>-</td><td>0</td><td>Set to ‘0’</td></tr>
</table>
Note:
1. For Bits Madctl[7…5], also refer to Section 10.2.3 MCU to Memory write/read direction.
2. For Bits Madctl[4] also refer to 9.2.1.27 Memory Access Control (36h).
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep in or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

9.2.1.7 Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD(Read Display COLMOD)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0C
1st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd parameter	1	↑	1	XX	rim	dpi[2:0]			X	dbi[2:0]			66

Description

This command indicates the current status of the display as described in the table below:

rim	dpi[2:0]			RGB interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16bit/pixel
0	1	1	0	18bit/pixel
0	1	1	1	Reserved
1	1	0	1	16bit/pixel(6-bit 3 times data transfer)
1	1	1	0	18bit/pixel(6-bit 3 times data transfer)

dbi[2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16bit/pixel
1	1	0	18bit/pixel
1	1	1	Reserved

X=Don't care.

Restriction

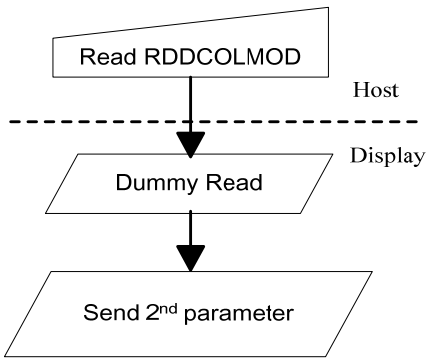
Register Availability

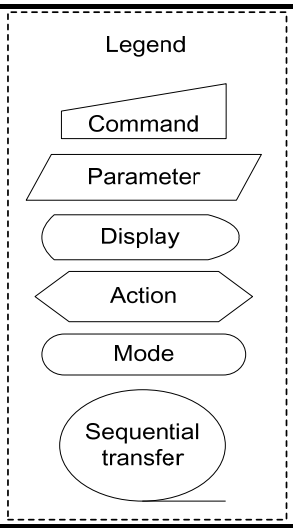
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	66h
S/W Reset	No change
H/W Reset	66h

Flow Chart





9.2.1.8 Read Display Image Mode (0Dh)

0Dh	RDDIM(Read Display Image Mode)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0D
1st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd parameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00
Description	No Description.												
Restriction													

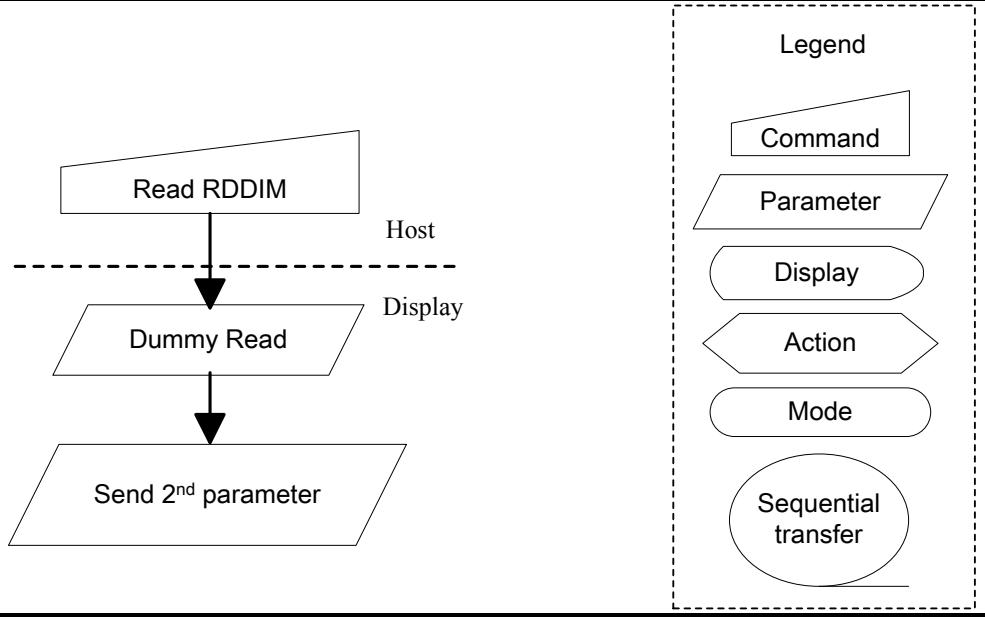
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No change
H/W Reset	00h

Flow Chart



9.2.1.9 Read Display Signal Mode (0Eh)

0EH	RDDSM(Read Display Signal Mode)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd parameter	1	↑	1	XX	te_on_off	tear_mode	rcm[2:0]			de_mode	X	X	3c

Description

This command indicates the current status of the display as described below:

Bit	Value	Description
te_on_off	0	Tearing Effect Line Off
	1	Tearing Effect On
tear_mode	0	Mode 1（Tearing Effect Line Output Mode, see section 10.3）
	1	Mode 2（Tearing Effect Line Output Mode, see section 10.3）
rcm[2]	0	set to ‘0’
rcm[1]	0	set to ‘0’
rcm[0]	0	set to ‘0’
others	0	set to ‘0’

X=Don’t care.

Restriction

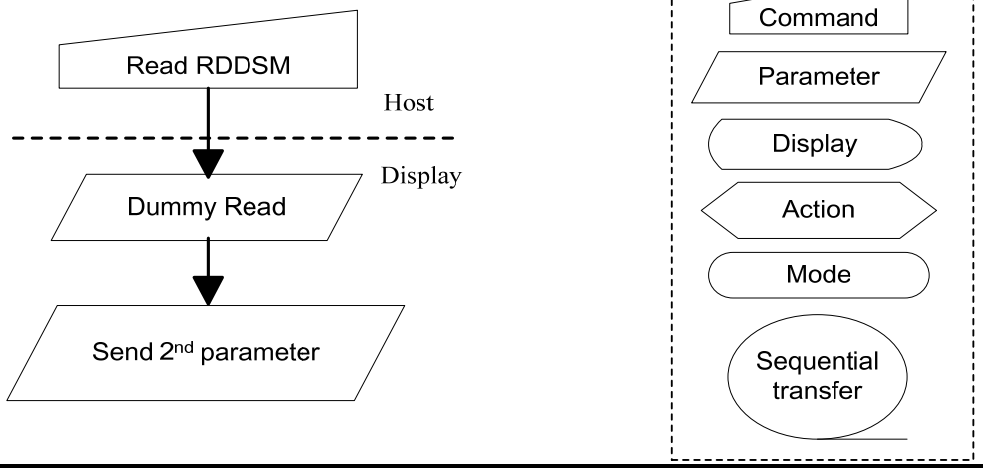
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3ch
S/W Reset	3ch
H/W Reset	3ch

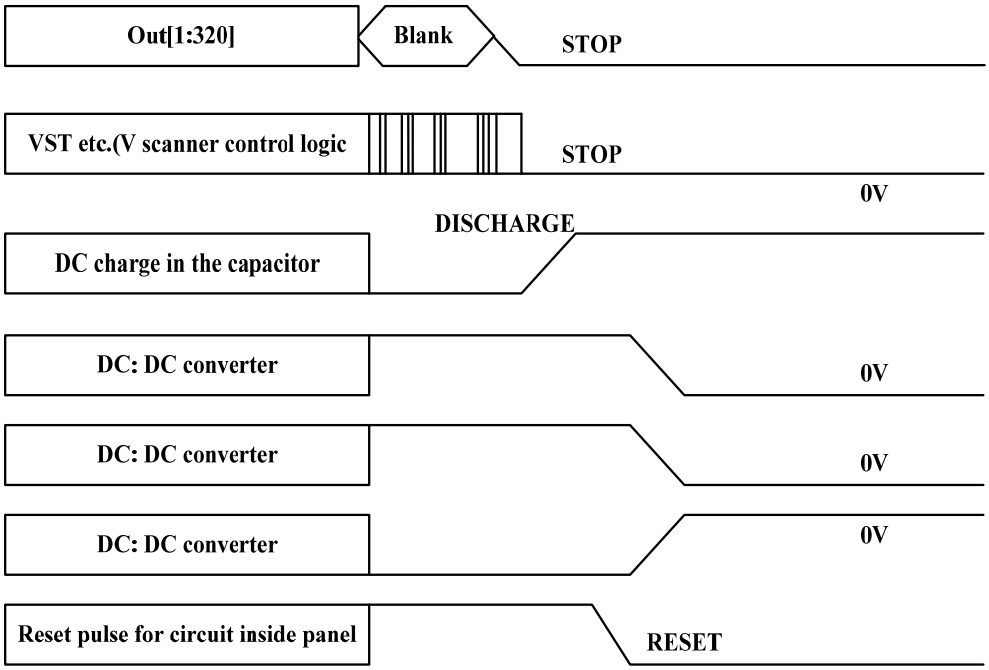
Flow Chart



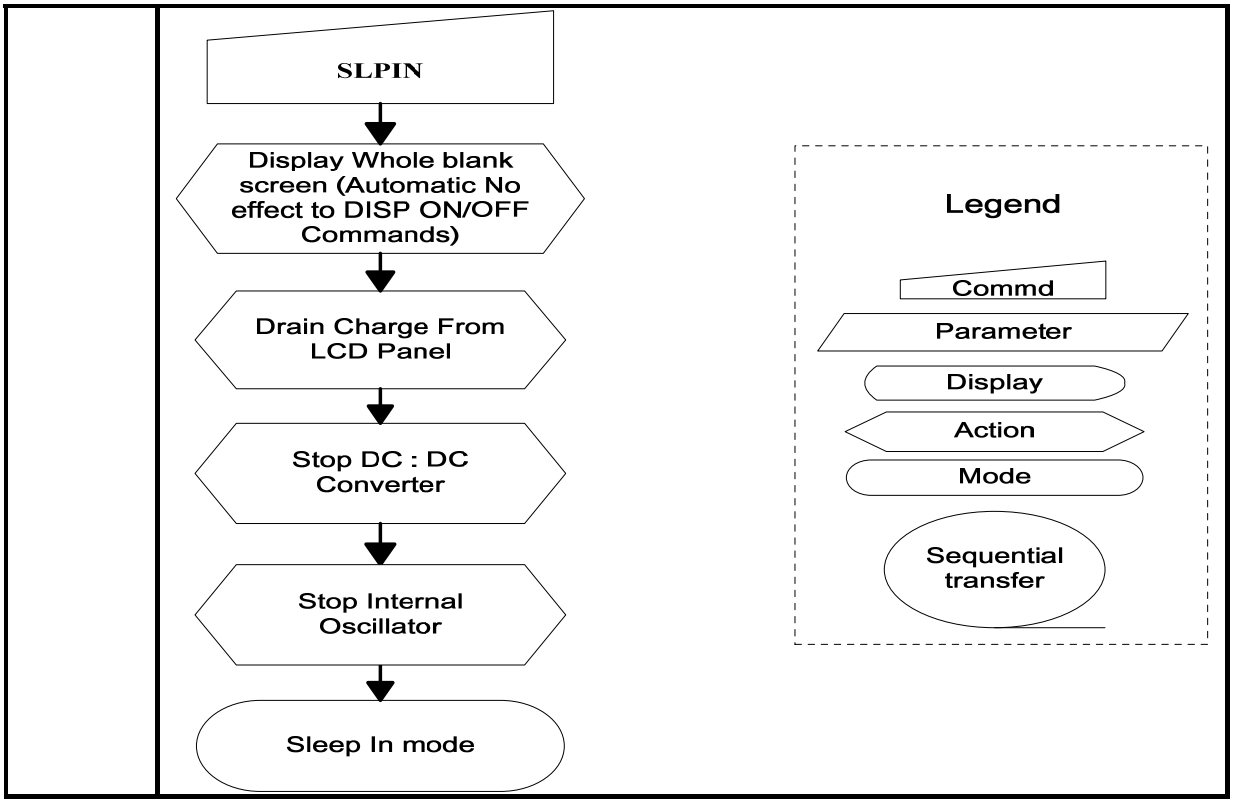
9.2.1.10 Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><td>0Fh</td><td colspan="13">RDDSDR(Read Display Self-Diagnostic Result)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0F</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>reg_load_det</td><td>func_det</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Action</th></tr>
<tr><td>reg_load_det</td><td>Register loading detection</td><td>Inverting the D7 bit if registers values loading work properly</td></tr>
<tr><td>func_det</td><td>Functionality detection</td><td>Inverting the D6 bit if the display is on function</td></tr>
<tr><td>others</td><td>-</td><td>Set to‘0’</td></tr>
</table>
X=Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

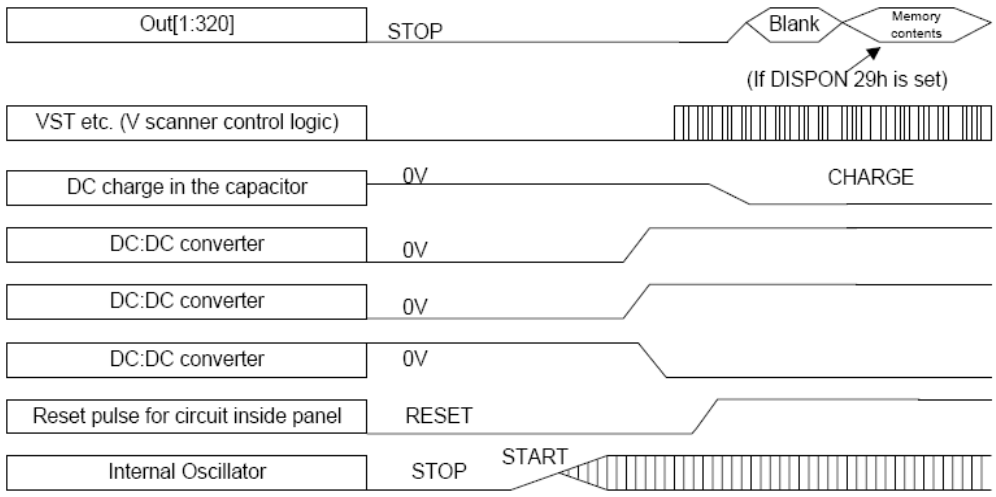
9.2.1.11 Sleep In (10h)

<table>
<tr><td>10h</td><td colspan="13">SLPIN(Sleep In)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode.
In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. MCU interfaces and memory are still working and the memory keeps its contents.
See also section 10.5.2.
 

X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in Sleep in mode. Sleep in mode can only be left by the Sleep Out command (11h).It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize.It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">It takes 120msec to get into Sleep In mode after SLPIN command issued.</td></tr>
</table>


SLPIN
Display Whole blank screen (Automatic No effect to DISP ON/OFF Commands)
Drain Charge From LCD Panel
Stop DC : DC Converter
Stop Internal Oscillator
Sleep In mode
Legend
Commd
Parameter
Display
Action
Mode
Sequential transfer

9.2.1.12 Sleep Out (11h)

11h	SLPOUT(Sleep Out)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. See also section 10.5.2.  X = Don't care.												
Restriction	This command has no effect when module is already in Sleep Out mode,Sleep Out mode can only be left by the Sleep in command(10h).It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done when the display module is already Sleep Out-mode.The display module is doing self-diagnostic function during this 5msec.It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out Mode) before Sleep Out command can be sent.												

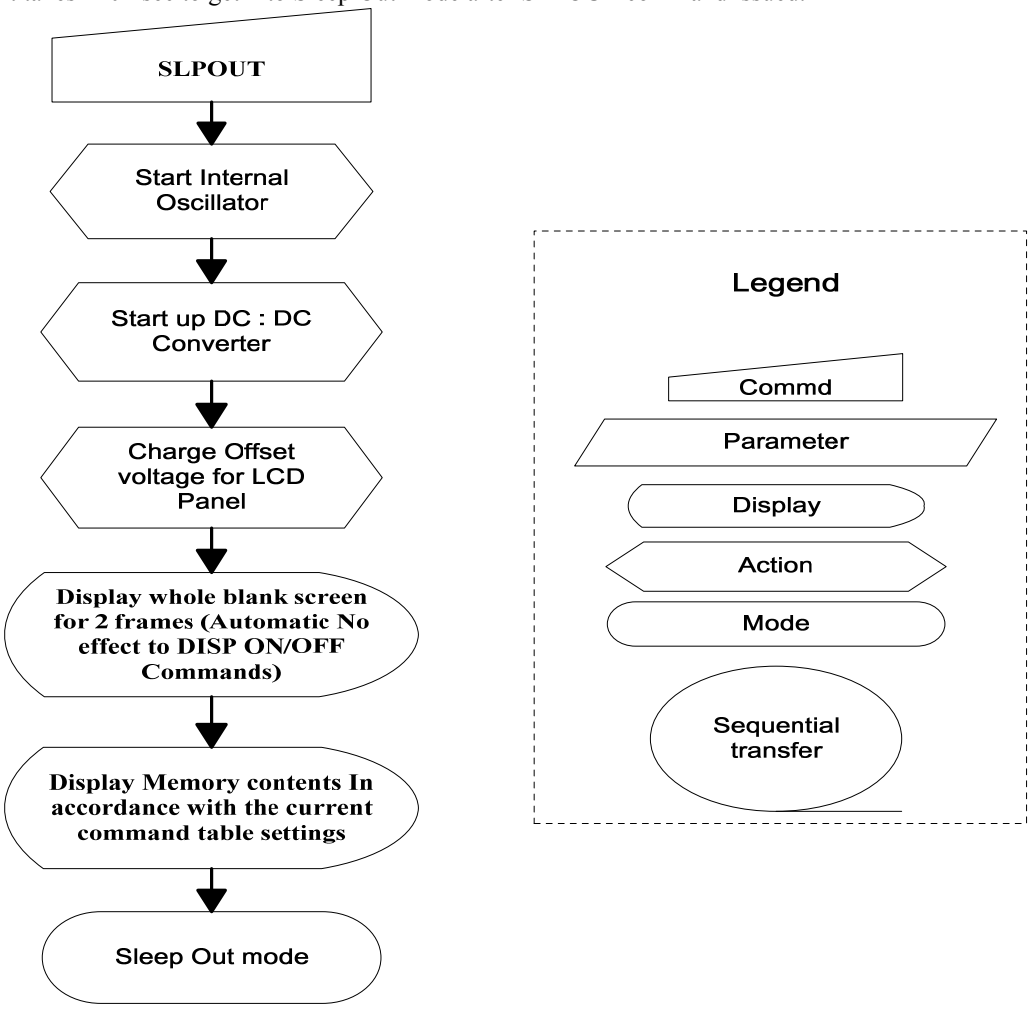
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart	It takes 120msec to get into Sleep Out mode after SLPOUT command issued.



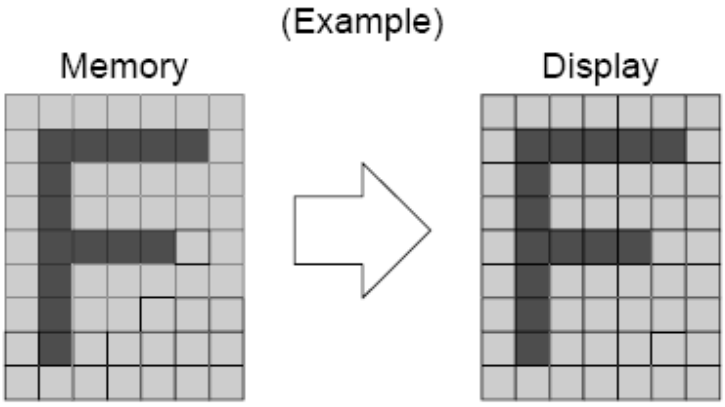
9.2.1.13 Partial Mode On (12h)

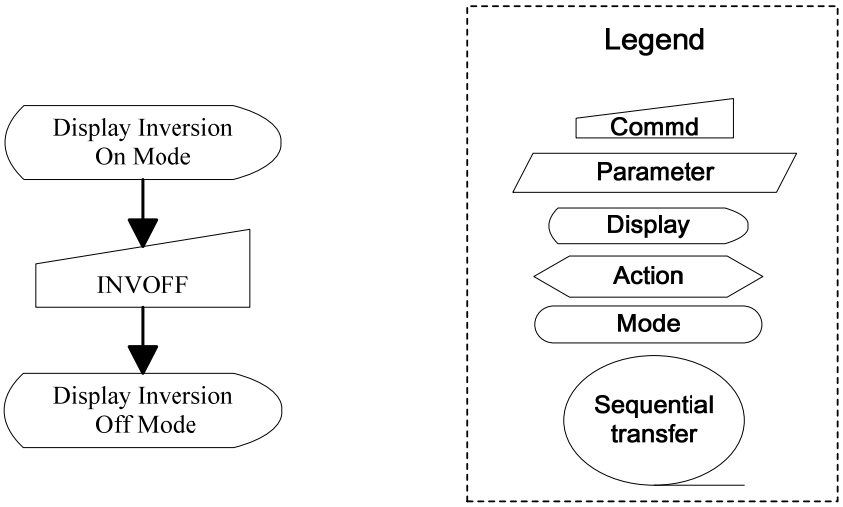
12h	PTLON(Partial Mode On)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Parameter	NO PARAMETER												
Description	This command turns on partial mode. The partial mode window is described by the Partial Area Command (30H).To leave Partial mode, the Normal Display Mode command (13H) should be written. See also section 10.5.2. X = Don't care.												
Restriction	This command has no effect when Partial mode is active.												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: Normal Display Mode On Status: S/W Reset — Default Value: Normal Display Mode On Status: H/W Reset — Default Value: Normal Display Mode On												
Flow Chart	See Partial Area (30h).												

9.2.1.14 Normal Display Mode On (13h)

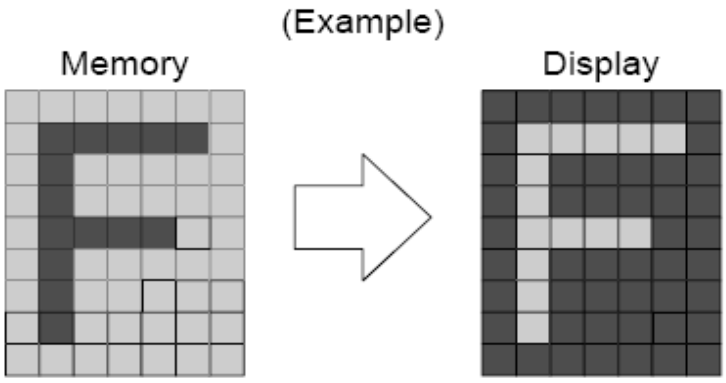
13h	NORON (Normal Display Mode On)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER												
Description	This command returns the display to normal mode. Normal Display Mode On means Partial mode off. See also section 10.5.2. X = Don't care.												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In or Booster Off — Availability: Yes												
Default	Status: Power On Sequence — Default Value: Normal Display Mode On Status: S/W Reset — Default Value: Normal Display Mode On Status: H/W Reset — Default Value: Normal Display Mode On												
Flow Chart	See Partial Area(30h).												

9.2.1.15 Display Inversion Off (20h)

<table>
<tr><td>20h</td><td colspan="12">DINVOFF (Display Inversion Off)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20h</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to receover from display in version mode. This command makes No Change of contents of frame memory.
This command does not change any other status.
 

X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in inversion off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

9.2.1.16 Display Inversion On (21h)

21h	DINVON (Display Inversion On)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	NO PARAMETER												
Description	This command is used to enter into display inversion mode. This command makes No Change of contents of frame memory.  X=Don't care.												
Restriction	This command has no effect when module is already in inversion on mode.												

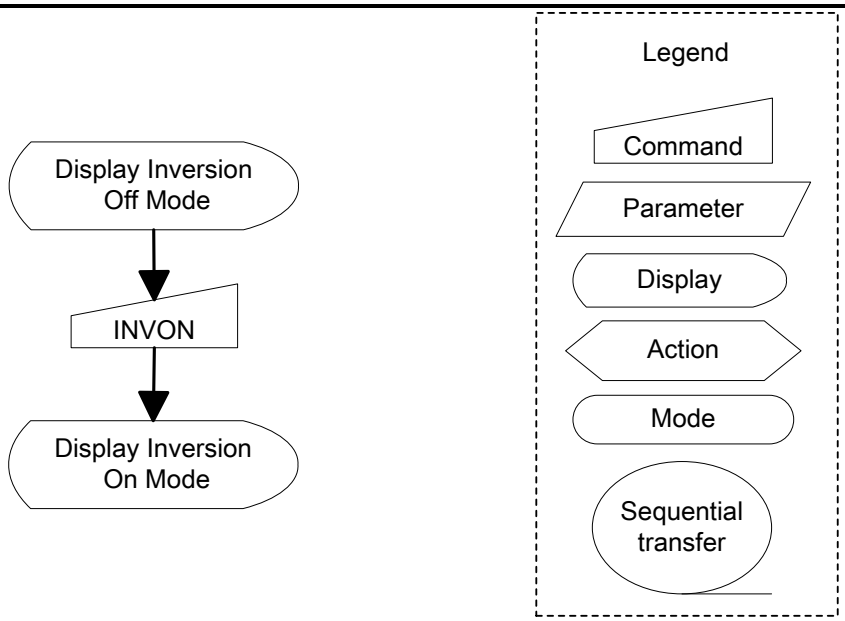
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

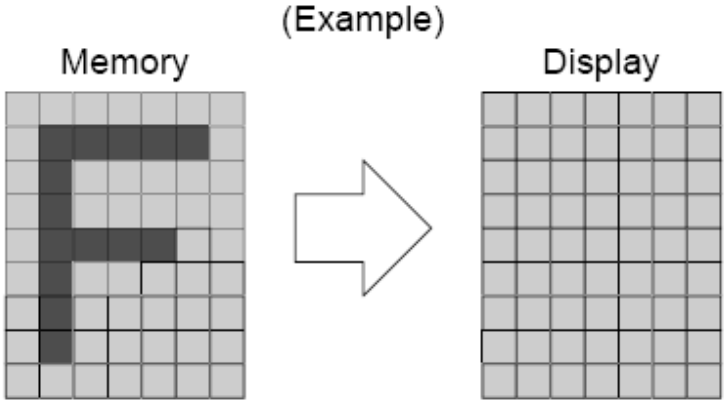
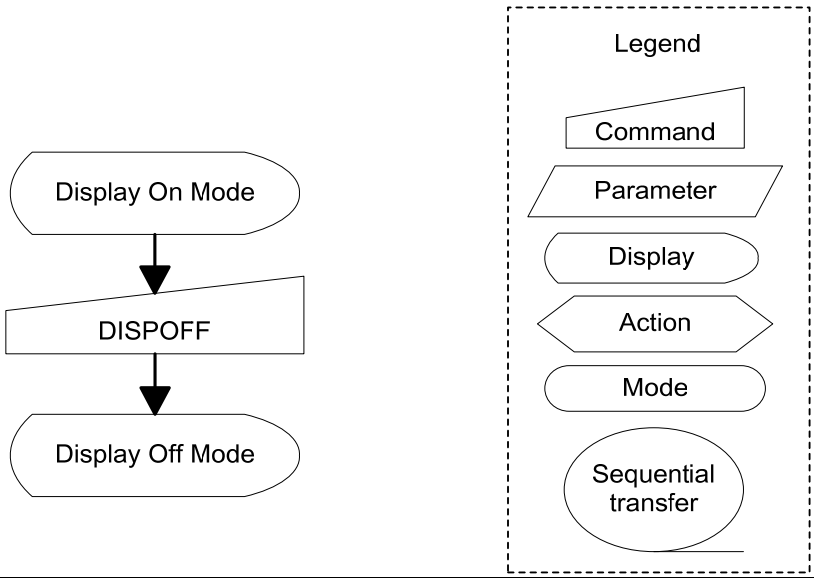
Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

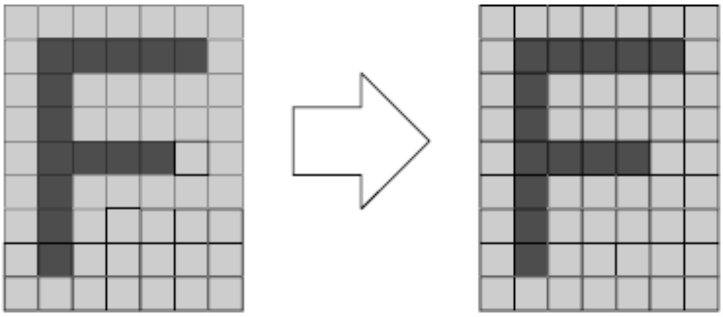
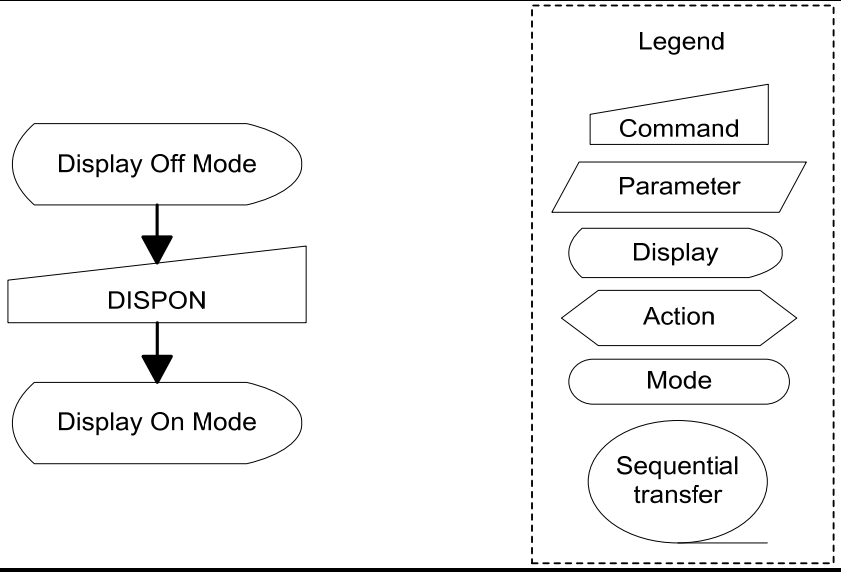
Flow Chart



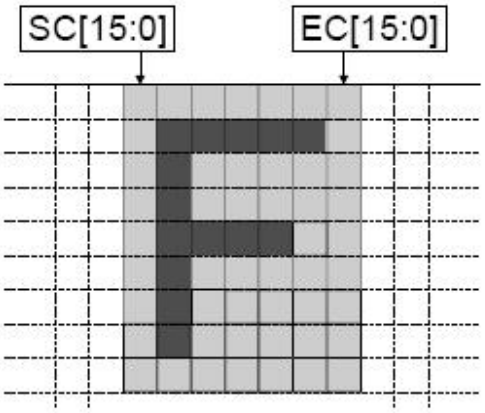
9.2.1.17 Display Off (28h)

<table>
<tr><td>28h</td><td colspan="12">DISPOFF(Display Off)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into Display Off mode.
In this mode, the output from Frame Memory is disabled and blank page is inserted.
This command is makes No Change any other status.
There will be no abnormal visible effect on the display.
This command is makes No Change of contents of frame memory.
 
X=Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">  </td></tr>
</table>

9.2.1.18 Display On(29h)

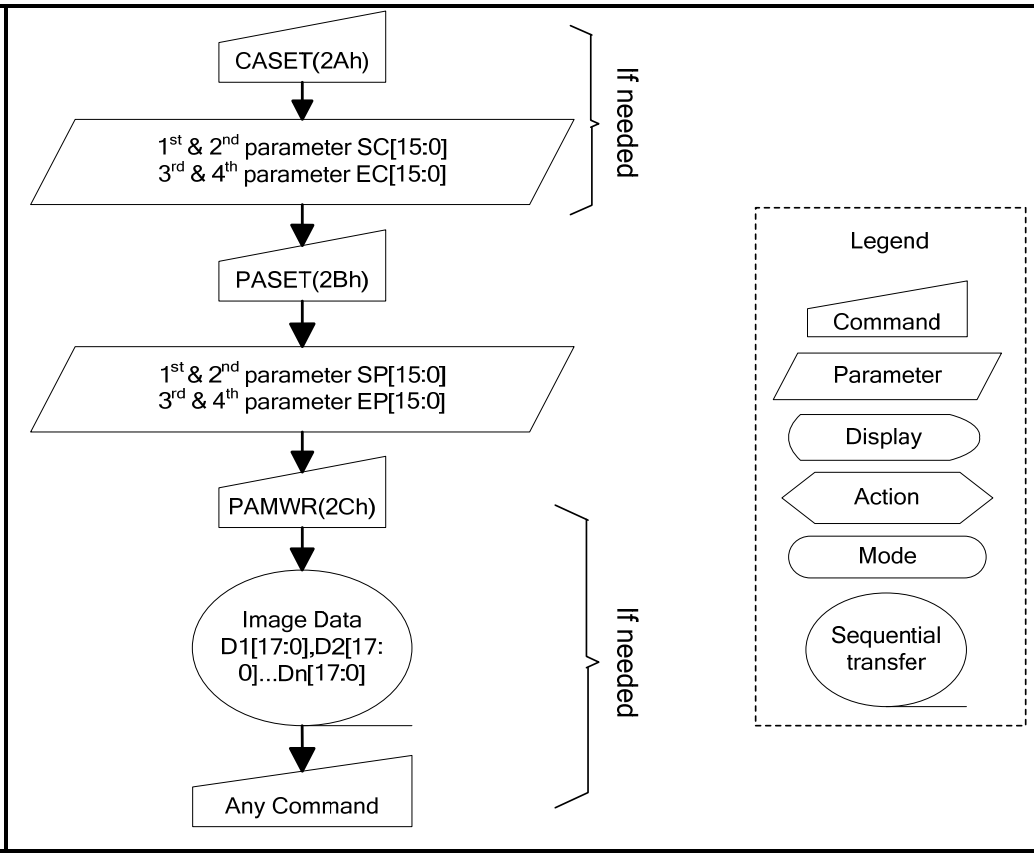
<table>
<tr><td>29h</td><td colspan="13">DISPON(Display On)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Display Off Mode. Output from the Frame Memory is enabled.
This command makes No Change of contents of frame memory.
This command does not change any other status.
(Example)
Memory Display
 
X=Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

9.2.1.19 Column Address Set (2Ah)

<table>
<tr><td>2Ah</td><td colspan="12">CASET(Column Address Set)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2Ah</td></tr>
<tr><td>1st parameter</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">SC[15:8]</td><td>00</td></tr>
<tr><td>2nd parameter</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">SC[7:0]</td><td>00</td></tr>
<tr><td>3rd parameter</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">EC[15:8]</td><td>00</td></tr>
<tr><td>4th parameter</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">EC[7:0]</td><td>ef</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes No Change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.
(Example)
 

X=Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">SC[15:0] always must be equal to or less than EC[15:0].
Note: When SC[15:0] or EC[15:0] is greater than 00Efh (When MADCTL’s B5 = 0) or 013Fh (When MADCTL’s B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SC[15:0]=0000h</td><td>EC[15:0]=00h</td></tr><tr><td>S/W Reset</td><td>SC[15:0]=0000h</td><td>If MADCTL’S B5=0:EC[15:0]=00Efh
If MADCTL’S B5=1:EC[15:0]=00Efh</td></tr><tr><td>H/W Reset</td><td>SC[15:0]=0000h</td><td>EC[15:0]=00Efh</td></tr></table></td></tr>
</table>

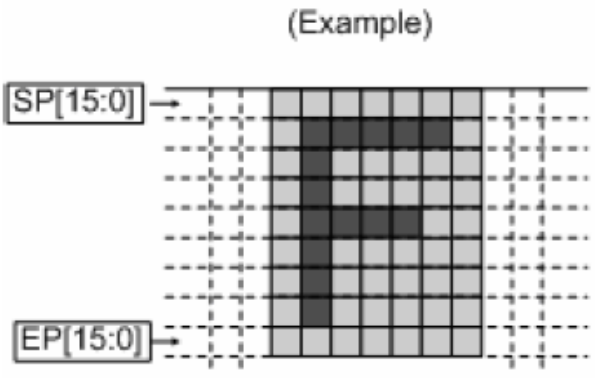
Flow Chart



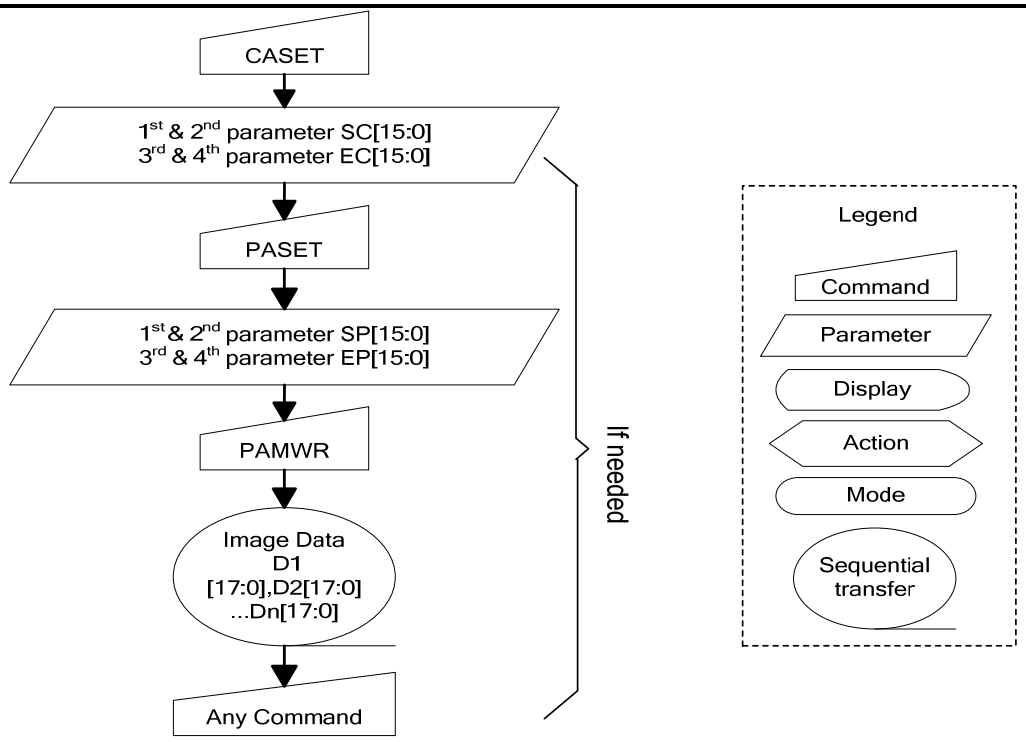
9.2.1.20 Page Address Set (2Bh)

2Bh	PASET(Page Address Set)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st parameter	0	1	↑	XX	SP[15:8]								00
2nd parameter	0	1	↑	XX	SP[7:0]								00
3rd parameter	0	1	↑	XX	EP[15:8]								01
4th parameter	0	1	↑	XX	EP[7:0]								3f

This command is used to define area of frame memory where MCU can access. This command makes No Change on the other driver status.The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

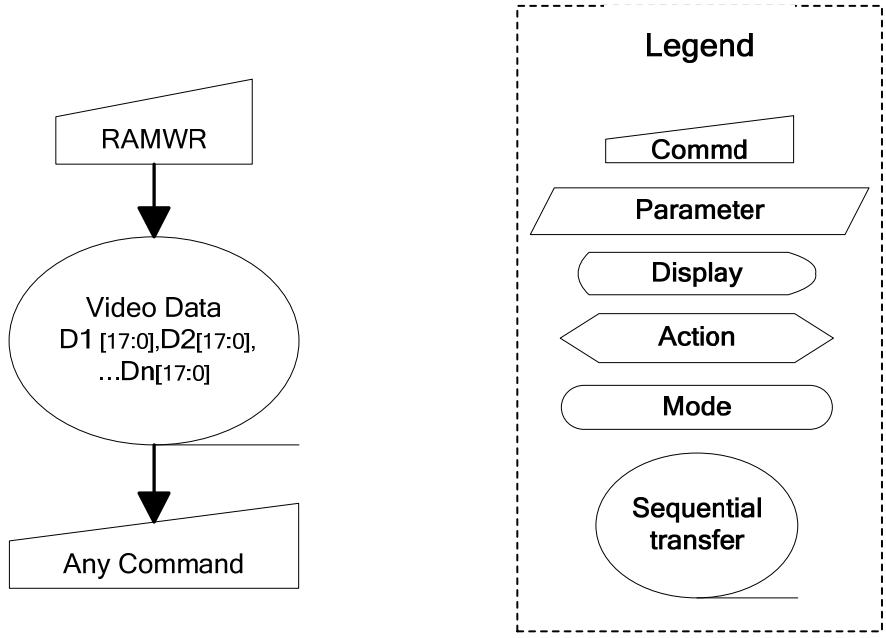


X=Don't care.

<table>
<tr><td>Restriction</td><td>SP[15:0] always must be equal to or less than EP[15:0].
Note : When SP[15:0] or EP[15:0] is greater than 00Efh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>SP[15:0]=0000h</td><td>EP[15:0]=013Fh</td></tr>
<tr><td>S/W Reset</td><td>SP[15:0]=0000h</td><td>If MADCTL'S B5=0:EP[15:0]=013Fh
If MADCTL'S B5=1:EP[15:0]=013Fh</td></tr>
<tr><td>H/W Reset</td><td>SP[15:0]=0000h</td><td>EP[15:0]=013Fh</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

9.2.1.21 Memory Write (2Ch)

2Ch	RAMWR(Memory Write)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2C
Parameter	NO PARAMETER												
Description	This command is used to transfer data from MCU to frame memory. This command makes No Change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page position.The Start Column/Start Page positions are different in accordance with MADCTL setting. (See Section 10.2.3) Then D[17:0] is stored in frame memory and the column register and the page register incremented as in Table "MADCTL conditions". Sending any other command can stop frame write. See section 10.1.5 "Display Module Data Color Coding" for color coding, when there is used 8(IM0 is low– D[7:0] are used and D[17:8] are not used) or 16(IM0 is high – D[17:0] are												

<table>
<tr><td></td><td>used) data lines for image data.
X=Don’t care.</td></tr>
<tr><td>Restriction</td><td>In all color modes, there is no restriction on length of parameters.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr>
<tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

9.2.1.22 Memory Read (2Eh)

2Eh	RAMRD(Memory Read)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
Parameter	NO PARAMETER												
Description	This command is used to transfer data from frame memory to MCU(See section 10.1.). This command makes No Change to the other driver status.When this command is accepted, the column register and the page register are reset to the Start Column/Start Page position.The Start Column/Start positions are different in accordance with MADCTL setting (see section 10.2.3). Then D[17:0] is read back from the frame memory and the column register and the page register incremented as in the Table “MADCTL conditions”. Frame Read can be stopped by sending any other command.See section **10**.1.5 “Display Module Data Color Coding” for color coding (18 bit cases), when there is used 8 or 6 data lines for image data. X = Don’t care.												
Restriction	In all color modes, the Frame Read is always 18bit so there is no restriction on length of parameters. *Note:* Memory Read is only possible via the Parallel Interface.												

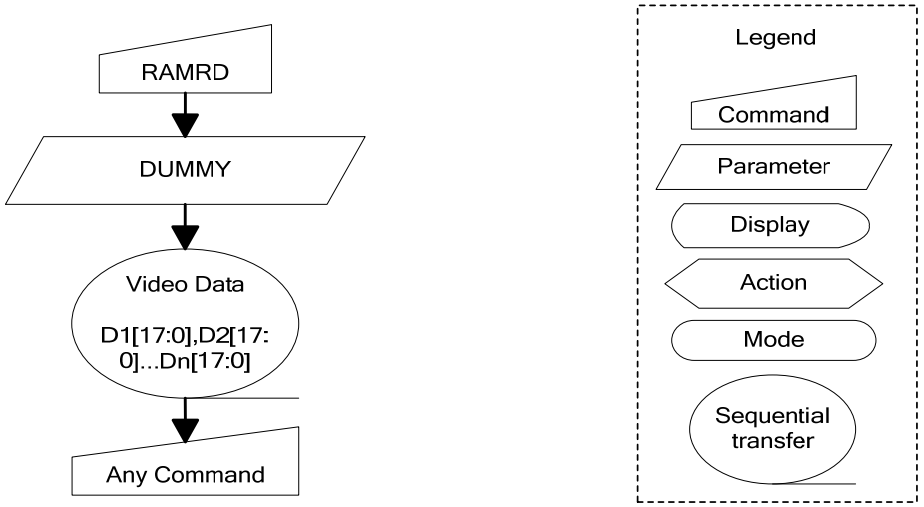
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

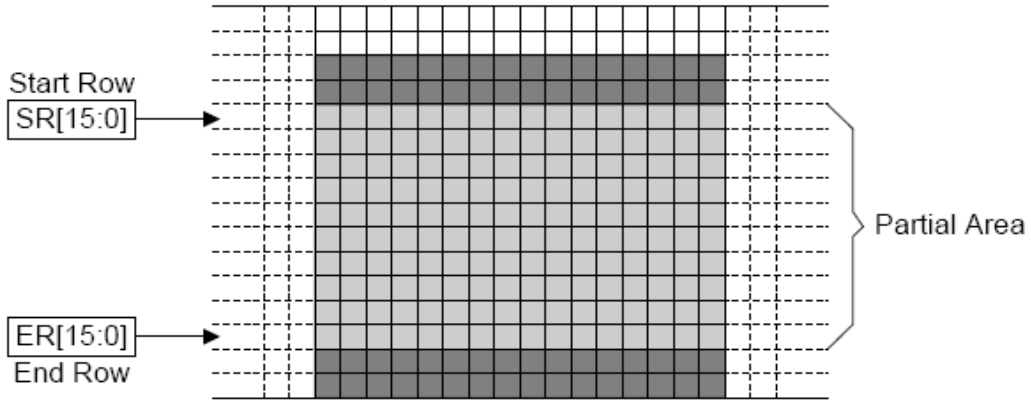
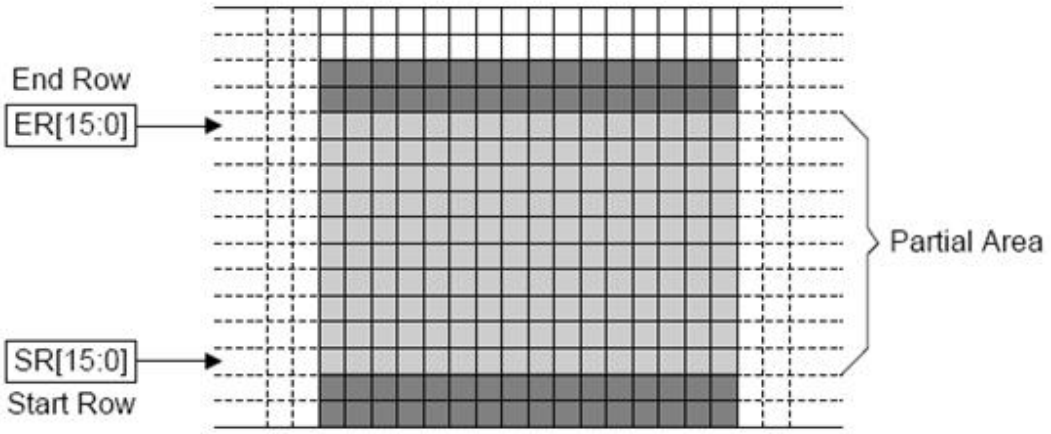
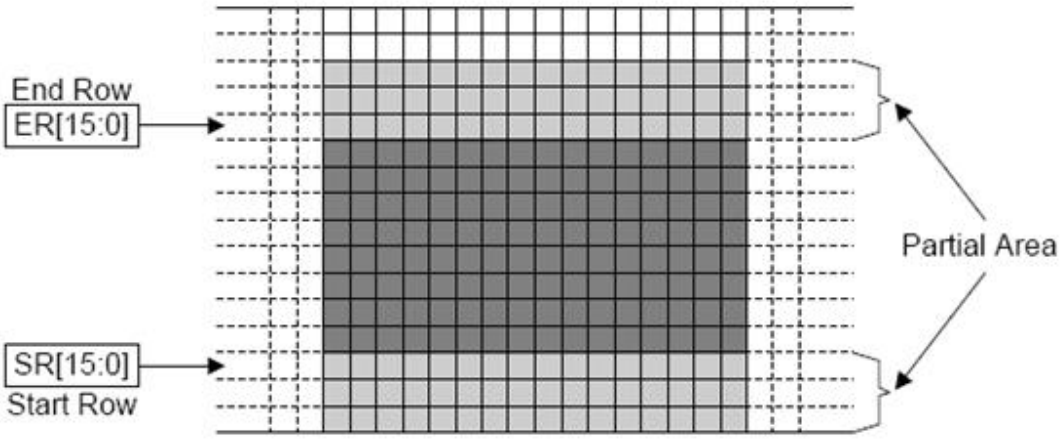
Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



9.2.1.23 Partial Area (30h)

30h	PLTAR(Partial Area)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30
1st parameter	1	1	↑	XX	SR[15:8]								00
2nd parameter	1	1	↑	XX	SR[7:0]								00
3rd parameter	1	1	↑	XX	ER[15:8]								01
4th parameter	1	1	↑	XX	ER[7:0]								3f

Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second defines the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. **If End Row > Start Row When MADCTL B4=0:**  **If End Row > Start Row when MADCTL B4=1:**  **If End Row < Start Row When Madctl B4=0:**  **If End Row=Start Row** then the Partial Area will be one row deep. X=Don't care.
Restriction	SR[15..0] and ER[15..0] cannot be 0000h nor exceed 013Fh.

Register Availability

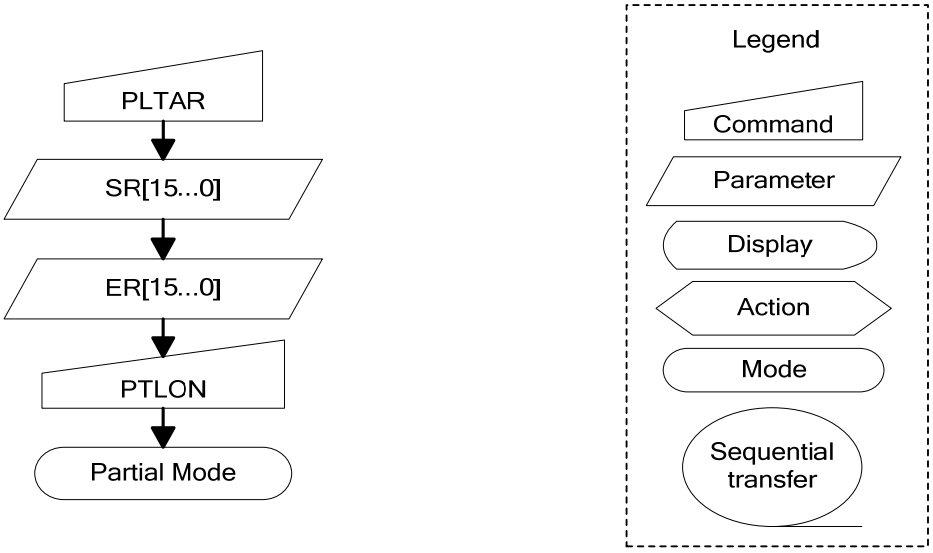
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

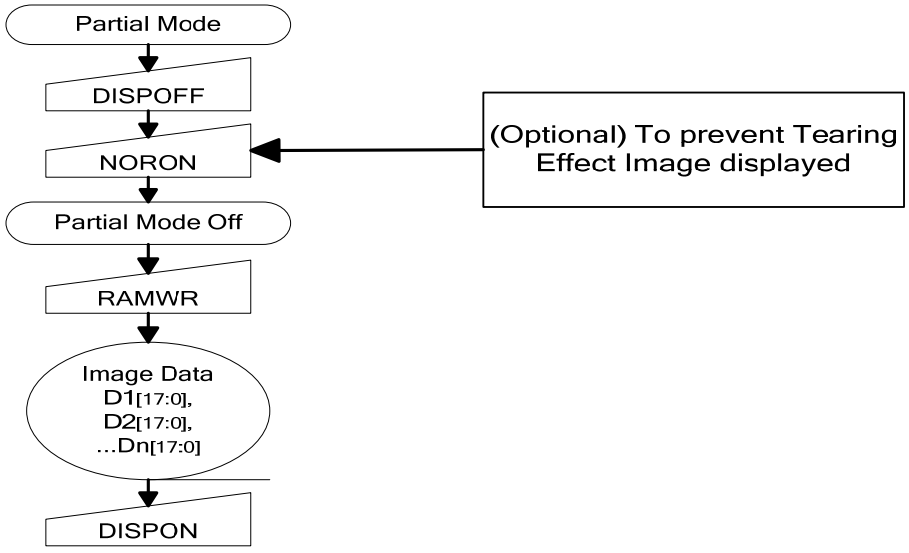
Status	Default Value	
Power On Sequence	SR[15:0]=0000h	ER[15:0]=013Fh
S/W Reset	SR[15:0]=0000h	ER[15:0]=013Fh
H/W Reset	SR[15:0]=0000h	ER[15:0]=013Fh

Flow Chart

0- **To enter Partial Mode:**



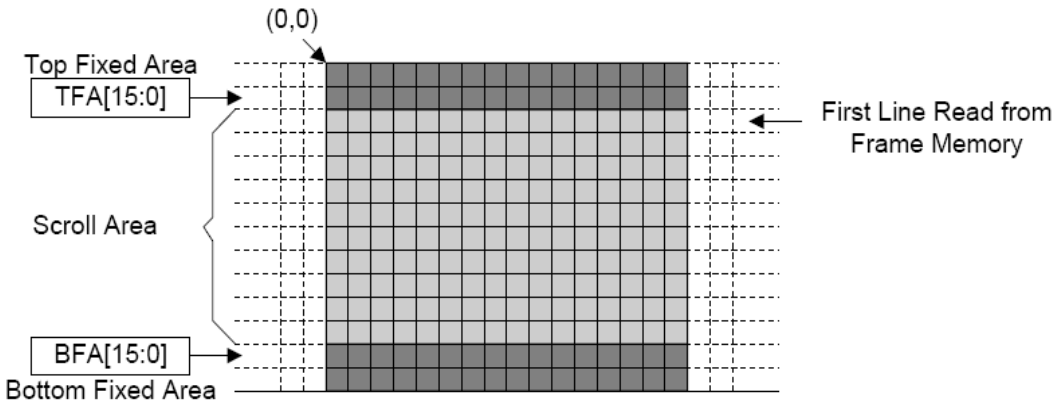
0- **To exit Partial Mode:**



9.2.1.24 Vertical Scrolling Definition (33h)

33h	VSCRDEF(Vertical Scrolling Definition)												
	DC	RD	WR	D 17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st parameter	1	1	↑	XX	TFA[15:8]								00
2nd parameter	1	1	↑	XX	TFA[7:0]								00
3rd parameter	1	1	↑	XX	VSA[15:8]								01
4th parameter	1	1	↑	XX	VSA[7:0]								40
5th parameter	1	1	↑	XX	BFA[15:8]								00
6th parameter	1	1	↑	XX	BFA[7:0]								00
	This command defines the Vertical Scrolling Area of the display. **When MADCTL B4 = 0** The 1st & 2nd parameter TFA[15…0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15…0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.The 5th and 6th parameter BFA[15…0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).TFA, VSA and BFA refer to the Frame Memory Line Pointer.												

Description

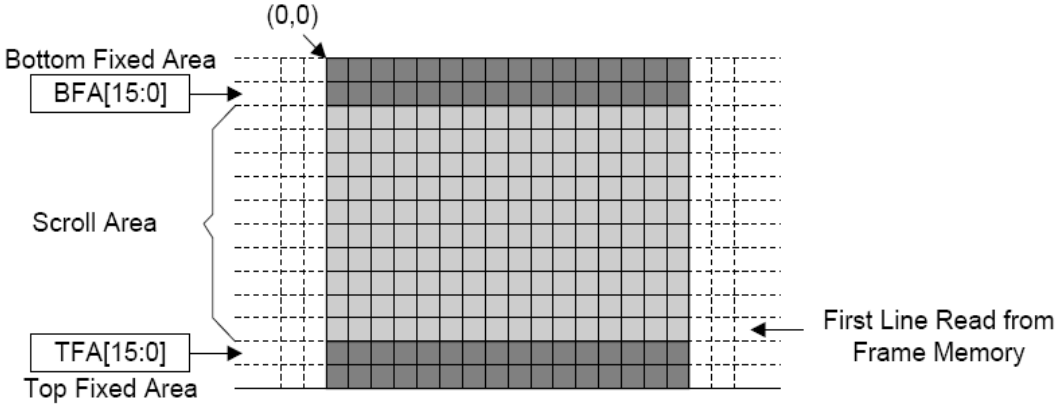


When MADCTL B4 = 1

The 1st & 2nd parameter TFA[15…0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA[15…0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA[15…0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



See also Section 10.2.2 for details of the Memory to Display mappings.

X=Don't care.

Restriction

The condition is TFA + VSA + BFA = 320, otherwise Scrolling mode is undefined..In Vertical Scroll Mode, MADCTL B5 should be set to '0, this only affects the Frame Memory Write.

Register Availability

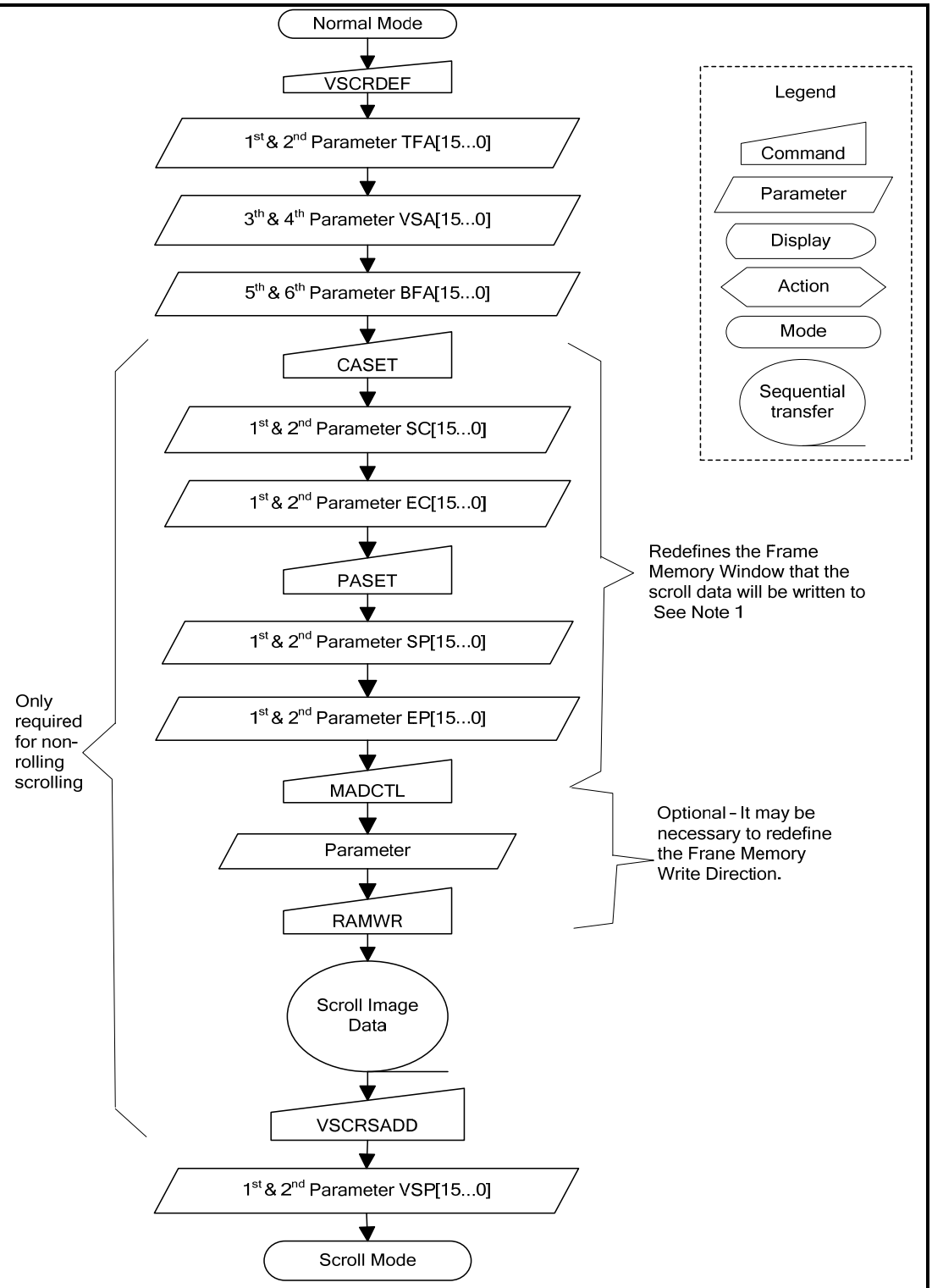
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=0140Fh	BFA[15:0]=0000Fh
S/W Reset	TFA[15:0]=0000h	VSA[15:0]=0140Fh	BFA[15:0]=0000Fh
H/W Reset	TFA[15:0]=0000h	VSA[15:0]=0140Fh	BFA[15:0]=0000Fh

Flow chart

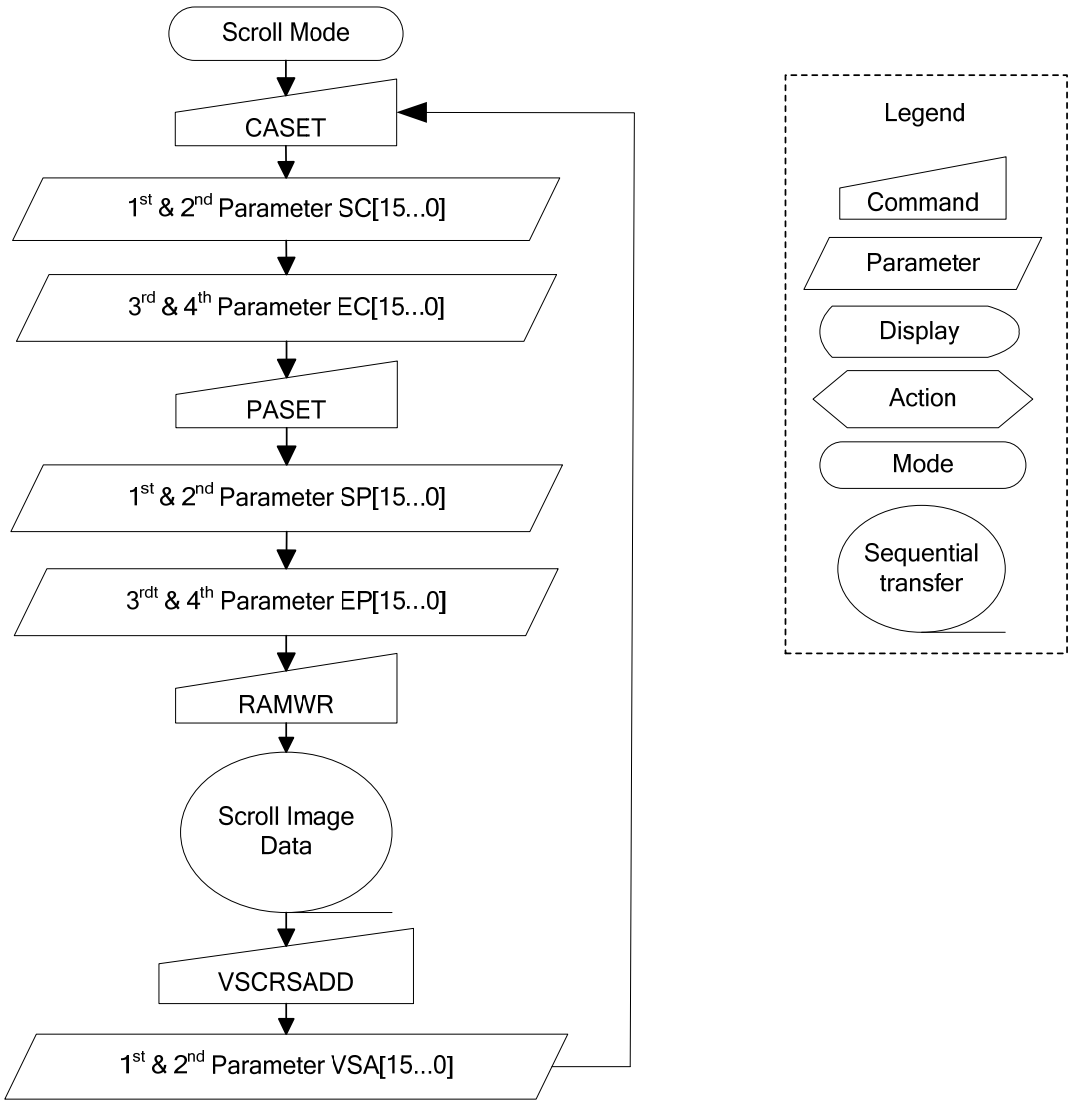
0- **To enter Scroll Mode:**



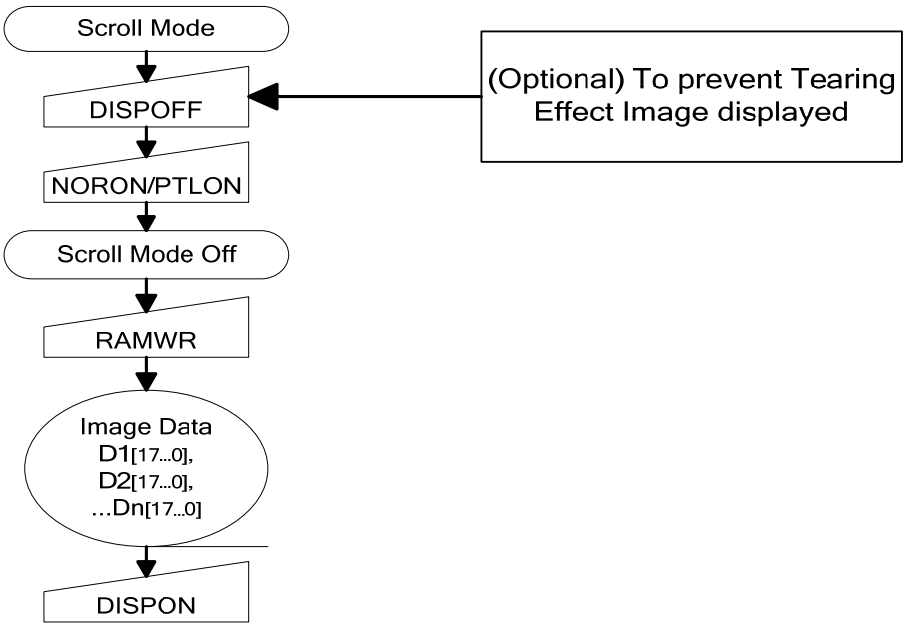
Note 1:

The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

0- **Continuous Scroll:**



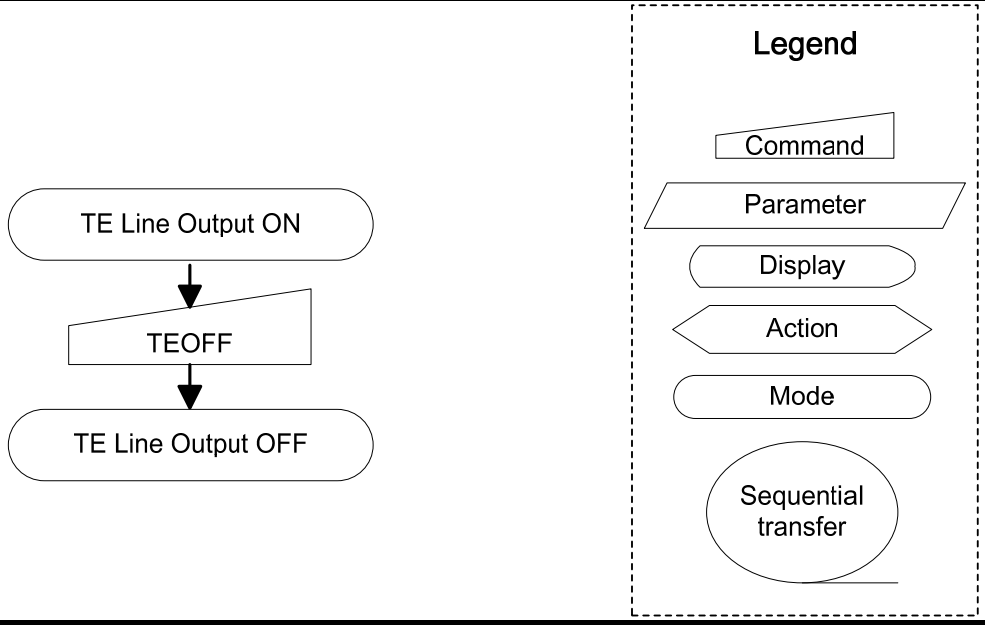
0- **To leave Vertical Scroll Mode:**



Note 2：

Scroll Mode can be left by both the Normal Display Mode ON(13h) and Partial Mode on(12h) commands.

9.2.1.25 Tearing Effect Line Off (34h)

<table>
<tr><td>34h</td><td colspan="13">TEOFF(Tearing Effect Line Off)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output ignal from the TE signal line.
X=Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output in already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

9.2.1.26 Tearing Effect Line ON (35h)

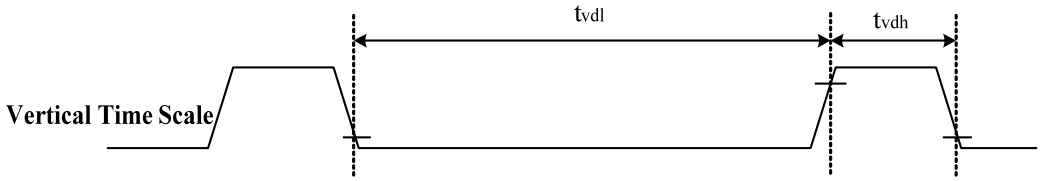
35h	TEON(Tearing Effect Line ON)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35
parameter	1	1	↑	XX	X	X	X	X	X	X	X	tear_en	00

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADTCTL bit B4. The Tearing Effect Line On has one parameter that describes the mode of the Tearing Effect Output Line.

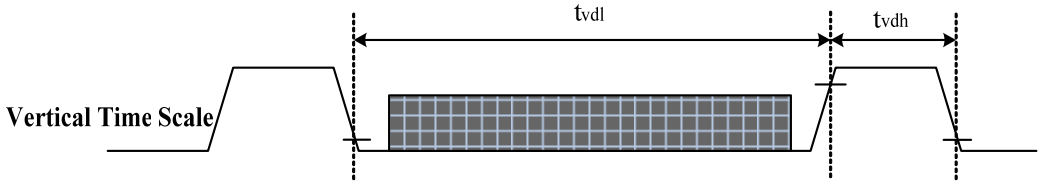
When tear_en =0:

The Tearing Effect Output line consists of V-blanking information only:



When tear_en =1:

The Tearing Effect Output line consists of V-blanking & H-blanking information:



Note:

During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X=Don't care.

Restriction

This command has no effect when Tearing Effect output in already On.

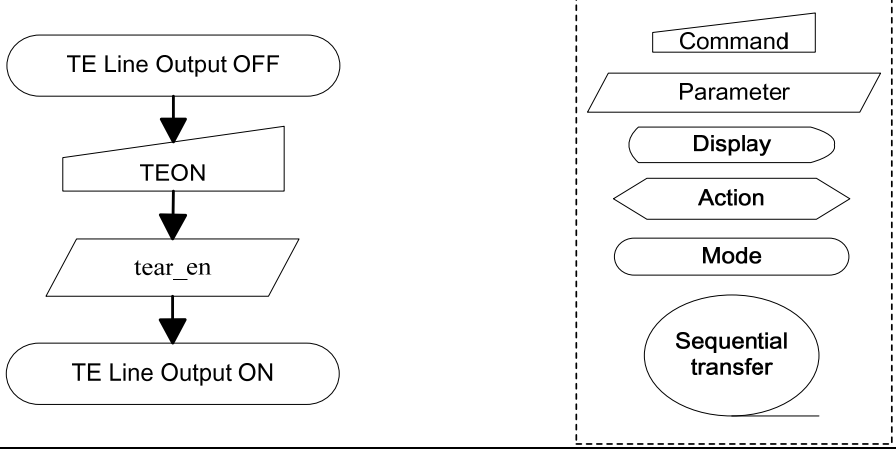
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



9.2.1.27 Memory Data Access Control (36h)

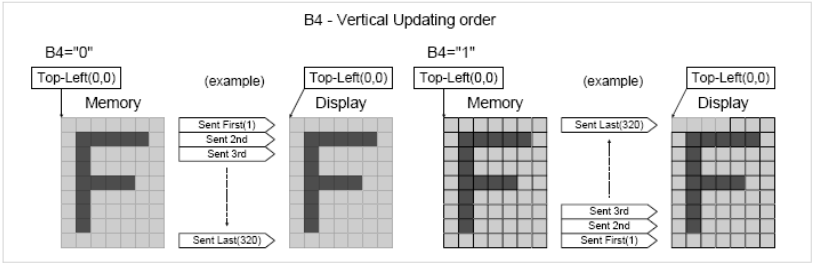
36h	MADCTL(Memory Data Access Control)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36
Parameter	1	1	↑	XX	my	mx	mv	ml	bgr	mh	X	X	00

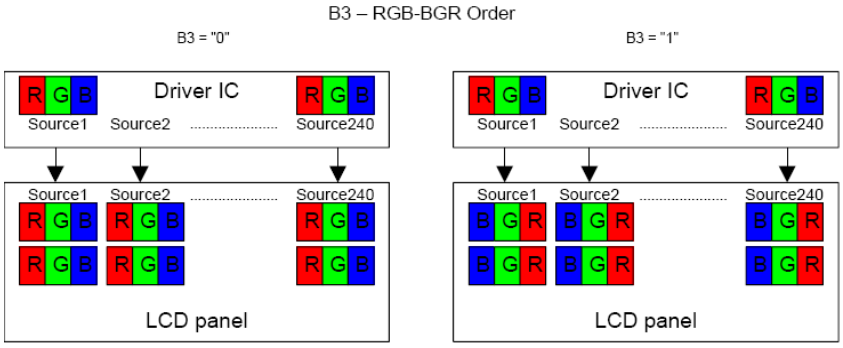
Description

This command defines read/write scanning direction of frame memory.

This command makes No Change on the other driver status.

Bit	Description	Value	Comment
my	Page Address Order	0	Top to Bottom (When MADCTL B7 = '0')
		1	Bottom to Top (When MADCTL B7 = '1')
mx	Column Address Order	0	Left to Right (When MADCTL B6 = '0')
		1	Right to Left (When MADCTL B6 = '1')
mv	Page/Column Address Order	0	Normal Mode (When MADCTL B5 = '0')
		1	Reverse Mode (When MADCTL B5 = '1')
ml	Line Address Order	0	LCD Refresh Top to Bottom (When MADCTL B4 = '0')
		1	LCD Refresh Bottom to Top (When MADCTL B4 = '1')
bgr	RGB / BGR Order	0	RGB (When MADCTL B3 = '0')
		1	BGR (When MADCTL B3= '1')
mh	LCD Horizontal refresh direction control	0	Horizontal refresh order(MH)
others	-	0	Set to '0'





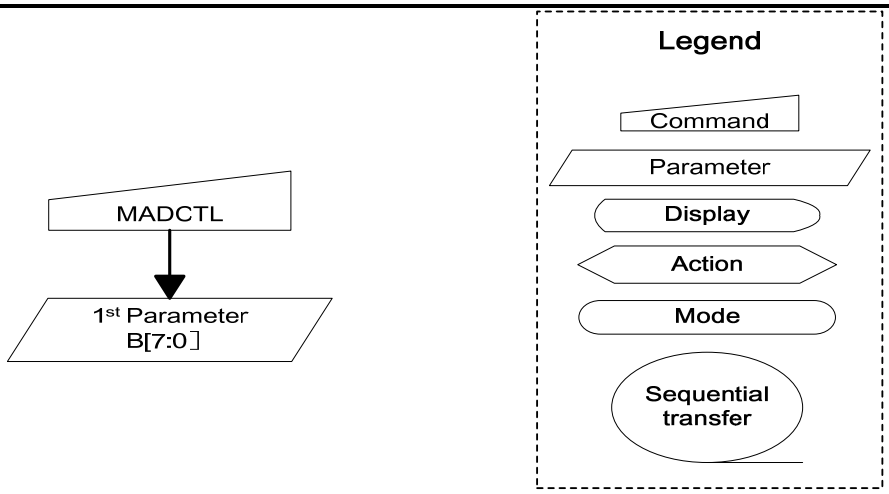
Note: Top- Left(0,0)means a physical memory location.

X = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	Status / Default Value Power On Sequence: 00h S/W Reset: No Change H/W Reset: 00h
Flow Chart	

9.2.1.28 Vertical Scrolling Start Address (37h)

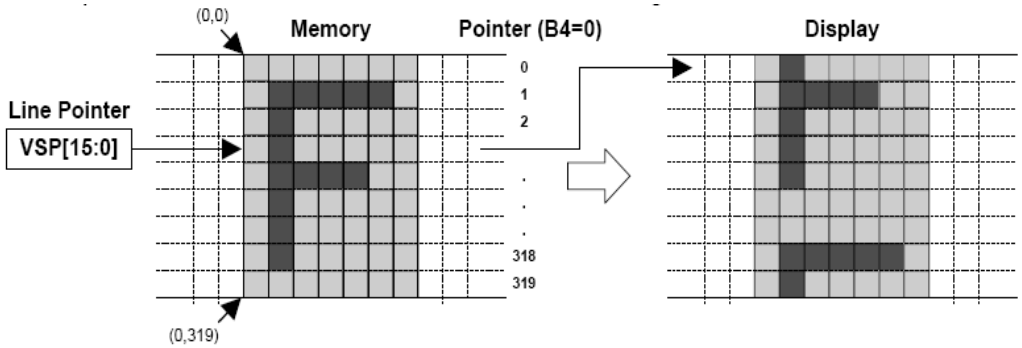
37h	VSCRSADD(Vertical Scrolling Start Address)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	XX	VSP[15:8]								00
2nd parameter	1	1	↑	XX	VSP[7:0]								00

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below.

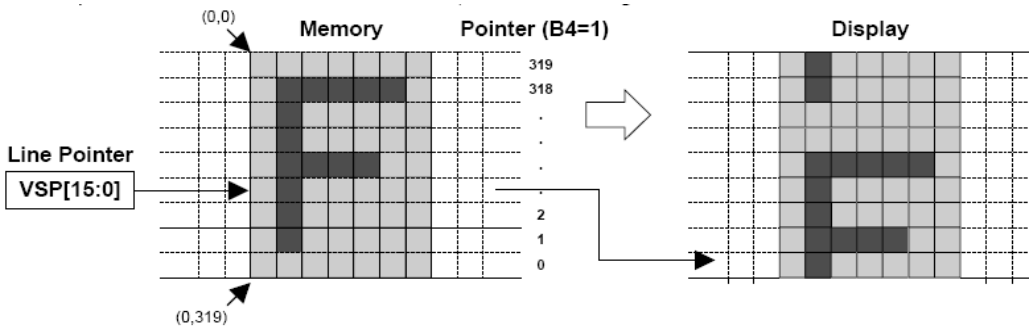
When MADCTL B4 = 0

Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP= '3'.



When MADCTL B4=1

Example:
When Top Fixed Area=Bottom Fixed Area=00,Vertical Scrolling Area=320and VSP='3'.



Notes:

1. When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
2. VSP refers to the Vertical Scrolling Start Address.

X = Don't care.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition 33h) – otherwise undesirable image will be displayed on the Panel.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	16'h0000
S/W Reset	16'h0000
H/W Reset	16'h0000

Flow Chart

See Vertical Scrolling Definition (33h) description.

9.2.1.29 Idle Mode Off (38h)

38h	IDMOFF(Idle Mode Off)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38
parameter	NO PARAMETER												
Description	This command is used to recover from idle mode on. In the idle off mode, LCD can display maximum 262,144 colors. See also section 10.5.2. X = Don't care.												
Restriction	This command has no effect when module is already in idle off mode.												

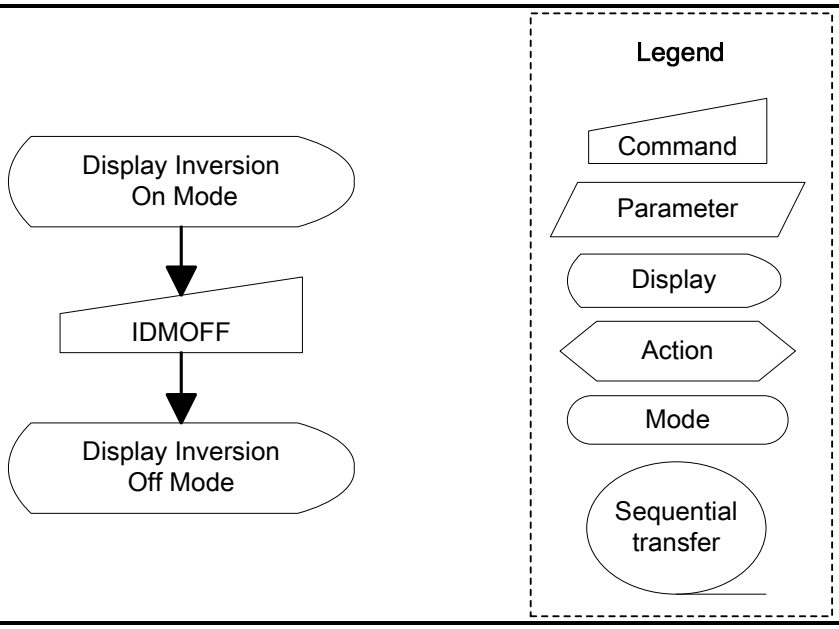
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	In idle off
S/W Reset	In idle off
H/W Reset	In idle off

Flow Chart



9.2.1.30 Idle Mode On (39h)

39h	IDMON(Idle Mode On)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39
parameter	NO PARAMETER												

Description

This command is used to enter into idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
See also section 10.5.2.

Memory contents vs Display Color			
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	0 X X X X X	0 X X X X X	0 X X X X X
Blue	0 X X X X X	0 X X X X X	1 X X X X X
Red	1 X X X X X	0 X X X X X	0 X X X X X
Magenta	1 X X X X X	0 X X X X X	1 X X X X X
Green	0 X X X X X	1 X X X X X	0 X X X X X
Cyan	0 X X X X X	1 X X X X X	1 X X X X X
Yellow	1 X X X X X	1 X X X X X	0 X X X X X
White	1 X X X X X	1 X X X X X	1 X X X X X

X = Don't care.

Restriction

This command has no effect when module is already in idle on mode.

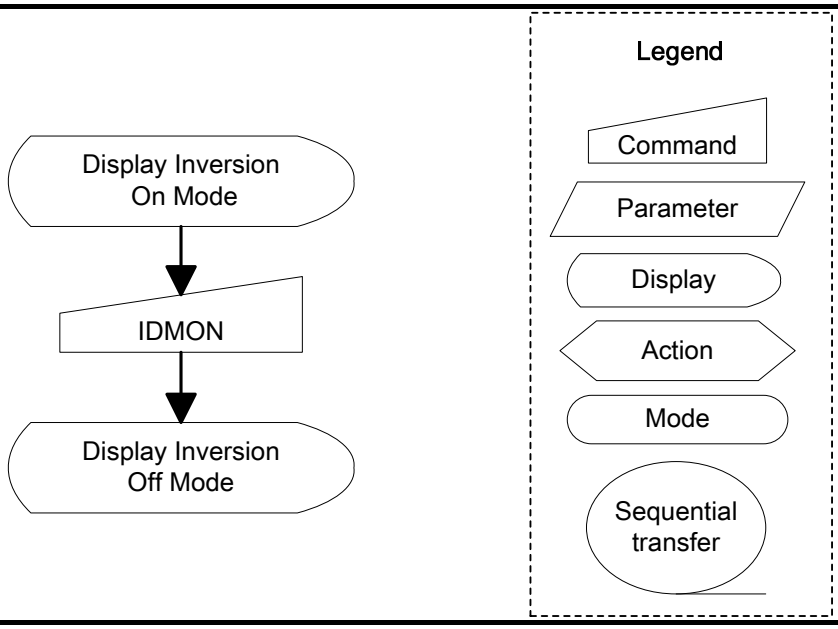
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle off Mode
S/W Reset	Idle off Mode
H/W Reset	Idle off Mode

Flow Chart



9.2.1.31 Interface Pixel Format (3Ah)

3Ah	PIXSET(Interface Pixel Format)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3A
Parameter	1	1	↑	XX	X	dpi[2:0]			X	dbi[2:0]			66

Description

dpi[2:0] is the pixel format select of RGB interface.
Dbi[2:1] is the pixel format of MCU interface.
If using RGB interface, serial interface must be selected.

Dpi[2:0]			RGB interface format	dbi[2:1]			MCU interfaceformat
0	0	0	reserved	0	0	0	reserved
0	0	1	reserved	0	0	1	reserved
0	1	0	reserved	0	1	0	reserved
0	1	1	reserved	0	1	1	reserved
1	0	0	reserved	1	0	0	reserved
1	0	1	16 bits/pixel	1	0	1	16 bits/pixel
1	1	0	18 bits/pixel	1	1	0	18 bits/pixel
1	1	1	reserved	1	1	1	reserved

X = Don't care.

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

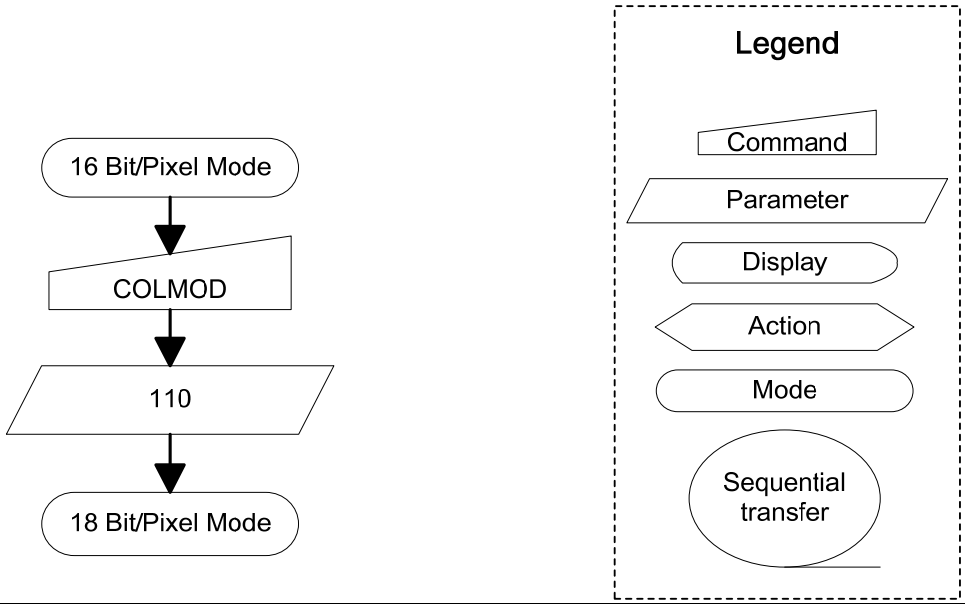
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
S/W Reset	No Change
H/W Reset	66h

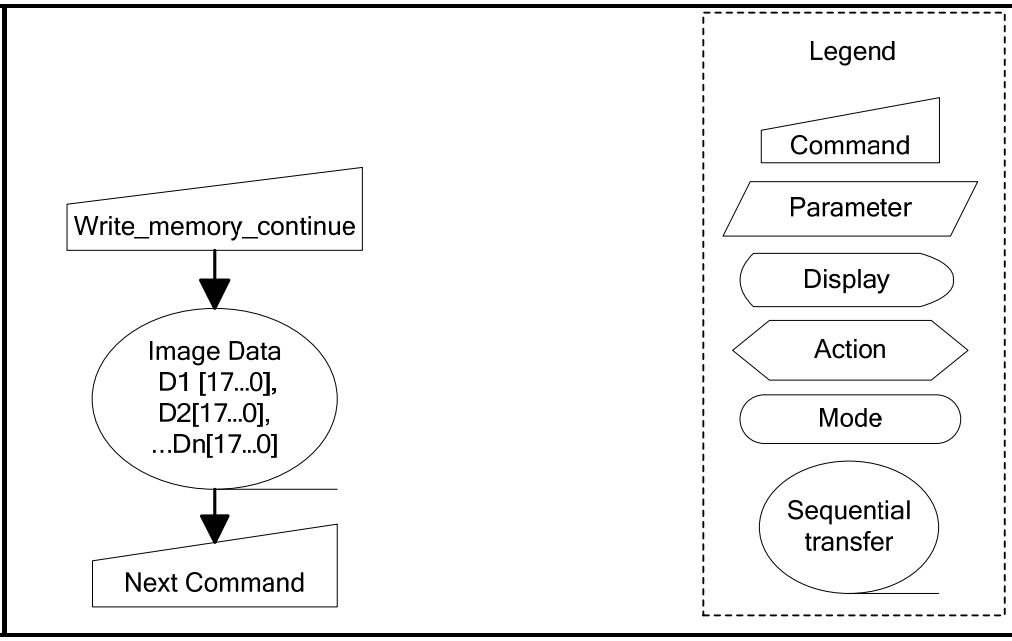
Flow Chart

Example:



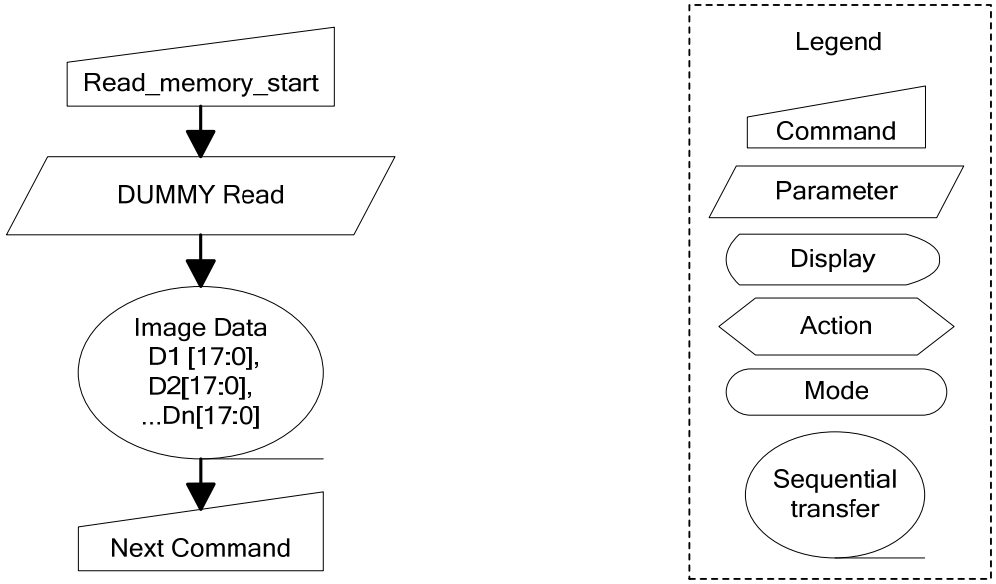
9.2.1.32 Write_Memory_Continue（3Ch）

<table>
<tr><td>3Ch</td><td colspan="12">Write_Memory_Continue</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>3C</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>D[17..8]</td><td colspan="8">D[7:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="12">This command transfers image data from the host processor to the display module’s frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.
If set_address_mode B5 = 0:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.
If set_address_mode B5 = 1:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command.
If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.
Sending any other command can stop frame Write.
Frame Memory Access and Interface setting (B3h), WEMODE=0
When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.
Frame Memory Access and Interface setting (B3h), WEMODE=1
When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12">A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Random data</td></tr><tr><td>S/W Reset</td><td>No change</td></tr><tr><td>H/W Reset</td><td>No change</td></tr></table></td></tr>
</table>

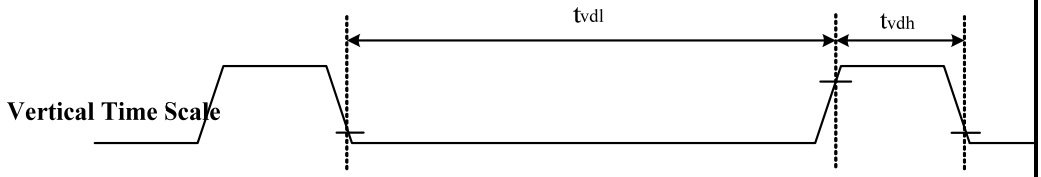
Flow Chart	

9.2.1.33 Read_Memory_Continue（3Eh）

3Eh	Read_Memory_Continue												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3E
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2st Parameter	1	↑	1	Dx [17..8]	D1[7:0]								000 3FF
Xth Parameter	1	↑	1	Dx [17..8]	Dx[7:0]								000 3FF
Nth parameter	1	↑	1	Dn [17..8]	Dn[7:0]								000 3FF
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command. **If set_address_mode B5 = 0:** Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. **If set_address_mode B5 = 1:** Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command. This command makes no change to the other driver status. X = Don't care.												

Restriction	A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: Random data S/W Reset: No change H/W Reset: No change
Flow Chart	

9.2.1.34 Set_Tear_Scanline（44h）

44h	Set Tear Scanline												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	STS [8]	00
2th Parameter	1	1	↑	XX	STS[7:0]								00
Description	This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.  *Note:* That set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0.The Tearing Effect Output line shall be active low when the display module is in Sleep mode. X = Don't care.												

Restriction	
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: STS [8:0]=0000h S/W Reset: STS [8:0]=0000h H/W Reset: STS [8:0]=0000h
Flow Chart	

9.2.1.35 Get_Scanline（45h）

45h	Get_Scanline												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	1	↑	XX	X	X	X	X	X	X	GTS[9:8]		00
3rd Parameter	1	1	↑	XX	GTS[7:0]								00
Description	The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined. X = Don't care.												
Restriction	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes												
Default	Status / Default Value Power On Sequence: 16'h0000 S/W Reset: 16'h0000 H/W Reset: 16'h0000												
Flow Chart													

9.2.1.36 Read IDD3 (D3h)

D3h	Read IDD3												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2th Parameter	1	↑	1	XX	idd3[23:16]								00
3rd Parameter	1	↑	1	XX	idd3[15:8]								30
4th Parameter	1	↑	1	XX	idd3[7:0]								33
Description	This read byte returns 24-bits display identification information. The 1st Parameter is dummy read. The 2nd Parameter identifies the LCD module's manufacture. The 3rd Parameter identifies the LCD module/driver version ID. The 4th Parameter identifies the LCD module/driver ID. X = Don't care.												
Restriction	EXTC should be high to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h003031
S/W Reset	24'h003031
H/W Reset	24'h003031

9.2.1.37 Read ID1 (DAh)

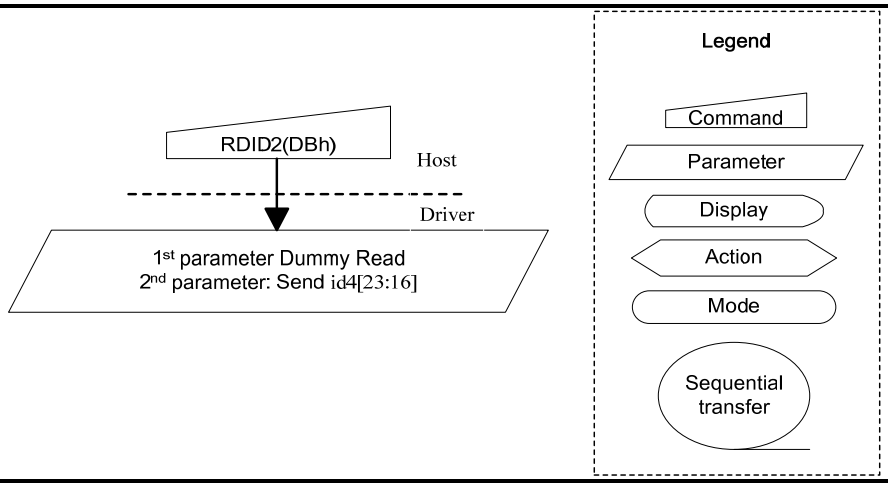
Dah	RDID1(Read ID1)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DA
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2th Parameter	1	↑	1	XX	id4[23:16]								00
Description	The 1st Parameter is dummy read. The 2nd Parameter identifies the LCD module's manufacture. X = Don't care.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart	

9.2.1.38 Read ID2 (DBh)

DBh	RDID2(Read ID2)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D1	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DB
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	id4[15:8]								30
Description	The 1st Parameter is dummy read. The 2nd Parameter identifies the LCD module/driver version ID. X = Don't care.												
Restriction													

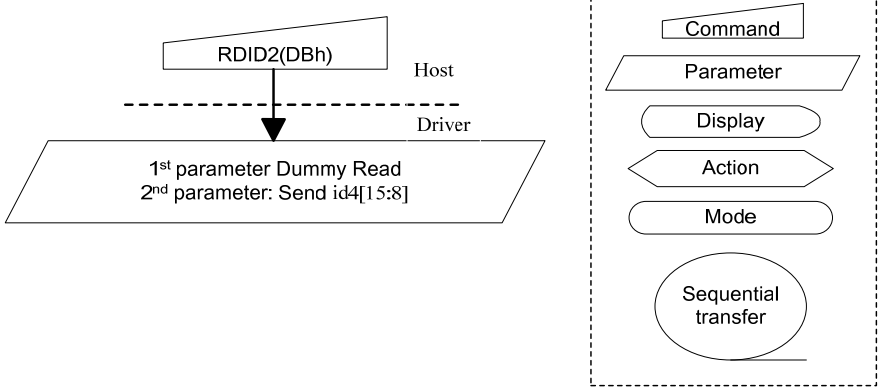
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	30h
S/W Reset	30h
H/W Reset	30h

Flow Chart



9.2.1.39 Read ID3 (DCh)

DCh	RDID3(Read ID3)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D1	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DC
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	id4[7:0]								33
Description	The 1st Parameter is dummy read. The 2nd Parameter identifies the LCD module/driver ID. X = Don't care.												
Restriction													

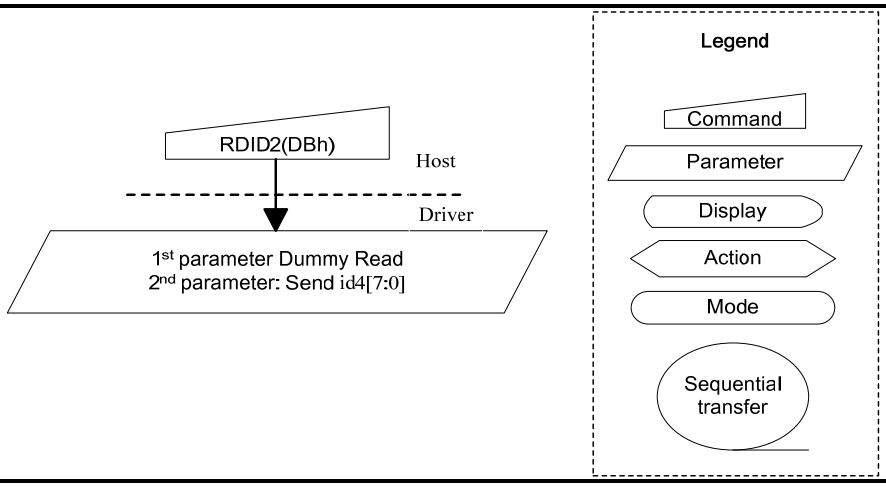
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	31h
S/W Reset	31h
H/W Reset	31h

Flow Chart



9.2.2 Description of level2 command (extended command)

（Set FDH register when accessing Extended commands）

9.2.2.1 RGB interface control (B0h)

<table>
<tr><td>B0h</td><td colspan="12">IFMODE(interface mode control)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>Bypass_mode</td><td colspan="2">Rcm[1:0]</td><td>X</td><td>vspl</td><td>hspl</td><td>dpl</td><td>epl</td><td>40</td></tr>
<tr><td>Description</td><td colspan="13">Set the operation status of display interface. The setting becomes effective as soon as the command is seted.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">bypass_mode</td><td rowspan="2">Select the display data bypass</td><td>0</td><td>through memory</td></tr>
<tr><td>1</td><td>direct to shift register</td></tr>
<tr><td rowspan="2">rcm[1:0]</td><td rowspan="2">RGB interface selection</td><td>0</td><td>Left to Right (When MADCTL B6=’0’)</td></tr>
<tr><td>1</td><td>Right to Left (when MADCTL B6=’1’</td></tr>
<tr><td rowspan="2">vspl</td><td rowspan="2">VSYNC polarity</td><td>0</td><td>Low level sync clock</td></tr>
<tr><td>1</td><td>High level sync clock</td></tr>
<tr><td rowspan="2">hspl</td><td rowspan="2">HSYNC polarity</td><td>0</td><td>Low level sync clock</td></tr>
<tr><td>1</td><td>High level sync clock</td></tr>
<tr><td rowspan="2">dpl</td><td rowspan="2">Dotclock polarity</td><td>0</td><td>data fetched at the rising time</td></tr>
<tr><td>1</td><td>data fetched at the falling time</td></tr>
<tr><td rowspan="2">epl</td><td rowspan="2">DE polarity</td><td>0</td><td>High enable for RGB interface</td></tr>
<tr><td>1</td><td>Low enable for RGB interface</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>40h</td></tr>
<tr><td>S/W Reset</td><td>40h</td></tr>
<tr><td>H/W Reset</td><td>40h</td></tr>
</table></td></tr>
</table>

9.2.2.2 Frame rate control 1(B1h)

<table>
<tr><td>B1h</td><td colspan="13">FRMCTR1 (Frame rate control)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>B1</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">divi[1:0]</td><td>00</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td colspan="5">rtni[4:0]</td><td>17</td></tr>
<tr><td>Description</td><td colspan="13">
RTNI[4:0]: Sets 1H (line) period when synchronizing NV3029G-01’s display operation with internal clock signal.
<table>
<tr><th>RTNI[4:0]</th><th>Clock per line</th><th>RTNI[4:0]</th><th>Clock per line</th></tr>
<tr><td>5’h10</td><td>-</td><td>5’h18</td><td>24 clocks</td></tr>
<tr><td>5’h11</td><td>17 clocks</td><td>5’h19</td><td>25 clocks</td></tr>
<tr><td>5’h12</td><td>18 clocks</td><td>5’h1A</td><td>26 clocks</td></tr>
<tr><td>5’h13</td><td>19 clocks</td><td>5’h1B</td><td>27 clocks</td></tr>
<tr><td>5’h14</td><td>20 clocks</td><td>5’h1C</td><td>28 clocks</td></tr>
<tr><td>5’h15</td><td>21 clocks</td><td>5’h1D</td><td>29 clocks</td></tr>
<tr><td>5’h16</td><td>22 clocks</td><td>5’h1E</td><td>30 clocks</td></tr>
<tr><td>5’h17</td><td>23 clocks</td><td>5’h1F</td><td>31 clocks</td></tr>
</table>
clocks per line (internal clock operation: 1 clock = 1 OSC)
DIVI[1:0]: set the division ratio of the internal oscillation clock, when NV3029G-01’s display operation is synchronized with internal oscillation clock. NV3029G-01’s internal operation is synchronized with the frequency divided internal oscillation clock. When changing the DIVI[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed. The frame frequency can be adjusted by setting RTNI[4:0] and DIVI[1:0].
<table>
<tr><th>DIVI[1:0]</th><th>Division Ratio</th><th>Internal Operation Clock Unit</th></tr>
<tr><td>2’h0</td><td>1/1 fosc</td><td>One OSC clock</td></tr>
<tr><td>2’h1</td><td>1/2 fosc</td><td>2 OSC clock</td></tr>
<tr><td>2’h2</td><td>1/4 fosc</td><td>4 OSC clock</td></tr>
<tr><td>2’h3</td><td>1/8 fosc</td><td>8 OSC clock</td></tr>
</table>
OSC: internal oscillation clock
Division ratio of the internal operation clock frequency
The frame frequency can be adjusted setting (RTNI and DIVI bits), When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see” Frame-Frequency Adjustment Function”. The setting in DIVI[1:0] is disabled in RGB interface operation.
Frame Frequency Calculation
$$\text{Frame frequency} = \frac{fosc}{\text{Clocks per line x division ratio x (line + BP + FP)}} \quad [Hz]$$
fosc : RC oscillation frequency
Line: Number of lines to drive the LCD (NL bits)
Division ratio: DIVI
Clocks per line: RTNI

Internal Clock Frequency (fosc) is determined by register (66h, D4-D0).
<table>
<tr><th>66h, D4-D0</th><th>Internal Clock frequency(KHz)</th></tr>
<tr><td>08h</td><td>460</td></tr>
<tr><td>10h</td><td>575</td></tr>
</table>
Note:
Register 66h, D4-D0 default value is 10h. In this setting, The Frame Rate is about 77Hz; If 66h, D4-D0 setting is 08h, The Frame Rate is about 62Hz.
X = Don’t care.
</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
</table>

Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: 16'h0017 S/W Reset: 16'h0017 H/W Reset: 16'h0017

9.2.2.3 Frame rate control 2(B2h)

B2h	FRMCTR2(Frame rate control 2)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2
Parameter	1	1	↑	XX	X	X	X	X	X	X	dive[1:0]		00

Description

DIVE[1:0]: DIVE[1:0] sets the division ratio of DOTCLK, when the NV3029G-01 performs display operation via RGB interface. The NV3029G-01's internal operation is synchronized with the frequency divided DOTCLK in RGB interface operation.

DIVE[1:0]	Division Ratio	18-bit,1transfer RGB interface	DOTCLK=5 MHZ	8-bit,3 transfer RGB interface	DOTCLK=5M HZ
2'h0	Setting disabled	Setting disabled	-	Setting disabled	-
2'h1	1/4	4DOTCLKS	0.8us	12DOTCLKS	0.8us
2'h2	1/8	8DOTCLKS	1.6uS	24DOTCLKS	1.6us
2'h3	1/161	16DOTCLKS	3.2uS	48DOTCLKS	3.2us

Note: Internal operation clock unit: DOTCLK.

X = Don't care.

Restriction	This command has no effect when module is already in idle off mode.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: 00h S/W Reset: 00h H/W Reset: 00h

9.2.2.4 Display inversion (B4h)

B4h	INVTR(Display inversion control)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4
parameter	1	1	↑	XX	X	X	X	X	X	nla	nlb	nlc	02
Description	Display inversion mode set. Nla: inversion setting in normal mode; nlb: inversion setting in idle mode; nlc: inversion setting in partial mode. 0: line inversion; 1: frame inversion. X = Don't care.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

9.2.2.5 Blanking porch control(B5h)

B5h	PRCTR(Blanking porch)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5
1st parameter	1	1	↑	XX	X	vfp[6:0]							02
2nd parameter	1	1	↑	XX	X	vbp[6:0]							02
3rd parameter	1	1	↑	XX	X	X	X	hfp[4:0]					0a
4th parameter	1	1	↑	XX	X	X	X	hbp[4:0]					14
Description	Vfp[6:0]/vbp[6:0]: vfp[6:0] and vbp[6:0] set the line number vertical front and back porch period respectively.												

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

hfp[6:0]/hbp[6:0]: hfp[6:0] and hbp[6:0] set the line number horizontal front and back porch period respectively.

HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back porch	HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch
00000	Setting prohibited	10000	16
00001	Setting prohibited	10001	17
00010	2	10010	18
00011	3	10011	19
00100	4	10100	20
00101	5	10101	21
00110	6	10110	22
00111	7	10111	23
01000	8	11000	24
01001	9	11001	25
01010	10	11010	26
01011	11	11011	27
01100	12	11100	28
01101	13	11101	29
01110	14	11110	30
01111	15	11111	31

X = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	Vfp[6:0]	Vbp[6:0]	Hfp[4:0]	Hbp[4:0]
Power On Sequence	7'h02	7'h02	5'h0a	5'h14
S/W Reset	7'h02	7'h02	5'h0a	5'h14
H/W Reset	7'h02	7'h02	5'h0a	5'h14

9.2.2.6 Display function control (B6h)

B6h	DISCTRL(Display function control)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6
1st parameter	1	1	↑	XX	X	X	X	X	ptg[1:0]		pts[1:0]		0A
2nd parameter	1	1	↑	XX	rev	gs	ss	sm	isc[3:0]				82
3rd parameter	1	1	↑	XX	X	X	nl[5:0]						27

Description

Ptg[1:0]: set the scan mode in non-display area.

Ptg[1:0]		Gate outputs in non-display area	Source output in non-display area	VCOM output
0	0	Normal scan	Set with the PT[2:0] bits	VCOMH/VCOML
0	1	Setting prohibited	…	…
1	0	Interval scan	Set with the PT[2:0] bits	
1	1	Setting prohibited	…	…

Pts[1:0]: determine source and Vcom output in non-display area in the partial display mode.

Pts[1:0]		Source output in non-display area		Vcom output in non-display area	
		Positive polarity	Negative polarity	Positive polarity	Negative polarity
0	0	V63	V0	Vcoml	Vcomh
0	1	V0	V63	Vcoml	Vcomh
1	0	Vssa	Vssa	Vsa	Vssa
1	1	Hi-z	Hi-z	Vssa	Vssa

ss: selects the shift direction of outputs of the source driver.
0: Source output S1- S720;
1: Source output S720 – S1.

GS: Sets the direction of scan by the gate driver in the range determined by SCN[5:0] and NL[5:0].
When GS = 0, the scan direction is from G1 to G320.
When GS = 1, the scan direction is from G320 to G1

Rev: select the liquid crystal type is the white type or the normal black type.
0: normal black;
1: normal white.

ISC[3:0]: Specify the scan cycle of the gate driver when the PTG[1:0] are set to "10" in non-display area. The scan cycle can be set in odd number of frames from 0 to 31. In this case, polarity is inverted every scan cycle.

ISC	Scan cycle	(Fflm)=60HZ
0000	0 frame	-
0001	3 frame	50ms
0010	5 frame	84ms
0011	7 frame	117ms
0100	9 frame	150ms
0101	11 frame	184ms
0110	13frame	217ms
0111	15frame	251ms
1000	17frame	284ms
1001	19frame	317ms
1010	21frame	351ms
1011	23 frame	384ms
1100	25frame	418ms
1101	27frame	451ms
1110	29 frame	484ms

1111	31frame	518ms

Sm: scan mode selection.
When NL = 6'1d, SCN = 6'h02, the gate scan sequence shows below:

	GS = 0	GS = 1
SM = 0	G17,18…255,256	G304,303…66,65
SM = 1	G18,17….256,255	G303,304…65,66
SM = 2	G33,35…317,319,2,4…190,192	G288,286…4,2,319,317…131,129
SM = 3	G35,33…319,317,4,2…192,190	G286,288…2,4,317,319…129,131
SM = 4	G17,18…255,256	G304,303…66,65
SM = 5	G18,17….256,255	G303,304…65,66
SM = 6	G33,35…269,271,34,36…270,272	G288,286…52,50,287,285…51,49
SM = 7	G35,33…271,269,36,34…272,270	G286,288…50,52,285,287…49,51

NL[5:0]: Set the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by this instruction. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.
Liquid crystal drive lines

NL[5:0]	Number of lines	NL[5:0]	Number of lines	NL[5:0]	Number of lines
6'h00	Setting inhibited	6'h0E	Setting inhibited	6'h1C	Setting inhibited
6'h01	Setting inhibited	6'h0F	Setting inhibited	6'h1D	240(lines)
6'h02	Setting inhibited	6'h10	Setting inhibited	6'h1E	248
6'h03	Setting inhibited	6'h11	Setting inhibited	6'h1F	256
6'h04	Setting inhibited	6'h12	Setting inhibited	6'h20	264
6'h05	Setting inhibited	6'h13	Setting inhibited	6'h21	272
6'h06	Setting inhibited	6'h14	Setting inhibited	6'h22	280
6'h07	Setting inhibited	6'h15	176lines	6'h23	288
6'h08	Setting inhibited	6'h16	Setting inhibited	6'h24	296
6'h09	Setting inhibited	6'h17	Setting inhibited	6'h25	304
6'h0A	Setting inhibited	6'h18	Setting inhibited	6'h26	312
6'h0B	Setting inhibited	6'h19	Setting inhibited	6'h27	320
6'h0C	Setting inhibited	6'h1A	Setting inhibited	6'h28-6'h3F	Setting inhibited
6'h0D	Setting inhibited	6'h1B	Setting inhibited		

X = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value							
	ptg[1:0]	pts[1:0]	rev	gs	ss	sm	isc[3:0]	nl[5:0]
Power On Sequence	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'h0010	6'h27
S/W Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'h0010	6'h27
H/W Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'h0010	6'h27

9.2.2.7 Entry mode set (B7h)

<table>
<tr><td>B7h</td><td colspan="12">ETMOD(Entry mode set)</td></tr>
<tr><td></td><td>DC</td><td>RD</td><td>WR</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>B7</td></tr>
<tr><td>parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>gon</td><td>dte</td><td>X</td><td>06</td></tr>
<tr><td>Description</td><td colspan="12">Gon/dte: set output level of gate driver.
<table><tr><th>Gon</th><th>dte</th><th>G1-G320 gate output</th></tr><tr><td>0</td><td>0</td><td>Vgh</td></tr><tr><td>0</td><td>1</td><td>Vgh</td></tr><tr><td>1</td><td>0</td><td>Vgl</td></tr><tr><td>1</td><td>1</td><td>Normal display</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06h</td></tr><tr><td>S/W Reset</td><td>06h</td></tr><tr><td>H/W Reset</td><td>06h</td></tr></table></td></tr>
</table>

9.2.2.8 Power control 0(60h)

60h	PWRCTRL1(power control 0)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	0	0	0	0	60h
parameter	1	1	↑	XX	X	vrh[6:0]							10h

Description

Vrh[5:0]: set the vreg1out level, which is the reference voltage of Vcom and grayscale voltage.

Vrh[6:0]	Vreg1out VCI	Vrh[6:0]	Vreg1out Bandgap
7'b1000000	2.85	7'b0000000	2.85
7'b1000001	2.90	7'b0000001	2.90
7'b1000010	2.95	7'b0000010	2.95
7'b1000011	3.00	7'b0000011	3.00
7'b1000100	3.05	7'b0000100	3.05
7'b1000101	3.10	7'b0000101	3.10
7'b1000110	3.15	7'b0000110	3.15
7'b1000111	3.20	7'b0000111	3.20
7'b1001000	3.25	7'b0001000	3.25
7'b1001001	3.30	7'b0001001	3.30
7'b1001010	3.35	7'b0001010	3.35
7'b1001011	3.40	7'b0001011	3.40
7'b1001100	3.45	7'b0001100	3.45
7'b1001101	3.50	7'b0001101	3.50
7'b1001110	3.55	7'b0001110	3.55
7'b1001111	3.60	7'b0001111	3.60
7'b1010000	3.65	7'b0010000	3.65
7'b1010001	3.70	7'b0010001	3.70
7'b1010010	3.75	7'b0010010	3.75
7'b1010011	3.80	7'b0010011	3.80
7'b1010100	3.85	7'b0010100	3.85
7'b1010101	3.90	7'b0010101	3.90
7'b1010110	3.95	7'b0010110	3.95
7'b1010111	4.00	7'b0010111	4.00
7'b1011000	4.05	7'b0011000	4.05
7'b1011001	4.10	7'b0011001	4.10
7'b1011010	4.15	7'b0011010	4.15
7'b1011011	4.20	7'b0011011	4.20
7'b1011100	4.25	7'b0011100	4.25
7'b1011101	4.30	7'b0011101	4.30
7'b1011110	4.35	7'b0011110	4.35
7'b1011111	4.40	7'b0011111	4.40
7'b1100000	4.45	7'b0100000	4.45
7'b1100001	4.50	7'b0100001	4.50
7'b1100010	4.55	7'b0100010	4.55
7'b1100011	4.60	7'b0100011	4.60
7'b1100100	4.65	7'b0100100	4.65
7'b1100101	4.70	7'b0100101	4.70
7'b1100110	4.75	7'b0100110	4.75
7'b1100111	4.80	7'b0100111	4.80
7'b1101000	4.85	7'b0101000	4.85
7'b1101001	4.90	7'b0101001	4.90
7'b1101010	4.95	7'b0101010	4.95

	7'b1101011	5.00	7'b0101011	5.00
	7'b1101100	5.05	7'b0101100	5.05
	7'b1101101	5.10	7'b0101101	5.10
	7'b1101110	5.15	7'b0101110	5.15
	7'b1101111	5.20	7'b0101111	5.20
	7'b1110000	5.25	7'b0110000	5.25
	7'b1110001	5.30	7'b0110001	5.30
	7'b1110010	5.35	7'b0110010	5.35
	7'b1110011	5.40	7'b0110011	5.40
	7'b1110100	5.45	7'b0110100	5.45
	7'b1110101	5.50	7'b0110101	5.50
	7'b1110110	5.55	7'b0110110	5.55
	7'b1110111	5.60	7'b0110111	5.60
	7'b1111000	5.65	7'b0111000	5.65
	7'b1111001	5.70	7'b0111001	5.70
	7'b1111010	5.75	7'b0111010	5.75
	7'b1111011	5.80	7'b0111011	5.80
	7'b1111100	5.85	7'b0111100	5.85
	7'b1111101	5.90	7'b0111101	5.90
	7'b1111110	5.95	7'b0111110	5.95
	7'b1111111	6.00	7'b0111111	6.00

Note: Make sure that VRH setting restriction: VREG1OUT≤(DDVDH-0.3).
X = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	10h
S/W Reset	10h
H/W Reset	10h

9.2.2.9 Power control 1, 2, 5(64h,65h,6ah)

	PWRCTRL1(power control 1,2,5)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	0	1	0	0	64h
Parameter	1	1	↑	XX	x	x	ga_ap[1:0]		com_ap[1:0]		cmp_ap[1:0]		00h
Command	0	1	↑	XX	0	1	1	0	0	1	0	1	65h
Parameter	1	1	↑	XX	X	X	X	X	vreg_ap[1:0]		X	X	00h
Command	0	1	↑	XX	0	1	1	0	1	0	1	0	6ah
Parameter	1	1	↑	XX	src_str	com_str	X	X	sap2[1:0]		sap[1:0]		00h
Description	**ga_ap:** gamma bias current setting **com_ap:** VCOM bias current setting **cmp_ap**: charge pump comparator bias current setting **vreg_ap[1:0]：** VREG1 amplifier bias current setting **src_str:** strong source driving **com_str:** strong VCOM driving **sap2[1:0]:** source driver bias current setting **sap[1:0]:** source driver bias current setting X = Don't care.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	64h	65h	6ah
Power On Sequence	00h	00h	00h
S/W Reset	00h	00h	00h
H/W Reset	00h	00h	00h

9.2.2.10 Power control 3 (66h)

66h	PWRCTRLA(power control 3)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	0	1	1	0	66h
Parameter	1	1	↑	XX	vram[1:0]		X	osc_trim[4:0]					90h
Description	**vram[1:0]:** VDD voltage setting **osc_trim[4:0]:** oscillator trimming X = Don't care.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	90h
S/W Reset	90h
H/W Reset	90h

9.2.2.11 Power control 4 (69h)

69h	PWRCTRLA(power control a)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	1	0	0	1	69h
Parameter	1	1	↑	XX	X	X	dc_vghl[1:0]		dc_vcl[1:0]		dc_ddvdh[1:0]		1ah
Description	**Dc_vghl[1:0]:** VGH, VGL charge pump clock requency selection **Dc_vcl[1:0]:** VCL charge pump clock requency selection **Dc_ddvdh[1:0]:** DDVDH charge pump clock requency selection X = Don't care.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	1ah
S/W Reset	1ah
H/W Reset	1ah

9.2.2.12 Power control 6,7 (6eh,71h)

	PWRCTRLA(power control 6,7)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	1	1	1	0	6eh
Parameter	1	1	↑	XX	ddvdh_set[3:0]				X	X	X	X	84h
Command	0	1	↑	XX	0	1	1	1	0	0	0	1	71h
Parameter	1	1	↑	XX	X	vgh_set[2:0]			X	vgl_set[2:0]			52h
Description	**ddvdh_set[3:0]:** DDVDH voltage setting, "0000": 4.18V, "1111": 6.36V, 0.145V per step. **Vgh_set[2:0]:** VGH voltage setting, "000": 13.25V, "111": 16.1V, 0.405V per step. **Vgl_set[2:0]:** VGL voltage setting, "000": -10.8V, "111": -8V, 0.405V per step. X = Don't care.												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	6eh	71h
Power On Sequence	84h	52h
S/W Reset	84h	52h
H/W Reset	84h	52h

9.2.2.13 Vcom control 1-2(6bh, 6ch)

	Vcom control 1-2												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	1	0	1	1	6bh
Parameter	1	1	↑	XX	X	X	vcm[5:0]						31h
Command	0	1	↑	XX	0	1	1	0	1	1	0	0	6ch
Parameter	1	1	↑	XX	X	X	X	vdv[4:0]					18h

Description

VCM[5:0]: Adjust the VcomH level (the higher level of Vcom AC voltage). The VCM5-0 bits can set the VcomH level 0.4 ~ 0.98 times the VREG1OUT level. When VCM4-0 = "111111", stop the internal volume adjustment and adjust the VcomH with external resistance from VcomR.

VCM5:0	VCOMH	VCM5:0	VCOMH
000000	Vreg1out*0.685	100000	Vreg1out*0.845
000001	Vreg1out*0.690	100001	Vreg1out*0.850
000010	Vreg1out*0.695	100010	Vreg1out*0.855
000011	Vreg1out*0.700	100011	Vreg1out*0.860
000100	Vreg1out*0.705	100100	Vreg1out*0.865
000101	Vreg1out*0.710	100101	Vreg1out*0.870
000110	Vreg1out*0.715	100110	Vreg1out*0.875
000111	Vreg1out*0.720	100111	Vreg1out*0.880
001000	Vreg1out*0.725	101000	Vreg1out*0.885
001001	Vreg1out*0.730	101001	Vreg1out*0.890
001010	Vreg1out*0.735	101010	Vreg1out*0.895
001011	Vreg1out*0.740	101011	Vreg1out*0.900
001100	Vreg1out*0.745	101100	Vreg1out*0.905
001101	Vreg1out*0.750	101101	Vreg1out*0.910
001110	Vreg1out*0.755	101110	Vreg1out*0.915
001111	Vreg1out*0.760	101111	Vreg1out*0.920
010000	Vreg1out*0.765	110000	Vreg1out*0.925
010001	Vreg1out*0.770	110001	Vreg1out*0.930
010010	Vreg1out*0.775	110010	Vreg1out*0.935
010011	Vreg1out*0.780	110011	Vreg1out*0.940
010100	Vreg1out*0.785	110100	Vreg1out*0.945
010101	Vreg1out*0.790	110101	Vreg1out*0.950
010110	Vreg1out*0.795	110110	Vreg1out*0.955
010111	Vreg1out*0.800	110111	Vreg1out*0.960
011000	Vreg1out*0.805	111000	Vreg1out*0.965
011001	Vreg1out*0.810	111001	Vreg1out*0.970
011010	Vreg1out*0.815	111010	Vreg1out*0.975
011011	Vreg1out*0.820	111011	Vreg1out*0.980
011100	Vreg1out*0.825	111100	Vreg1out*0.985
011101	Vreg1out*0.830	111101	Vreg1out*0.990
011110	Vreg1out*0.835	111110	Vreg1out*0.995
011111	Vreg1out*0.840	111111	Vreg1out*1.000

Description

VDV[4:0] Adjust the factor of VREG1OUT to set the amplitude of Vcom.

VDV4:0	|COMH-VCOML|	VDV4:0	|VCOMH-VCOML|
00000	Vreg1out*0.70	10000	Vreg1out*0.94
00001	Vreg1out*0.72	10001	Vreg1out*0.96
00010	Vreg1out*0.74	10010	Vreg1out*0.98
00011	Vreg1out*0.76	10011	Vreg1out*1.00
00100	Vreg1out*0.78	10100	Vreg1out*1.02
00101	Vreg1out*0.80	10101	Vreg1out*1.04
00110	Vreg1out*0.82	10110	Vreg1out*1.06
00111	Vreg1out*0.84	10111	Vreg1out*1.08
01000	Vreg1out*0.86	11000	Vreg1out*1.10
01001	Vreg1out*0.88	11001	Vreg1out*1.12
01010	Vreg1out*0.90	11010	Vreg1out*1.14
01011	Vreg1out*0.92	11011	Vreg1out*1.16
01100	Vreg1out*0.94	11100	Vreg1out*1.18
01101	Vreg1out*0.96	11101	Vreg1out*1.20
01110	Vreg1out*0.98	11110	Vreg1out*1.22
01111	Vreg1out*1.00	11111	Vreg1out*1.24

Note :
1. Adjust VREG1OUT and VCM0-5 so that the VcomH level is set within the range of 3.0V~ (DDVDH-0.3)V.
2. Adjust VREG1OUT and VDV0-4 so that the Vcom amplitude is set to 6.0V or less.

X = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	6bh	6ch
Power On Sequence	31h	18h
S/W Reset	No change	No change
H/W Reset	31h	18h

9.2.2.14 Gamma control 1-6(E0h, E1h, E2h, E3h, E4h, E5h)

	Gamma control 1-6												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0
1st parameter	1	1	↑	XX	X	X	X	pkp0[4:0]					0bh
2nd parameter	1	1	↑	XX	X	X	X	pkp1[4:0]					17h
3rd parameter	1	1	↑	XX	X	X	X	pkp2[4:0]					06h

4th parameter	1	1	↑	XX	X	X	X	pkp3[4:0]					10h
5thparameter	1	1	↑	XX	X	X	X	pkp4[4:0]					05h
6thparameter	1	1	↑	XX	X	X	X	pkp5[4:0]					12h
7thparameter	1	1	↑	XX	X	X	X	Pkp6[4:0]					0ah
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1
1stparameter	1	1	↑	XX	X	prp0[6:0]							1bh
2ndparameter	1	1	↑	XX	X	prp1[6:0]							5ah
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2
1stparameter	1	1	↑	XX	X	X	Vrp0[5:0]						0ah
2ndparameter	1	1	↑	XX	X	X	Vrp1[5:0]						2eh
3rd parameter	1	1	↑	XX	X	X	Vrp2[5:0]						27h
4th parameter	1	1	↑	XX	X	X	Vrp3[5:0]						19h
5thparameter	1	1	↑	XX	X	X	Vrp4[5:0]						18h
6thparameter	1	1	↑	XX	X	X	Vrp5[5:0]						2bh
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3
1stparameter	1	1	↑	XX	X	X	X	pkn0[4:0]					0ch
2ndparameter	1	1	↑	XX	X	X	X	pkn1[4:0]					19h
3rd parameter	1	1	↑	XX	X	X	X	pkn2[4:0]					0fh
4th parameter	1	1	↑	XX	X	X	X	pkn3[4:0]					19h
5thparameter	1	1	↑	XX	X	X	X	pkn4[4:0]					08h
6thparameter	1	1	↑	XX	X	X	X	pkn5[4:0]					13h
7thparameter	1	1	↑	XX	X	X	X	Pkn6[4:0]					13h
Command	0	1	↑	XX	1	1	1	0	0	1	0	0	E4
1stparameter	1	1	↑	XX	X	prn0[6:0]							1bh
2ndparameter	1	1	↑	XX	X	prn1[6:0]							5ah
Command	0	1	↑	XX	1	1	1	0	0	1	0	1	E5
1stparameter	1	1	↑	XX	X	X	vrn0[5:0]						0ah
2ndparameter	1	1	↑	XX	X	X	vrn1[5:0]						22h
3rd parameter	1	1	↑	XX	X	X	vrn2[5:0]						20h
4th parameter	1	1	↑	XX	X	X	vrn3[5:0]						13h
5thparameter	1	1	↑	XX	X	X	vrn4[5:0]						0ch
6thparameter	1	1	↑	XX	X	X	vrn5[5:0]						2bh

Description	E0h to E5h are gamma adjust registers. See gamma correction section for reference. X = Don't care.
Restriction	

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

9.2.2.15 Gate driver timing (Ech)

Ech	Gate driver timing												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	0	0	EC
1st Parameter	1	1	↑	XX	nowe[3:0]				nowi[3:0]				33h
2nd Parameter	1	1	↑	XX	nowi_e[7:0]								16h
3rd Parameter	1	1	↑	XX	nowe_e[7:0]								16h
4th parameter	1	1	↑	XX	gcse[3:0]				gcsi[3:0]				44h
5th parameter	1	1	↑	XX	gcsi_e[7:0]								15h
6th parameter	1	1	↑	XX	gcse_e[7:0]								15h

Description

NOWI[3:0]: Set the gate output start point from a reference point when synchronizing with internal clock signal.
Note: The clock in this table is a frequency-divided internal clock.

NOWI[3:0]		NOWI[3:0]	
4'h0	0clock	4'h8	8clock
4'h1	1clock	4'h9	9clock
4'h2	2clocks	4'hA	10clocks
4'h3	3clocks	4'hB	11clocks
4'h4	4clocks	4'hC	12clocks
4'h5	5clocks	4'hD	13clocks
4'h6	6clocks	4'hE	14clocks
4'h7	7clocks	4'hF	15clocks

NOWE[3:0]: Set the gate output start point in RGB operation.

NOWE[3:0]		NOWE[3:0]	
4'h0	0(internal clock period*see note)	4'h8	8(internal clock period*see note)
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

Note:
1clock=(Number of data transfers/pixel) x DIVE (division ratio)[DOTCLK]

NOWI_E[7:0]: Set the gate output end point from a reference point when synchronizing with internal clock signal.
NOWE_E[7:0]: Set the gate output end point in RGB operation.

GCSE [3:0]: gate_cs falling edge (external clock)

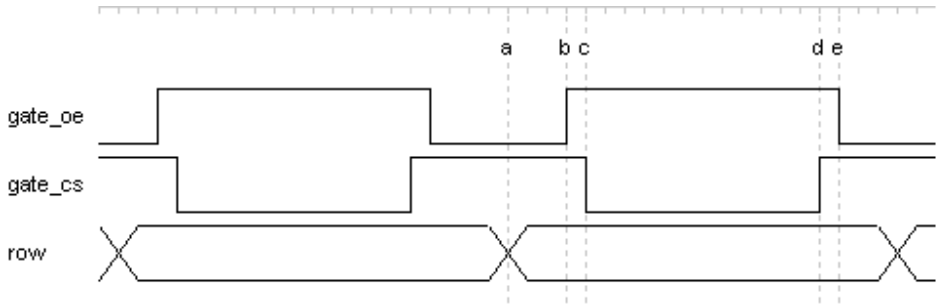
GCSE[3:0]		GCSE[3:0]	
4'h0	0clock	4'h8	8clock
4'h1	1clock	4'h9	9clock
4'h2	2clocks	4'hA	10clocks
4'h3	3clocks	4'hB	11clocks
4'h4	4clocks	4'hC	12clocks
4'h5	5clocks	4'hD	13clocks
4'h6	6clocks	4'hE	14clocks
4'h7	7clocks	4'hF	15clocks

GCSI [3:0]: gate_cs falling edge (internal clock)

GCSI[3:0]		GCSI[3:0]	
4'h0	0clock	4'h8	8clock

	4’h1	1clock	4’h9	9clock
	4’h2	2clocks	4’hA	10clocks
	4’h3	3clocks	4’hB	11clocks
	4’h4	4clocks	4’hC	12clocks
	4’h5	5clocks	4’hD	13clocks
	4’h6	6clocks	4’hE	14clocks
	4’h7	7clocks	4’hF	15clocks

GCSI_E[7:0]: gate_cs rising edge (internal clock)
GCSE_E [7:0]: gate_cs rising edge (external clock)



Time a: row switching point, base time point
Time a-b: nowi, nowe
Time a-c: gcsi, gcse
Time a-d: gcsi_e, gcse_e
Time a-e: nowi_e, nowe_e

X = Don’t care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

9.2.2.16 Source, VCOM driver timing (Edh)

Edh	Source, VCOM driver timing												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	0	1	edh
1st Parameter	1	1	↑	XX	vcsie	vcsiv[2:0]			scsie	scsiv[2:0]			bbh
2nd Parameter	1	1	↑	XX	vcsee	vcsev[2:0]			scsee	scsev[2:0]			bbh
3rd Parameter	1	1	↑	XX	X	mcpe[2:0]			X	mcpi[2:0]			00h
4th parameter	1	1	↑	XX	X	mspe[2:0]			X	mspi[2:0]			00h
5th parameter	1	1	↑	XX	X	lde[2:0]			X	ldi[2:0]			11h
6th parameter	1	1	↑	XX	X	com_cs_str_delay[2:0]			X	X	cs_delay[1:0]		21h

Description

COM_CS_STR_DELAY[2:0]： delay of fully turn on com charge sharing switches

CS_DELAY[1:0]: control source charge sharing delay between 4 blocks

VCSIE：Set Vcom charge sharing off/on when synchronizing with internal clock signal.

VCSIV [2:0]：Sets Vcom charge sharing time when synchronizing with internal clock signal.

0	Setting disabled
1	1clock
2	2clocks
3	3clocks
4	4clocks
5	5clocks
6	6clocks
7	7clocks

SCSIE：Set Source charge sharing off/on when synchronizing with internal clock signal.

SCSIV [2:0]：Sets Source charge sharing time when synchronizing with internal clock signal.

0	Setting disabled
1	1clock
2	2clocks
3	3clocks
4	4clocks
5	5clocks
6	6clocks
7	7clocks

VCSEE：Set Vcom charge sharing off/on when synchronizing in RGB operation

VCSEV [2:0]：Sets Vcom charge sharing time when synchronizing in RGB operation.

0	Setting disabled
1	1clock
2	2clocks
3	3clocks
4	4clocks
5	5clocks
6	6clocks
7	7clocks

SCSEE：Set Source charge sharing off/on when synchronizing in RGB operation.

SCSEV [2:0]：Sets Source charge sharing time when synchronizing in RGB operation.

0	Setting disabled
1	1clock
2	2clocks
3	3clocks
4	4clocks
5	5clocks

6	6clocks
7	7clocks

MCPE [2:0]：Specify theVcom output timing for liquid crystal AC drive in RGB operation.

MCPE[2;0]	Vcom output position
3'h0	Setting disabled
3'h1	1clock
3'h2	2clocks
3'h3	3clocks
3'h4	4clocks
3'h5	5clocks
3'h6	6clocks
3'h7	7clocks

Vcom output timing from a reference point

Note:
1clock=(Number of data transfers/pixel) x DIVE (division ratio)[DOTCLK]

MCPI[2:0]: Set the Vcom output timing when synchronizing with internal clock signal.
MCPI[2:0] Vcom output timing from a reference point

3'h0	Setting disabled
3'h1	1clock
3'h2	2clocks
3'h3	3clocks
3'h4	4clocks
3'h5	5clocks
3'h6	6clocks
3'h7	7clocks

Note:
The clock in this table is a frequency-divided internal clock.

MSPE [2:0]：Specify the source output timing and Vcom alternating timing for liquid crystal AC drive in RGB operation.

MSPE[2;0]	Source output position
3'h0	Setting disabled
3'h1	1clock
3'h2	2clocks
3'h3	3clocks
3'h4	4clocks
3'h5	5clocks
3'h6	6clocks
3'h7	7clocks

Source output timing from a reference point

Note:
1clock=(Number of data transfers/pixel) x DIVE (division ratio)[DOTCLK].

MSPI[2:0]: Set the source output timing when synchronizing with internal clock signal.
MSPI[2:0] Source output timing from a reference point

3'h0	Setting disabled
3'h1	1clock
3'h2	2clocks
3'h3	3clocks
3'h4	4clocks
3'h5	5clocks
3'h6	6clocks
3'h7	7clocks

LDE [2:0]：ld start point (external clock)

0	Setting disabled
1	1clock
2	2clocks
3	3clocks
4	4clocks
5	5clocks
6	6clocks
7	7clocks

LDI [2:0]：ld start point (internal clock)

0	Setting disabled
1	1clock
2	2clocks
3	3clocks
4	4clocks
5	5clocks
6	6clocks
7	7clocks

X = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

9.2.2.17 Interface control (F6h)

F6h	IFCTL(Interface control)												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6
1st Parameter	1	1	↑	XX	my_eor	mx_eor	mv_eor	0	bgr_eor	0	0	we mode	01
2nd Parameter	1	1	↑	XX	X	X	Epf[1:0]		X	X	Mdt[1:0]		10
3rd Parameter	1	1	↑	XX	spi_2wire_mode	X	endian	X	Dm[1:0]		rm	rim	00

Description

my_eor/mx_eor/mv_eor/bgr_eor: the set of value MADCTL is used in the IC is derived as exclusive OR between first parameter of IFCTL and MADCTL parameter.

Mdt[1:0]: select the method of display data transferring.
We_mode: memory write control.
We_mode=0: when the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.
We_mode=1: when the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

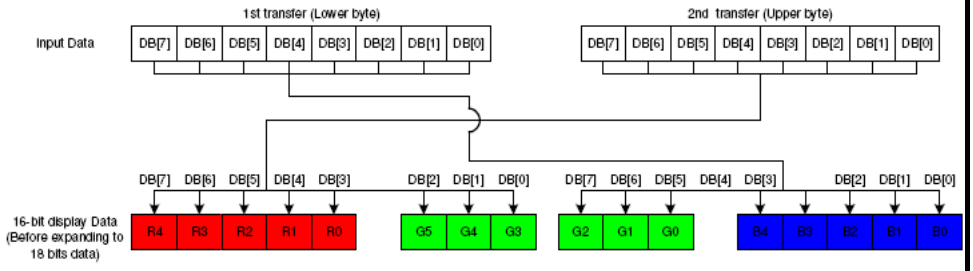
spi_2wire_mode： enable 2-wire data lane serial interface mode

Endian: select the little endian interface bit. At little endian mode, the host sends LSB data first.

Endian	Data transfer mode
0	Normal (MSB first)
1	Little endian (LSB first)

Note:
the little endian is valid on only 65k 8bit and 9bit MCU interface mode.

X = Don't care.



Dm[1:0]: select the display operation mode.

Dm[1]	Dm[0]	Display operation mode
0	0	Internal clock operation
0	1	RGB interface mode
1	0	Vsync interface mode
1	1	prohibit

The dm][1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation and the Vsync interface is prohibited.

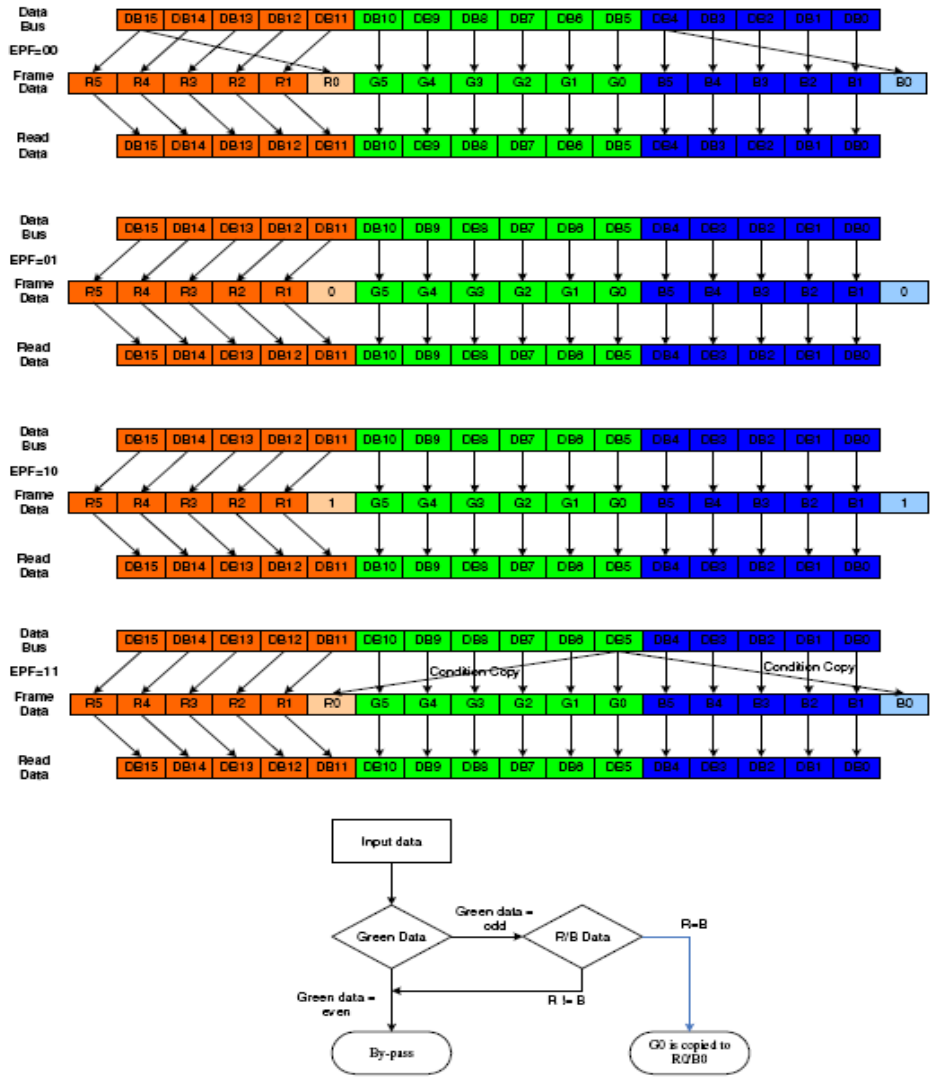
Rm: select the interface to access the GRAM.

Rm	Interface for RAM access
0	System interface/Vsync interface
1	RGB interface

Rim: specify the RGB interface mode when RGB interface is used. These bits should be set before display operation through RGB interface and should not be set during operation.

Rim	COLMOD[6:4]	Display operation mode
0	110(262k color)	18 bit RGB interface (1 transfer/pixel)
	101(65k color)	16 bit RGB interface (1 transfer/pixel)
1	110(262k color)	6 bit RGB interface (3 transfer/pixel)
	101(65k color)	6 bit RGB interface (3 transfer/pixel)

Description



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h011000
S/W Reset	24'h011000
H/W Reset	24'h011000

9.2.2.18 lcd ac drive control (F7h)

F7h	lcd ac drive control											
	DC	RD	WR	D17 -8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	1	F7
1st Parameter	1	1	↑	XX	X	X	X	frc_en	X	X	nw[1:0]		10h

Description	**FRC_EN**:if frc_en=1, FRC enable; if frc_en=0,FRC disable. **NW [1:0]** / Function: 0 – VCOM toggle per one line; 1 – VCOM toggle two lines; 2 – VCOM toggle three lines; 3 – VCOM toggle four lines X = Don't care.
Restriction	
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out – Yes Normal Mode On, Idle Mode On, Sleep Out – Yes Partial Mode On, Idle Mode Off, Sleep Out – Yes Partial Mode On, Idle Mode On, Sleep Out – Yes Sleep In – Yes
Default	Power On Sequence – 10h S/W Reset – 10h H/W Reset – 10h

9.2.2.19 Private access (FD)

F7h	Private access												
	DC	RD	WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	0	1	FD
1st Parameter	1	1	↑	XX	private_access[15:8]								00h
2nd Parameter	1	1	↑	XX	private_access[7:0]								00h

Description	private_access : private registers access control Private access / private_access[15:8] / private_access[7:0]: enter private registers mode – 06h – 07h; exit private registers mode – fah – fbh X = Don't care.
Restriction	
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out – Yes Normal Mode On, Idle Mode On, Sleep Out – Yes Partial Mode On, Idle Mode Off, Sleep Out – Yes Partial Mode On, Idle Mode On, Sleep Out – Yes Sleep In – Yes
Default	Power On Sequence – 0000h S/W Reset – 0000h H/W Reset – 0000h

10. Functional description

10.1 Module CPU interface

10.1.1 Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

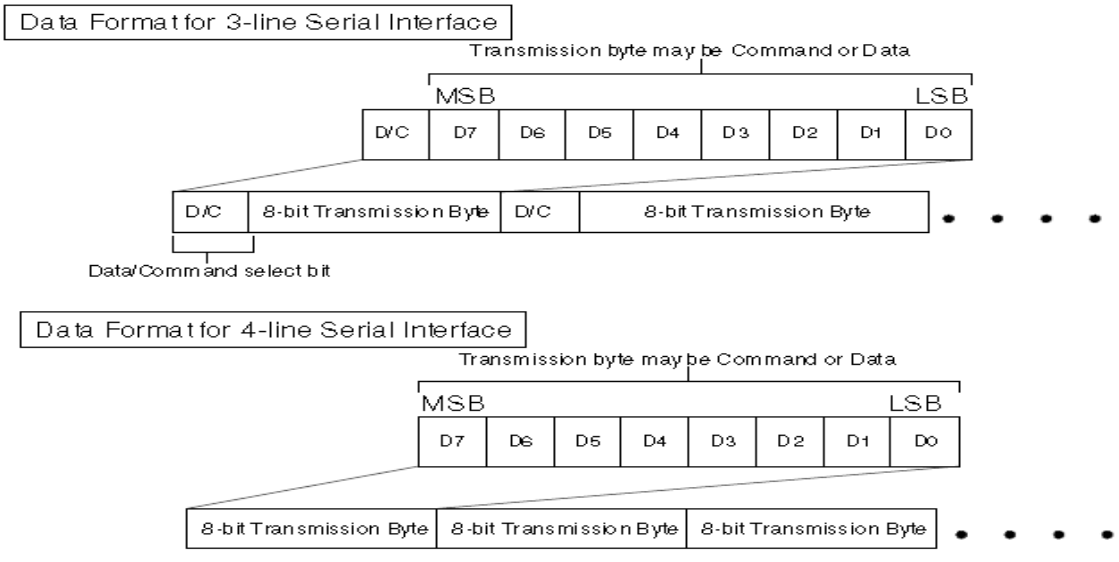
IM3	IM2	IM1	IM0	MCU-Interface Mode	CS	D/C	SCL	Function
0	1	0	1	3-line serial interface 2 data lane serial interface	"L"	-		Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	"H/L"		Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	"H/L"		Read/Write command, parameter or display data.

NV3029G-01 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and NV3029G-01. The 3-line serial mode consists of the chip enable input (CS), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (DC), chip enable input (CS), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

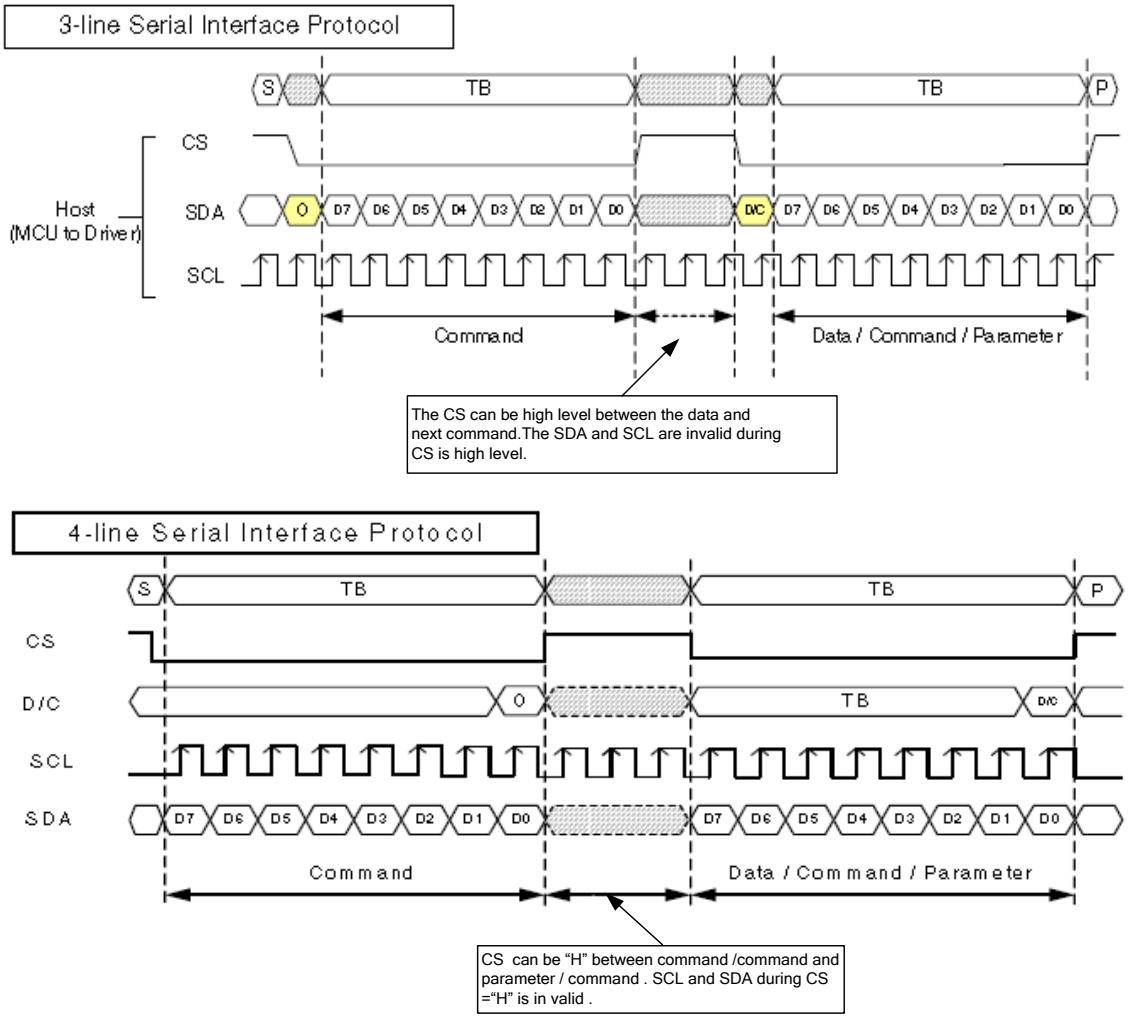
10.1.1.1 Write Cycle Sequence

The write mode of the interface means that host writes commands or data to NV3029G-01. The 3-lines serial data packet contains a data/command select bit (DC) and a transmission byte. If the DC bit is "low", the transmission byte is interpreted as a command byte. If the DC bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to NV3029G-01 and the MSB is transmitted first. The serial interface is initialized when CS is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CS enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.



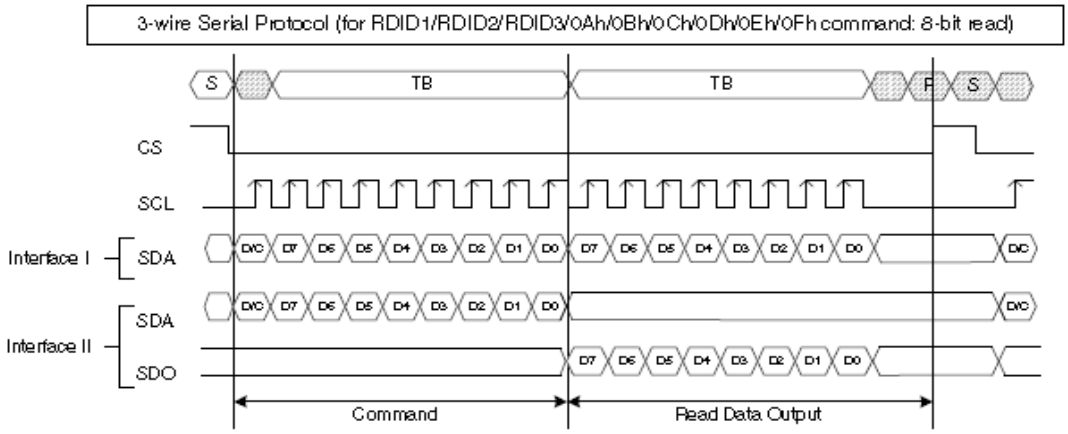
Host processor drives the CS pin to low and starts by setting the DC bit on SDA. The bit is read by NV3029G-01 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional DC signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

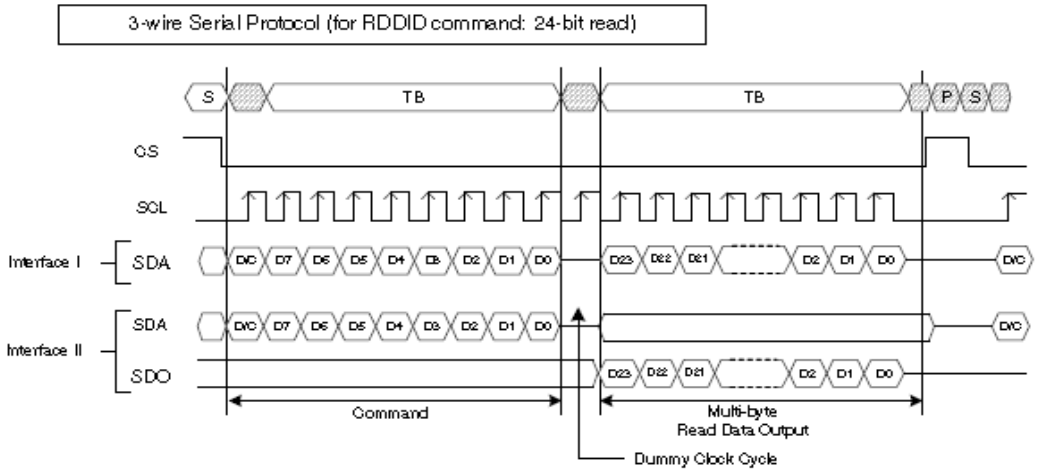


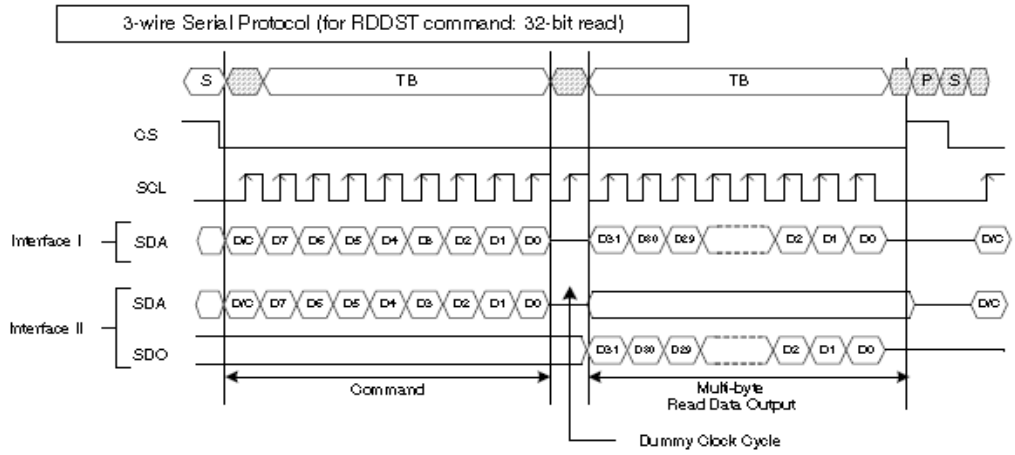
10.1.1.2 Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from NV3029G-01. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. NV3029G-01 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol

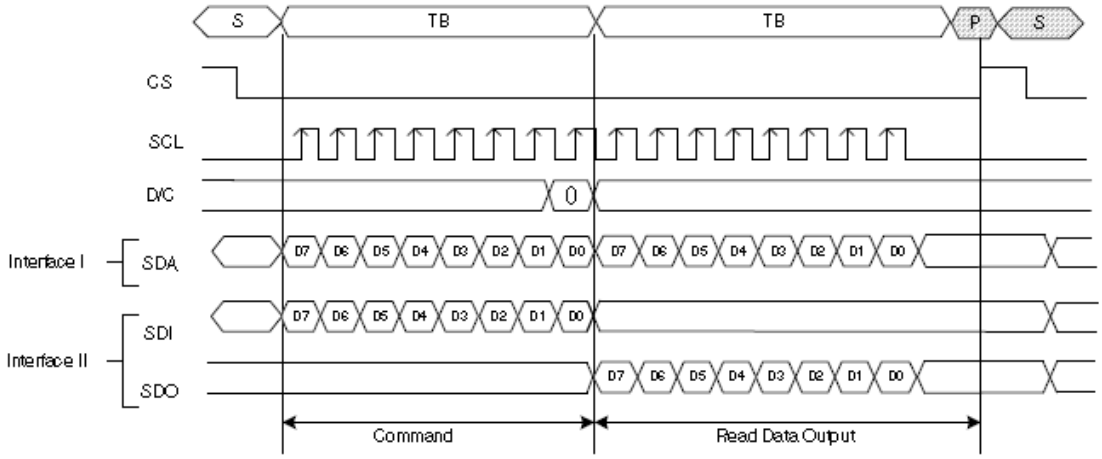




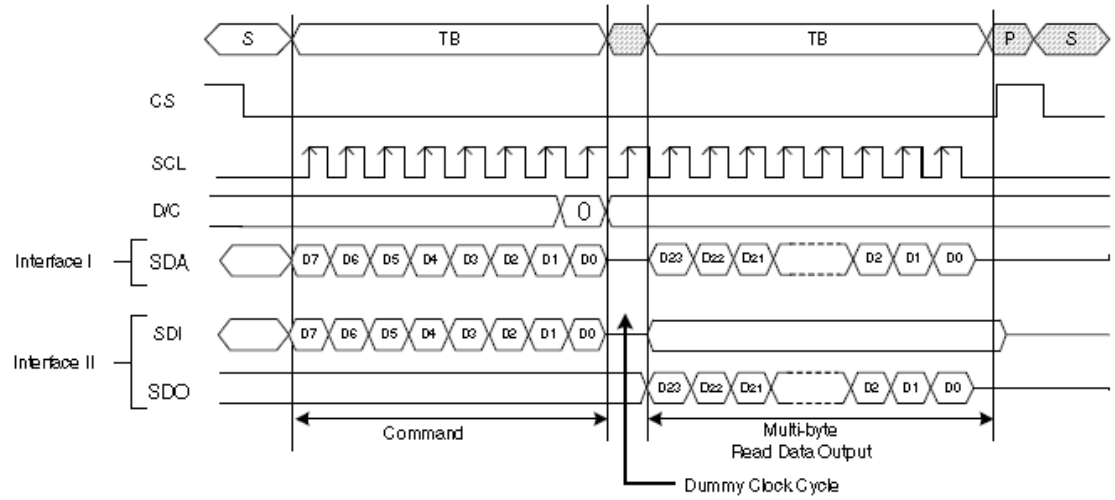


4-wire Serial Interface Protocol

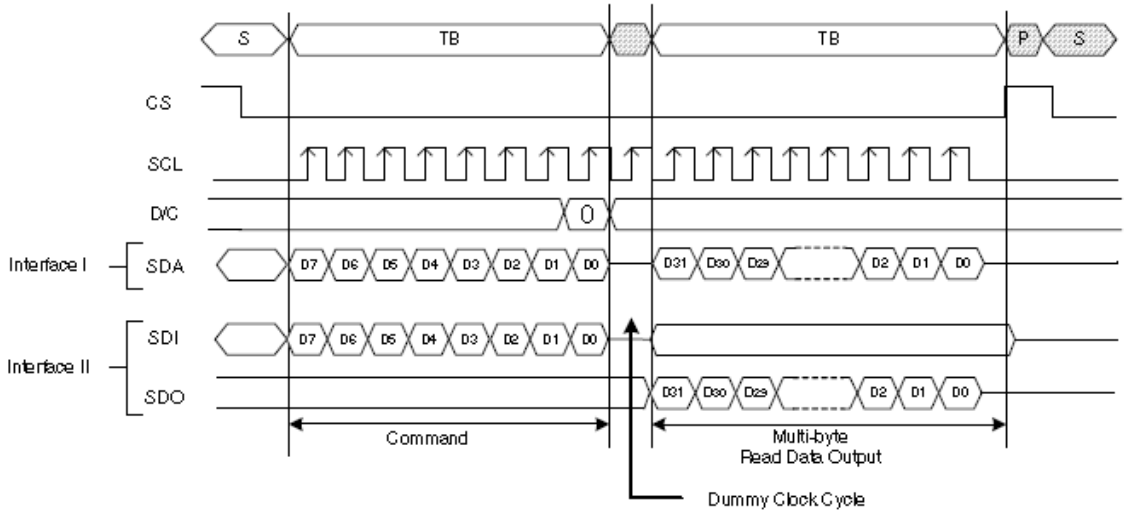
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-wire Serial Protocol (for RDDID command: 24-bit read)

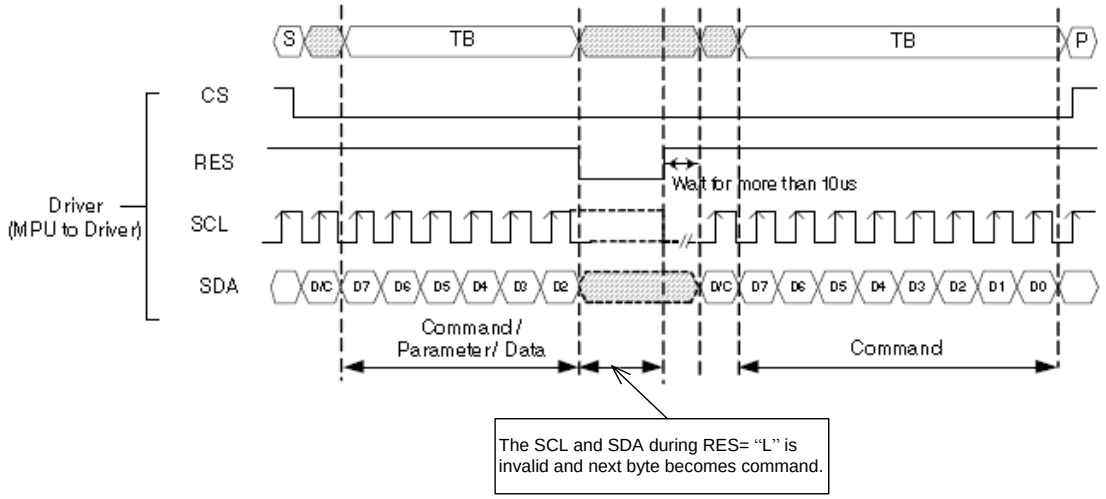


4-wire Serial Protocol (for RDDST command: 32-bit read)

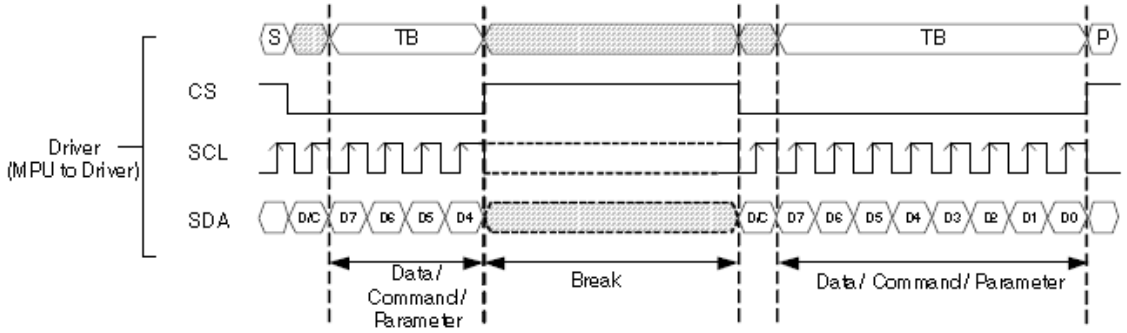


10.1.1.3 Data Transfer Break and Recovery

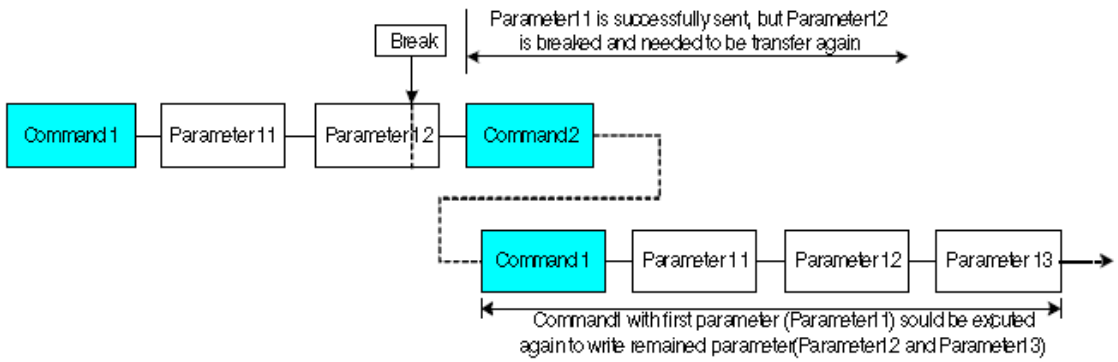
If there is a break in data transmission by RES pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CS) is activated after RES have been high state.



If there is a break in data transmission by CS pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CS) is next activated.



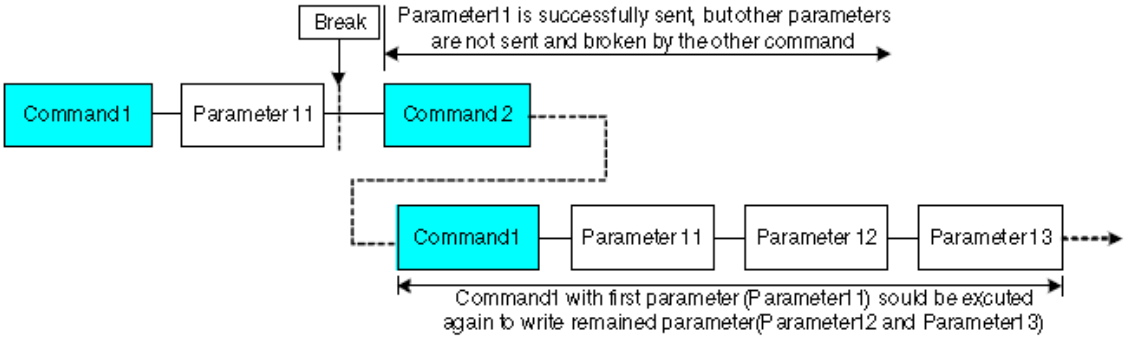
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

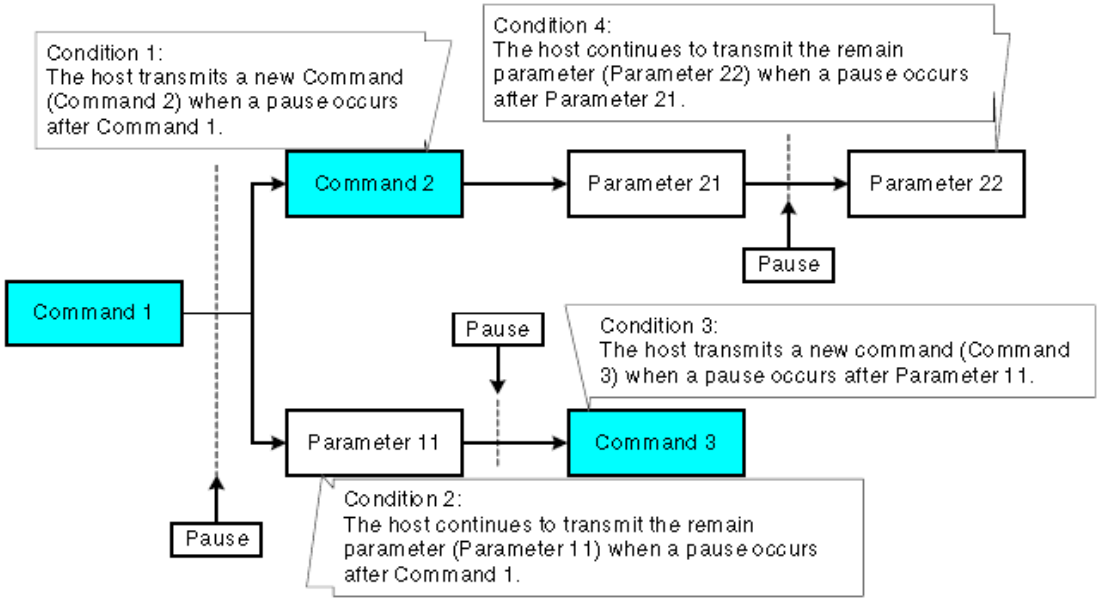
10.1.1.4 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CS) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then NV3029G-01 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

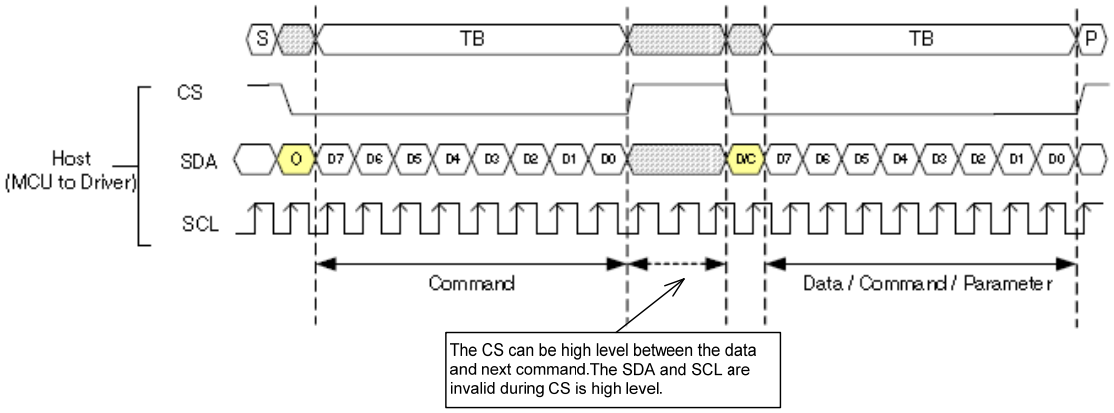


This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter



10.1.1.5 Serial Interface Pause (3_wire)



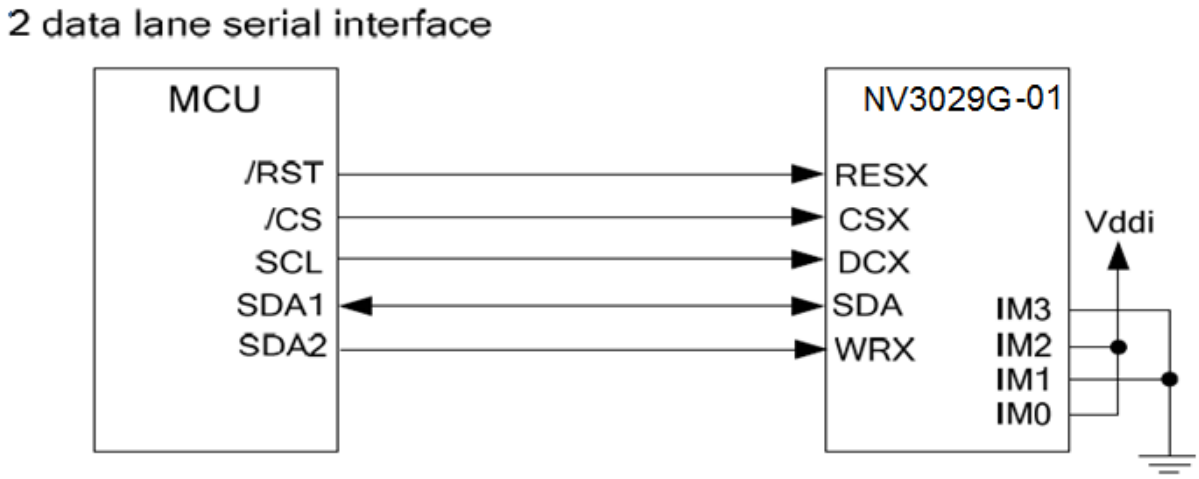
10.1.1.6 2 data lane serial interface

Interface selection:

IM3	IM2	IM1	IM0	Interface	Read back selection
0	1	0	1	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read)

2-wire data lane serial interface use: CSX (chip enable), DCX (serial clock) and SDA (serial data input/output 1), and WRX (serial data input 2). To enter this interface, register spi_2wire_mode, which is located in the 3rd parameter of command F6, should be set.

2 data lane hardware suggestion and Pin description:
2 data lane serial interface, IM[3:0]=0101

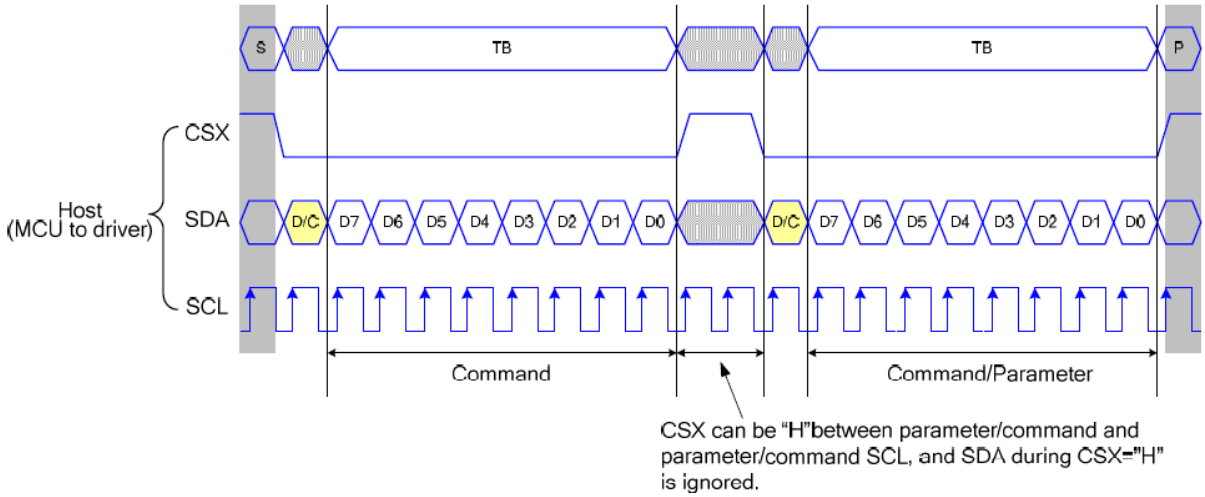


Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial data input/output1
WRX	Serial data input2

Command write mode:

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface,so users can ignore the input data of WRX.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



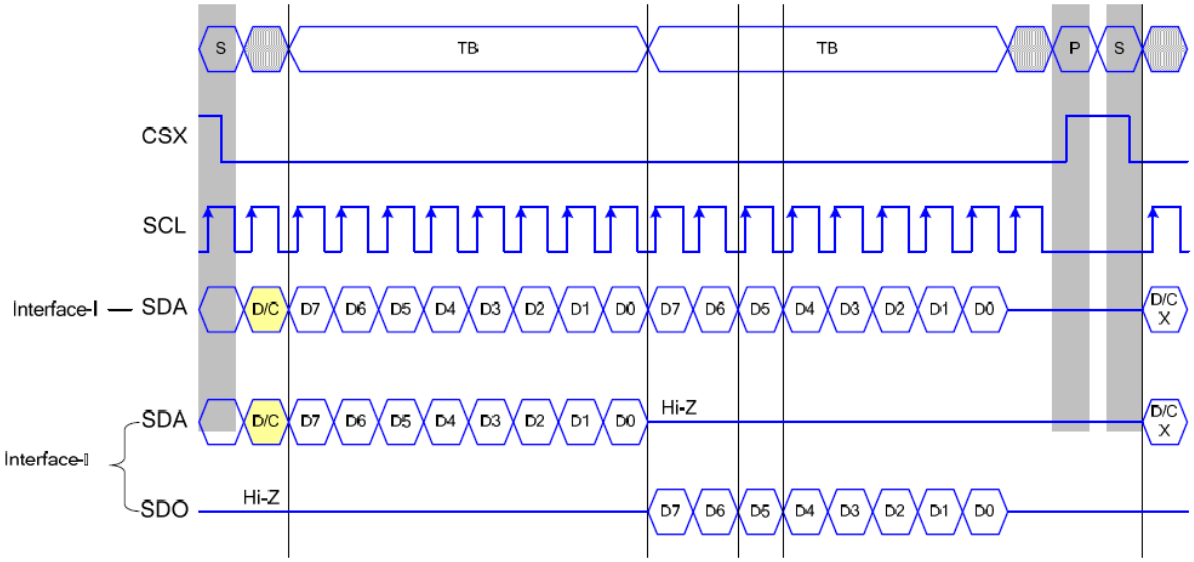
SRAM write mode:

The SRAM write mode of 2-wire data line serial interface need use SDA pin and WRX pin to be data input pins.

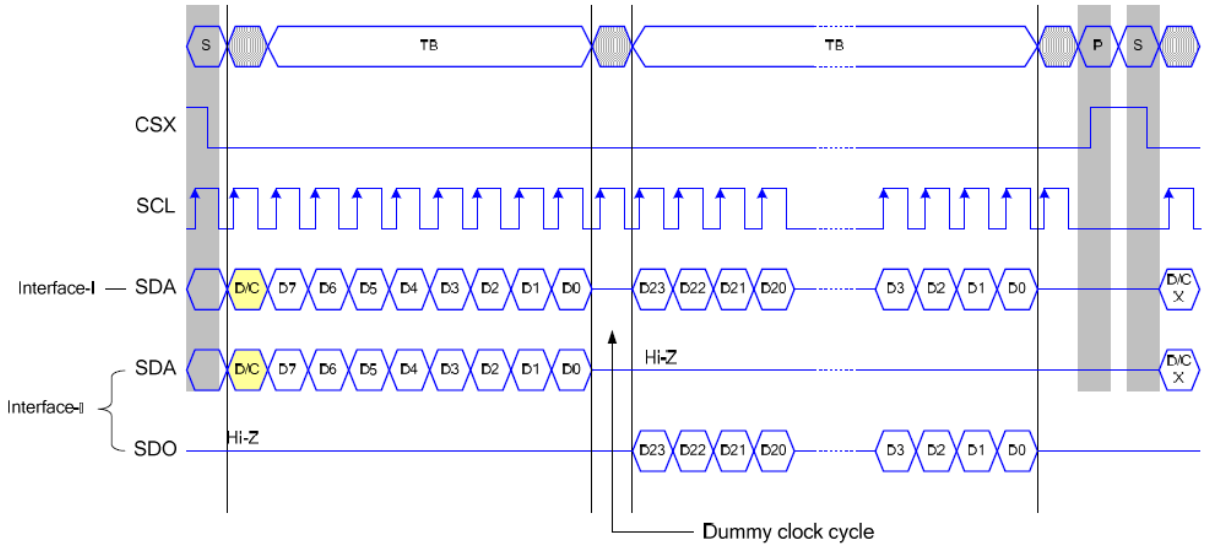
Read function:

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and WRX pin can be ignored. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

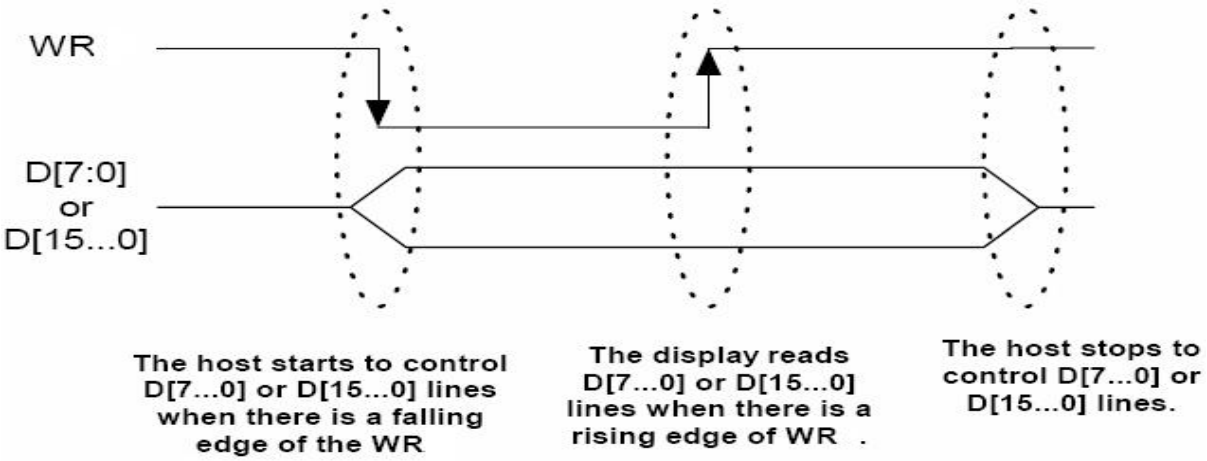
10.1.2 Parallel Interface

The Module uses a 11-wires 8-data parallel interface (IM0 = Low) or 19-wires 16-bit parallel interface (IM0 = High). The chip-select CS (active low) enables and disables the parallel interface. REST (active low) is an external reset signal. WR is the parallel data write, RD is the parallel data read and D[7…0] or D[15…0] is parallel data.
The Graphics Controller Chip reads the data at the rising edge of WR signal. The RS is data/command flag. When RS = "1", D15 (or D7) to D0 bits are display RAM data or command parameters. When DC = "0" D15 (or D7) to D0 bits are commands.

10.1.2.1 Write Cycle/Sequence

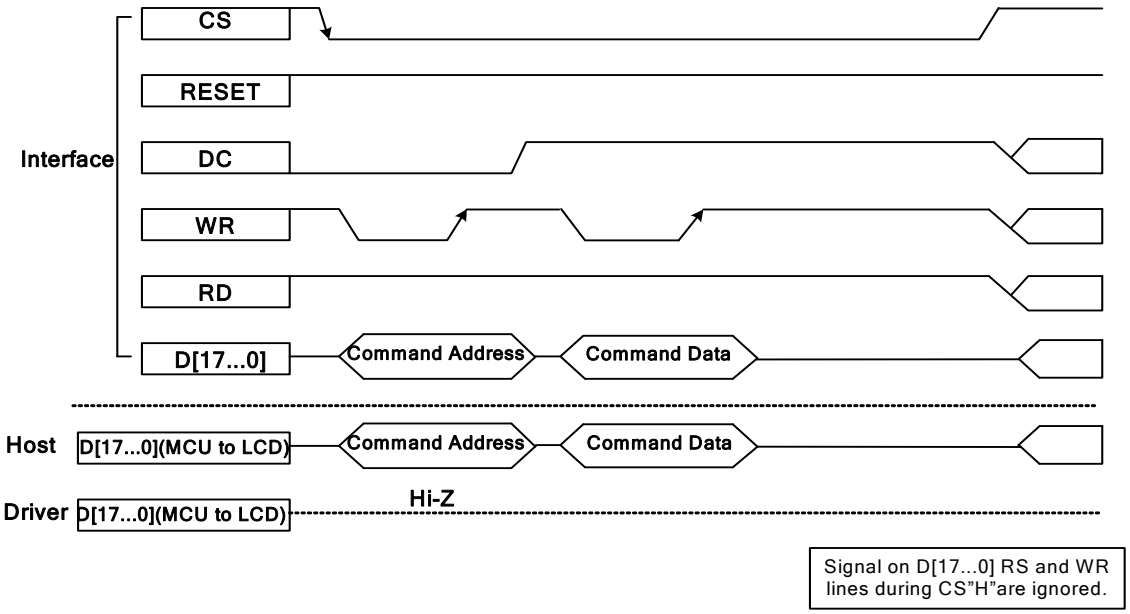
The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WR high-low-high sequence) consists of 3 control (DC, RD, WR) and 8 (D[7..0]) or 16 (D[15…0]) data signals. RS bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (='0') and vice versa it is data ('1').

The write cycle is described in the following figure.



Note: WR is an unsynchronized signal (it can be stopped).

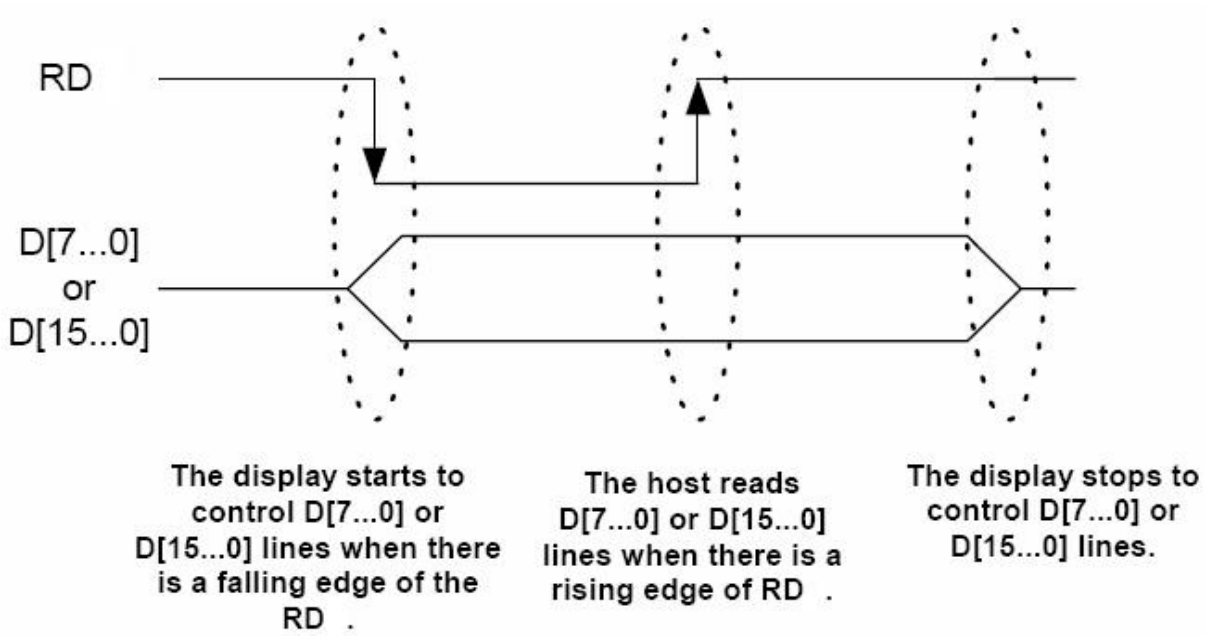
Parallel I/F write Sequence-Example



10.1.2.2 Read Cycle/Sequence

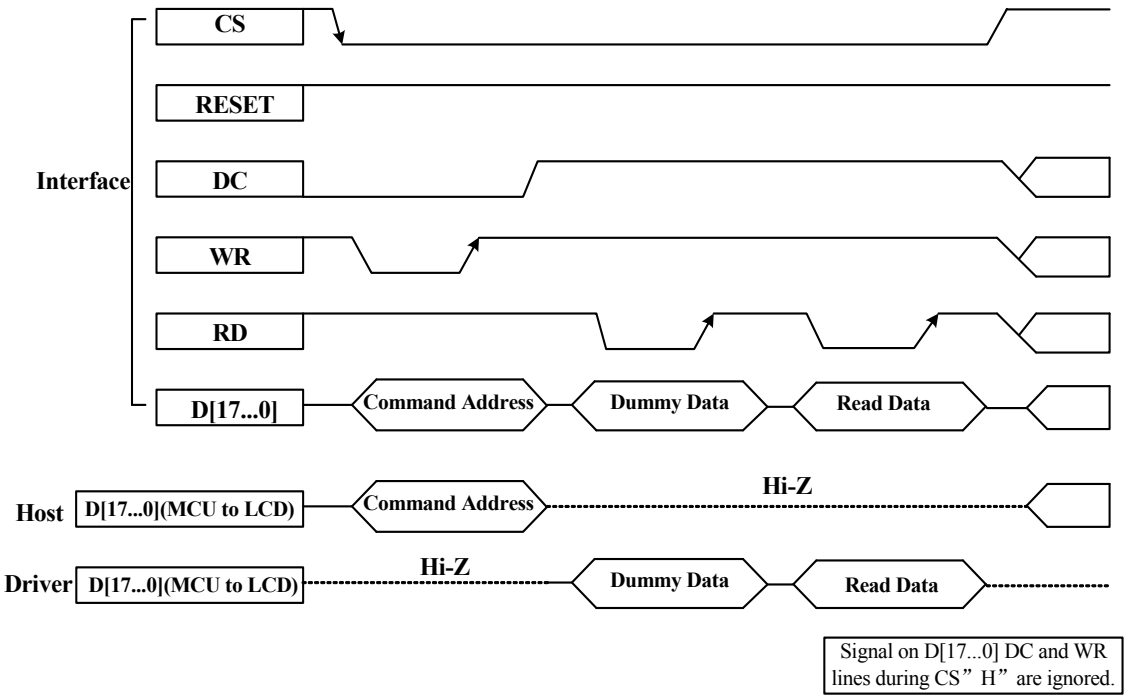
The read cycle (RD high-low-high sequence) means that the host reads information from the display via interface. The display sends data (D[7...0] or D[15…0]) to the host when there is a falling edge of RD and the host reads data when there is a rising edge of RD.

The RD cycle is described the following figure. . .



Note: RD is an unsynchronized signal (it can be stopped).

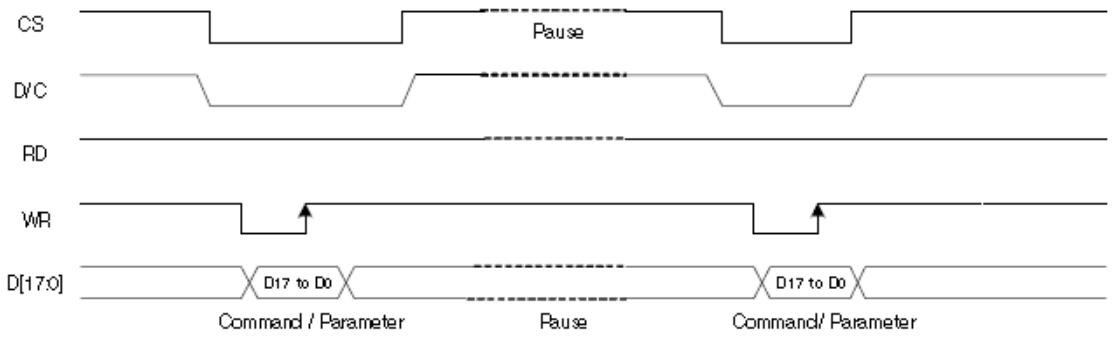
Parallel I/F Read Sequence-example



Note:

1. Read Data is only valid when DC input is set High, if DC is set Low during read then Driver Data line will be High Impedance.
2. This example is for commands: 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, Dah, DBh and DCh.
3. Other read commands are:
4. Command 04h →Dummy data (1 RD Cycle) →Data (3 RD Cycles)
5. Command 09h →Dummy data (1 RD Cycle) →Data (4 RD Cycles)
6. Command 2Eh →Dummy data (1 RD Cycle) →Data (Any Length RD Cycles More)

10.1.2.3 Parallel Interface Pause



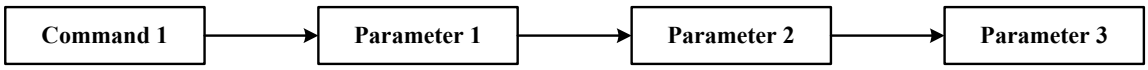
Note:

The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

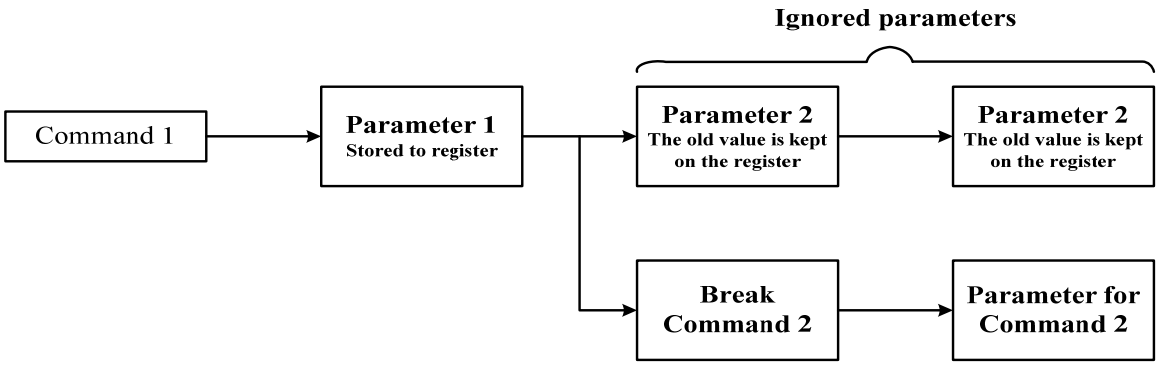
10.1.3 Display Module Data Transfer Break

If parameter 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameters after the break occurred is rejected if there is a new command as shown in the following example:

Without break

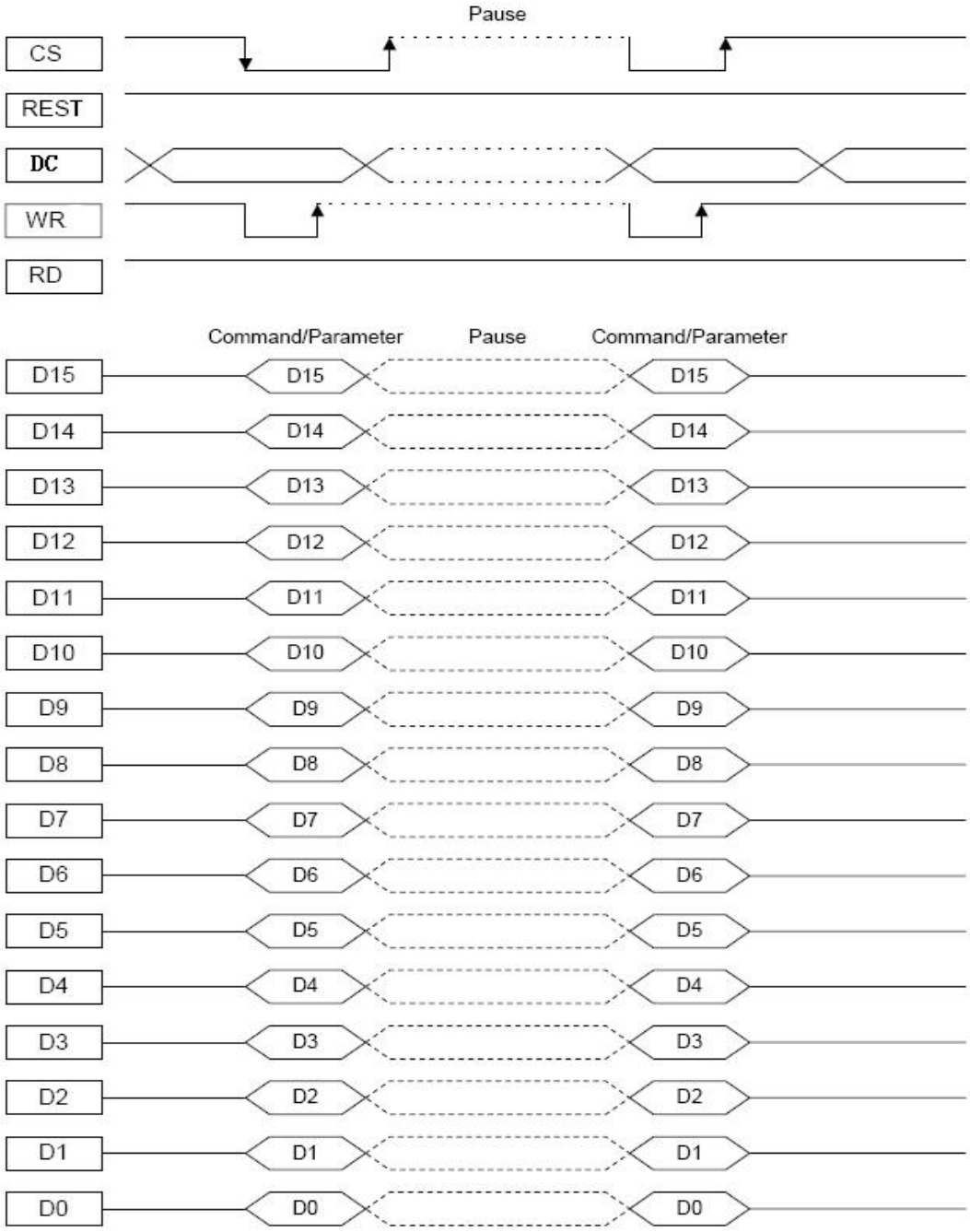


With break



Break can be e.g. another command or noise pulse.

10.1.4 Display Module Data Transfer Pause



This applies to the following 4 conditions:

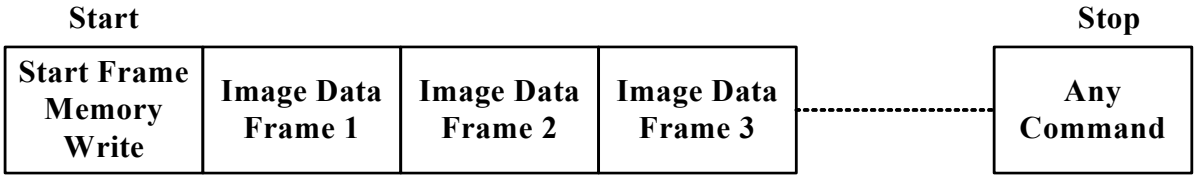
1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

10.1.5 Display Module Data Transfer Modes

The module has four color modes for transferring data to the display data RAM. These are 16-bit color per pixel, 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

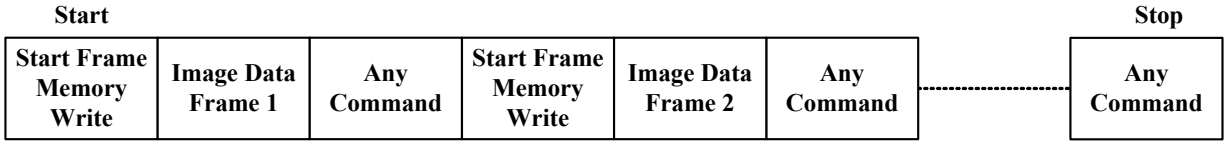
10.1.5.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start pint and the next Frame is written.



10.1.5.2 Method 2

The image data is sent and at end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame downloaded.



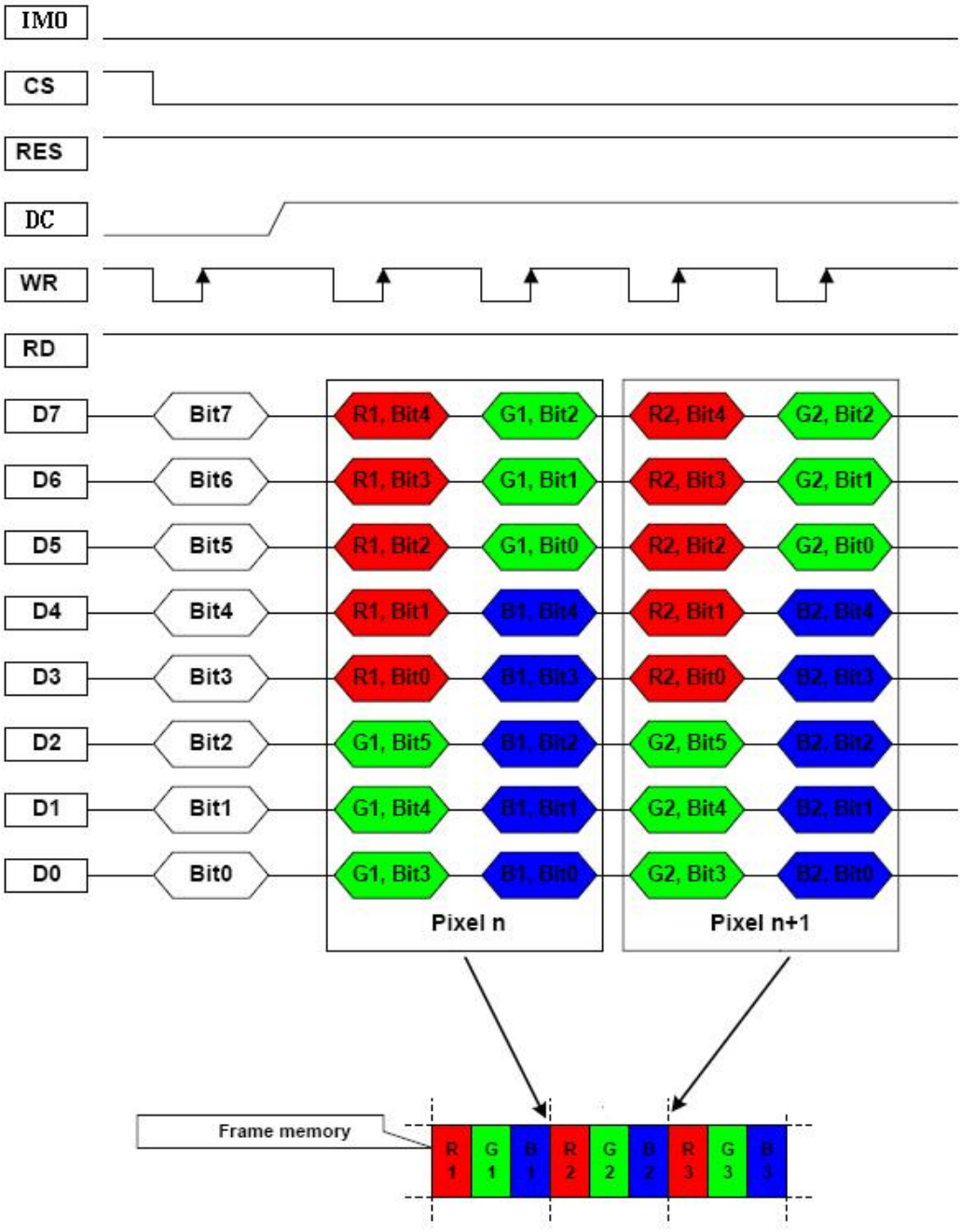
Note:

1. These apply to all Data Transfer Color modes on Parallel interface;
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored to the Frame Memory.

10.1.6 Display Module Data Color Coding

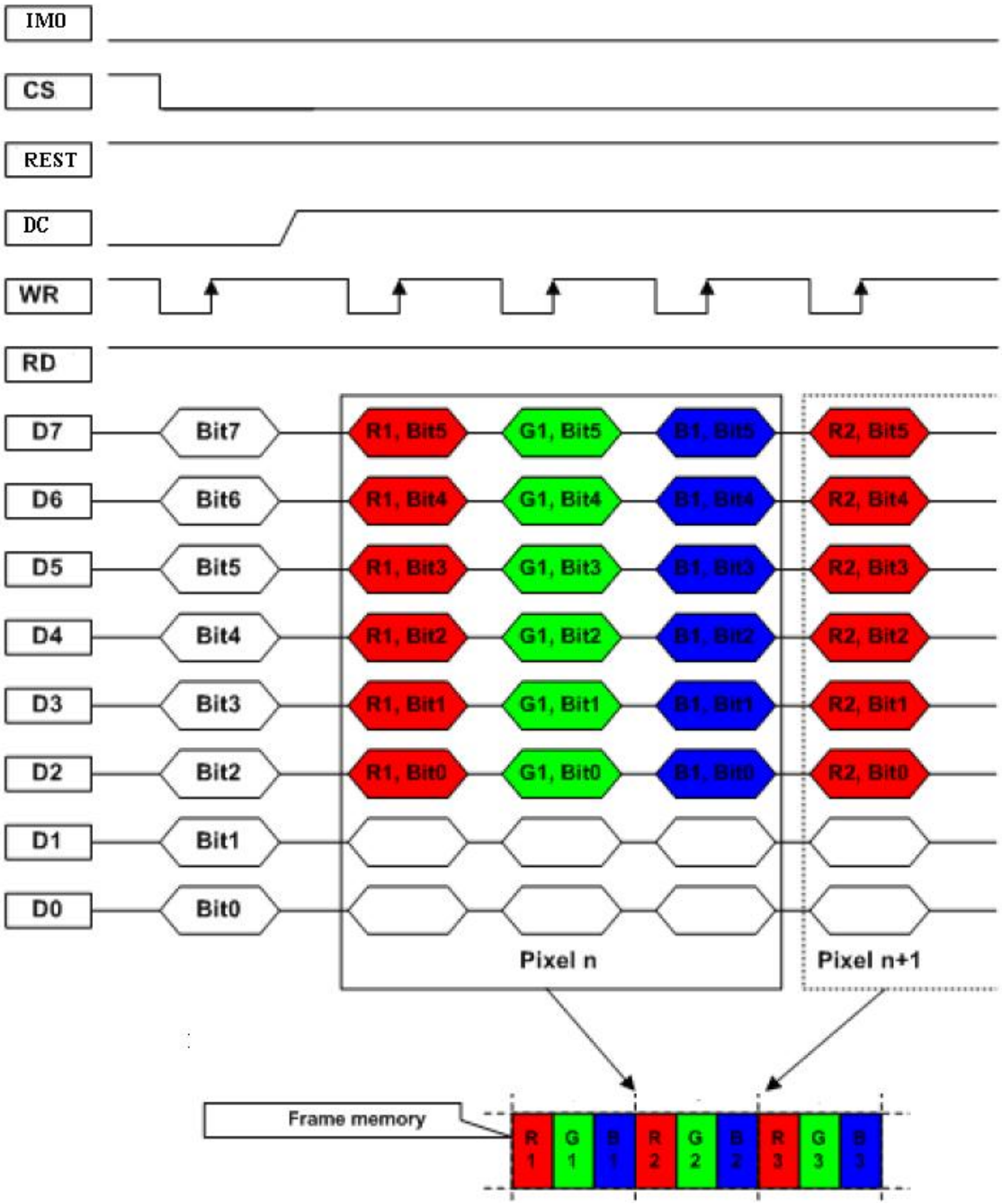
10.1.6.1 8 Data Line Parallel

16bit/Pixel(R 5-bit, G 6-bit, B 5-bit),65,536 colors



Note :
The Data order is as follows, MSB = D7, LSB = D0 and Picture Data is MSB = Bit5, LSB = Bit0 for Green data and MSB = Bit4, LSB = Bit0 for Red and Blue data.

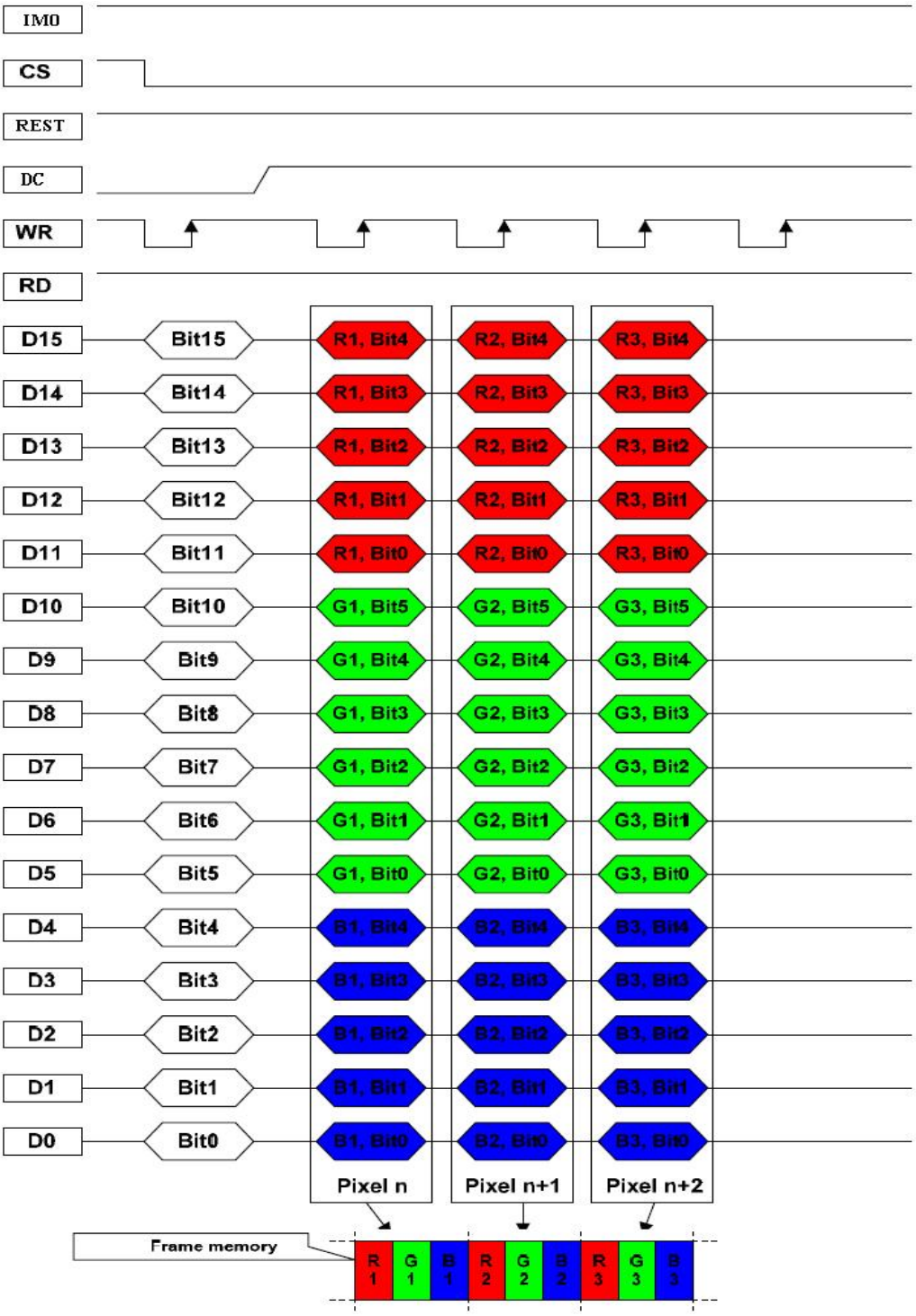
18 bit/pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 colors



Note:
The Data order is as follows, MSB = D7, LSB = D0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

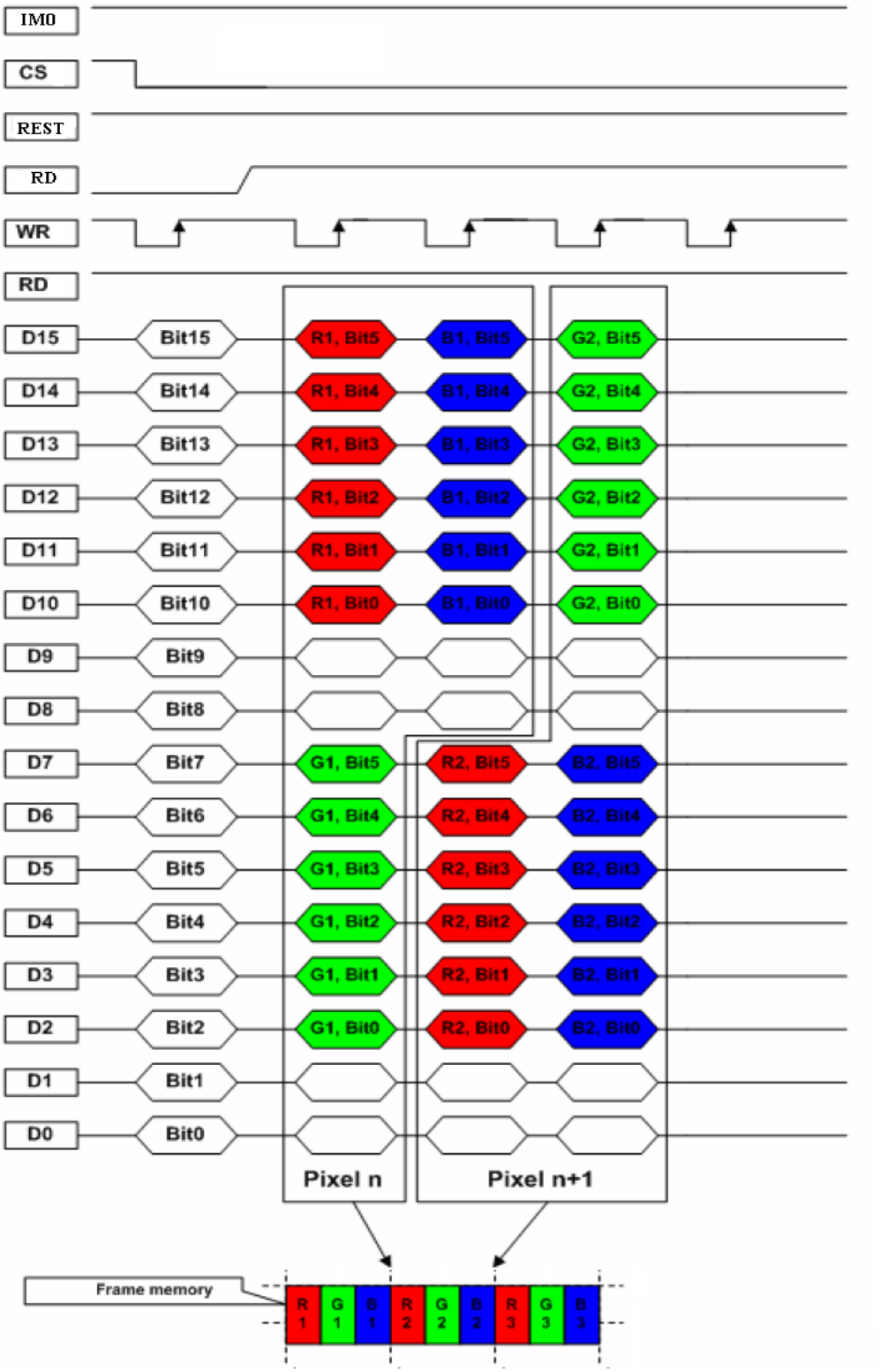
10.1.6.2 16 Data Line Parallel

16 bit/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 colors



Note :
The Data order is as follows, MSB = D15, LSB = D0 and Picture Data is MSB = Bit5, LSB = Bit0 for Green data and MSB = Bit4, LSB = Bit0 for Red and Blue data.

18 bit/pixel(R 6-bit,G 6-bit,B 6-bit),262,144colors

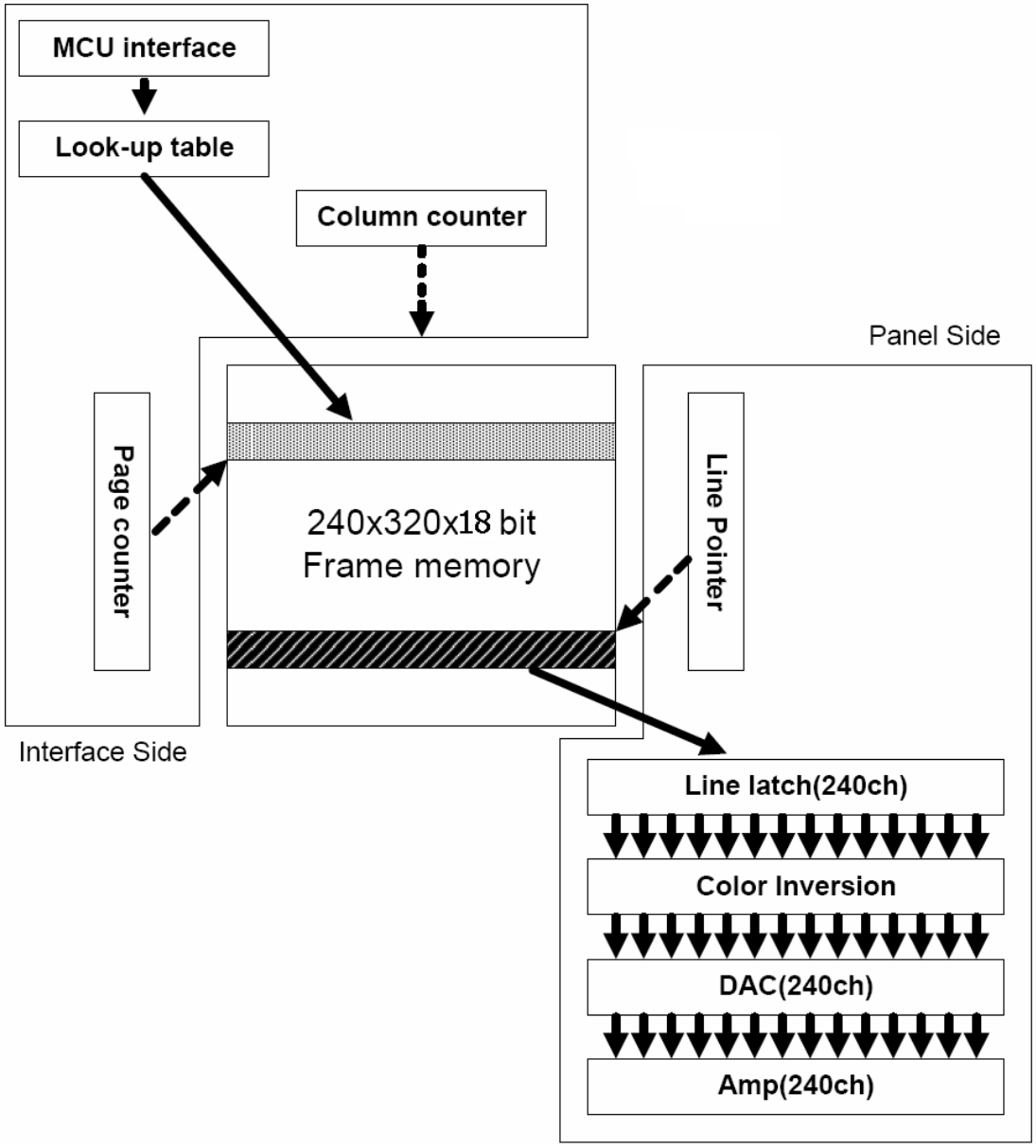


Note:
The Data Order is as follows MSB=D15, LSB=D0 and Picture Data is MSB=Bit 5, LSB=Bit0 for Red, Green and Blue data.

10.2 Display Data RAM

10.2.1 Configuration

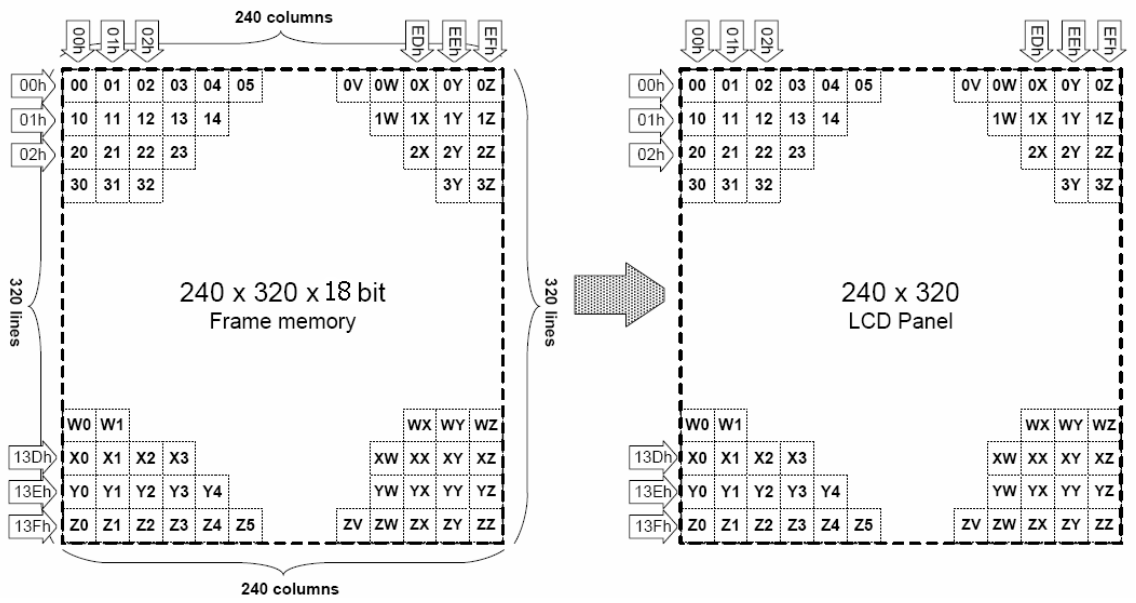
The display data RAM stores display dots and consists of 1,382,400 bits (240 X18X320 bits).There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



10.2.2 Memory to Display Address Mapping

10.2.2.1 Normal Display On or Partial Mode On, Vertical Scroll Off

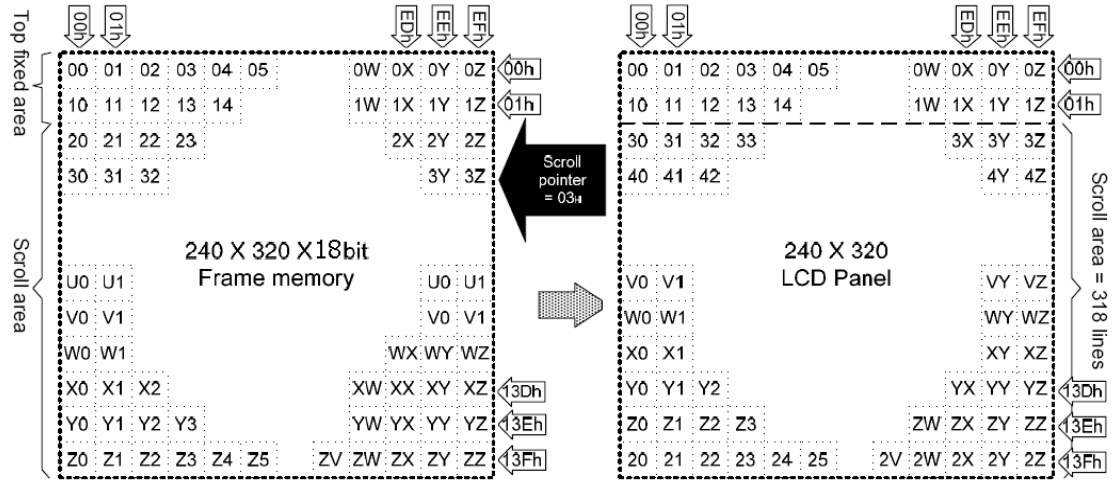
In this mode, contents of the frame memory within an area where column pointer is 0000h to 00Efh and page pointer is 0000h to 013Fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).



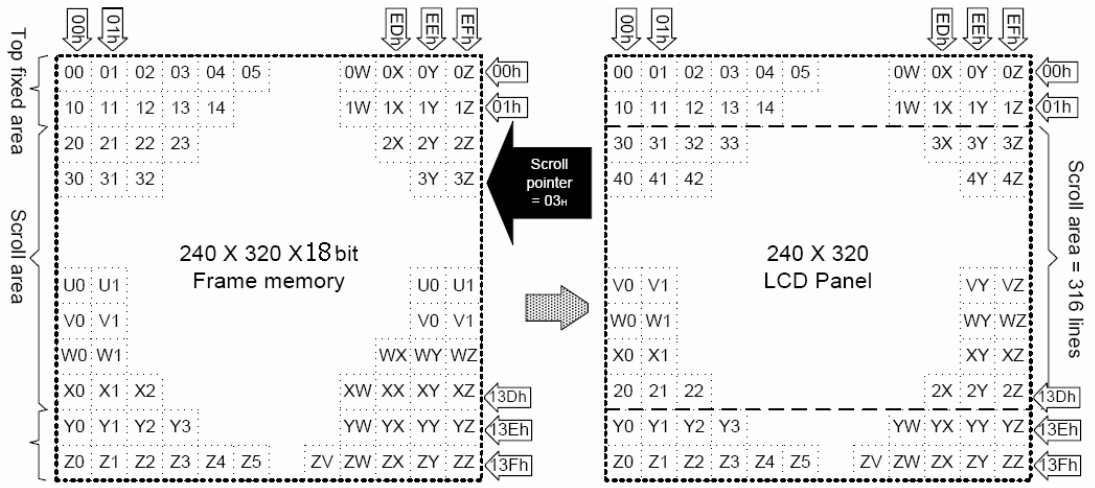
10.2.2.2 Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

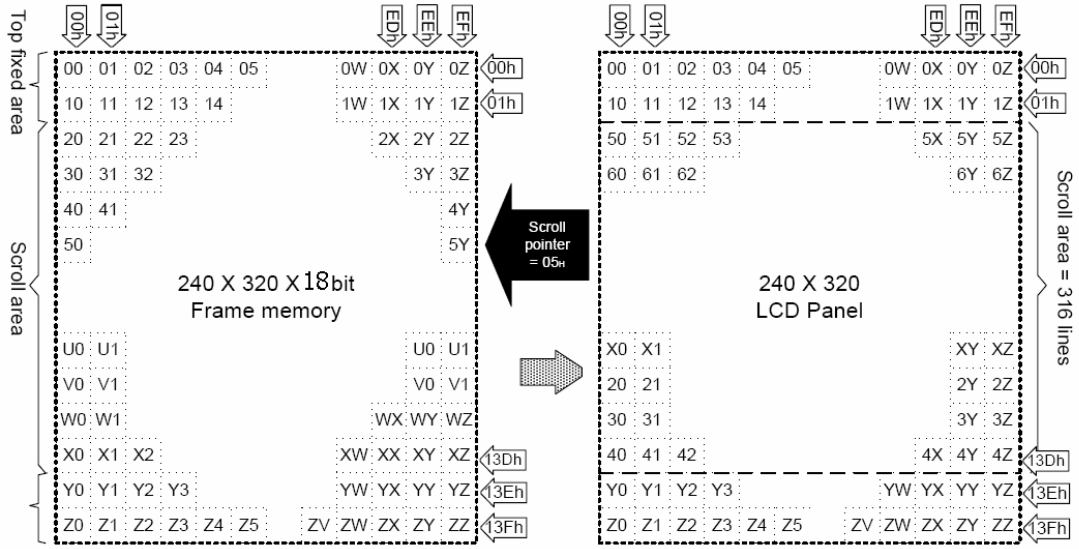
Example 1
TFA = 2, VSA = 318, BFA = 0 when MADCTL Bit B4 = 0



Example 2
TFA=2,VSA=316,BFA=2 when MADCTL bit B4=0



Example 3
TFA=2,VSA=316,BFA=4 when MADCTL bit B4=0



Note:
When Vertical Scrolling Definition Parameters(TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

10.2.2.3 Vertical Scroll example

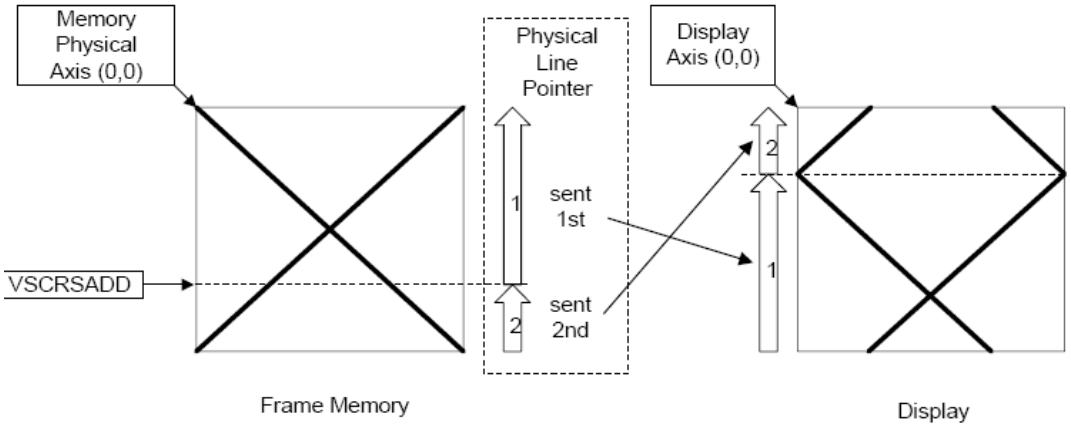
Case 1: TFA + VSA + BFA < 320

N/A. Do not set TFA + VSA + BFA < 320, unless unexpected picture will be shown.

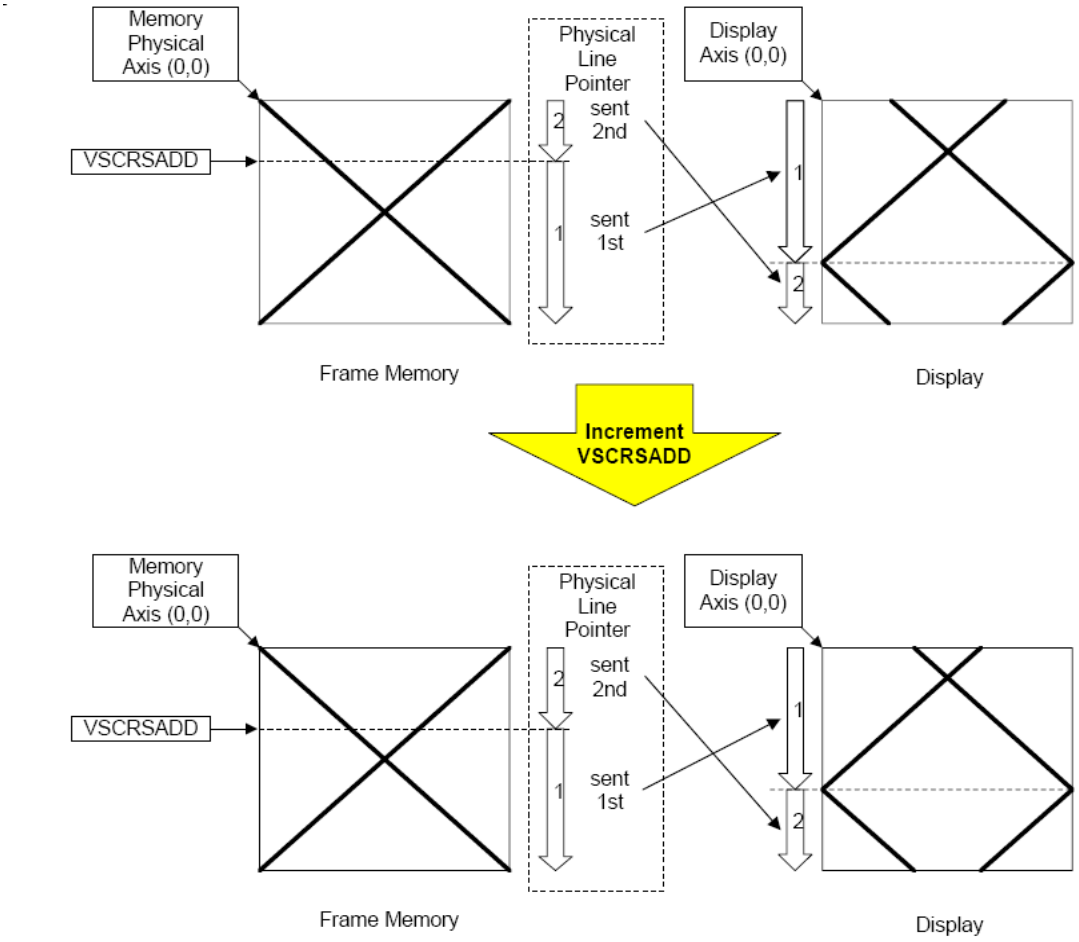
Case 2: TFA + VSA + BFA = 320 (Rolling Scrolling)

Example 2-a. When TFA = 0, VSA = 320, BFA = 0 and VSCRSADD = 40.

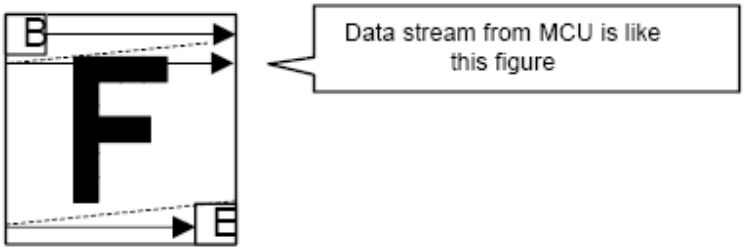
MADCTL parameter B4= "0"



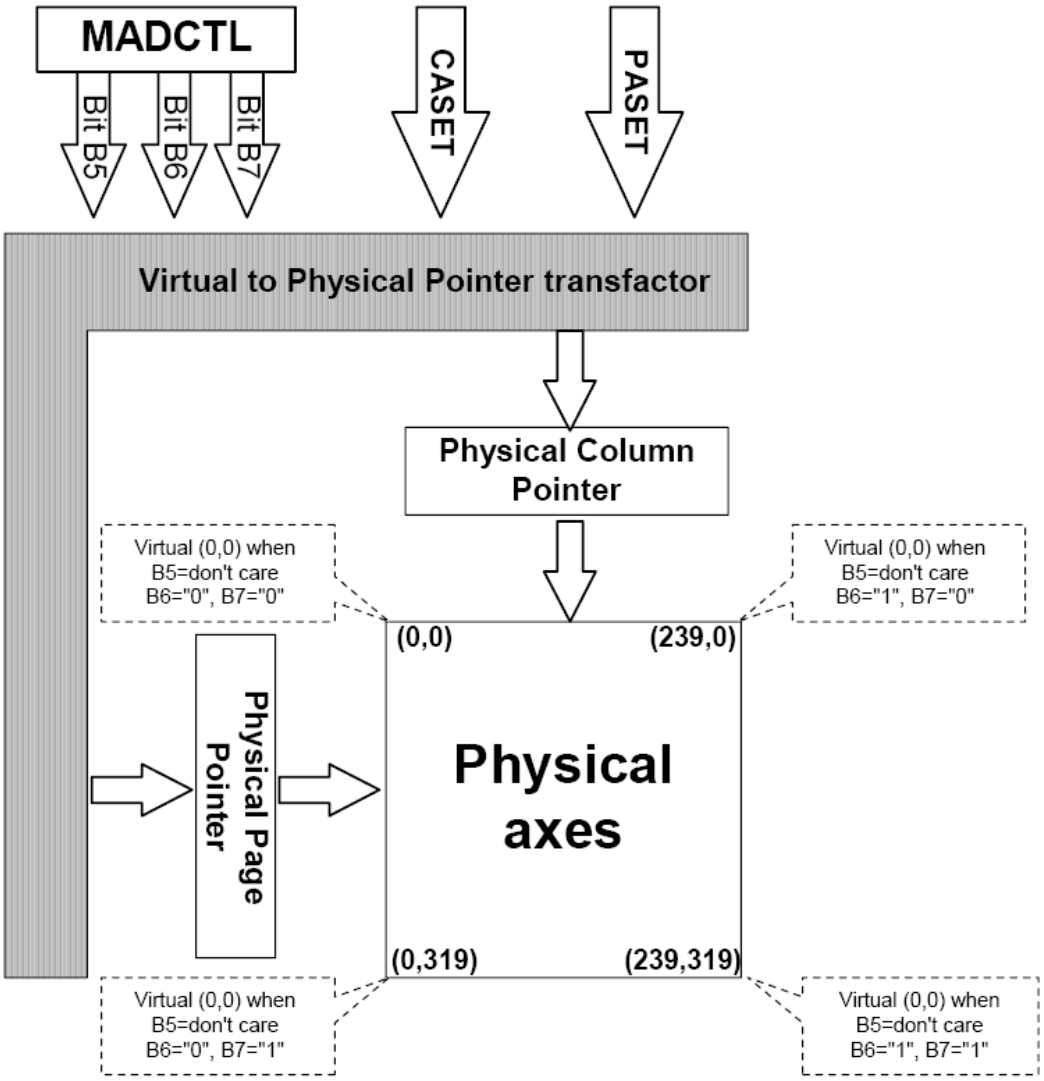
MADCTL parameter B4= "1"



10.2.3 MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” command, Bits B5, B6, B7 as described below.



For each image orientation, the controls for the column and page counters apply as below:

B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direc to(239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

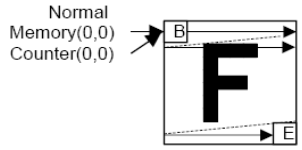
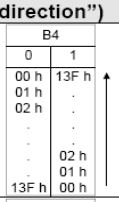
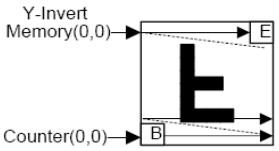
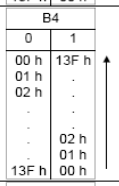
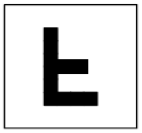
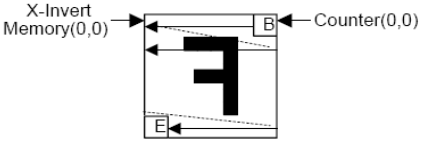
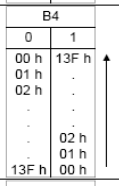
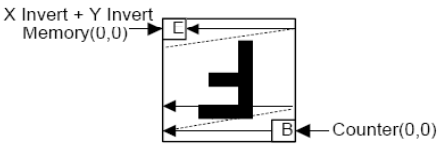
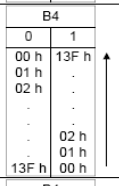
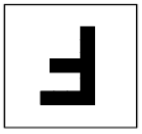
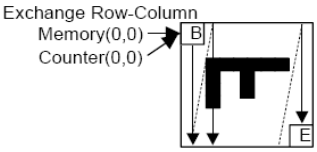
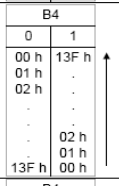
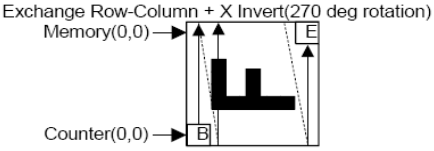
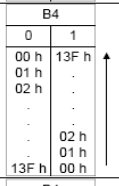
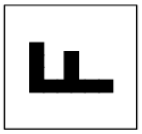
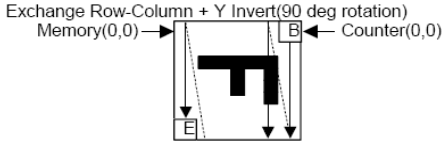
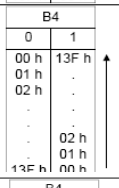
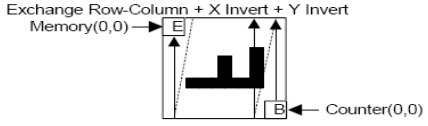
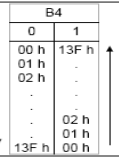
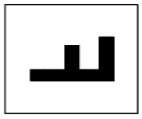
For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When MEMWR/MEMRD command is accepted	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End Column”	Return to “Start Column”	Increment by 1
The Column counter value is larger than “End Column” and the Page counter value is larger than “End Page”	Return to “Start Column”	Return to “Start Page”

Note:
Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

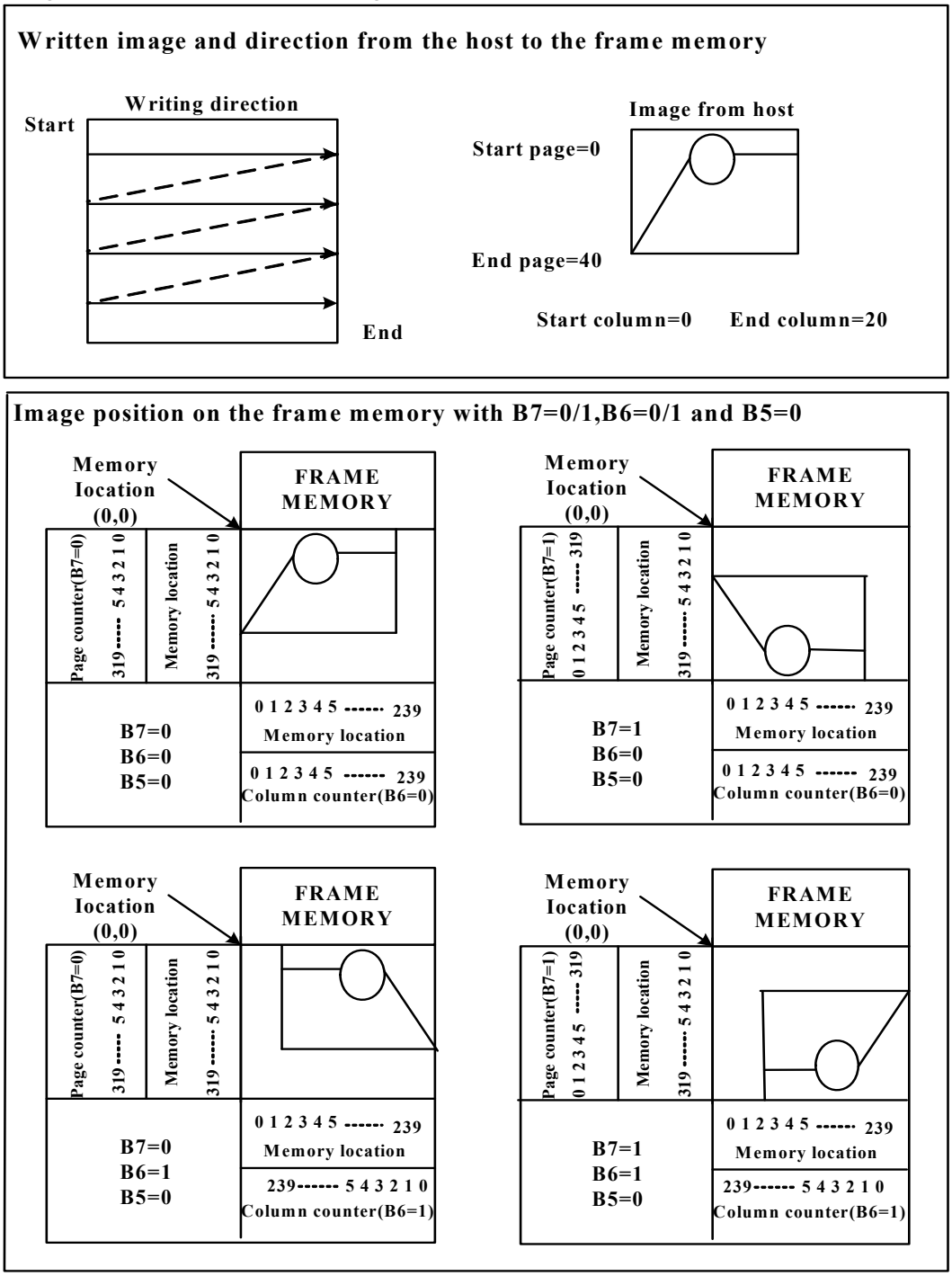
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.
This resultant image for each orientation setting is illustrated below:

B5 B6 B7 (Bits)	Image in the memory ("→" means "MCU to memory read/write direction")	B4 Bit ("→" means "RAM to display scan direction")	Image in the Display
0 0 0			
0 0 1			
0 1 0			
0 1 1			
1 0 0			
1 0 1			
1 1 0			
1 1 1			

Example for rotation with B7, B6 and B5
This example is using following values:
start page = 0, end page = 40, start column = 0 and end column = 20
= Commands: page address set (0,40) and column address set (0,20).

The sent figure is as follows and its sending order is as follows:



The sent figure is as follows and its sending order is as follows:

Written image and direction from the host to the frame memory

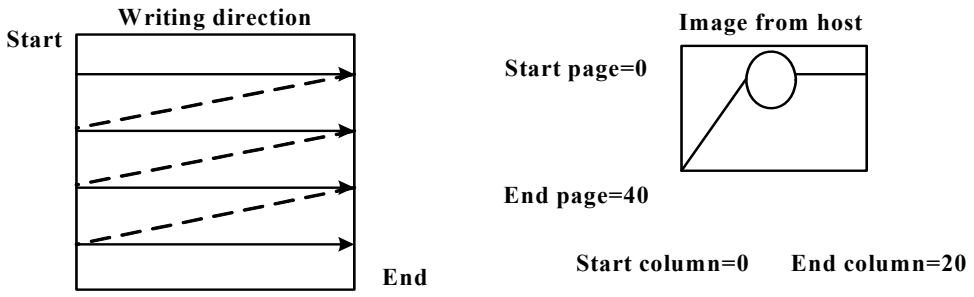
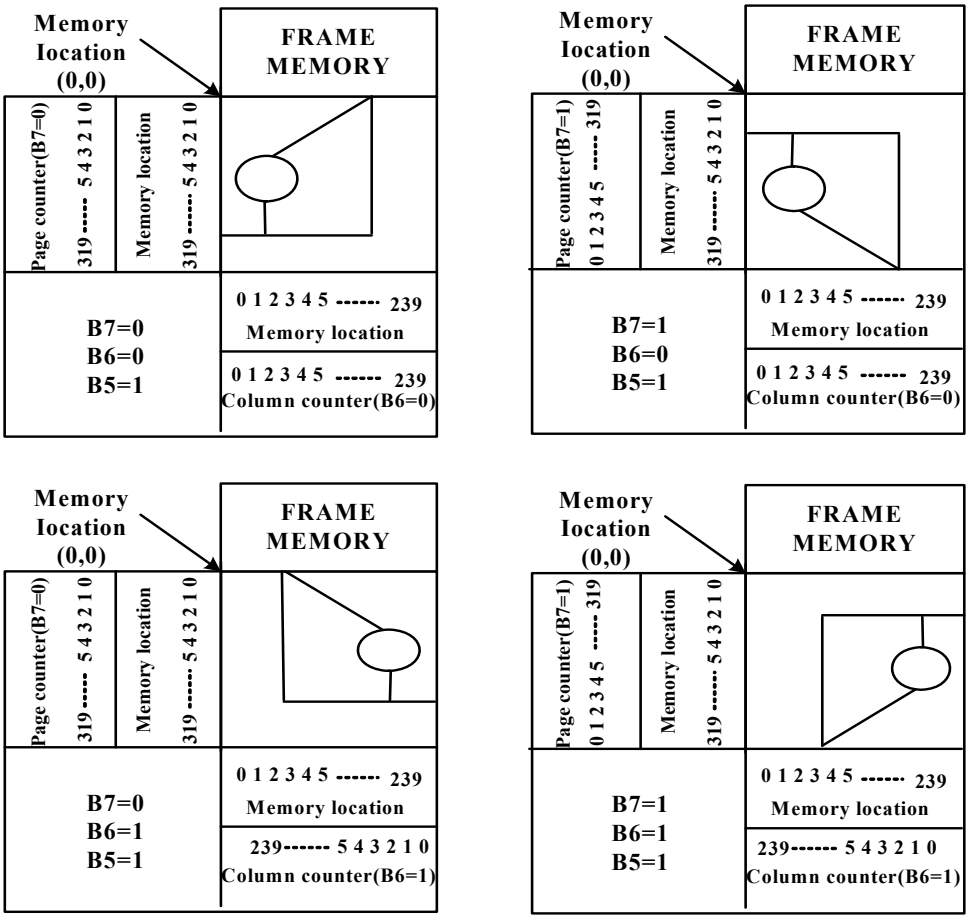


Image position on the frame memory with B7=0/1,B6=0/1 and B5=1



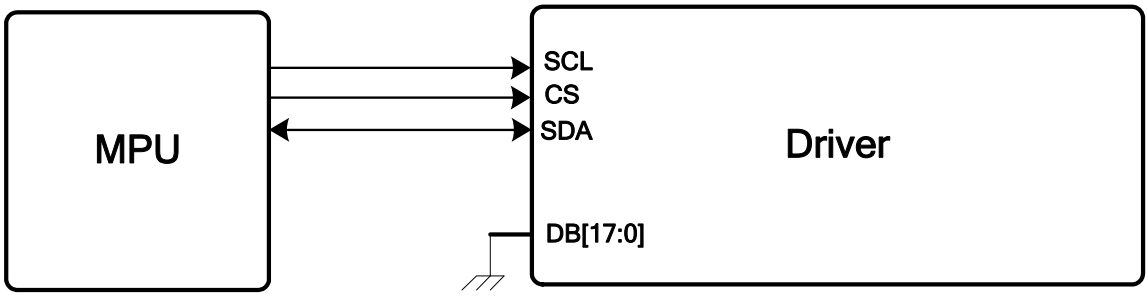
10.3 Display Data Format

NV3029G-01 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ /8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM [1:0].

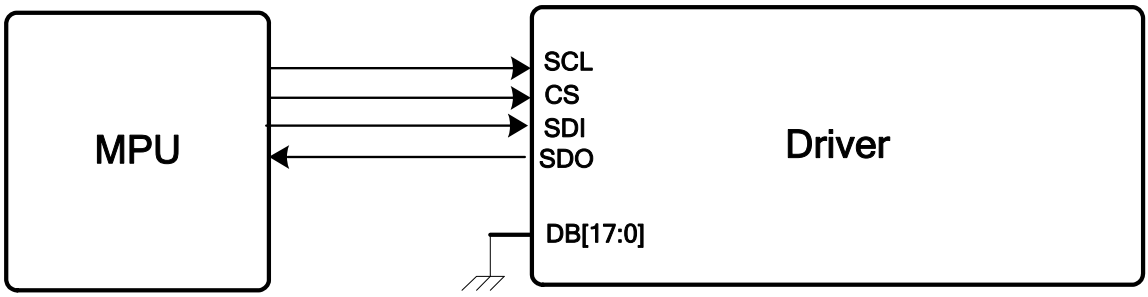
10.3.1 3-line Serial Interface

The 3-line/9-bit serial bus interface of NV3029G-01 can be used by setting external pin as IM [3:0] to "0101" for serial interface I or IM [3:0] to "1101" for serial interface II. The shown figure is the example of 3-line SPI interface.

3-line Serial interface Ⅰ

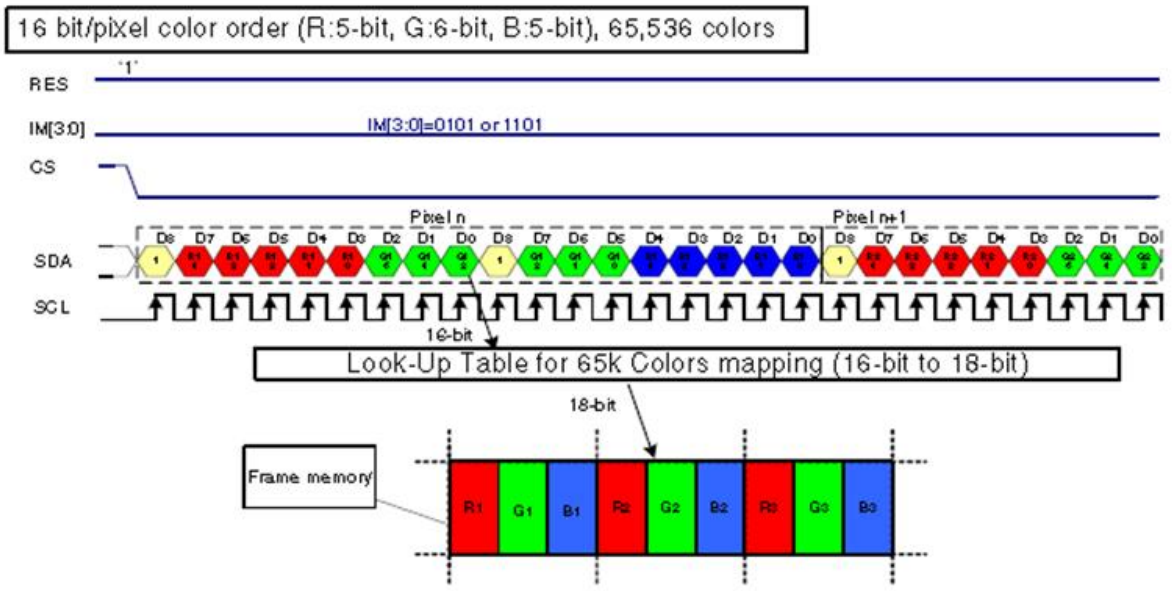


3-line Serial interface Ⅱ

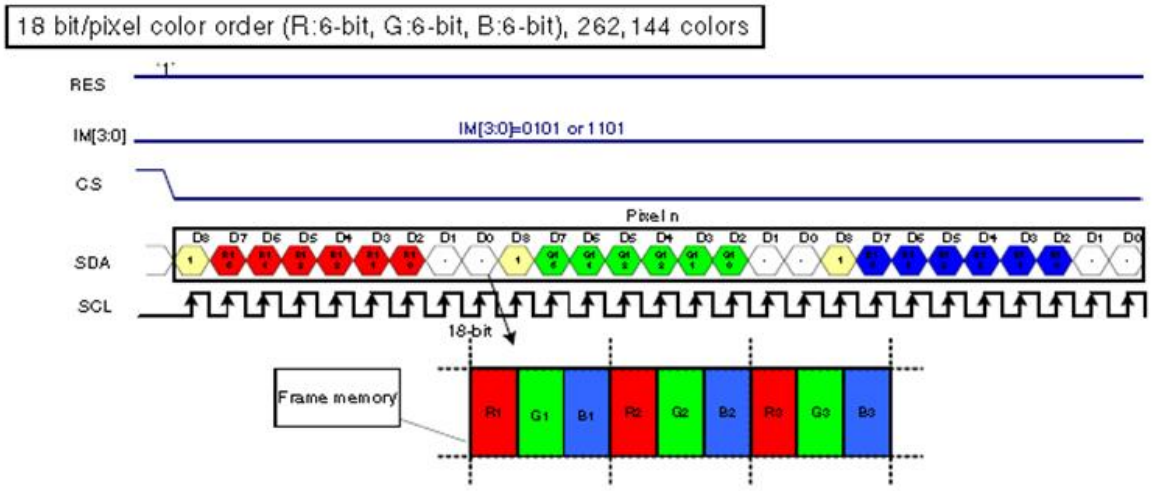


In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below:

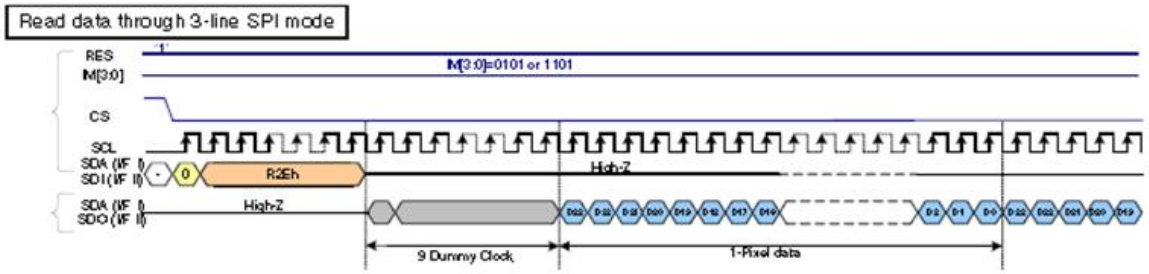
1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.



Note 1: The pixel data with 16-bit color depth information.
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
Note 4: "-" = Don't care –Can be set "0" or "1".



Note 1: The pixel data with 18-bit color depth information.
Note 2: The most significant bits are: Rx5, Gx5 and Bx5.
Note 3: The least significant bits are : Rx0, Gx0 and Bx0.
Note 4: "-" = Don't care – Can be set "0" or "1".

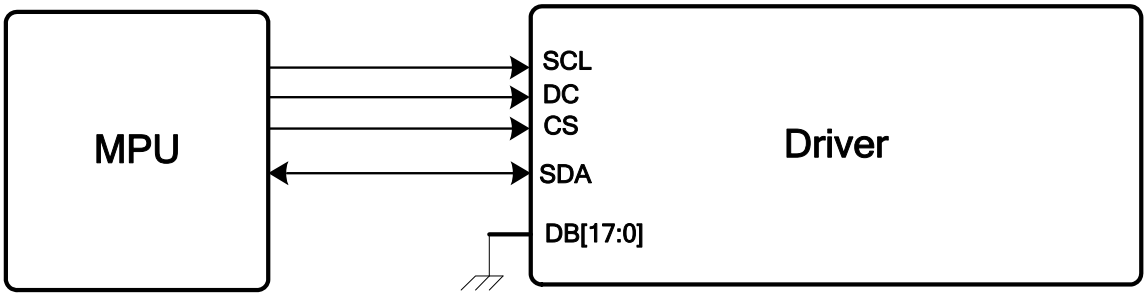


Note : "-" = Don't care – Can be set "0" or "1".

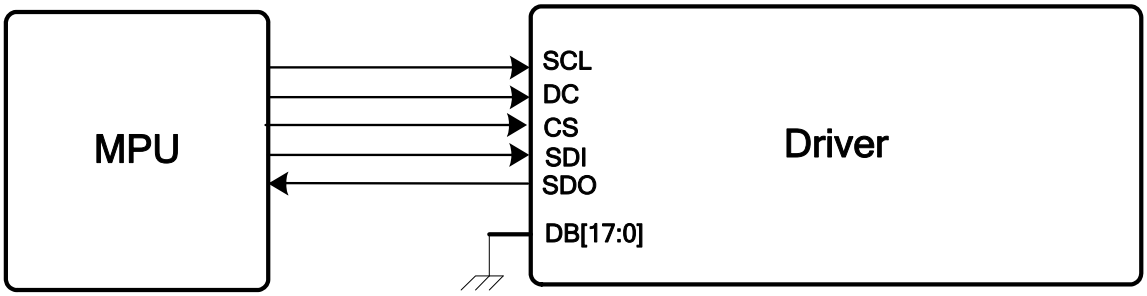
10.3.2 4-line Serial Interface

The 4-line/8-bit serial bus interface of NV3029G-01 can be used by setting external pin as IM [3:0] to "0110" for serial interface I or IM [3:0] to "1110" for serial interface II. The shown figure is the example of 4-line SPI interface.

4-line Serial interface I

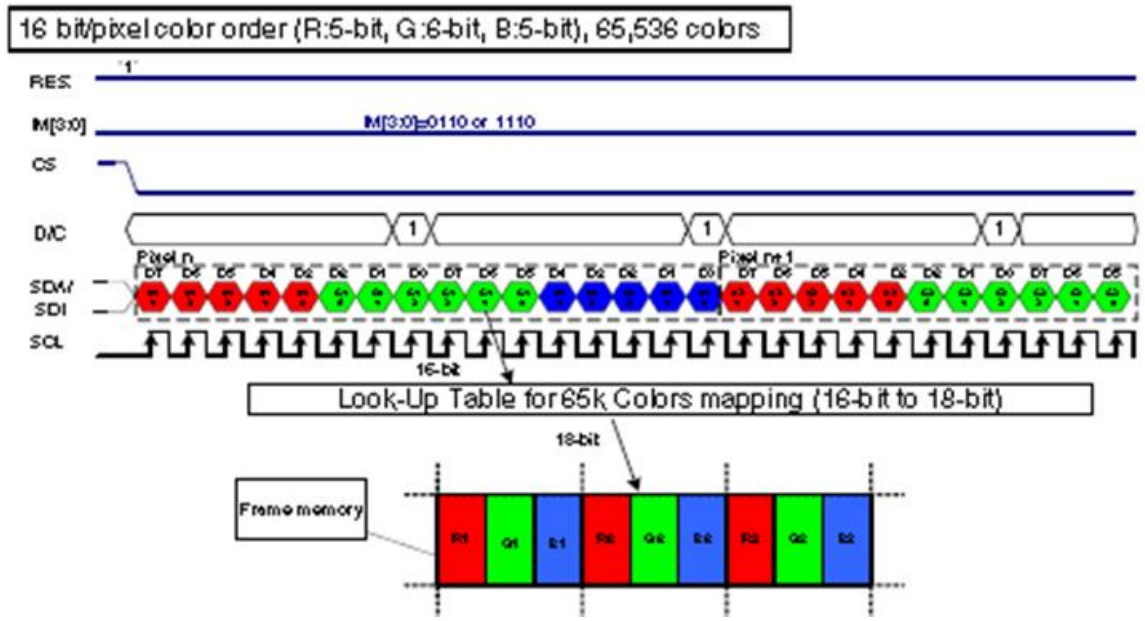


4-line Serial interface II

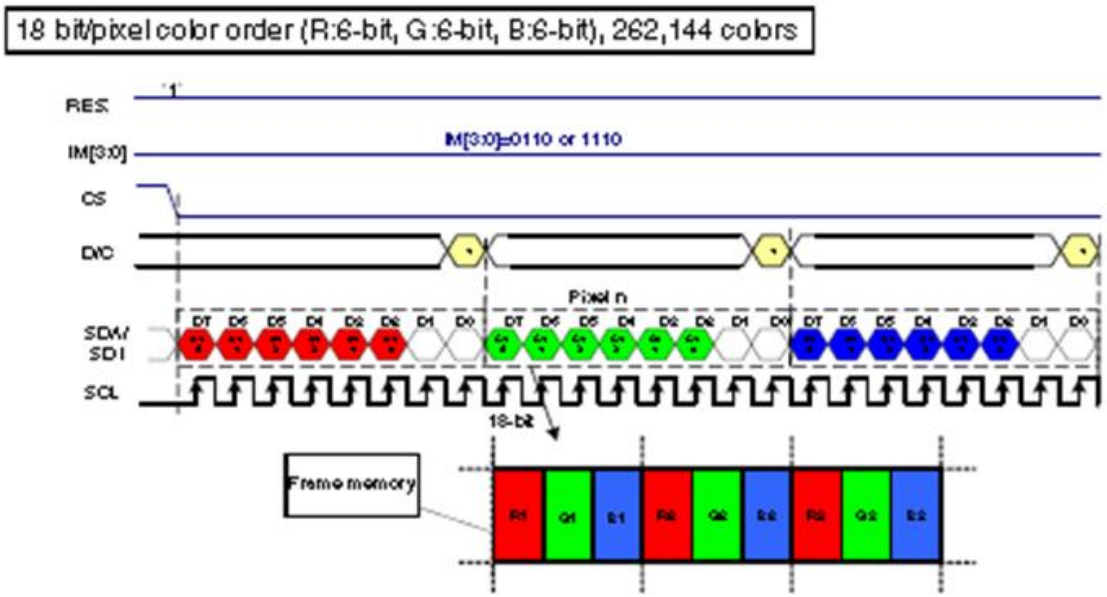


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below:

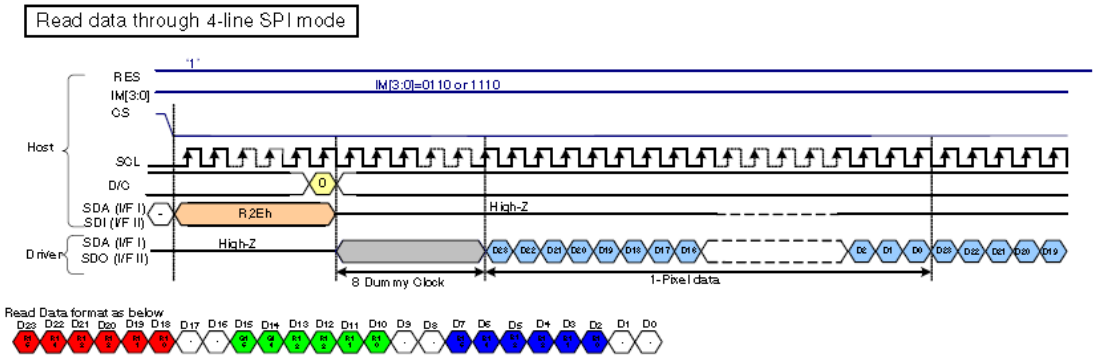
1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.



Note 1: The pixel data with 16-bit color depth information.
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
Note 4: '-'= Don't care –Can be set "0" or "1".



Note 1: The pixel data with 18-bit color depth information.
Note 2: The most significant bits are: Rx5, Gx5 and Bx5.
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
Note 4: '-'= Don't care –Can be set "0" or "1".



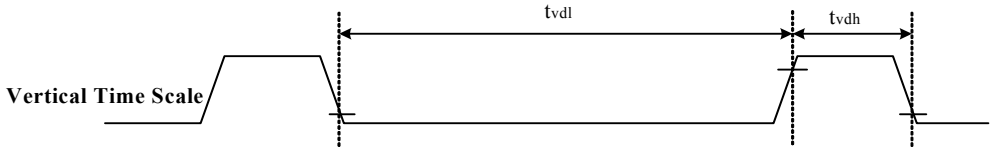
Note 1: '-'= Don't care – Can be set "0" or "1".

10.4 Tearing effect output line

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

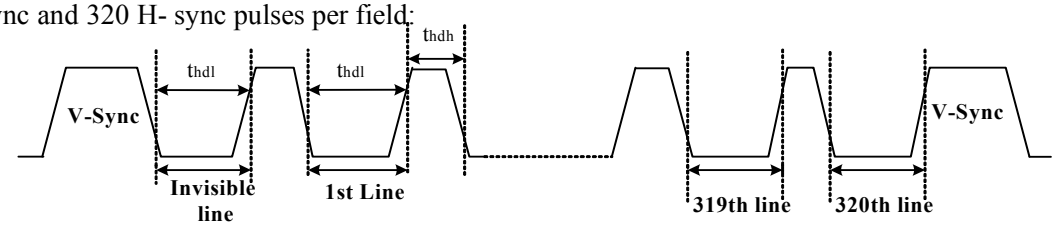
10.4.1 Tearing Effect line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync Information only:

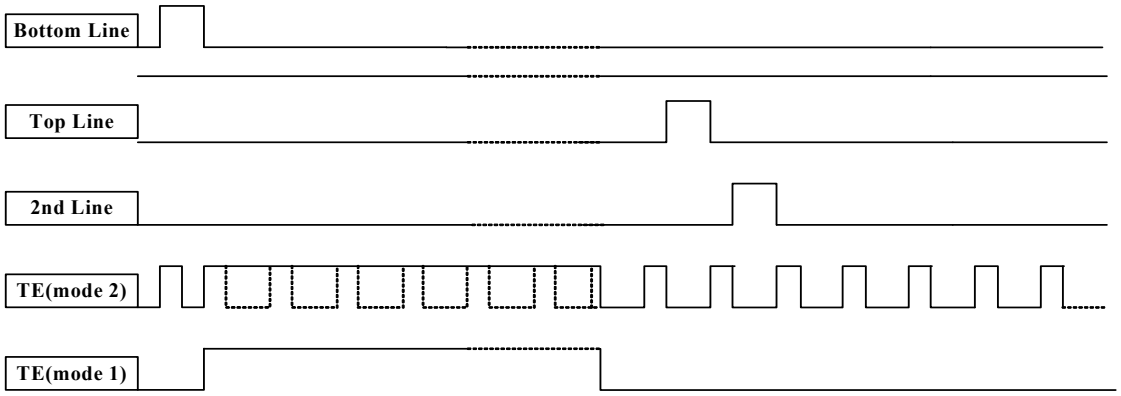


tvdh = The LCD display is not updated from the Frame Memory;
tvdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync Information, there is one V-sync and 320 H- sync pulses per field:



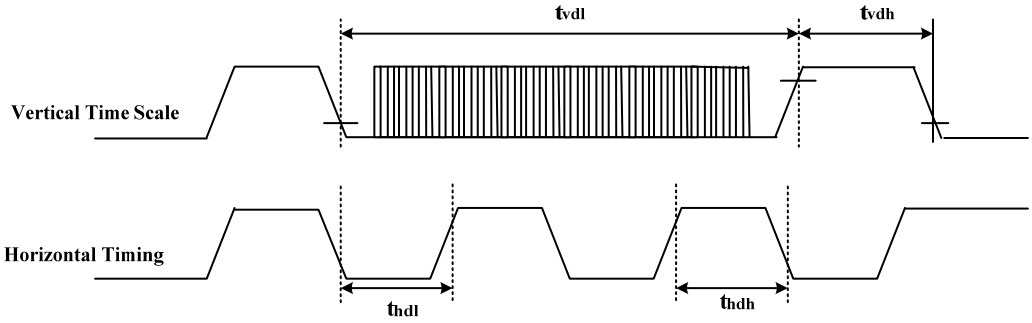
thdh = The LCD display is not updated from the Frame Memory;
thdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).



Note: During sleep in Mode,the tearing effect Output pin is active low.

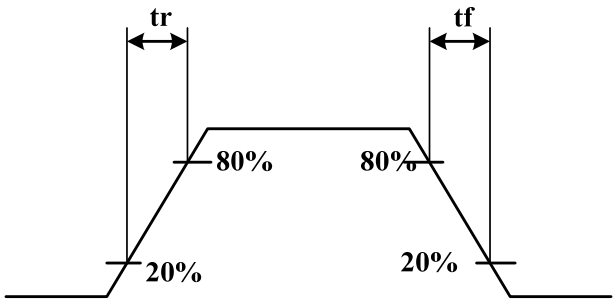
10.4.2 Tearing Effect line Timings

The Tearing Effect signal is described below:



Symbol	Parameter	Min.	Max	Unit
tvdl	Vertical Timing Low Duration	13	17	ms
tvdh	Vertical Timing High Duration	1000	1300	us
thdl	Horizontal Timing Low Duration	20	-	us
thdh	Horizontal Timing High Duration	10	500	us

Notes:
The timings in this table apply when MADCTL B4=0 and B4=1;
The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.



The tearing effect output line is fed back to the MCU and should be used to avoid tearing effect:

10.5 Power On/Off Sequence

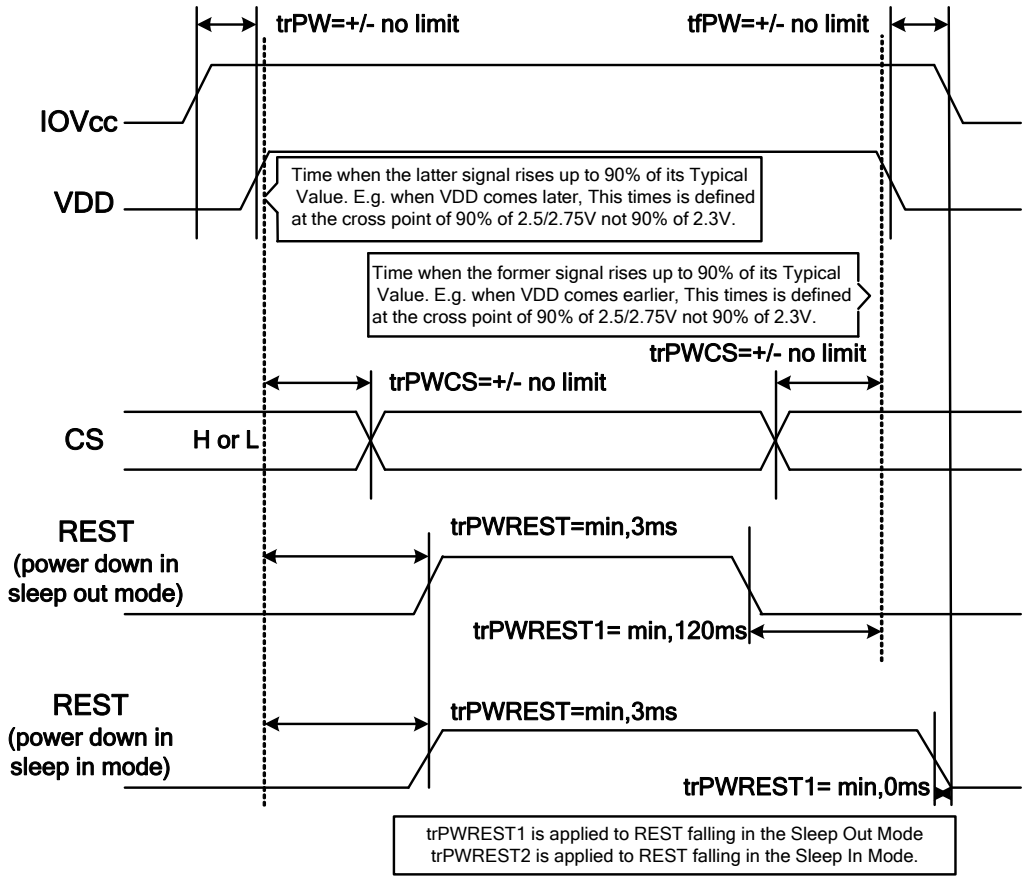
10.5.1 Power On/Off Sequence

IOVCC and VDD can be applied in any order.
VDD and IOVcc can be powered down in any order.
During power off, if LCD is in the Sleep Out Mode, VDD and IOVcc must be powered down minimum 120msec after REST has been released.
During power off, if LCD is in the Sleep In mode, IOVcc or VDD can be powered down minimum 0msec after REST has been released.
CS can be applied at any timing or can be permanently grounded. REST has priority over CS.

Notes:
1. There will be no damage to the display module if the above power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power off sequence.
4. If REST line is not held stable by host during Power On Sequence as defined in Sections "8.4.1.1 and 8.4.1.2, then it will be necessary to apply a Hardware Reset (REST) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

10.5.1.1 Case 1 – REST line is held high or Unstable by Host at Power On

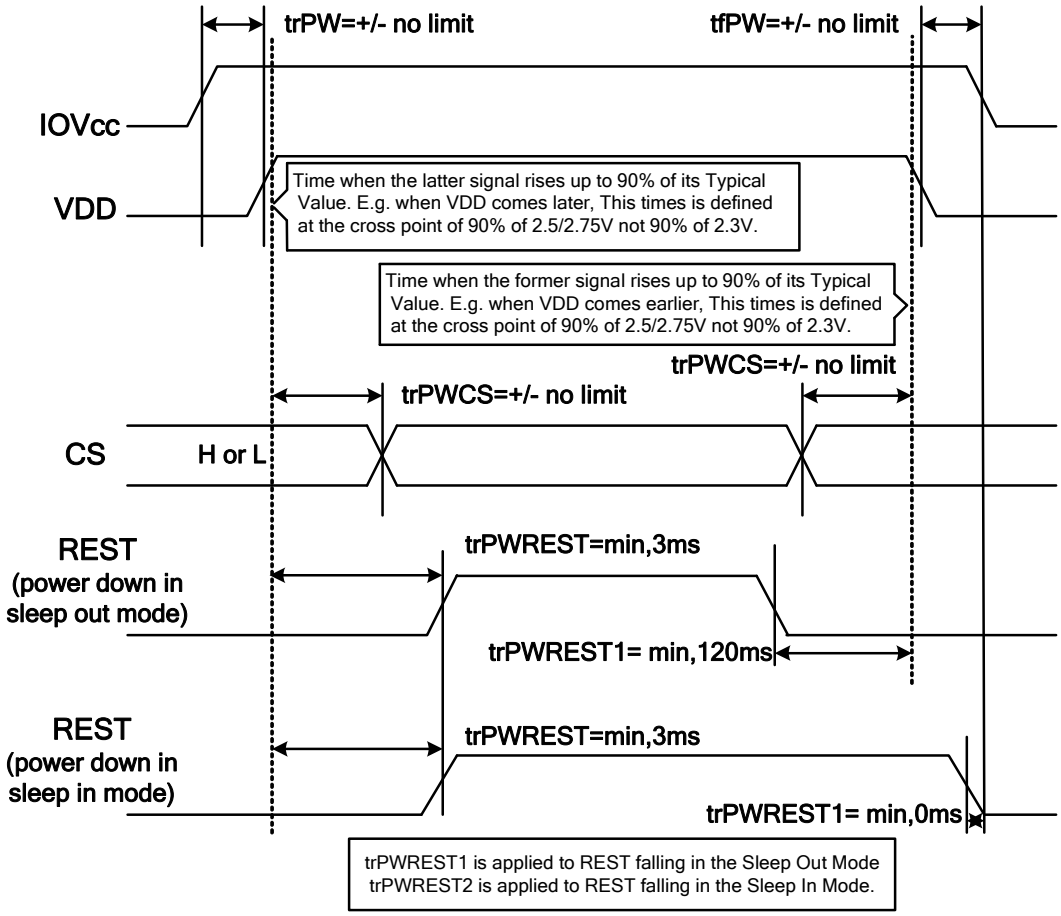
If REST line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and IOVcc have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timing herein show cross point at 50% of signal/power level.

10.5.1.2 Case 2 – REST line is held low by Host at Power On

If REST line is held Low (and stable) by the host during Power On, then the REST must be held low for minimum 3msec after both VDD and IOVcc have been applied.



Note: Unless otherwise specilied, timing herein show cross point at 50%of signal/power level.

10.6 Power Level Definition

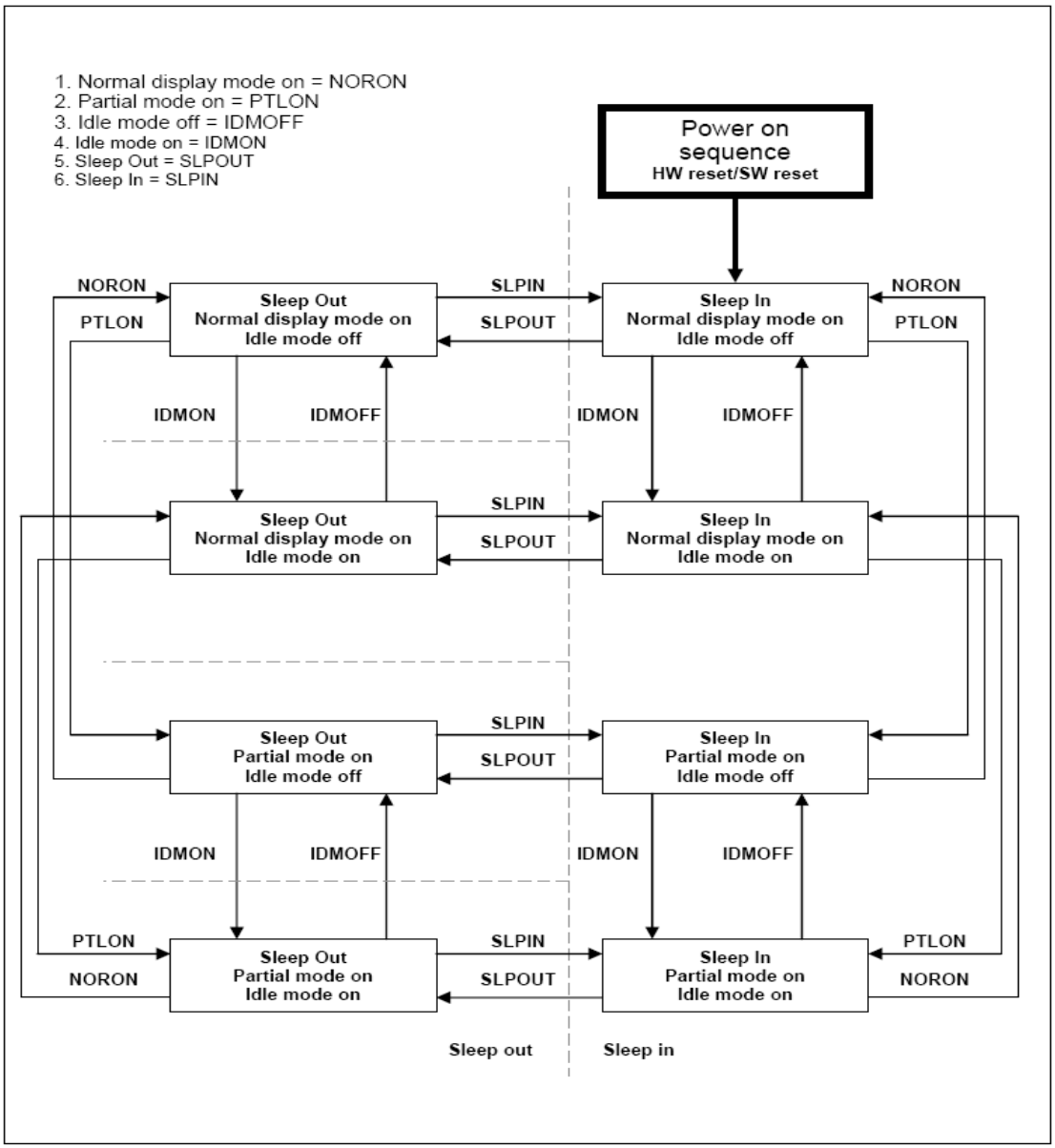
10.6.1 Power levels

6 level modes are defined they are in order of Maximum power consumption to Minimum power consumption.

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors
5. Sleep In Mode
   In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVcc power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDD and IOVcc are removed

Note:
Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

10.6.2 Power flow chart



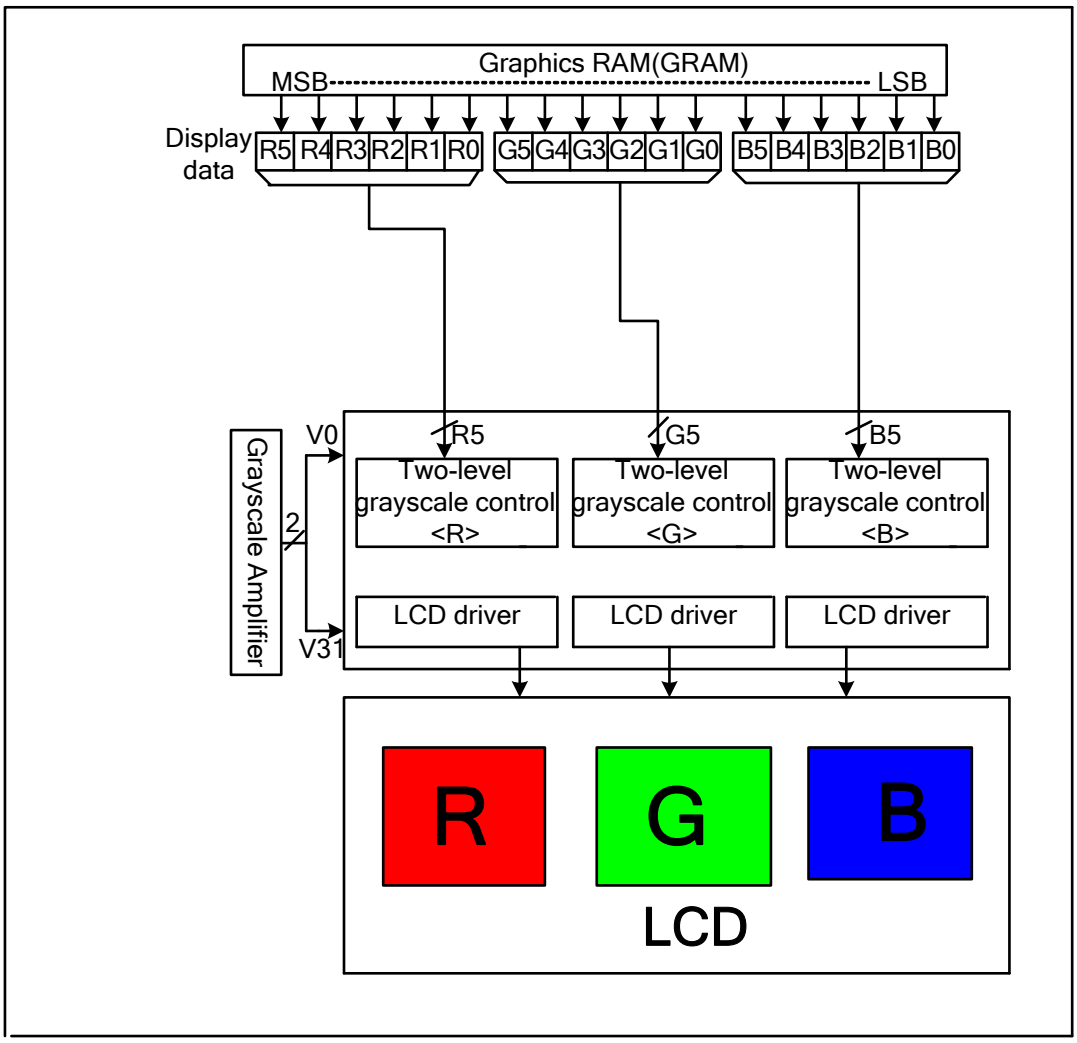
Notes:

1. There is not any abnormal visual effect when there is changing from one power mode to anther power mode.
2. There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

10.7 8-color Display Mode

The NV3029G-01 has a function to display in eight colors. In 8-color mode, the available grayscales are only V0 and V31, and the power supplies for other grayscales (V1 to V30) are cut off to reduce power consumption.

The γ- correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.
In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.



10.8 Gamma Correction

The NV3029G-01 incorporates gamma adjustment function for the 32,768-color display (32 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 14 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

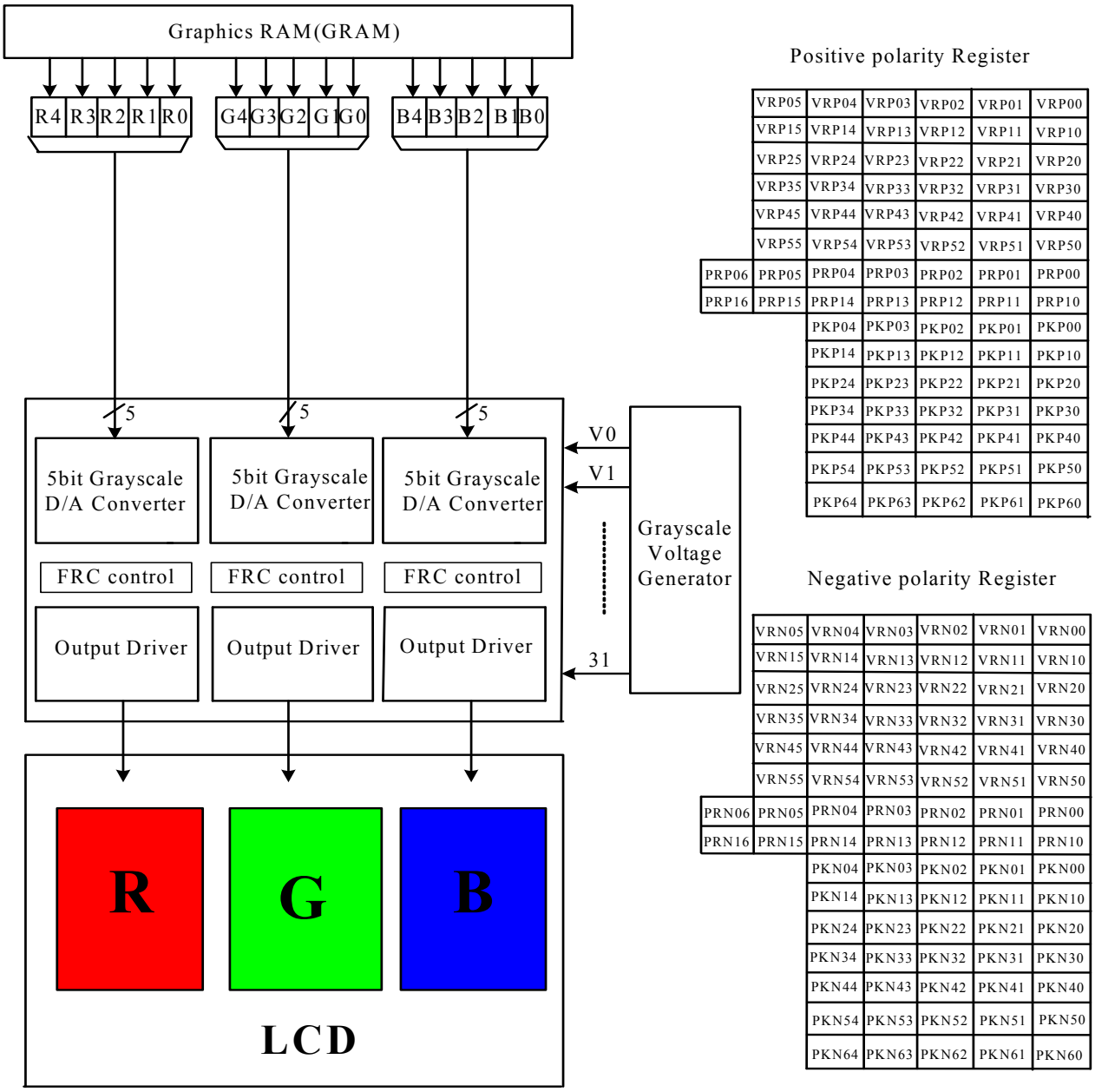


Figure 1: Grayscale control

10.8.1 Gamma-characteristics adjustment registers

This NV3029G-01 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

0- **Offset adjustment registers**

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- **Gamma center adjustment registers**

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- **Gamma macro adjustment registers**

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (VgP/N (3, 4, 10, 21, 27, 28)).

Gamma-adjustment registers			
Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor （PRP/N0）for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor （PRP/N1）for center adjustment
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 4)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 10)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 21)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 27)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 28)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 15)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor （VRP/N0）for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor （VRP/N1）for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor （VRP/N2）for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor （VRP/N3）for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor （VRP/N4）for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor （VRP/N5）for offset adjustment

10.8.2 Gamma resister stream

The block consists of one gamma resister stream. Use different register setting for positive or negative polarity. Each polarity includes fourteen gamma reference voltages. VgP/N (0, 1, 2, 3, 4, 5, 10, 21, 26, 27, 28, 29, 30, 31). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.[Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.]

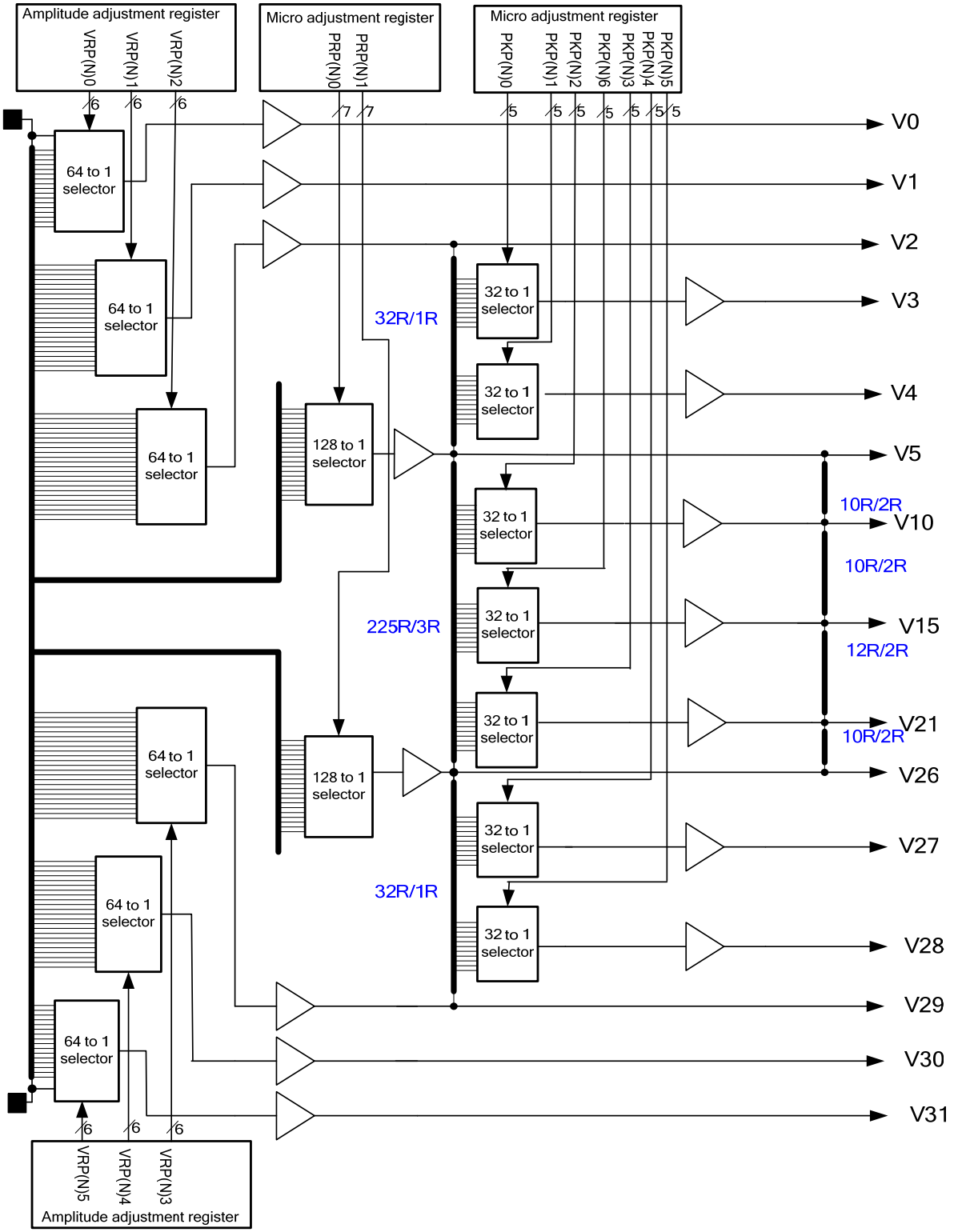


Figure 2 : Gamma resister stream and gamma reference voltage

10.8.3 Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below:

- Table 1: Offset adjustment 0 ~ 5

Register VR(P/N)0[5:0]	Resistance VR(P/N)0
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)1[5:0]	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)2[5:0]	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)3[5:0]	Resistance VR(P/N)3
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

Register VR(P/N)4[5:0]	Resistance VR(P/N)4
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

Register VR(P/N)5[5:0]	Resistance VR(P/N)5
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

- Table 2 : Center adjustment

Register PR(P/N)0[5:0]	Resistance PR(P/N)0
000000	0R
000001	2R
000010	4R
…	…
111101	250R
111110	252R
111111	254R

Register PR(P/N)1[5:0]	Resistance PR(P/N)1
000000	0R
000001	2R
000010	4R
…	…
111101	250R
111110	252R
111111	254R

10.8.4 The grayscale levels are determined by the following formulas.

Table 3 : VinP/N0

Reference Voltage	Macro Adjustment value	VinP/N0 formula
VinP/N0	VRP/N0 5-0 = 000000	Vreg1
	VRP/N0 5-0 = 000001	((450R -2R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 000010	((450R -4R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 000011	((450R -6R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 000100	((450R -8R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 000101	((450R -10R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 000110	((450R -12R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 000111	((450R -14R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001000	((450R -16R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001001	((450R -18R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001010	((450R -20R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001011	((450R -22R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001100	((450R -24R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001101	((450R -26R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001110	((450R -28R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 001111	((450R -30R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010000	((450R -32R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010001	((450R -34R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010010	((450R -36R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010011	((450R -38R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010100	((450R -40R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010101	((450R -42R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010110	((450R -44R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 010111	((450R -46R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011000	((450R -48R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011001	((450R -50R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011010	((450R -52R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011011	((450R -54R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011100	((450R -56R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011101	((450R -58R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011110	((450R -60R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 011111	((450R -62R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100000	((450R -66R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100001	((450R -70R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100010	((450R -74R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100011	((450R -78R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100100	((450R -82R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100101	((450R -86R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100110	((450R -90R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 100111	((450R -94R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101000	((450R -98R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101001	((450R -102R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101010	((450R -106R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101011	((450R -110R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101100	((450R -114R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101101	((450R -118R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101110	((450R -122R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 101111	((450R -126R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110000	((450R -130R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110001	((450R -134R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110010	((450R -138R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110011	((450R -142R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110100	((450R -146R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110101	((450R -150R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110110	((450R -154R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 110111	((450R -158R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111000	((450R -162R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111001	((450R -166R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111010	((450R -170R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111011	((450R -174R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111100	((450R -178R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111101	((450R -182R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111110	((450R -186R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N0 5-0 = 111111	((450R -190R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 4 : VinP/N1

Reference Voltage	Macro Adjustment value	VinP/N1 formula
VinP/N1	VRP/N1 5-0 = 000000	VREG1
	VRP/N1 5-0 = 000001	((450R -2R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 000010	((450R -4R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 000011	((450R -6R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 000100	((450R -8R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 000101	((450R -10R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 000110	((450R -12R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 000111	((450R -14R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001000	((450R -16R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001001	((450R -18R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001010	((450R -20R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001011	((450R -22R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001100	((450R -24R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001101	((450R -26R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001110	((450R -28R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 001111	((450R -30R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010000	((450R -32R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010001	((450R -34R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010010	((450R -36R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010011	((450R -38R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010100	((450R -40R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010101	((450R -42R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010110	((450R -44R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 010111	((450R -46R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011000	((450R -48R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011001	((450R -50R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011010	((450R -52R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011011	((450R -54R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011100	((450R -56R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011101	((450R -58R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011110	((450R -60R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 011111	((450R -62R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100000	((450R -66R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100001	((450R -70R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100010	((450R -74R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100011	((450R -78R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100100	((450R -82R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100101	((450R -86R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100110	((450R -90R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 100111	((450R -94R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101000	((450R -98R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101001	((450R -102R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101010	((450R -106R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101011	((450R -110R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101100	((450R -114R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101101	((450R -118R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101110	((450R -122R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 101111	((450R -126R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110000	((450R -130R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110001	((450R -134R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110010	((450R -138R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110011	((450R -142R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110100	((450R -146R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110101	((450R -150R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110110	((450R -154R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 110111	((450R -158R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111000	((450R -162R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111001	((450R -166R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111010	((450R -170R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111011	((450R -174R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111100	((450R -178R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111101	((450R -182R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111110	((450R -186R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N1 5-0 = 111111	((450R -190R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 5: VinP/N2

Reference Voltage	Macro Adjustment value	VinP/N2 formula
VinP/N2	VRP/N2 5-0 = 000000	(410R / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 000001	((410R -2R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 000010	((410R -4R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 000011	((410R -6R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 000100	((410R -8R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 000101	((410R -10R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 000110	((410R -12R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 000111	((410R -14R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001000	((410R -16R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001001	((410R -18R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001010	((410R -20R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001011	((410R -22R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001100	((410R -24R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001101	((410R -26R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001110	((410R -28R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 001111	((410R -30R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010000	((410R -32R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010001	((410R -34R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010010	((410R -36R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010011	((410R -38R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010100	((410R -40R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010101	((410R -42R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010110	((410R -44R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 010111	((410R -46R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011000	((410R -48R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011001	((410R -50R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011010	((410R -52R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011011	((410R -54R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011100	((410R -56R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011101	((410R -58R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011110	((410R -60R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 011111	((410R -62R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100000	((410R -66R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100001	((410R -70R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100010	((410R -74R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100011	((410R -78R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100100	((410R -82R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100101	((410R -86R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100110	((410R -90R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 100111	((410R -94R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101000	((410R -98R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101001	((410R -102R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101010	((410R -106R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101011	((410R -110R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101100	((410R -114R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101101	((410R -118R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101110	((410R -122R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 101111	((410R -126R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110000	((410R -130R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110001	((410R -134R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110010	((410R -138R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110011	((410R -142R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110100	((410R -146R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110101	((410R -150R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110110	((410R -154R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 110111	((410R -158R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111000	((410R -162R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111001	((410R -166R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111010	((410R -170R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111011	((410R -174R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111100	((410R -178R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111101	((410R -182R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111110	((410R -186R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N2 5-0 = 111111	((410R -190R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 6 : VinP/N10

Reference Voltage	Macro Adjustment value	VinP/N10 formula
VinP/N10	VRP/N3 5-0 = 000000	(230R / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 000001	((230R -4R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 000010	((230R -8R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 000011	((230R -12R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 000100	((230R -16R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 000101	((230R -20R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 000110	((230R -24R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 000111	((230R -28R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001000	((230R -32R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001001	((230R -36R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001010	((230R -40R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001011	((230R -44R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001100	((230R -48R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001101	((230R -52R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001110	((230R -56R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 001111	((230R -60R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010000	((230R -64R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010001	((230R -68R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010010	((230R -72R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010011	((230R -76R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010100	((230R -80R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010101	((230R -84R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010110	((230R -88R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 010111	((230R -92R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011000	((230R -96R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011001	((230R -100R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011010	((230R -104R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011011	((230R -108R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011100	((230R -112R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011101	((230R -116R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011110	((230R -120R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 011111	((230R -124R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100000	((230R -128R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100001	((230R -130R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100010	((230R -132R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100011	((230R -134R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100100	((230R -136R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100101	((230R -138R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100110	((230R -140R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 100111	((230R -142R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101000	((230R -144R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101001	((230R -146R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101010	((230R -148R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101011	((230R -150R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101100	((230R -152R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101101	((230R -154R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101110	((230R -156R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 101111	((230R -158R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110000	((230R -160R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110001	((230R -162R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110010	((230R -164R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110011	((230R -166R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110100	((230R -168R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110101	((230R -170R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110110	((230R -172R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 110111	((230R -174R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111000	((230R -176R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111001	((230R -178R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111010	((230R -180R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111011	((230R -182R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111100	((230R -184R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111101	((230R -186R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111110	((230R -188R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N3 5-0 = 111111	((230R -190R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 7 : VinP/N11

Reference Voltage	Macro Adjustment value	VinP/N11 formula
VinP/N11	VRP/N4 5-0 = 000000	(190R / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 000001	((190R -4R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 000010	((190R -8R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 000011	((190R -12R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 000100	((190R -16R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 000101	((190R -20R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 000110	((190R -24R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 000111	((190R -28R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001000	((190R -32R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001001	((190R -36R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001010	((190R -40R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001011	((190R -44R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001100	((190R -48R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001101	((190R -52R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001110	((190R -56R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 001111	((190R -60R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010000	((190R -64R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010001	((190R -68R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010010	((190R -72R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010011	((190R -76R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010100	((190R -80R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010101	((190R -84R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010110	((190R -88R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 010111	((190R -92R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011000	((190R -96R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011001	((190R -100R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011010	((190R -104R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011011	((190R -108R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011100	((190R -112R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011101	((190R -116R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011110	((190R -120R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 011111	((190R -124R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100000	((190R -128R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100001	((190R -130R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100010	((190R -132R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100011	((190R -134R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100100	((190R -136R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100101	((190R -138R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100110	((190R -140R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 100111	((190R -142R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101000	((190R -144R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101001	((190R -146R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101010	((190R -148R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101011	((190R -150R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101100	((190R -152R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101101	((190R -154R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101110	((190R -156R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 101111	((190R -158R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110000	((190R -160R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110001	((190R -162R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110010	((190R -164R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110011	((190R -166R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110100	((190R -168R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110101	((190R -170R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110110	((190R -172R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 110111	((190R -174R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111000	((190R -176R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111001	((190R -178R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111010	((190R -180R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111011	((190R -182R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111100	((190R -184R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111101	((190R -186R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111110	((190R -188R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N4 5-0 = 111111	VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 8 : VinP/N12

Reference Voltage	Macro Adjustment value	VinP/N12 formula
VinP/N12	VRP/N5 5-0 = 000000	(190R / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 000001	((190R -4R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 000010	((190R -8R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 000011	((190R -12R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 000100	((190R -16R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 000101	((190R -20R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 000110	((190R -24R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 000111	((190R -28R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001000	((190R -32R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001001	((190R -36R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001010	((190R -40R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001011	((190R -44R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001100	((190R -48R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001101	((190R -52R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001110	((190R -56R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 001111	((190R -60R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010000	((190R -64R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010001	((190R -68R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010010	((190R -72R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010011	((190R -76R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010100	((190R -80R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010101	((190R -84R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010110	((190R -88R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 010111	((190R -92R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011000	((190R -96R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011001	((190R -100R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011010	((190R -104R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011011	((190R -108R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011100	((190R -112R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011101	((190R -116R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011110	((190R -120R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 011111	((190R -124R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100000	((190R -128R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100001	((190R -130R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100010	((190R -132R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100011	((190R -134R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100100	((190R -136R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100101	((190R -138R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100110	((190R -140R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 100111	((190R -142R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101000	((190R -144R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101001	((190R -146R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101010	((190R -148R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101011	((190R -150R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101100	((190R -152R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101101	((190R -154R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101110	((190R -156R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 101111	((190R -158R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110000	((190R -160R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110001	((190R -162R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110010	((190R -164R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110011	((190R -166R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110100	((190R -168R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110101	((190R -170R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110110	((190R -172R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 110111	((190R -174R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111000	((190R -176R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111001	((190R -178R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111010	((190R -180R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111011	((190R -182R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111100	((190R -184R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111101	((190R -186R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111110	((190R -188R) / 450R) * (VREG1 –VGS) + VGS
	VRP/N5 5-0 = 111111	VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 9 : VinP/N4

Reference Voltage	Macro Adjustment value	VinP/N4 formula
VinP/N4	PRP/N0 6-0 = 0000000	(350R / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0000001	((350R – 2R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0000010	((350R – 4R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0000011	((350R – 6R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0000100	((350R – 8R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0000101	((350R – 10R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0000110	((350R – 12R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0000111	((350R – 14R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001000	((350R – 16R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001001	((350R – 18R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001010	((350R – 20R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001011	((350R – 22R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001100	((350R – 24R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001101	((350R – 26R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001110	((350R – 28R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0001111	((350R – 30R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010000	((350R – 32R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010001	((350R – 34R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010010	((350R – 36R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010011	((350R – 38R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010100	((350R – 40R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010101	((350R – 42R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010110	((350R – 44R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0010111	((350R – 46R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011000	((350R – 48R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011001	((350R – 50R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011010	((350R – 52R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011011	((350R – 54R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011100	((350R – 56R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011101	((350R – 58R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011110	((350R – 60R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0011111	((350R – 62R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100000	((350R – 64R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100001	((350R – 66R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100010	((350R – 68R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100011	((350R – 70R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100100	((350R – 72R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100101	((350R – 74R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100110	((350R – 76R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0100111	((350R – 78R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101000	((350R – 80R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101001	((350R – 82R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101010	((350R – 84R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101011	((350R – 86R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101100	((350R – 88R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101101	((350R – 90R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101110	((350R – 92R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0101111	((350R – 94R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110000	((350R – 96R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110001	((350R – 98R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110010	((350R – 100R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110011	((350R – 102R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110100	((350R – 104R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110101	((350R – 106R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110110	((350R – 108R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0110111	((350R – 110R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111000	((350R – 112R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111001	((350R – 114R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111010	((350R – 116R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111011	((350R – 118R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111100	((350R – 120R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111101	((350R – 122R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111110	((350R – 124R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 0111111	((350R – 126R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1000000	((350R – 128R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1000001	((350R – 130R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1000010	((350R – 132R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1000011	((350R – 134R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1000100	((350R – 136R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Reference Voltage	Macro Adjustment value	VinP/N4 formula
VinP/N4	PRP/N0 6-0 = 1000101	((350R – 138R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1000110	((350R – 140R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1000111	((350R – 142R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001000	((350R – 144R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001001	((350R – 146R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001010	((350R – 148R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001011	((350R – 150R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001100	((350R – 152R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001101	((350R – 154R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001110	((350R – 156R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1001111	((350R – 158R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010000	((350R – 160R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010001	((350R – 162R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010010	((350R – 164R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010011	((350R – 166R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010100	((350R – 168R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010101	((350R – 170R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010110	((350R – 172R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1010111	((350R -174R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011000	((350R – 176R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011001	((350R – 178R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011010	((350R – 180R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011011	((350R – 182R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011100	((350R – 184R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011101	((350R – 186R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011110	((350R – 188R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1011111	((350R – 190R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100000	((350R – 192R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100001	((350R – 194R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100010	((350R – 196R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100011	((350R – 198R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100100	((350R – 200R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100101	((350R – 202R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100110	((350R – 204R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1100111	((350R – 206R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101000	((350R – 208R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101001	((350R – 210R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101010	((350R – 212R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101011	((350R – 214R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101100	((350R – 216R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101101	((350R – 218R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101110	((350R – 220R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1101111	((350R – 222R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110000	((350R – 224R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110001	((350R – 226R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110010	((350R – 228R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110011	((350R – 230R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110100	((350R – 232R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110101	((350R – 234R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110110	((350R – 236R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1110111	((350R – 238R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111000	((350R – 240R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111001	((350R – 242R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111010	((350R – 244R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111011	((350R – 246R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111100	((350R – 248R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111101	((350R – 250R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111110	((350R – 252R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N0 6-0 = 1111111	((350R – 254R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 10 : VinP/N8

Reference Voltage	Macro Adjustment value	VinP/N8 formula
VinP/N8	PRP/N1 6-0 = 0000000	(354R / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0000001	((354R -2R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0000010	((354R -4R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0000011	((354R – 6R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0000100	((354R – 8R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0000101	((354R – 10R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0000110	((354R – 12R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0000111	((354R -14R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001000	((354R – 16R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001001	((354R – 18R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001010	((354R – 20R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001011	((354R – 22R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001100	((354R – 24R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001101	((354R – 26R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001110	((354R – 28R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0001111	((354R – 30R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010000	((354R – 32R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010001	((354R -34R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010010	((354R – 36R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010011	((354R – 38R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010100	((354R – 40R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010101	((354R – 42R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010110	((354R – 44R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0010111	((354R – 46R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011000	((354R – 48R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011001	((354R – 50R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011010	((354R – 52R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011011	((354R -54R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011100	((354R – 56R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011101	((354R – 58R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011110	((354R – 60R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0011111	((354R – 62R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100000	((354R -64R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100001	((354R – 66R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100010	((354R – 68R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100011	((354R – 70R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100100	((354R – 72R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100101	((354R – 74R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100110	((354R – 76R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0100111	((354R – 78R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101000	((354R – 80R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101001	((354R – 82R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101010	((354R -84R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101011	((354R – 86R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101100	((354R – 88R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101101	((354R – 90R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101110	((354R – 92R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0101111	((354R – 94R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110000	((354R – 96R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110001	((354R – 98R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110010	((354R – 100R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110011	((354R – 102R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110100	((354R – 104R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110101	((354R – 106R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110110	((354R – 108R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0110111	((354R – 110R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111000	((354R – 112R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111001	((354R – 114R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111010	((354R – 116R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111011	((354R – 118R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111100	((354R – 120R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111101	((354R – 122R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111110	((354R -124R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 0111111	((354R – 126R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1000000	((354R – 128R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1000001	((354R – 130R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1000010	((354R -132R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1000011	((354R – 134R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1000100	((354R – 136R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Reference Voltage	Macro Adjustment value	VinP/N8 formula
VinP/N8	PRP/N1 6-0 = 1000101	((354R – 138R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1000110	((354R – 140R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1000111	((354R – 142R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001000	((354R – 144R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001001	((354R – 146R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001010	((354R – 148R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001011	((354R – 150R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001100	((354R -152R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001101	((354R – 154R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001110	((354R – 156R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1001111	((354R – 158R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010000	((354R – 160R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010001	((354R – 162R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010010	((354R – 164R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010011	((354R – 166R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010100	((354R – 168R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010101	((354R – 170R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010110	((354R – 172R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1010111	((354R -174R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011000	((354R – 176R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011001	((354R – 178R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011010	((354R – 180R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011011	((354R – 182R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011100	((354R – 184R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011101	((354R – 186R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011110	((354R – 188R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1011111	((354R – 190R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100000	((354R – 192R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100001	((354R – 194R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100010	((354R – 196R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100011	((354R – 198R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100100	((354R – 200R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100101	((354R – 202R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100110	((354R – 204R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1100111	((354R – 206R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101000	((354R – 208R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101001	((354R – 210R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101010	((354R – 212R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101011	((354R – 214R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101100	((354R – 216R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101101	((354R – 218R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101110	((354R – 220R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1101111	((354R – 222R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110000	((354R – 224R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110001	((354R – 226R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110010	((354R – 228R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110011	((354R – 230R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110100	((354R – 232R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110101	((354R – 234R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110110	((354R – 236R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1110111	((354R – 238R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111000	((354R – 240R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111001	((354R – 242R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111010	((354R – 244R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111011	((354R – 246R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111100	((354R – 248R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111101	((354R – 250R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111110	((354R – 252R) / 450R) * (VREG1 –VGS) + VGS
	PRP/N1 6-0 = 1111111	((354R – 254R) / 450R) * (VREG1 –VGS) + VGS

Note:VGS[pin coordinate are(-932.5,-245.523);(-872.5,-245.523)]has been connected to GNDA.

Table 11: VinP/N3

Reference Voltage	Macro Adjustment value	VinP/N3 formula
VinP/N3	PKP/N0 4-0 = 00000	(31R / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01010	((31R -10R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01011	((31R -11R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01100	((31R -12R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01101	((31R -13R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01110	((31R -14R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01111	((31R -15R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10000	((31R -16R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10001	((31R -17R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10010	((31R -18R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10011	((31R -19R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10100	((31R -20R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10101	((31R -21R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10110	((31R -22R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10111	((31R -23R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11000	((31R -24R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11001	((31R -25R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11010	((31R -26R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11011	((31R -27R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11100	((31R -28R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11101	((31R -29R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11110	((31R -30R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11111	((31R -31R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4

Table 12: VinP/N3_2

Reference Voltage	Macro Adjustment value	VinP/N3_2 formula
VinP/N3_2	PKP/N1 4-0 = 00000	(31R / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01010	((31R -10R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01011	((31R -11R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01100	((31R -12R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01101	((31R -13R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01110	((31R -14R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01111	((31R -15R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10000	((31R -16R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10001	((31R -17R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10010	((31R -18R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10011	((31R -19R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10100	((31R -20R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10101	((31R -21R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10110	((31R -22R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10111	((31R -23R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11000	((31R -24R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11001	((31R -25R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11010	((31R -26R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11011	((31R -27R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11100	((31R -28R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11101	((31R -29R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11110	((31R -30R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11111	((31R -31R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4

Table 13: VinP/N5

Reference Voltage	Macro Adjustment value	VinP/N5 formula
VinP/N5	PKP/N2 4-0 = 00000	(195R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00001	((195R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00010	((195R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00011	((195R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00100	((195R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00101	((195R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00110	((195R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00111	((195R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01000	((195R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01001	((195R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01010	((195R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01011	((195R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01100	((195R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01101	((195R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01110	((195R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01111	((195R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10000	((195R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10001	((195R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10010	((195R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10011	((195R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10100	((195R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10101	((195R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10110	((195R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10111	((195R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11000	((195R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11001	((195R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11010	((195R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11011	((195R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11100	((195R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11101	((195R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11110	((195R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11111	((195R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 13a: VinP/N6

Reference Voltage	Macro Adjustment value	VinP/N5 formula
VinP/N6	PKP/N6 4-0 = 00000	(159R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00001	((159R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00010	((159R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00011	((159R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00100	((159R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00101	((159R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00110	((159R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00111	((159R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01000	((159R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01001	((159R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01010	((159R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01011	((159R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01100	((159R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01101	((159R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01110	((159R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01111	((159R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10000	((159R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10001	((159R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10010	((159R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10011	((159R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10100	((159R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10101	((159R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10110	((159R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10111	((159R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11000	((159R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11001	((159R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11010	((159R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11011	((159R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11100	((159R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11101	((159R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11110	((159R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11111	((159R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 14: VinP/N7

Reference Voltage	Macro Adjustment value	VinP/N7 formula
VinP/N7	PKP/N3 4-0 = 00000	(123R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00001	((123R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00010	((123R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00011	((123R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00100	((123R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00101	((123R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00110	((123R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00111	((123R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01000	((123R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01001	((123R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01010	((123R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01011	((123R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01100	((123R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01101	((123R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01110	((123R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01111	((123R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10000	((123R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10001	((123R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10010	((123R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10011	((123R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10100	((123R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10101	((123R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10110	((123R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10111	((123R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11000	((123R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11001	((123R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11010	((123R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11011	((123R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11100	((123R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11101	((123R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11110	((123R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11111	((123R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 15: VinP/N9_2

Reference Voltage	Macro Adjustment value	VinP/N9_2 formula
VinP/N9_2	PKP/N4 4-0 = 00000	(31R / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00001	((31R -1R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00010	((31R -2R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00011	((31R -3R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00100	((31R -4R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00101	((31R -5R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00110	((31R -6R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00111	((31R -7R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01000	((31R -8R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01001	((31R -9R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01010	((31R -10R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01011	((31R -11R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01100	((31R -12R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01101	((31R -13R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01110	((31R -14R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01111	((31R -15R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10000	((31R -16R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10001	((31R -17R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10010	((31R -18R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10011	((31R -19R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10100	((31R -20R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10101	((31R -21R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10110	((31R -22R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10111	((31R -23R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11000	((31R -24R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11001	((31R -25R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11010	((31R -26R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11011	((31R -27R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11100	((31R -28R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11101	((31R -29R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11110	((31R -30R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11111	((31R -31R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10

Table 16: VinP/N9

Reference Voltage	Macro Adjustment value	VinP/N9 formula
VinP/N9	PKP/N5 4-0 = 00000	(31R / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00001	((31R -1R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00010	((31R -2R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00011	((31R -3R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00100	((31R -4R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00101	((31R -5R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00110	((31R -6R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00111	((31R -7R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01000	((31R -8R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01001	((31R -9R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01010	((31R -10R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01011	((31R -11R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01100	((31R -12R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01101	((31R -13R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01110	((31R -14R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01111	((31R -15R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10000	((31R -16R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10001	((31R -17R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10010	((31R -18R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10011	((31R -19R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10100	((31R -20R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10101	((31R -21R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10110	((31R -22R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10111	((31R -23R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11000	((31R -24R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11001	((31R -25R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11010	((31R -26R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11011	((31R -27R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11100	((31R -28R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11101	((31R -29R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11110	((31R -30R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11111	((31R -31R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10

Table 17:Positive polarity

Grayscale voltage	Formula
v0	VinP0
v1	VinP1
v2	VinP2
v3	VinP3
v4	VinP3_2
v5	VinP4
v6	VinP5+(VinP4-VinP5)*(8R/10R)
v7	VinP5+(VinP4-VinP5)*(6R/10R)
v8	VinP5+(VinP4-VinP5)*(4R/10R)
v9	VinP5+(VinP4-VinP5)*(2R/10R)
v10	VinP5
v11	VinP6+(VinP5-VinP6)*(8R/10R)
v12	VinP6+(VinP5-VinP6)*(6R/10R)
v13	VinP6+(VinP5-VinP6)*(4R/10R)
v14	VinP6+(VinP5-VinP6)*(2R/10R)
v15	VinP6
v16	VinP7+(VinP6-VinP7)*(10R/12R)
v17	VinP7+(VinP6-VinP7)*(8R/12R)
v18	VinP7+(VinP6-VinP7)*(6R/12R)
v19	VinP7+(VinP6-VinP7)*(4R/12R)
v20	VinP7+(VinP6-VinP7)*(2R/12R)
v21	VinP7
v22	VinP8+(VinP7-VinP8)*(8R/10R)
v23	VinP8+(VinP7-VinP8)*(6R/10R)
v24	VinP8+(VinP7-VinP8)*(4R/10R)
v25	VinP8+(VinP7-VinP8)*(2R/10R)
v26	VinP8
v27	VinP9_2
v28	VinP9
v29	VinP10
v30	VinP11
v31	VinP12

Table 18: Negative polarity

Grayscale voltage	Formula
v31	VinN0
v30	VinN1
v29	VinN2
v28	VinN3
v27	VinN3_2
v26	VinN4
v25	VinN5+(VinN4-VinN5)*(8R/10R)
v24	VinN5+(VinN4-VinN5)*(6R/10R)
v23	VinN5+(VinN4-VinN5)*(4R/10R)
v22	VinN5+(VinN4-VinN5)*(2R/10R)
v21	VinN5
v20	VinN6+(VinN5-VinN6)*(8R/10R)
v19	VinN6+(VinN5-VinN6)*(6R/10R)
v18	VinN6+(VinN5-VinN6)*(4R/10R)
v17	VinN6+(VinN5-VinN6)*(2R/10R)
v16	VinN6
v15	VinN7+(VinN6-VinN7)*(10R/12R)
v14	VinN7+(VinN6-VinN7)*(8R/12R)
v13	VinN7+(VinN6-VinN7)*(6R/12R)
v12	VinN7+(VinN6-VinN7)*(4R/12R)
v11	VinN7+(VinN6-VinN7)*(2R/12R)
v10	VinN7
v9	VinN8+(VinN7-VinN8)*(8R/10R)
v8	VinN8+(VinN7-VinN8)*(6R/10R)
v7	VinN8+(VinN7-VinN8)*(4R/10R)
v6	VinN8+(VinN7-VinN8)*(2R/10R)
v5	VinN8
v4	VinN9_2
v3	VinN9
v2	VinN10
v1	VinN11
v0	VinN12

10.8.5 Relationship between GRAM Data and Output Level

("Normally White Panel",GRAM data=0)

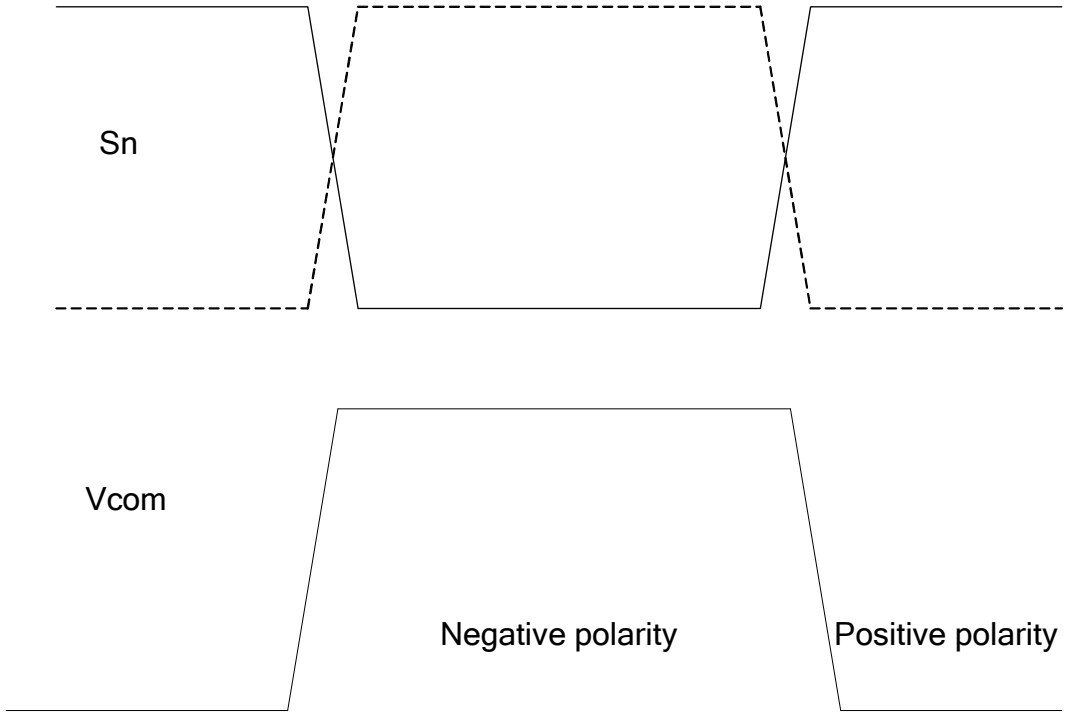
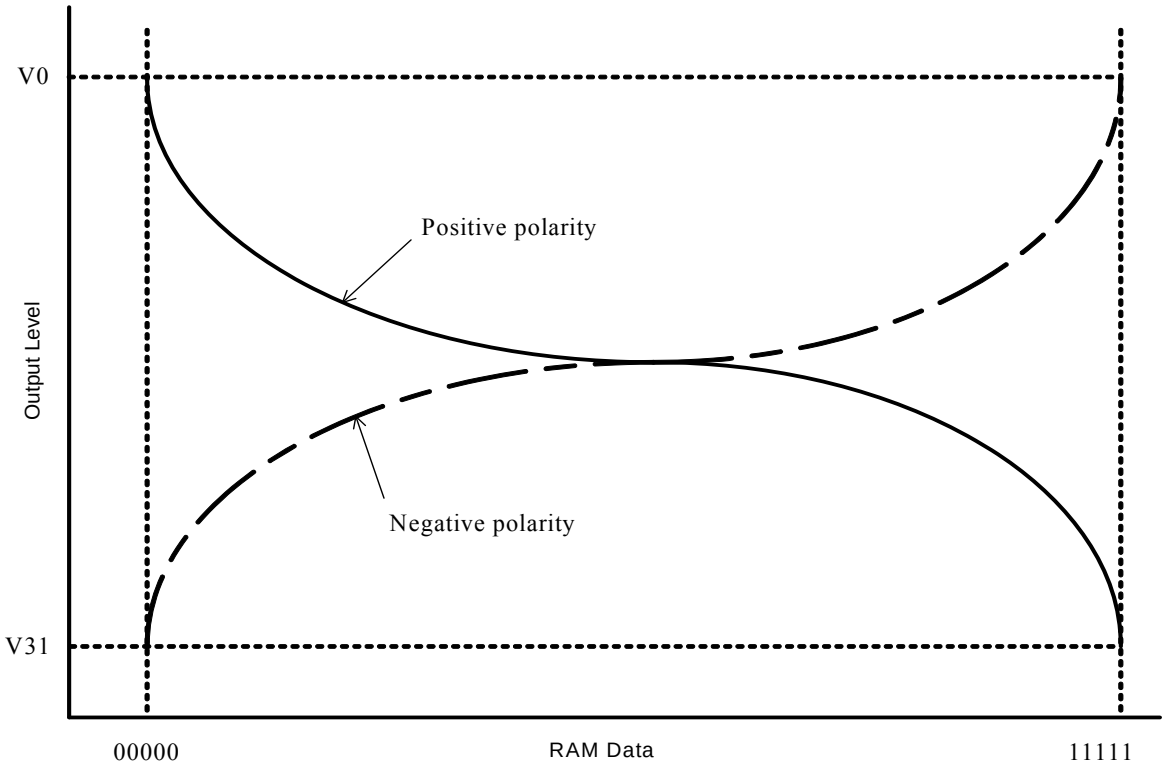


Figure 3: Relationship between source output and Vcom

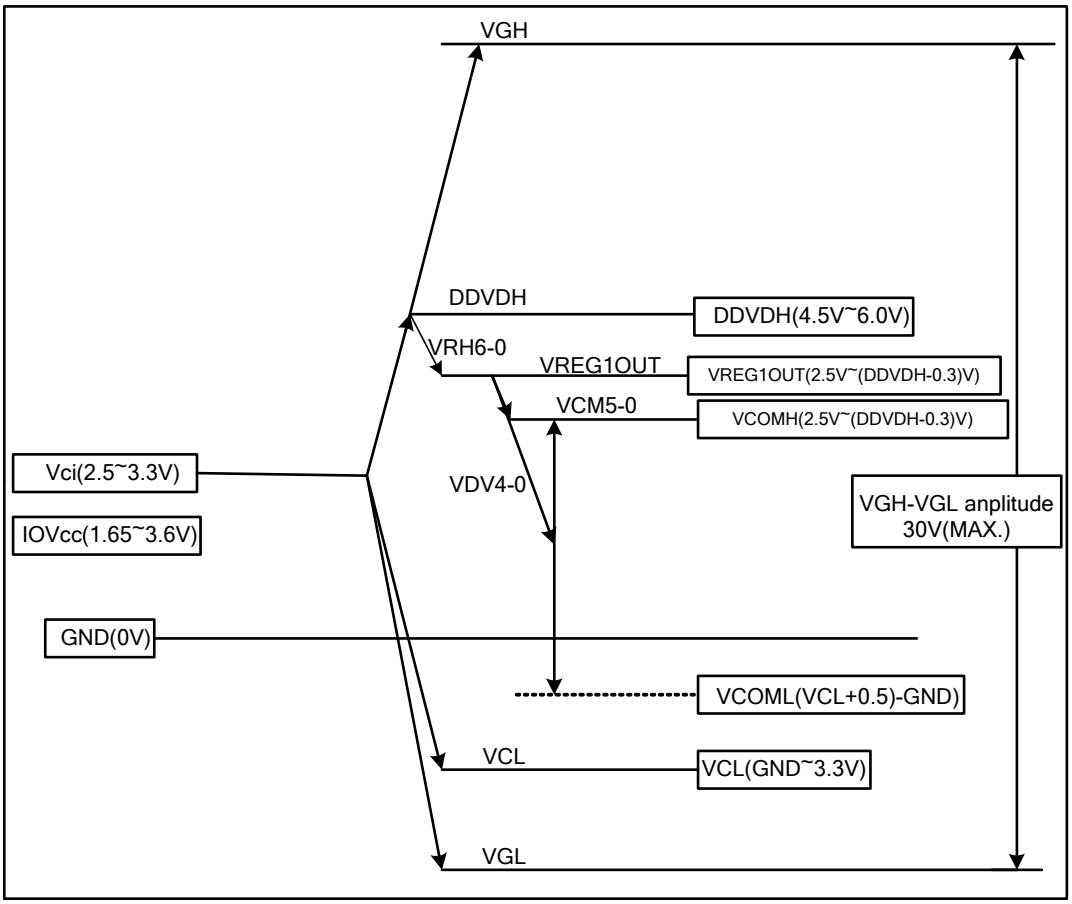


(Same characteristic for each RGB)

Figure 4: Relationship between GRAM data and output level (normal white panel)

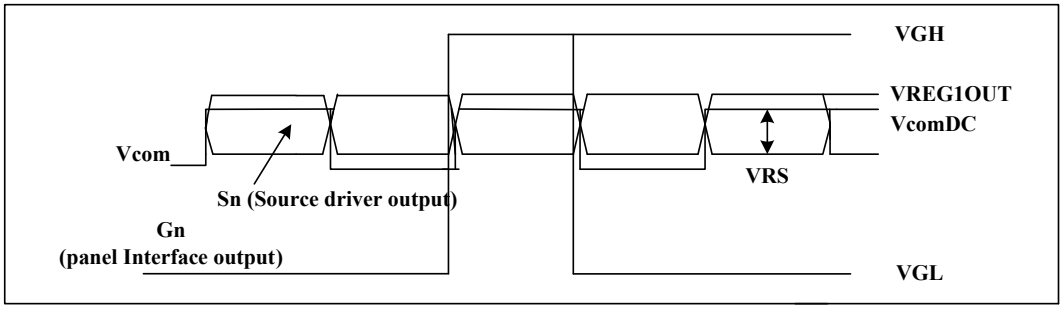
10.9 Voltage Generation

The pattern diagram of voltage setting and an example of waveforms of NV3029G-01 are as follows.



Note:

The DDVDH, VGH and VGL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. The voltage levels in the following relationships (DDVDH – VREG1OUT) 0.5V and (VCOMDC – GND) 0.5V are the actual voltage levels. When the alternating cycle of VCOM is set high (e.g., the polarity inverts at every line cycle), current consumption will increase. In this case, check the voltage before use.



10.10 Reset

10.10.1 Registers

The registers that are initialized are listed below.

	After Power On	After H/W Reset	After S/W Reset
Frame Memory	Random	No Change	No Change
Sleep	In	In	In
Display mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000h	0000h	0000h
Column End Address	00Efh	00Efh	If MADCTL's B5=0:00Efh If MADCTL's B5=1:013Fh
Page Start Address	0000h	0000h	0000h
Page End Address	013Fh	013Fh	If MADCTL's B5=0:013Fh If MADCTL's B5=1:00Efh
Partial Area Start	0000h	0000h	0000h
Partial Area End	013Fh	013Fh	013Fh
Memory Data Access Control	00h	00h	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	06h	06h	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
FMARK Output Line	Off	Off	Off
FMARK Line Mode	Mode 1(3)	Mode 1(3)	Mode 1(3)

Note:

1. There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.
2. After Powered-on Reset finishes within 10us after both VDD & IOVcc are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Sync Information only.

10.10.2 Module Input/Output Pins

10.10.2.1 Output Pins, I/O Pins

	After Power On	After Hardware Reset	After Software Reset
FMARK Line	High	High	High
D[15…0](output driver)	High-Z(inactive)	High-Z(inactive)	High-Z(inactive)

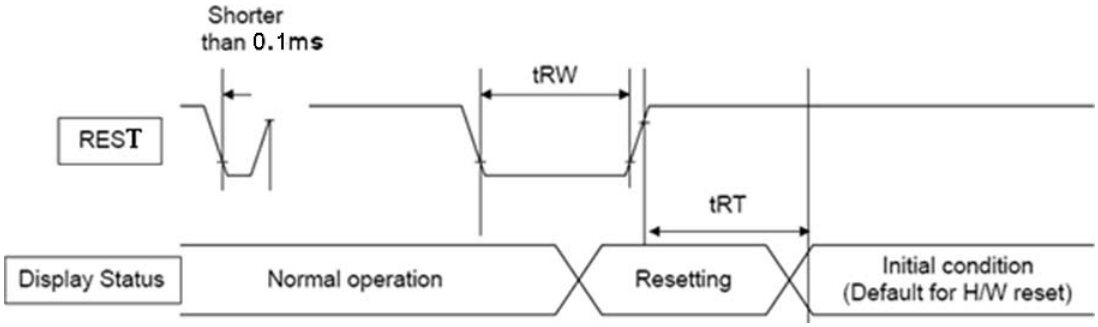
Note:

There will be no output from D[15…0] during Power On/Off sequence, Hardware Reset and Software Reset.

10.10.2.2 Input Pins

	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off
REST	See 10.5	Input valid	Input valid	Input valid	See 10.5
CS	Input valid	Input valid	Input valid	Input valid	Input valid
DC	Input valid	Input valid	Input valid	Input valid	Input valid
IM0	Input valid	Input valid	Input valid	Input valid	Input valid
WR	Input valid	Input valid	Input valid	Input valid	Input valid
RD	Input valid	Input valid	Input valid	Input valid	Input valid
D[15…0] (Input driver)	Input valid	Input valid	Input valid	Input valid	Input valid

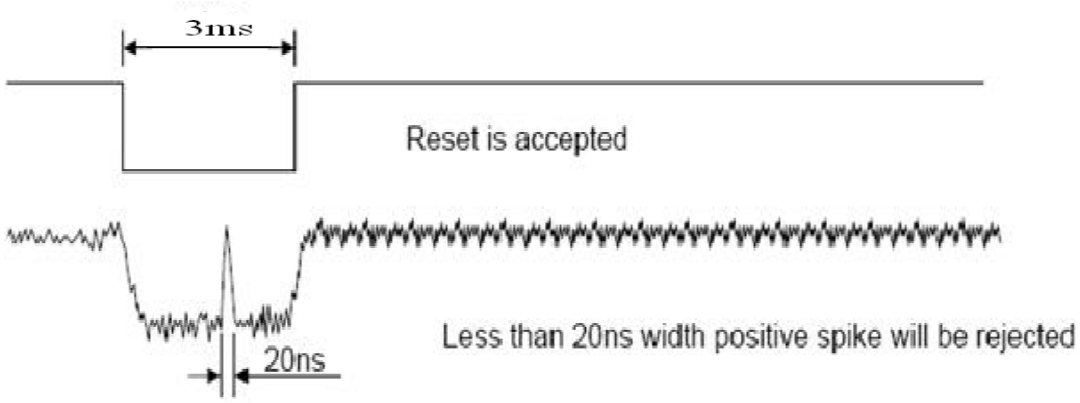
10.10.2.3 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESET	tRW	Reset pulse duration	0.1		ms
	tRT	Reset cancel		5(note 5)	ms
				120(note 6,7)	ms

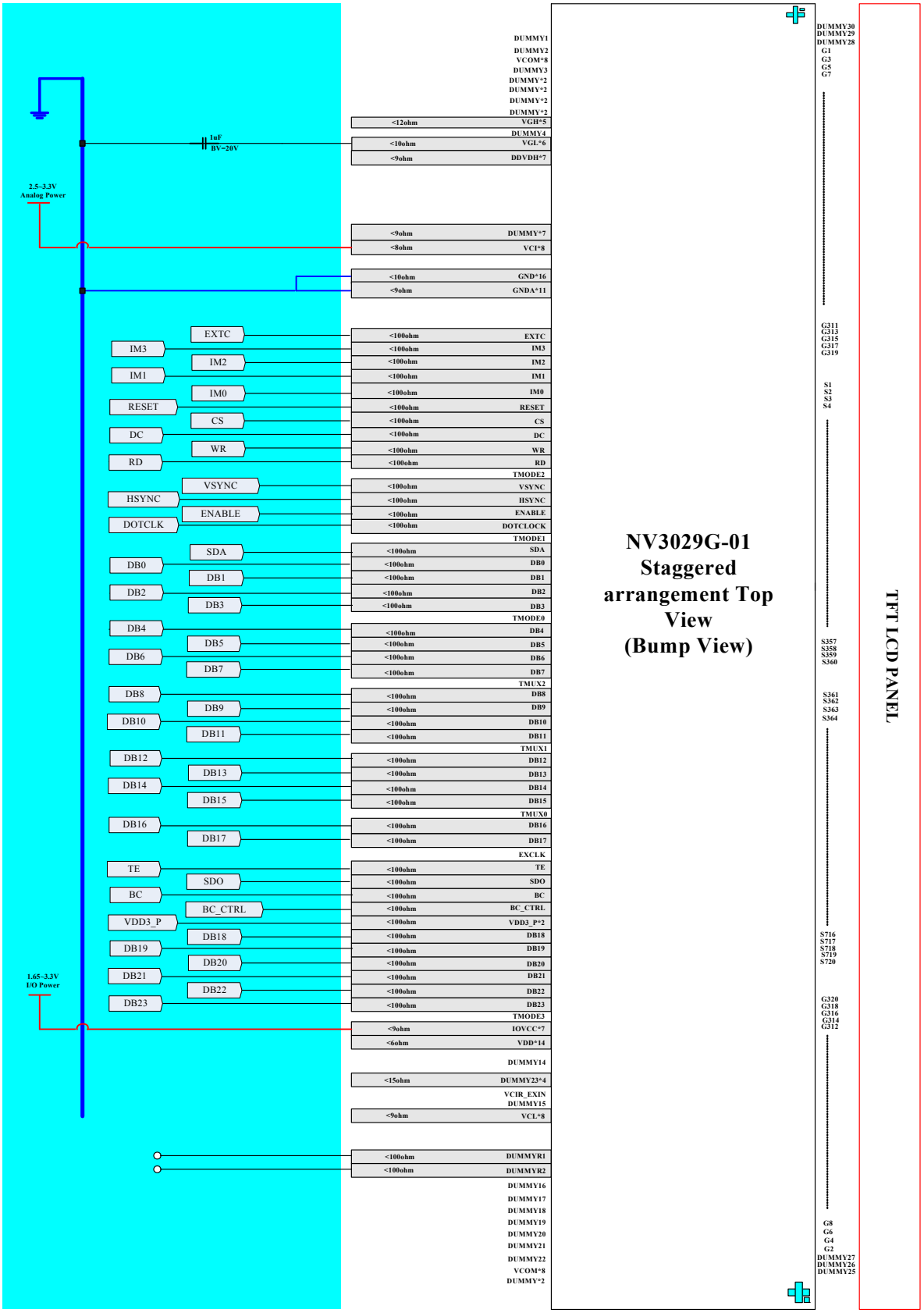
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time(RT) within 5ms after a rising edge of RESET.
2. Spice due to and electrostatic discharge on RESET line does not cause irregular system reset.
   When short than 0.1ms, reset rejected.
3. During the Resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in sleep in-mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120 msec.

11. Application



12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Item	Symbol	Unit	Ratings	Notes
Power-supply voltage(1)	Vci,IOVcc	V	-0.3 to +3.6	1,2
Power-supply voltage(2)	Vci-GNDA	V	-0.3 to +3.6	1,3
Power-supply voltage(3)	DDVDH-GNDA	V	-0.3 to +6.0	1,4
Power-supply voltage(4)	VGH-VGL	V	-0.3 to +30.0	1,4
Power-supply voltage(5)	GNDA-VGL	V	+3.0 to +13.0	1,7
Power-supply voltage(6)	DDVDH-VGL	V	+4.0 to +19.0	1,5
Power-supply voltage(7)	Vci-VGL	V	+3.0 to + 16.8	1,7
Power-supply voltage(7)	VCOMH-VCOML	V	+3.0 to + 6.0	1,8
Input voltage	Vt	V	-0.3 to 3.9	1
Operating temperature	Topr	℃	-40 to +85	1,8
Storage temperature	Tstg	℃	-55 to +110	1

12.2 DC Characteristic

Vci = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, Ta = -40 ~ 85 °C

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVcc = 1.65V ~ 3.3 V	0.8* IOVcc	-	IOVcc	2,3
Input low voltage	V_{IL}	V	IOVcc = 1.65V ~ 3.3 V	– 0.3V	-	0.2* IOVcc	2,3
Output high voltage (D0-17 pins, FMARK)	V_{OH}	V	IOH = -0.1mA	0.8 * IOVcc	-	-	2
Output low voltage (D0-17 pins, FMARK)	V_{OL}	V	IOVcc = 1.65 ~ 2.4 V I_{OL} = 0.1mA	-	-	0.2* IOVcc	2
I/O leak current	Ili	μA	Vin = 0 ~ IOVcc	-1		1	4
Current consumption during normal operation (Vci-GNDD)+(IOVcc-GND)	IOP(Vci)	mA	Vci=IOVcc=Vci=2.8V, Ta=25C, Fosc=6MHZ(320 Line)GRAM data =0000h, Frame rate=70HZ, REV=0, SAP=100,AP=100,DC0 =000,DC1=010,B/C=0, VC=001,VRH=0011, VCM=10011,VDV=100 00,VCOMG=1,CL=0, NO panel load	-	TBD	-	
Current consumption during standby operation (Vci-GNDD)+(IOVcc-GND)	IOP(Vci)	μA		-	45		5,6

Notes:

1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI within the electrical characteristics conditions in normal operation. Exposure to a condition not within the electrical characteristics may affect reliability of the device.
2. Make sure (Rvci=Vci) (high) ≥ GND (low) and IOVcc (high) ≥ GND (low).
3. Make sure Vci (high) ≥ GNDA (low).
4. Make sure DDVDH (high) ≥ GNDA (low).
5. Make sure DDVDH (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ GNDA (low).
7. Make sure GNDA (high) ≥ VGL (low).
8. Make sure VCOMH(high) ≥ VCOML (low).
9. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

12.3 AC Characteristics

80-system Bus Interface Timing Characteristics (18-bit/16-bit Transfer Mode)

IOVcc = 1.65V to 3.30V, Vci = 2.4V ~ 3.3V

Item		symbol	Unit	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	125	-	-
	Read	t_{CYCR}	ns	450	-	-
Setup time	Write (RS~CS, WR)	t_{AS}	ns	0	-	-
	Read (RS~CS, RD*)			10		
Write high-level pulse width		PW_{HW}	ns	70	-	-
Read high-level pulse width		PW_{HR}	ns	250	-	-
Write/Read rise/fall time		t_{WRr} ,t_{WRf}	ns	-	-	25
Address hold time		t_{AH}	ns	2	-	-
Write data setup time		t_{DSW}	ns	10	-	-
Write data hold time		t_{H}	ns	10	-	-
Read data delay time		t_{DD}	ns	-	-	150
Read data hold time		t_{DHR}	ns	5	-	-
Write low-level pulse width		PW_{LW}	ns	45	-	500
Read low-level pulse width		PW_{LR}	ns	170	-	-

80-system Bus Interface Timing Characteristics (9-bit /8-bit Transfer Mode)

IOVcc = 1.65V to 3.30V, Vci = 2.4V ~3.3V

Item		symbol	Unit	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	70	-	-
	Read	t_{CYCR}	ns	450	-	-
Setup time	Write (RS~CS, WR)	t_{AS}	ns	0	-	-
	Read (RS~CS, RD)			10		
Write high-level pulse width		PW_{HW}	ns	25	-	-
Read high-level pulse width		PW_{HR}	ns	250	-	-
Write/Read rise/fall time		t_{WRr} ,t_{WRf}	ns	-	-	25
Address hold time		t_{AH}	ns	2	-	-
Write data setup time		t_{DSW}	ns	10	-	-
Write data hold time		t_{H}	ns	10	-	-
Read data delay time		t_{DD}	ns	-	-	150
Read data hold time		t_{DHR}	ns	5	-	-
Write low-level pulse width		PW_{LW}	ns	30	-	-
Read low-level pulse width		PW_{LR}	ns	170	-	-

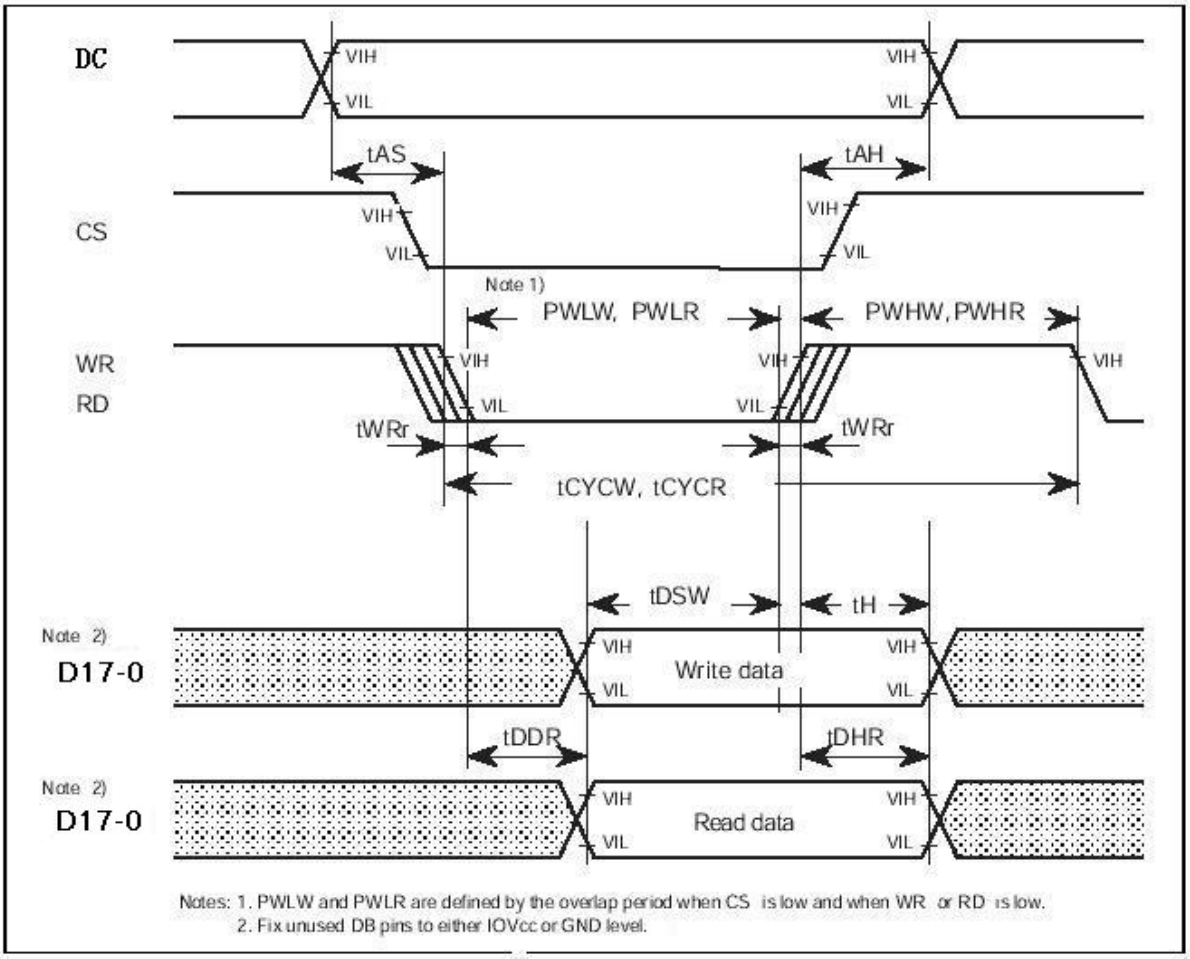
Liquid crystal driver Output Characteristics

Item	symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Source-drive output delay time	Tdd1	us	Vci=3.00v,DDVDH=5.50V VREG1OUT=5.00V, RC oscillation fosc=6MHZ (drive 320 lines),Ta=25℃ REV=0,AP=010,SAP=010, VRP14-00=0,VRN14-00=0, PKP52-00=0,PKN52-00=0, PRP12-00=0,PRN12-00=0,	-	-	17	10

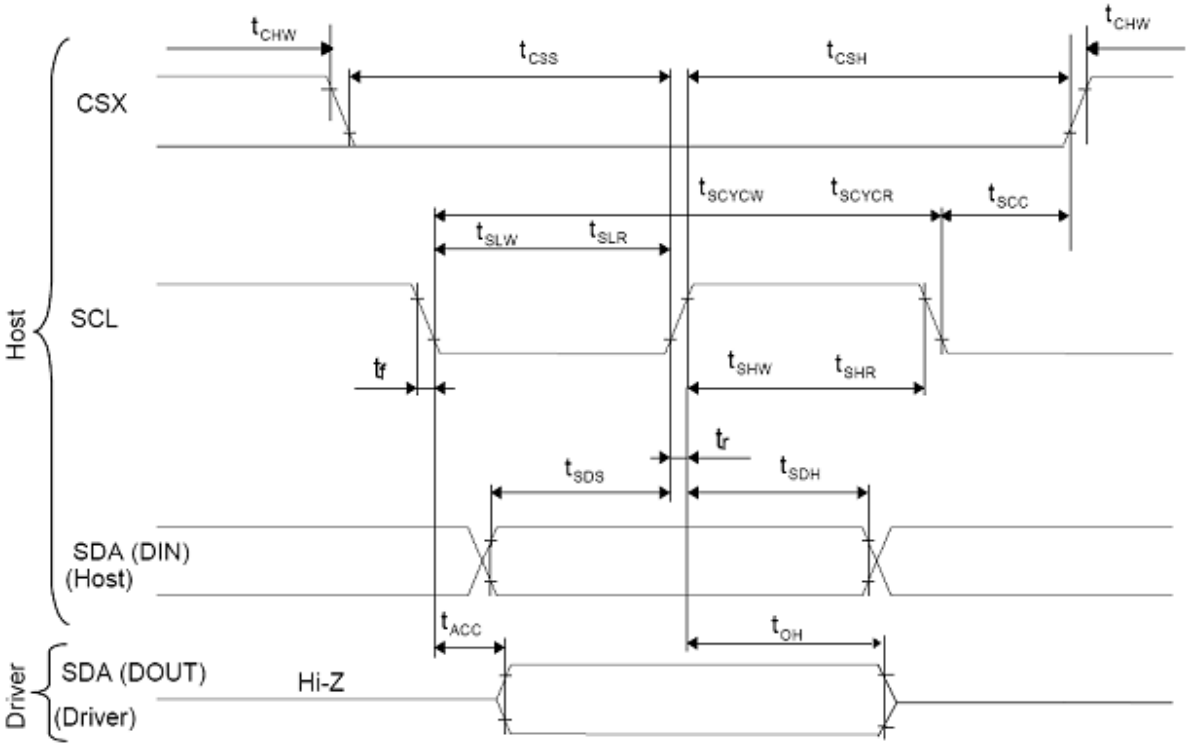
	Tdd2	us	Load resistance R=10kΩ, Load capacitance C=20Pf Time to reach the target voltage level+/-35mv from VCOM Polarity inversion timing Transient from a same grayscale at all source pins	-	-	17	11

12.4 Timing Characteristics Diagram

80-system Bus Interface Operation

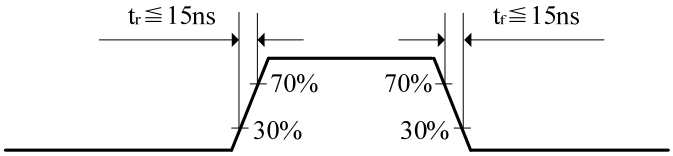


12.5 Display Serial Interface Timing Characteristics (3-line SPI system)

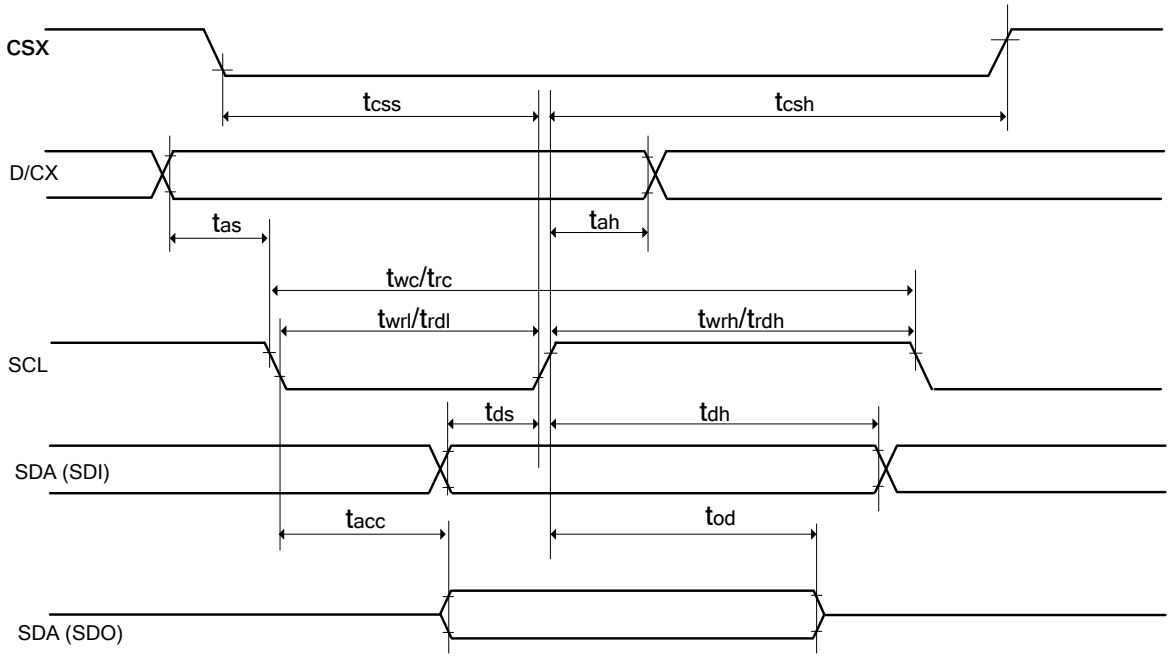


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	25	-	ns	
	tshw	SCL “H” Pulse Width (Write)	10	-	ns	
	tslw	SCL “L” Pulse Width (Write)	10	-	ns	
	tscycr	Serial Clock Cycle (Read)	80	-	ns	
	tshr	SCL “H” Pulse Width (Read)	32	-	ns	
	tslr	SCL “L” Pulse Width (Read)	32	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	12	-	ns	
	tsdh	Data hold time (Write)	12	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	5	20	ns	
	toh	Output disable time (Read)	15	60	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	15	-	ns	
	tcsh		30	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, GNDA=VSS=0V

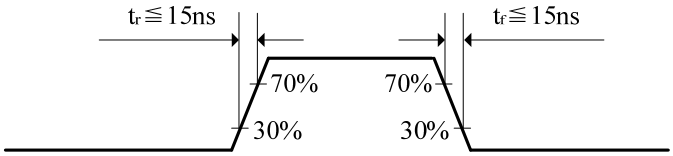


12.6 Display Serial Interface Timing Characteristics (4-line SPI system)

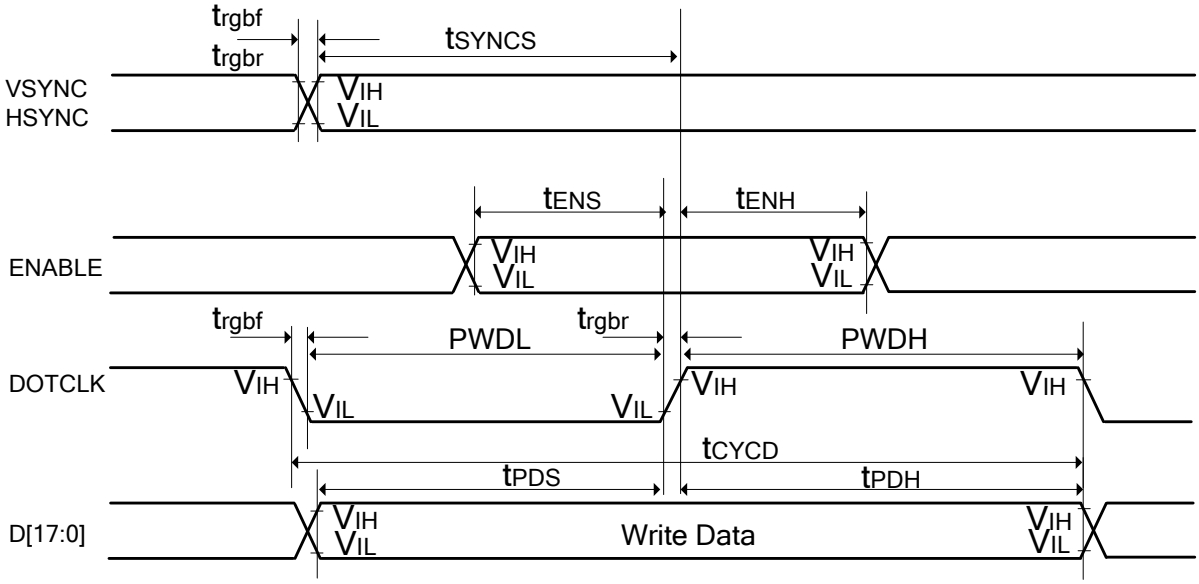


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	30	-	ns	
SCL	twc	Serial clock cycle (Write)	25	-	ns	
	twrh	SCL “H” pulse width (Write)	10	-	ns	
	twrl	SCL “L” pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	80	-	ns	
	trdh	SCL “H” pulse width (Read)	32	-	ns	
	trdl	SCL “L” pulse width (Read)	32	-	ns	
D/CX	tas	D/CX setup time	2	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	12	-	ns	
	tdh	Data hold time (Write)	12	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	5	20	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	60	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, GNDA=VSS=0V

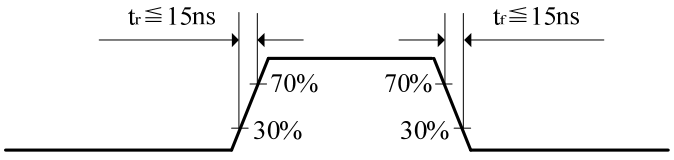


12.7 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100		ns	
	trgbr , trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low- level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100		ns	
	trgbr , trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, GNDA=VSS=0V



Revision history

Version No.	Date	Page	Introduction
0.1	2015-11-30	All	New build.