DATA SHEET

NV3029S

240RGB x 320dot, 262,144-color

TFT Controller Driver with Internal RAM

Version 1.0

Aug 25, 2017

Contents

1. Introduction

NV3029S is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

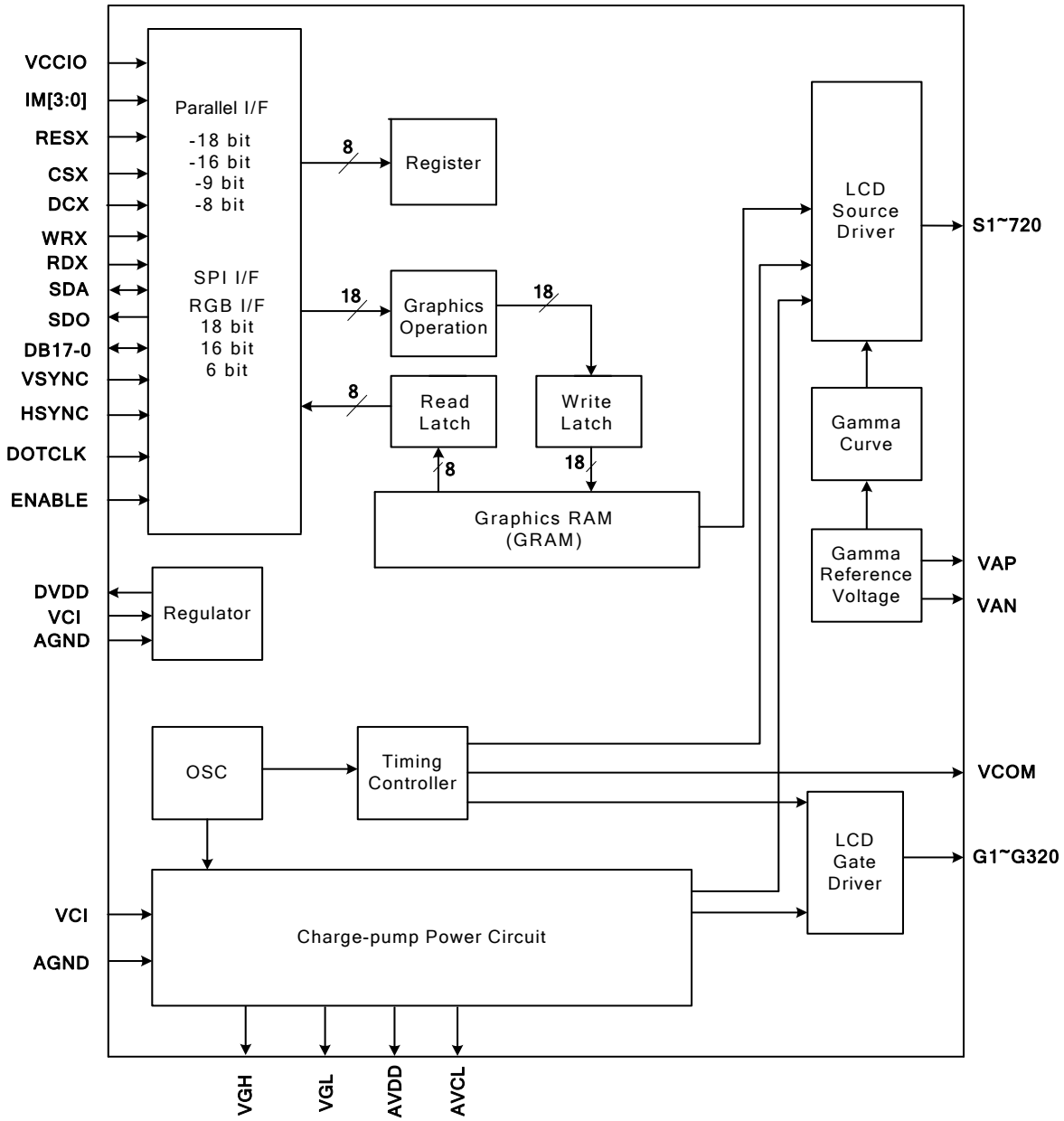
NV3029S supports 8-/9-/16-/18-bit data bus parallel interface, 6-/16-/18-bit data bus RGB interface and 3-/4-wire serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

NV3029S can operate with 1.65V ~ 3.6V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. NV3029S supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the NV3029S an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- One-chip controller driver for 240RGB x 320 dot graphics display in 262,144 colors on TFT panel
- One-chip solution for a-Si TFT panel
- System interface
  - 8-, 9-, 16-, 18-bit parallel ports
  - 3-/4-wire serial peripheral interface
- Moving picture display interface
  - RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 6-, 16-, 18-bit ports
- Window address function to specify a rectangular area in the internal RAM to write data
  - Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
- Display Colors (Color Mode)
  - Full Color:262K, RGB=(666)max.,Idle Mode Off
  - Color Reduce: 8-color, RGB=(111),Idle Mode On
- Low–power consumption architecture (allowing direct input of interface I/O power supply)
  - 8-color display function
  - Input power supply voltages: VCCIO = 1.65V ~ 3.6V(interface I/O power supply)
    VCI = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)
- Driving Algorithm
  - Dot Inversion
  - Column Inversion
- On-Chip Power System
  - Source Voltage (VAP to VAN): +6.4~ -4.6V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to AGND): +13.3V ~ +16V
  - Gate driver LOW level (VGL to AGND): -10.2V ~ -7.9V
- Internal liquid crystal drive circuit: 720-channel source output and 320-channel gate output
- Internal oscillator, Hardware and software Reset
- TFT storage capacitor: Cst only
- Don't need any external capacitor
- Optimized layout for COG Assembly

3. Block Diagram



4. Pin Function

4.1 Power Supply Pins

Signal	I/O	Connect to	Function
VCCIO	I	I/O voltage	Low voltage power supply for interface logic circuits. (1.65~3.6V).
VCI	I	Analog Power	High voltage power supply for analog circuit blocks. Connect to an external power supply of 2.5V ~ 3.3V.
DGND	I	Logic Ground	System ground level for logic blocks.
AGND	I	Analog Ground	System ground level for analog circuit blocks. Connect to GND on the FPC to prevent noise.
AVDD	O	-	Source driver power supply.
AVCL	O	-	Source driver power supply.
VGH	O	-	Gate driver positive power supply.
VGL	O	-	Gate driver negative power supply.
DVDD	O	-	Digital circuit power pad.
VAP	O	-	A power output of grayscale voltage generator.
VAN	O	-	A power output (Negative) of grayscale voltage generator.
V20	O	-	A power output of grayscale voltage generator.
VDDS	O	-	Source driver power supply.

4.2 Interface Logic Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>Select the system interface mode.
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">interface Mode</th><th colspan="2">DB pins</th></tr>
<tr><th>Register</th><th>Gram</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>i80-system
8-bit interface I</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>i80-system
16-bit interface I</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system
9-bit interface I</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system
18-bit interface I</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-wire 9-bit data
Serial interface I</td><td colspan="2" rowspan="2">SDA: in/out</td></tr>
<tr><td>2 data lane serial
interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data
Serial interface I</td><td colspan="2">SDA: in/out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>i80-system
16-bit interface
II</td><td>DB[8:1]</td><td>DB[8:1],
DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>i80-system
8-bit interface II</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system
18-bit interface
II</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system
9-bit interface II</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data
Serial interface
II</td><td colspan="2">SDA: in
SDO: out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data
Serial interface
II</td><td colspan="2">SDA: in
SDO: out</td></tr>
</table>
If pad not used, please fix this pin to VCCIO or DGND level.</td></tr>
<tr><td>RESX</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>A chip select signal.
Low: the NV3029S is selected and accessible.
High: the NV3029S is not selected and not accessible.</td></tr>
</table>

<table>
<tr><td>DCX</td><td>I</td><td>This pin is used to select “Data or Command” in the parallel interface.
When DCX = ’1’, data is selected.
When DCX = ’0’, command is selected.
This pin is used serial interface clock.
If not used, this pin should be connected to VCCIO or DGND.</td></tr>
<tr><td>WRX</td><td>I</td><td>A write strobe signal and enables an operation to write data when the signal is low.
Fix to either VCCIO or DGND level when not in use.
SPI 4-wire system: Serves as command or parameter select.
2 data lane serial interface: the second data lane.</td></tr>
<tr><td>RDX</td><td>I</td><td>A read strobe signal and enables an operation to read out data when the signal is low.
Fix to VCCIO level in parallel I/F when not in use.
And fix to either VCCIO or DGND level in other I/F when not in use.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>When serial I/F I: it is SPI interface input/output pin.
When serial I/F Ⅱ: it is SPI interface input pin.
The data is latched on the rising edge of the serial interface clock signal.
If not used, please fix this pin at VCCIO or DGND level.</td></tr>
<tr><td>SDO</td><td>O</td><td>SPI interface output pin.
The data is outputted on the falling edge of the serial interface clock signal.
If not used, open this pin.</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low.
If not used, open this pin.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>Pixel clock signal in RGB I/F mode.
If not used, fix this pin at VCCIO or DGND.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Vertical sync. Signal in RGB I/F mode.
If not used, fix this pin at VCCIO or DGND.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>Horizontal sync. Signal in RGB I/F mode.
If not used, fix this pin at VCCIO or DGND.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>Data enable signal in RGB I/F mode. If not used, fix this pin at VCCIO or DGND.</td></tr>
<tr><td>DB17-DB0</td><td>I/O</td><td>18-bit parallel bi-directional data bus for system interface. Refer to IM[3:0] pin description.
18-bit data bus for RGB interface mode.
<table>
<tr><th>RGB Interface Mode</th><th>DB Pin</th></tr>
<tr><td>6-bit RGB</td><td>DB[5:0]</td></tr>
<tr><td>16-bit RGB</td><td>DB[17:13],DB[11:1]</td></tr>
<tr><td>18-bit RGB</td><td>DB[17:0]</td></tr>
</table>
If not used, fix this pin at VCCIO or DGND level.</td></tr>
<tr><td>OSC_SW</td><td>I</td><td>Input pin only for test.</td></tr>
<tr><td>MEC_BPS</td><td>I</td><td>Input pin only for test.</td></tr>
</table>

4.3 Driver Output Pins

Signal	I/O	Function
S1 to S720	O	Source driver output pads.
G1 to G320	O	Gate driver output pads.
VCOM	O	A power supply for the TFT-LCD common electrode.

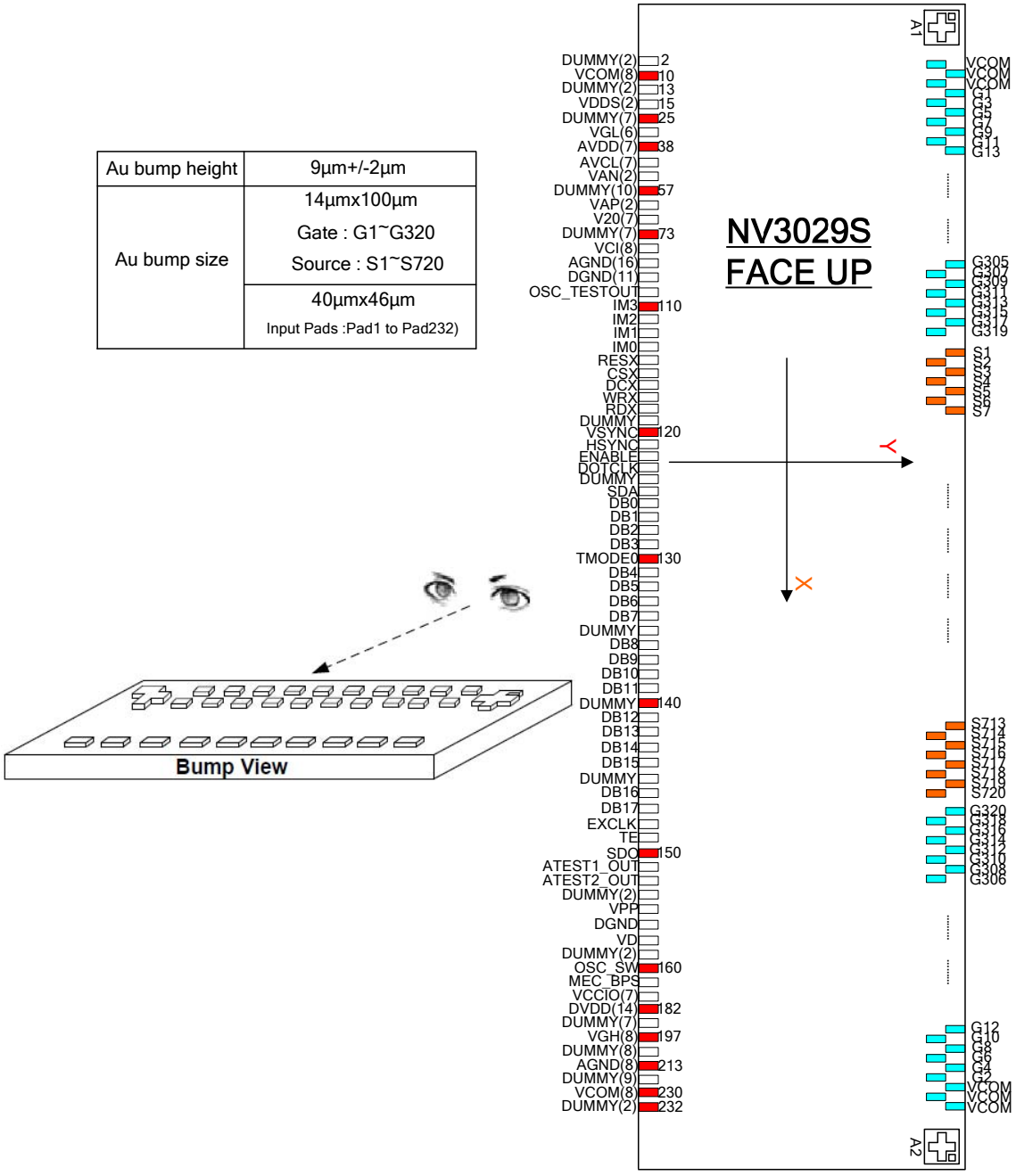
4.4 Test and other pins

Name	I/O	Description
VPP	I	Test pin.Leave these pads open.
VD	I	Test pin.Leave these pads open.
ATEST1_OUT/ ATEST2_OUT/ OSC_TESTOUT	O	Output pins for testing. Please keep these pins floating.
EXCLK	-	Dummy pin.Leave these pads open.
TMODE0	-	Dummy pin.Leave these pads open.
DUMMY	-	These pins are dummy (no electrical characteristic) Can pass signal through these pads on TFT panel. Please open these pins.

5. Pad Arrangement

5.1 Output Bump Dimension

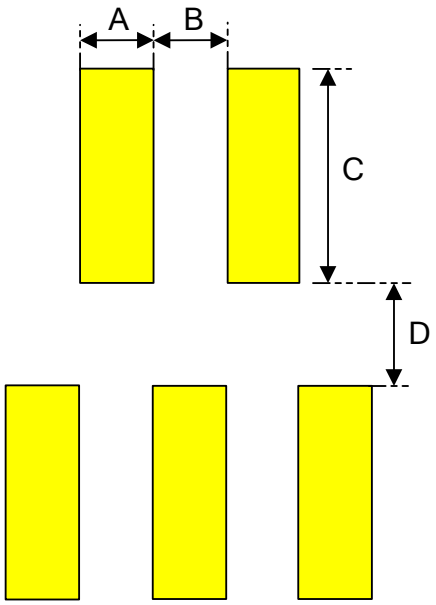
Au bump height	9μm+/-2μm
Au bump size	14μmx100μm Gate : G1~G320 Source : S1~S720
	40μmx46μm Input Pads :Pad1 to Pad232)



5.2 Input Bump Dimension

✧ **Output Pads**S1~S720、G1~G320、VCOM

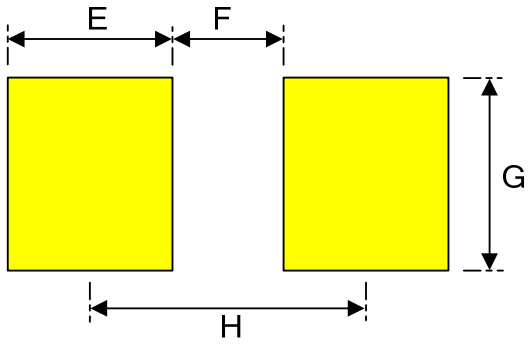
(No.233~1278)



Symbol	Item	Size
A	Bump Width	14um
B	Bump Gap 1 (Horizontal)	14um
C	Bump Height	100um
D	Bump Gap 2 (Vertical)	31um

✧ **Input Pads**

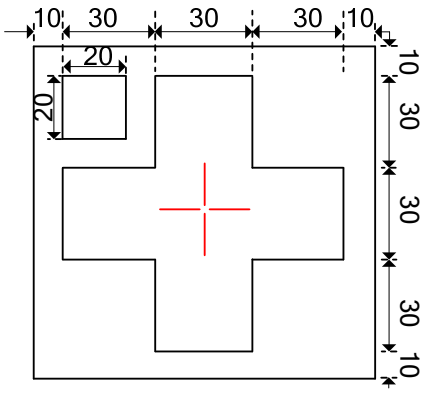
No.1~232



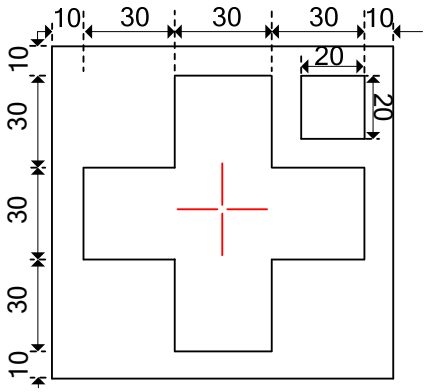
Symbol	Item	Size
E	Bump Width	40 um
F	Bump Gap	20,80,140,32.5,45 um
G	Bump Height	46 um
H	Bump Pitch	60,120,180,72.5,85 um

5.3 Alignment Mark Dimension

✧ Alignment Mark : A1(X,Y)=(-7480,225)



✧ Alignment Mark : A2(X,Y)=(7480,225)



5.4 Chip Information

Chip size	15960um x 648um
Chip thickness	280um
Pad Location	Pad center
Coordinate Origin	(-40,0)

6 PAD CENTER COORDINATES

(Pad NO. refered to competitor's datasheet)

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
	DUMMY	-7592.475	-246	34	AVDD	-5312.475	-246
	DUMMY	-7532.475	-246	35	AVDD	-5252.475	-246
	DUMMY	-7472.475	-246	36	AVDD	-5192.475	-246
	DUMMY	-7412.475	-246	37	AVDD	-5132.475	-246
1	DUMMY	-7292.475	-246	38	AVDD	-5072.475	-246
2	DUMMY	-7232.475	-246	39	AVCL	-5012.475	-246
3	VCOM	-7172.475	-246	40	AVCL	-4952.475	-246
4	VCOM	-7112.475	-246	41	AVCL	-4892.475	-246
5	VCOM	-7052.475	-246	42	AVCL	-4832.475	-246
6	VCOM	-6992.475	-246	43	AVCL	-4772.475	-246
7	VCOM	-6932.475	-246	44	AVCL	-4712.475	-246
8	VCOM	-6872.475	-246	45	AVCL	-4652.475	-246
9	VCOM	-6812.475	-246	46	VAN	-4592.475	-246
10	VCOM	-6752.475	-246	47	VAN	-4532.475	-246
11	DUMMY	-6692.475	-246	48	DUMMY	-4472.475	-246
12	No pad	-6632.5	-256.62	49	DUMMY	-4412.475	-246
13	DUMMY	-6572.475	-246	50	DUMMY	-4352.475	-246
14	VDDS	-6512.475	-246	51	DUMMY	-4292.475	-246
15	VDDS	-6452.475	-246	52	DUMMY	-4232.475	-246
16	No pad	-6392.5	-256.62	53	DUMMY	-4172.475	-246
17	No pad	-6332.5	-256.62	54	DUMMY	-4112.475	-246
18	DUMMY	-6272.475	-246	55	DUMMY	-4052.475	-246
19	No pad	-6212.5	-256.62	56	DUMMY	-3992.475	-246
20	DUMMY	-6152.475	-246	57	DUMMY	-3932.475	-246
21	DUMMY	-6092.475	-246	58	VAP	-3872.475	-246
22	DUMMY	-6032.475	-246	59	VAP	-3812.475	-246
23	DUMMY	-5972.475	-246	60	V20	-3752.475	-246
24	DUMMY	-5912.475	-246	61	V20	-3692.475	-246
25	DUMMY	-5852.475	-246	62	V20	-3632.475	-246
26	VGL	-5792.475	-246	63	V20	-3572.475	-246
27	VGL	-5732.475	-246	64	V20	-3512.475	-246
28	VGL	-5672.475	-246	65	V20	-3452.475	-246
29	VGL	-5612.475	-246	66	V20	-3392.475	-246
30	VGL	-5552.475	-246	67	DUMMY	-3332.475	-246
31	VGL	-5492.475	-246	68	DUMMY	-3272.475	-246
32	AVDD	-5432.475	-246	69	DUMMY	-3212.475	-246
33	AVDD	-5372.475	-246	70	DUMMY	-3152.475	-246

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
71	DUMMY	-3092.475	-246	104	DGND	-1112.475	-246
72	DUMMY	-3032.475	-246	105	DGND	-1052.475	-246
73	DUMMY	-2972.475	-246	106	DGND	-992.475	-246
74	VCI	-2912.475	-246	107	DGND	-932.475	-246
75	VCI	-2852.475	-246	108	DGND	-872.475	-246
76	VCI	-2792.475	-246	109	OSC_TESTOUT	-812.475	-246
77	VCI	-2732.475	-246	110	IM<3>	-752.475	-246
78	VCI	-2672.475	-246	111	IM<2>	-692.475	-246
79	VCI	-2612.475	-246	112	IM<1>	-632.475	-246
80	VCI	-2552.475	-246	113	IM<0>	-572.475	-246
81	VCI	-2492.475	-246	114	RESX	-512.475	-246
82	AGND	-2432.475	-246	115	CSX	-452.475	-246
83	AGND	-2372.475	-246	116	DCX	-392.475	-246
84	AGND	-2312.475	-246	117	WRX	-332.475	-246
85	AGND	-2252.475	-246	118	RDX	-272.475	-246
86	AGND	-2192.475	-246	119	DUMMY	-212.475	-246
87	AGND	-2132.475	-246	120	VSYNC	-152.475	-246
88	AGND	-2072.475	-246	121	HSYNC	-92.475	-246
89	AGND	-2012.475	-246	122	ENABLE	-32.475	-246
90	AGND	-1952.475	-246	123	DOTCLK	27.525	-246
91	AGND	-1892.475	-246	124	DUMMY	87.525	-246
92	AGND	-1832.475	-246	125	SDA	160.025	-246
93	AGND	-1772.475	-246	126	DB<0>	245.025	-246
94	AGND	-1712.475	-246	127	DB<1>	330.025	-246
95	AGND	-1652.475	-246	128	DB<2>	415.025	-246
96	AGND	-1592.475	-246	129	DB<3>	500.025	-246
97	AGND	-1532.475	-246	130	TMODE<0>	572.525	-246
98	DGND	-1472.475	-246	131	DB<4>	645.025	-246
99	DGND	-1412.475	-246	132	DB<5>	730.025	-246
100	DGND	-1352.475	-246	133	DB<6>	815.025	-246
101	DGND	-1292.475	-246	134	DB<7>	900.025	-246
102	DGND	-1232.475	-246	135	DUMMY	972.525	-246
103	DGND	-1172.475	-246	136	DB<8>	1045.025	-246

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
137	DB<9>	1130.025	-246	170	DVDD	3572.525	-246
138	DB<10>	1215.025	-246	171	DVDD	3632.525	-246
139	DB<11>	1300.025	-246	172	DVDD	3692.525	-246
140	DUMMY	1372.525	-246	173	DVDD	3752.525	-246
141	DB<12>	1445.025	-246	174	DVDD	3812.525	-246
142	DB<13>	1530.025	-246	175	DVDD	3872.525	-246
143	DB<14>	1615.025	-246	176	DVDD	3932.525	-246
144	DB<15>	1700.025	-246	177	DVDD	3992.525	-246
145	DUMMY	1772.525	-246	178	DVDD	4052.525	-246
146	DB<16>	1845.025	-246	179	DVDD	4112.525	-246
147	DB<17>	1930.025	-246	180	DVDD	4172.525	-246
148	EXCLK	2002.525	-246	181	DVDD	4232.525	-246
149	TE	2075.025	-246	182	DVDD	4292.525	-246
150	SDO	2160.025	-246	183	DUMMY	4352.525	-246
151	ATEST1_OUT	2245.025	-246	184	DUMMY	4412.525	-246
152	ATEST2_OUT	2330.025	-246	185	DUMMY	4472.525	-246
153	DUMMY	2402.525	-246	186	DUMMY	4532.525	-246
154	DUMMY	2462.525	-246	187	DUMMY	4592.525	-246
155	VPP	2535.025	-246	188	DUMMY	4652.525	-246
156	DGND	2620.025	-246	189	DUMMY	4712.525	-246
157	VD	2705.025	-246	190	VGH	4772.525	-246
158	DUMMY	2790.025	-246	191	VGH	4832.525	-246
159	DUMMY	2875.025	-246	192	VGH	4892.525	-246
160	OSC_SW	2960.025	-246	193	VGH	4952.525	-246
161	MEC_BPS	3032.525	-246	194	VGH	5012.525	-246
162	VCCIO	3092.525	-246	195	VGH	5072.525	-246
163	VCCIO	3152.525	-246	196	VGH	5132.525	-246
164	VCCIO	3212.525	-246	197	VGH	5192.525	-246
165	VCCIO	3272.525	-246	198	DUMMY	5252.525	-246
166	VCCIO	3332.525	-246	199	DUMMY	5312.525	-246
167	VCCIO	3392.525	-246	200	DUMMY	5372.525	-246
168	VCCIO	3452.525	-246	201	DUMMY	5432.525	-246
169	DVDD	3512.525	-246	202	DUMMY	5492.525	-246

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	DUMMY	5552.525	-246		DUMMY	7532.525	-246
204	DUMMY	5612.525	-246		DUMMY	7592.525	-246
205	DUMMY	5672.525	-246		DUMMY	7652.525	-246
206	AGND	5732.525	-246		DUMMY	7749.385	92.975
207	AGND	5792.525	-246		DUMMY	7709.385	92.975
208	AGND	5852.525	-246		DUMMY	7669.385	92.975
209	AGND	5912.525	-246		DUMMY	7629.385	92.975
210	AGND	5972.525	-246		DUMMY	7589.385	92.975
211	AGND	6032.525	-246		DUMMY	7549.385	92.975
212	AGND	6092.525	-246		DUMMY	7509.385	92.975
213	AGND	6152.525	-246		DUMMY	7469.385	92.975
214	DUMMY	6212.525	-246		DUMMY	7429.385	92.975
215	DUMMY	6272.525	-246	233	VCOM	7396.385	224
216	DUMMY	6332.525	-246	234	VCOM	7382.385	92.975
217	DUMMY	6392.525	-246	235	VCOM	7368.385	224
218	DUMMY	6452.525	-246	236	G<2>	7354.425	92.975
219	DUMMY	6512.525	-246	237	G<4>	7340.425	224
220	DUMMY	6572.525	-246	238	G<6>	7326.425	92.975
221	DUMMY	6632.525	-246	239	G<8>	7312.425	224
222	DUMMY	6692.525	-246	240	G<10>	7298.425	92.975
223	VCOM	6752.525	-246	241	G<12>	7284.425	224
224	VCOM	6812.525	-246	242	G<14>	7270.425	92.975
225	VCOM	6872.525	-246	243	G<16>	7256.425	224
226	VCOM	6932.525	-246	244	G<18>	7242.465	92.975
227	VCOM	6992.525	-246	245	G<20>	7228.465	224
228	VCOM	7052.525	-246	246	G<22>	7214.465	92.975
229	VCOM	7112.525	-246	247	G<24>	7200.465	224
230	VCOM	7172.525	-246	248	G<26>	7186.465	92.975
231	DUMMY	7232.525	-246	249	G<28>	7172.465	224
232	DUMMY	7292.525	-246	250	G<30>	7158.465	92.975
	DUMMY	7352.525	-246	251	G<32>	7144.465	224
	DUMMY	7412.525	-246	252	G<34>	7130.505	92.975
	DUMMY	7472.525	-246	253	G<36>	7116.505	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
254	G<38>	7102.505	92.975	287	G<104>	6640.665	224
255	G<40>	7088.505	224	288	G<106>	6626.665	92.975
256	G<42>	7074.505	92.975	289	G<108>	6612.665	224
257	G<44>	7060.505	224	290	G<110>	6598.665	92.975
258	G<46>	7046.505	92.975	291	G<112>	6584.665	224
259	G<48>	7032.505	224	292	G<114>	6570.705	92.975
260	G<50>	7018.545	92.975	293	G<116>	6556.705	224
261	G<52>	7004.545	224	294	G<118>	6542.705	92.975
262	G<54>	6990.545	92.975	295	G<120>	6528.705	224
263	G<56>	6976.545	224	296	G<122>	6514.705	92.975
264	G<58>	6962.545	92.975	297	G<124>	6500.705	224
265	G<60>	6948.545	224	298	G<126>	6486.705	92.975
266	G<62>	6934.545	92.975	299	G<128>	6472.705	224
267	G<64>	6920.545	224	300	G<130>	6458.745	92.975
268	G<66>	6906.585	92.975	301	G<132>	6444.745	224
269	G<68>	6892.585	224	302	G<134>	6430.745	92.975
270	G<70>	6878.585	92.975	303	G<136>	6416.745	224
271	G<72>	6864.585	224	304	G<138>	6402.745	92.975
272	G<74>	6850.585	92.975	305	G<140>	6388.745	224
273	G<76>	6836.585	224	306	G<142>	6374.745	92.975
274	G<78>	6822.585	92.975	307	G<144>	6360.745	224
275	G<80>	6808.585	224	308	G<146>	6346.785	92.975
276	G<82>	6794.625	92.975	309	G<148>	6332.785	224
277	G<84>	6780.625	224	310	G<150>	6318.785	92.975
278	G<86>	6766.625	92.975	311	G<152>	6304.785	224
279	G<88>	6752.625	224	312	G<154>	6290.785	92.975
280	G<90>	6738.625	92.975	313	G<156>	6276.785	224
281	G<92>	6724.625	224	314	G<158>	6262.785	92.975
282	G<94>	6710.625	92.975	315	G<160>	6248.785	224
283	G<96>	6696.625	224	316	G<162>	6234.825	92.975
284	G<98>	6682.665	92.975	317	G<164>	6220.825	224
285	G<100>	6668.665	224	318	G<166>	6206.825	92.975
286	G<102>	6654.665	92.975	319	G<168>	6192.825	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
320	G<170>	6178.825	92.975	353	G<236>	5716.985	224
321	G<172>	6164.825	224	354	G<238>	5702.985	92.975
322	G<174>	6150.825	92.975	355	G<240>	5688.985	224
323	G<176>	6136.825	224	356	G<242>	5675.025	92.975
324	G<178>	6122.865	92.975	357	G<244>	5661.025	224
325	G<180>	6108.865	224	358	G<246>	5647.025	92.975
326	G<182>	6094.865	92.975	359	G<248>	5633.025	224
327	G<184>	6080.865	224	360	G<250>	5619.025	92.975
328	G<186>	6066.865	92.975	361	G<252>	5605.025	224
329	G<188>	6052.865	224	362	G<254>	5591.025	92.975
330	G<190>	6038.865	92.975	363	G<256>	5577.025	224
331	G<192>	6024.865	224	364	G<258>	5563.065	92.975
332	G<194>	6010.905	92.975	365	G<260>	5549.065	224
333	G<196>	5996.905	224	366	G<262>	5535.065	92.975
334	G<198>	5982.905	92.975	367	G<264>	5521.065	224
335	G<200>	5968.905	224	368	G<266>	5507.065	92.975
336	G<202>	5954.905	92.975	369	G<268>	5493.065	224
337	G<204>	5940.905	224	370	G<270>	5479.065	92.975
338	G<206>	5926.905	92.975	371	G<272>	5465.065	224
339	G<208>	5912.905	224	372	G<274>	5451.105	92.975
340	G<210>	5898.945	92.975	373	G<276>	5437.105	224
341	G<212>	5884.945	224	374	G<278>	5423.105	92.975
342	G<214>	5870.945	92.975	375	G<280>	5409.105	224
343	G<216>	5856.945	224	376	G<282>	5395.105	92.975
344	G<218>	5842.945	92.975	377	G<284>	5381.105	224
345	G<220>	5828.945	224	378	G<286>	5367.105	92.975
346	G<222>	5814.945	92.975	379	G<288>	5353.105	224
347	G<224>	5800.945	224	380	G<290>	5339.145	92.975
348	G<226>	5786.985	92.975	381	G<292>	5325.145	224
349	G<228>	5772.985	224	382	G<294>	5311.145	92.975
350	G<230>	5758.985	92.975	383	G<296>	5297.145	224
351	G<232>	5744.985	224	384	G<298>	5283.145	92.975
352	G<234>	5730.985	92.975	385	G<300>	5269.145	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
386	G<302>	5255.145	92.975	419	S<697>	4751.305	224
387	G<304>	5241.145	224	420	S<696>	4737.345	92.975
388	G<306>	5227.185	92.975	421	S<695>	4723.345	224
389	G<308>	5213.185	224	422	S<694>	4709.345	92.975
390	G<310>	5199.185	92.975	423	S<693>	4695.345	224
391	G<312>	5185.185	224	424	S<692>	4681.345	92.975
392	G<314>	5171.185	92.975	425	S<691>	4667.345	224
393	G<316>	5157.185	224	426	S<690>	4653.345	92.975
394	G<318>	5143.185	92.975	427	S<689>	4639.345	224
395	G<320>	5129.185	224	428	S<688>	4625.385	92.975
396	S<720>	5073.225	92.975	429	S<687>	4611.385	224
397	S<719>	5059.225	224	430	S<686>	4597.385	92.975
398	S<718>	5045.225	92.975	431	S<685>	4583.385	224
399	S<717>	5031.225	224	432	S<684>	4569.385	92.975
400	S<716>	5017.225	92.975	433	S<683>	4555.385	224
401	S<715>	5003.225	224	434	S<682>	4541.385	92.975
402	S<714>	4989.225	92.975	435	S<681>	4527.385	224
403	S<713>	4975.225	224	436	S<680>	4513.425	92.975
404	S<712>	4961.265	92.975	437	S<679>	4499.425	224
405	S<711>	4947.265	224	438	S<678>	4485.425	92.975
406	S<710>	4933.265	92.975	439	S<677>	4471.425	224
407	S<709>	4919.265	224	440	S<676>	4457.425	92.975
408	S<708>	4905.265	92.975	441	S<675>	4443.425	224
409	S<707>	4891.265	224	442	S<674>	4429.425	92.975
410	S<706>	4877.265	92.975	443	S<673>	4415.425	224
411	S<705>	4863.265	224	444	S<672>	4401.465	92.975
412	S<704>	4849.305	92.975	445	S<671>	4387.465	224
413	S<703>	4835.305	224	446	S<670>	4373.465	92.975
414	S<702>	4821.305	92.975	447	S<669>	4359.465	224
415	S<701>	4807.305	224	448	S<668>	4345.465	92.975
416	S<700>	4793.305	92.975	449	S<667>	4331.465	224
417	S<699>	4779.305	224	450	S<666>	4317.465	92.975
418	S<698>	4765.305	92.975	451	S<665>	4303.465	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
452	S<664>	4289.505	92.975	485	S<631>	3827.665	224
453	S<663>	4275.505	224	486	S<630>	3813.665	92.975
454	S<662>	4261.505	92.975	487	S<629>	3799.665	224
455	S<661>	4247.505	224	488	S<628>	3785.665	92.975
456	S<660>	4233.505	92.975	489	S<627>	3771.665	224
457	S<659>	4219.505	224	490	S<626>	3757.665	92.975
458	S<658>	4205.505	92.975	491	S<625>	3743.665	224
459	S<657>	4191.505	224	492	S<624>	3729.705	92.975
460	S<656>	4177.545	92.975	493	S<623>	3715.705	224
461	S<655>	4163.545	224	494	S<622>	3701.705	92.975
462	S<654>	4149.545	92.975	495	S<621>	3687.705	224
463	S<653>	4135.545	224	496	S<620>	3673.705	92.975
464	S<652>	4121.545	92.975	497	S<619>	3659.705	224
465	S<651>	4107.545	224	498	S<618>	3645.705	92.975
466	S<650>	4093.545	92.975	499	S<617>	3631.705	224
467	S<649>	4079.545	224	500	S<616>	3617.745	92.975
468	S<648>	4065.585	92.975	501	S<615>	3603.745	224
469	S<647>	4051.585	224	502	S<614>	3589.745	92.975
470	S<646>	4037.585	92.975	503	S<613>	3575.745	224
471	S<645>	4023.585	224	504	S<612>	3561.745	92.975
472	S<644>	4009.585	92.975	505	S<611>	3547.745	224
473	S<643>	3995.585	224	506	S<610>	3533.745	92.975
474	S<642>	3981.585	92.975	507	S<609>	3519.745	224
475	S<641>	3967.585	224	508	S<608>	3505.785	92.975
476	S<640>	3953.625	92.975	509	S<607>	3491.785	224
477	S<639>	3939.625	224	510	S<606>	3477.785	92.975
478	S<638>	3925.625	92.975	511	S<605>	3463.785	224
479	S<637>	3911.625	224	512	S<604>	3449.785	92.975
480	S<636>	3897.625	92.975	513	S<603>	3435.785	224
481	S<635>	3883.625	224	514	S<602>	3421.785	92.975
482	S<634>	3869.625	92.975	515	S<601>	3407.785	224
483	S<633>	3855.625	224	516	S<600>	3393.825	92.975
484	S<632>	3841.665	92.975	517	S<599>	3379.825	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
518	S<598>	3365.825	92.975	551	S<565>	2903.985	224
519	S<597>	3351.825	224	552	S<564>	2889.985	92.975
520	S<596>	3337.825	92.975	553	S<563>	2875.985	224
521	S<595>	3323.825	224	554	S<562>	2861.985	92.975
522	S<594>	3309.825	92.975	555	S<561>	2847.985	224
523	S<593>	3295.825	224	556	S<560>	2834.025	92.975
524	S<592>	3281.865	92.975	557	S<559>	2820.025	224
525	S<591>	3267.865	224	558	S<558>	2806.025	92.975
526	S<590>	3253.865	92.975	559	S<557>	2792.025	224
527	S<589>	3239.865	224	560	S<556>	2778.025	92.975
528	S<588>	3225.865	92.975	561	S<555>	2764.025	224
529	S<587>	3211.865	224	562	S<554>	2750.025	92.975
530	S<586>	3197.865	92.975	563	S<553>	2736.025	224
531	S<585>	3183.865	224	564	S<552>	2722.065	92.975
532	S<584>	3169.905	92.975	565	S<551>	2708.065	224
533	S<583>	3155.905	224	566	S<550>	2694.065	92.975
534	S<582>	3141.905	92.975	567	S<549>	2680.065	224
535	S<581>	3127.905	224	568	S<548>	2666.065	92.975
536	S<580>	3113.905	92.975	569	S<547>	2652.065	224
537	S<579>	3099.905	224	570	S<546>	2638.065	92.975
538	S<578>	3085.905	92.975	571	S<545>	2624.065	224
539	S<577>	3071.905	224	572	S<544>	2610.105	92.975
540	S<576>	3057.945	92.975	573	S<543>	2596.105	224
541	S<575>	3043.945	224	574	S<542>	2582.105	92.975
542	S<574>	3029.945	92.975	575	S<541>	2568.105	224
543	S<573>	3015.945	224	576	S<540>	2554.105	92.975
544	S<572>	3001.945	92.975	577	S<539>	2540.105	224
545	S<571>	2987.945	224	578	S<538>	2526.105	92.975
546	S<570>	2973.945	92.975	579	S<537>	2512.105	224
547	S<569>	2959.945	224	580	S<536>	2498.145	92.975
548	S<568>	2945.985	92.975	581	S<535>	2484.145	224
549	S<567>	2931.985	224	582	S<534>	2470.145	92.975
550	S<566>	2917.985	92.975	583	S<533>	2456.145	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
584	S<532>	2442.145	92.975	617	S<499>	1980.305	224
585	S<531>	2428.145	224	618	S<498>	1966.305	92.975
586	S<530>	2414.145	92.975	619	S<497>	1952.305	224
587	S<529>	2400.145	224	620	S<496>	1938.345	92.975
588	S<528>	2386.185	92.975	621	S<495>	1924.345	224
589	S<527>	2372.185	224	622	S<494>	1910.345	92.975
590	S<526>	2358.185	92.975	623	S<493>	1896.345	224
591	S<525>	2344.185	224	624	S<492>	1882.345	92.975
592	S<524>	2330.185	92.975	625	S<491>	1868.345	224
593	S<523>	2316.185	224	626	S<490>	1854.345	92.975
594	S<522>	2302.185	92.975	627	S<489>	1840.345	224
595	S<521>	2288.185	224	628	S<488>	1826.385	92.975
596	S<520>	2274.225	92.975	629	S<487>	1812.385	224
597	S<519>	2260.225	224	630	S<486>	1798.385	92.975
598	S<518>	2246.225	92.975	631	S<485>	1784.385	224
599	S<517>	2232.225	224	632	S<484>	1770.385	92.975
600	S<516>	2218.225	92.975	633	S<483>	1756.385	224
601	S<515>	2204.225	224	634	S<482>	1742.385	92.975
602	S<514>	2190.225	92.975	635	S<481>	1728.385	224
603	S<513>	2176.225	224	636	S<480>	1714.425	92.975
604	S<512>	2162.265	92.975	637	S<479>	1700.425	224
605	S<511>	2148.265	224	638	S<478>	1686.425	92.975
606	S<510>	2134.265	92.975	639	S<477>	1672.425	224
607	S<509>	2120.265	224	640	S<476>	1658.425	92.975
608	S<508>	2106.265	92.975	641	S<475>	1644.425	224
609	S<507>	2092.265	224	642	S<474>	1630.425	92.975
610	S<506>	2078.265	92.975	643	S<473>	1616.425	224
611	S<505>	2064.265	224	644	S<472>	1602.465	92.975
612	S<504>	2050.305	92.975	645	S<471>	1588.465	224
613	S<503>	2036.305	224	646	S<470>	1574.465	92.975
614	S<502>	2022.305	92.975	647	S<469>	1560.465	224
615	S<501>	2008.305	224	648	S<468>	1546.465	92.975
616	S<500>	1994.305	92.975	649	S<467>	1532.465	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
650	S<466>	1518.465	92.975	683	S<433>	1056.625	224
651	S<465>	1504.465	224	684	S<432>	1042.665	92.975
652	S<464>	1490.505	92.975	685	S<431>	1028.665	224
653	S<463>	1476.505	224	686	S<430>	1014.665	92.975
654	S<462>	1462.505	92.975	687	S<429>	1000.665	224
655	S<461>	1448.505	224	688	S<428>	986.665	92.975
656	S<460>	1434.505	92.975	689	S<427>	972.665	224
657	S<459>	1420.505	224	690	S<426>	958.665	92.975
658	S<458>	1406.505	92.975	691	S<425>	944.665	224
659	S<457>	1392.505	224	692	S<424>	930.705	92.975
660	S<456>	1378.545	92.975	693	S<423>	916.705	224
661	S<455>	1364.545	224	694	S<422>	902.705	92.975
662	S<454>	1350.545	92.975	695	S<421>	888.705	224
663	S<453>	1336.545	224	696	S<420>	874.705	92.975
664	S<452>	1322.545	92.975	697	S<419>	860.705	224
665	S<451>	1308.545	224	698	S<418>	846.705	92.975
666	S<450>	1294.545	92.975	699	S<417>	832.705	224
667	S<449>	1280.545	224	700	S<416>	818.745	92.975
668	S<448>	1266.585	92.975	701	S<415>	804.745	224
669	S<447>	1252.585	224	702	S<414>	790.745	92.975
670	S<446>	1238.585	92.975	703	S<413>	776.745	224
671	S<445>	1224.585	224	704	S<412>	762.745	92.975
672	S<444>	1210.585	92.975	705	S<411>	748.745	224
673	S<443>	1196.585	224	706	S<410>	734.745	92.975
674	S<442>	1182.585	92.975	707	S<409>	720.745	224
675	S<441>	1168.585	224	708	S<408>	706.785	92.975
676	S<440>	1154.625	92.975	709	S<407>	692.785	224
677	S<439>	1140.625	224	710	S<406>	678.785	92.975
678	S<438>	1126.625	92.975	711	S<405>	664.785	224
679	S<437>	1112.625	224	712	S<404>	650.785	92.975
680	S<436>	1098.625	92.975	713	S<403>	636.785	224
681	S<435>	1084.625	224	714	S<402>	622.785	92.975
682	S<434>	1070.625	92.975	715	S<401>	608.785	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
716	S<400>	594.825	92.975	749	S<367>	132.985	224
717	S<399>	580.825	224	750	S<366>	118.985	92.975
718	S<398>	566.825	92.975	751	S<365>	104.985	224
719	S<397>	552.825	224	752	S<364>	90.985	92.975
720	S<396>	538.825	92.975	753	S<363>	76.985	224
721	S<395>	524.825	224	754	S<362>	62.985	92.975
722	S<394>	510.825	92.975	755	S<361>	48.985	224
723	S<393>	496.825	224	756	S<360>	-48.935	92.975
724	S<392>	482.865	92.975	757	S<359>	-62.935	224
725	S<391>	468.865	224	758	S<358>	-76.935	92.975
726	S<390>	454.865	92.975	759	S<357>	-90.935	224
727	S<389>	440.865	224	760	S<356>	-104.935	92.975
728	S<388>	426.865	92.975	761	S<355>	-118.935	224
729	S<387>	412.865	224	762	S<354>	-132.935	92.975
730	S<386>	398.865	92.975	763	S<353>	-146.935	224
731	S<385>	384.865	224	764	S<352>	-160.895	92.975
732	S<384>	370.905	92.975	765	S<351>	-174.895	224
733	S<383>	356.905	224	766	S<350>	-188.895	92.975
734	S<382>	342.905	92.975	767	S<349>	-202.895	224
735	S<381>	328.905	224	768	S<348>	-216.895	92.975
736	S<380>	314.905	92.975	769	S<347>	-230.895	224
737	S<379>	300.905	224	770	S<346>	-244.895	92.975
738	S<378>	286.905	92.975	771	S<345>	-258.895	224
739	S<377>	272.905	224	772	S<344>	-272.855	92.975
740	S<376>	258.945	92.975	773	S<343>	-286.855	224
741	S<375>	244.945	224	774	S<342>	-300.855	92.975
742	S<374>	230.945	92.975	775	S<341>	-314.855	224
743	S<373>	216.945	224	776	S<340>	-328.855	92.975
744	S<372>	202.945	92.975	777	S<339>	-342.855	224
745	S<371>	188.945	224	778	S<338>	-356.855	92.975
746	S<370>	174.945	92.975	779	S<337>	-370.855	224
747	S<369>	160.945	224	780	S<336>	-384.815	92.975
748	S<368>	146.985	92.975	781	S<335>	-398.815	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
782	S<334>	-412.815	92.975	815	S<301>	-874.655	224
783	S<333>	-426.815	224	816	S<300>	-888.655	92.975
784	S<332>	-440.815	92.975	817	S<299>	-902.655	224
785	S<331>	-454.815	224	818	S<298>	-916.655	92.975
786	S<330>	-468.815	92.975	819	S<297>	-930.655	224
787	S<329>	-482.815	224	820	S<296>	-944.615	92.975
788	S<328>	-496.775	92.975	821	S<295>	-958.615	224
789	S<327>	-510.775	224	822	S<294>	-972.615	92.975
790	S<326>	-524.775	92.975	823	S<293>	-986.615	224
791	S<325>	-538.775	224	824	S<292>	-1000.615	92.975
792	S<324>	-552.775	92.975	825	S<291>	-1014.615	224
793	S<323>	-566.775	224	826	S<290>	-1028.615	92.975
794	S<322>	-580.775	92.975	827	S<289>	-1042.615	224
795	S<321>	-594.775	224	828	S<288>	-1056.575	92.975
796	S<320>	-608.735	92.975	829	S<287>	-1070.575	224
797	S<319>	-622.735	224	830	S<286>	-1084.575	92.975
798	S<318>	-636.735	92.975	831	S<285>	-1098.575	224
799	S<317>	-650.735	224	832	S<284>	-1112.575	92.975
800	S<316>	-664.735	92.975	833	S<283>	-1126.575	224
801	S<315>	-678.735	224	834	S<282>	-1140.575	92.975
802	S<314>	-692.735	92.975	835	S<281>	-1154.575	224
803	S<313>	-706.735	224	836	S<280>	-1168.535	92.975
804	S<312>	-720.695	92.975	837	S<279>	-1182.535	224
805	S<311>	-734.695	224	838	S<278>	-1196.535	92.975
806	S<310>	-748.695	92.975	839	S<277>	-1210.535	224
807	S<309>	-762.695	224	840	S<276>	-1224.535	92.975
808	S<308>	-776.695	92.975	841	S<275>	-1238.535	224
809	S<307>	-790.695	224	842	S<274>	-1252.535	92.975
810	S<306>	-804.695	92.975	843	S<273>	-1266.535	224
811	S<305>	-818.695	224	844	S<272>	-1280.495	92.975
812	S<304>	-832.655	92.975	845	S<271>	-1294.495	224
813	S<303>	-846.655	224	846	S<270>	-1308.495	92.975
814	S<302>	-860.655	92.975	847	S<269>	-1322.495	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
848	S<268>	-1336.495	92.975	881	S<235>	-1798.335	224
849	S<267>	-1350.495	224	882	S<234>	-1812.335	92.975
850	S<266>	-1364.495	92.975	883	S<233>	-1826.335	224
851	S<265>	-1378.495	224	884	S<232>	-1840.295	92.975
852	S<264>	-1392.455	92.975	885	S<231>	-1854.295	224
853	S<263>	-1406.455	224	886	S<230>	-1868.295	92.975
854	S<262>	-1420.455	92.975	887	S<229>	-1882.295	224
855	S<261>	-1434.455	224	888	S<228>	-1896.295	92.975
856	S<260>	-1448.455	92.975	889	S<227>	-1910.295	224
857	S<259>	-1462.455	224	890	S<226>	-1924.295	92.975
858	S<258>	-1476.455	92.975	891	S<225>	-1938.295	224
859	S<257>	-1490.455	224	892	S<224>	-1952.255	92.975
860	S<256>	-1504.415	92.975	893	S<223>	-1966.255	224
861	S<255>	-1518.415	224	894	S<222>	-1980.255	92.975
862	S<254>	-1532.415	92.975	895	S<221>	-1994.255	224
863	S<253>	-1546.415	224	896	S<220>	-2008.255	92.975
864	S<252>	-1560.415	92.975	897	S<219>	-2022.255	224
865	S<251>	-1574.415	224	898	S<218>	-2036.255	92.975
866	S<250>	-1588.415	92.975	899	S<217>	-2050.255	224
867	S<249>	-1602.415	224	900	S<216>	-2064.215	92.975
868	S<248>	-1616.375	92.975	901	S<215>	-2078.215	224
869	S<247>	-1630.375	224	902	S<214>	-2092.215	92.975
870	S<246>	-1644.375	92.975	903	S<213>	-2106.215	224
871	S<245>	-1658.375	224	904	S<212>	-2120.215	92.975
872	S<244>	-1672.375	92.975	905	S<211>	-2134.215	224
873	S<243>	-1686.375	224	906	S<210>	-2148.215	92.975
874	S<242>	-1700.375	92.975	907	S<209>	-2162.215	224
875	S<241>	-1714.375	224	908	S<208>	-2176.175	92.975
876	S<240>	-1728.335	92.975	909	S<207>	-2190.175	224
877	S<239>	-1742.335	224	910	S<206>	-2204.175	92.975
878	S<238>	-1756.335	92.975	911	S<205>	-2218.175	224
879	S<237>	-1770.335	224	912	S<204>	-2232.175	92.975
880	S<236>	-1784.335	92.975	913	S<203>	-2246.175	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
914	S<202>	-2260.175	92.975	947	S<169>	-2722.015	224
915	S<201>	-2274.175	224	948	S<168>	-2735.975	92.975
916	S<200>	-2288.135	92.975	949	S<167>	-2749.975	224
917	S<199>	-2302.135	224	950	S<166>	-2763.975	92.975
918	S<198>	-2316.135	92.975	951	S<165>	-2777.975	224
919	S<197>	-2330.135	224	952	S<164>	-2791.975	92.975
920	S<196>	-2344.135	92.975	953	S<163>	-2805.975	224
921	S<195>	-2358.135	224	954	S<162>	-2819.975	92.975
922	S<194>	-2372.135	92.975	955	S<161>	-2833.975	224
923	S<193>	-2386.135	224	956	S<160>	-2847.935	92.975
924	S<192>	-2400.095	92.975	957	S<159>	-2861.935	224
925	S<191>	-2414.095	224	958	S<158>	-2875.935	92.975
926	S<190>	-2428.095	92.975	959	S<157>	-2889.935	224
927	S<189>	-2442.095	224	960	S<156>	-2903.935	92.975
928	S<188>	-2456.095	92.975	961	S<155>	-2917.935	224
929	S<187>	-2470.095	224	962	S<154>	-2931.935	92.975
930	S<186>	-2484.095	92.975	963	S<153>	-2945.935	224
931	S<185>	-2498.095	224	964	S<152>	-2959.895	92.975
932	S<184>	-2512.055	92.975	965	S<151>	-2973.895	224
933	S<183>	-2526.055	224	966	S<150>	-2987.895	92.975
934	S<182>	-2540.055	92.975	967	S<149>	-3001.895	224
935	S<181>	-2554.055	224	968	S<148>	-3015.895	92.975
936	S<180>	-2568.055	92.975	969	S<147>	-3029.895	224
937	S<179>	-2582.055	224	970	S<146>	-3043.895	92.975
938	S<178>	-2596.055	92.975	971	S<145>	-3057.895	224
939	S<177>	-2610.055	224	972	S<144>	-3071.855	92.975
940	S<176>	-2624.015	92.975	973	S<143>	-3085.855	224
941	S<175>	-2638.015	224	974	S<142>	-3099.855	92.975
942	S<174>	-2652.015	92.975	975	S<141>	-3113.855	224
943	S<173>	-2666.015	224	976	S<140>	-3127.855	92.975
944	S<172>	-2680.015	92.975	977	S<139>	-3141.855	224
945	S<171>	-2694.015	224	978	S<138>	-3155.855	92.975
946	S<170>	-2708.015	92.975	979	S<137>	-3169.855	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
980	S<136>	-3183.815	92.975	1013	S<103>	-3645.655	224
981	S<135>	-3197.815	224	1014	S<102>	-3659.655	92.975
982	S<134>	-3211.815	92.975	1015	S<101>	-3673.655	224
983	S<133>	-3225.815	224	1016	S<100>	-3687.655	92.975
984	S<132>	-3239.815	92.975	1017	S<99>	-3701.655	224
985	S<131>	-3253.815	224	1018	S<98>	-3715.655	92.975
986	S<130>	-3267.815	92.975	1019	S<97>	-3729.655	224
987	S<129>	-3281.815	224	1020	S<96>	-3743.615	92.975
988	S<128>	-3295.775	92.975	1021	S<95>	-3757.615	224
989	S<127>	-3309.775	224	1022	S<94>	-3771.615	92.975
990	S<126>	-3323.775	92.975	1023	S<93>	-3785.615	224
991	S<125>	-3337.775	224	1024	S<92>	-3799.615	92.975
992	S<124>	-3351.775	92.975	1025	S<91>	-3813.615	224
993	S<123>	-3365.775	224	1026	S<90>	-3827.615	92.975
994	S<122>	-3379.775	92.975	1027	S<89>	-3841.615	224
995	S<121>	-3393.775	224	1028	S<88>	-3855.575	92.975
996	S<120>	-3407.735	92.975	1029	S<87>	-3869.575	224
997	S<119>	-3421.735	224	1030	S<86>	-3883.575	92.975
998	S<118>	-3435.735	92.975	1031	S<85>	-3897.575	224
999	S<117>	-3449.735	224	1032	S<84>	-3911.575	92.975
1000	S<116>	-3463.735	92.975	1033	S<83>	-3925.575	224
1001	S<115>	-3477.735	224	1034	S<82>	-3939.575	92.975
1002	S<114>	-3491.735	92.975	1035	S<81>	-3953.575	224
1003	S<113>	-3505.735	224	1036	S<80>	-3967.535	92.975
1004	S<112>	-3519.695	92.975	1037	S<79>	-3981.535	224
1005	S<111>	-3533.695	224	1038	S<78>	-3995.535	92.975
1006	S<110>	-3547.695	92.975	1039	S<77>	-4009.535	224
1007	S<109>	-3561.695	224	1040	S<76>	-4023.535	92.975
1008	S<108>	-3575.695	92.975	1041	S<75>	-4037.535	224
1009	S<107>	-3589.695	224	1042	S<74>	-4051.535	92.975
1010	S<106>	-3603.695	92.975	1043	S<73>	-4065.535	224
1011	S<105>	-3617.695	224	1044	S<72>	-4079.495	92.975
1012	S<104>	-3631.655	92.975	1045	S<71>	-4093.495	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1046	S<70>	-4107.495	92.975	1079	S<37>	-4569.335	224
1047	S<69>	-4121.495	224	1080	S<36>	-4583.335	92.975
1048	S<68>	-4135.495	92.975	1081	S<35>	-4597.335	224
1049	S<67>	-4149.495	224	1082	S<34>	-4611.335	92.975
1050	S<66>	-4163.495	92.975	1083	S<33>	-4625.335	224
1051	S<65>	-4177.495	224	1084	S<32>	-4639.295	92.975
1052	S<64>	-4191.455	92.975	1085	S<31>	-4653.295	224
1053	S<63>	-4205.455	224	1086	S<30>	-4667.295	92.975
1054	S<62>	-4219.455	92.975	1087	S<29>	-4681.295	224
1055	S<61>	-4233.455	224	1088	S<28>	-4695.295	92.975
1056	S<60>	-4247.455	92.975	1089	S<27>	-4709.295	224
1057	S<59>	-4261.455	224	1090	S<26>	-4723.295	92.975
1058	S<58>	-4275.455	92.975	1091	S<25>	-4737.295	224
1059	S<57>	-4289.455	224	1092	S<24>	-4751.255	92.975
1060	S<56>	-4303.415	92.975	1093	S<23>	-4765.255	224
1061	S<55>	-4317.415	224	1094	S<22>	-4779.255	92.975
1062	S<54>	-4331.415	92.975	1095	S<21>	-4793.255	224
1063	S<53>	-4345.415	224	1096	S<20>	-4807.255	92.975
1064	S<52>	-4359.415	92.975	1097	S<19>	-4821.255	224
1065	S<51>	-4373.415	224	1098	S<18>	-4835.255	92.975
1066	S<50>	-4387.415	92.975	1099	S<17>	-4849.255	224
1067	S<49>	-4401.415	224	1100	S<16>	-4863.215	92.975
1068	S<48>	-4415.375	92.975	1101	S<15>	-4877.215	224
1069	S<47>	-4429.375	224	1102	S<14>	-4891.215	92.975
1070	S<46>	-4443.375	92.975	1103	S<13>	-4905.215	224
1071	S<45>	-4457.375	224	1104	S<12>	-4919.215	92.975
1072	S<44>	-4471.375	92.975	1105	S<11>	-4933.215	224
1073	S<43>	-4485.375	224	1106	S<10>	-4947.215	92.975
1074	S<42>	-4499.375	92.975	1107	S<9>	-4961.215	224
1075	S<41>	-4513.375	224	1108	S<8>	-4975.175	92.975
1076	S<40>	-4527.335	92.975	1109	S<7>	-4989.175	224
1077	S<39>	-4541.335	224	1110	S<6>	-5003.175	92.975
1078	S<38>	-4555.335	92.975	1111	S<5>	-5017.175	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1112	S<4>	-5031.175	92.975	1145	G<261>	-5535.015	224
1113	S<3>	-5045.175	224	1146	G<259>	-5549.015	92.975
1114	S<2>	-5059.175	92.975	1147	G<257>	-5563.015	224
1115	S<1>	-5073.175	224	1148	G<255>	-5576.975	92.975
1116	G<319>	-5129.135	92.975	1149	G<253>	-5590.975	224
1117	G<317>	-5143.135	224	1150	G<251>	-5604.975	92.975
1118	G<315>	-5157.135	92.975	1151	G<249>	-5618.975	224
1119	G<313>	-5171.135	224	1152	G<247>	-5632.975	92.975
1120	G<311>	-5185.135	92.975	1153	G<245>	-5646.975	224
1121	G<309>	-5199.135	224	1154	G<243>	-5660.975	92.975
1122	G<307>	-5213.135	92.975	1155	G<241>	-5674.975	224
1123	G<305>	-5227.135	224	1156	G<239>	-5688.935	92.975
1124	G<303>	-5241.095	92.975	1157	G<237>	-5702.935	224
1125	G<301>	-5255.095	224	1158	G<235>	-5716.935	92.975
1126	G<299>	-5269.095	92.975	1159	G<233>	-5730.935	224
1127	G<297>	-5283.095	224	1160	G<231>	-5744.935	92.975
1128	G<295>	-5297.095	92.975	1161	G<229>	-5758.935	224
1129	G<293>	-5311.095	224	1162	G<227>	-5772.935	92.975
1130	G<291>	-5325.095	92.975	1163	G<225>	-5786.935	224
1131	G<289>	-5339.095	224	1164	G<223>	-5800.895	92.975
1132	G<287>	-5353.055	92.975	1165	G<221>	-5814.895	224
1133	G<285>	-5367.055	224	1166	G<219>	-5828.895	92.975
1134	G<283>	-5381.055	92.975	1167	G<217>	-5842.895	224
1135	G<281>	-5395.055	224	1168	G<215>	-5856.895	92.975
1136	G<279>	-5409.055	92.975	1169	G<213>	-5870.895	224
1137	G<277>	-5423.055	224	1170	G<211>	-5884.895	92.975
1138	G<275>	-5437.055	92.975	1171	G<209>	-5898.895	224
1139	G<273>	-5451.055	224	1172	G<207>	-5912.855	92.975
1140	G<271>	-5465.015	92.975	1173	G<205>	-5926.855	224
1141	G<269>	-5479.015	224	1174	G<203>	-5940.855	92.975
1142	G<267>	-5493.015	92.975	1175	G<201>	-5954.855	224
1143	G<265>	-5507.015	224	1176	G<199>	-5968.855	92.975
1144	G<263>	-5521.015	92.975	1177	G<197>	-5982.855	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1178	G<195>	-5996.855	92.975	1211	G<129>	-6458.695	224
1179	G<193>	-6010.855	224	1212	G<127>	-6472.655	92.975
1180	G<191>	-6024.815	92.975	1213	G<125>	-6486.655	224
1181	G<189>	-6038.815	224	1214	G<123>	-6500.655	92.975
1182	G<187>	-6052.815	92.975	1215	G<121>	-6514.655	224
1183	G<185>	-6066.815	224	1216	G<119>	-6528.655	92.975
1184	G<183>	-6080.815	92.975	1217	G<117>	-6542.655	224
1185	G<181>	-6094.815	224	1218	G<115>	-6556.655	92.975
1186	G<179>	-6108.815	92.975	1219	G<113>	-6570.655	224
1187	G<177>	-6122.815	224	1220	G<111>	-6584.615	92.975
1188	G<175>	-6136.775	92.975	1221	G<109>	-6598.615	224
1189	G<173>	-6150.775	224	1222	G<107>	-6612.615	92.975
1190	G<171>	-6164.775	92.975	1223	G<105>	-6626.615	224
1191	G<169>	-6178.775	224	1224	G<103>	-6640.615	92.975
1192	G<167>	-6192.775	92.975	1225	G<101>	-6654.615	224
1193	G<165>	-6206.775	224	1226	G<99>	-6668.615	92.975
1194	G<163>	-6220.775	92.975	1227	G<97>	-6682.615	224
1195	G<161>	-6234.775	224	1228	G<95>	-6696.575	92.975
1196	G<159>	-6248.735	92.975	1229	G<93>	-6710.575	224
1197	G<157>	-6262.735	224	1230	G<91>	-6724.575	92.975
1198	G<155>	-6276.735	92.975	1231	G<89>	-6738.575	224
1199	G<153>	-6290.735	224	1232	G<87>	-6752.575	92.975
1200	G<151>	-6304.735	92.975	1233	G<85>	-6766.575	224
1201	G<149>	-6318.735	224	1234	G<83>	-6780.575	92.975
1202	G<147>	-6332.735	92.975	1235	G<81>	-6794.575	224
1203	G<145>	-6346.735	224	1236	G<79>	-6808.535	92.975
1204	G<143>	-6360.695	92.975	1237	G<77>	-6822.535	224
1205	G<141>	-6374.695	224	1238	G<75>	-6836.535	92.975
1206	G<139>	-6388.695	92.975	1239	G<73>	-6850.535	224
1207	G<137>	-6402.695	224	1240	G<71>	-6864.535	92.975
1208	G<135>	-6416.695	92.975	1241	G<69>	-6878.535	224
1209	G<133>	-6430.695	224	1242	G<67>	-6892.535	92.975
1210	G<131>	-6444.695	92.975	1243	G<65>	-6906.535	224

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1244	G<63>	-6920.495	92.975	1266	G<19>	-7228.415	92.975
1245	G<61>	-6934.495	224	1267	G<17>	-7242.415	224
1246	G<59>	-6948.495	92.975	1268	G<15>	-7256.375	92.975
1247	G<57>	-6962.495	224	1269	G<13>	-7270.375	224
1248	G<55>	-6976.495	92.975	1270	G<11>	-7284.375	92.975
1249	G<53>	-6990.495	224	1271	G<9>	-7298.375	224
1250	G<51>	-7004.495	92.975	1272	G<7>	-7312.375	92.975
1251	G<49>	-7018.495	224	1273	G<5>	-7326.375	224
1252	G<47>	-7032.455	92.975	1274	G<3>	-7340.375	92.975
1253	G<45>	-7046.455	224	1275	G<1>	-7354.375	224
1254	G<43>	-7060.455	92.975	1276	VCOM	-7368.335	92.975
1255	G<41>	-7074.455	224	1277	VCOM	-7382.335	224
1256	G<39>	-7088.455	92.975	1278	VCOM	-7396.335	92.975
1257	G<37>	-7102.455	224		DUMMY	-7427.335	92.975
1258	G<35>	-7116.455	92.975		DUMMY	-7467.335	92.975
1259	G<33>	-7130.455	224		DUMMY	-7507.33	92.975
1260	G<31>	-7144.415	92.975		DUMMY	-7547.33	92.975
1261	G<29>	-7158.415	224		DUMMY	-7587.33	92.975
1262	G<27>	-7172.415	92.975		DUMMY	-7627.325	92.975
1263	G<25>	-7186.415	224		DUMMY	-7667.325	92.975
1264	G<23>	-7200.415	92.975		A1	-7480	225
1265	G<21>	-7214.415	224		A2	7480	225

7. Command

7.1 Public command

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
No operation	W	0	0	0	0	0	0	0	0	(00h)
Software reset	W	0	0	0	0	0	0	0	1	(01h)
Read display ID	W	0	0	0	0	0	1	0	0	(04h)
	R	id[23:16]								00h
	R	id[15:8]								31h
	R	id[7:0]								35h
Read display status	W	0	0	0	0	1	0	0	1	(09h)
	R	boost_ status	madctl[7:2]						X	00h
	R	X	color_mode[2:0]			idle	partial_ mode	sleep	normal_ mode	61h
	R	scroll_ mode	X	inv_en	X	X	display_ en	tear_en	X	00h
	R	X	X	tear_mode	X	X	X	X	X	00h
Read display Power mode	W	0	0	0	0	1	0	1	0	(0Ah)
	R	boost_ status	idle	partial_ mode	sleep	normal_ mode	display_ en	X	X	08h
Read display MADCTL	W	0	0	0	0	1	0	1	1	(0Bh)
	R	madctl[7:0]								00h
Read display Pixel format	W	0	0	0	0	1	1	0	0	(0Ch)
	R	rim	dpi[2:0]			X	dbi[2:0]			66h
Read display Image mode	W	0	0	0	0	1	1	0	1	(0Dh)
	R	0	0	0	0	0	0	0	0	00h
Read display Signal mode	W	0	0	0	0	1	1	1	0	(0Eh)
	R	te_on_ off	tear_ mode	rcm[2:0]			de_ mode	X	X	3Ch
Read display self-diagnostic result	W	0	0	0	0	1	1	1	1	(0Fh)
	R	reg_load_ det	func_ det	X	X	X	X	X	X	00h
Sleep in	W	0	0	0	1	0	0	0	0	(10h)
Sleep out	W	0	0	0	1	0	0	0	1	(11h)
Partial mode on	W	0	0	0	1	0	0	1	0	(12h)

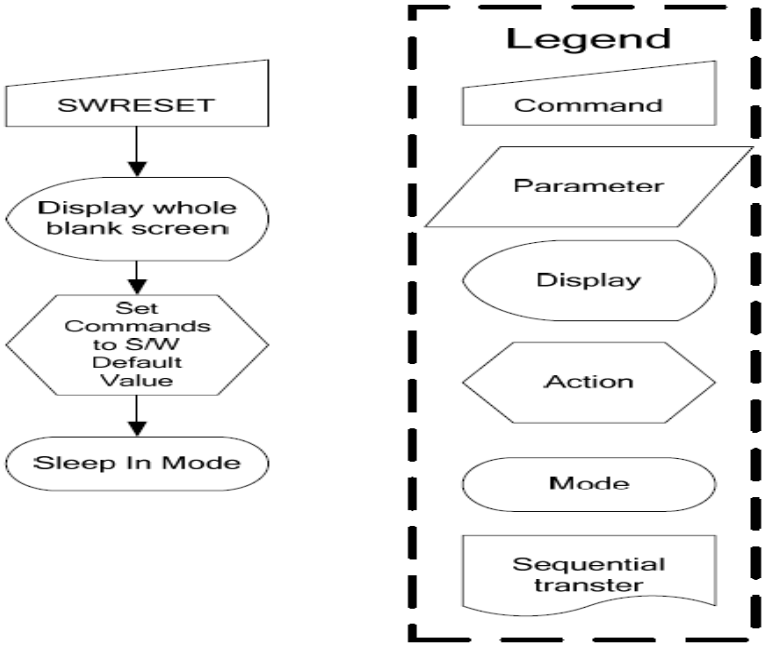
Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
normal mode on and partial mode off	W	0	0	0	1	0	0	1	1	(13h)
Display inversion off	W	0	0	1	0	0	0	0	0	(20h)
Display inversion on	W	0	0	1	0	0	0	0	1	(21h)
Display off	W	0	0	1	0	1	0	0	0	(28h)
Display on	W	0	0	1	0	1	0	0	1	(29h)
Column address	W	0	0	1	0	1	0	1	0	(2Ah)
	W	caset_sc[15:8]								00h
	W	caset_sc[7:0]								00h
	W	caset_ec[15:8]								00h
	W	caset_ec[7:0]								EFh
page address	W	0	0	1	0	1	0	1	1	(2Bh)
	W	paset_sp[15:8]								00h
	W	paset_sp[7:0]								00h
	W	paset_ep[15:8]								01h
	W	paset_ep[7:0]								3Fh
memory write	W	0	0	1	0	1	1	0	0	(2Ch)
memory read	R	0	0	1	0	1	1	1	0	(2Eh)
partial area	W	0	0	1	1	0	0	0	0	(30h)
	W	paset_sr[15:8]								00h
	W	paset_sr[7:0]								00h
	W	paset_er[15:8]								01h
	W	paset_er[7:0]								3Fh
Vertical scrolling	W	0	0	1	1	0	0	1	1	(33h)
	W	vscrdef_tfa[15:8]								00h
	W	vscrdef_tfa[7:0]								00h
	W	vscrdef_vsa[15:8]								01h
	W	vscrdef_vsa[7:0]								40h
	W	vscrdef_bfa[15:8]								00h
	W	vscrdef_bfa[7:0]								00h
Tearing effect line off	W	0	0	1	1	0	1	0	0	(34h)
Tearing effect line on	W	0	0	1	1	0	1	0	1	(35h)
	W	X	X	X	X	X	X	X	tem	00h
MADCTL (memory data access control)	W	0	0	1	1	0	1	1	0	(36h)
	W	my	mx	mv	ml	bgr	mh	X	X	00h
Vertical scrolling start address	W	0	0	1	1	0	1	1	1	(37h)
	W	vscrdef_vsp[15:8]								00h
	W	vscrdef_vsp[7:0]								00h
Idle mode off	W	0	0	1	1	1	0	0	0	(38h)
idle mode on and other mode off	W	0	0	1	1	1	0	0	1	(39h)

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Interface pixel format	W	0	0	1	1	1	0	1	0	(3Ah)
	W	X	dpi[2:0]			X	dbi[2:0]			66h
write memory continue	W	0	0	1	1	1	1	0	0	(3Ch)
read memory continue	W	0	0	1	1	1	1	1	0	(3Eh)
Set tear scanline	W	0	1	0	0	0	1	0	0	(44h)
	W	X	X	X	X	X	X	X	sts[8]	00h
	W	sts[7:0]								00h
Get tear scan line	W	0	1	0	0	0	1	0	1	(45h)
	R	X	X	X	X	X	X	gts[9:8]		00h
	R	gts[7:0]								00h
read idd3	W	1	1	0	1	0	0	1	1	(D3h)
	R	id[23:16]								00h
	R	id[15:8]								31h
	R	id[7:0]								35h
read display id 1	W	1	1	0	1	1	0	1	0	(DAh)
	R	id[23:16]								00h
read display id 2	W	1	1	0	1	1	0	1	1	(DBh)
	R	id[15:8]								31h
read display id 3	W	1	1	0	1	1	1	0	0	(DCh)
	R	id[7:0]								35h

7.1.1 no operation (00h)

<table>
<tr><th>00h</th><th colspan="10">no operation</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>no operation</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(00h)</td></tr>
<tr><td>Parameter</td><td colspan="9">No Parameter.</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is empty command.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

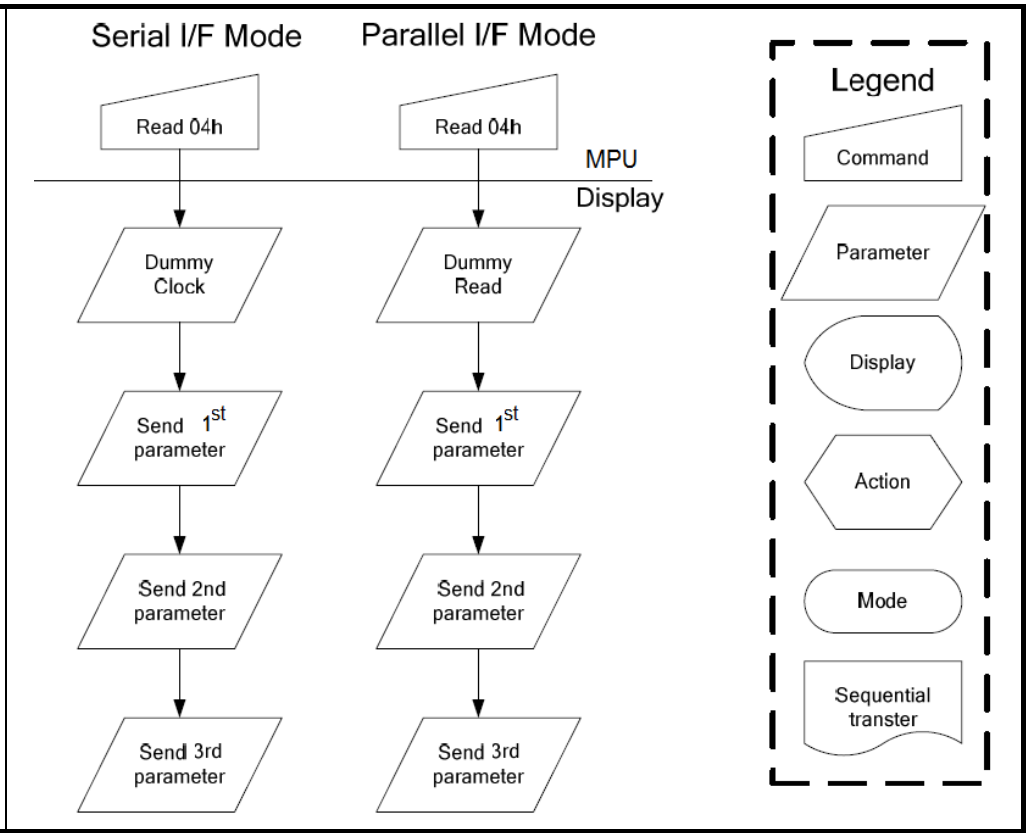
7.1.2 software reset (01h)

<table>
<tr><th>01h</th><th colspan="10">software reset</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>software reset</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(01h)</td></tr>
<tr><td>Parameter</td><td colspan="9">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">The display module performs a software reset, registers are written with their SW reset default values.Frame memory contents are unaffected by this command.“-“ Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">It will be necessary to wait 5msec before sending new command following software reset.
The display module loads all display suppliers’ factory default values to the registers during this 5msec.If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command.Software reset command cannot be sent during sleep out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.3 read display ID (04h)

<table>
<tr><th>04h</th><th colspan="10">read display ID</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display ID</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(04h)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id[23:16]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>R</td><td colspan="8">id[15:8]</td><td>31h</td></tr>
<tr><td>3rd parameter</td><td>R</td><td colspan="8">id[7:0]</td><td>35h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 24-bit display identification information.
id[23:0]:LCD module/driver ID.
Commands RDID1/2/3(Dah, DBh, DCh) read data correspond to the parameters 1,2,3 of the command 04h,respectively.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>id[23:16]</th><th>id[15:8]</th><th>id[7:0]</th></tr><tr><td>Power On Sequence</td><td>00h</td><td>31h</td><td>35h</td></tr><tr><td>S/W Reset</td><td>00h</td><td>31h</td><td>35h</td></tr><tr><td>H/W Reset</td><td>00h</td><td>31h</td><td>35h</td></tr></table></td></tr>
</table>

Flow Chart



7.1.4 read display status (09h)

09h	read display status									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display status	W	0	0	0	0	1	0	0	1	(09h)
1st parameter	R	boost_status	madctl[7:2]						X	00h
2nd parameter	R	X	color_mode[2:0]			idle	partial_mode	sleep	normal_mode	61h
3rd parameter	R	scroll_mode	X	inv_en	X	X	display_en	tear_en	X	00h
4th parameter	R	X	X	tear_mode	X	X	X	X	X	00h

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Comment
boost_status	Booster Voltage Status	0	Booster Off
		1	Booster On
madctl [7...2]	Page Address Order	0	Top to Bottom (When memory data access control D7 = '0')
		1	Bottom to Top (When memory data access control D7 = '1')
	Column Address Order	0	Left to Right (When memory data access control D6 = '0')
		1	Right to Left (When memory data access control D6 = '1')
	Page/Column Order	0	Normal Mode (When memory data access control D5 = '0')
		1	Reverse Mode (When memory data access control D5 = '1')
	Line Address Order	0	LCD Refresh Top to Bottom (When memory data access control D4 = '0')
		1	LCD Refresh Bottom to Top (When memory data access control D4 = '1')
	RGB/BGR Order	0	RGB (When memory data access control D3 = '0')
		1	BGR (When memory data access control D3 = '1')
	mh	-	Reserved
idle	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
partial_mode	Partial Mode On/Off	0	Partial Mode Off
		1	Partial Mode On
sleep	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
normal_mode	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
scroll_mode	Vertical Scrolling Status	0	Vertical Scrolling is Off
		1	Vertical Scrolling is On
inv_en	Inversion Status	0	Inversion is Off
		1	Inversion is On
display_en	Display On/Off	0	Display is Off
		1	Display is On
tear_en	Tearing Effect Line On/Off	0	Tearing Effect Line Off
		1	Tearing Effect Line On
tear_mode	Tearing Effect Output Line Mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking
D[4…0]	For Future Use	0	Set to '0'
Others	-	0	Set to '0'

Bits color_mode[2:0]: Interface Color Pixel Format Definition.

Interface Format	color_mode[2]	color_mode[1]	color_mode[0]
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

Note:

1. For Bits madctl [7:5], also refer to Section 8.2.3 MPU to memory write/read direction.
2. For Bits madctl [4:2] also refer to 7.1.27 memory data access control (36h).

"-" Don't care.

Restriction

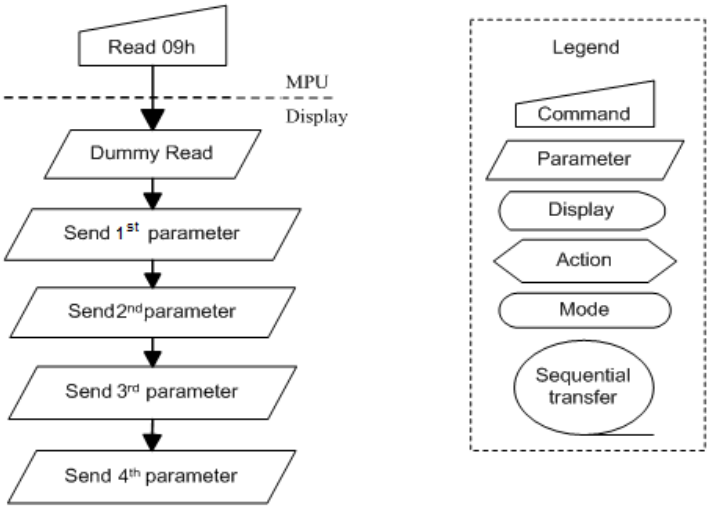
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

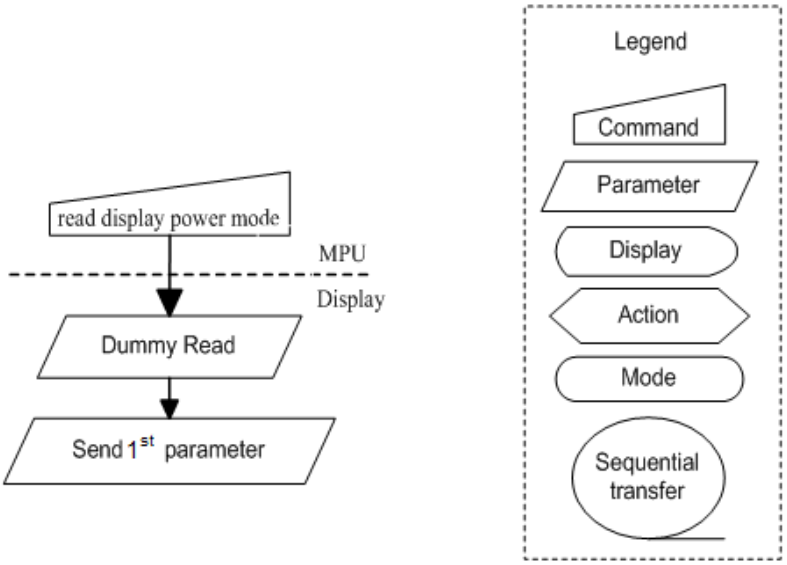
Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart



7.1.5 read display power mode (0Ah)

<table>
<tr><th>0Ah</th><th colspan="10">read display power mode</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display power mode</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(0Ah)</td></tr>
<tr><td>parameter</td><td>R</td><td>boost_status</td><td>idle</td><td>partial_mode</td><td>sleep</td><td>normal_ mode</td><td>display_ en</td><td>X</td><td>X</td><td>08h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">boost_status</td><td rowspan="2">Booster Voltage Status</td><td>0</td><td>Booster Off or has a fault</td></tr>
<tr><td>1</td><td>Booster On and working OK</td></tr>
<tr><td rowspan="2">idle</td><td rowspan="2">Idle Mode On/Off</td><td>0</td><td>Idle Mode Off</td></tr>
<tr><td>1</td><td>Idle Mode On</td></tr>
<tr><td rowspan="2">partial_mode</td><td rowspan="2">Partial Mode On/Off</td><td>0</td><td>Partial Mode Off</td></tr>
<tr><td>1</td><td>Partial Mode On</td></tr>
<tr><td rowspan="2">sleep</td><td rowspan="2">Sleep In/Out</td><td>0</td><td>Sleep In Mode</td></tr>
<tr><td>1</td><td>Sleep Out Mode</td></tr>
<tr><td rowspan="2">normal_mode</td><td rowspan="2">Display Normal Mode On/Off</td><td>0</td><td>Display Normal Mode Off</td></tr>
<tr><td>1</td><td>Display Normal Mode On</td></tr>
<tr><td rowspan="2">display_en</td><td rowspan="2">Display On/Off</td><td>0</td><td>Display Off</td></tr>
<tr><td>1</td><td>Display On</td></tr>
<tr><td>others</td><td>-</td><td>0</td><td>Set to ‘0’</td></tr>
</table>
“X“ Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>08h</td></tr>
<tr><td>S/W Reset</td><td>08h</td></tr>
<tr><td>H/W Reset</td><td>08h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

7.1.6 read display MADCTL (0Bh)

0Bh	read display MADCTL									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display MADCTL	W	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	R	madctl[7:0]								00h

Description

This command indicates the current status of the display as described in the table below:

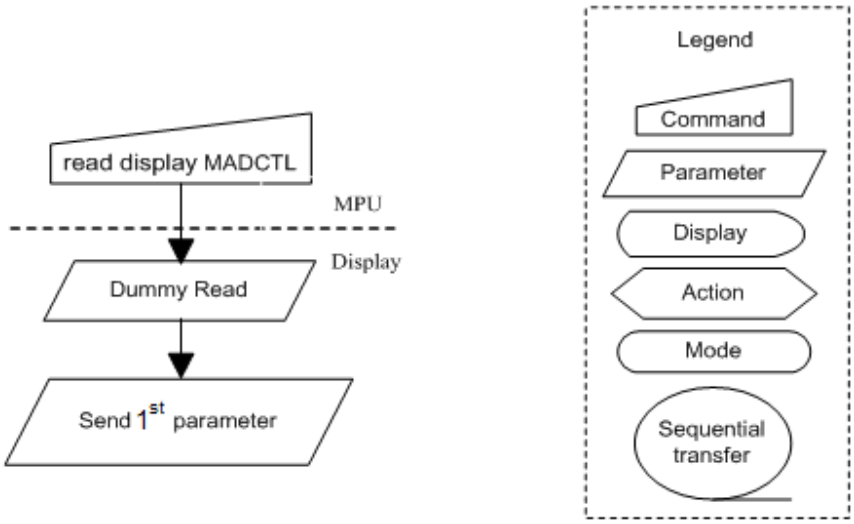
Bit	Description	Value	Comment
Madctl[7]	Page Address Order	0	Top to Bottom (When memory data access control D7='0').
		1	Bottom to Top (When memory data access control D7='1').
Madctl[6]	Column Address Order	0	Left to Right (When memory data access control D6='0')
		1	Right to Left (when memory data access control D6='1'
Madctl[5]	Page/Column Order	0	Normal Mode (When memory data access control D5='0').
		1	Reverse Mode (When memory data access control D5='1')
Madctl[4]	Line Address Order	0	LCD Refresh Top to Bottom (When memory data access control D4='0')
		1	LCD Refresh Bottom to Top (When memory data access control D4='1')
Madctl[3]	RGB/BGR Order	0	RGB (When memory data access control D3='0')
		1	"1": BGR (When memory data access control D3='1')
Madctl[2]	mh	-	Reserved
others	-	0	Set to '0'

Note:

1. For Bits Madctl[7…5], also refer to Section 8.2.3 MPU to memory write/read direction.
2. For Bits Madctl [4:2] also refer to 7.1.27 memory dataaccess control (36h).

"X" Don't care.

Restriction

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

7.1.7 read display pixel format (0Ch)

0Ch	read display pixel format									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display pixel format	W	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	R	rim	dpi[2:0]			X	dbi[2:0]			66h

Description

This command indicates the current status of the display as described in the table below:

rim	dpi[2:0]			RGB interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16bit/pixel
0	1	1	0	18bit/pixel
0	1	1	1	Reserved
1	1	0	1	16bit/pixel(6-bit 3 times data transfer)
1	1	1	0	18bit/pixel(6-bit 3 times data transfer)

dbi[2:0]			system Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16bit/pixel
1	1	0	18bit/pixel
1	1	1	Reserved

Restriction

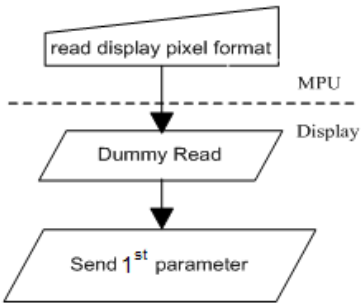
Register Availability

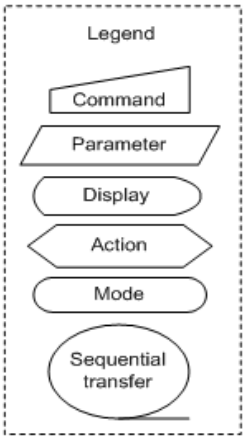
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
S/W Reset	No change
H/W Reset	66h

Flow Chart





7.1.8 read display image mode (0Dh)

0Dh	read display image mode									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display image mode	W	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	R	0	0	0	0	0	0	0	0	00h
Restriction										

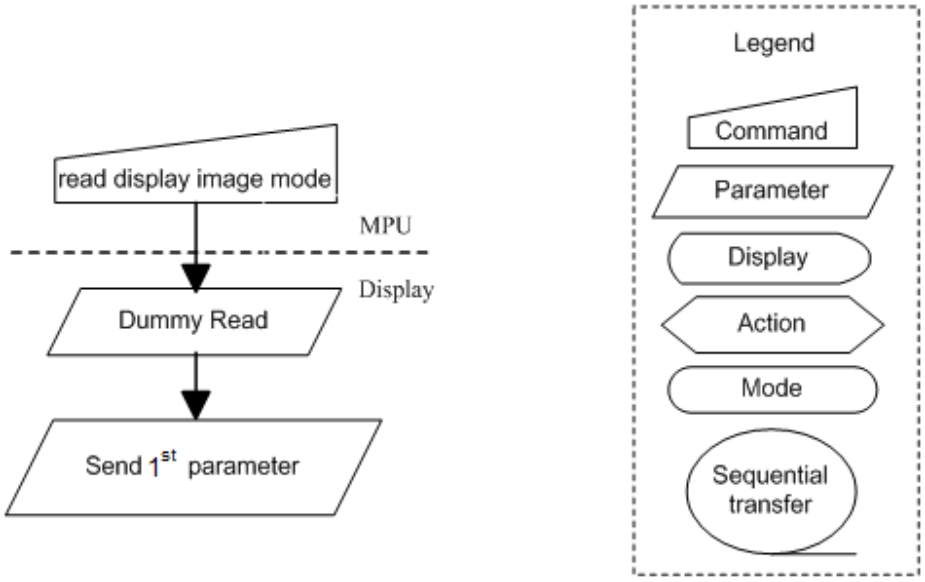
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

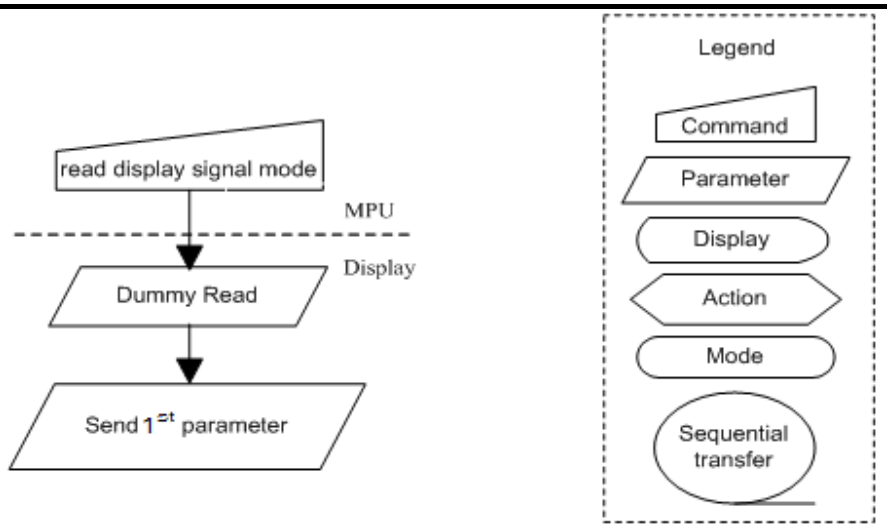
Status	Default Value
Power On Sequence	00h
S/W Reset	no change
H/W Reset	00h

Flow Chart



7.1.9 read display signal mode (0Eh)

<table>
<tr><th>0Eh</th><th colspan="10">read display signal mode</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display signal mode</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(0Eh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td>te_on_off</td><td>tear_mode</td><td>rcm[1]</td><td>rcm[1]</td><td>rcm[1]</td><td>de_mode</td><td>X</td><td>X</td><td>3Ch</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">te_on_off</td><td>0</td><td>Tearing Effect Line Off</td></tr>
<tr><td>1</td><td>Tearing Effect Line On</td></tr>
<tr><td rowspan="2">tear_mode</td><td>0</td><td>Mode 1（Tearing Effect Line Output Mode, see section 8.4.1）</td></tr>
<tr><td>1</td><td>Mode 2（Tearing Effect Line Output Mode, see section 8.4.1）</td></tr>
<tr><td>de_mode</td><td>-</td><td>RGB DE mode.</td></tr>
</table>
<table>
<tr><th>rcm[1]</th><th>de_mode</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td rowspan="2">MCU interface</td></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>DE mode</td></tr>
<tr><td>1</td><td>1</td><td>SYNC mode</td></tr>
</table>
“X” Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>3Ch</td></tr>
<tr><td>S/W Reset</td><td>3Ch</td></tr>
<tr><td>H/W Reset</td><td>3Ch</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>



7.1.10 read display self-diagnostic result (0Fh)

0Fh	read display self-diagnostic result									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display self-diagnostic result	W	0	0	0	0	1	1	1	1	(0Fh)
parameter	R	reg_load_det	func_det	X	X	X	X	X	X	00h

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Action
reg_load_det	Register loading detection	Inverting the D7 bit if registers values loading work properly
func_det	Functionality detection	Inverting the D6 bit if the display is on function
others	-	Set to‘0’

“X”Don’t care.

Restriction

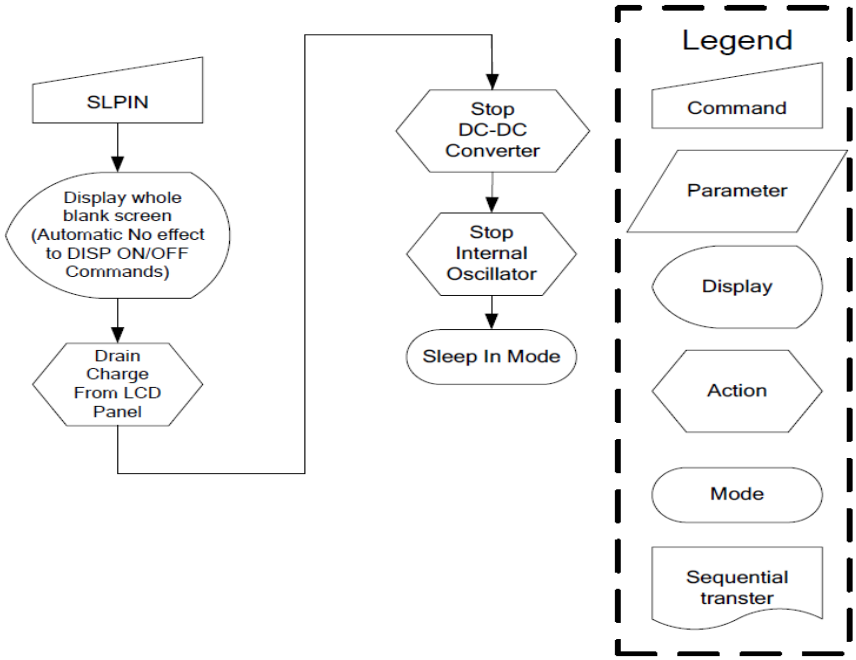
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

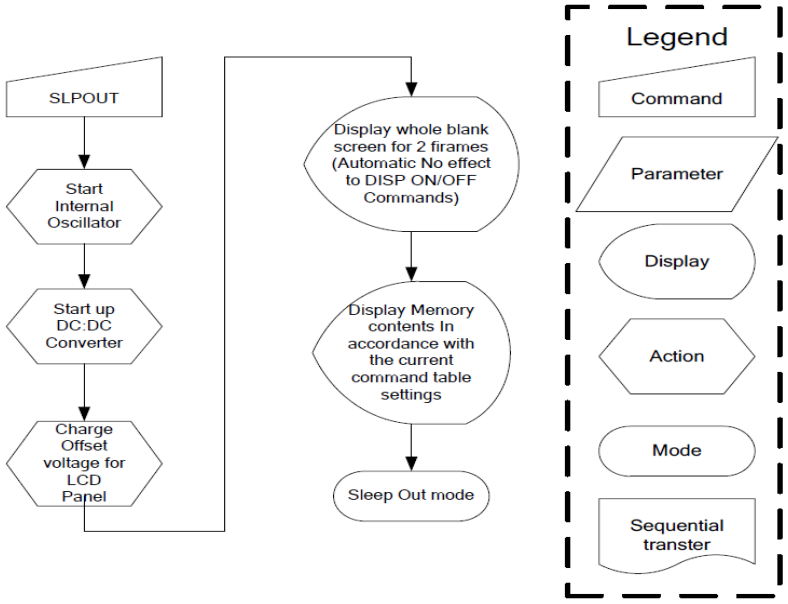
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

7.1.11 sleep in (10h)

<table>
<tr><th>10h</th><th colspan="10">sleep in</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>sleep in</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(10h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the LCD module to enter the minimum power consumption mode.
In this mode the DC-DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped.
Interface and memory are still working and the memory keeps its contents.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h).
It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.12 sleep out (11h)

11h	sleep out									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
sleep out	W	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter									
Description	This command turn off sleep mode. In this mode the DC-DC converter is enabled, internal display oscillator is started, and panel scanning is started.									
Restriction	This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h). It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode)before sending an sleep in command. The display module runs the self-diagnostic functions after this command is received.									
Register Availability										
Default										
Flow Chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

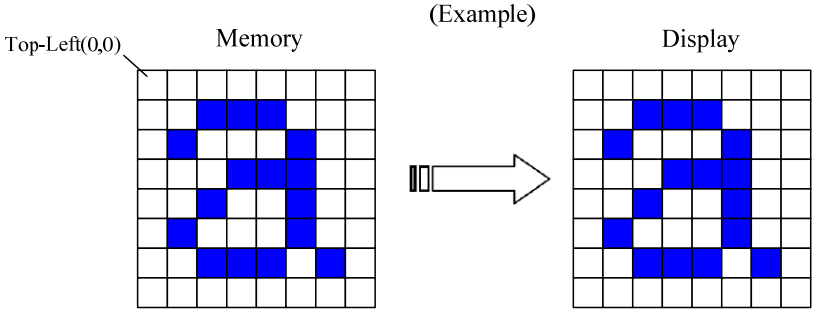
7.1.13 partial mode on (12h)

<table>
<tr><th>12h</th><th colspan="9">partial mode on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>partial mode on</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(12h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h).
To leave Partial mode, the Normal Display Mode On command (13h) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode on</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode on</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode on</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10">See Partial Area (30h).</td></tr>
</table>

7.1.14 normal mode on and partial mode off (13h)

<table>
<tr><th>13h</th><th colspan="10">normal mode on and partial mode off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>normal mode on and partial mode off</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(13h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command turns the display to normal mode.
Normal display mode on means partial mode off.
Exit from normal mode on by the partial mode on command.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when normal display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal display mode on</td></tr><tr><td>S/W Reset</td><td>Normal display mode on</td></tr><tr><td>H/W Reset</td><td>Normal display mode on</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10">See Partial Area (30h).</td></tr>
</table>

7.1.15 display inversion off (20h)

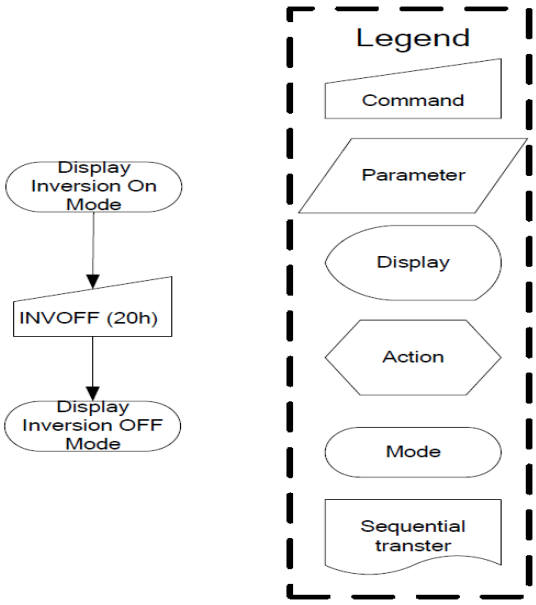
20h	display inversion off									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
display inversion off	W	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter									
Description	This command is used to recover from display inversion mode. (Example) Top-Left(0,0) Memory Display 									
Restriction	This command has no effect when module is already in inversion off mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

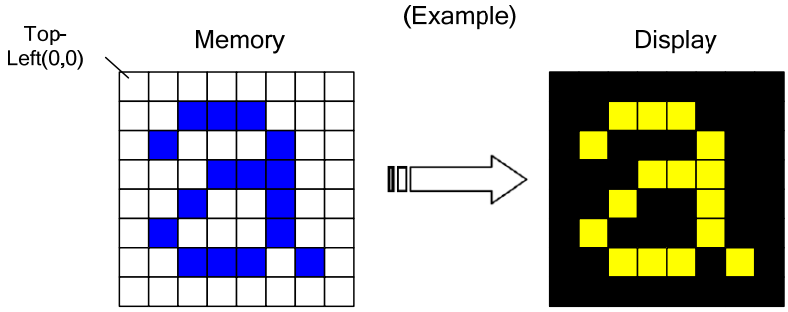
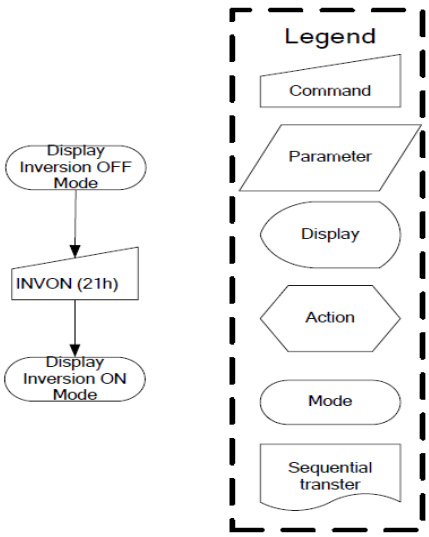
Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

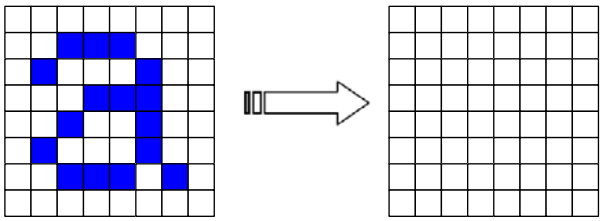
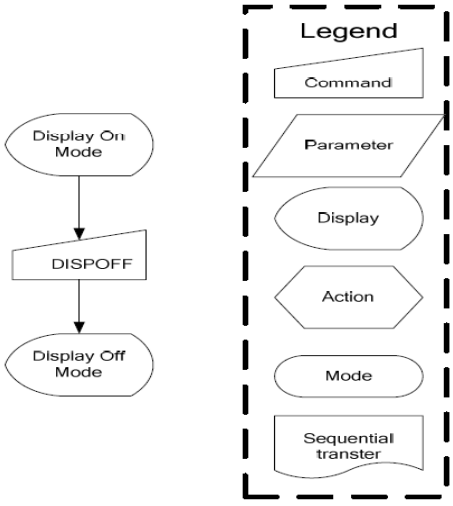
Flow Chart



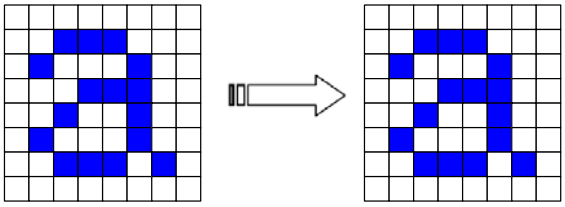
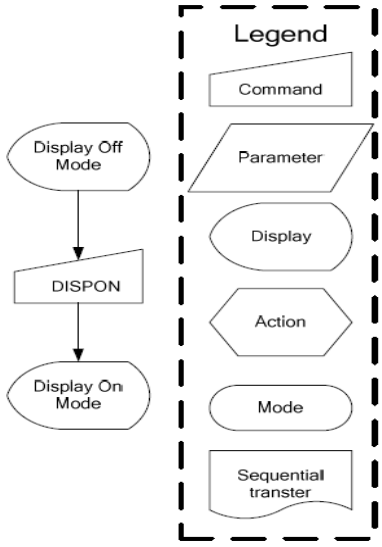
7.1.16 display inversion on (21h)

<table>
<tr><th>21h</th><th colspan="9">display inversion on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display inversion on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(21h)</td></tr>
<tr><td>parameter</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to enter into display inversion mode.
 
</td></tr>
<tr><td>Restriction</td><td colspan="9">This command has no effect when module is already in inversion on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="9"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="9"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Display inversion off</td></tr>
<tr><td>S/W Reset</td><td>Display inversion off</td></tr>
<tr><td>H/W Reset</td><td>Display inversion off</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="9"> 
</td></tr>
</table>

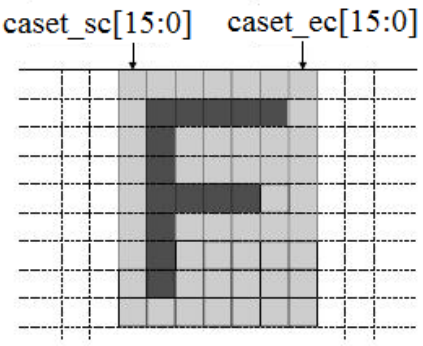
7.1.17 display off (28h)

<table>
<tr><th>28h</th><th colspan="9">display off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(28h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into display off mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h) .
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

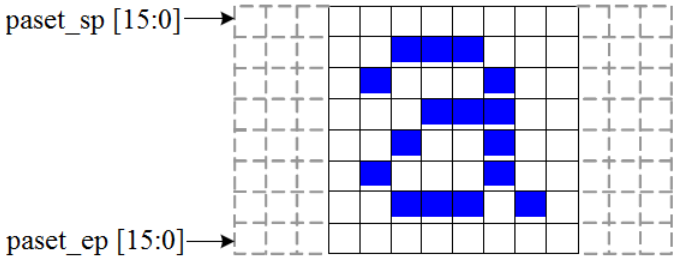
7.1.18 display on (29h)

<table>
<tr><th>29h</th><th colspan="9">display on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>(29h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from display off mode.
Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.19 column address (2Ah)

<table>
<tr><th>2Ah</th><th colspan="10">column address</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>column address</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(2Ah)</td></tr>
<tr><td>1st parameter</td><td>W</td><td colspan="8">caset_sc[15:8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">caset_sc[7:0]</td><td>00h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td colspan="8">caset_ec[15:8]</td><td>00h</td></tr>
<tr><td>4th parameter</td><td>W</td><td colspan="8">caset_ec[7:0]</td><td>EFh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to define area of frame memory where system interface can access. This command makes no change on the other driver status.
The values of caset_sc[15:0] and caset_ec[15:0] are referred when memory write command comes. Each value represents one column line in the Frame Memory.
(Example)
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">caset_sc [15:0] always must be equal to or less than caset_ec [15:0].
When caset_sc [15:0] or caset_ec [15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 < caset_sc [15:0] < caset_ec [15:0] < =239(00EFh)): mv=”0”)
(Parameter range: 0 < caset_sc [15:0] < caset_ec [15:0] < =319(013Fh)): mv=”1”)</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>caset_sc[15:0]</th><th>caset_ec[15:0]</th></tr><tr><td>Power On Sequence</td><td>0000h</td><td>00EFh</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>If MADCTL’s D5=0: caset_ec[15:0]=00EFh
If MADCTL’s D5=1: caset_ec[15:0]=013Fh</td></tr><tr><td>H/W Reset</td><td>0000h</td><td>00EFh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.20 page address (2Bh)

<table>
<tr><th>2Bh</th><th colspan="10">page address</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>page address</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>(2Bh)</td></tr>
<tr><td>1st parameter</td><td>W</td><td colspan="8">paset_sp[15:8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">paset_sp[7:0]</td><td>00h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td colspan="8">paset_ep[15:8]</td><td>01h</td></tr>
<tr><td>4th parameter</td><td>W</td><td colspan="8">paset_ep[7:0]</td><td>3Fh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to defined area of frame memory where system interface can access.
The value of paset_sp [15:0] and paset_ep [15:0] are referred when memory write command comes.
Each value represents one page line in the Frame Memory.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">paset_sp[15:0] always must be equal to or less than paset_ep[15:0].
When paset_sp[15:0] or paset_ep[15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 < paset_sp[15:0] < paset_ep[15:0] <239 (00EFh)): mv=”1”)
(Parameter range: 0 < paset_sp[15:0] < paset_ep[15:0] <319 (013Fh)): mv=”0”)</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>paset_sp[15:0]</th><th>paset_ep[15:0]</th></tr><tr><td>Power On Sequence</td><td>0000h</td><td>013Fh</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>If MADCTL’s D5=0: paset_ep[15:0]=013Fh
If MADCTL’s D5=1: paset_ep[15:0]=00EFh</td></tr><tr><td>H/W Reset</td><td>0000h</td><td>013Fh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

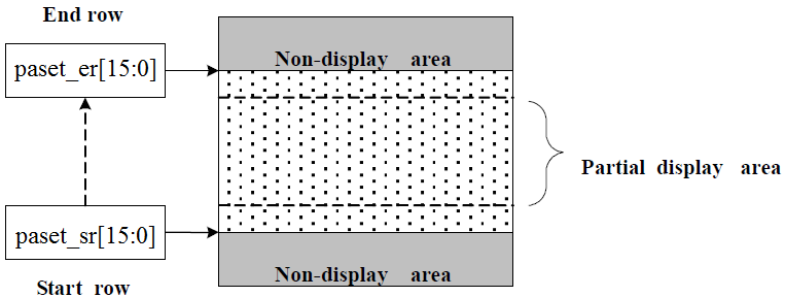
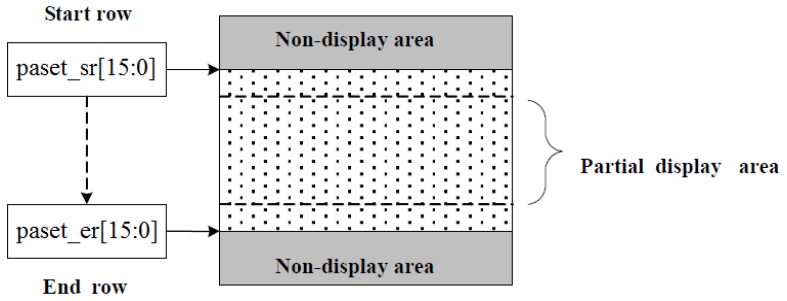
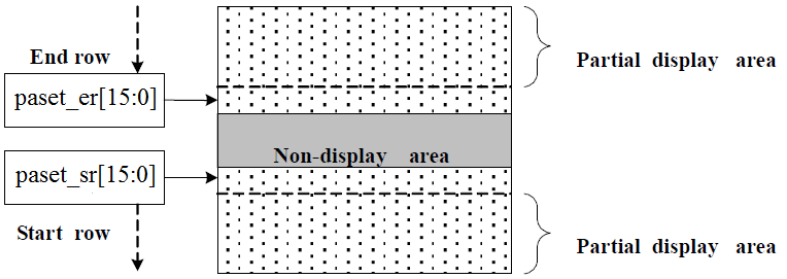
7.1.21 memory write (2Ch)

<table>
<tr><th>2Ch</th><th colspan="10">memory write</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>memory write</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(2Ch)</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to transfer data from MPU to frame memory.
When this command is accepted, the column register and the page register are reset to the start column/start page positions.
The start column/start page positions are different in accordance with MADCTL setting.
Sending any other command can stop frame write.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

7.1.22 memory read (2Eh)

<table>
<tr><th>2Eh</th><th colspan="10">memory read</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>memory read</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(2Eh)</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to transfer data from frame memory to MPU.
When this command is accepted, the column register and the page register are reset to the Start Column/Start page positions.
The Start Column/Start page positions are different in accordance with MADCTL setting.
Frame Read can be cancelled by sending any other command.
The data color coding is fixed to 18-bit in reading function. Please see section 8.3.4.9 “ Read Memory Data Color Coding” for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

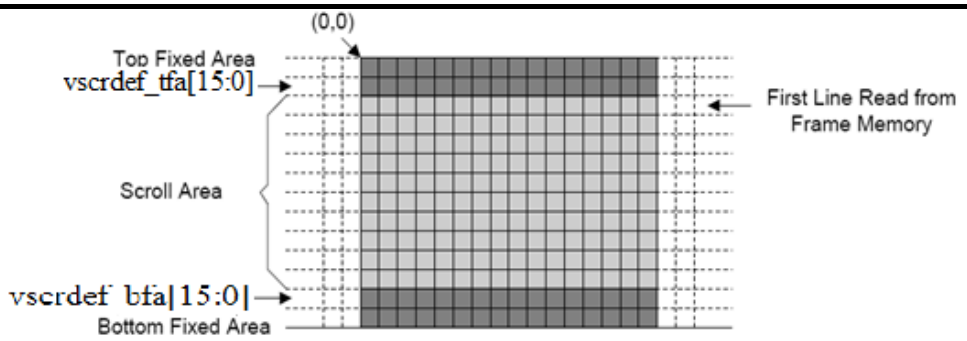
7.1.23 partial area (30h)

30h	partial area									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
partial area	W	0	0	1	1	0	0	0	0	(30h)
1st parameter	W	paset_sr[15:8]								00h
2nd parameter	W	paset_sr[7:0]								00h
3rd parameter	W	paset_er[15:8]								01h
4th parameter	W	paset_er[7:0]								3Fh
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (paset_sr[15:0]) and the second the End Row (paset_er[15:0]), as illustrated in the figures below. paset_sr[15:0] and paset_er[15:0] refer to the Frame Memory row address counter. If End Row > Start Row, when MADCTL ml='1'  If End Row > Start Row, when MADCTL ml='0'  If End Row < Start Row, when MADCTL ml='0'  If End Row = Start Row then the Partial Area will be one row deep.									
Restriction	paset_sr[15:0] and paset_er[15:0] cannot be 0000h nor exceed 013Fh.									

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>paset_sr[15:0]</th><th>paset_er[15:0]</th></tr><tr><td>Power On Sequence</td><td>0000h</td><td>013Fh</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>013Fh</td></tr><tr><td>H/W Reset</td><td>0000h</td><td>013Fh</td></tr></table>
Flow Chart	

7.1.24 vertical scrolling (33h)

33h	**vertical scrolling**									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vertical scrolling	W	0	0	1	1	0	0	1	1	(33h)
1st parameter	W	vscrdef_tfa[15:8]								00h
2nd parameter	W	vscrdef_tfa[7:0]								00h
3rd parameter	W	vscrdef_vsa[15:8]								01h
4th parameter	W	vscrdef_vsa[7:0]								40h
5th parameter	W	vscrdef_bfa[15:8]								00h
6th parameter	W	vscrdef_bfa[7:0]								00h
Description	This command defines the Vertical Scrolling Area of the display. **When MADCTL ml = '0'** The 1st &2nd parameter vscrdef_tfa[15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd &4th parameter vscrdef_vsa[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter vscrdef_bfa[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). vscrdef_tfa[15:0], vscrdef_vsa[15:0] and vscrdef_bfa[15:0] refer to the Frame Memory Line Pointer.									

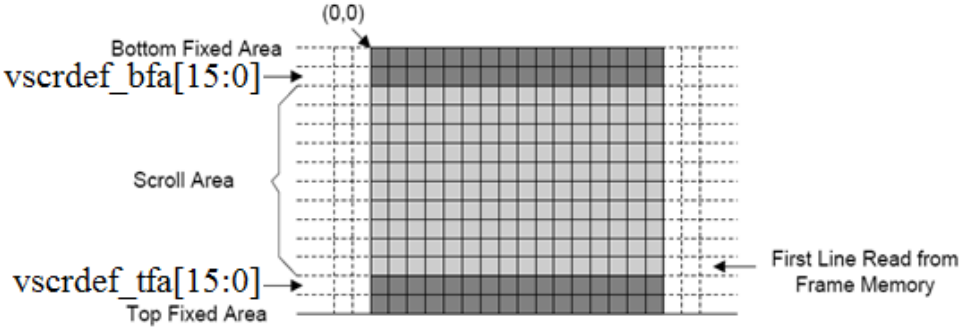


When MADCTL ml = '1'

The 1st &2nd parameter vscrdef_tfa[15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd &4th parameter vscrdef_vsa[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th &6th parameter vscrdef_bfa[15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



See also Section 8.2.2.2 and 8.2.2.3 for details of Vertical Scroll Mode and Vertical Scroll example.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	vscrdef_tfa[15:0]	vscrdef_vsa[15:0]	vscrdef_bfa[15:0]
Power On Sequence	0000h	0140h	0000h
S/W Reset	0000h	0140h	0000h
H/W Reset	0000h	0140h	0000h

Flow Chart

7.1.25 tearing effect line off (34h)

34h	tearing effect line off									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
tearing effect line off	W	0	0	1	1	0	1	0	0	(34h)
parameter	No Parameter									
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when tearing effect output is already off.									

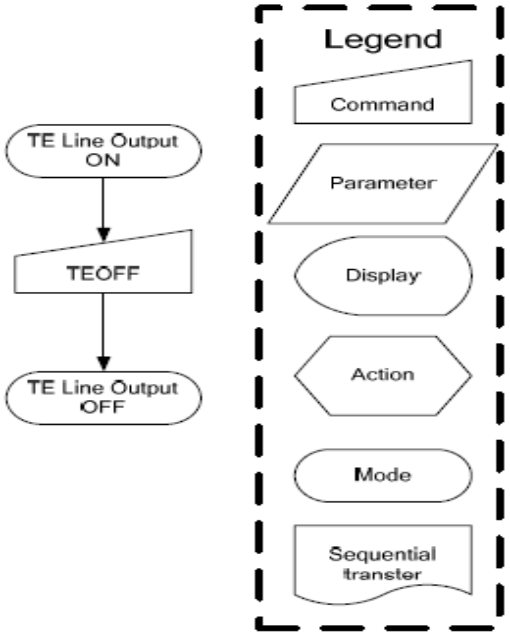
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

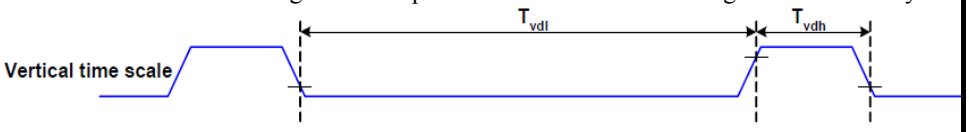
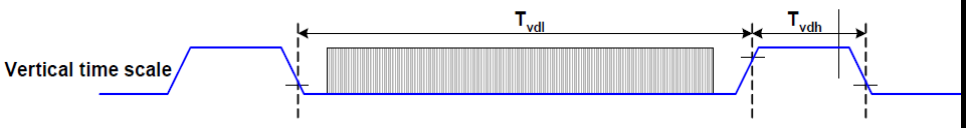
Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



7.1.26 tearing effect line on (35h)

35h	tearing effect line on									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
tearing effect line on	W	0	0	1	1	0	1	0	1	(35h)
parameter	W	X	X	X	X	X	X	X	tem	00h
Description	This command is used to turn on the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ml. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. When tem ='0': The Tearing Effect output line consists of V-Blanking information only:  When tem ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information:  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.									
Restriction	This command has no effect when tearing effect output is already on.									
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes									
Default	Status: Default Value Power On Sequence: 00h S/W Reset: 00h H/W Reset: 00h									

7.1.27 MADCTL(memory data access control) (36h)

36h	MADCTL(memory data access control)									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
MADCTL(memory data access control)	W	0	0	1	1	0	1	1	0	(36h)
parameter	W	my	mx	mv	ml	bgr	mh	X	X	00h
Description	This command defines read/write scanning direction of frame memory.									

Bit	name	Description
D7	my	Page Address Order
D6	mx	Column Address Order
D5	mv	Page/Column Order
D4	ml	Line Address Order
D3	bgr	RGB/BGR Order
D2	mh	Reserved

-Bit Assignment

Bit D7- Page Address Order

"0" = Top to Bottom (When MADCTL D7="0").

"1" = Bottom to Top (When MADCTL D7="1").

Bit D6- Column Address Order

"0" = Left to Right (When MADCTL D6="0").

"1" = Right to Left (When MADCTL D6="1").

Bit D5- Page/Column Order

"0" = Normal Mode (When MADCTL D5="0").

"1" = Reverse Mode (When MADCTL D5="1")

Bit D4- Line Address Order

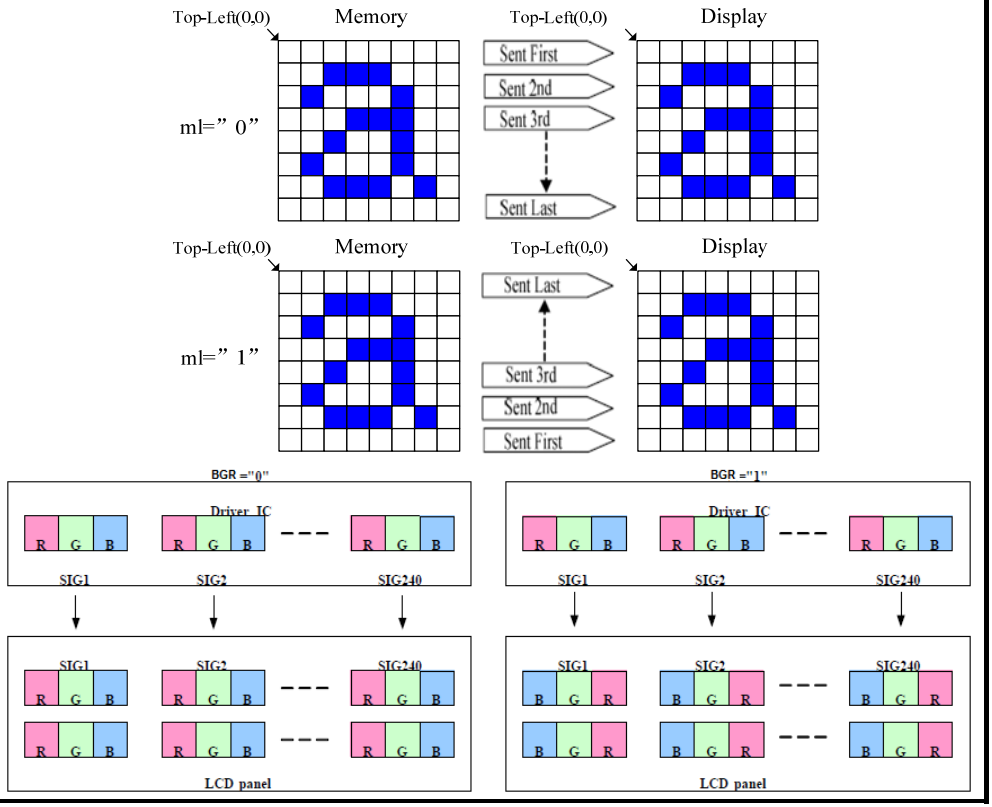
"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

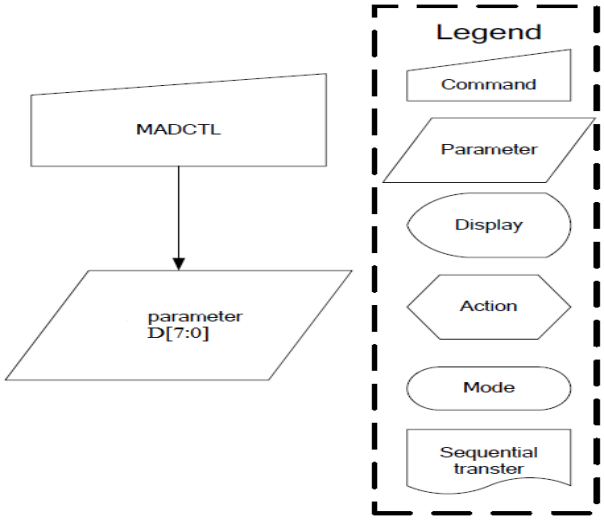
"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

Bit D3- RGB/BGR Order

"0" = RGB (When MADCTL D3="0")

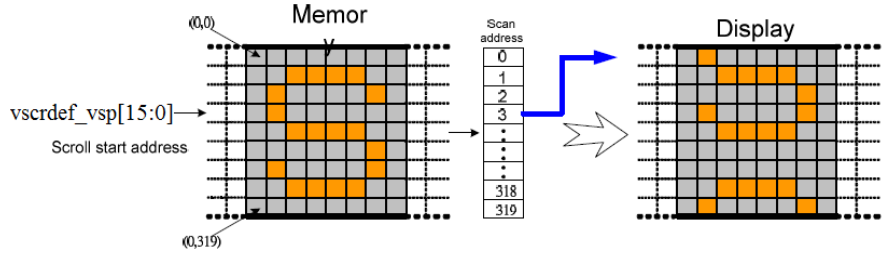
"1" = BGR (When MADCTL D3="1")

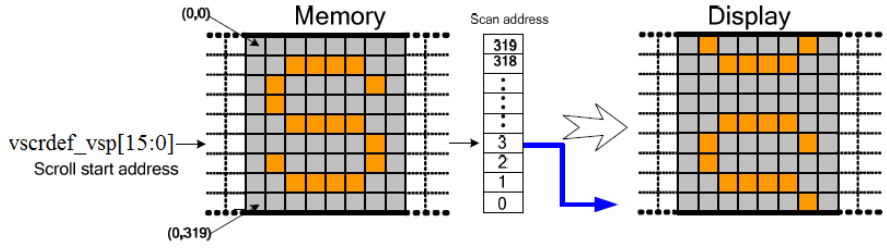


<table>
<tr><td></td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

7.1.28 vertical scrolling start address (37h)

37h	vertical scrolling start address									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vertical scrolling start address	W	0	0	1	1	0	1	1	1	(37h)
1st parameter	W	vscrdef_vsp[15:8]								00h
2nd parameter	W	vscrdef_vsp[7:0]								00h

<table>
<tr><td>Description</td><td>
This command is used together with Vertical scrolling (33h).
These two commands describe the scrolling area and the scrolling mode.
The Vertical scrolling start address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
When ml=’0’
Example:
When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vscrdef_vsp = ‘3’.


When ml=’1’
Example:
When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vscrdef_vsp = ‘3’.


Note: When new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect.
Vscrdef_vsp refers to the Frame Memory line pointer.
</td></tr>
<tr><td>Restriction</td><td>Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by vertical scrolling (33h)- otherwise undesirable image will be displayed on the panel).</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.1.29 idle mode off (38h)

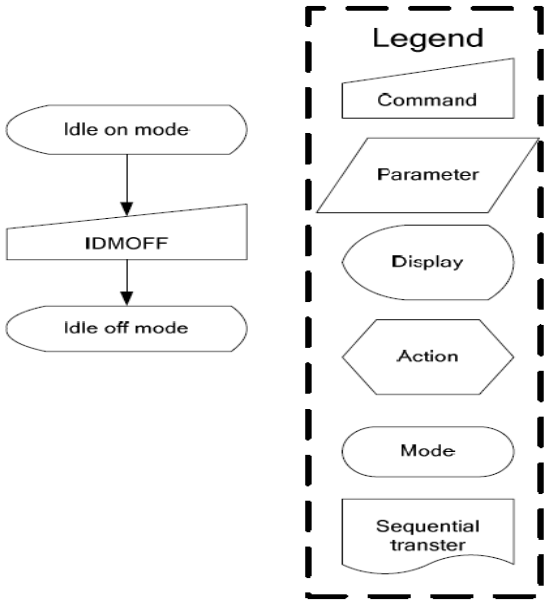
38h	idle mode off									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
idle mode off	W	0	0	1	1	1	0	0	0	(38h)
parameter	No Parameter									
Description	This command is used to recover from idle mode on. In the idle off mode 1. LCD can display 65k or 262k colors. 2. Normal frame frequency is applied.									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

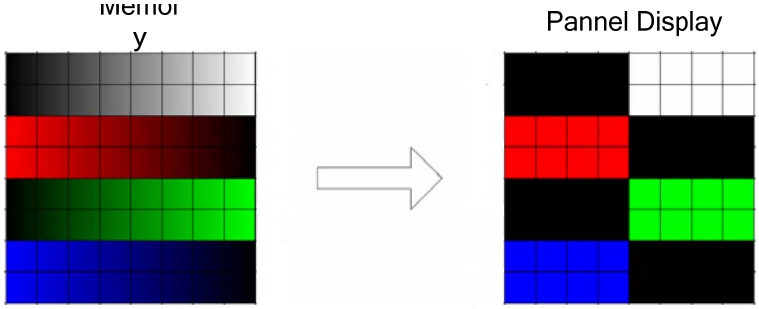
Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart



7.1.30 idle mode on and other mode off (39h)

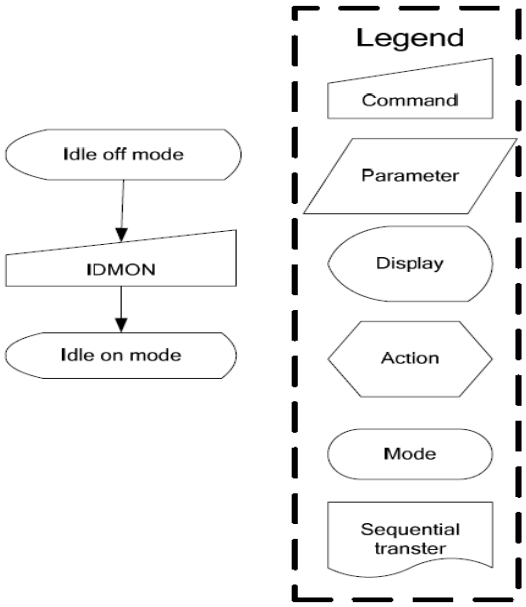
39h	idle mode on and other mode off									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
idle mode on and other mode off	W	0	0	1	1	1	0	0	1	(39h)
parameter	No Parameter									
Description	This command is used to enter into idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle on mode, 1. Color expression is reduced. The colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from idle mode on by idle mode off (38h) command.									
Restriction	This command has no effect when module is already in idle on mode.									
Register Availability										
Default										



Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart	

7.1.31 interface pixel format (3Ah)

3Ah	interface pixel format									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
interface pixel format	W	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	W	X	dpi[2:0]			X	dbi[2:0]			66h

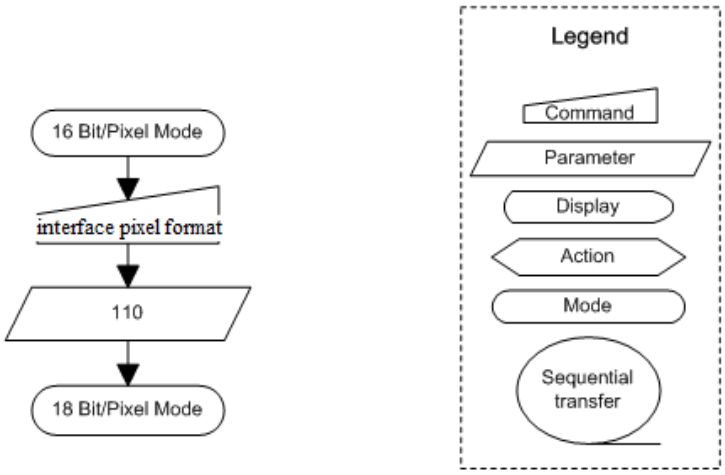
Description

dpi[2:0] is the pixel format select of RGB interface.

dbi[2:0] is the pixel format of system interface. If using RGB interface, serial interface must be selected.

dpi[2:0]			RGB interface format	dbi[2:0]			system interface format
0	0	0	reserved	0	0	0	reserved
0	0	1	reserved	0	0	1	reserved
0	1	0	reserved	0	1	0	reserved
0	1	1	reserved	0	1	1	reserved
1	0	0	reserved	1	0	0	reserved
1	0	1	16 bits/pixel	1	0	1	16 bits/pixel
1	1	0	18 bits/pixel	1	1	0	18 bits/pixel
1	1	1	reserved	1	1	1	reserved

“X” = Don’t care.

<table>
<tr><td>Restriction</td><td>There is no visible effect until the Frame Memory is written to.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>66h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>66h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>Example:
 
</td></tr>
</table>

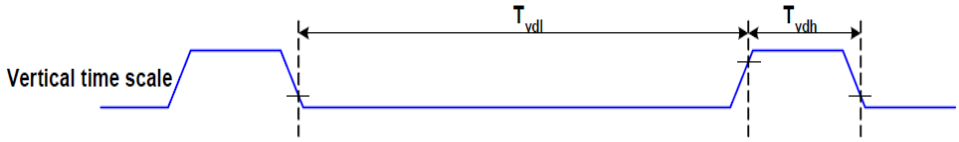
7.1.32 write memory continue (3Ch)

<table>
<tr><th>3Ch</th><th colspan="10">write memory continue</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>write memory continue</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(3Ch)</td></tr>
<tr><td>Description</td><td colspan="10">This command transfers image data from the host processor to the display module’s frame memory continuing from the pixel location following the previous write memory continue or memory write command.
If mv= ‘0’:
Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (caset_ec) value. The column register is then reset to caset_sc and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (paset_ep) value and the column register equals the caset_ec value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.
If mv= ‘1’:
Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (paset_ep) value. The page register is then reset to paset_sp and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (caset_ec) value and the page register equals the paset_ep value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.</td></tr>
<tr><td>Restriction</td><td colspan="10">A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

7.1.33 read memory continue (3Eh)

<table>
<tr><th>3Eh</th><th colspan="9">read memory continue</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read memory continue</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(3Eh)</td></tr>
<tr><td>Description</td><td colspan="10">This command transfers image data from the display module’s frame memory to the MPU. The image data continues from the pixel location following the previous read memory continue or memory read command.
If mv= ’0’:
Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (caset_ec) value. The column register is then reset to caset_sc and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (paset_ep) value and the column register equals the caset_ec value, or the MPU sends another command.
If mv= ‘1’:
Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (paset_ep) value. The page register is then reset to paset_sp and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (caset_ec) value and the page register equals the paset_ep value, or the MPU sends another command.</td></tr>
<tr><td>Restriction</td><td colspan="10">Regardless of the color mode set in interface pixel format, the pixel format returned by read memory continue is always 18-bit so there is no restriction on the length of data.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

7.1.34 set tear scanline (44h)

<table>
<tr><th>44h</th><th colspan="10">set tear scanline</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>set tear scanline</td><td>W</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(44h)</td></tr>
<tr><td>1st Parameter</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>sts[8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">sts[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on the display module’s tearing effect output signal on the TE signal line when the display module reaches line sts.
The TE signal is not affected by changing mv.
The tearing effect line on has one parameter that describes the tearing effect output line mode.
The tearing effect output line consist of V-blanking information only.
 

Note:
That set tear scanline with sts = ‘0’ is equivalent to tearing effect line on with tear_mode= ‘0’.
The tearing effect output line shall be low when the display module is in sleep mode.
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command takes affect on the frame following the current frame. Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.35 get tear scan line (45h)

<table>
<tr><th>45h</th><th colspan="10">get tear scan line</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>get tear scan line</td><td>R</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(45h)</td></tr>
<tr><td>1st Parameter</td><td>R</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">gts[9:8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>R</td><td colspan="8">gts[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">The display module returns the current scanline gts, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.When in sleep in mode, the value returned by get scanline is undefined.
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.36 read idd3 (D3h)

D3h	read idd3									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read idd3	R	1	1	0	1	0	0	1	1	(D3h)
1st parameter	R	id[23:16]								00h
2nd parameter	R	id[15:8]								31h
3rd parameter	R	id[7:0]								35h
Description	This read byte returns 24-bits display identification information. id[23:0]:LCD module/driver ID.									
Restriction										
Register Availability										
Default										
Flow Chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

7.1.37 read display id 1 (DAh)

DAh	read display id 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display id 1	R	1	1	0	1	1	0	1	0	(DAh)
1st parameter	R	id[23:16]								00h
Description	id[23:16]:LCD module/driver ID.									
Restriction	-									

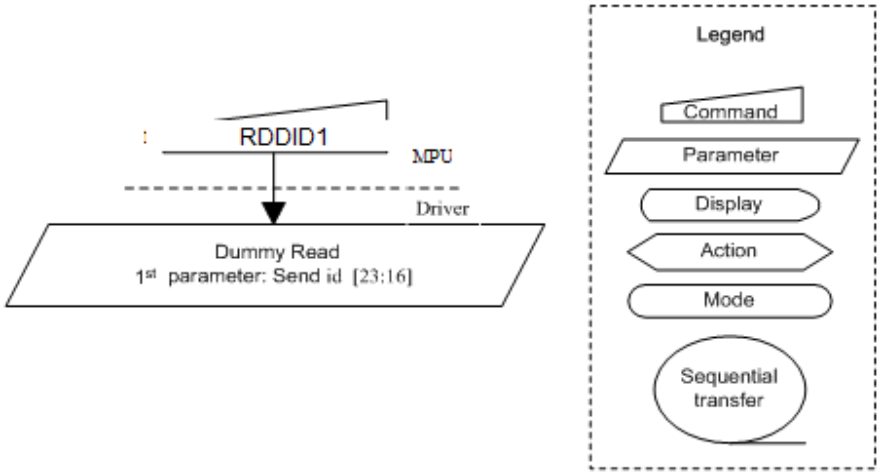
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

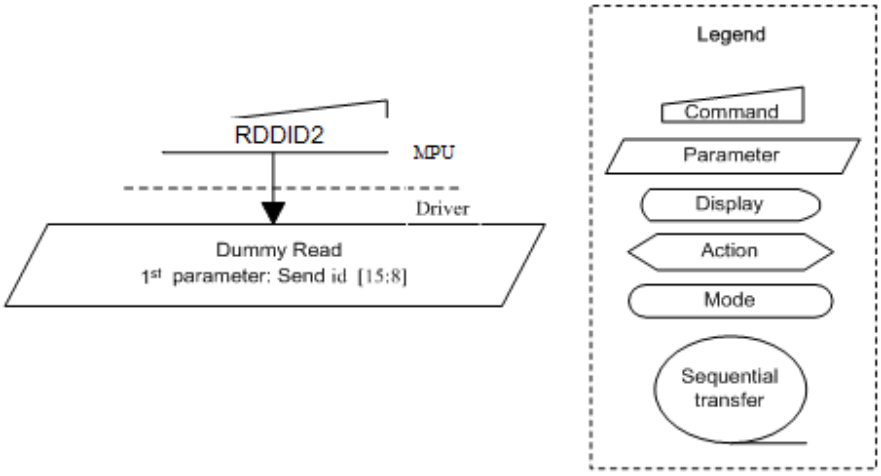
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

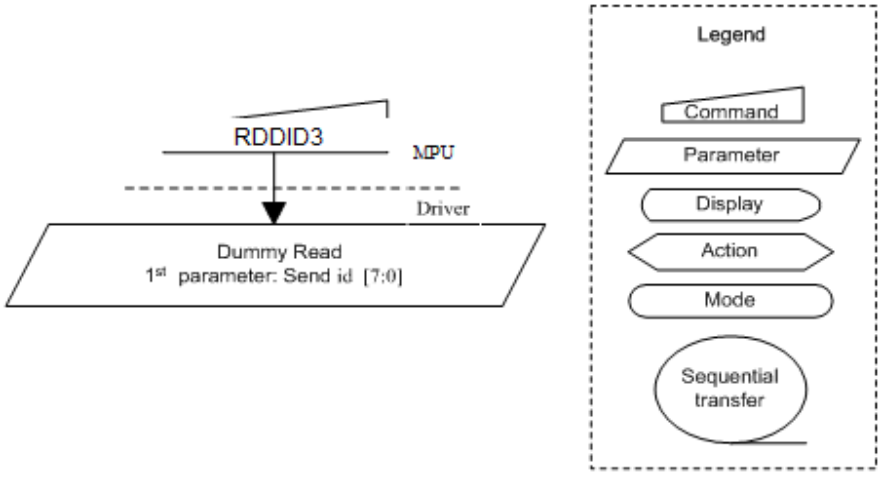
Flow Chart



7.1.38 read display id 2 (DBh)

<table>
<tr><td>DBh</td><td colspan="10">read display id 2</td></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display id 2</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>(DBh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id[15:8]</td><td>31h</td></tr>
<tr><td>Description</td><td colspan="10">id[15:8]:LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>31h</td></tr><tr><td>S/W Reset</td><td>31h</td></tr><tr><td>H/W Reset</td><td>31h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.39 read display id 3 (DCh)

<table>
<tr><td>DCh</td><td colspan="10">read display id 3</td></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display id 3</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(DCh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id[7:0]</td><td>35h</td></tr>
<tr><td>Description</td><td colspan="10">id[7:0]:LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>35h</td></tr><tr><td>S/W Reset</td><td>35h</td></tr><tr><td>H/W Reset</td><td>35h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.2 Private command

When enter read/write private register,need send 06h, 07h to FDh register;When exit read/write private register,need send fah, fbh to FDh register.

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
osc setting	RW	0	1	1	0	0	0	0	0	(60h)
	RW	X	X	X	osc_trim[4:0]					10h
	RW	div3_duty	X	X	X	1	0	0	0	08h
dvdd setting	RW	0	1	1	0	0	0	0	1	(61h)
	RW	X	X	X	X	X	X	dvdd_vs[1:0]		01h
vgl setting	RW	0	1	1	0	0	0	1	1	(63h)
	RW	1	0	vgl_set[2:0]			0	0	1	91h
	RW	X	X	X	X	0	0	1	0	02h
	RW	X	0	1	1	X	0	0	1	31h
	RW	X	X	X	X	0	0	0	0	00h
vgh setting	RW	0	1	1	0	0	1	0	0	(64h)
	RW	X	0	vgh_set[2:0]			0	0	1	29h
	RW	X	X	1	0	0	0	1	0	22h
	RW	X	0	1	0	X	1	0	0	24h
	RW	X	X	X	X	0	0	0	0	00h
mv setting (avcl, avdd)	RW	0	1	1	0	0	1	0	1	(65h)
	RW	1	avdd_btvs[1:0]		1	1	avcl_btvs[1:0]		1	B9h
	RW	1	1	X	X	0	0	1	X	C2h
	RW	X	0	0	1	X	0	1	1	13h
	RW	X	X	X	X	0	0	0	0	00h
vdds trim	RW	0	1	1	0	0	1	1	0	(66h)
	RW	X	X	X	X	X	vdds_res_trim[2:0]			04h
gamma ref 1	RW	0	1	1	0	1	0	0	0	(68h)
	RW	X	X	vmf[5:0]						00h
	RW	X	X	vcmp[5:0]						1Ch
	RW	X	vrh[6:0]							13h
	RW	X	vrh2[6:0]							13h
RGB interface control	RW	1	0	1	1	0	0	0	0	(B0h)
	RW	bypass_mode	rcm[1:0]		X	vspl	hspl	dpl	epl	40h

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
frame rate1 (normal)	RW	1	0	1	1	0	0	0	1	(B1h)
	RW	fr1_h[5:0]						fr1_div[1:0]		92h
	RW	X	X	X	fr1_v[4:0]					0Bh
frame rate2 (partial)	RW	1	0	1	1	0	0	1	0	(B2h)
	RW	fr2_h[5:0]						fr2_div[1:0]		92h
	RW	X	X	X	fr2_v[4:0]					0Bh
frame rate3 (8-color)	RW	1	0	1	1	0	0	1	1	(B3h)
	RW	fr3_h[5:0]						fr3_div[1:0]		92h
	RW	X	X	X	fr3_v[4:0]					0Bh
display pol control	RW	1	0	1	1	0	1	0	0	(B4h)
	RW	X	X	X	X	X	X	dinv[1:0]		01h
blanking porch	RW	1	0	1	1	0	1	0	1	(B5h)
	RW	X	vfp[6:0]							02h
	RW	X	vbp[6:0]							02h
	RW	X	hfp[6:0]							0Ah
	RW	X	hbp[6:0]							14h
display function	RW	1	0	1	1	0	1	1	0	(B6h)
	RW	isc[3:0]				X	X	ptg	pts	22h
	RW	rev	gs	ss	sm	X	X	X	normal_black	00h
	RW	X	X	nl[5:0]						27h
entry mode set	RW	1	0	1	1	0	1	1	1	(B7h)
	RW	X	X	X	X	X	gon	dte	X	06h
gamma positive 1	RW	1	1	1	0	0	0	0	0	(E0h)
	RW	X	X	X	pkp0[4:0]					0Bh
	RW	X	X	X	pkp1[4:0]					17h
	RW	X	X	X	pkp2[4:0]					06h
	RW	X	X	X	pkp3[4:0]					10h
	RW	X	X	X	pkp4[4:0]					05h
	RW	X	X	X	pkp5[4:0]					12h
	RW	X	X	X	pkp6[4:0]					0Ah
gamma positive 2	RW	1	1	1	0	0	0	0	1	(E1h)
	RW	X	prp0[6:0]							1Bh
	RW	X	prp1[6:0]							5Ah
gamma positive 3	RW	1	1	1	0	0	0	1	0	(E2h)
	RW	X	X	vrp0[5:0]						0Ah
	RW	X	X	vrp1[5:0]						2Eh
	RW	X	X	vrp2[5:0]						27h
	RW	X	X	vrp3[5:0]						19h
	RW	X	X	vrp4[5:0]						18h
	RW	X	X	vrp5[5:0]						2Bh

Instruction	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma negative 1	RW	1	1	1	0	0	0	1	1	(E3h)
	RW	X	X	X	pkn0[4:0]					0Ch
	RW	X	X	X	pkn1[4:0]					19h
	RW	X	X	X	pkn2[4:0]					0Fh
	RW	X	X	X	pkn3[4:0]					19h
	RW	X	X	X	pkn4[4:0]					08h
	RW	X	X	X	pkn5[4:0]					13h
	RW	X	X	X	pkn6[4:0]					13h
gamma negative 2	RW	1	1	1	0	0	1	0	0	(E4h)
	RW	X	prn0[6:0]							1Bh
	RW	X	prn1[6:0]							5Ah
gamma negative 3	RW	1	1	1	0	0	1	0	1	(E5h)
	RW	X	X	vrn0[5:0]						0Ah
	RW	X	X	vrn1[5:0]						22h
	RW	X	X	vrn2[5:0]						20h
	RW	X	X	vrn3[5:0]						13h
	RW	X	X	vrn4[5:0]						0Ch
	RW	X	X	vrn5[5:0]						2Bh
Frame rate 4	RW	1	1	1	1	0	0	0	0	(F0h)
	RW	src_v[3:0]				src_h[3:0]				48h
interface control	RW	1	1	1	1	0	1	1	0	(F6h)
	RW	my_eor	mx_eor	mv_eor	0	bgr_eor	0	0	We_mode	09h
	RW	X	X	epf[1:0]		X	X	mdt[1:0]		10h
	RW	spi_2wire_mode	X	endian	X	dm[1:0]		rm	rim	00h
private access	W	1	1	1	1	1	1	0	1	(FDh)
	W	private_access[15:8]								00h
	W	private_access[7:0]								00h

7.2.1 osc setting (60h)

<table>
<tr><th>60h</th><th colspan="10">osc setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>osc setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(60h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td colspan="5">osc_trim[4:0]</td><td>10h</td></tr>
<tr><td>2nd Parameter</td><td>RW</td><td>div3_duty</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td><td>0</td><td>08h</td></tr>
<tr><td>Description</td><td colspan="10">div3_duty: When div3_duty＝ ‘0’: OSC three points frequency clock duty cycle 67%. When div3_duty= ‘1’: OSC three points frequency clock duty cycle 33%.
osc_trim[4:0]:oscillator trimming.
<table>
<tr><th>Osc_trim[4:0]</th><th>Freq(MHz)</th><th>Osc_trim[4:0]</th><th>Freq(MHz)</th></tr>
<tr><td>00000</td><td>4.06</td><td>10000</td><td>15.07</td></tr>
<tr><td>00001</td><td>8.52</td><td>10001</td><td>15.52</td></tr>
<tr><td>00010</td><td>8.97</td><td>10010</td><td>15.89</td></tr>
<tr><td>00011</td><td>9.42</td><td>10011</td><td>16.26</td></tr>
<tr><td>00100</td><td>9.83</td><td>10100</td><td>16.79</td></tr>
<tr><td>00101</td><td>10.28</td><td>10101</td><td>17.08</td></tr>
<tr><td>00110</td><td>10.77</td><td>10110</td><td>17.49</td></tr>
<tr><td>00111</td><td>11.18</td><td>10111</td><td>17.98</td></tr>
<tr><td>01000</td><td>11.55</td><td>11000</td><td>18.27</td></tr>
<tr><td>01001</td><td>12.04</td><td>11001</td><td>18.64</td></tr>
<tr><td>01010</td><td>12.49</td><td>11010</td><td>19.13</td></tr>
<tr><td>01011</td><td>12.94</td><td>11011</td><td>19.50</td></tr>
<tr><td>01100</td><td>13.31</td><td>11100</td><td>19.87</td></tr>
<tr><td>01101</td><td>13.76</td><td>11101</td><td>20.28</td></tr>
<tr><td>01110</td><td>14.21</td><td>11110</td><td>20.68</td></tr>
<tr><td>01111</td><td>14.62</td><td>11111</td><td>21.09</td></tr>
</table></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>1008h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>1008h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.2 dvdd setting (61h)

<table>
<tr><th>61h</th><th colspan="10">dvdd setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>dvdd setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(61h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">dvdd_vs[1:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">dvdd_vs[1:0]:DVDD setting is as below:
<table><tr><th>dvdd_vs[1:0]</th><th>DVDD</th></tr><tr><td>00</td><td>1.65V</td></tr><tr><td>01</td><td>1.75V</td></tr><tr><td>10</td><td>1.83V</td></tr><tr><td>11</td><td>1.94V</td></tr></table></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>01h</td></tr><tr><td>S/W Reset</td><td>no change</td></tr><tr><td>H/W Reset</td><td>01h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.3 vgl setting(63h)

<table>
<tr><th>63h</th><th colspan="9">vgl setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vgl setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(63h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>1</td><td>0</td><td colspan="3">vgl_set[2:0]</td><td>0</td><td>0</td><td>1</td><td>91h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td><td>0</td><td>02h</td></tr>
<tr><td>3rdparameter</td><td>RW</td><td>X</td><td>0</td><td>1</td><td>1</td><td>X</td><td>0</td><td>0</td><td>1</td><td>31h</td></tr>
<tr><td>4thparameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">vgl_set[2:0]:VGL voltage Setting.
<table>
<tr><th>vgl_set[2:0]</th><th>VGL(V)</th></tr>
<tr><td>000</td><td>-10.875</td></tr>
<tr><td>001</td><td>-10.5</td></tr>
<tr><td>010</td><td>-10.125</td></tr>
<tr><td>011</td><td>-9.7</td></tr>
<tr><td>100</td><td>-10.85</td></tr>
<tr><td>101</td><td>-8.875</td></tr>
<tr><td>110</td><td>-8.5</td></tr>
<tr><td>111</td><td>-8.1</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.4 vgh setting (64h)

<table>
<tr><td>64h</td><td colspan="10">vgh setting</td></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vgh setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(64h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td>0</td><td colspan="3">vgh_set[2:0]</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>22h</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td>0</td><td>1</td><td>0</td><td>X</td><td>1</td><td>0</td><td>0</td><td>24h</td></tr>
<tr><td>4th parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">Vgh_set[2:0]: VGH voltage setting
<table>
<tr><th>vgh_set[2:0]</th><th>VGH(V)</th></tr>
<tr><td>000</td><td>13</td></tr>
<tr><td>001</td><td>13.3</td></tr>
<tr><td>010</td><td>13.6</td></tr>
<tr><td>011</td><td>13.9</td></tr>
<tr><td>100</td><td>14.5</td></tr>
<tr><td>101</td><td>14.9</td></tr>
<tr><td>110</td><td>15.25</td></tr>
<tr><td>111</td><td>15.68</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.5 mv setting (avcl, avdd) (65h)

<table>
<tr><th>65h</th><th colspan="10">mv setting (avcl, avdd)</th></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>mv setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(65h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>1</td><td colspan="2">avdd_btvs[1:0]</td><td>1</td><td>1</td><td colspan="2">avcl_btvs[1:0]</td><td>1</td><td>B9h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>1</td><td>1</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td><td>X</td><td>C2h</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td>0</td><td>0</td><td>1</td><td>X</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>4th parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">avdd_btvs[1:0]/ avcl_btvs[1:0]: AVDD/AVCL setting is as below.
<table>
<tr><th>avdd_ btvs[1:0]</th><th>AVDD</th><th>avdd_ btvs[1:0]</th><th>AVDD</th></tr>
<tr><td>00</td><td>6.20V</td><td>10</td><td>6.60V</td></tr>
<tr><td>01</td><td>6.40V</td><td>11</td><td>6.80V</td></tr>
</table>
<table>
<tr><th>avcl_ btvs[1:0]</th><th>AVCL</th><th>avcl_ btvs[1:0]</th><th>AVCL</th></tr>
<tr><td>00</td><td>-4.40V</td><td>10</td><td>-4.80V</td></tr>
<tr><td>01</td><td>-4.60V</td><td>11</td><td>-5.00V</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.6 vdds trim (66h)

<table>
<tr><th>66h</th><th colspan="10">vdds trim</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vdds trim</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(66h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">vdds_res_trim[2:0]</td><td>04h</td></tr>
<tr><td>Description</td><td colspan="10">vdds_res_trim[2:0]: VDDS setting is as below:
<table>
<tr><th>vdds_res_trim[2:0]</th><th>VDDS</th></tr>
<tr><td>000</td><td>1.77V</td></tr>
<tr><td>001</td><td>1.86V</td></tr>
<tr><td>010</td><td>1.95V</td></tr>
<tr><td>011</td><td>2.06V</td></tr>
<tr><td>100</td><td>2.17V</td></tr>
<tr><td>101</td><td>2.30V</td></tr>
<tr><td>110</td><td>2.45V</td></tr>
<tr><td>111</td><td>2.62V</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>04h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>04h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.7 gamma ref 1 (68h)

68h	gamma ref 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma ref 1	RW	0	1	1	0	1	0	0	0	(68h)
1st parameter	RW	X	X	vmf[5:0]						00h
2nd parameter	RW	X	X	vcmp[5:0]						1Ch
3rd parameter	RW	X	vrh[6:0]							13h
4th parameter	RW	X	vrh2[6:0]							13h

Description

vmf[5:0]: add an offset to vcmp(for optimum display quality).

vmf[5:0]	Offset	vmf[5:0]	Offset
011111b	31	111111b	-1
011110b	30	111110b	-2
:	:	:	:
000010b	2	100010b	-30
000001b	1	100001b	-31
000000b	0	100000b	-32

vcmp[5:0]:Set the relative of VCOM.

vcmp[5:0]	VCOM	vcmp[5:0]	VCOM	vcmp[5:0]	VCOM	vcmp[5:0]	VCOM
0	0.3	16	0.72	32	1.12	48	1.53
1	0.32	17	0.74	33	1.15	49	1.56
2	0.35	18	0.76	34	1.18	50	1.58
3	0.37	19	0.79	35	1.2	51	1.6
4	0.4	20	0.81	36	1.22	52	1.62
5	0.42	21	0.84	37	1.26	53	1.66
6	0.45	22	0.87	38	1.29	54	1.69
7	0.48	23	0.89	39	1.31	55	1.71
8	0.5	24	0.91	40	1.33	56	1.74
9	0.52	25	0.94	41	1.36	57	1.76
10	0.56	26	0.97	42	1.38	58	1.79
11	0.58	27	0.99	43	1.4	59	1.81
12	0.61	28	1.02	44	1.42	60	1.84
13	0.63	29	1.05	45	1.46	61	1.87
14	0.66	30	1.07	46	1.49	62	1.9
15	0.7	31	1.09	47	1.51	63	1.92

Note: VCOM = vcmp[5:0] + vmf[5:0] < 1.875.

vrh[6:0]: Set VAP voltage level.

vrh[6:0]	VAP (V)	vrh[6:0]	VAP (V)
00h	3.55+(vcom+vcom offset)	15h	4.6+(vcom+vcom offset)
01h	3.6+(vcom+vcom offset)	16h	4.65+(vcom+vcom offset)
02h	3.65+(vcom+vcom offset)	17h	4.7+(vcom+vcom offset)
03h	3.7+(vcom+vcom offset)	18h	4.75+(vcom+vcom offset)
04h	3.75+(vcom+vcom offset)	19h	4.8+(vcom+vcom offset)
05h	3.8+(vcom+vcom offset)	1Ah	4.85+(vcom+vcom offset)
06h	3.85+(vcom+vcom offset)	1Bh	4.9+(vcom+vcom offset)
07h	3.9+(vcom+vcom offset)	1Ch	4.95+(vcom+vcom offset)
08h	3.95+(vcom+vcom offset)	1Dh	5+(vcom+vcom offset)
09h	4+(vcom+vcom offset)	1Eh	5.05+(vcom+vcom offset)
0Ah	4.05+(vcom+vcom offset)	1Fh	5.1+(vcom+vcom offset)
0Bh	4.10 +(vcom+vcom offset)	20h	5.15+(vcom+vcom offset)
0Ch	4.15+(vcom+vcom offset)	21h	5.2+(vcom+vcom offset)
0Dh	4.2+(vcom+vcom offset)	22h	5.25+(vcom+vcom offset)
0Eh	4.25+(vcom+vcom offset)	23h	5.3+(vcom+vcom offset)
0Fh	4.3+(vcom+vcom offset)	24h	5.35+(vcom+vcom offset)
10h	4.35+(vcom+vcom offset)	25h	5.4+(vcom+vcom offset)
11h	4.4+(vcom+vcom offset)	26h	5.45+(vcom+vcom offset)
12h	4.45+(vcom+vcom offset)	27h	5.5+(vcom+vcom offset)
13h	4.5+(vcom+vcom offset)	28h～3Fh	Reserved
14h	4.55+(vcom+vcom offset)	--	--

Vrh2[6:0]: Set VAN voltage level.

vrh2[6:0]	**VAN (V)**	vrh2[6:0]	**VAN (V)**
00h	-3.55+(vcom+vcom offset)	15h	-4.6+(vcom+vcom offset)
01h	-3.6+(vcom+vcom offset)	16h	-4.65+(vcom+vcom offset)
02h	-3.65+(vcom+vcom offset)	17h	-4.7+(vcom+vcom offset)
03h	-3.7+(vcom+vcom offset)	18h	-4.75+(vcom+vcom offset)
04h	-3.75+(vcom+vcom offset)	19h	-4.8+(vcom+vcom offset)
05h	-3.8+(vcom+vcom offset)	1Ah	-4.85+(vcom+vcom offset)
06h	-3.85+(vcom+vcom offset)	1Bh	-4.9+(vcom+vcom offset)
07h	-3.9+(vcom+vcom offset)	1Ch	-4.95+(vcom+vcom offset)
08h	-3.95+(vcom+vcom offset)	1Dh	-5+(vcom+vcom offset)
09h	-4+(vcom+vcom offset)	1Eh	-5.05+(vcom+vcom offset)
0Ah	-4.05+(vcom+vcom offset)	1Fh	-5.1+(vcom+vcom offset)
0Bh	-4.10 +(vcom+vcom offset)	20h	-5.15+(vcom+vcom offset)
0Ch	-4.15+(vcom+vcom offset)	21h	-5.2+(vcom+vcom offset)
0Dh	-4.2+(vcom+vcom offset)	22h	-5.25+(vcom+vcom offset)
0Eh	-4.25+(vcom+vcom offset)	23h	-5.3+(vcom+vcom offset)
0Fh	-4.3+(vcom+vcom offset)	24h	-5.35+(vcom+vcom offset)
10h	-4.35+(vcom+vcom offset)	25h	-5.4+(vcom+vcom offset)
11h	-4.4+(vcom+vcom offset)	26h	-5.45+(vcom+vcom offset)
12h	-4.45+(vcom+vcom offset)	27h	-5.5+(vcom+vcom offset)
13h	-4.5+(vcom+vcom offset)	28h～3Fh	Reserved
14h	-4.55+(vcom+vcom offset)	--	--

Note:
Vcom default value is 1ch(Vcom = 1.0V)
Vcom offset value is 00h(Vcom offset = 0 step)
'X': Don't care.

Restriction	-

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.2.8 RGB interface control (B0h)

<table>
<tr><th>B0h</th><th colspan="10">RGB interface control</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>RGB interface control</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(B0h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>bypass_mode</td><td colspan="2">rcm[1:0]</td><td>X</td><td>vspl</td><td>hspl</td><td>dpl</td><td>epl</td><td>40h</td></tr>
<tr><td>Description</td><td colspan="10">Set the operation status of display interface. The setting becomes effective as soon as the command is seted.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">bypass_mode</td><td rowspan="2">Select the display data bypass</td><td>0</td><td>direct to shift register</td></tr>
<tr><td>1</td><td>through memory</td></tr>
<tr><td rowspan="2">vspl</td><td rowspan="2">VSYNC polarity</td><td>0</td><td>Low level sync clock</td></tr>
<tr><td>1</td><td>High level sync clock</td></tr>
<tr><td rowspan="2">hspl</td><td rowspan="2">HSYNC polarity</td><td>0</td><td>Low level sync clock</td></tr>
<tr><td>1</td><td>High level sync clock</td></tr>
<tr><td rowspan="2">dpl</td><td rowspan="2">Dot clock polarity</td><td>0</td><td>data fetched at the rising time</td></tr>
<tr><td>1</td><td>data fetched at the falling time</td></tr>
<tr><td rowspan="2">epl</td><td rowspan="2">DE polarity</td><td>0</td><td>High enable for RGB interface</td></tr>
<tr><td>1</td><td>Low enable for RGB interface</td></tr>
</table>
rcm[1:0]:RGB interface enable mode selection.
<table>
<tr><th>rcm[1:0]</th><th>Mode</th></tr>
<tr><td>00</td><td rowspan="2">system interface</td></tr>
<tr><td>01</td></tr>
<tr><td>10</td><td>RGB DE mode</td></tr>
<tr><td>11</td><td>RGB SYNC mode</td></tr>
</table>
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>40h</td></tr>
<tr><td>S/W Reset</td><td>40h</td></tr>
<tr><td>H/W Reset</td><td>40h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.9 frame rate1 (normal) (B1h)

<table>
<tr><th>B1h</th><th colspan="9">frame rate1 (normal)</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>frame rate1</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(B1h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td colspan="6">fr1_h[5:0]</td><td colspan="2">fr1_div[1:0]</td><td>92h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td colspan="5">fr1_v[4:0]</td><td>0bh</td></tr>
<tr><td>Description</td><td colspan="10">It is adjustable frame rate in normal mode.
fr1_h[5:0]: Adjustable the number of clocks.
fr1_v[4:0]: Adjustable the number of lines.
fr1_div[1:0]:set the division ratio of the internal oscillation clock, when NV3029S's display operation is synchronized with internal oscillation clock. NV3029S's internal operation is synchronized with the frequency divided internal oscillation clock. When changing the fr1_div[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed.
<table><tr><th>fr1_div[1:0]</th><th>Division Ratio</th><th>Internal Operation Clock Unit</th></tr><tr><td>2'h0</td><td>1/1 fosc</td><td>One OSC clock</td></tr><tr><td>2'h1</td><td>1/2 fosc</td><td>2 OSC clock</td></tr><tr><td>2'h2</td><td>1/3 fosc</td><td>3 OSC clock</td></tr><tr><td>2'h3</td><td>1/4 fosc</td><td>4 OSC clock</td></tr></table>Frame Frequency Calculation
$\text{Frame Frequency} = \frac{\text{Fosc}}{\text{fr1\_div[1:0]} \times (240 + \text{src\_h} + \text{fr1\_h[5:0]}) \times (320 + \text{src\_v} + \text{fr1\_v[4:0]})}$
1.Fosc:RC oscillation frequency,adjustment by osc_trim and osc_fresh.
2.src_h:row pitch during source normal work.Source current row pitch is clock number.Insure source finished transfer and latched data when adjust the frame frequency.
3.src_v: interval frame during normal work.
4. fr1_h[5:0]: Adjustable the number of clocks. fr1_v[4:0]:Adjustable the number of lines.
5. fr1_div[1:0]: Division Ratio of clocks.
"X" = Don't care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>920Bh</td></tr><tr><td>S/W Reset</td><td>920Bh</td></tr><tr><td>H/W Reset</td><td>920Bh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.10 frame rate2 (partial) (B2h)

<table>
<tr><th>B2h</th><th colspan="10">frame rate2 (partial)</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>frame rate2</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(B2h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td colspan="6">fr2_h[5:0]</td><td colspan="2">fr2_div[1:0]</td><td>92h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td colspan="5">fr2_v[4:0]</td><td>0Bh</td></tr>
<tr><td>Description</td><td colspan="10">It is adjustable frame rate in partial mode.
See frame rate1(B1h) for detail description.
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>920Bh</td></tr><tr><td>S/W Reset</td><td>920Bh</td></tr><tr><td>H/W Reset</td><td>920Bh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.11 frame rate3 (8-color) (B3h)

B3h	frame rate3 (8-color)									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
frame rate3	RW	1	0	1	1	0	0	1	1	(B3h)
1st parameter	RW	fr3_h[5:0]						fr3_div[1:0]		92h
2nd parameter	RW	X	X	X	fr3_v[4:0]					0Bh
Description	It is adjustable frame rate in idle mode. See frame rate1(B1h) for detail description. "X" = Don't care.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	920Bh
S/W Reset	920Bh
H/W Reset	920Bh

Flow Chart

7.2.12 display pol control (B4h)

<table>
<tr><th>B4h</th><th colspan="10">display pol control</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display pol control</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(B4h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">dinv[1:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">dinv[1:0]:Set the inversion mode.
<table><tr><th>dinv [1:0]</th><th>Inversion mode</th></tr><tr><td>00</td><td>Column inversion</td></tr><tr><td>01</td><td>1-dot inversion</td></tr><tr><td>10</td><td>2-dot inversion</td></tr><tr><td>11</td><td>Reserved</td></tr></table>“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>01h</td></tr><tr><td>S/W Reset</td><td>01h</td></tr><tr><td>H/W Reset</td><td>01h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.13 blanking porch (B5h)

<table>
<tr><th>B5h</th><th colspan="10">blanking porch</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>blanking porch</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(B5h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td colspan="7">vfp[6:0]</td><td>02h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td colspan="7">vbp[6:0]</td><td>02h</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td colspan="7">hfp[6:0]</td><td>0Ah</td></tr>
<tr><td>4th parameter</td><td>RW</td><td>X</td><td colspan="7">hbp[6:0]</td><td>14h</td></tr>
<tr><td>Description</td><td colspan="10">vfp[6:0]/vbp[6:0]:The vfp[6:0] and vbp[6:0] bits specify the line number of vertical front and back porch period respectively.
hfp[6:0]/ hbp[6:0]:The hfp[6:0] and hbp [6:0] bits specify the dotclk number of horizontal front and back porch period respectively.
Note:when rim == 1， porch size is according to clock counter，isn’t according to pixel counter.
“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.14 display function (B6h)

<table>
<tr><th>B6h</th><th colspan="10">display function</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display function</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(B6h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td colspan="4">isc[3:0]</td><td>X</td><td>X</td><td>ptg</td><td>pts</td><td>22h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>rev</td><td>gs</td><td>ss</td><td>sm</td><td>X</td><td>X</td><td>X</td><td>normal_black</td><td>00h</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">nl[5:0]</td><td>27h</td></tr>
<tr><td>Description</td><td colspan="10">
normal_black: Panel selection. normal_black=’0’,normal white; normal_black=’1’,normal black.
pts: Determine source output in a non-display area in the partial display mode.
<table>
<tr><th>pts</th><th>Source output on non-display area</th></tr>
<tr><td>0</td><td>V63</td></tr>
<tr><td>1</td><td>V0</td></tr>
</table>
ptg:Set the scan mode in non-display area.
<table>
<tr><th>ptg</th><th>Gate outputs in non-display area</th></tr>
<tr><td>0</td><td>normal scan</td></tr>
<tr><td>1</td><td>Interval scan</td></tr>
</table>
rev: xor display inversion setting.
nl[5:0]: Set the number of gate line.
<table>
<tr><th>nl[5:0]</th><th>The number of gate line</th></tr>
<tr><td>0x00</td><td>8 gate line</td></tr>
<tr><td>0x01</td><td>16 gate line</td></tr>
<tr><td>0x02</td><td>24 gate line</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>0x27</td><td>320 gate line</td></tr>
</table>
gs: Gate scan direction.gs=”0”: Gate scan direction is 0→319;gs=”1”: Gate scan direction is 319→0.
ss: selects the shift direction of outputs of the source driver. 0: Source output S1→S720; 1: Source output S720→S1.
sm: Gate interlace mode selection.sm=”0”: Gate scan using interlace mode. sm=”1”: Gate scan using non-interlace mode.
isc[3:0]: Specify the scan cycle of the gate driver when the ptg is seted to “1” in non-display area. The scan cycle can be set in odd number of frames from 0 to 31. In this case, polarity is inverted every scan cycle.
<table>
<tr><th>Isc[3:0]</th><th>Scan cycle</th><th>(Ffrm)=60HZ</th></tr>
<tr><td>0000</td><td>0 frame</td><td>-</td></tr>
<tr><td>0001</td><td>3 frame</td><td>50ms</td></tr>
<tr><td>0010</td><td>5 frame</td><td>84ms</td></tr>
<tr><td>0011</td><td>7 frame</td><td>117ms</td></tr>
<tr><td>0100</td><td>9 frame</td><td>150ms</td></tr>
<tr><td>0101</td><td>11 frame</td><td>184ms</td></tr>
<tr><td>0110</td><td>13frame</td><td>217ms</td></tr>
<tr><td>0111</td><td>15frame</td><td>251ms</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>1000</td><td>17frame</td><td>284ms</td></tr>
<tr><td>1001</td><td>19frame</td><td>317ms</td></tr>
<tr><td>1010</td><td>21frame</td><td>351ms</td></tr>
<tr><td>1011</td><td>23 frame</td><td>384ms</td></tr>
<tr><td>1100</td><td>25frame</td><td>418ms</td></tr>
<tr><td>1101</td><td>27frame</td><td>451ms</td></tr>
<tr><td>1110</td><td>29 frame</td><td>484ms</td></tr>
<tr><td>1111</td><td>31frame</td><td>518ms</td></tr>
</table>
“X” = Don’t care.
</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.2.15 entry mode set (B7h)

<table>
<tr><th>B7h</th><th colspan="9">entry mode set</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>entry mode set</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>(B7h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>gon</td><td>dte</td><td>X</td><td>06h</td></tr>
<tr><td>Description</td><td colspan="10">gon/dte: Set the output level of gate driver:
<table><tr><th>gon</th><th>dte</th><th>G1~G320 Gate Output</th></tr><tr><td>0</td><td>0</td><td>VGH</td></tr><tr><td>0</td><td>1</td><td>VGH</td></tr><tr><td>1</td><td>0</td><td>VGL</td></tr><tr><td>1</td><td>1</td><td>Normal display</td></tr></table>“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06h</td></tr><tr><td>S/W Reset</td><td>06h</td></tr><tr><td>H/W Reset</td><td>06h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.16 gamma positive 1 (E0h)

E0h	gamma positive 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma positive 1	RW	1	1	1	0	0	0	0	0	(E0h)
1st parameter	RW	X	X	X	pkp0[4:0]					0Bh
2nd parameter	RW	X	X	X	pkp1[4:0]					17h
3rd parameter	RW	X	X	X	pkp2[4:0]					06h
4th parameter	RW	X	X	X	pkp3[4:0]					10h
5th parameter	RW	X	X	X	pkp4[4:0]					05h
6th parameter	RW	X	X	X	pkp5[4:0]					12h
7th parameter	RW	X	X	X	pkp6[4:0]					0Ah
Description	E0h is gamma adjust registers.See gamma correction section for reference. “X”: Don’t care.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.17 gamma positive 2 (E1h)

<table>
<tr><th>E1h</th><th colspan="10">gamma positive 2</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>gamma positive 2</td><td>RW</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(E1h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td colspan="7">prp0[6:0]</td><td>1Bh</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td colspan="7">prp1[6:0]</td><td>5Ah</td></tr>
<tr><td>Description</td><td colspan="10">E1h is gamma adjust registers.See gamma correction section for reference.
“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>1B5Ah</td></tr><tr><td>S/W Reset</td><td>no change</td></tr><tr><td>H/W Reset</td><td>1B5Ah</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.18 gamma positive 3 (E2h)

<table>
<tr><th>E2h</th><th colspan="10">gamma positive 3</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>gamma positive 3</td><td>RW</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(E2h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrp0[5:0]</td><td>0Ah</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrp1[5:0]</td><td>2Eh</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrp2[5:0]</td><td>27h</td></tr>
<tr><td>4th parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrp3[5:0]</td><td>19h</td></tr>
<tr><td>5th parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrp4[5:0]</td><td>18h</td></tr>
<tr><td>6th parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrp5[5:0]</td><td>2Bh</td></tr>
<tr><td>Description</td><td colspan="11">E2h is gamma adjust registers.See gamma correction section for reference.
“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="11">-</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11"></td></tr>
</table>

7.2.19 gamma negative 1 (E3h)

E3h	gamma negative 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma negative 1	RW	1	1	1	0	0	0	1	1	(E3h)
1st parameter	RW	X	X	X	pkn0[4:0]					0Ch
2nd parameter	RW	X	X	X	pkn1[4:0]					19h
3rd Parameter	RW	X	X	X	pkn2[4:0]					0Fh
4th Parameter	RW	X	X	X	pkn3[4:0]					19h
5th parameter	RW	X	X	X	pkn4[4:0]					08h
6th Parameter	RW	X	X	X	pkn5[4:0]					13h
7th Parameter	RW	X	X	X	pkn6[4:0]					13h
Description	E3h is gamma adjust registers.See gamma correction section for reference. “X” : Don’t care.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.20 gamma negative 2 (E4h)

E4h	gamma negative 2									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma negative 2	RW	1	1	1	0	0	1	0	0	(E4h)
1st parameter	RW	X	prn0[6:0]							1Bh
2nd parameter	RW	X	prn1[6:0]							5Ah
Description	E4h is gamma adjust registers.See gamma correction section for reference. “X”: Don’t care.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	1B5Ah
S/W Reset	no change
H/W Reset	1B5Ah

Flow Chart

7.2.21 gamma negative 3 (E5h)

<table>
<tr><th>E5h</th><th colspan="10">gamma negative 3</th></tr>
<tr><td>Inst / Para</td><td>W//R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>gamma negative 3</td><td>RW</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(E5h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrn0[5:0]</td><td>0Ah</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrn1[5:0]</td><td>22h</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrn2[5:0]</td><td>20h</td></tr>
<tr><td>4th parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrn3[5:0]</td><td>13h</td></tr>
<tr><td>5th parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrn4[5:0]</td><td>0Ch</td></tr>
<tr><td>6th parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">vrn5[5:0]</td><td>2Bh</td></tr>
<tr><td>Description</td><td colspan="11">E5h is gamma adjust registers.See gamma correction section for reference.
“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="11">-</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11"></td></tr>
</table>

7.2.22 Frame Rate 4 (F0h)

F0h	Frame Rate 4									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Frame Rate4	RW	1	1	1	1	0	0	0	0	(F0h)
1st Parameter	RW	src_v[3:0]				src_h[3:0]				48h
Description	src_h[3:0]:row pitch during source normal work.Source current row pitch is clock number.Insure source finished transfer and latched data when adjust frame rate. src_v[3:0]: interval frame during normal work.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	48h
S/W Reset	48h
H/W Reset	48h

7.2.23 Interface control (F6h)

F6h	Interface control									
Inst / Para	W/ R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Interface control	RW	1	1	1	1	0	1	1	0	(F6h)
1st Parameter	RW	my_eor	mx_eor	mv_eor	0	bgr_eor	0	0	we_mode	09h
2nd Parameter	RW	X	X	epf[1:0]		X	X	mdt[1:0]		10h
3rd Parameter	RW	spi_2wire_mode	X	endian	X	dm[1:0]		rm	rim	00h

Description

my_eor/mx_eor/mv_eor/bgr_eor:the set of value MADCTL is used in the IC is derived as exclusive OR between first parameter of interface control and MADCTL parameter.

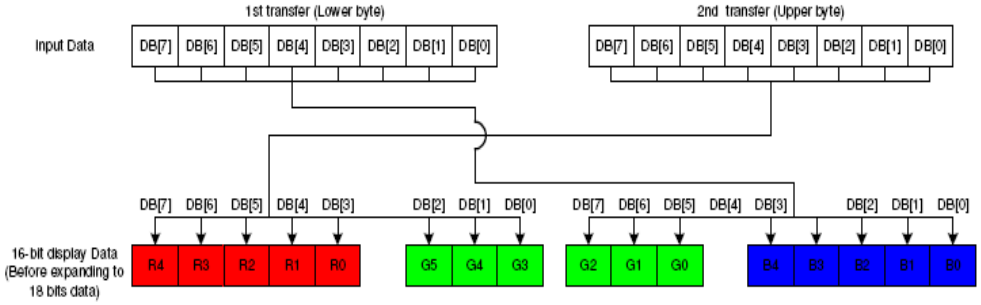
mdt[1:0]:select the method of display data transferring.
we_mode:memory write control.
we_mode=0:when the transfer number of data exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1), the exceeding data will be ignored.
we_mode=1:when the transfer number of data exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

spi_2wire_mode:enable 2 data lane serial interface mode.

endian: select the little endian interface bit. At little endian mode, the MPU sends LSB data first.

endian	Data transfer mode
0	Normal (MSB first)
1	Little endian (LSB first)

Note: the little endian is valid on only 65k 8bit and 9bit parallel interface mode.



dm[1:0]: select the display operation mode.

dm[1]	dm[0]	Display operation mode
0	0	Internal clock operation
0	1	RGB interface mode
1	0	reserved
1	1	reserved

The dm[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.
rm:select the interface to access the GRAM.

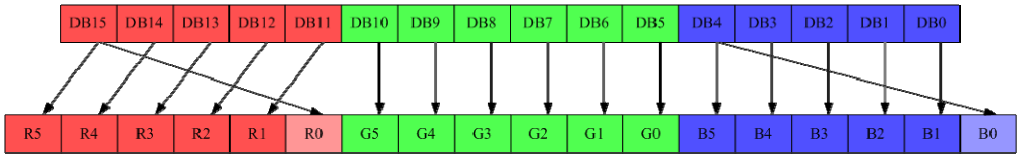
rm	Interface for RAM access
0	system interface
1	RGB interface

rim: specify the RGB interface mode when RGB interface is used. These bits should be set before display operation through RGB interface and should not be set during operation.

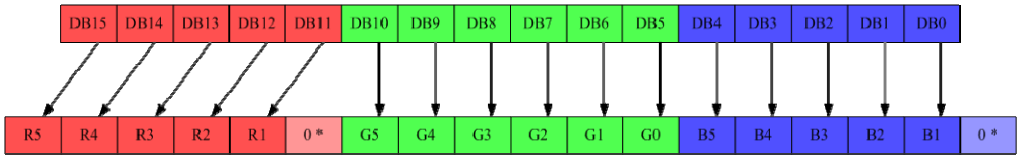
rim	dpi[1:0]	Display operation mode
0	110(262k color)	18 bit RGB interface (1 transfer/pixel)
	101(65k color)	16 bit RGB interface (1 transfer/pixel)
1	110(262k color)	6 bit RGB interface (3 transfer/pixel)
	101(65k color)	6 bit RGB interface (3 transfer/pixel)

epf[1:0]:

epf = 00

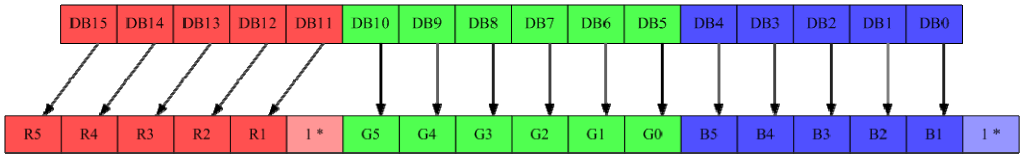


epf = 01



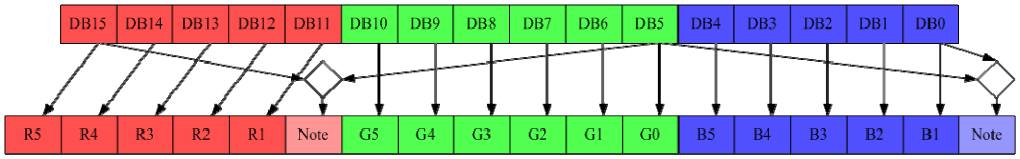
Note: Exception
1. R0 = 1 when R5~R1 = 1111
2. B0 = 1 when B4~B1 = 1111

epf = 10



Note: Exception
1. R0 = 0 when R5~R1 = 0000
2. B0 = 0 when B4~B1 = 0000

epf = 11



Note:
1. If DB15~DB11 = DB10~DB6, R0 = DB5, else R0 = DB15
2. If DB4~DB0 = DB10~DB16, B0 = DB5, else B0 = DB0

"X" = Don't care.

Restriction	

Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes; Normal Mode On, Idle Mode On, Sleep Out — Yes; Partial Mode On, Idle Mode Off, Sleep Out — Yes; Partial Mode On, Idle Mode On, Sleep Out — Yes; Sleep In — Yes
Default	Status / Default Value: Power On Sequence; S/W Reset; H/W Reset

7.2.24 Private access (FDh)

FDh	Private access								
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Private access	RW	1	1	1	1	1	1	0	1	(FDh)
1st Parameter	RW	private_access[15:8]								00h
2nd Parameter	RW	private_access[7:0]								00h
Description	private_access[15:0] : private registers access control.									

private access	private_access[15:8]	private_access[7:0]
enter private registers mode	06h	07h
exit private registers mode	FAh	FBh

Restriction	
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes; Normal Mode On, Idle Mode On, Sleep Out — Yes; Partial Mode On, Idle Mode Off, Sleep Out — Yes; Partial Mode On, Idle Mode On, Sleep Out — Yes; Sleep In — Yes
Default	Status / Default Value: Power On Sequence — 0000h; S/W Reset — 0000h; H/W Reset — 0000h

8. Functional description

8.1 Interface

8.1.1 Serial Interface

PAD Name	Serial Interface Pin Name	Description
CSX	CSX	A chip select signal.Signal is active low.
DCX	SCL	This pin is used serial interface clock.
WRX	DCX/SDI2	SPI 4-wire system: Serves as command or parameter select. 2 data lane serial interface: the second data lane.
SDA	SDA/SDI	SDA(When serial I/F Ⅰ): it is SPI interface input/output pin. SDI(When serial I/F Ⅱ): it is SPI interface input pin.
SDO	SDO	SPI interface output pin.

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

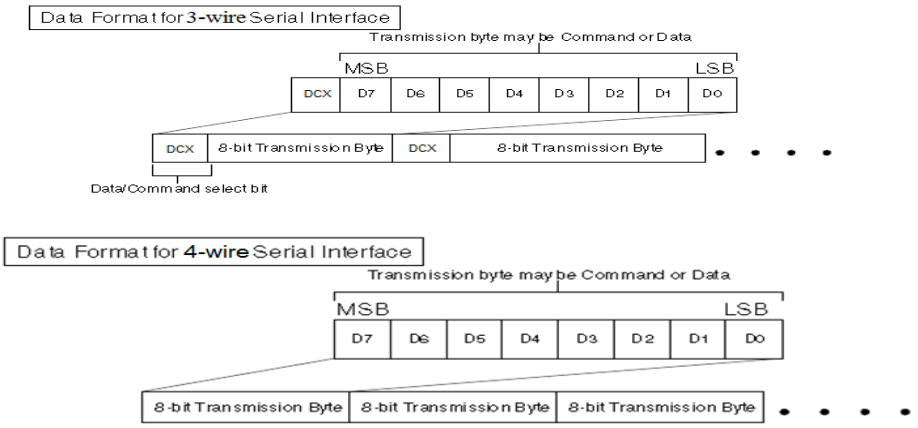
IM3	IM2	IM1	IM0	System Interface Mode	CSX	DCX	SCL	Function
0	1	0	1	3-wire serial interface 2 data lane serial interface	"L"	-		Read/Write command, parameter or display data.
0	1	1	0	4-wire serial interface	"L"	"H/L"		Read/Write command, parameter or display data.
1	1	0	1	3-wire serial interface	"L"	-		Read/Write command, parameter or display data.
1	1	1	0	4-wire serial interface	"L"	"H/L"		Read/Write command, parameter or display data.

NV3029S supplies 3-wire/ 9-bit and 4-wire/8-bit bi-directional serial interfaces for communication between MPU and NV3029S. The 3-wire serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDA/SDO). The 4-wire serial mode consists of the Data/Command selection input (DCX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDA/SDO) for data transmission. The data bus (D[17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

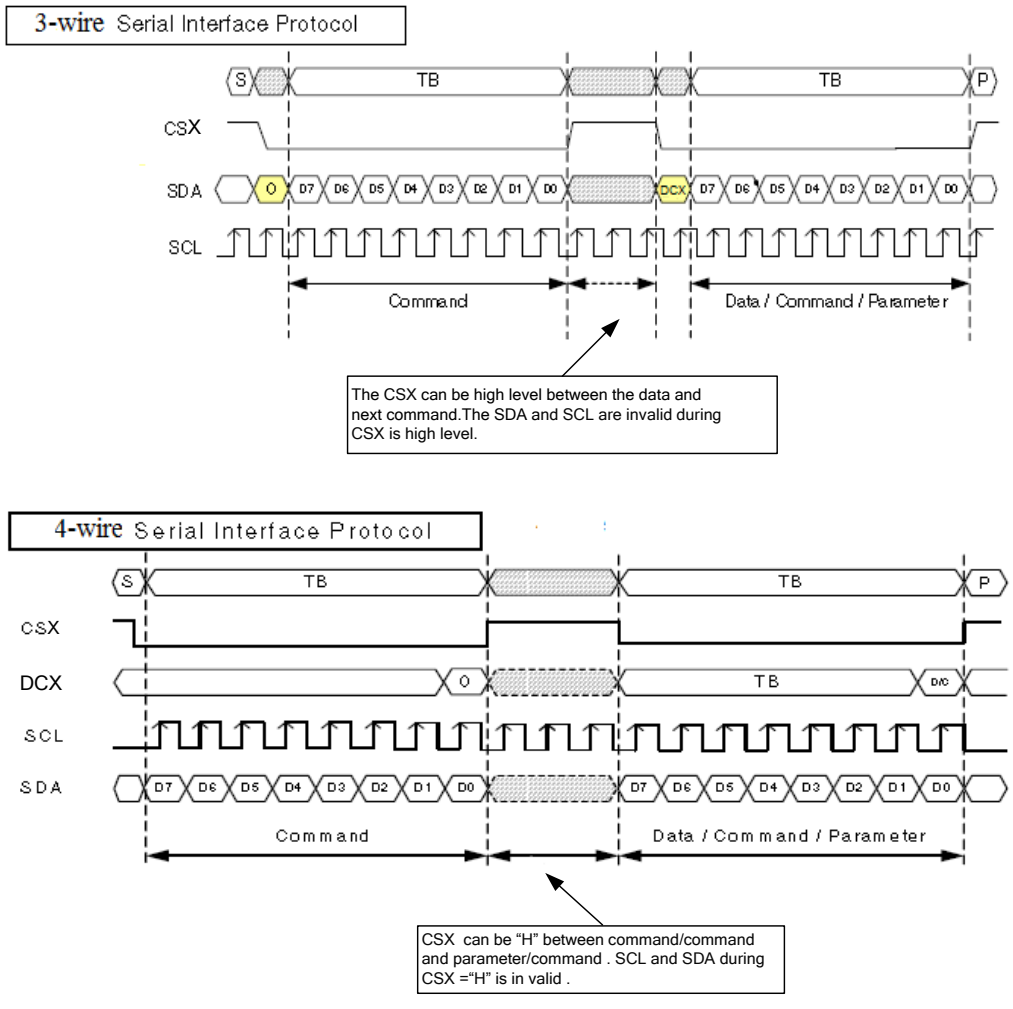
8.1.1.1 Write Cycle Sequence

The write mode of the interface means that MPU writes commands or data to NV3029S. The 3-wire serial data packet contains a data/command select bit (DCX) and a transmission byte. If the DCX bit is "low", the transmission byte is interpreted as a command byte. If the DCX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to NV3029S and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-wire serial interface.

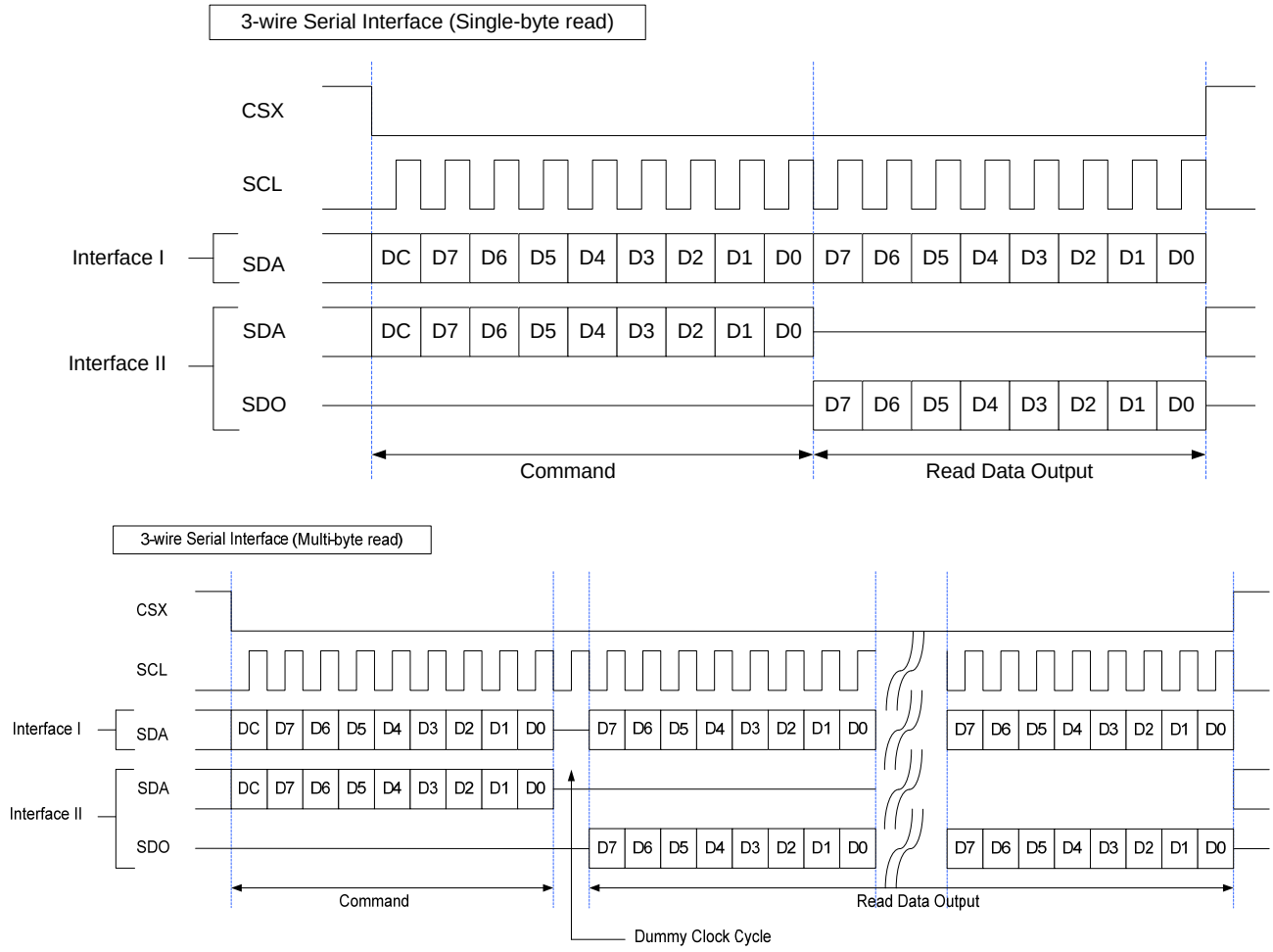


MPU drives the CSX pin to low and starts by setting the DCX bit on SDA. The bit is read by NV3029S on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the MPU. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional DCX signal is used, a byte is eight read cycle width. The 3/4-wire serial interface writes sequence described in the figure as below.

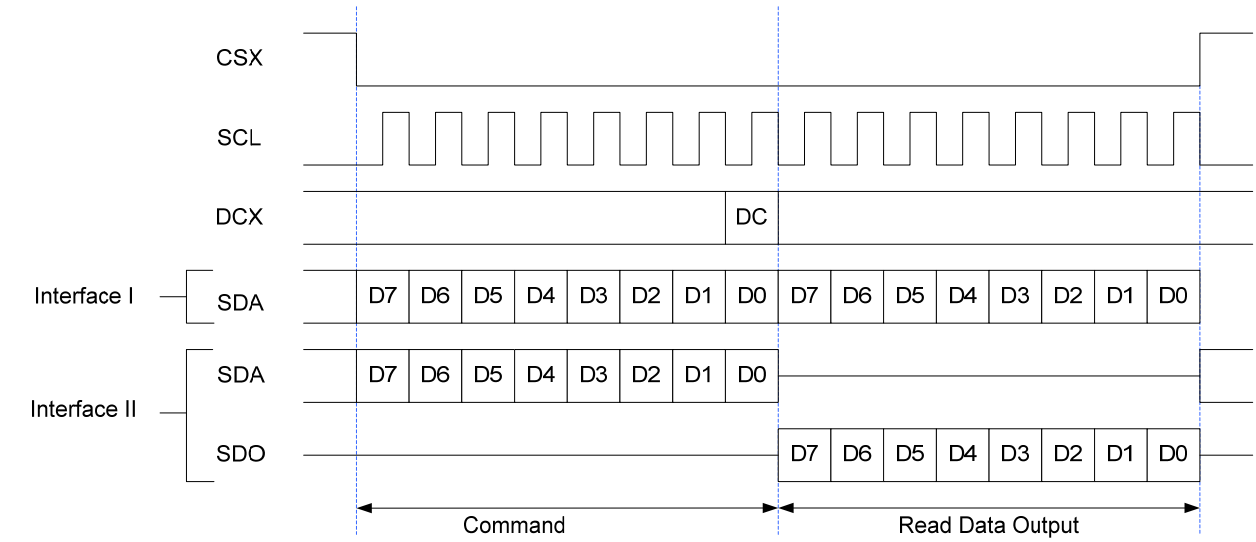


8.1.1.2 Read Cycle Sequence

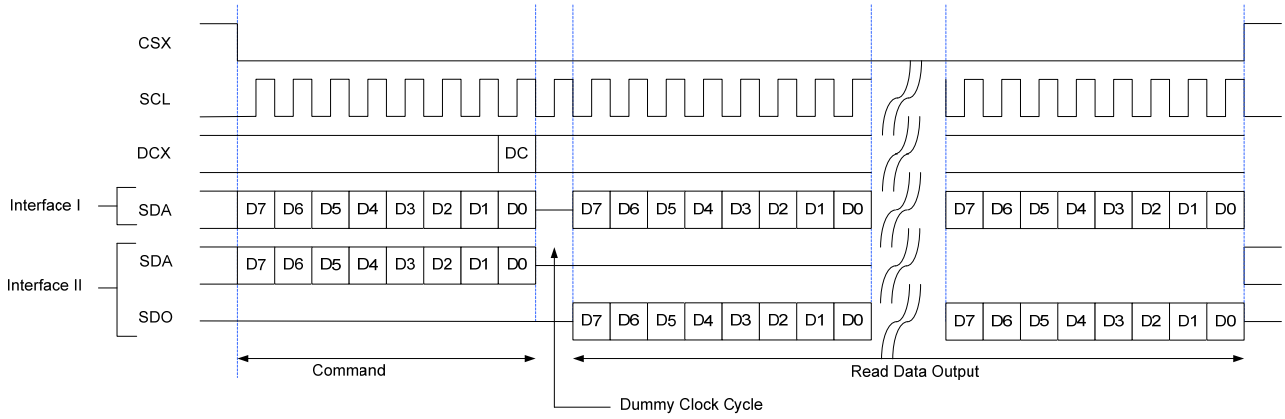
The read mode of interface means that the MPU reads register's parameter from NV3029S. The MPU has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. NV3029S latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has two types of transmitted command data (single/multi-byte) according to command code.



4-wire Serial Interface (Single-byte read)

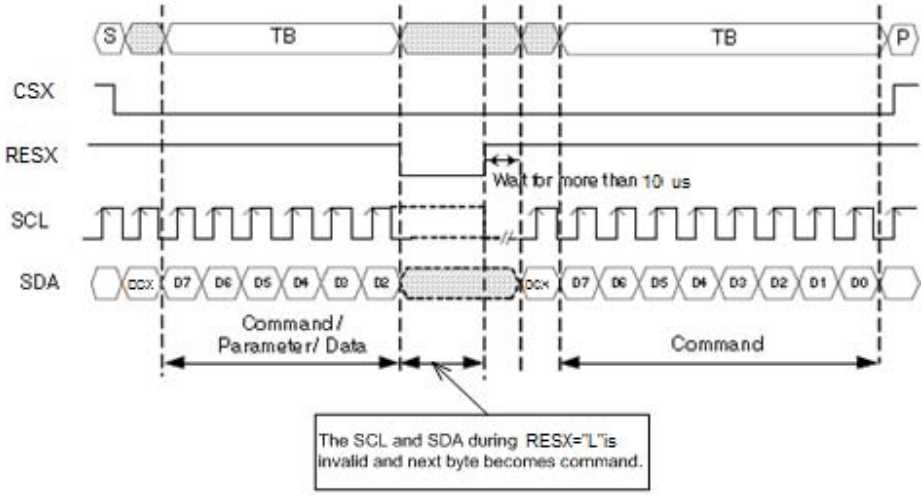


4-wire Serial Interface (Multi-byte read)

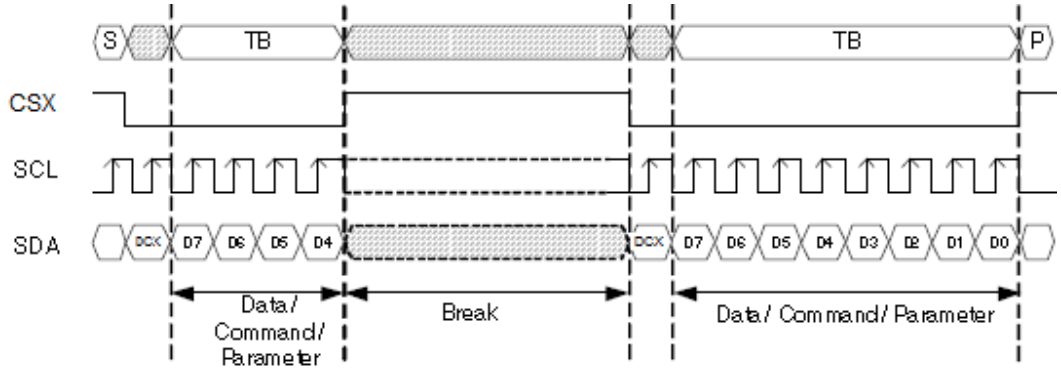


8.1.1.3 Data Transfer Break and Recovery

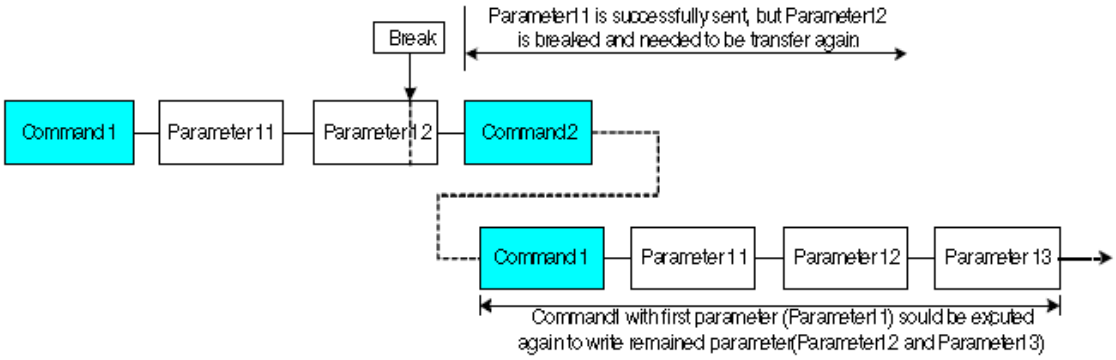
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



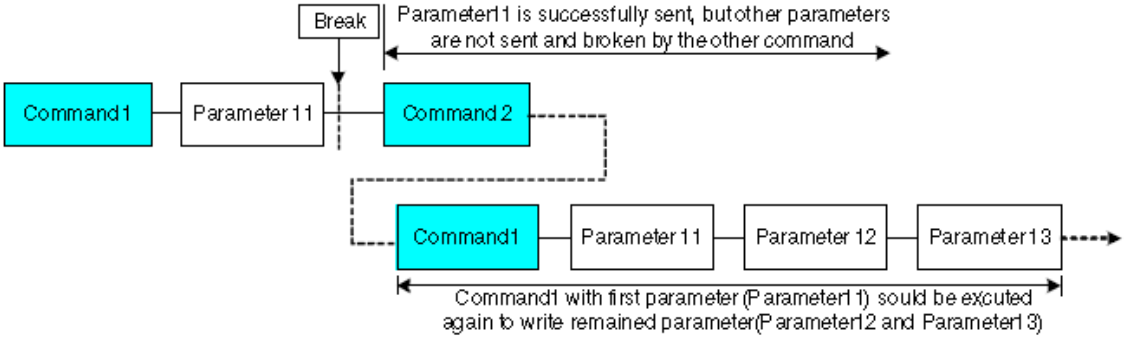
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the MPU then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

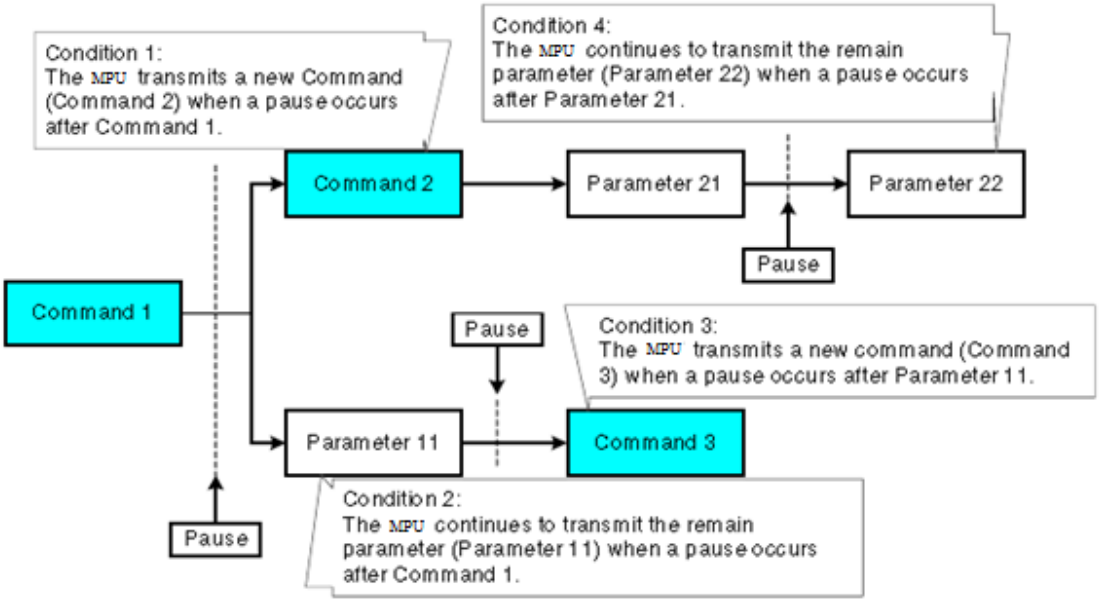
8.1.1.4 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then NV3029S will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.



This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter



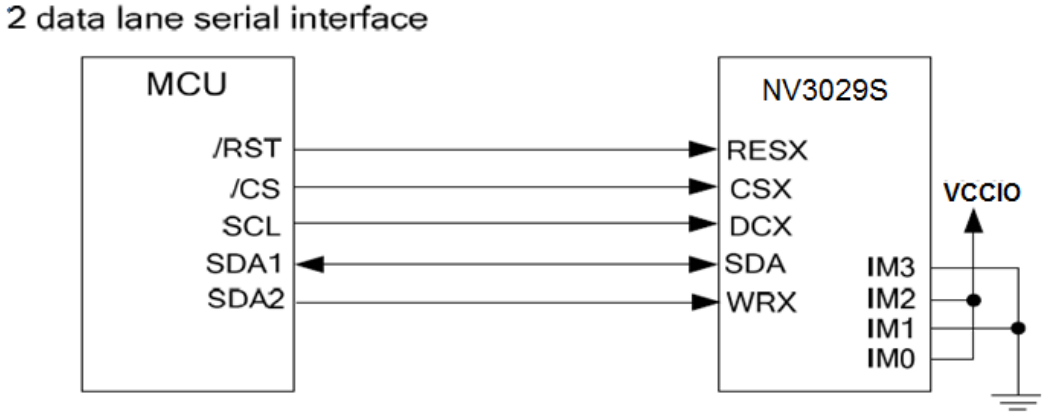
8.1.1.5 2 data lane serial interface

Interface selection:

IM3	IM2	IM1	IM0	Interface
0	1	0	1	2 data lane serial interface

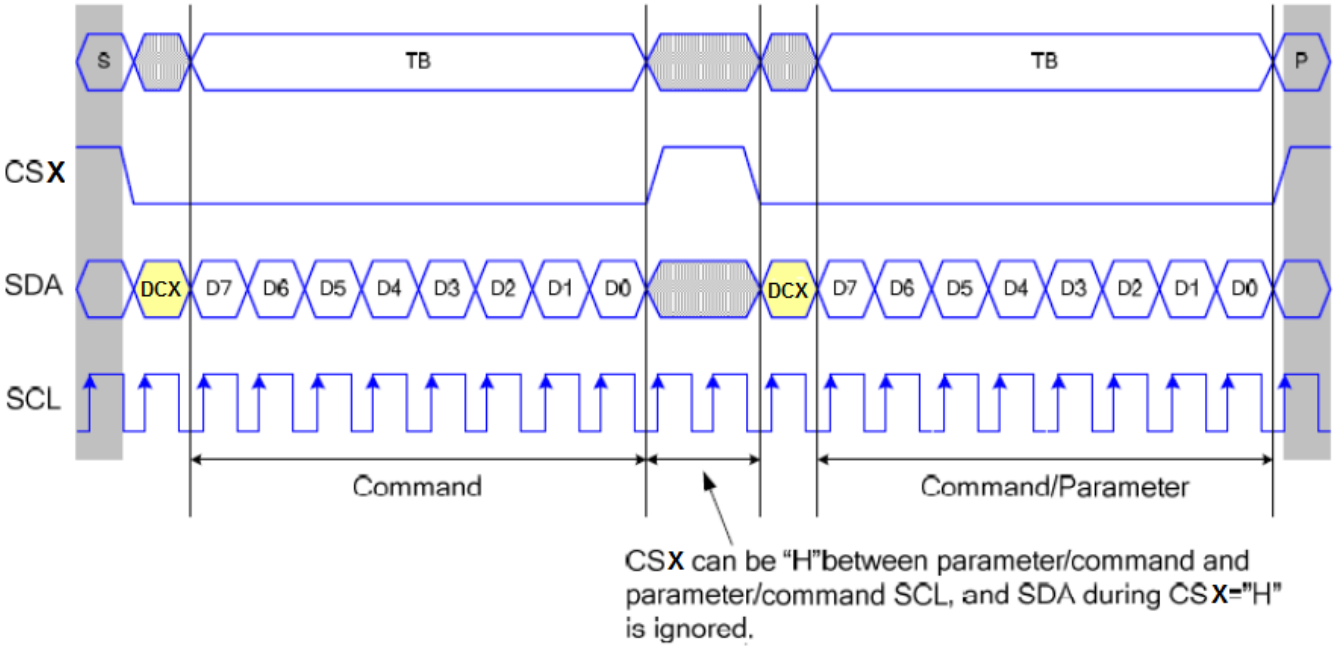
2 data lane serial interface use: CSX (chip enable), DCX (serial clock) and SDA (serial data input/output 1), and WRX (serial data input 2). To enter this interface, register spi_2wire_mode, which is located in the 3rd parameter of command F6h, should be set.

2 data lane hardware suggestion and Pin description:
2 data lane serial interface, IM[3:0]=0101



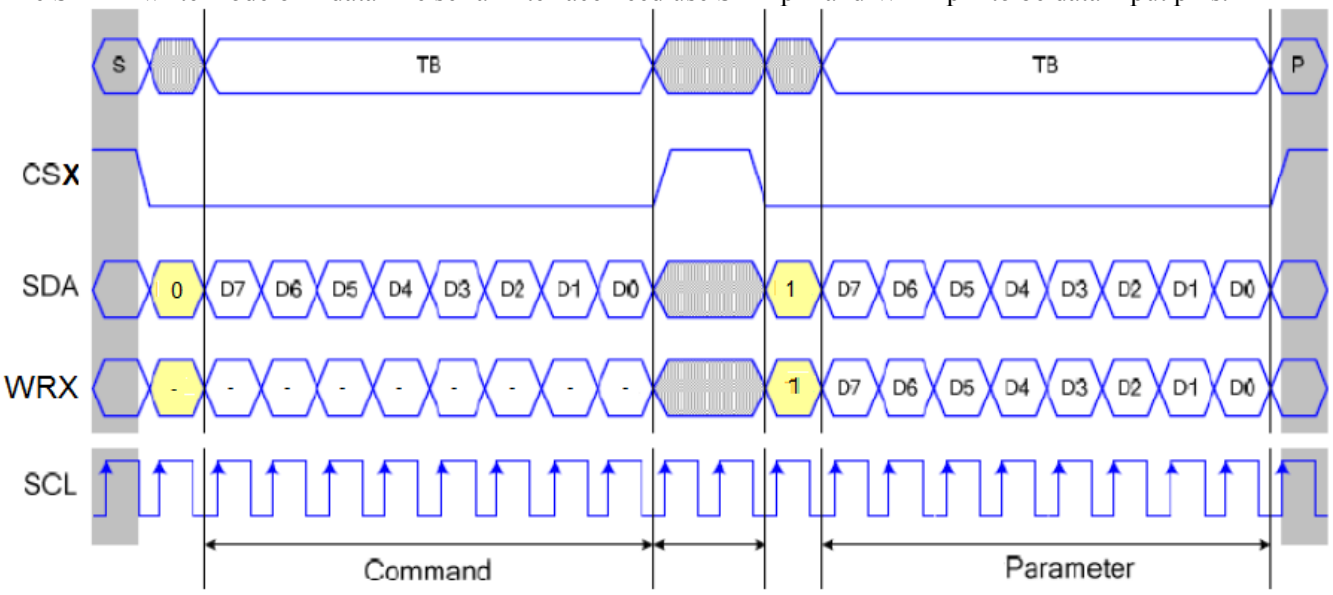
Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial data input/output1
WRX	Serial data input2

Command write mode:
The command write protocol of 2 data lane serial interface is the same with the 3-wire serial interface,so users can ignore the input data of WRX.
Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



SRAM write mode:

The SRAM write mode of 2 data line serial interface need use SDA pin and WRX pin to be data input pins.



Read function:

The read mode of 2 data lane serial interface is the same with the 3-wire serial interface and WRX pin can be ignored.

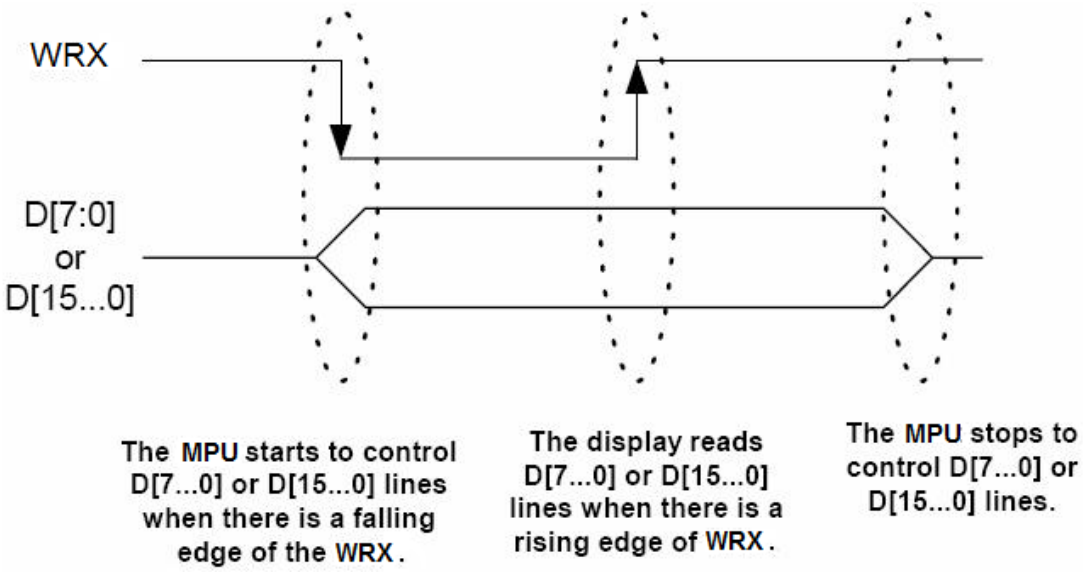
8.1.2 Parallel Interface

The Module uses a 11-wires 8-data parallel interface (IM0 = Low) or 19-wires 16-bit parallel interface (IM0 = High). The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[7…0] or D[15…0] is parallel data.
The Graphics Controller Chip reads the data at the rising edge of WRX signal. The DCX is data/command flag. When DCX = "1", D15 (or D7) to D0 bits are display RAM data or command parameters. When DCX = "0" D15 (or D7) to D0 bits are commands.

8.1.2.1 Write Cycle/Sequence

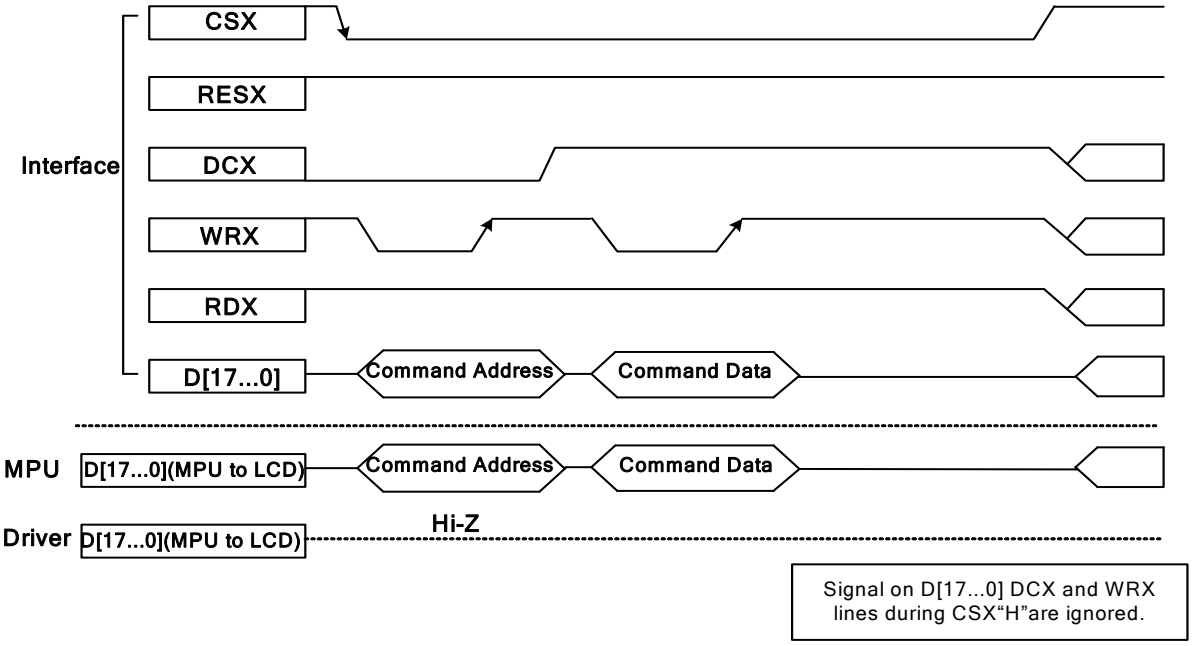
The write cycle means that the MPU writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and 8 (D[7..0]) or 16 (D[15…0]) data signals. DCX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (='0') and vice versa it is data ('1').

The write cycle is described in the following figure.



Note: WRX is an unsynchronized signal (it can be stopped).

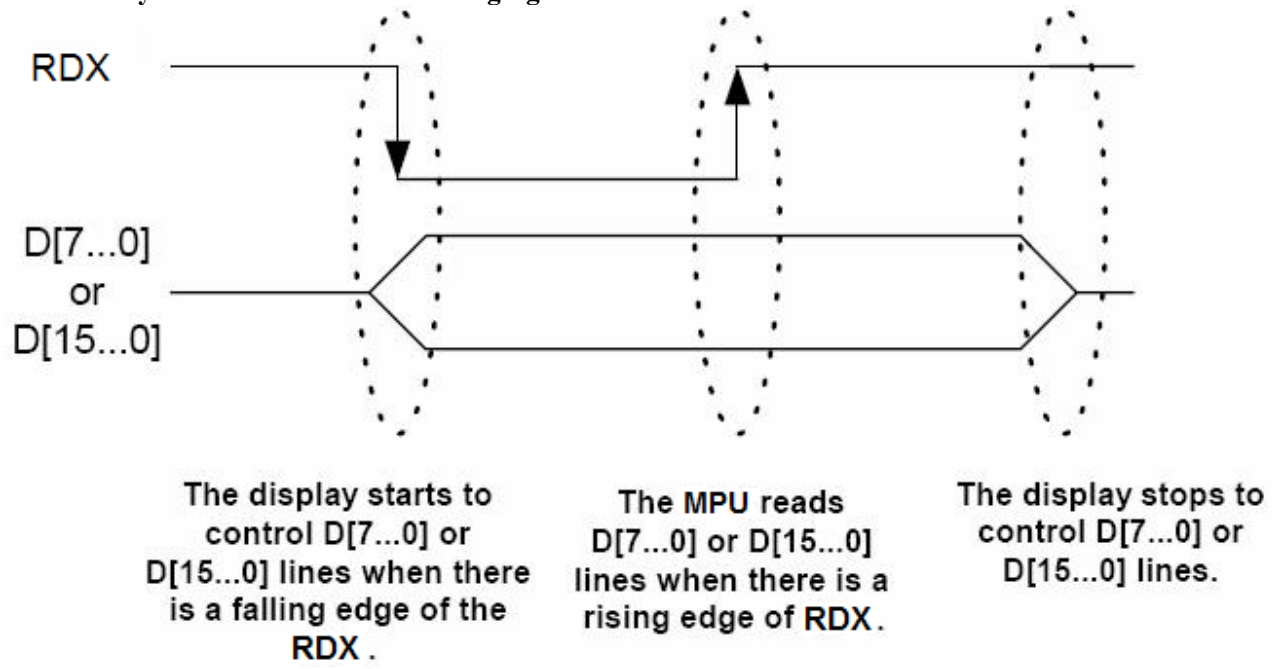
Parallel I/F write Sequence-Example



8.1.2.2 Read Cycle/Sequence

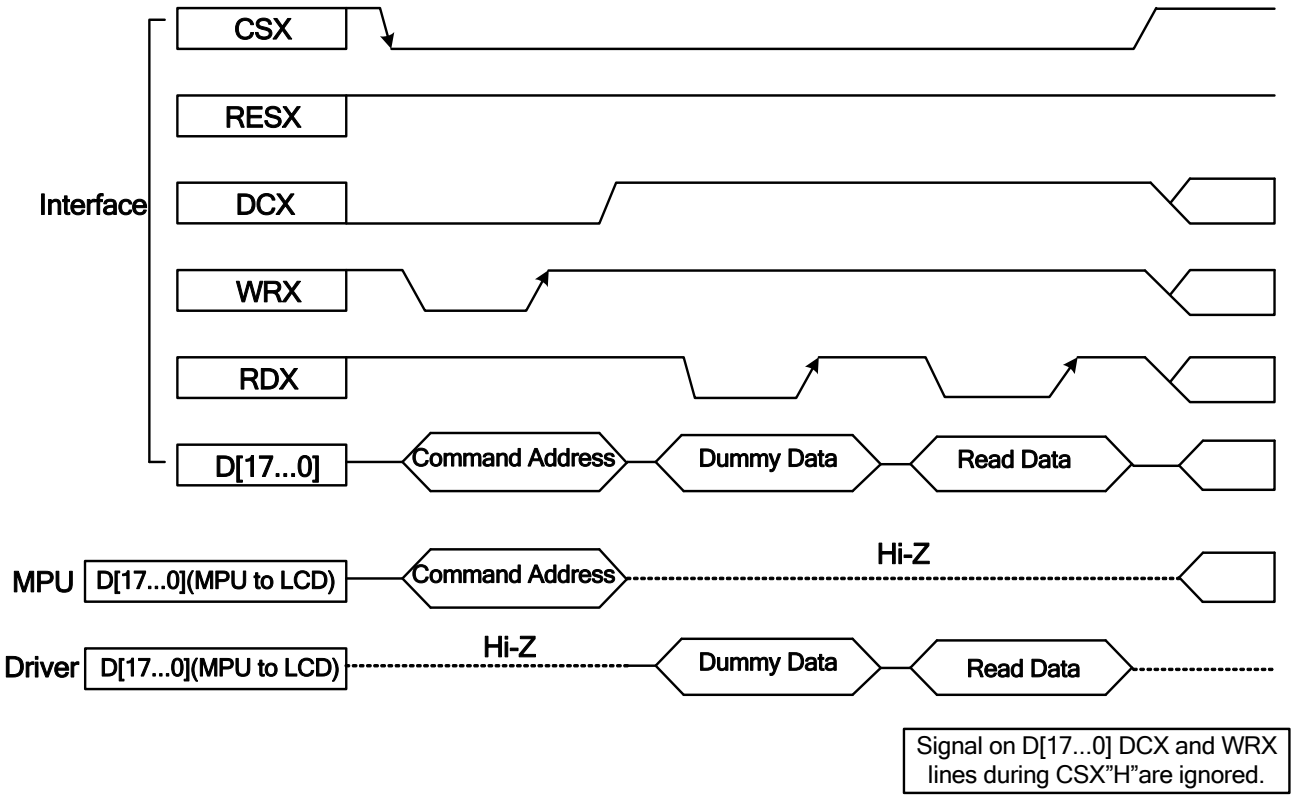
The read cycle (RDX high-low-high sequence) means that the MPU reads information from the display via interface. The display sends data (D[7...0] or D[15…0]) to the MPU when there is a falling edge of RDX and the MPU reads data when there is a rising edge of RDX.

The RDX cycle is described the following figure.



Note: RDX is an unsynchronized signal (it can be stopped).

Parallel I/F Read Sequence-example



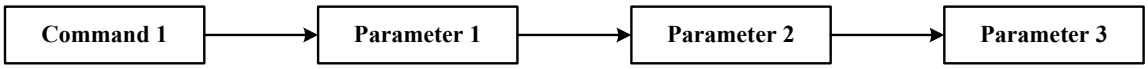
Note:

Read Data is only valid when DCX input is set High.

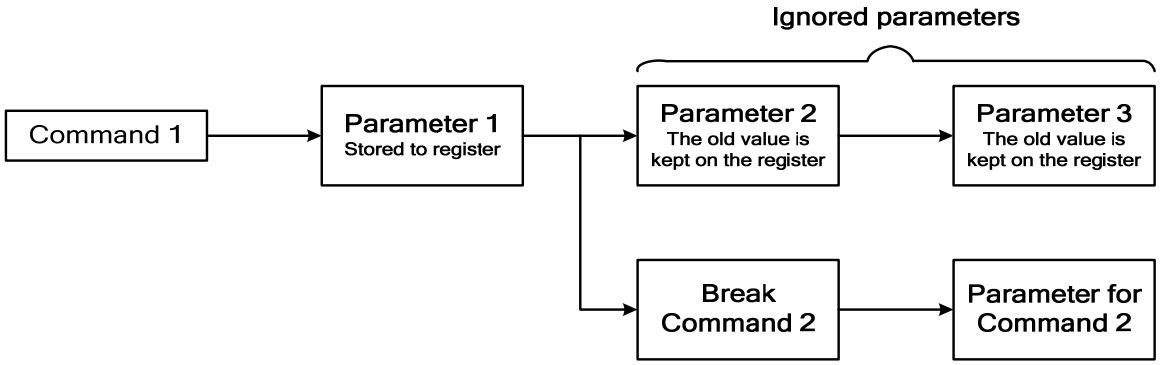
8.1.2.3 Display Module Data Transfer Break

If parameter 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the MPU then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameters after the break occurred is rejected if there is a new command as shown in the following example:

Without break

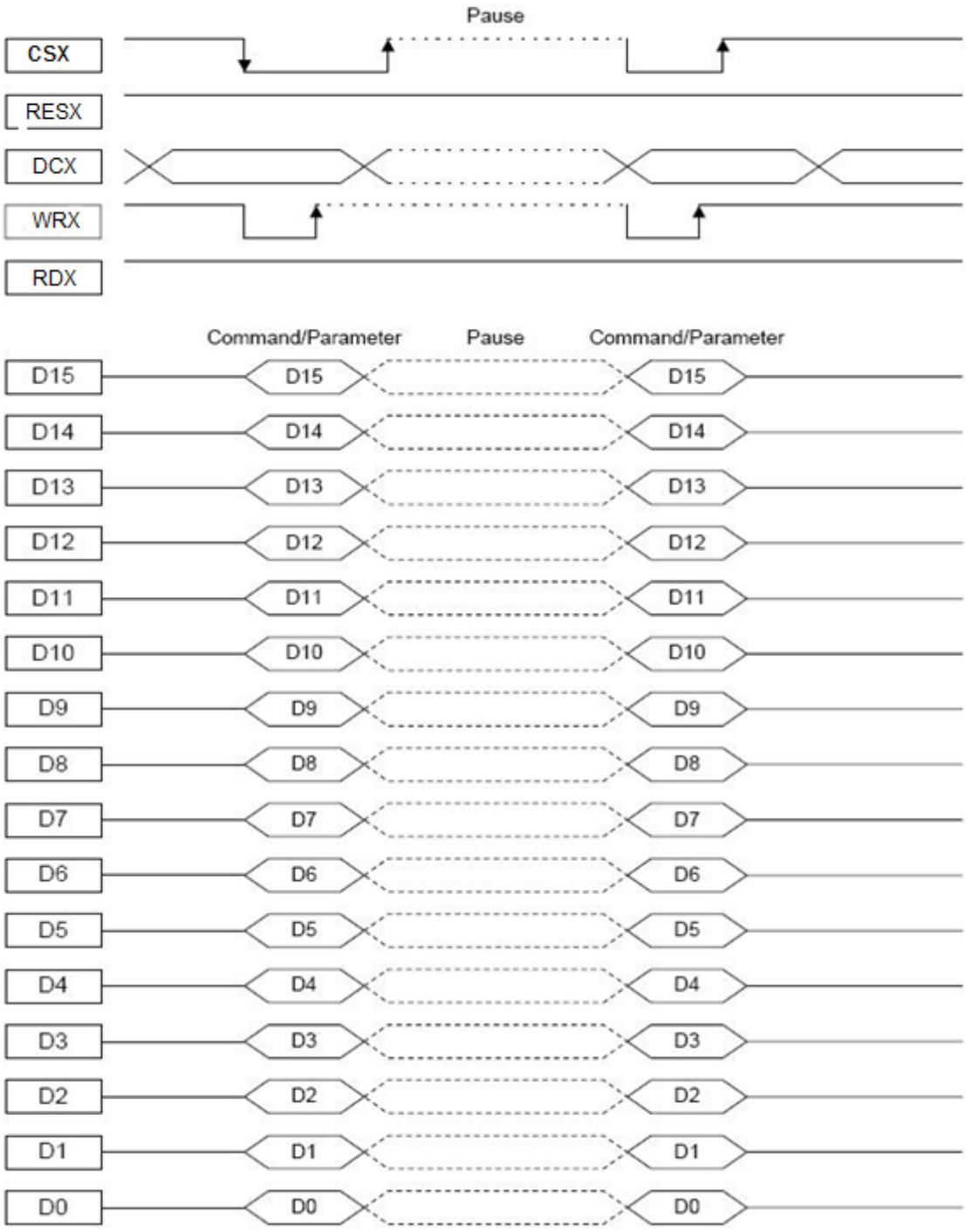


With break



Break can be another command or noise pulse.

8.1.2.4 Display Module Data Transfer Pause



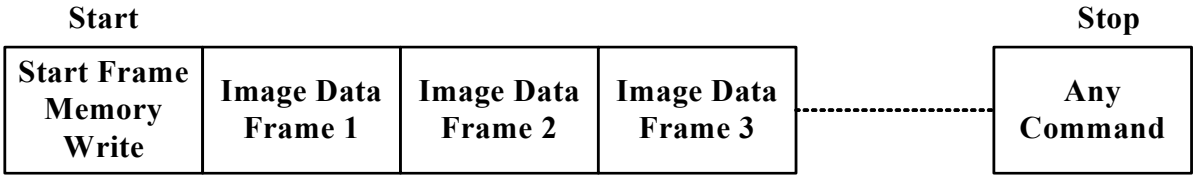
This applies to the following 4 conditions:
1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

8.1.2.5 Display Module Data Transfer Modes

The module has four color modes for transferring data to the display data RAM. These are 16-bit color per pixel, 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

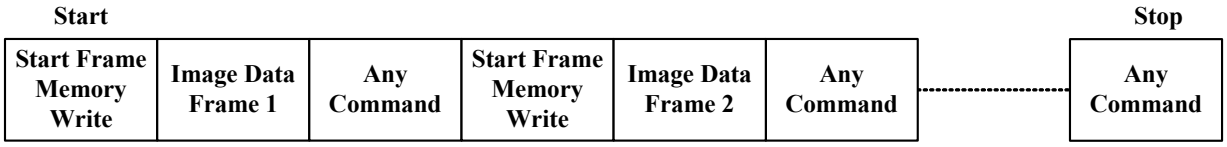
8.1.2.5.1 Method 1

The image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



8.1.2.5.2 Method 2

The image data is sent and at end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame downloaded.



Note:

1. These apply to all Data Transfer Color modes on Parallel interface;
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored to the Frame Memory.

8.1.3 RGB Interface

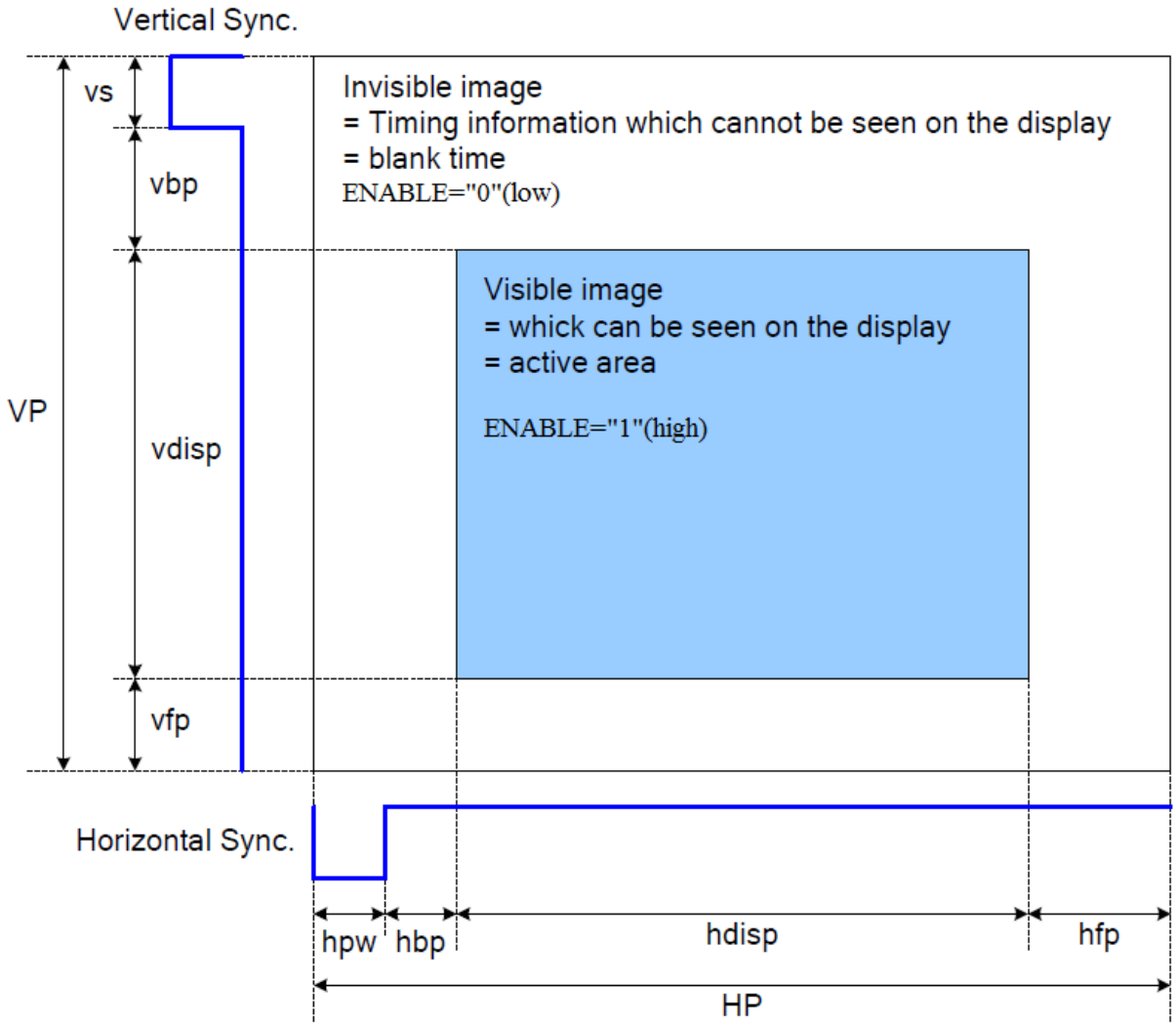
8.1.3.1 RGB interface Selection

The color format selection of RGB Interface for NV3029S is selected by setting the rim and dpi[2:0].

rim	dpi[2:0]	RGB Interface Mode	Data pins
0	110	18-bit 262K RGB Interface	DB[17:0]
0	101	16-bit 65K RGB Interface	DB[17:13], DB[11:1]
1	110	6-bit 262K RGB Interface	DB[5:0]
1	101	6-bit 65K RGB Interface	DB[5:0]

8.1.3.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	4	10	hpw+hbp=31	Clock
Horizontal Sync. Back Porch	hbp	8	10		Clock
Horizontal Sync. Front Porch	hfp	4	38	-	Clock
Vertical Sync. Width	vs	2	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

8.1.3.3 RGB Interface Mode Selection

NV3029S supports two kinds of RGB interface, DE mode and SYNC mode. Each mode also can select with ram and without ram. The table shown below uses command B0h to select RGB interface mode.

RCM[1:0]	bypass_mode	Mode	Data Path	Control Signals
10	0	DE mode	without Ram	DOTCLK, ENABLE, VSYNC(optional), HSYNC(optional)
	1		Ram	
11	0	SYNC mode	without Ram	DOTCLK, VSYNC, HSYNC
	1		Ram	

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Graphics operation function	Not available	Available

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

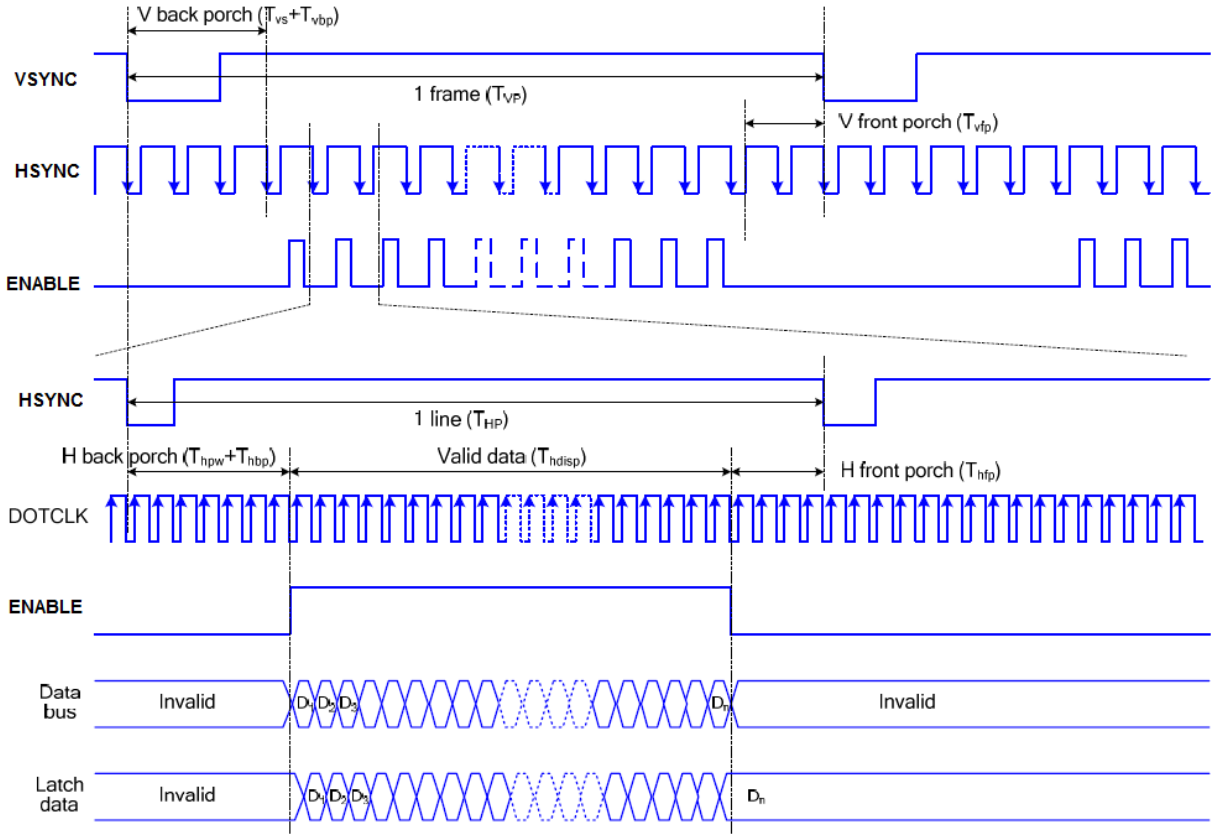
In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

Switching between the internal operation mode and the external RGB interface mode is prohibited.

8.1.3.4 RGB Interface Timing Diagram

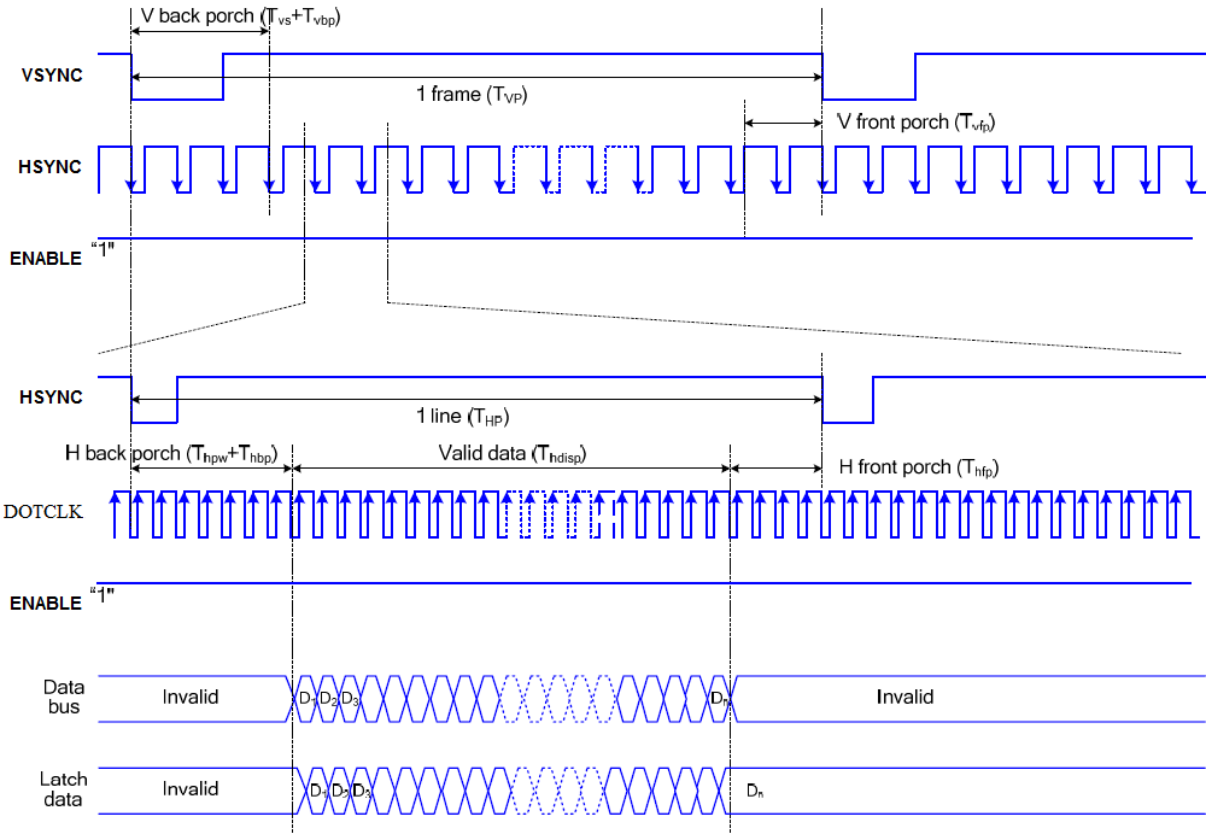
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

Note: The setting of front porch and back porch in MPU must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.

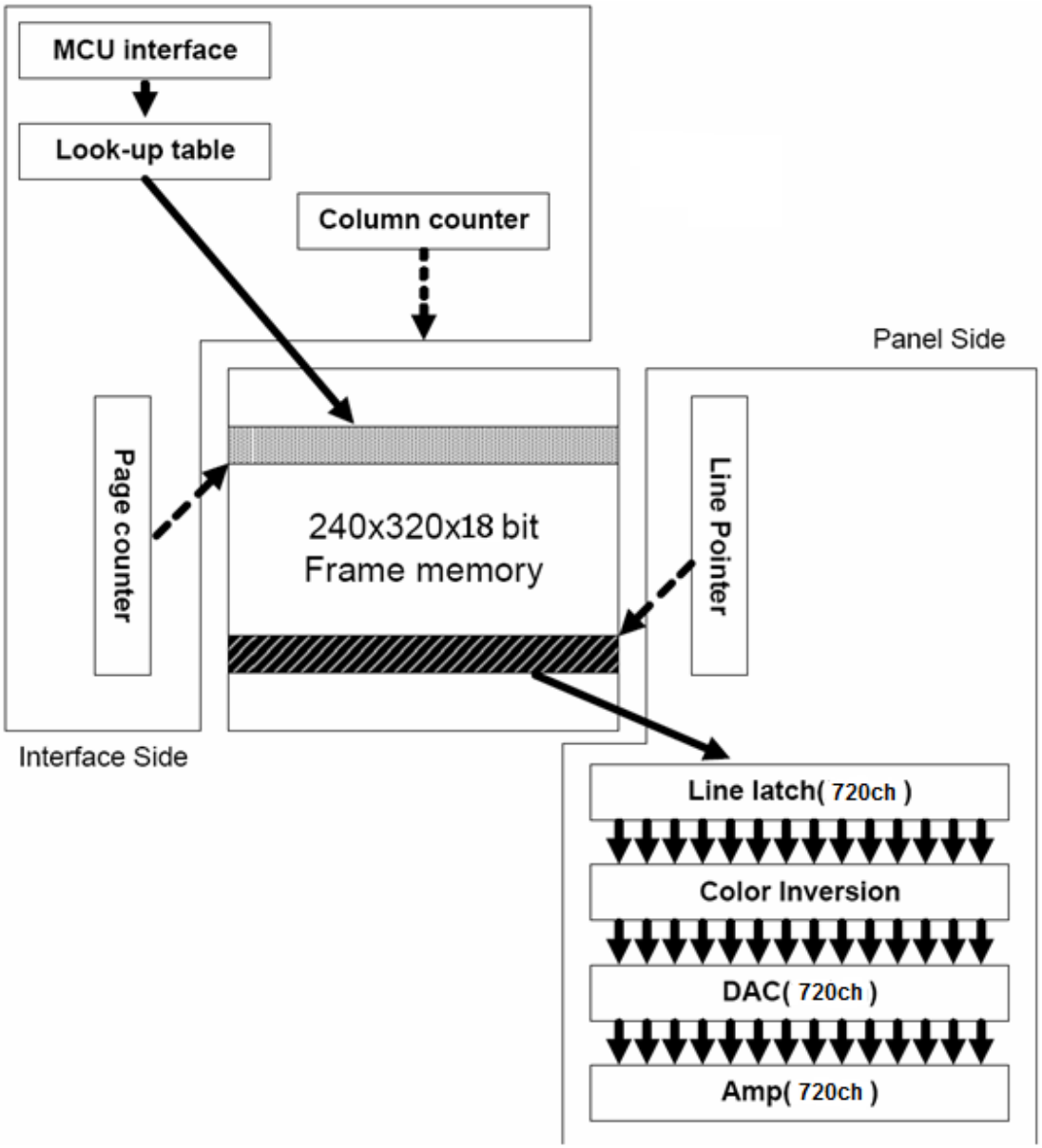


Timing chart of RGB interface SYNC mode

8.2 Display Data RAM

8.2.1 Configuration

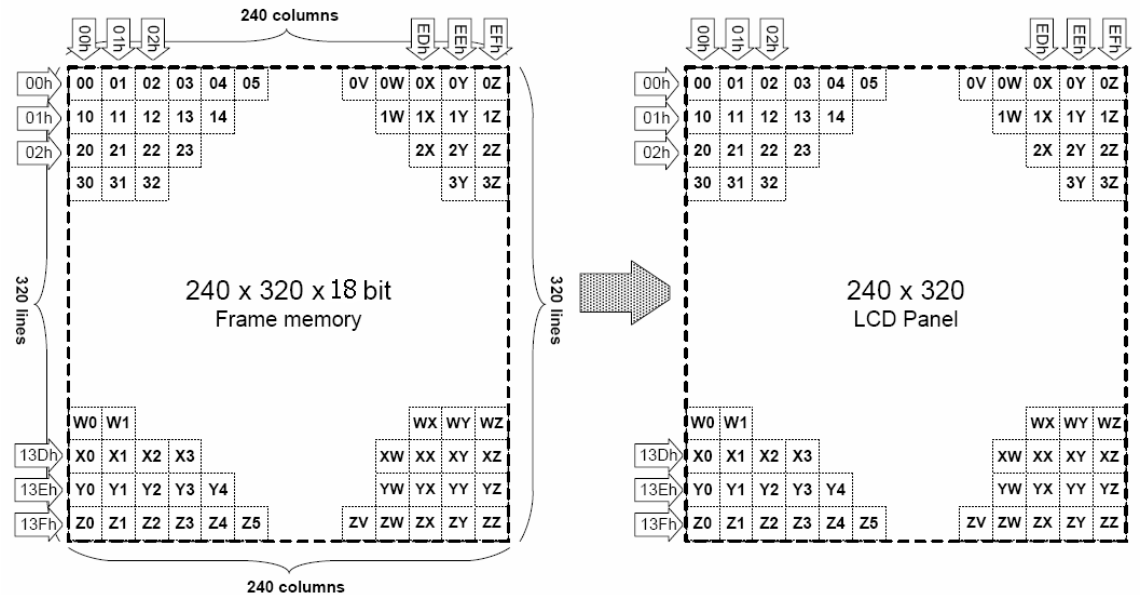
The display data RAM stores display dots and consists of 1,382,400 bits (240×320×18 bits).There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



8.2.2 Memory to Display Address Mapping

8.2.2.1 Normal Display On or Partial Mode On, Vertical Scroll Off

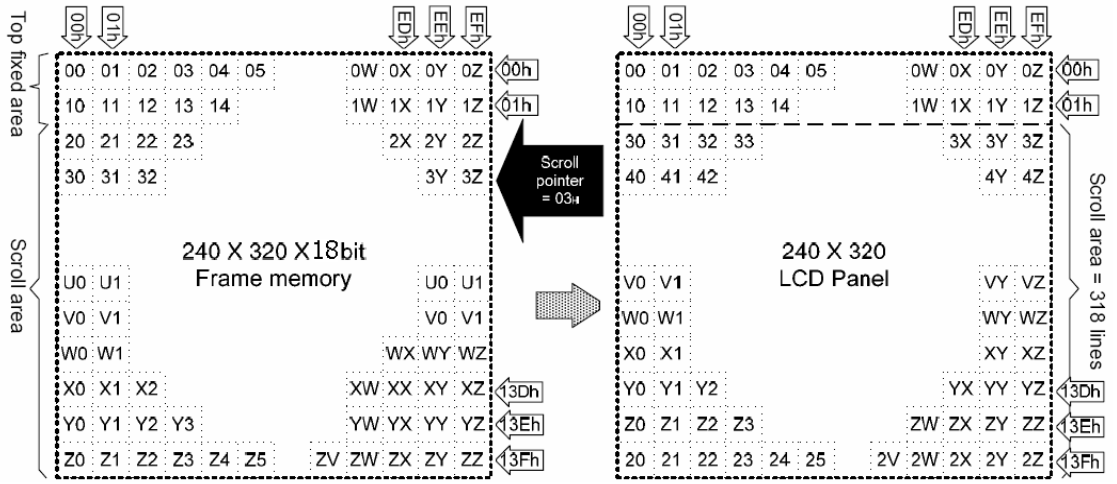
In this mode, contents of the frame memory within an area where column pointer is 0000h to 00Efh and page pointer is 0000h to 013Fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).



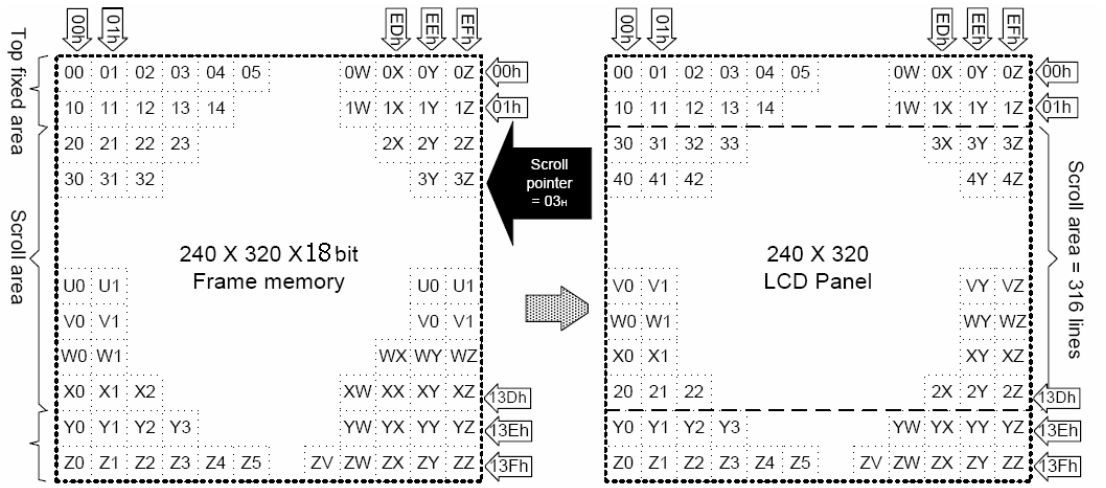
8.2.2.2 Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling” (33h) and “Vertical Scrolling Start Address” (37h).

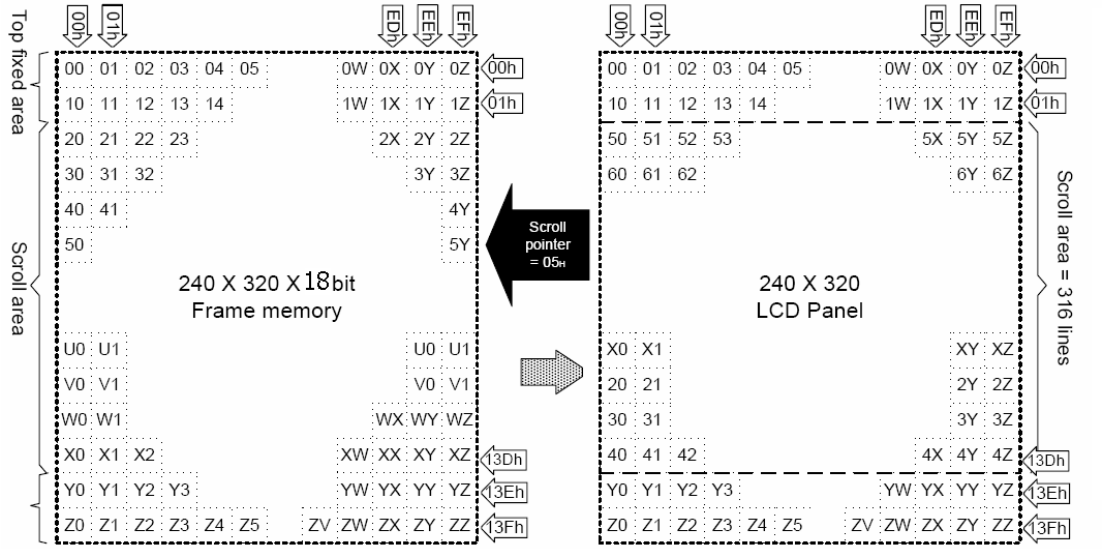
Example 1
TFA= 2, VSA = 318, BFA = 0 when MADCTL Bit B4 = 0



Example 2
TFA=2,VSA=316,BFA=2 when MADCTL bit B4=0



Example 3
TFA=2,VSA=316,BFA=4 when MADCTL bit B4=0



Note:
When Vertical Scrolling Parameters(TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

8.2.2.3 Vertical Scroll example

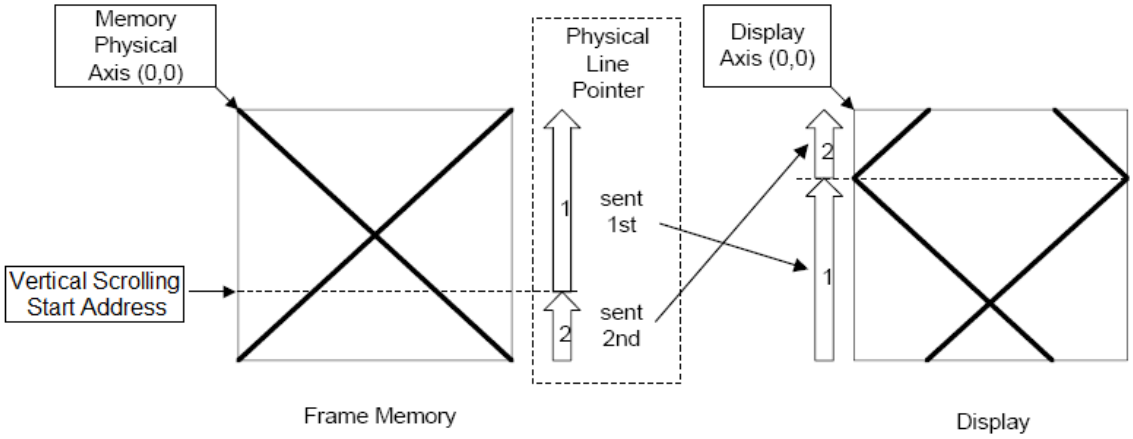
Case 1: TFA + VSA + BFA < 320

N/A. Do not set TFA + VSA + BFA < 320, unless unexpected picture will be shown.

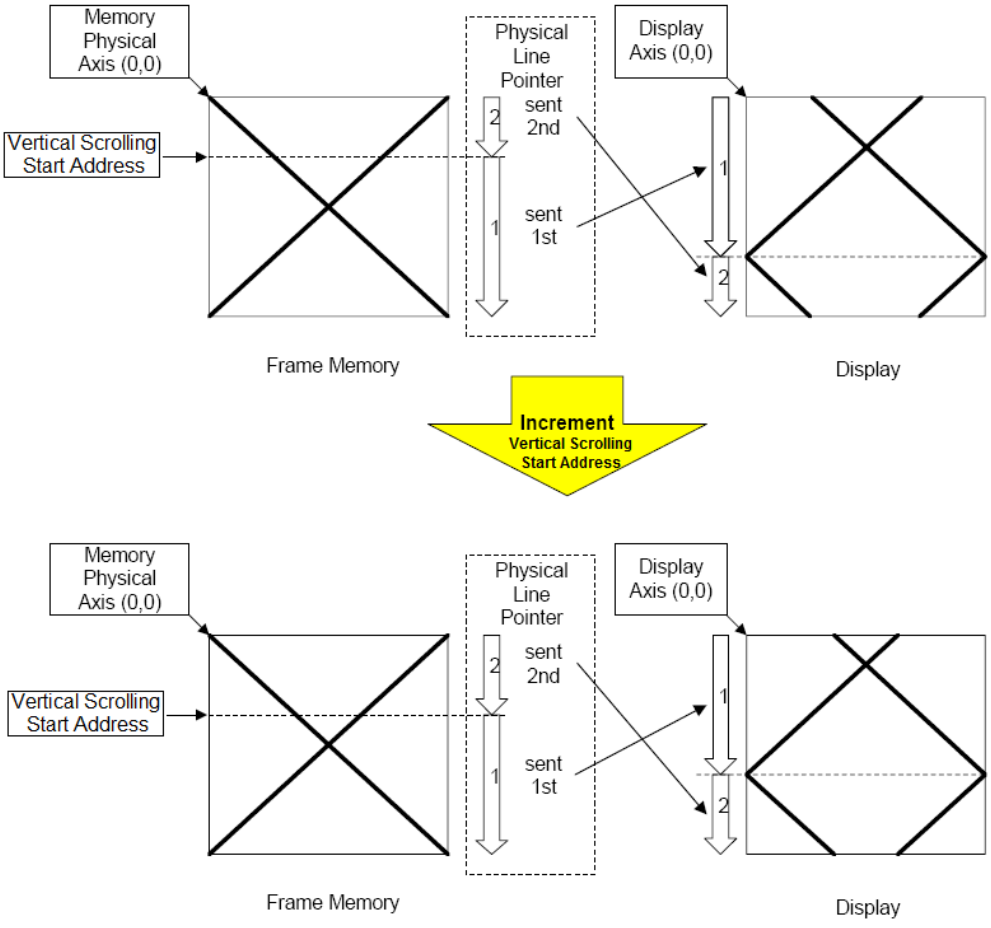
Case 2: TFA + VSA + BFA = 320 (Rolling Scrolling)

Example 2-a. When TFA = 0, VSA = 320, BFA = 0 and Vertical Scrolling Start Address = 40.

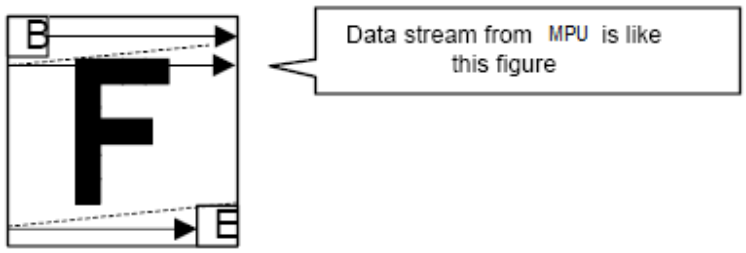
MADCTL parameter B4= "0"



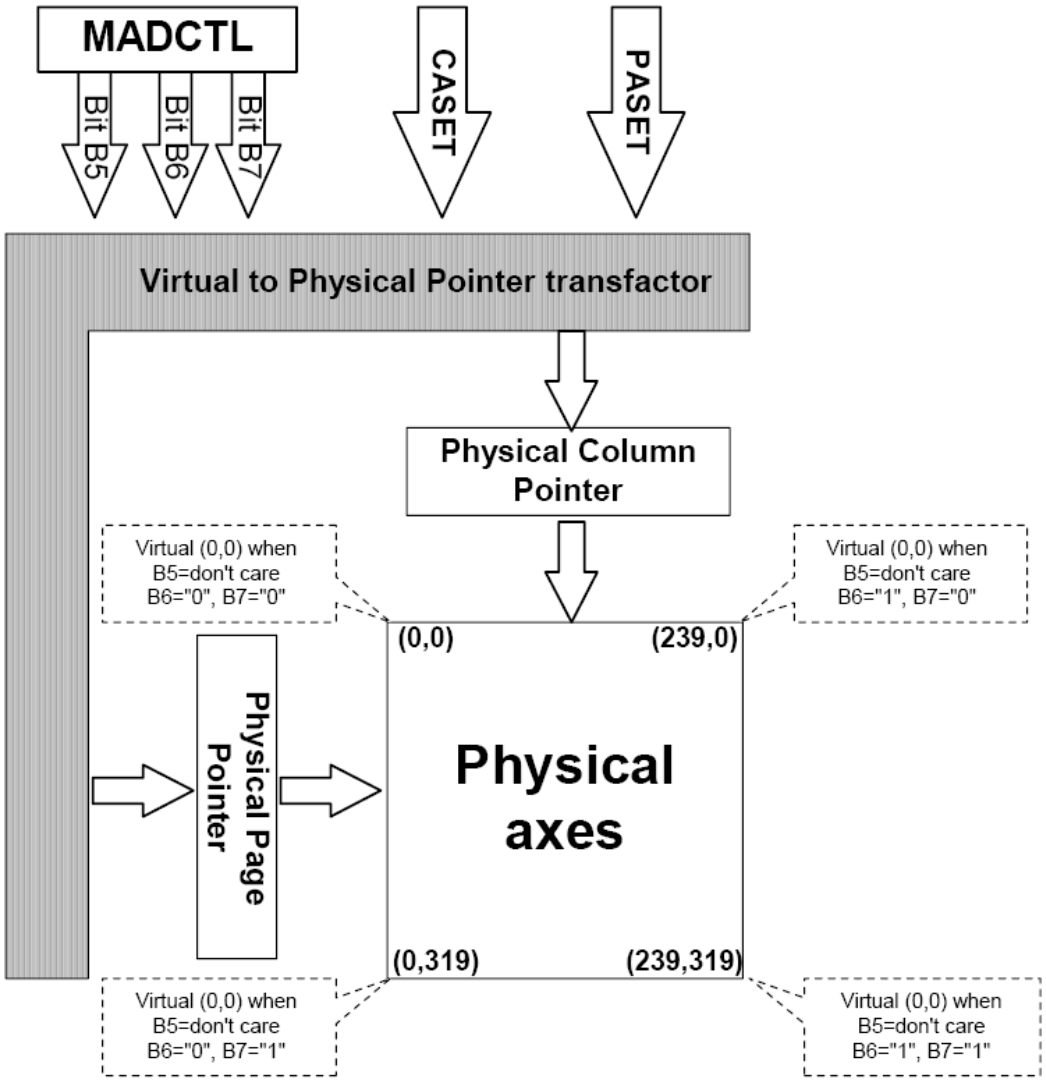
MADCTL parameter B4= "1"



8.2.3 MPU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” command, Bits B5, B6, B7 as described below.



For each image orientation, the controls for the column and page counters apply as below:

B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direc to(239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls for the column and page counters apply as below:

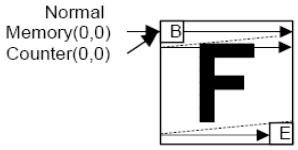
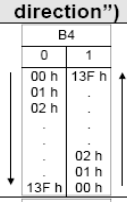
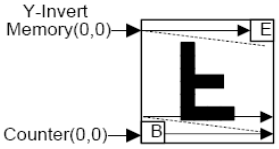
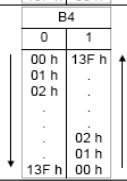
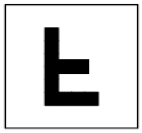
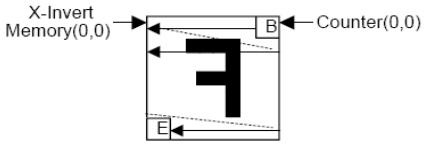
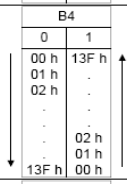
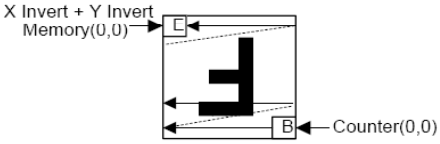
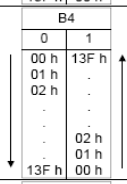
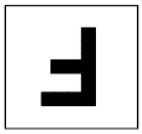
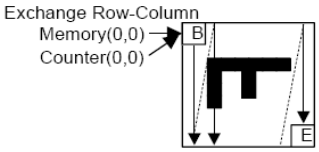
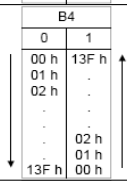
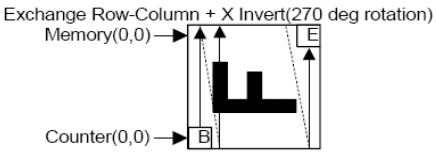
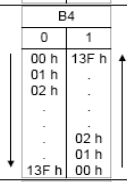
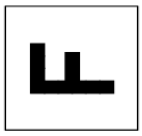
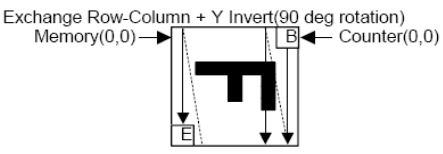
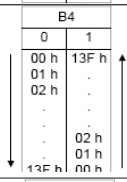
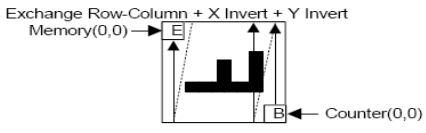
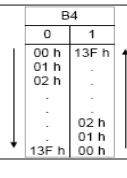
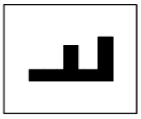
Condition	Column Counter	Page Counter
When memory write/memory read command is accepted	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End Column”	Return to “Start Column”	Increment by 1
The Column counter value is larger than “End Column” and the Page counter value is larger than “End Page”	Return to “Start Column”	Return to “Start Page”

Note:
Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

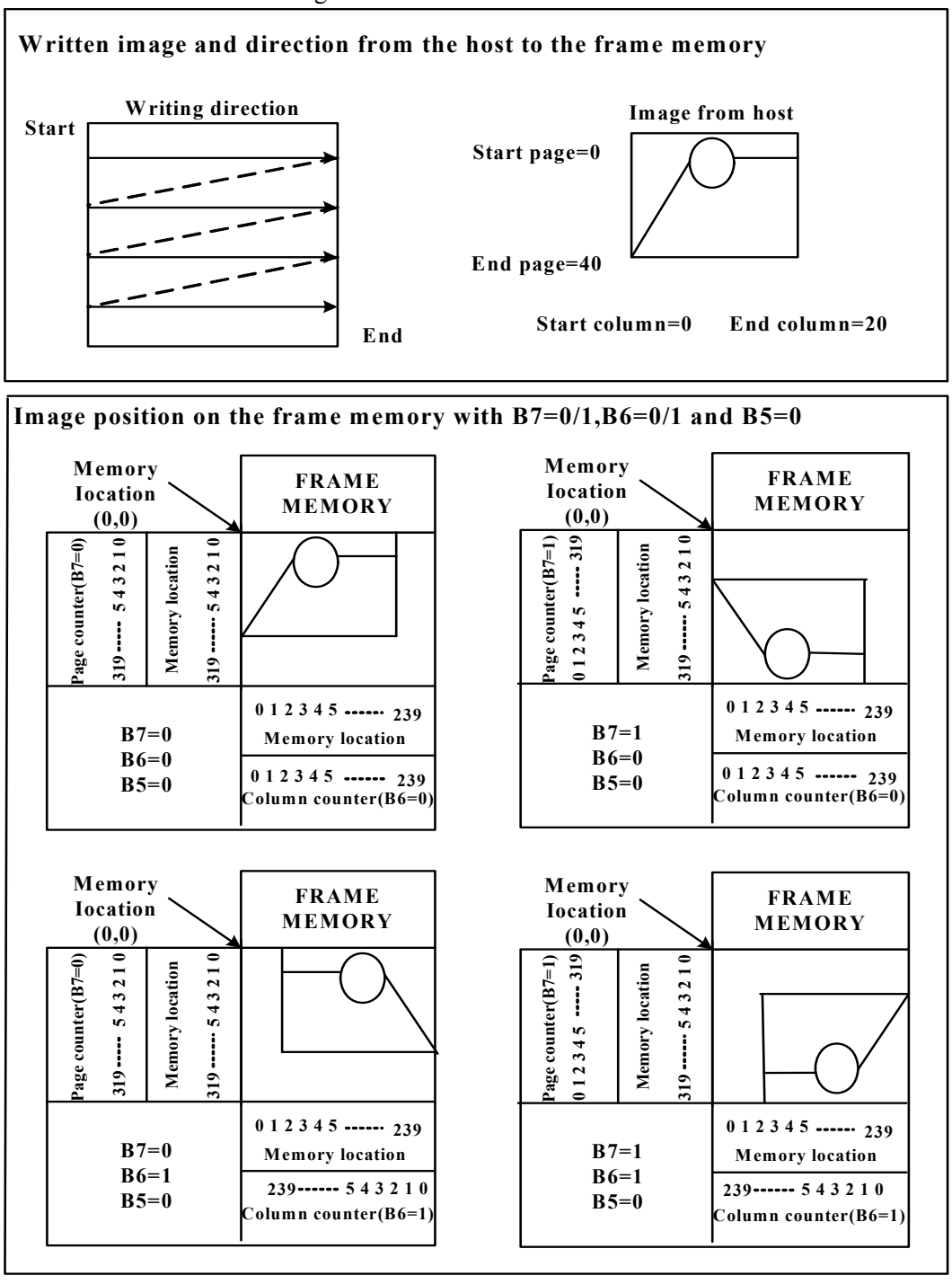
One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

This resultant image for each orientation setting is illustrated below:

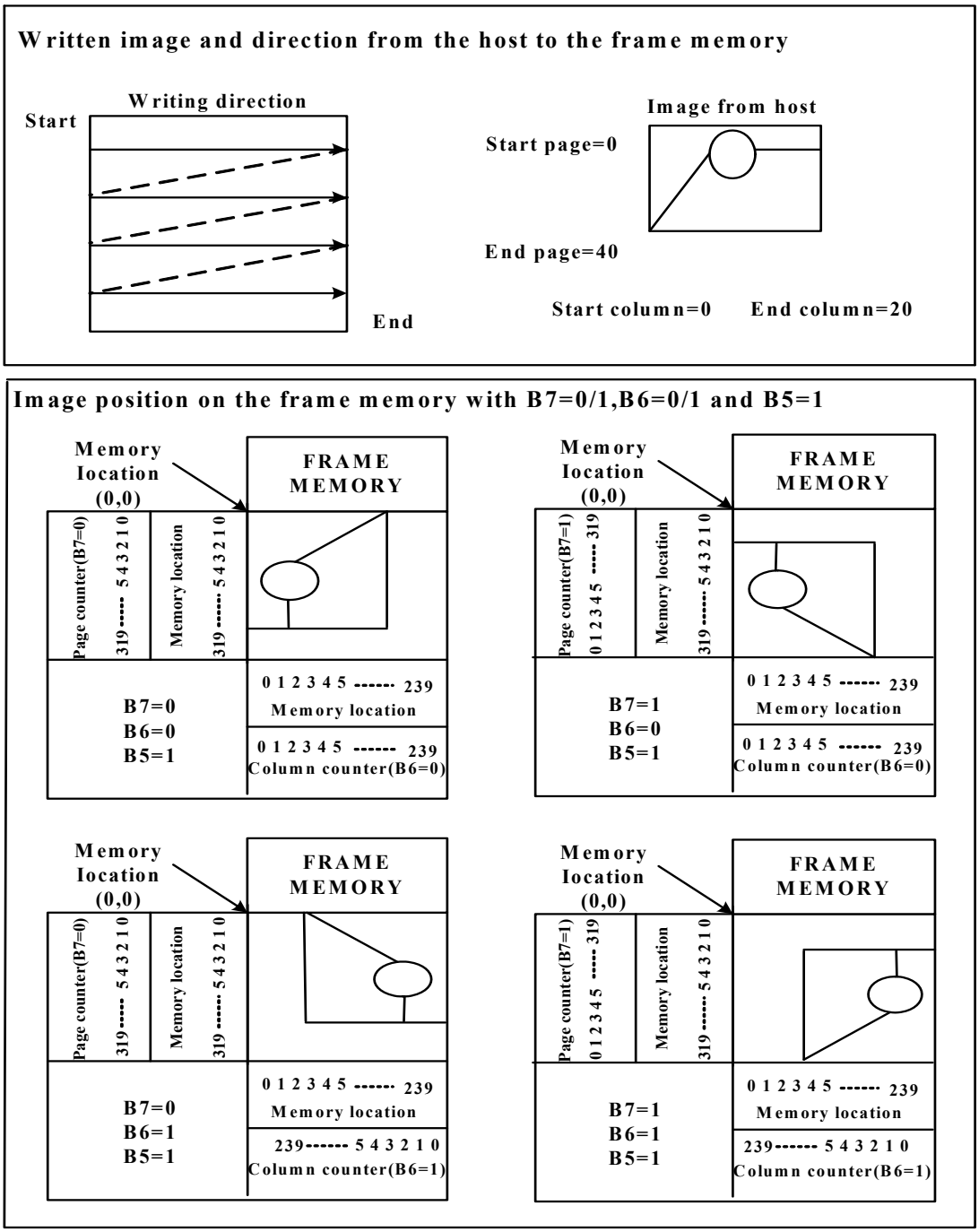
B5 B6 B7 (Bits)	Image in the memory ("→" means "MCU to memory read/write direction")	B4 Bit ("→" means "RAM to display scan direction")	Image in the Display
0 0 0			
0 0 1			
0 1 0			
0 1 1			
1 0 0			
1 0 1			
1 1 0			
1 1 1			

Example for rotation with B7, B6 and B5
This example is using following values:
start page = 0, end page = 40, start column = 0 and end column = 20
= Commands: page address set (0,40) and column address set (0,20).

The sent figure is as follows and its sending order is as follows:



The sent figure is as follows and its sending order is as follows:



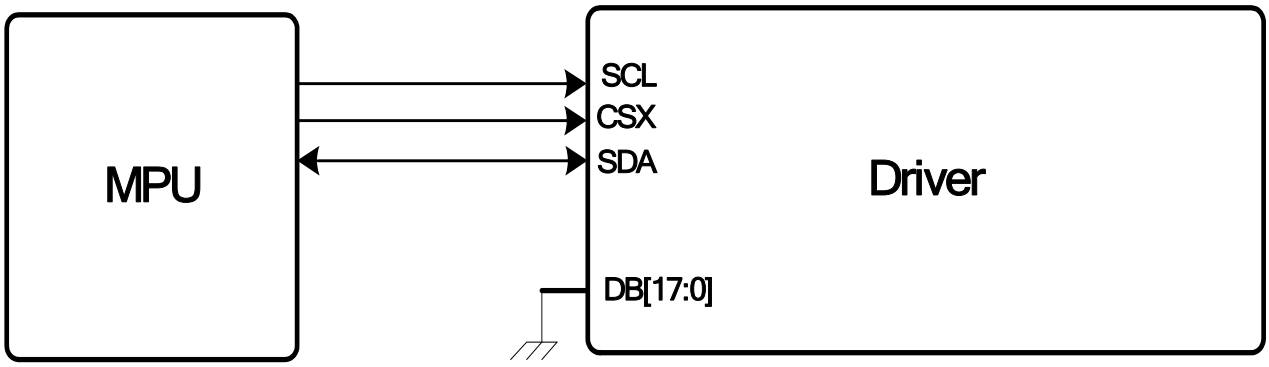
8.3 Display Data Format

NV3029S supplies 18-/16-/9-/8-bit parallel interface with 8080-Ⅰ /8080-Ⅱ series, 3-/4-wire serial interface and 6-/16-18-bit parallel RGB interface. The parallel interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters rcm[1:0].

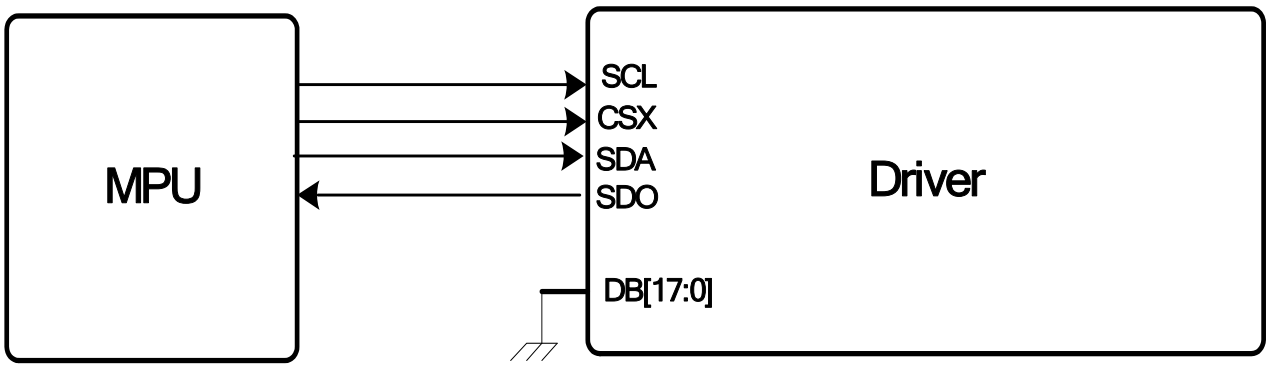
8.3.1 3-wire Serial Interface

The 3-wire/9-bit serial bus interface of NV3029S can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-wire SPI interface.

3-wire Serial interface Ⅰ

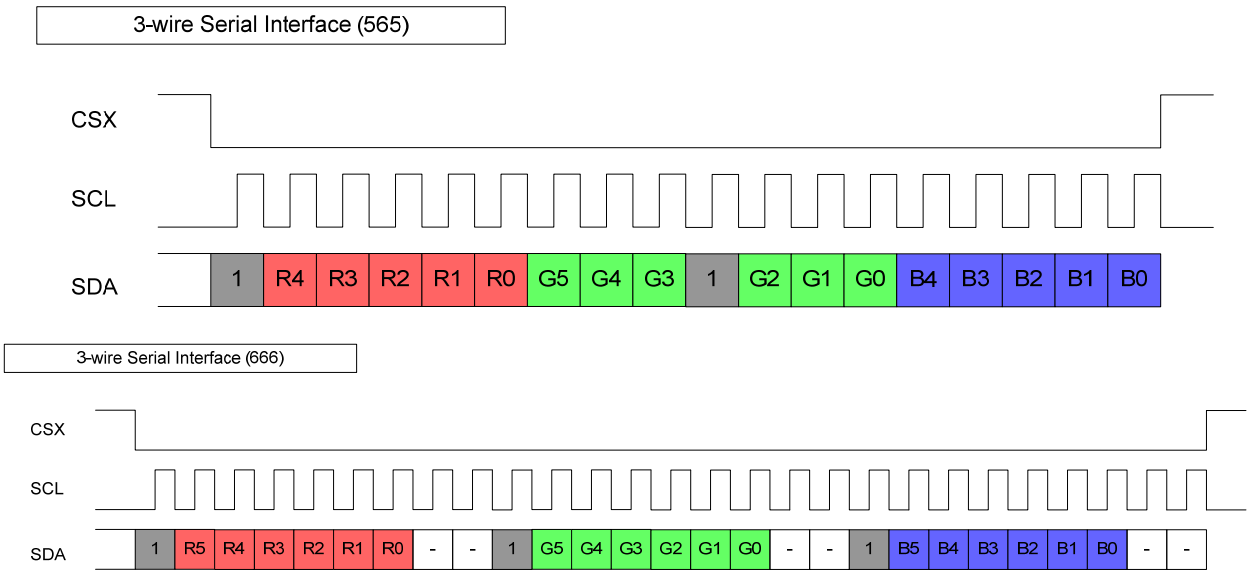


3-wire Serial interface Ⅱ



In 3-wire serial interface, different display data format is available for two color depths supported by the LCM listed below:

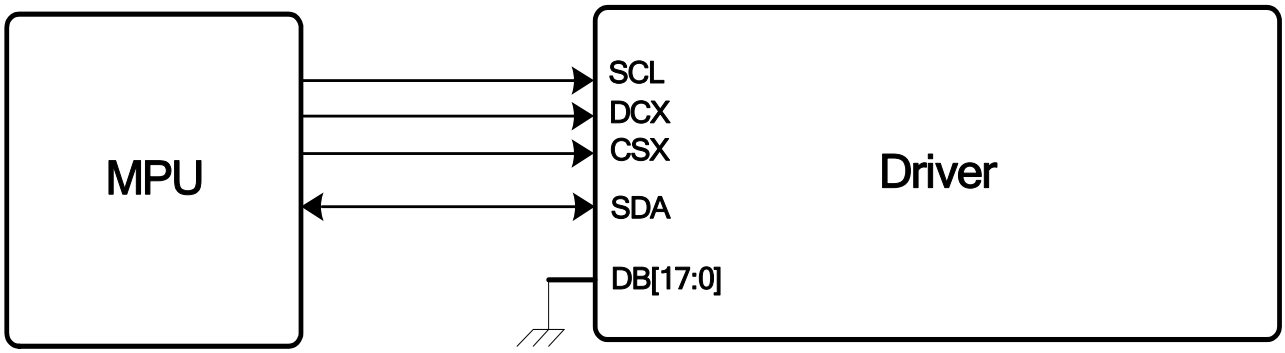
1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.



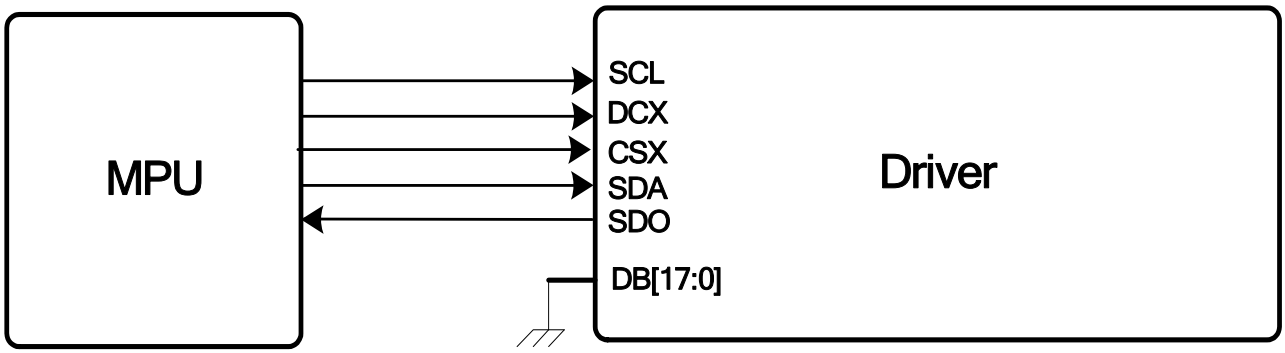
8.3.2 4-wire Serial Interface

The 4-wire/8-bit serial bus interface of NV3029S can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-wire SPI interface.

4-wire Serial interface I



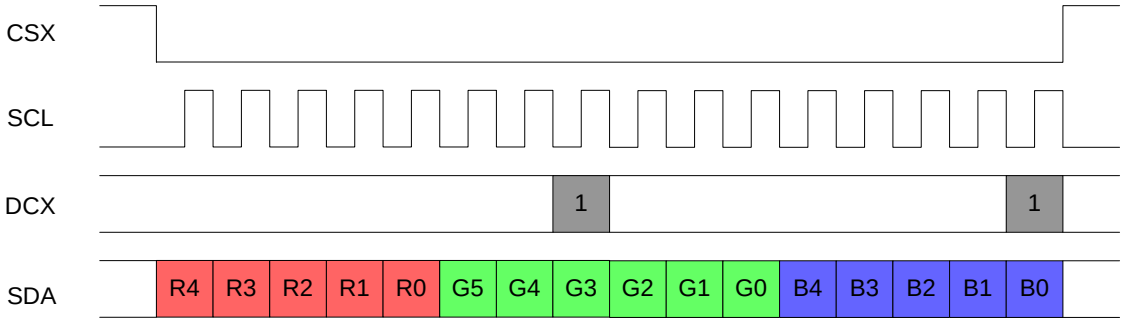
4-wire Serial interface II



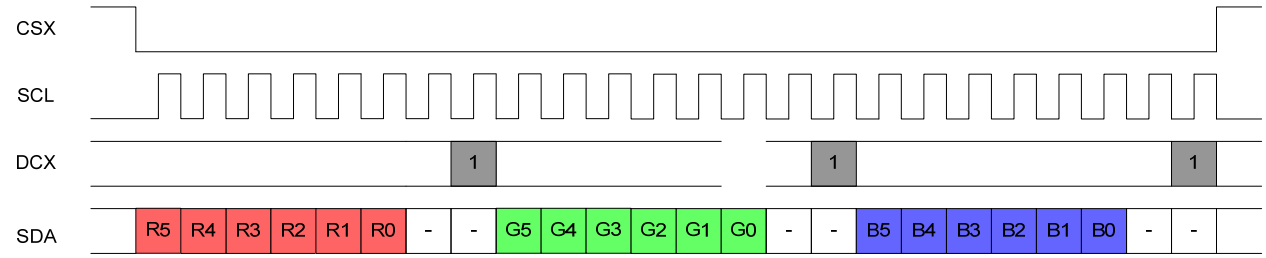
In 4-wire serial interface, different display data format is available for two color depths supported by the LCM listed below:

1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.

4-wire Serial Interface (565)

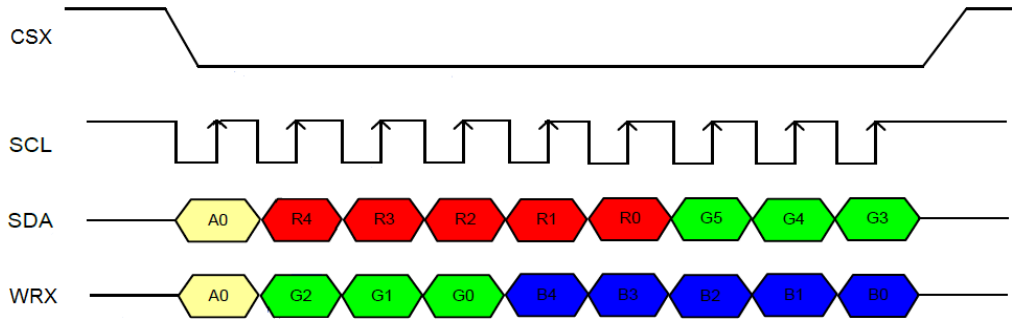


4-wire Serial Interface (666)

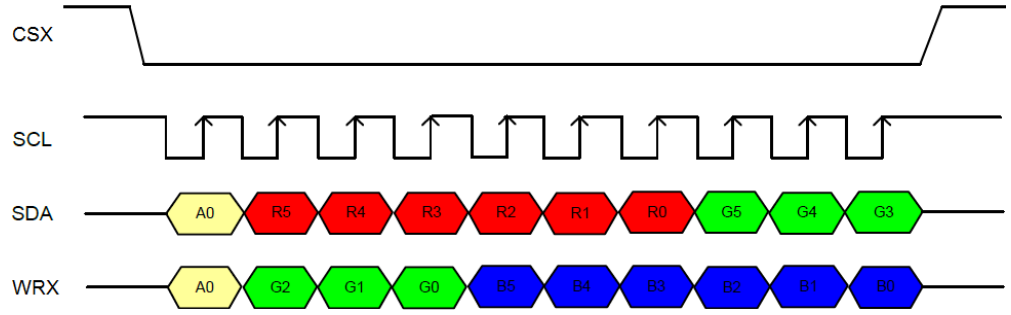


8.3.3 2 data lane serial interface

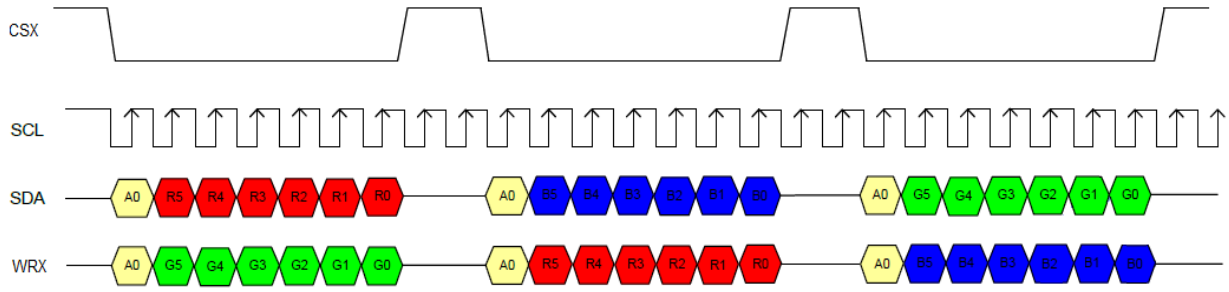
1) RGB565



2) RGB666,mdt=00



3) RGB666,mdt=01



8.3.4 Parallel Interface

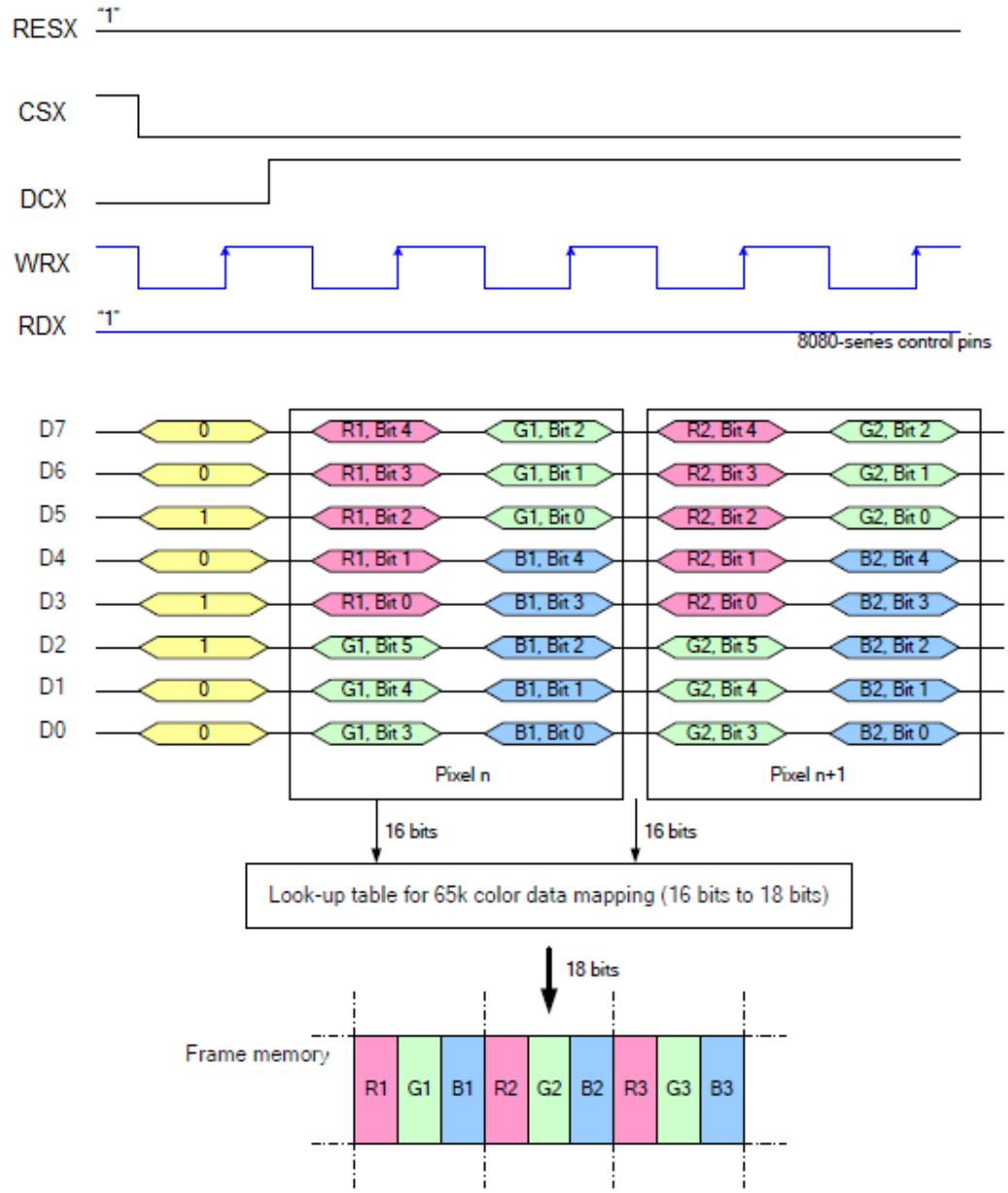
8.3.4.1 8080-Ⅰ series 8-bit Parallel Interface

The 8080-Ⅰ series 8-bit parallel interface of NV3029S can be used by setting IM[3:0]=”0000b”. Different display data formats are available for two Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.3.4.1.1 16-bit/pixel

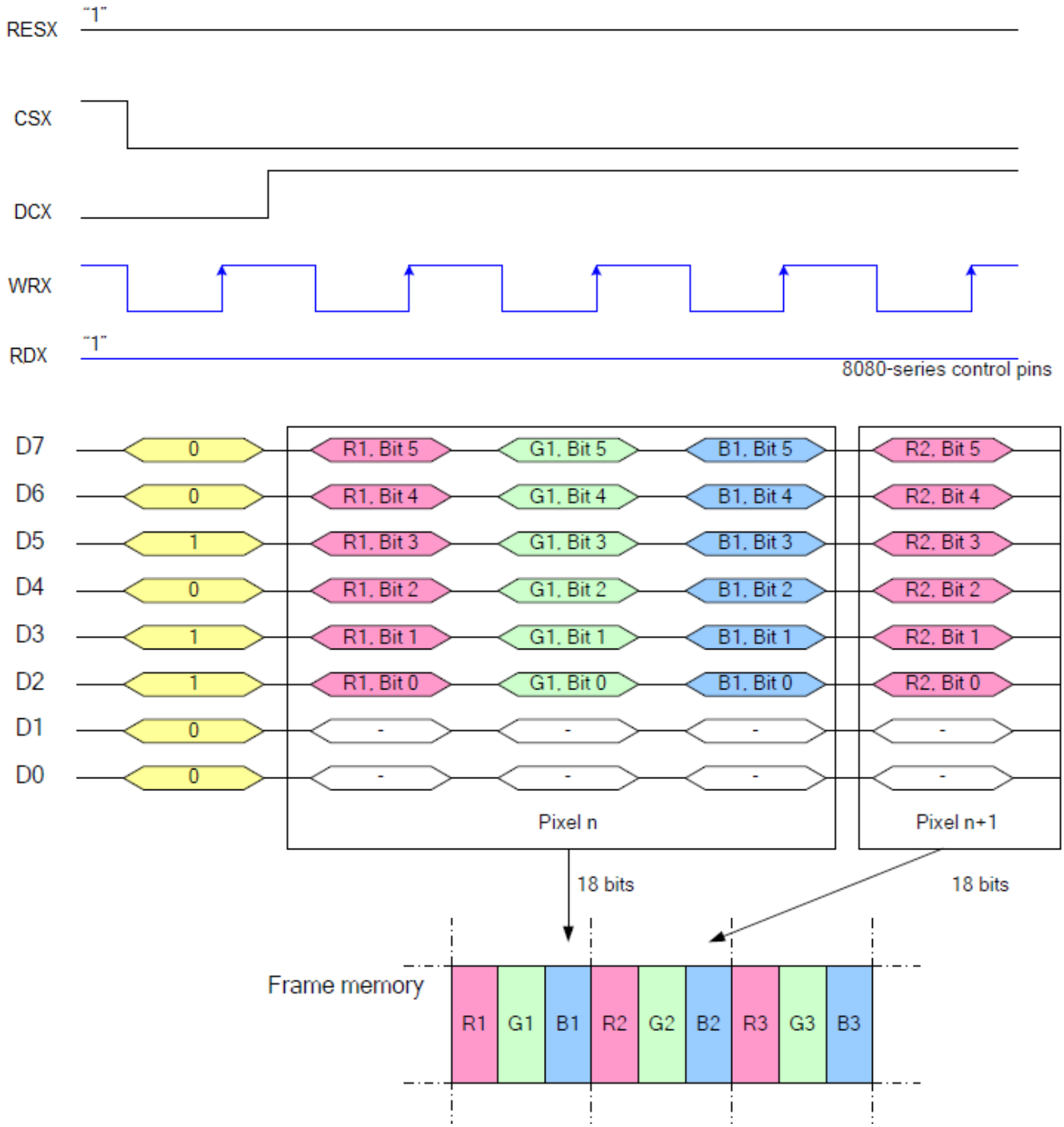
There is 1pixel (3 sub-pixels) per 2-byte



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.
Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.1.2 18-bit/pixel

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

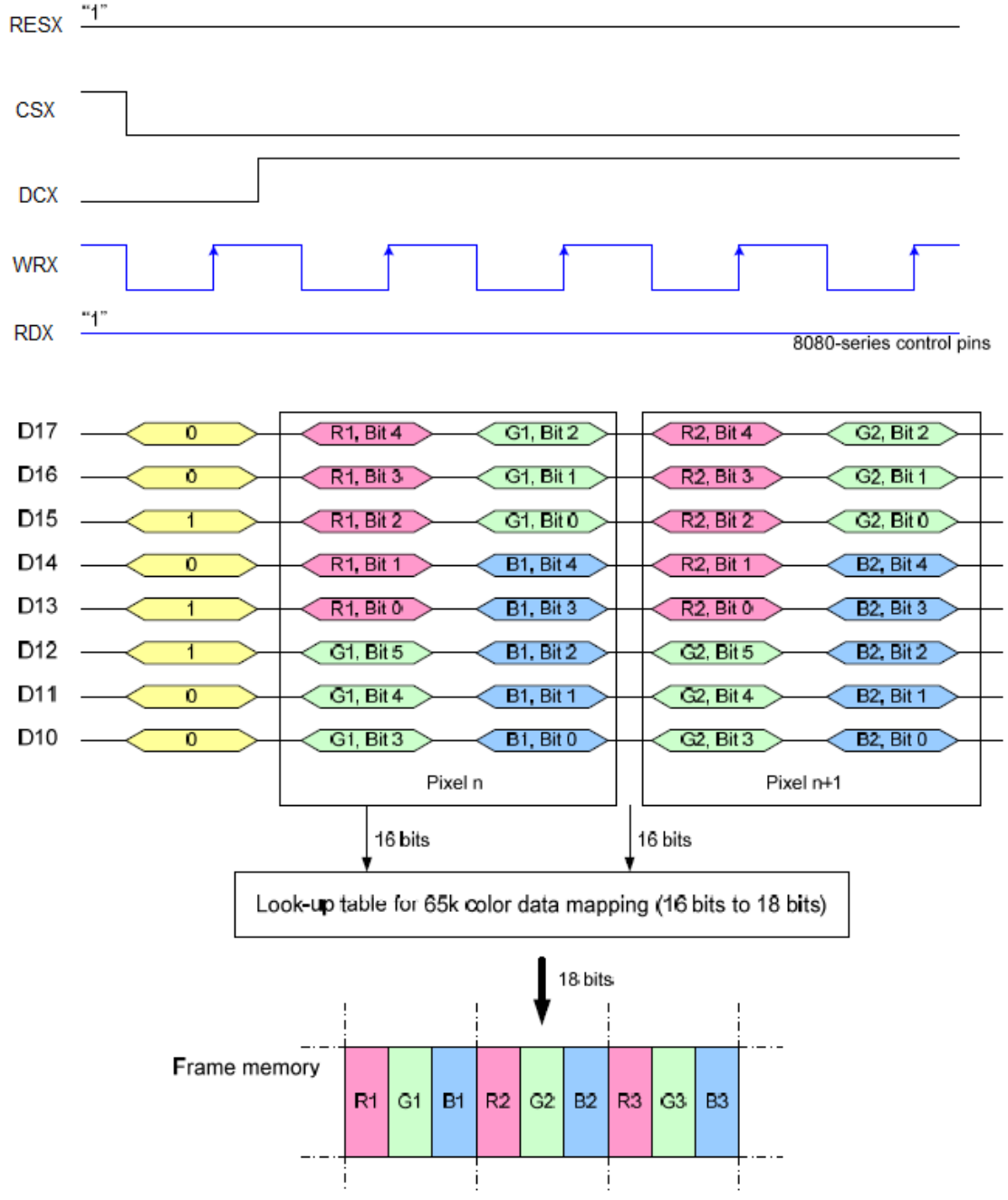
Note 3: '-' = Don't care – Can be set to '0' or '1'.

8.3.4.2 8080-Ⅱ series 8-bit Parallel Interface

The 8080-Ⅱ series 8-bit parallel interface of NV3029S can be used by setting IM[3:0]=”1001b”. Different display data formats are available for two Colors depth supported by listed below.

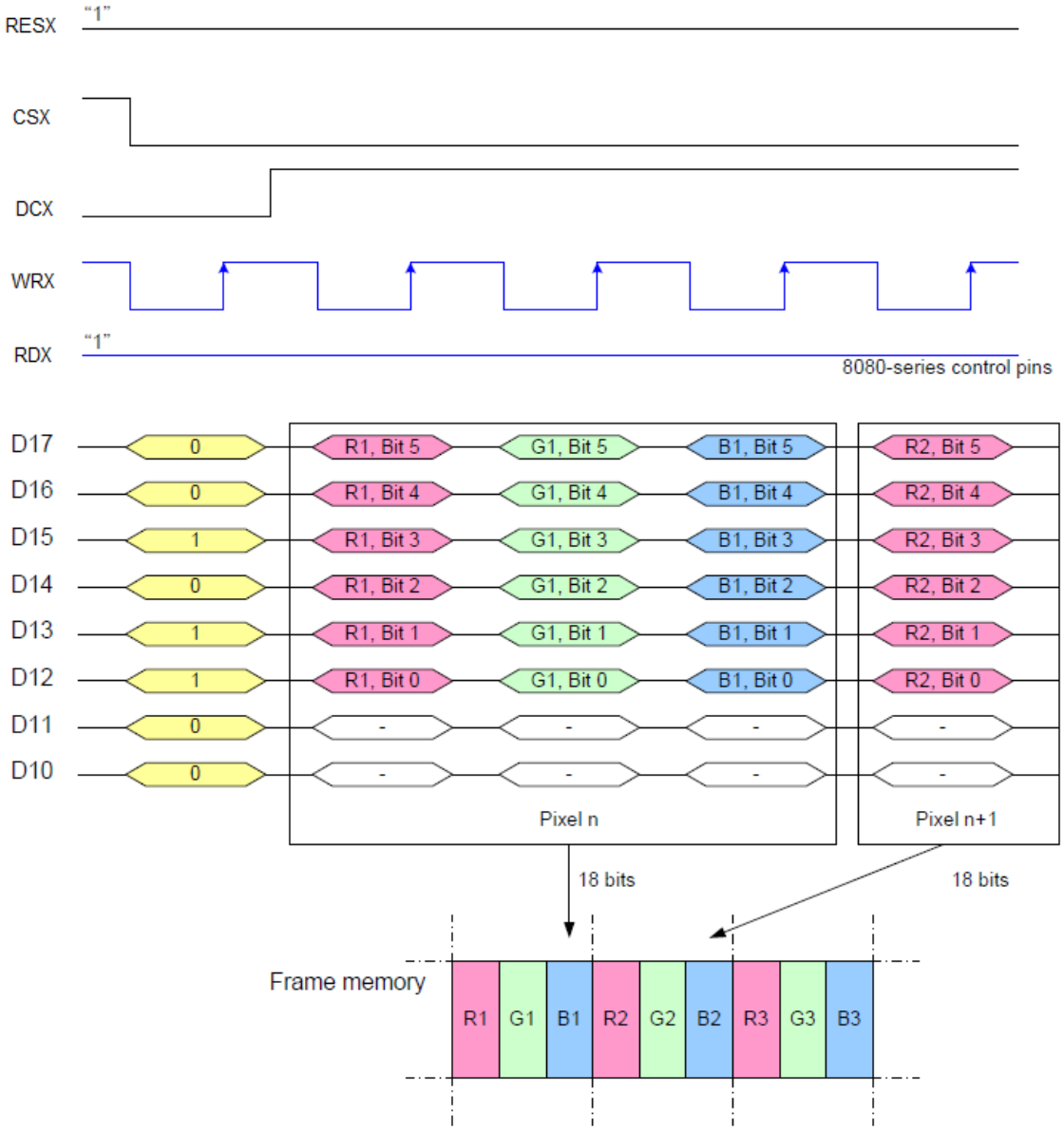
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.3.4.2.1 16-bit/pixel



Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
Note 2: 2-times transfer transmit 1 pixel data with the 16-bit color depth information.
Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.2.2 18-bit/pixel



Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

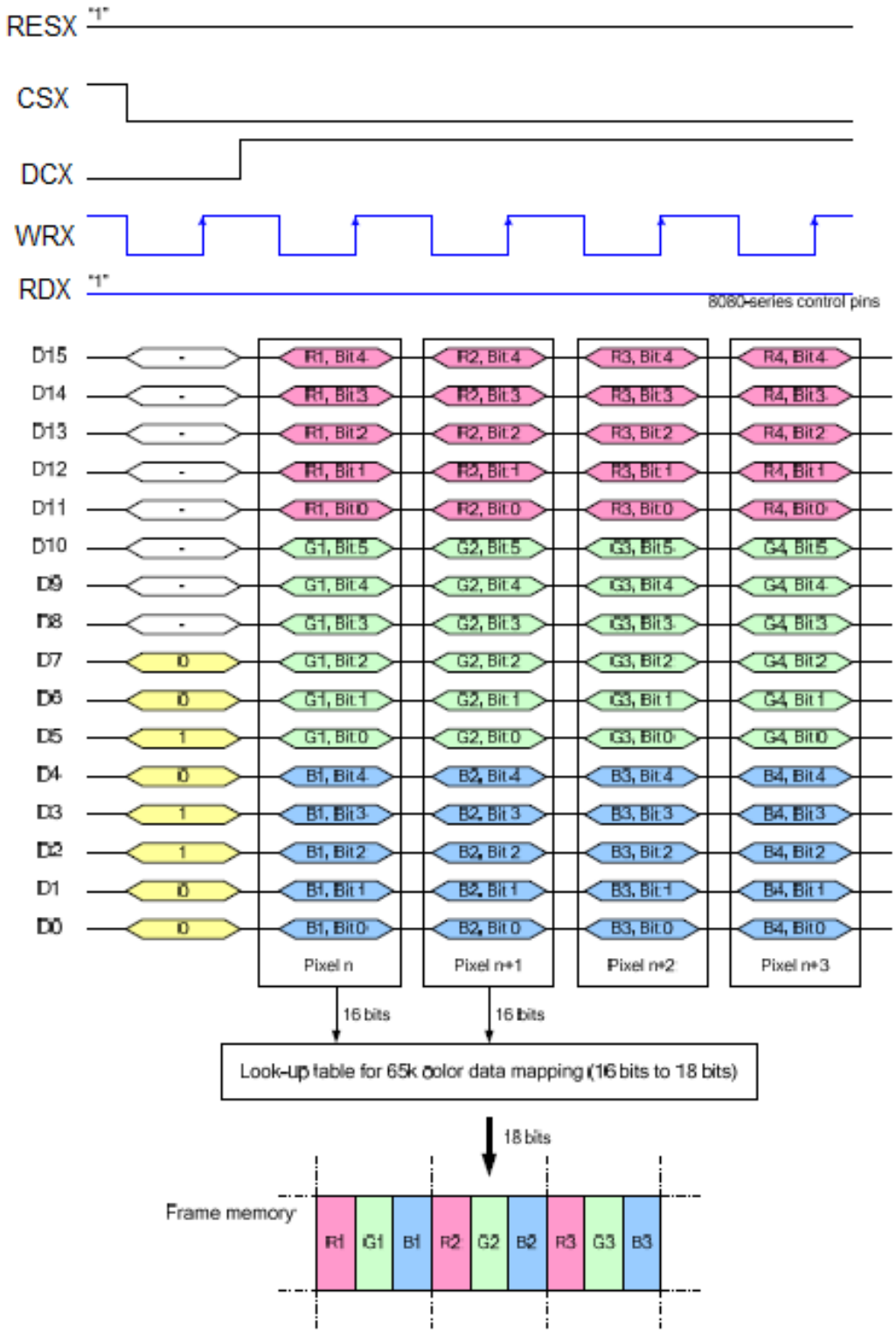
8.3.4.3 8080- Ⅰ series 16-Bit Parallel Interface

The 8080- Ⅰ series 16-bit parallel interface of NV3029S can be used by setting IM[3:0]="0001b". Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.3.1 16-bit/pixel

There is 1 pixel (3 sub-pixels) per 1 byte



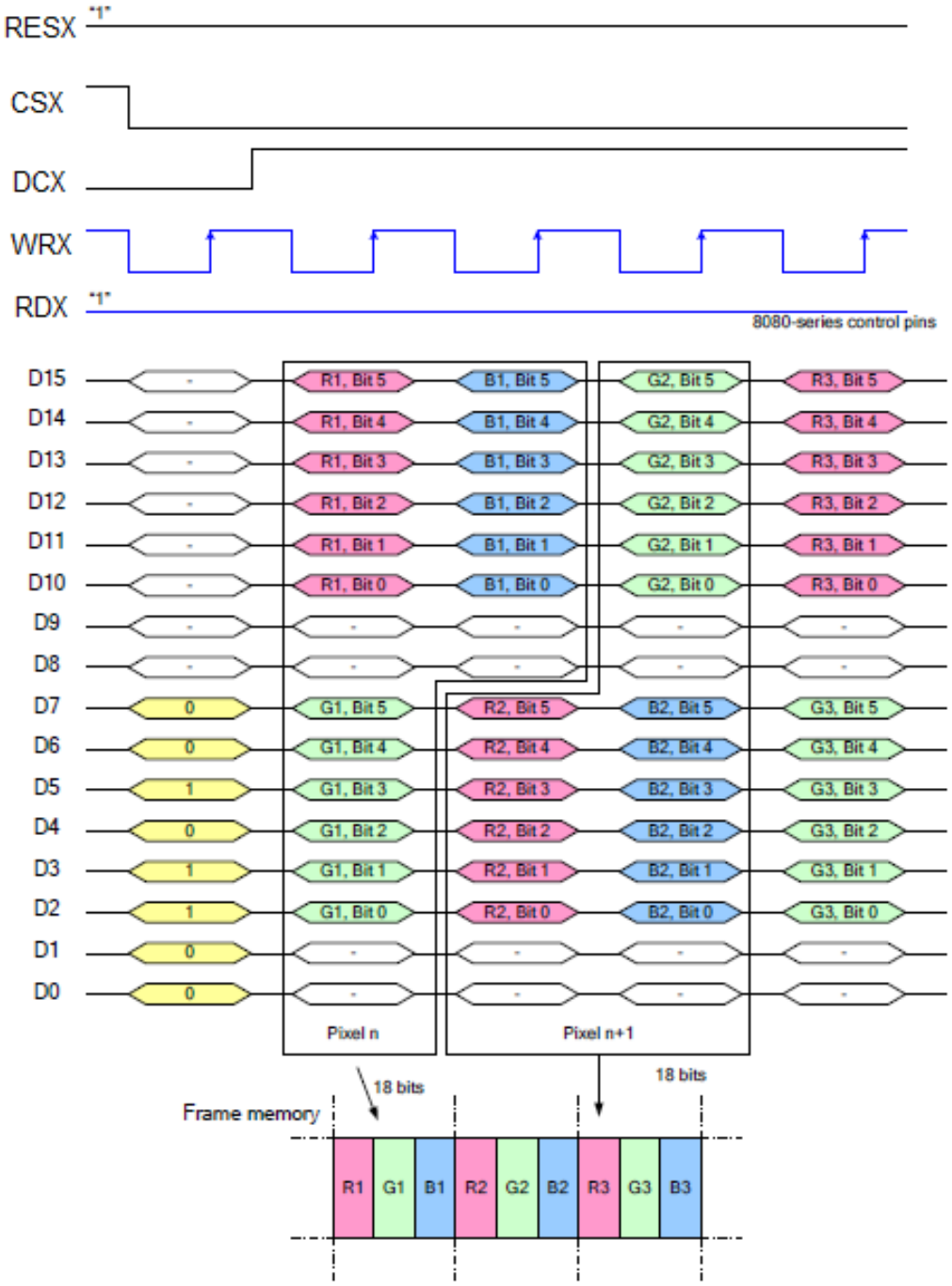
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1' .

8.3.4.3.2 18-bit/pixel(MDT[1:0]=”00b”)

There are 2 pixels (6 sub-pixels) per 3 bytes

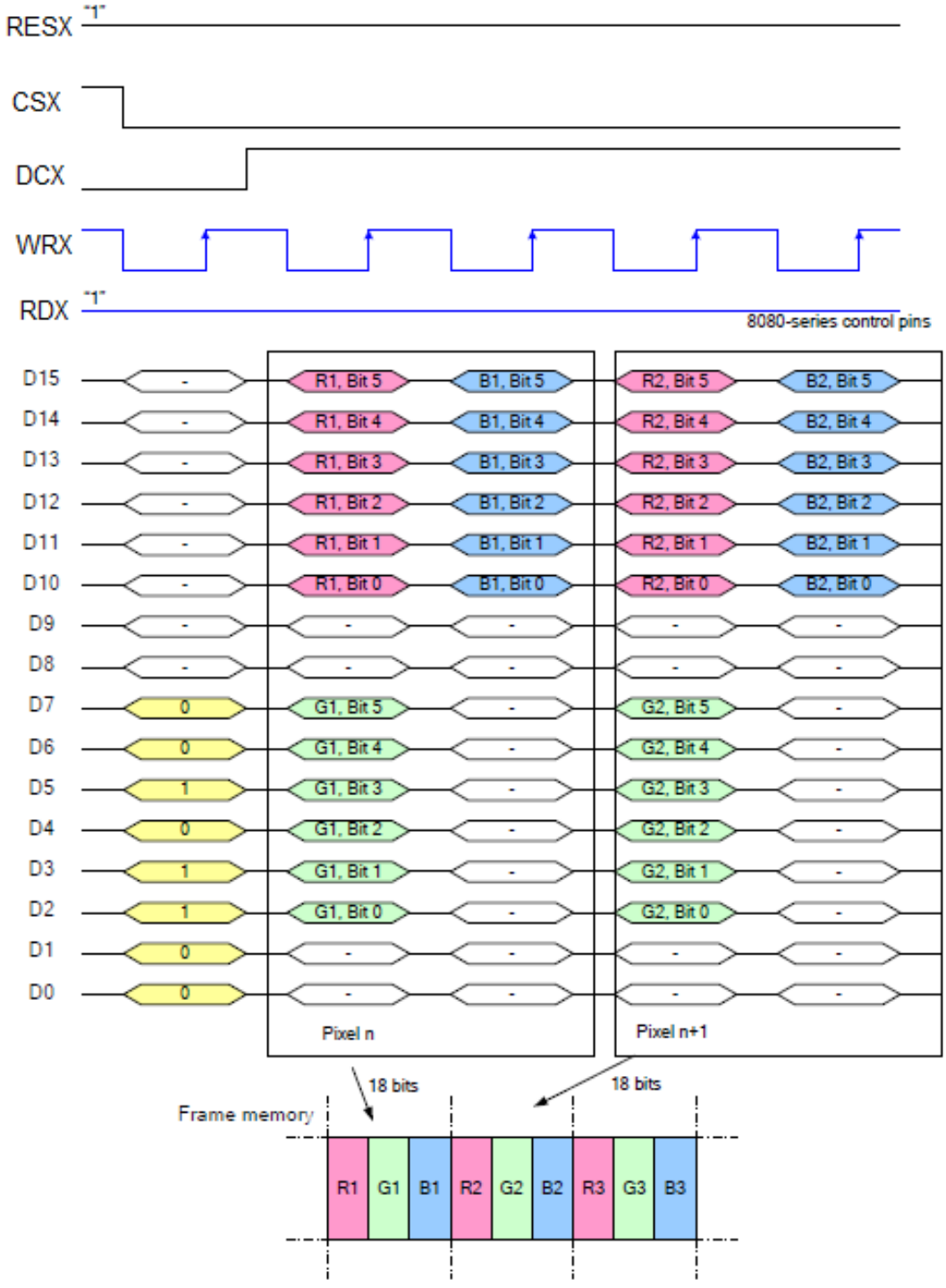


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.3 18-bit/pixel(MDT[1:0]=”01b”)

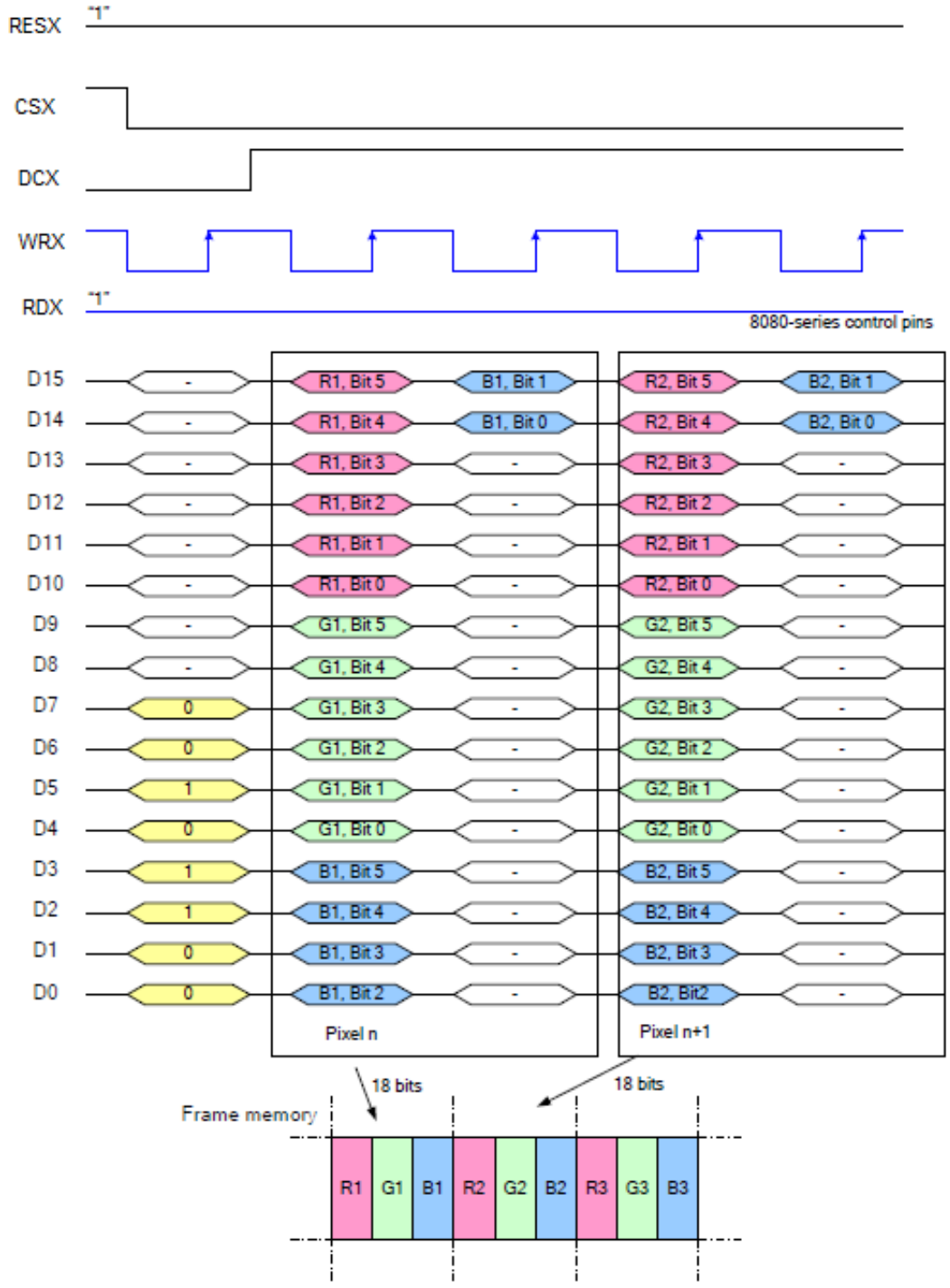


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’= Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.4 18-bit/pixel(MDT[1:0]=”10b”)

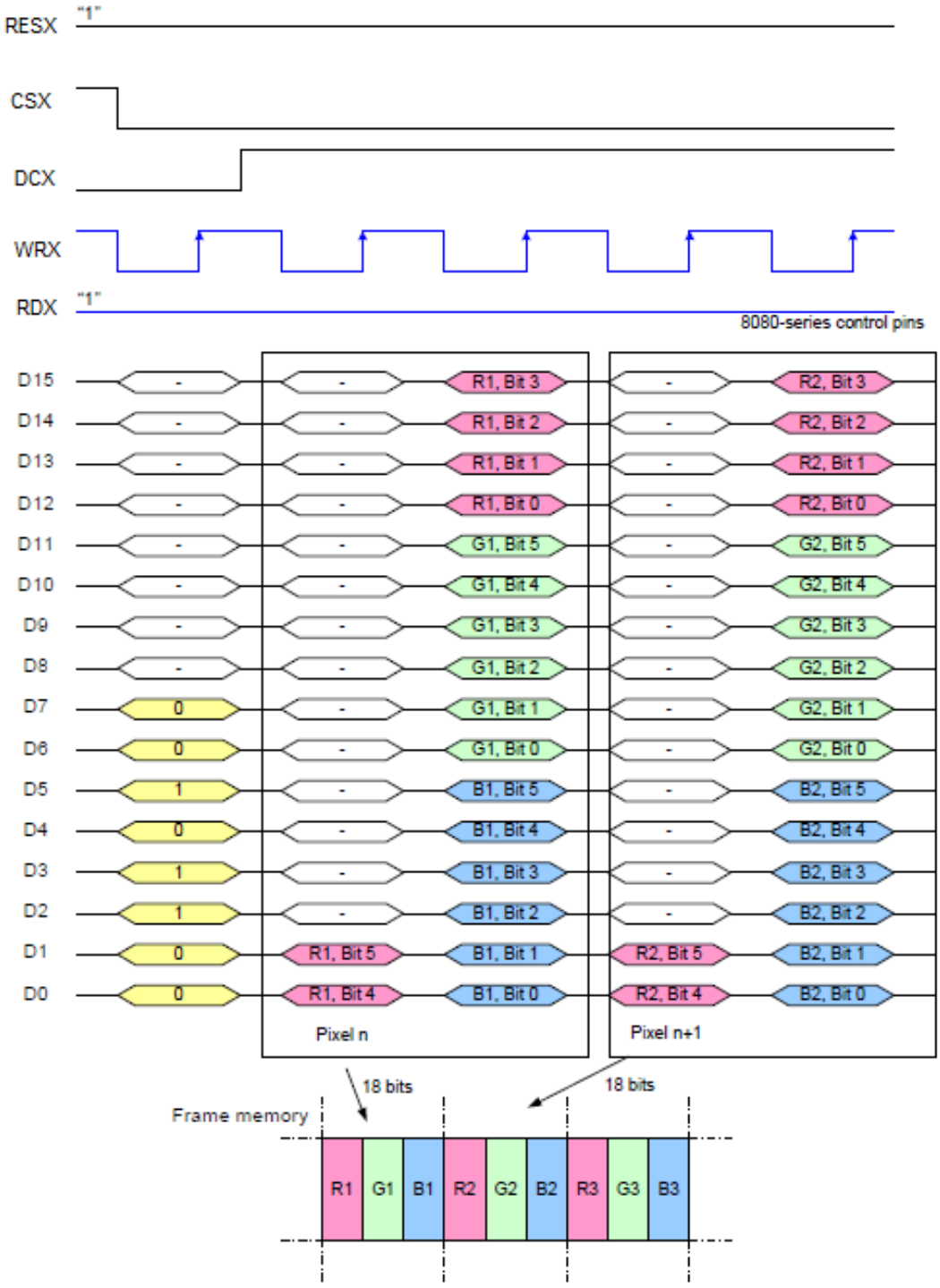


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.5 18-bit/pixel (MDT[1:0]=”11b”)



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

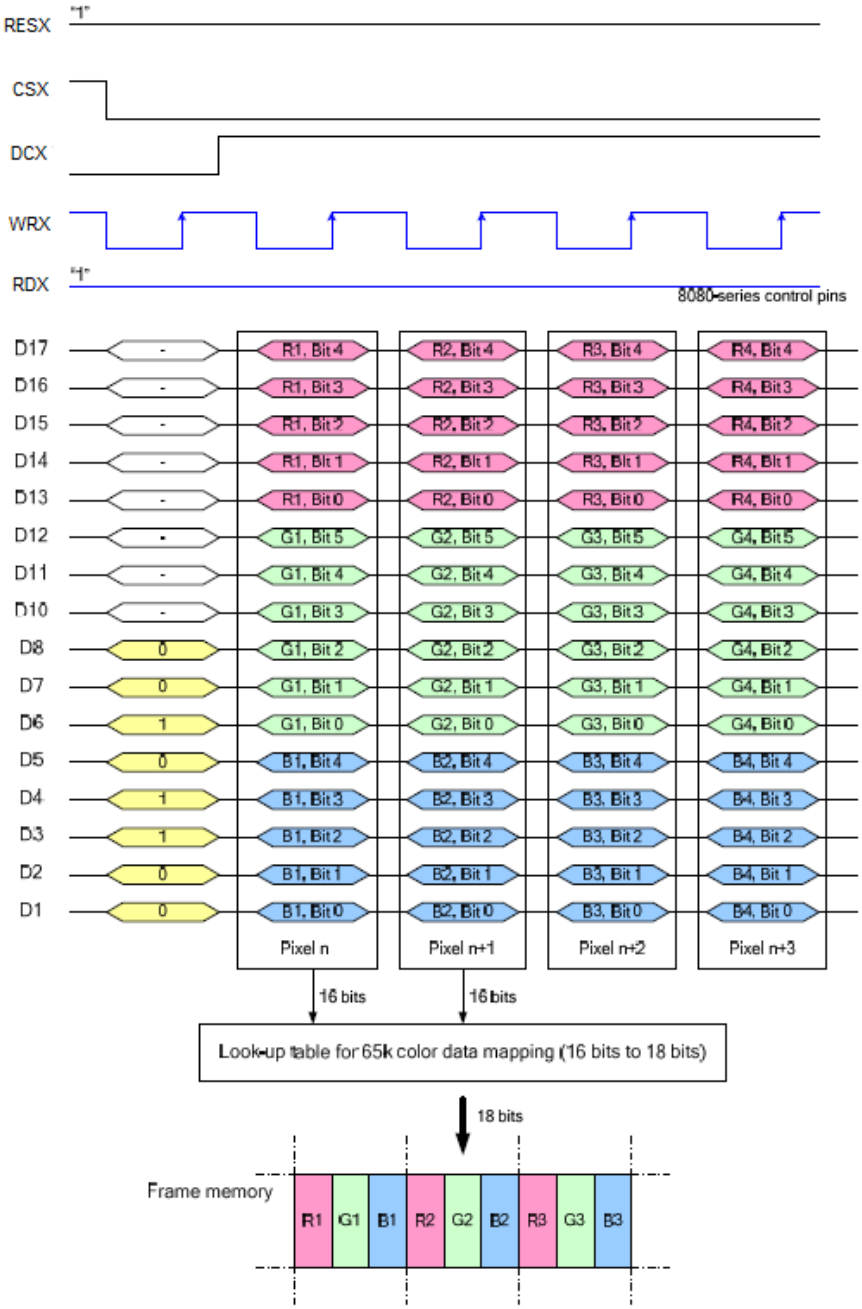
8.3.4.4 8080-Ⅱ series 16-Bit Parallel Interface

The 8080-Ⅱ series 16-bit parallel interface of NV3029S can be used by setting IM[3:0]=”1000b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.4.1 16-bit/pixel

There is 1 pixel (3 sub-pixels) per 1 byte



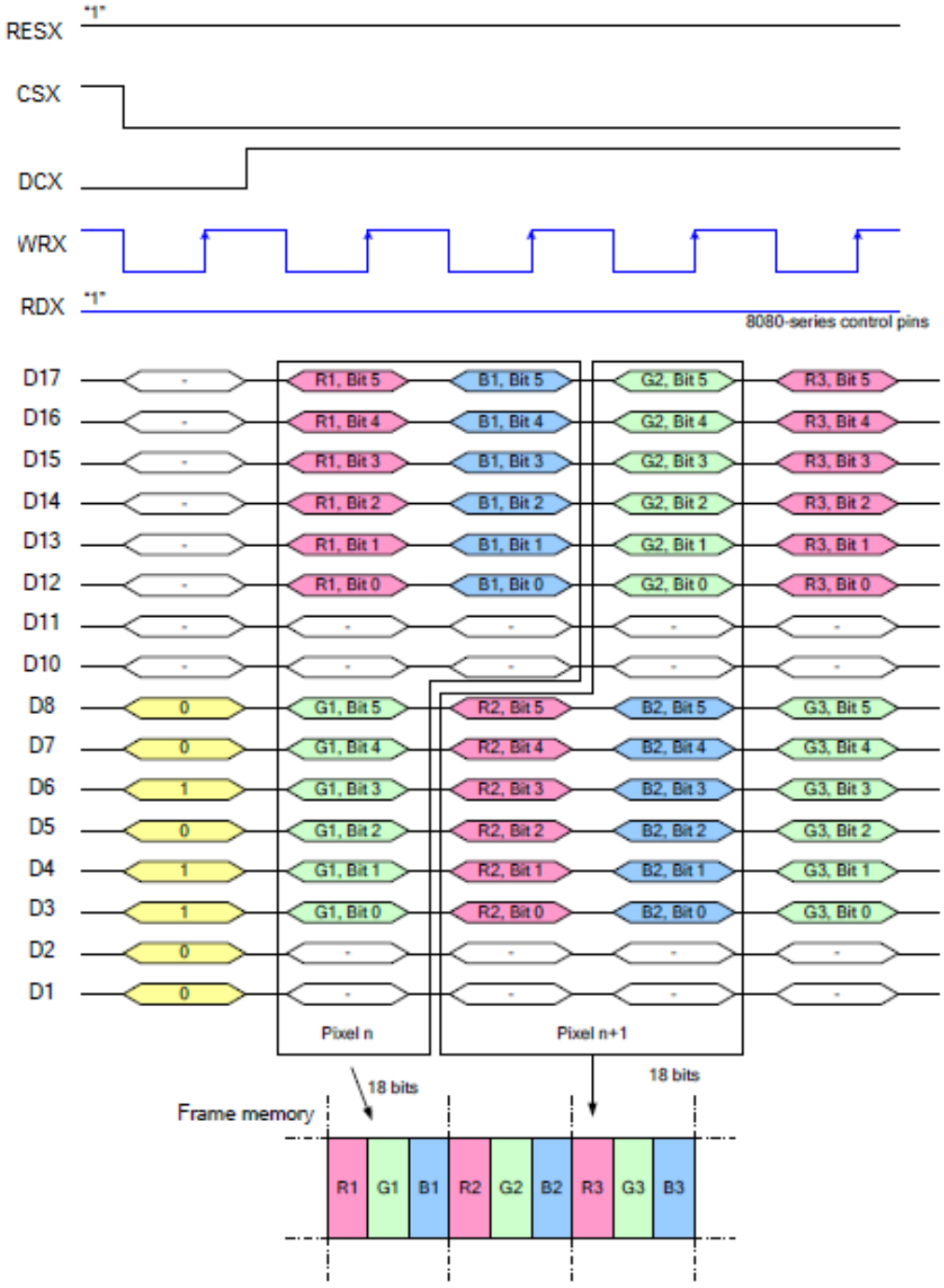
Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D17~D10, D8~D1) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’= Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.2 18-bit/pixel(MDT[1:0]=”00b”)

There are 2 pixels (6 sub-pixels) per 3 bytes

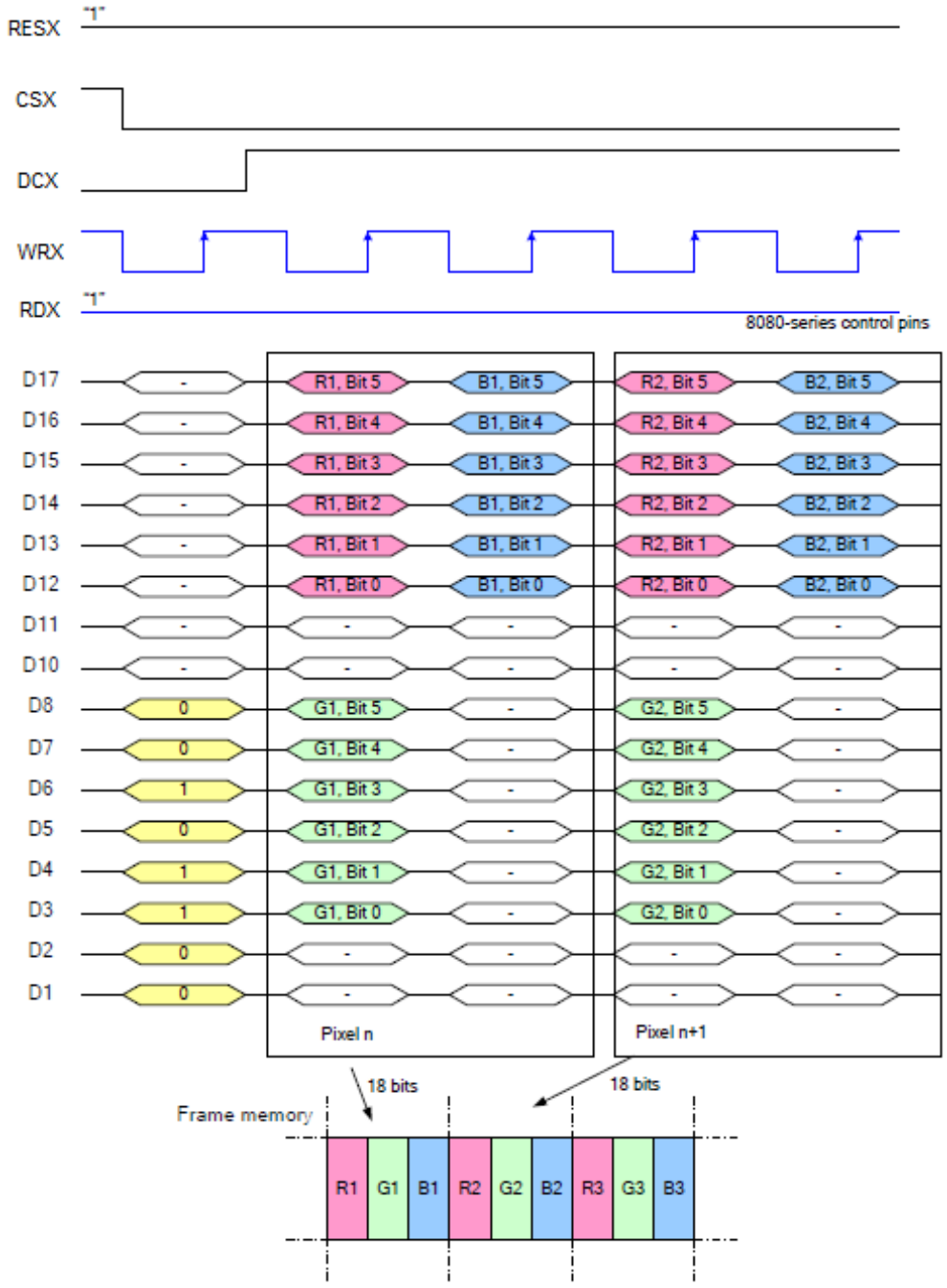


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.3 18-bit/pixel(MDT[1:0]=”01b”)

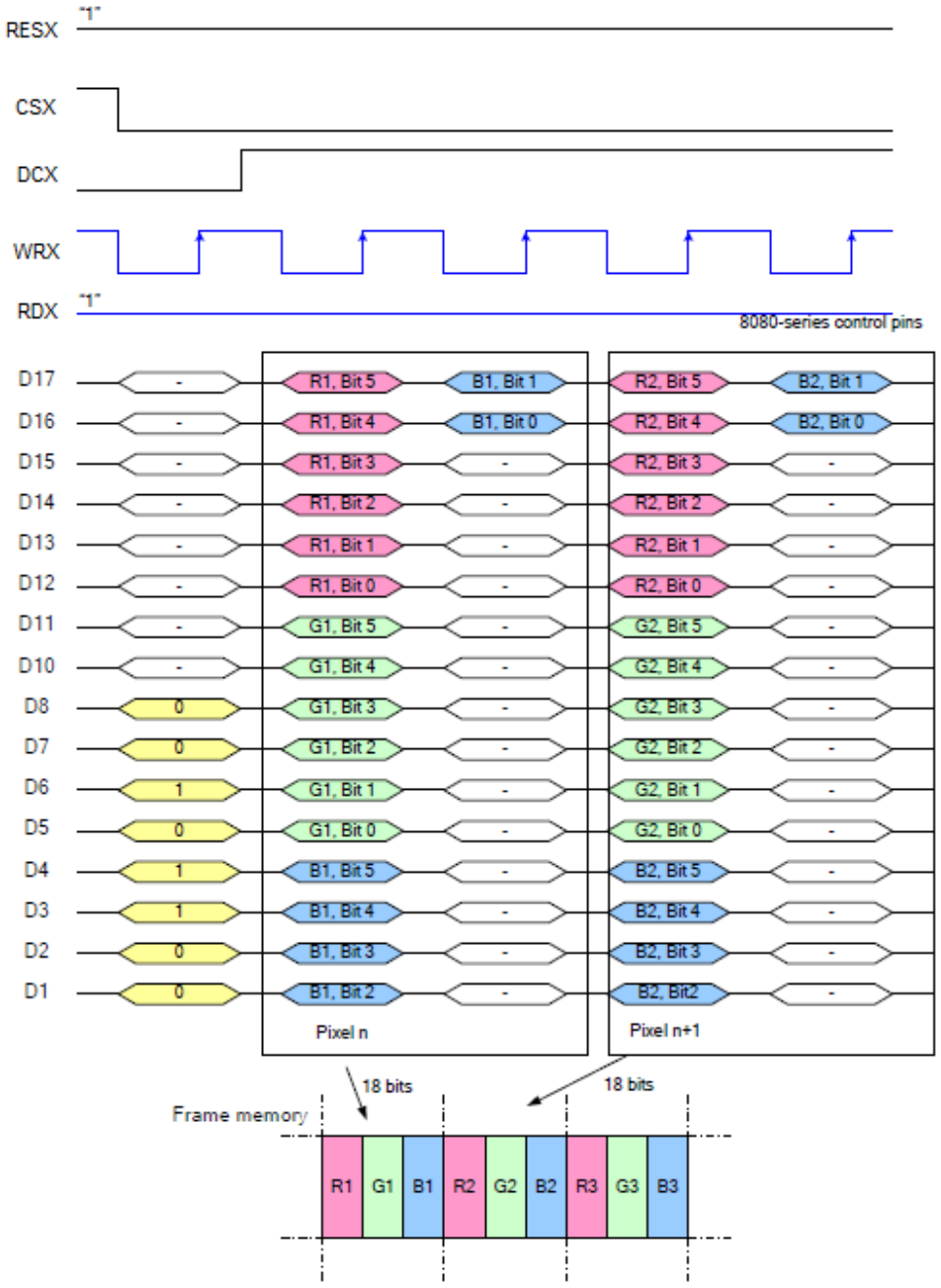


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.4 18-bit/pixel(MDT[1:0]=”10b”)

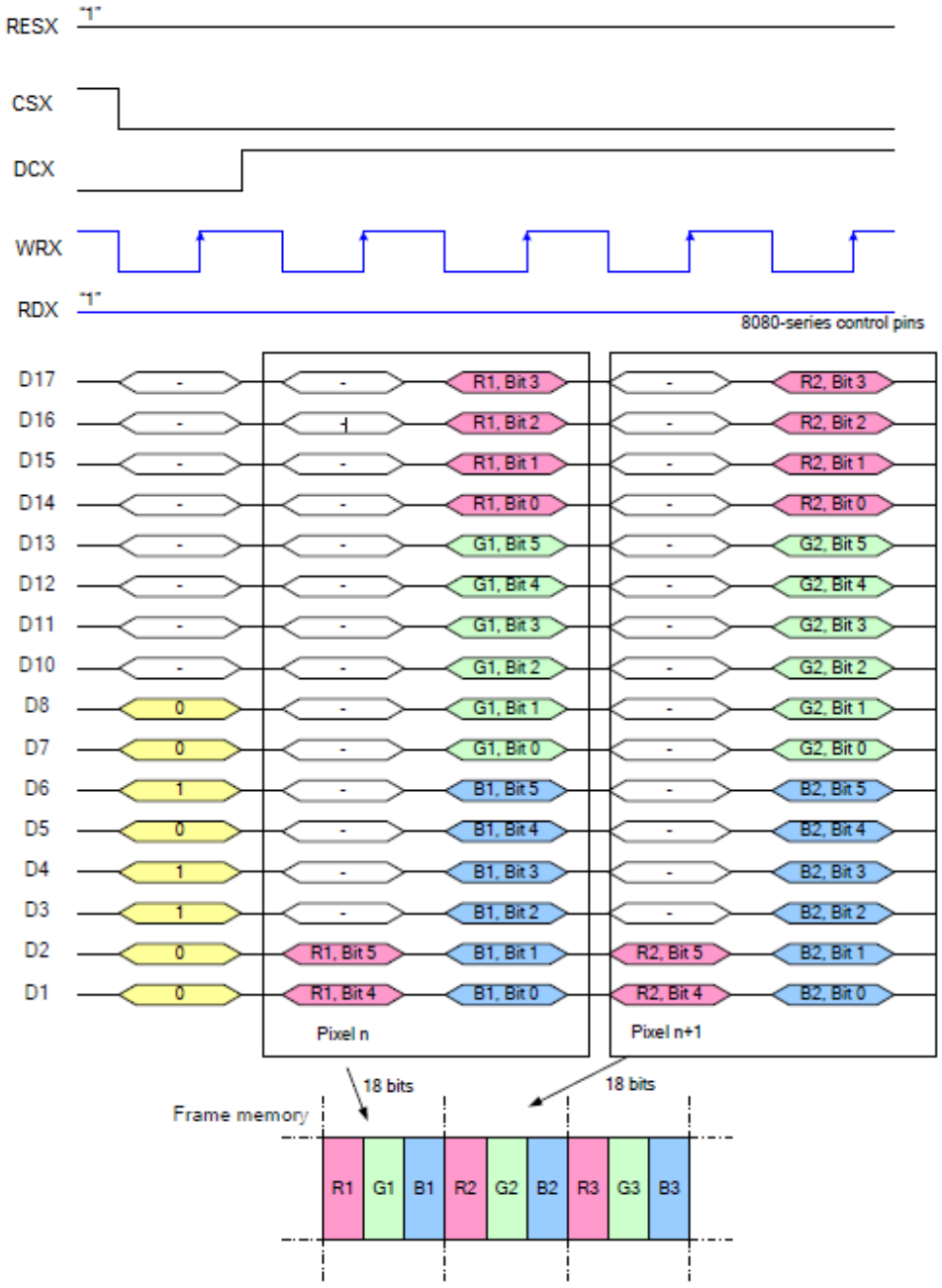


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.5 18-bit/pixel(MDT[1:0]=”11b”)



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

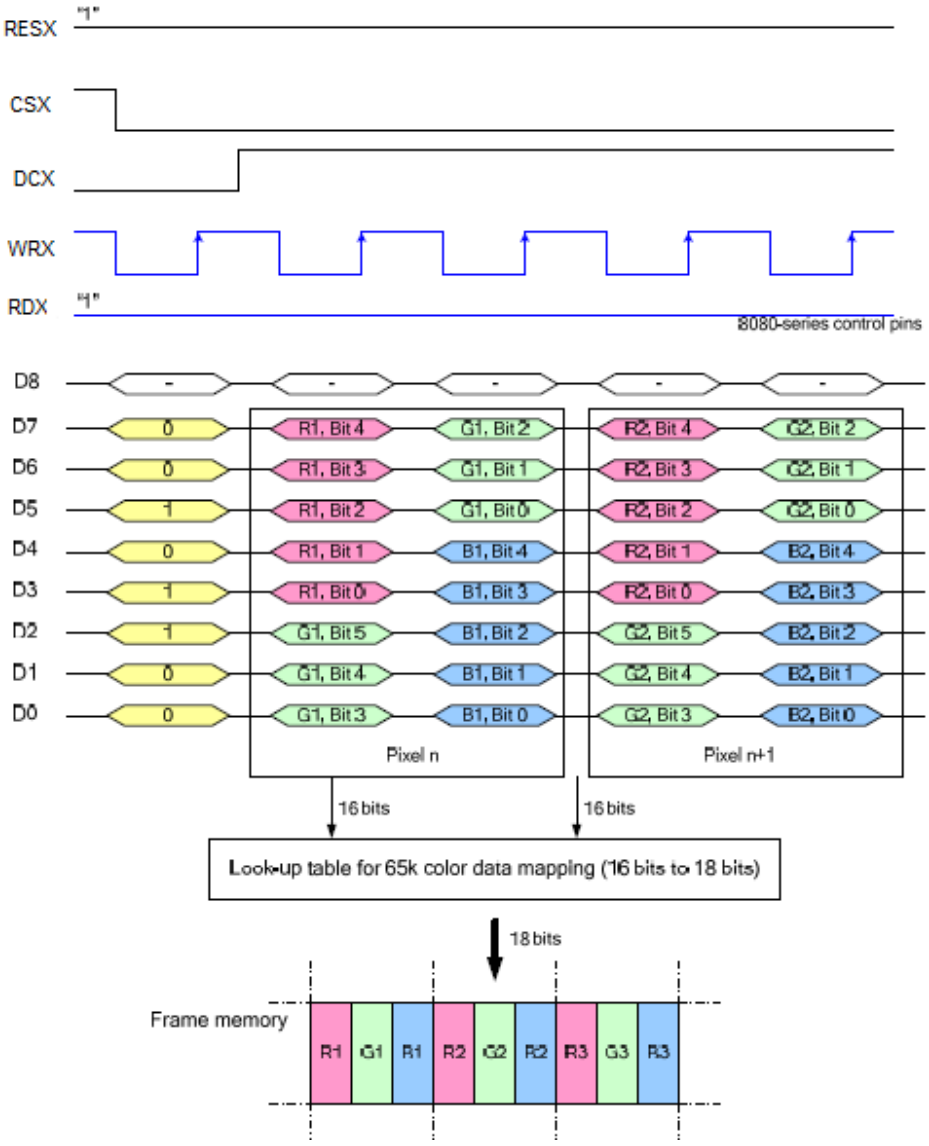
8.3.4.5 8080-Ⅰ series 9-Bit Parallel Interface

The 8080-Ⅰ series 9-bit parallel interface of NV3029S can be used by setting IM[3:0]=”0010b” Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.3.4.5.1 16-bit/pixel



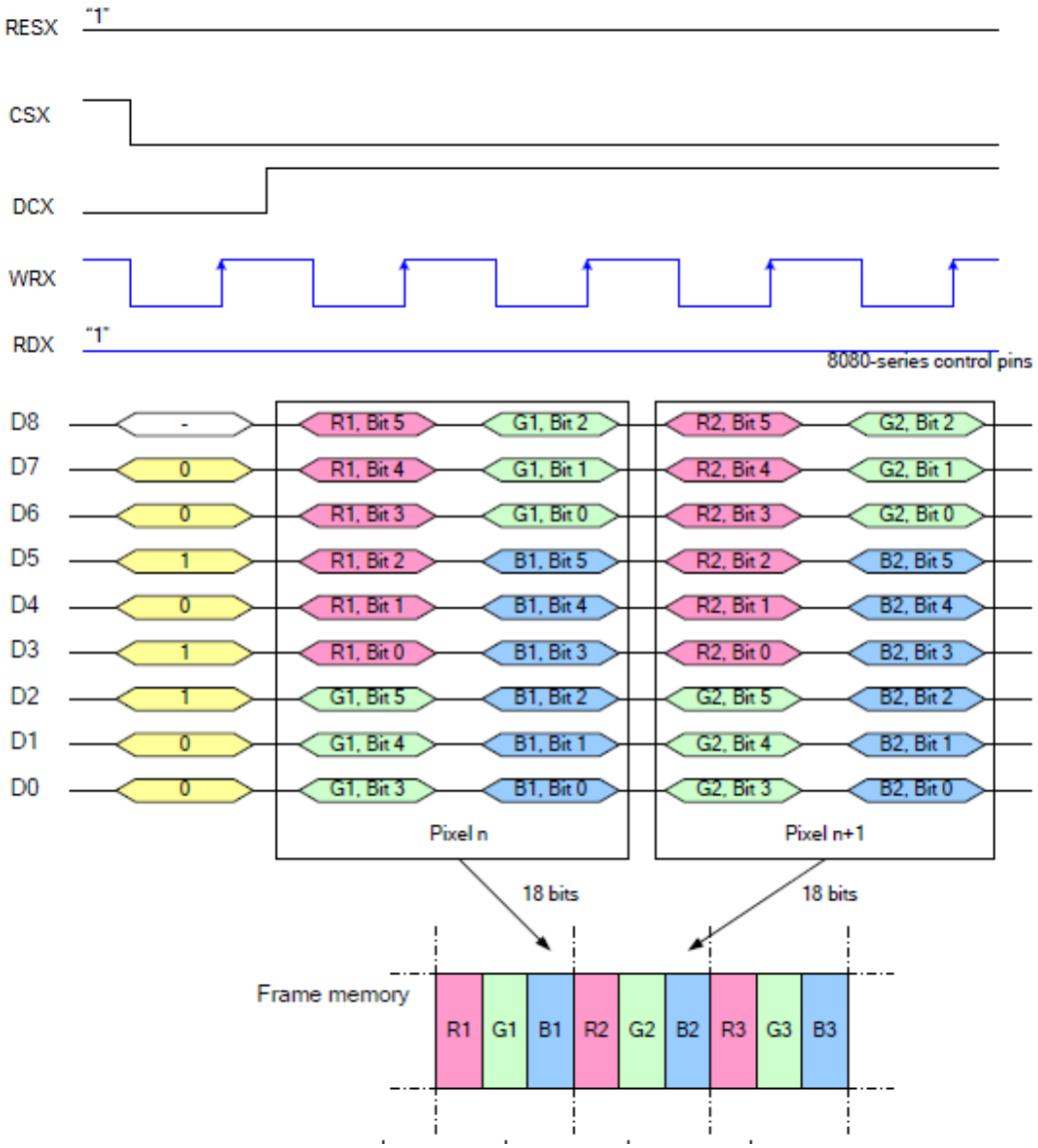
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.5.2 18-bit/pixel(MDT[1:0]=”00b”)

There is 1 pixel (3 sub-pixels) per 2bytes

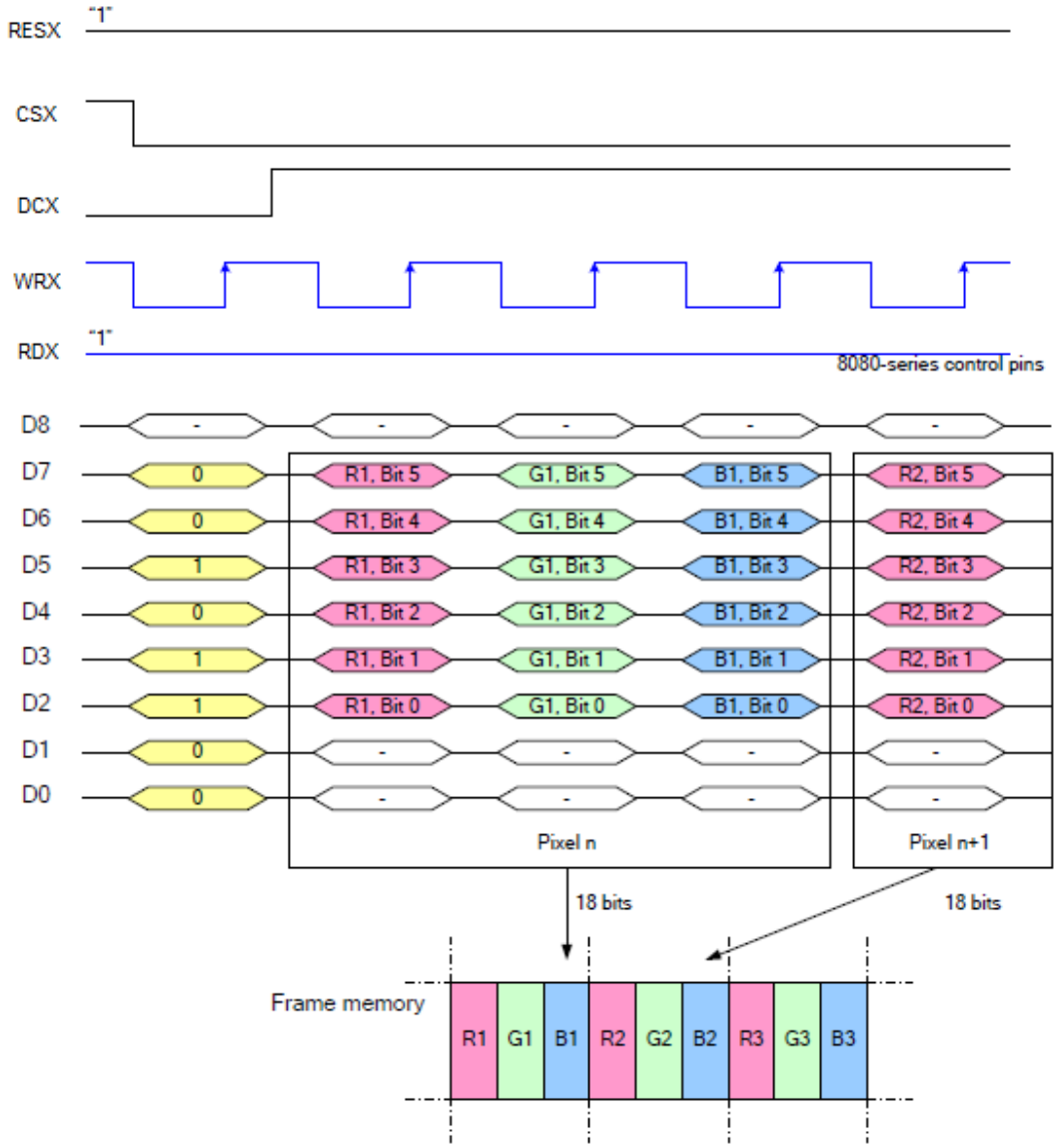


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Greenand Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.5.3 18-bit/pixel(MDT[1:0]=”01b”)



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

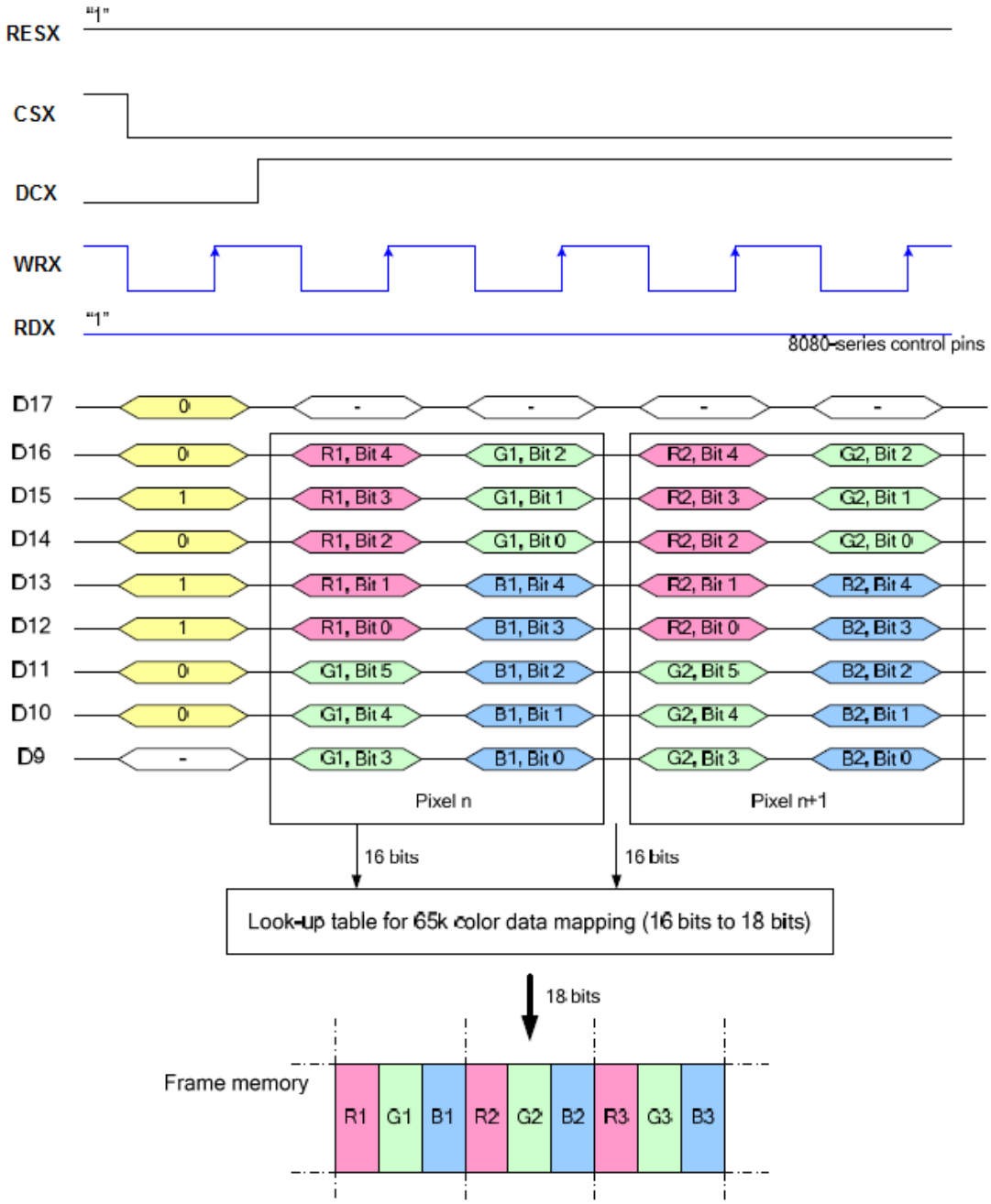
8.3.4.6 8080-Ⅱ series 9-bit Parallel Interface

The 8080-Ⅱ series 9-bit parallel interface of NV3029S can be used by setting IM[3:0]=”1011b”Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.3.4.6.1 16-bit/pixel



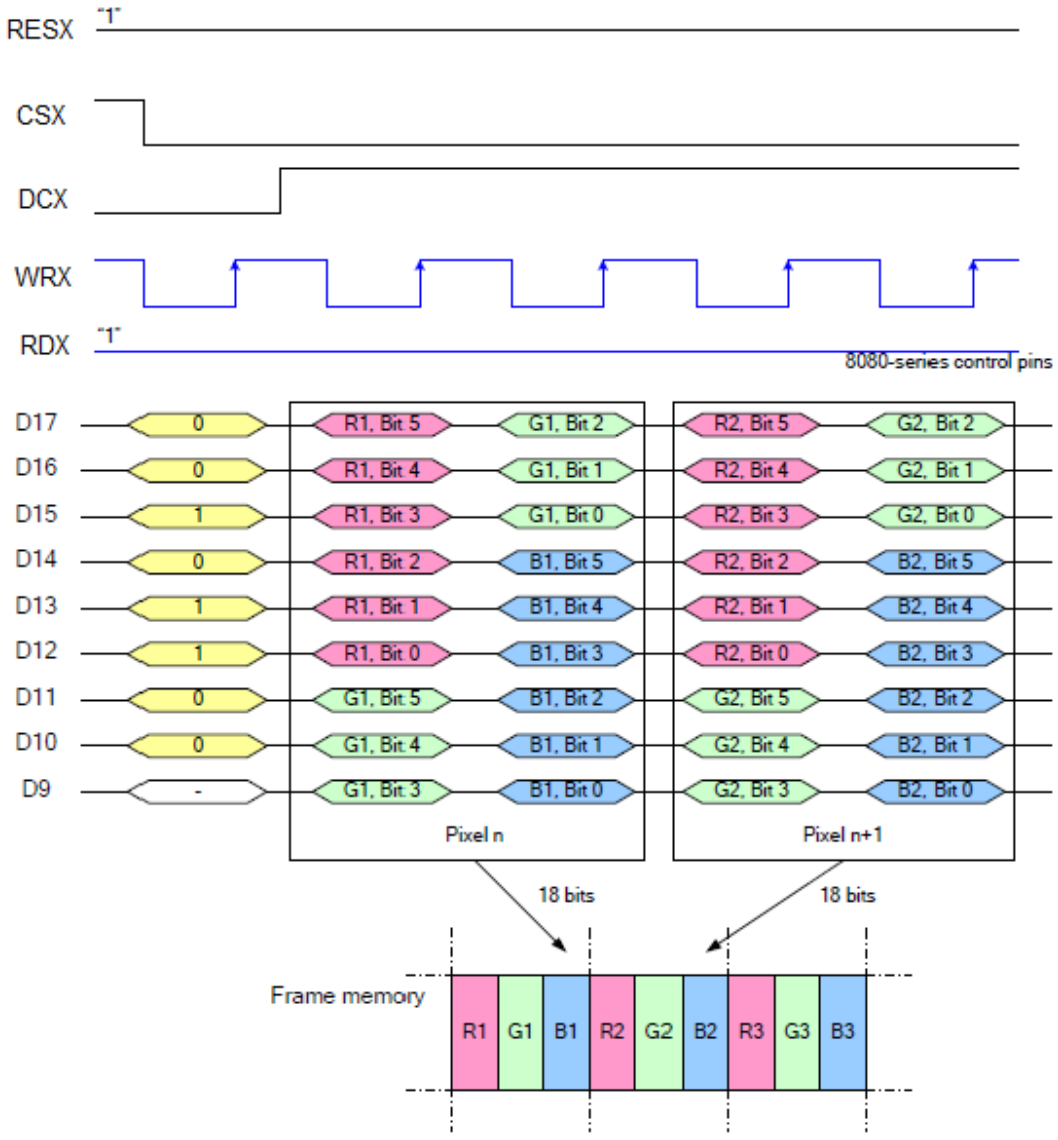
Note 1: The data order is as follows, MSB=D16, LSB=D9 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.6.2 18-bit/pixel(MDT[1:0]=”00b”)

There is 1 pixel (3 sub-pixels) per 2bytes

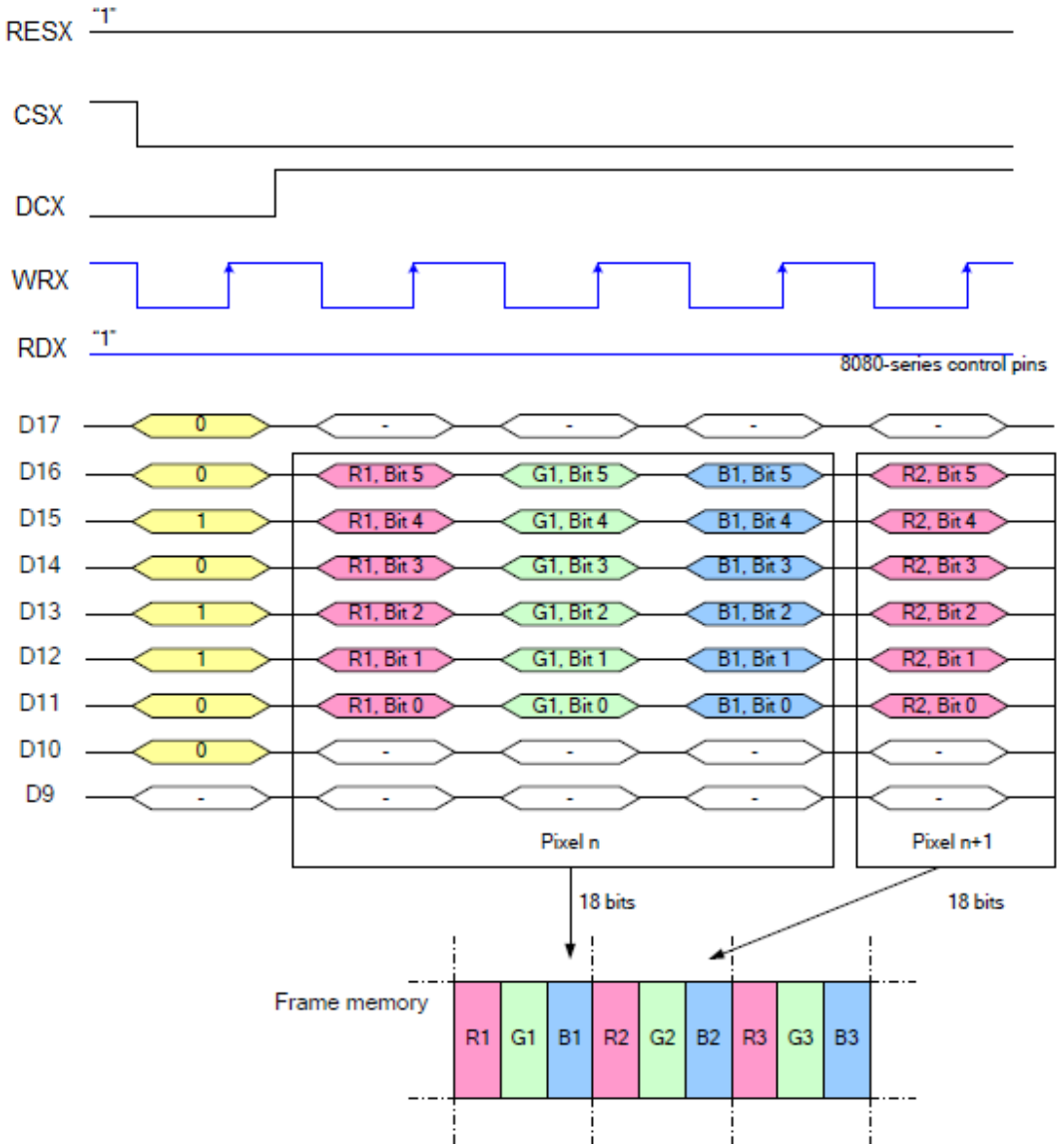


Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Red,Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.6.3 18-bit/pixel(MDT[1:0]=”01b”)



Note 1: The data order is as follows, MSB=D16, LSB=D11 and picture data is MSB=Bit 5, LSB=Bit 0 for Red,Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

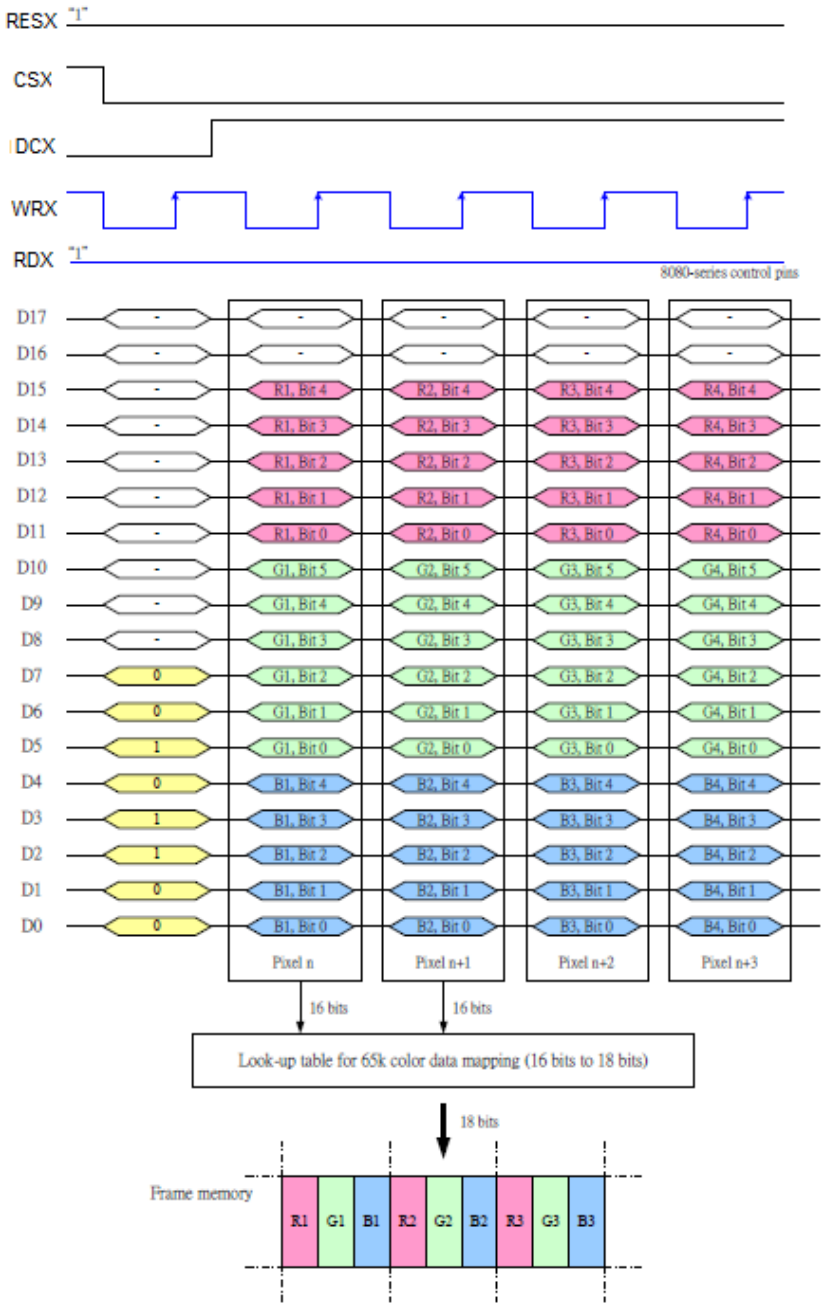
8.3.4.7 8080- Ⅰ series 18-Bit Parallel Interface

The 8080- Ⅰ series 18-bit parallel interface of NV3029S can be used by setting IM[3:0]=”0011b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.7.1 16-bit/pixel

There is one pixel (3 sub-pixels) per byte

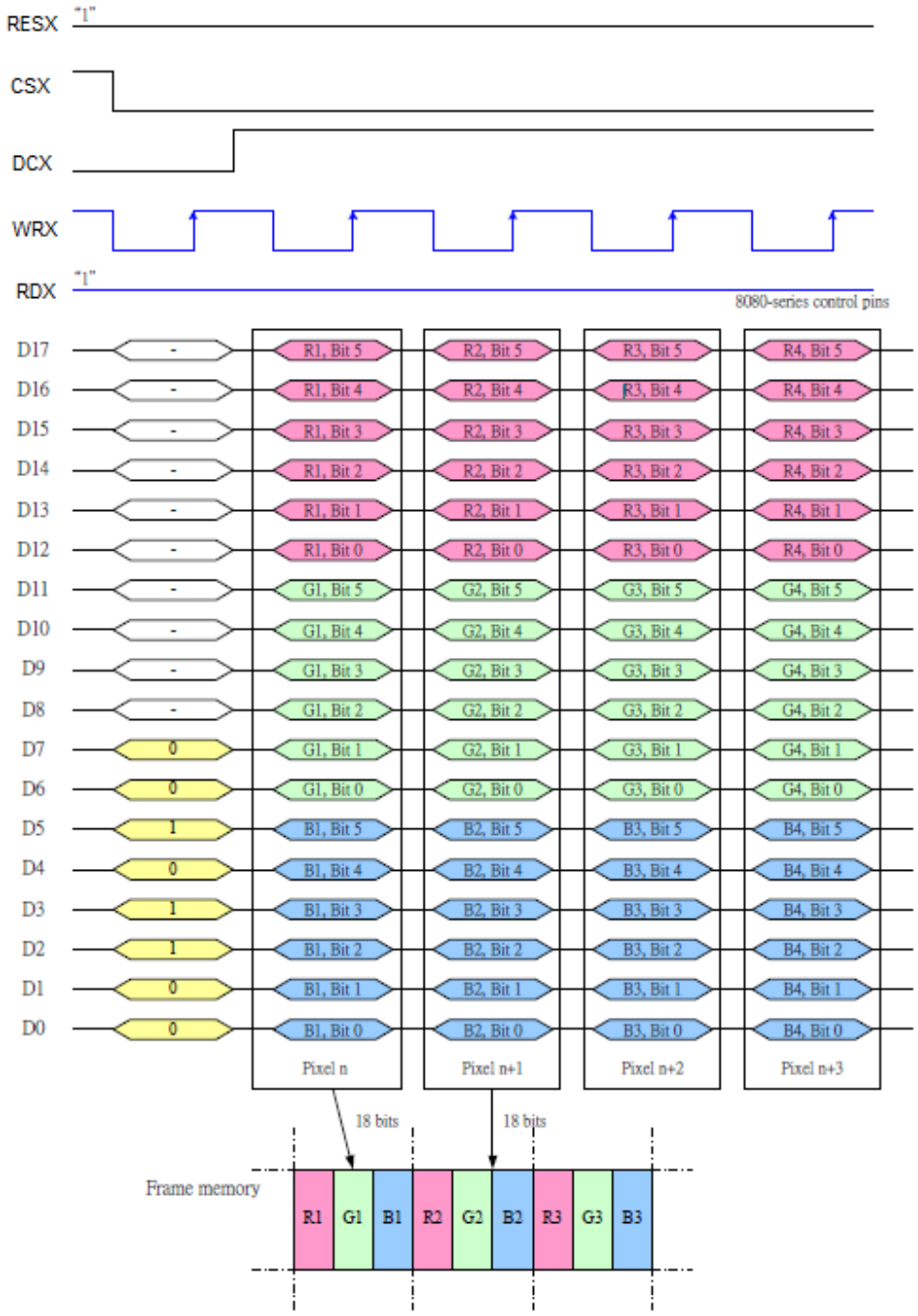


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

8.3.4.7.2 18-bit/pixel

There is 1 pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read,Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

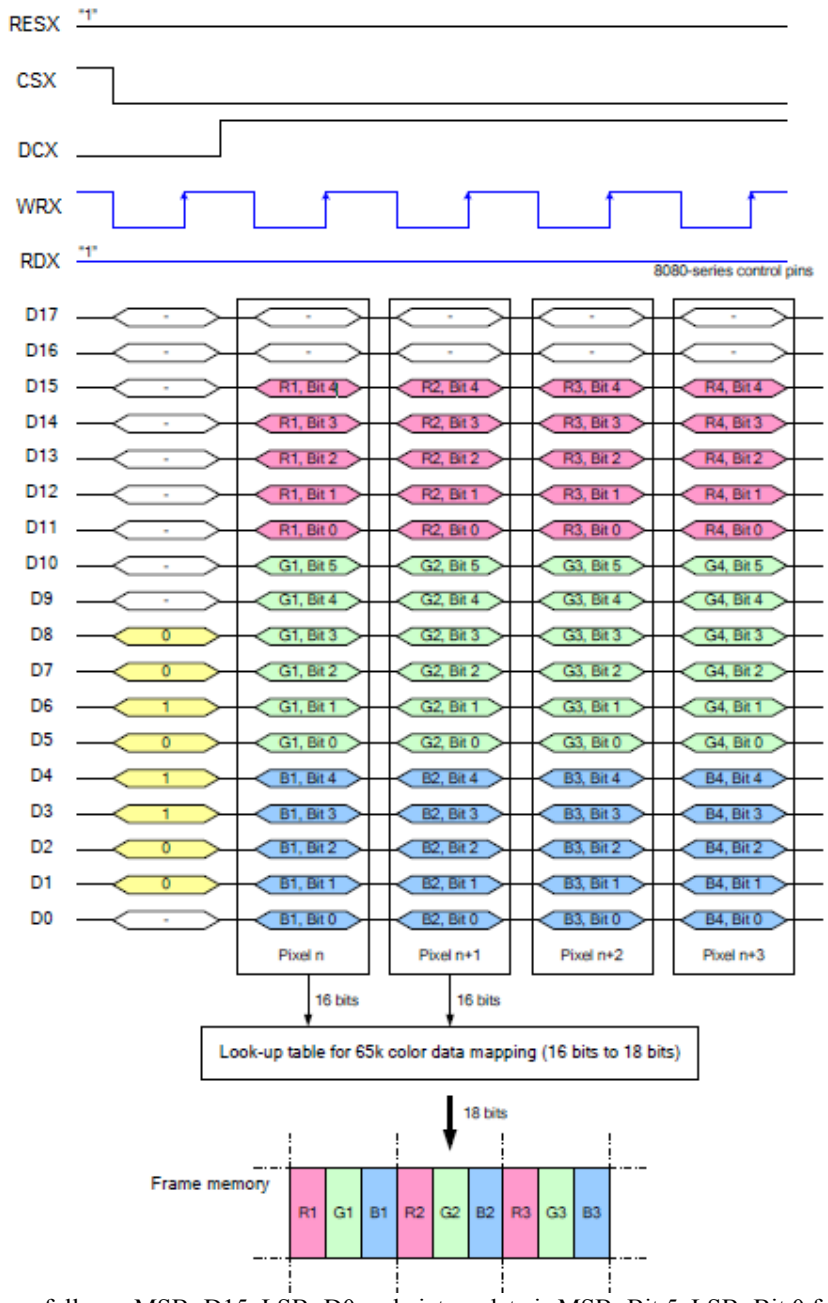
8.3.4.8 8080- Ⅱ series 18-Bit Parallel Interface

The 8080- Ⅱ series 18-bit parallel interface of NV3029S can be used by setting IM[3:0]=”1010b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

8.3.4.8.1 16-bit/pixel

There is one pixel (3 sub-pixels) per byte

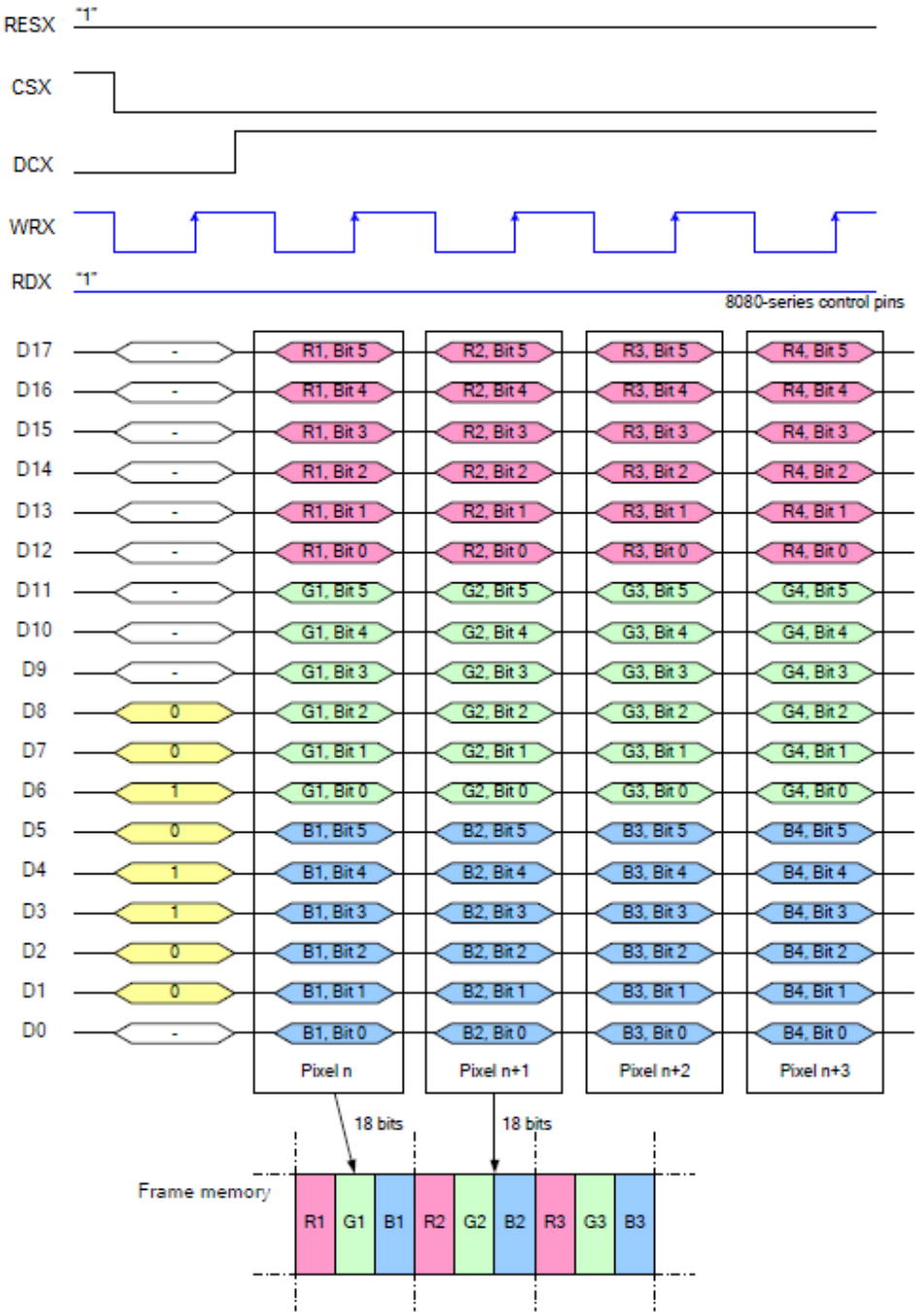


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green,and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

8.3.4.8.2 18-bit/pixel

There is 1 pixel (3 sub-pixels) per byte

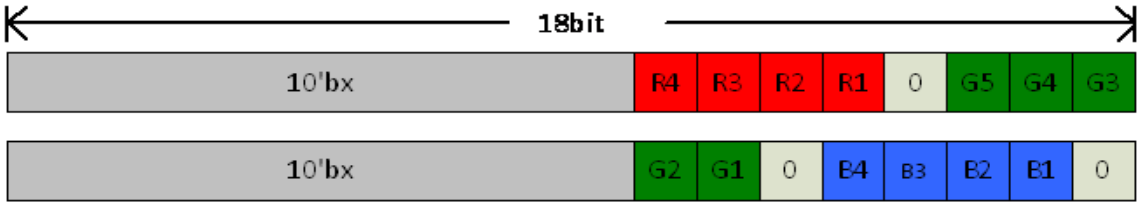


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

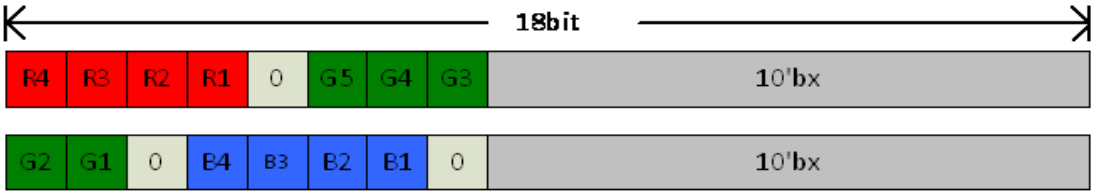
Note 2: 1-times transfer (D17 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.

8.3.4.9 Read Memory Data Color Coding

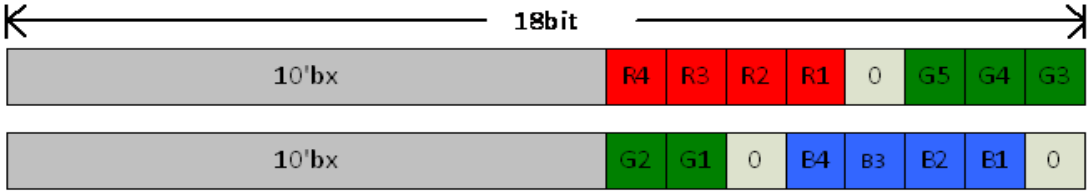
8.3.4.9.1 8 Data Line Parallel Interface I



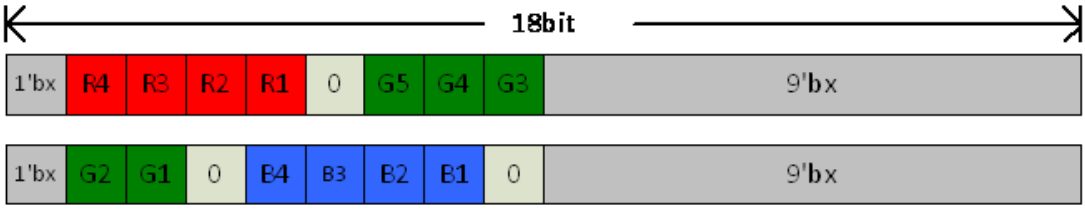
8 Data Line Parallel Interface II



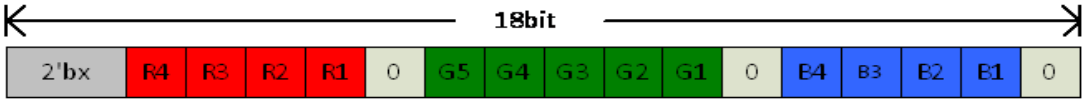
8.3.4.9.2 9 Data Line Parallel Interface I



9 Data Line Parallel Interface II

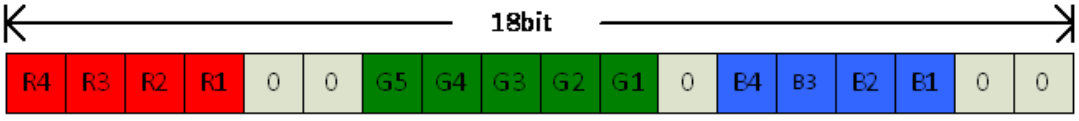


8.3.4.9.3 16 Data Line Parallel Interface I



16 Data Line Parallel Interface II

8.3.4.9.4 18 Data Line Parallel Interface I & II

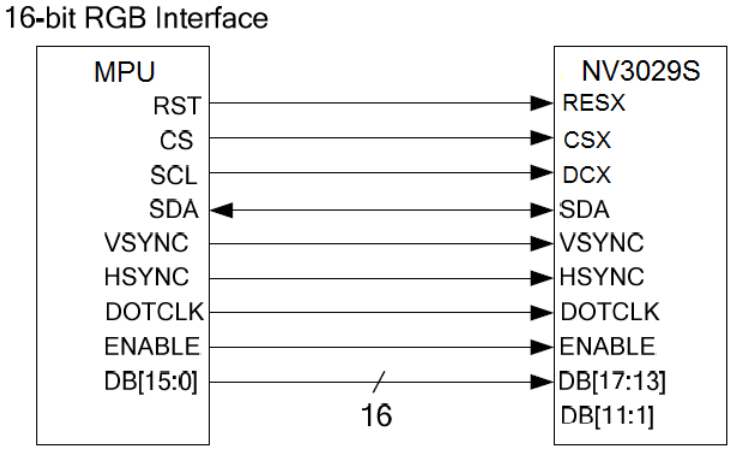


Note:‘bx’means these bits are not usable.

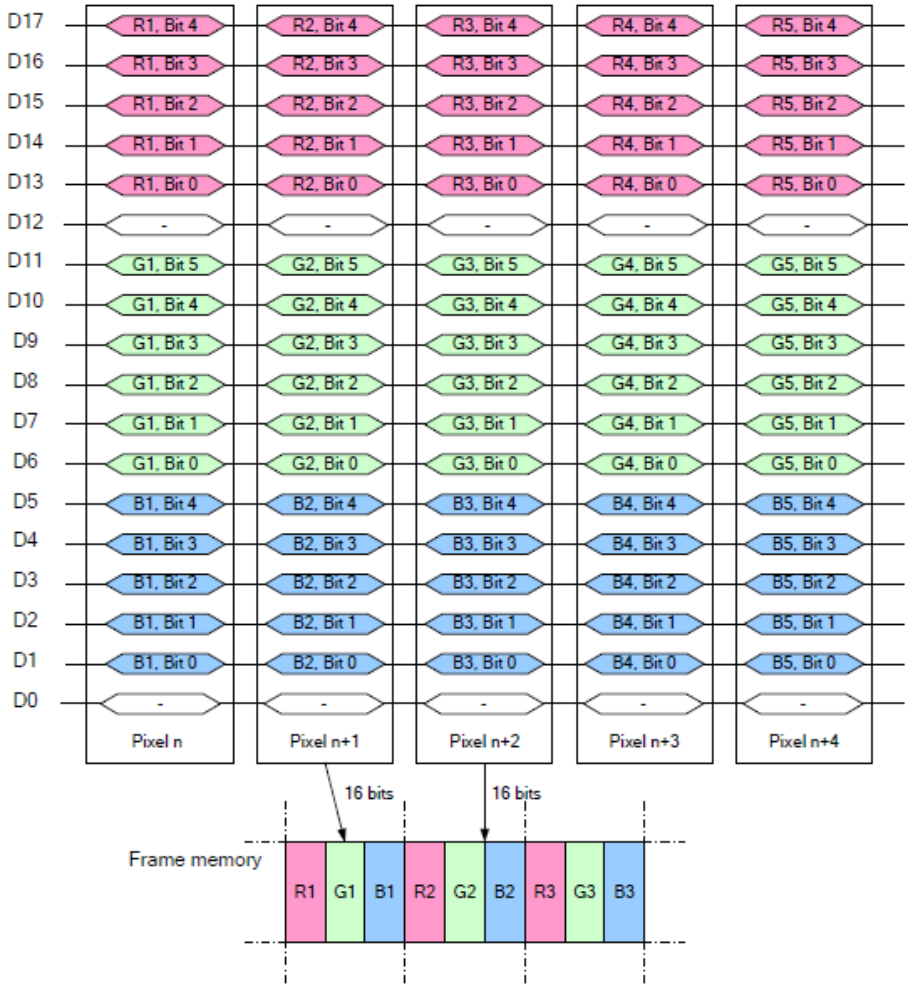
8.3.5 RGB Interface

NV3029S supports two kinds of RGB interface, DE mode and SYNC mode, and 16bit/18bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0] pins can be used; when SYNC mode is selected and the VSYNC, HSYNC, DOTCLK, DB[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

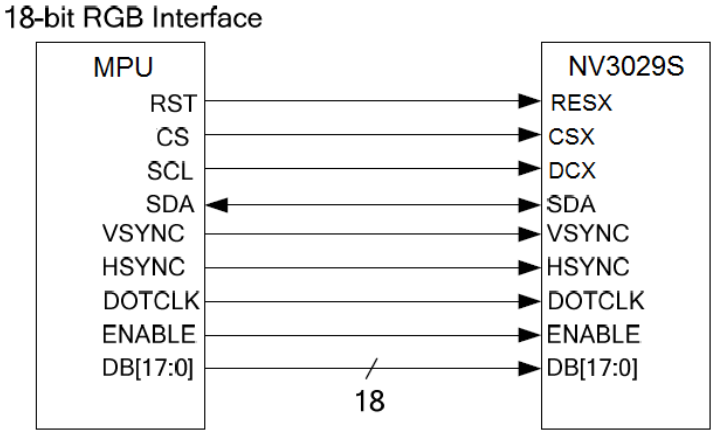
8.3.5.1 16-bit RGB interface



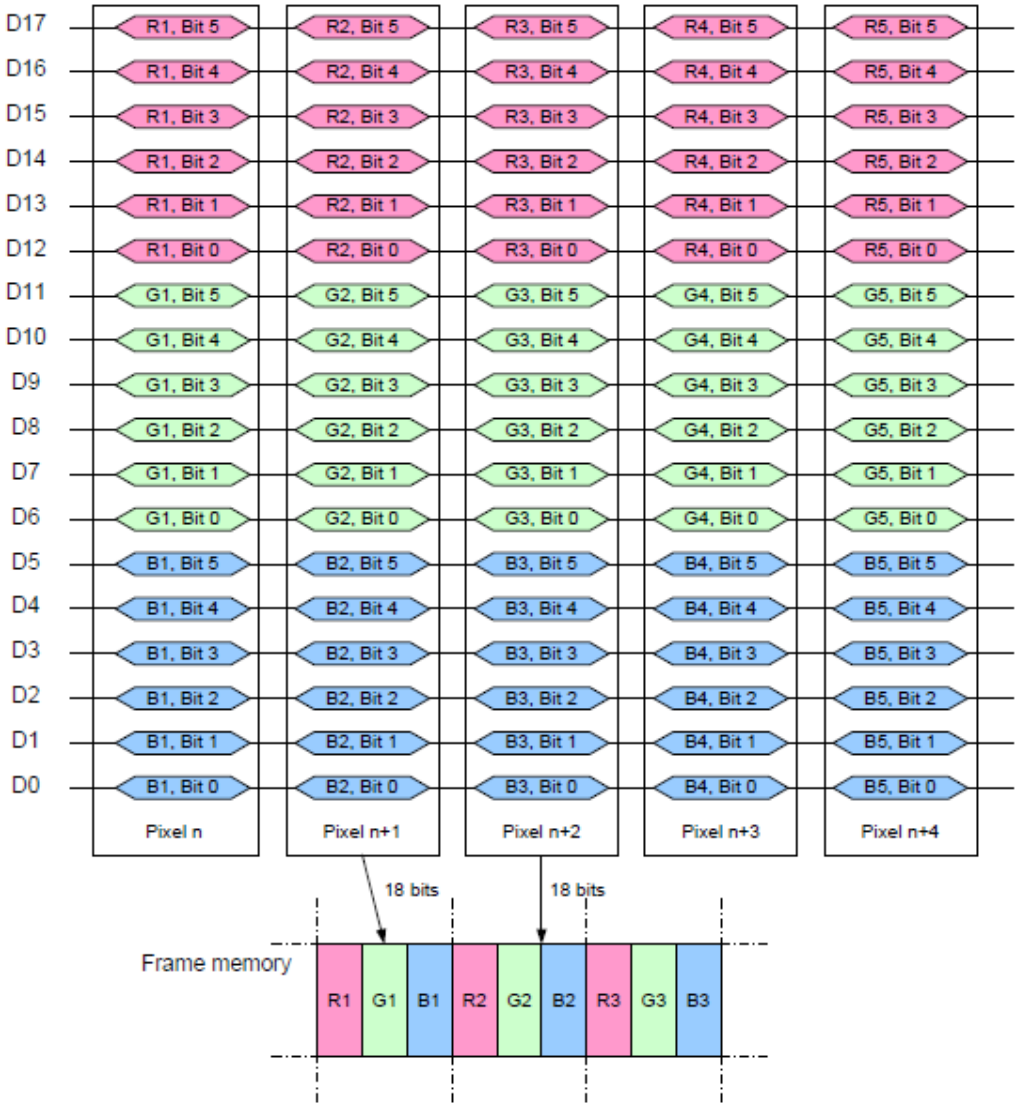
Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



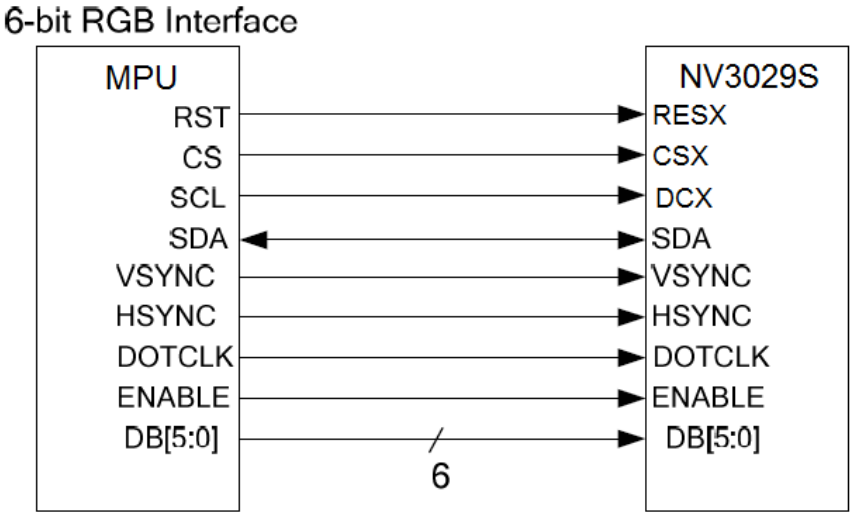
8.3.5.2 18-bit RGB interface



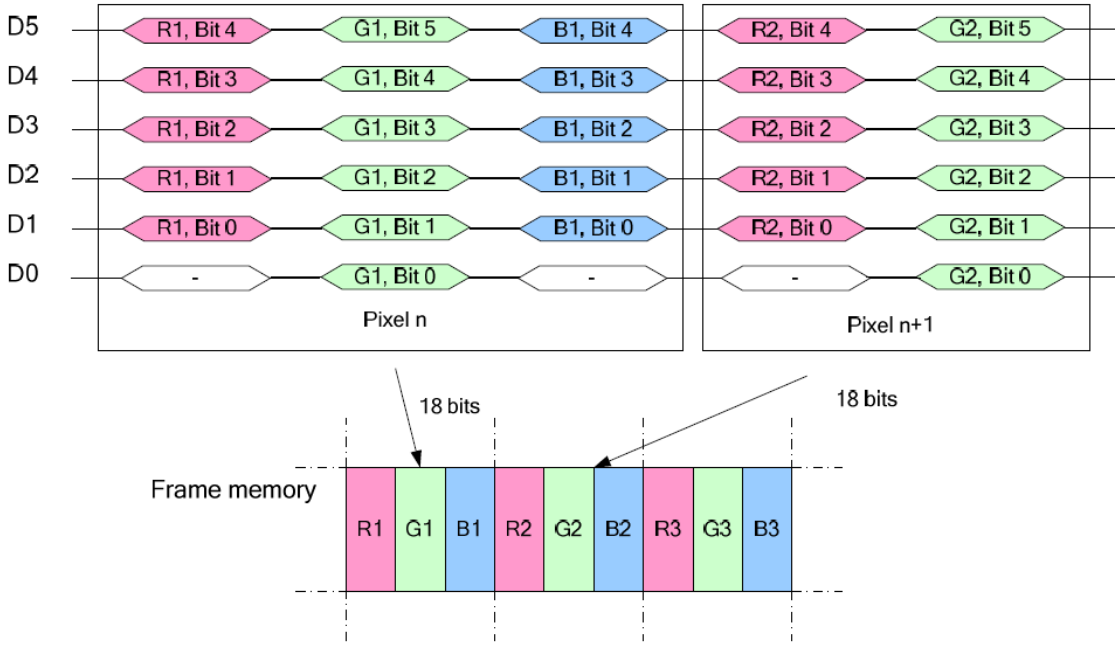
Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



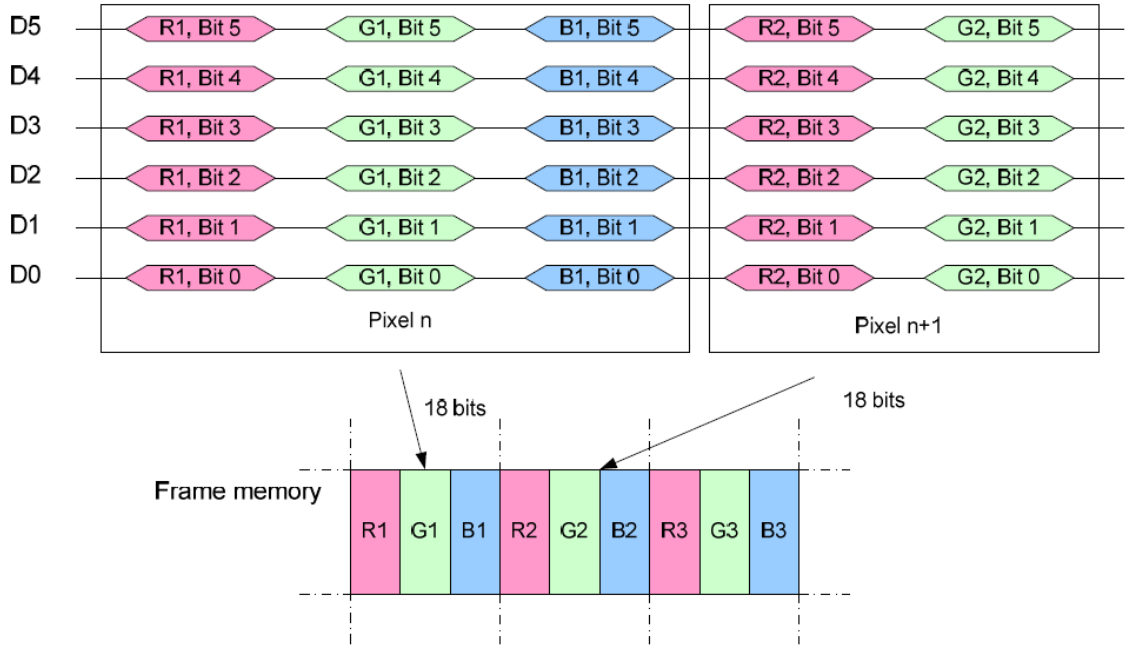
8.3.5.3 6-bit RGB interface



8.3.5.3.1 16-bit/pixel



8.3.5.3.2 18-bit/pixel

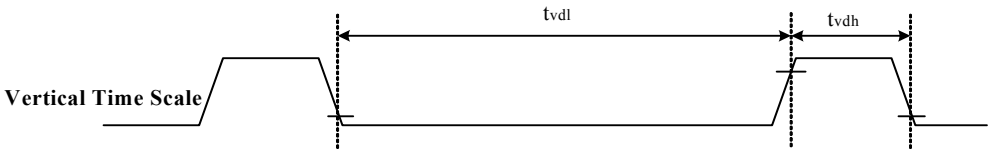


8.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

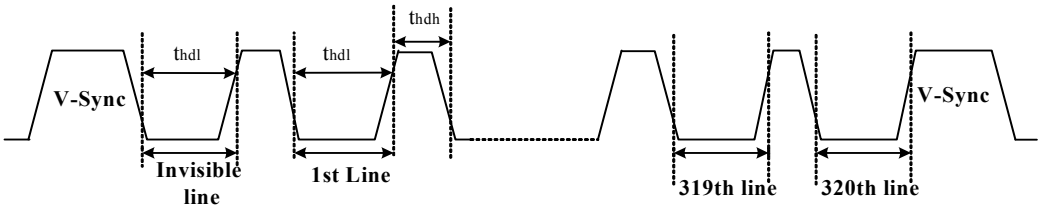
8.4.1 Tearing Effect line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync Information only:

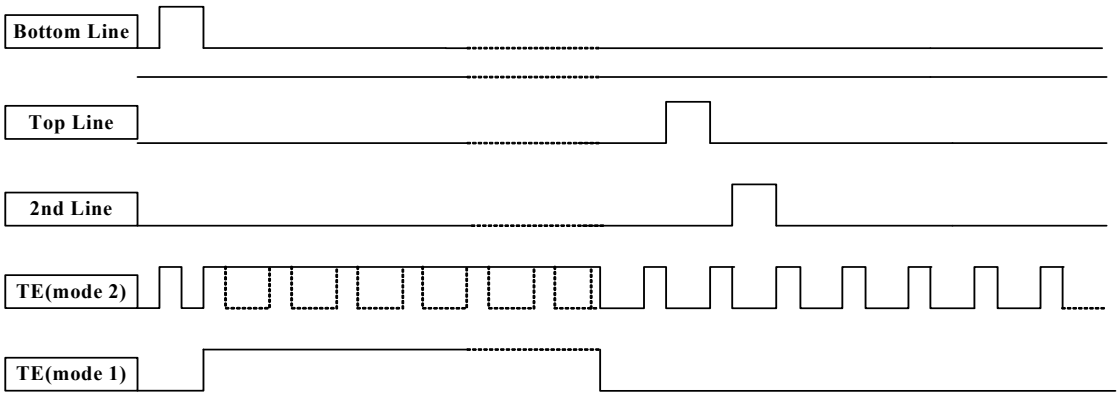


tvdh = The LCD display is not updated from the Frame Memory;
tvdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync Information, there is one V-sync and 320 H- sync pulses per field:



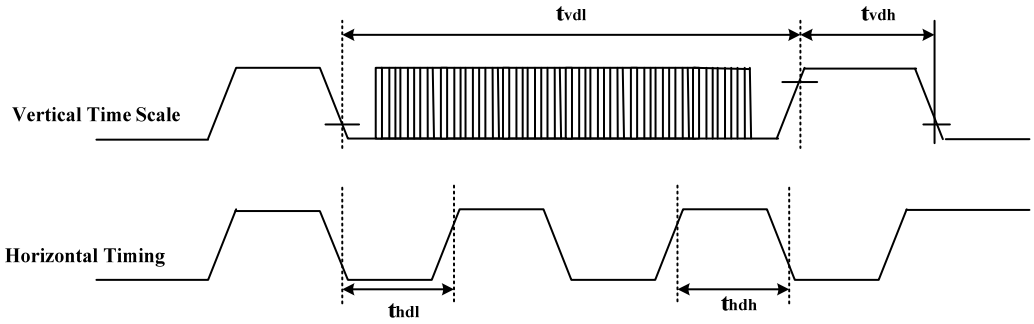
thdh = The LCD display is not updated from the Frame Memory;
thdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).



Note: During sleep in Mode,the tearing effect Output pin is active low.

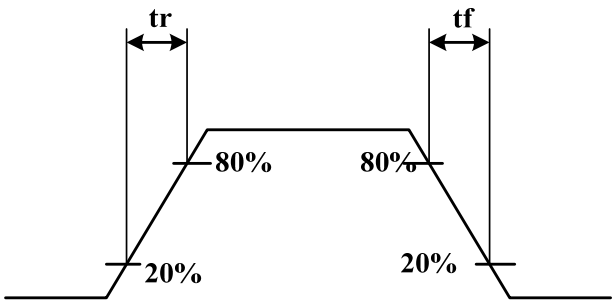
8.4.2 Tearing Effect line Timings

The Tearing Effect signal is described below:



Symbol	Parameter	Min.	Max	Unit
tvdl	Vertical Timing Low Duration	13	17	ms
tvdh	Vertical Timing High Duration	1000	1300	us
thdl	Horizontal Timing Low Duration	20	-	us
thdh	Horizontal Timing High Duration	10	500	us

Notes:
The timings in this table apply when MADCTL B4=0 and B4=1.
The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.



The tearing effect output line is fed back to the MPU and should be used to avoid tearing effect.

8.5 Power On/Off Sequence

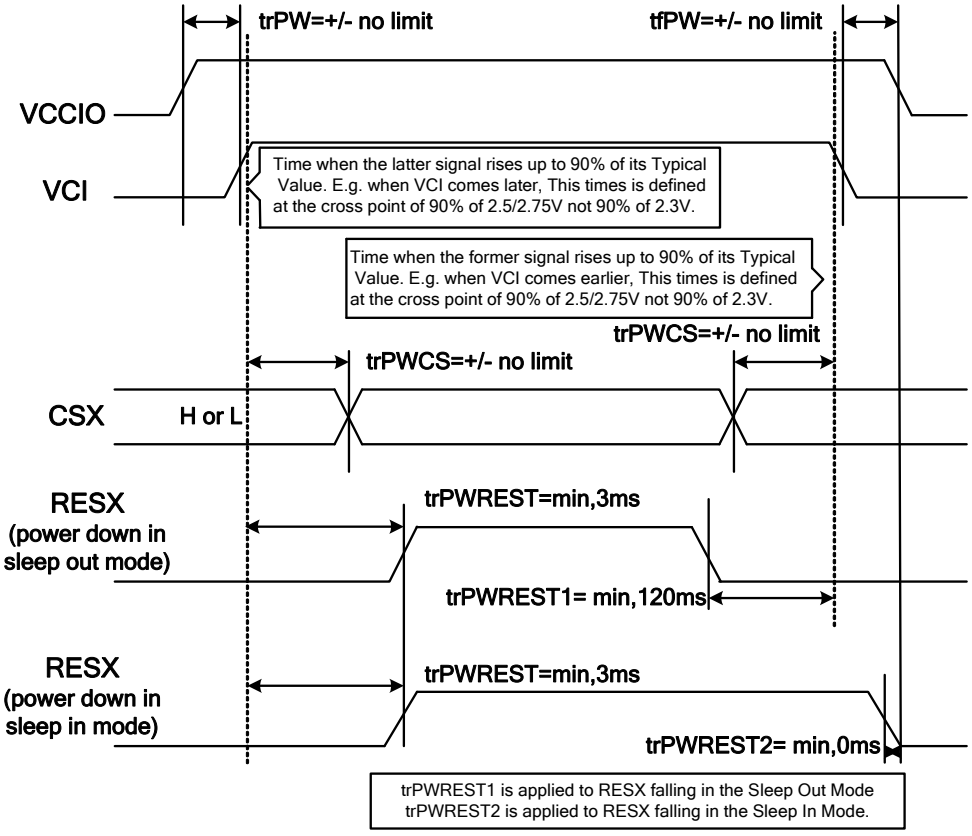
8.5.1 Power On/Off Sequence

VCCIO and VCI can be applied in any order.
VCI and VCCIO can be powered down in any order.
During power off, if LCD is in the Sleep Out Mode, VCI and VCCIO must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VCCIO or VCI can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:
1. There will be no damage to the display module if the above power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power off sequence.
4. If RESX line is not held stable by MPU during Power On Sequence ,it will be necessary to apply a Hardware Reset (RESX) after MPU Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

8.5.1.1 Case 1 – RESX line is held high or Unstable by MPU at Power On

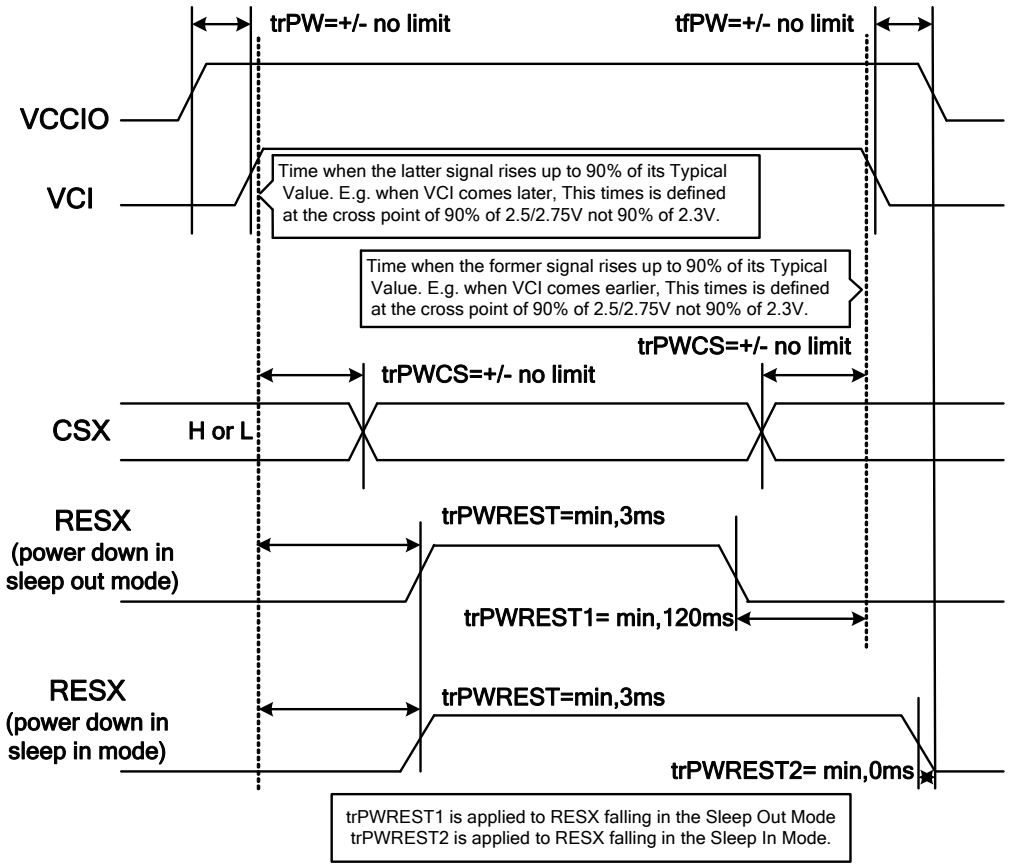
If RESX line is held High or unstable by the MPU during Power On, then a Hardware Reset must be applied after both VCI and VCCIO have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timing here in show cross point at 50% of signal/power level.

8.5.1.2 Case 2 – RESX line is held low by MPU at Power On

If RESX line is held Low (and stable) by the MPU during Power On, then the RESX must be held low for minimum 3msec after both VCI and VCCIO have been applied.



Note: Unless otherwise specilied, timing here in show cross point at 50% of signal/power level.

8.6 Power Level Definition

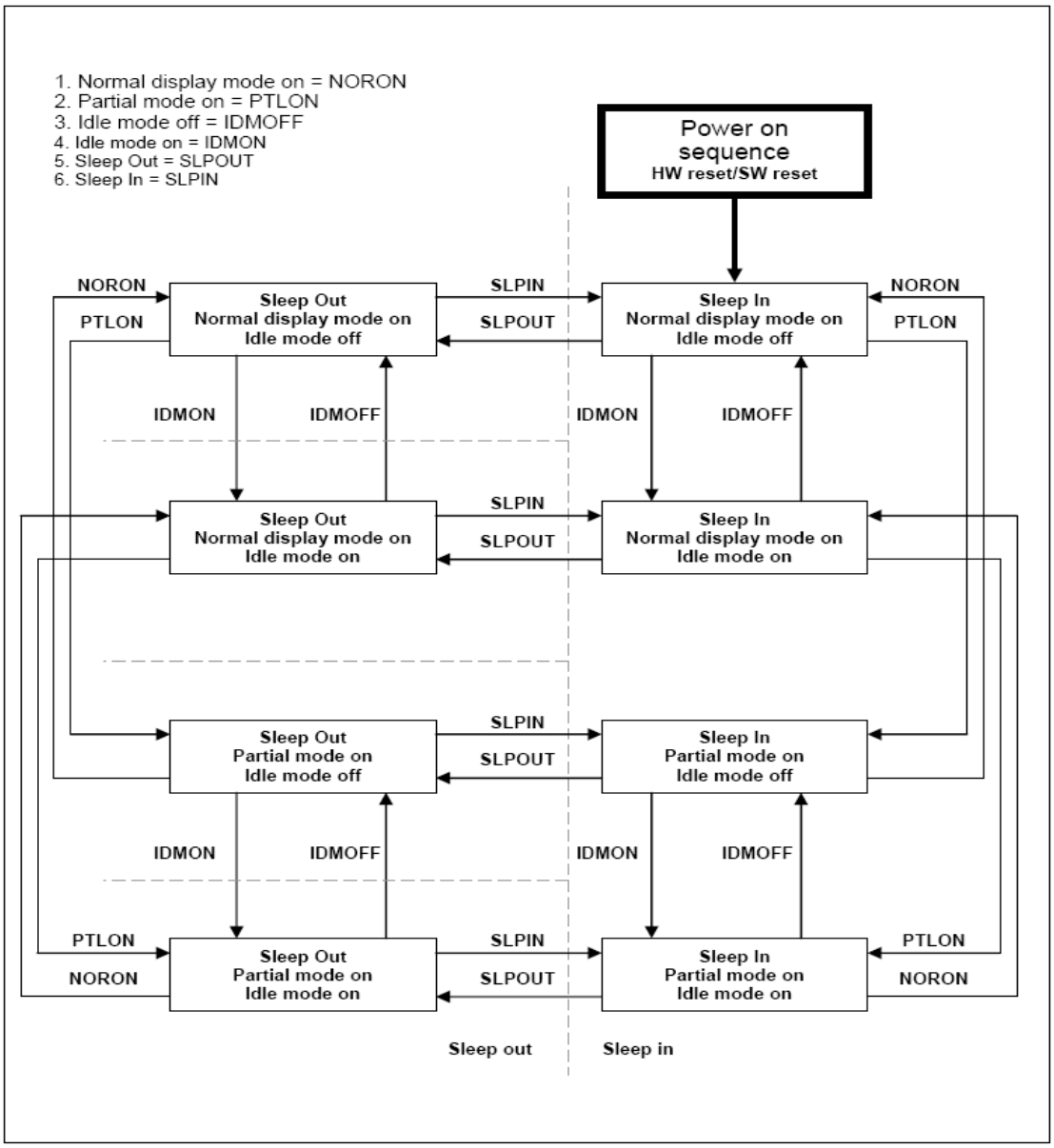
8.6.1 Power levels

6 level modes are defined they are in order of Maximum power consumption to Minimum power consumption.

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors
5. Sleep In Mode
   In this mode, the DC/DC converter, Internal oscillator and panel driver circuit are stopped. Only the interface and memory works with VCCIO power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and VCCIO are removed

Note:
Transition between modes 1-5 is controllable by commands. Mode 6 is entered only when both Power supplies are removed.

8.6.2 Power flow chart



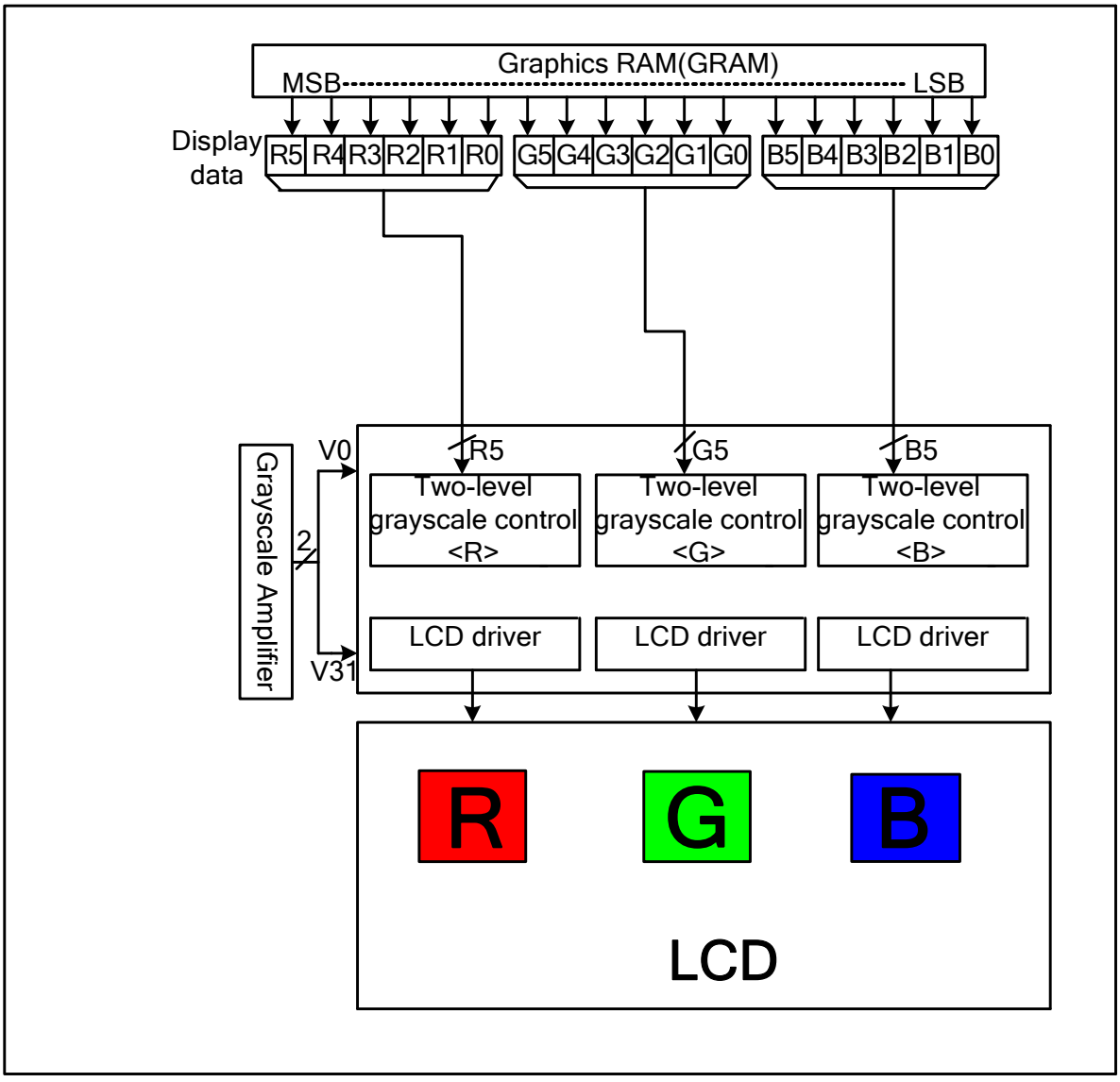
Notes:

1. There is not any abnormal visual effect when there is changing from one power mode to anther power mode.
2. There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

8.7 8-color Display Mode

The NV3029S has a function to display in eight colors. In 8-color mode, the available grayscales are only V0 and V31, and the power supplies for other grayscales (V1 to V30) are cut off to reduce power consumption.

The γ-correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.
In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.



8.8 Gamma Correction

The NV3029S incorporates gamma adjustment function for the 32,768-color display (32 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 15 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

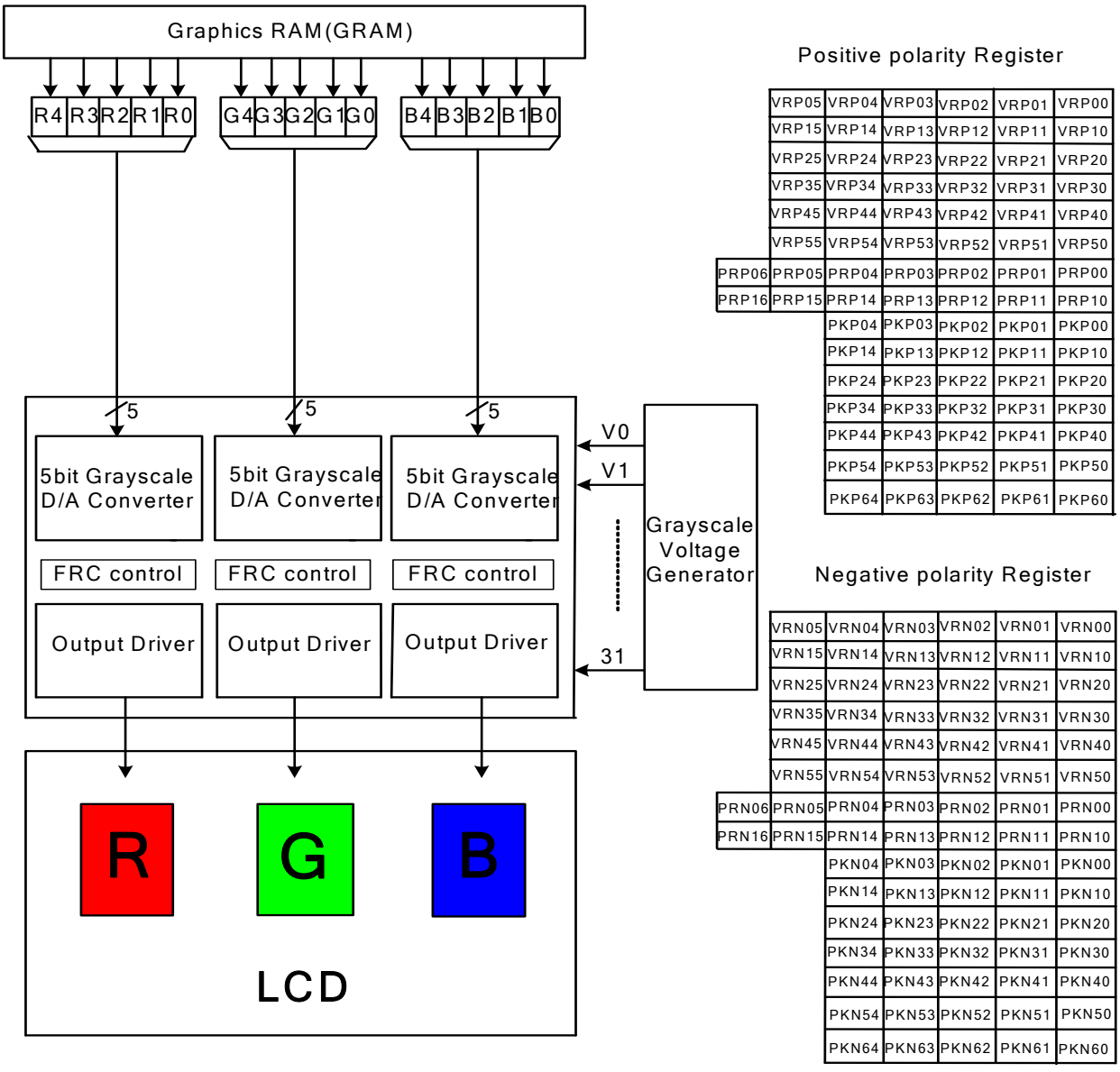


Figure 1: Grayscale control

8.8.1 Gamma-characteristics adjustment registers

This NV3029S has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into three groups, which correspond to the gradient, amplitude, and Micro Adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

0- **Offset adjustment registers**

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- **Gamma center adjustment registers**

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- **Gamma Micro Adjustment registers**

The gamma Micro Adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~6), each of which has 5 inputs and generates one reference voltage output (VgP/N (3,4,10,15,21,27,28)).

Gamma-adjustment registers			
Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor （PRP/N0） for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor （PRP/N1） for center adjustment
Micro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 4)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 10)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 21)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 27)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 28)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 15)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor （VRP/N0） for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor （VRP/N1） for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor （VRP/N2） for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor （VRP/N3） for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor （VRP/N4） for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor （VRP/N5） for offset adjustment

8.8.2 Gamma resister stream

The block consists of one gamma resister stream. Use different register setting for positive or negative polarity. Each polarity includes fifteen gamma reference voltages. VgP/N (0, 1, 2, 3, 4, 5, 10, 15, 21, 26, 27, 28, 29, 30, 31).

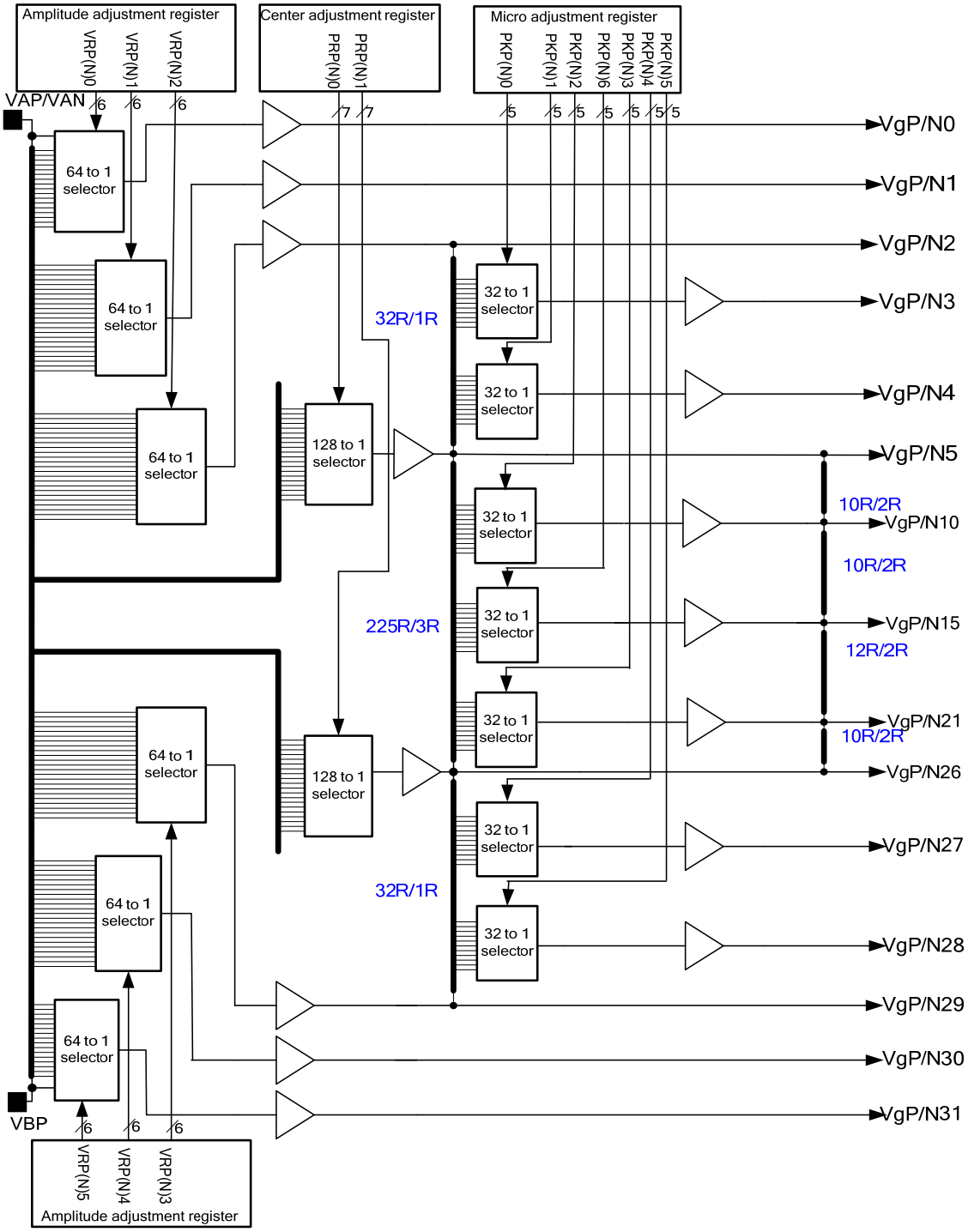


Figure 2 : Gamma resister stream and gamma reference voltage

8.8.3 Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below:

- Table 1: Offset adjustment 0 ~ 5

Register VR(P/N)0[5:0]	Resistance VR(P/N)0
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)1[5:0]	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)2[5:0]	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)3[5:0]	Resistance VR(P/N)3
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

Register VR(P/N)4[5:0]	Resistance VR(P/N)4
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

Register VR(P/N)5[5:0]	Resistance VR(P/N)5
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

- Table 2 : Center adjustment

Register PPR(P/N)0[6:0]	Resistance PR(P/N)0
0000000	0R
0000001	2R
0000010	4R
…	…
1111101	250R
1111110	252R
1111111	254R

Register PPR(P/N)1[6:0]	Resistance PR(P/N)1
0000000	0R
0000001	2R
0000010	4R
…	…
1111101	250R
1111110	252R
1111111	254R

8.8.4 The grayscale levels are determined by the following formulas.

Table 3 : VinP/N0

Reference Voltage	Micro Adjustment value	VinP/N0 formula
VinP/N0	VRP/N0 5-0 = 000000	VAP/VAN
	VRP/N0 5-0 = 000001	((450R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000010	((450R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000011	((450R -6R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000100	((450R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000101	((450R -10R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000110	((450R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000111	((450R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001000	((450R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001001	((450R -18R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001010	((450R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001011	((450R -22R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001100	((450R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001101	((450R -26R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001110	((450R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001111	((450R -30R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010000	((450R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010001	((450R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010010	((450R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010011	((450R -38R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010100	((450R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010101	((450R -42R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010110	((450R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010111	((450R -46R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011000	((450R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011001	((450R -50R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011010	((450R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011011	((450R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011100	((450R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011101	((450R -58R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011110	((450R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011111	((450R -62R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100000	((450R -66R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100001	((450R -70R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100010	((450R -74R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100011	((450R -78R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100100	((450R -82R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100101	((450R -86R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100110	((450R -90R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100111	((450R -94R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101000	((450R -98R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101001	((450R -102R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101010	((450R -106R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101011	((450R -110R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101100	((450R -114R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101101	((450R -118R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101110	((450R -122R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101111	((450R -126R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110000	((450R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110001	((450R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110010	((450R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110011	((450R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110100	((450R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110101	((450R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110110	((450R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110111	((450R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111000	((450R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111001	((450R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111010	((450R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111011	((450R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111100	((450R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111101	((450R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111110	((450R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111111	((450R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 4 : VinP/N1

Reference Voltage	Micro Adjustment value	VinP/N1 formula
VinP/N1	VRP/N1 5-0 = 000000	VAP/VAN
	VRP/N1 5-0 = 000001	((450R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000010	((450R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000011	((450R -6R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000100	((450R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000101	((450R -10R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000110	((450R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000111	((450R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001000	((450R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001001	((450R -18R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001010	((450R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001011	((450R -22R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001100	((450R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001101	((450R -26R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001110	((450R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001111	((450R -30R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010000	((450R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010001	((450R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010010	((450R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010011	((450R -38R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010100	((450R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010101	((450R -42R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010110	((450R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010111	((450R -46R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011000	((450R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011001	((450R -50R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011010	((450R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011011	((450R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011100	((450R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011101	((450R -58R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011110	((450R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011111	((450R -62R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100000	((450R -66R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100001	((450R -70R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100010	((450R -74R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100011	((450R -78R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100100	((450R -82R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100101	((450R -86R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100110	((450R -90R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100111	((450R -94R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101000	((450R -98R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101001	((450R -102R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101010	((450R -106R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101011	((450R -110R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101100	((450R -114R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101101	((450R -118R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101110	((450R -122R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101111	((450R -126R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110000	((450R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110001	((450R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110010	((450R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110011	((450R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110100	((450R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110101	((450R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110110	((450R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110111	((450R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111000	((450R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111001	((450R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111010	((450R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111011	((450R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111100	((450R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111101	((450R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111110	((450R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111111	((450R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 5: VinP/N2

Reference Voltage	Micro Adjustment value	VinP/N2 formula
VinP/N2	VRP/N2 5-0 = 000000	(410R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000001	((410R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000010	((410R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000011	((410R -6R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000100	((410R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000101	((410R -10R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000110	((410R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000111	((410R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001000	((410R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001001	((410R -18R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001010	((410R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001011	((410R -22R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001100	((410R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001101	((410R -26R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001110	((410R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001111	((410R -30R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010000	((410R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010001	((410R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010010	((410R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010011	((410R -38R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010100	((410R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010101	((410R -42R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010110	((410R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010111	((410R -46R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011000	((410R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011001	((410R -50R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011010	((410R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011011	((410R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011100	((410R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011101	((410R -58R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011110	((410R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011111	((410R -62R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100000	((410R -66R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100001	((410R -70R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100010	((410R -74R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100011	((410R -78R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100100	((410R -82R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100101	((410R -86R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100110	((410R -90R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100111	((410R -94R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101000	((410R -98R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101001	((410R -102R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101010	((410R -106R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101011	((410R -110R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101100	((410R -114R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101101	((410R -118R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101110	((410R -122R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101111	((410R -126R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110000	((410R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110001	((410R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110010	((410R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110011	((410R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110100	((410R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110101	((410R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110110	((410R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110111	((410R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111000	((410R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111001	((410R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111010	((410R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111011	((410R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111100	((410R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111101	((410R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111110	((410R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111111	((410R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 6 : VinP/N10

Reference Voltage	Micro Adjustment value	VinP/N10 formula
VinP/N10	VRP/N3 5-0 = 000000	(230R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000001	((230R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000010	((230R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000011	((230R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000100	((230R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000101	((230R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000110	((230R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000111	((230R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001000	((230R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001001	((230R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001010	((230R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001011	((230R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001100	((230R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001101	((230R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001110	((230R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001111	((230R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010000	((230R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010001	((230R -68R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010010	((230R -72R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010011	((230R -76R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010100	((230R -80R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010101	((230R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010110	((230R -88R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010111	((230R -92R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011000	((230R -96R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011001	((230R -100R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011010	((230R -104R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011011	((230R -108R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011100	((230R -112R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011101	((230R -116R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011110	((230R -120R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011111	((230R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100000	((230R -128R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100001	((230R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100010	((230R -132R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100011	((230R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100100	((230R -136R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100101	((230R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100110	((230R -140R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100111	((230R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101000	((230R -144R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101001	((230R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101010	((230R -148R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101011	((230R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101100	((230R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101101	((230R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101110	((230R -156R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101111	((230R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110000	((230R -160R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110001	((230R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110010	((230R -164R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110011	((230R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110100	((230R -168R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110101	((230R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110110	((230R -172R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110111	((230R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111000	((230R -176R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111001	((230R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111010	((230R -180R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111011	((230R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111100	((230R -184R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111101	((230R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111110	((230R -188R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111111	((230R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 7 : VinP/N11

Reference Voltage	Micro Adjustment value	VinP/N11 formula
VinP/N11	VRP/N4 5-0 = 000000	(190R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000001	((190R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000010	((190R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000011	((190R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000100	((190R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000101	((190R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000110	((190R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000111	((190R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001000	((190R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001001	((190R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001010	((190R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001011	((190R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001100	((190R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001101	((190R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001110	((190R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001111	((190R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010000	((190R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010001	((190R -68R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010010	((190R -72R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010011	((190R -76R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010100	((190R -80R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010101	((190R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010110	((190R -88R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010111	((190R -92R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011000	((190R -96R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011001	((190R -100R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011010	((190R -104R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011011	((190R -108R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011100	((190R -112R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011101	((190R -116R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011110	((190R -120R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011111	((190R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100000	((190R -128R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100001	((190R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100010	((190R -132R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100011	((190R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100100	((190R -136R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100101	((190R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100110	((190R -140R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100111	((190R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101000	((190R -144R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101001	((190R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101010	((190R -148R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101011	((190R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101100	((190R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101101	((190R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101110	((190R -156R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101111	((190R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110000	((190R -160R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110001	((190R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110010	((190R -164R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110011	((190R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110100	((190R -168R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110101	((190R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110110	((190R -172R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110111	((190R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111000	((190R -176R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111001	((190R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111010	((190R -180R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111011	((190R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111100	((190R -184R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111101	((190R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111110	((190R -188R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111111	VBP

Table 8 : VinP/N12

Reference Voltage	Micro Adjustment value	VinP/N12 formula
VinP/N12	VRP/N5 5-0 = 000000	(190R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000001	((190R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000010	((190R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000011	((190R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000100	((190R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000101	((190R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000110	((190R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000111	((190R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001000	((190R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001001	((190R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001010	((190R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001011	((190R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001100	((190R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001101	((190R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001110	((190R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001111	((190R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010000	((190R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010001	((190R -68R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010010	((190R -72R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010011	((190R -76R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010100	((190R -80R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010101	((190R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010110	((190R -88R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010111	((190R -92R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011000	((190R -96R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011001	((190R -100R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011010	((190R -104R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011011	((190R -108R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011100	((190R -112R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011101	((190R -116R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011110	((190R -120R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011111	((190R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100000	((190R -128R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100001	((190R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100010	((190R -132R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100011	((190R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100100	((190R -136R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100101	((190R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100110	((190R -140R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100111	((190R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101000	((190R -144R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101001	((190R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101010	((190R -148R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101011	((190R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101100	((190R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101101	((190R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101110	((190R -156R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101111	((190R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110000	((190R -160R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110001	((190R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110010	((190R -164R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110011	((190R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110100	((190R -168R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110101	((190R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110110	((190R -172R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110111	((190R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111000	((190R -176R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111001	((190R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111010	((190R -180R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111011	((190R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111100	((190R -184R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111101	((190R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111110	((190R -188R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111111	VBP

Table 9 : VinP/N4

Reference Voltage	Micro Adjustment value	VinP/N4 formula
VinP/N4	PRP/N0 6-0 = 0000000	(350R / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000001	((350R – 2R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000010	((350R – 4R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000011	((350R – 6R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000100	((350R – 8R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000101	((350R – 10R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000110	((350R – 12R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000111	((350R – 14R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001000	((350R – 16R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001001	((350R – 18R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001010	((350R – 20R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001011	((350R – 22R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001100	((350R – 24R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001101	((350R – 26R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001110	((350R – 28R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001111	((350R – 30R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010000	((350R – 32R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010001	((350R – 34R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010010	((350R – 36R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010011	((350R – 38R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010100	((350R – 40R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010101	((350R – 42R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010110	((350R – 44R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010111	((350R – 46R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011000	((350R – 48R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011001	((350R – 50R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011010	((350R – 52R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011011	((350R – 54R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011100	((350R – 56R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011101	((350R – 58R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011110	((350R – 60R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011111	((350R – 62R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100000	((350R – 64R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100001	((350R – 66R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100010	((350R – 68R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100011	((350R – 70R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100100	((350R – 72R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100101	((350R – 74R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100110	((350R – 76R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100111	((350R – 78R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101000	((350R – 80R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101001	((350R – 82R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101010	((350R – 84R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101011	((350R – 86R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101100	((350R – 88R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101101	((350R – 90R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101110	((350R – 92R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101111	((350R – 94R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110000	((350R – 96R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110001	((350R – 98R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110010	((350R – 100R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110011	((350R – 102R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110100	((350R – 104R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110101	((350R – 106R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110110	((350R – 108R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110111	((350R – 110R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111000	((350R – 112R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111001	((350R – 114R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111010	((350R – 116R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111011	((350R – 118R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111100	((350R – 120R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111101	((350R – 122R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111110	((350R – 124R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111111	((350R – 126R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000000	((350R – 128R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000001	((350R – 130R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000010	((350R – 132R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000011	((350R – 134R) / 450R) * (VAP/VAN–VBP) + VBP

Reference Voltage	Micro Adjustment value	VinP/N4 formula
	PRP/N0 6-0 = 1000100	((350R – 136R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000101	((350R – 138R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000110	((350R – 140R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000111	((350R – 142R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001000	((350R – 144R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001001	((350R – 146R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001010	((350R – 148R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001011	((350R – 150R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001100	((350R – 152R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001101	((350R – 154R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001110	((350R – 156R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001111	((350R – 158R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010000	((350R – 160R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010001	((350R – 162R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010010	((350R – 164R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010011	((350R – 166R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010100	((350R – 168R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010101	((350R – 170R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010110	((350R – 172R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010111	((350R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011000	((350R – 176R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011001	((350R – 178R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011010	((350R – 180R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011011	((350R – 182R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011100	((350R – 184R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011101	((350R – 186R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011110	((350R – 188R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011111	((350R – 190R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100000	((350R – 192R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100001	((350R – 194R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100010	((350R – 196R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100011	((350R – 198R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100100	((350R – 200R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100101	((350R – 202R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100110	((350R – 204R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100111	((350R – 206R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101000	((350R – 208R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101001	((350R – 210R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101010	((350R – 212R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101011	((350R – 214R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101100	((350R – 216R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101101	((350R – 218R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101110	((350R – 220R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101111	((350R – 222R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110000	((350R – 224R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110001	((350R – 226R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110010	((350R – 228R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110011	((350R – 230R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110100	((350R – 232R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110101	((350R – 234R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110110	((350R – 236R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110111	((350R – 238R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111000	((350R – 240R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111001	((350R – 242R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111010	((350R – 244R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111011	((350R – 246R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111100	((350R – 248R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111101	((350R – 250R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111110	((350R – 252R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111111	((350R – 254R) / 450R) * (VAP/VAN–VBP) + VBP

Table 10 : VinP/N8

Reference Voltage	Micro Adjustment value	VinP/N8 formula
VinP/N8	PRP/N1 6-0 = 0000000	(354R / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000001	((354R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000010	((354R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000011	((354R – 6R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000100	((354R – 8R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000101	((354R – 10R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000110	((354R – 12R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000111	((354R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001000	((354R – 16R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001001	((354R – 18R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001010	((354R – 20R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001011	((354R – 22R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001100	((354R – 24R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001101	((354R – 26R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001110	((354R – 28R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001111	((354R – 30R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010000	((354R – 32R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010001	((354R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010010	((354R – 36R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010011	((354R – 38R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010100	((354R – 40R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010101	((354R – 42R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010110	((354R – 44R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010111	((354R – 46R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011000	((354R – 48R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011001	((354R – 50R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011010	((354R – 52R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011011	((354R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011100	((354R – 56R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011101	((354R – 58R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011110	((354R – 60R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011111	((354R – 62R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100000	((354R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100001	((354R – 66R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100010	((354R – 68R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100011	((354R – 70R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100100	((354R – 72R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100101	((354R – 74R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100110	((354R – 76R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100111	((354R – 78R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101000	((354R – 80R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101001	((354R – 82R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101010	((354R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101011	((354R – 86R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101100	((354R – 88R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101101	((354R – 90R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101110	((354R – 92R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101111	((354R – 94R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110000	((354R – 96R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110001	((354R – 98R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110010	((354R – 100R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110011	((354R – 102R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110100	((354R – 104R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110101	((354R – 106R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110110	((354R – 108R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110111	((354R – 110R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111000	((354R – 112R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111001	((354R – 114R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111010	((354R – 116R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111011	((354R – 118R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111100	((354R – 120R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111101	((354R – 122R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111110	((354R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111111	((354R – 126R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000000	((354R – 128R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000001	((354R – 130R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000010	((354R -132R) / 450R) * (VAP/VAN–VBP) + VBP

Reference Voltage	Micro Adjustment value	VinP/N8 formula
VinP/N8	PRP/N1 6-0 = 1000011	((354R – 134R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000100	((354R – 136R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000101	((354R – 138R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000110	((354R – 140R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000111	((354R – 142R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001000	((354R – 144R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001001	((354R – 146R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001010	((354R – 148R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001011	((354R – 150R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001100	((354R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001101	((354R – 154R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001110	((354R – 156R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001111	((354R – 158R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010000	((354R – 160R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010001	((354R – 162R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010010	((354R – 164R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010011	((354R – 166R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010100	((354R – 168R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010101	((354R – 170R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010110	((354R – 172R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010111	((354R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011000	((354R – 176R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011001	((354R – 178R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011010	((354R – 180R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011011	((354R – 182R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011100	((354R – 184R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011101	((354R – 186R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011110	((354R – 188R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011111	((354R – 190R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100000	((354R – 192R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100001	((354R – 194R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100010	((354R – 196R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100011	((354R – 198R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100100	((354R – 200R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100101	((354R – 202R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100110	((354R – 204R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100111	((354R – 206R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101000	((354R – 208R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101001	((354R – 210R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101010	((354R – 212R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101011	((354R – 214R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101100	((354R – 216R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101101	((354R – 218R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101110	((354R – 220R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101111	((354R – 222R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110000	((354R – 224R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110001	((354R – 226R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110010	((354R – 228R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110011	((354R – 230R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110100	((354R – 232R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110101	((354R – 234R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110110	((354R – 236R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110111	((354R – 238R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111000	((354R – 240R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111001	((354R – 242R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111010	((354R – 244R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111011	((354R – 246R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111100	((354R – 248R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111101	((354R – 250R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111110	((354R – 252R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111111	((354R – 254R) / 450R) * (VAP/VAN–VBP) + VBP

Table 11: VinP/N3

Reference Voltage	Micro Adjustment value	VinP/N3 formula
VinP/N3	PKP/N0 4-0 = 00000	(31R / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01010	((31R -10R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01011	((31R -11R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01100	((31R -12R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01101	((31R -13R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01110	((31R -14R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01111	((31R -15R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10000	((31R -16R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10001	((31R -17R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10010	((31R -18R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10011	((31R -19R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10100	((31R -20R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10101	((31R -21R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10110	((31R -22R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10111	((31R -23R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11000	((31R -24R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11001	((31R -25R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11010	((31R -26R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11011	((31R -27R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11100	((31R -28R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11101	((31R -29R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11110	((31R -30R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11111	((31R -31R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4

Table 12: VinP/N3_2

Reference Voltage	Micro Adjustment value	VinP/N3_2 formula
VinP/N3_2	PKP/N1 4-0 = 00000	(31R / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01010	((31R -10R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01011	((31R -11R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01100	((31R -12R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01101	((31R -13R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01110	((31R -14R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01111	((31R -15R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10000	((31R -16R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10001	((31R -17R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10010	((31R -18R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10011	((31R -19R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10100	((31R -20R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10101	((31R -21R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10110	((31R -22R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10111	((31R -23R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11000	((31R -24R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11001	((31R -25R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11010	((31R -26R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11011	((31R -27R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11100	((31R -28R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11101	((31R -29R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11110	((31R -30R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11111	((31R -31R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4

Table 13: VinP/N5

Reference Voltage	Micro Adjustment value	VinP/N5 formula
VinP/N5	PKP/N2 4-0 = 00000	(195R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00001	((195R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00010	((195R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00011	((195R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00100	((195R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00101	((195R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00110	((195R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00111	((195R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01000	((195R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01001	((195R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01010	((195R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01011	((195R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01100	((195R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01101	((195R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01110	((195R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01111	((195R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10000	((195R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10001	((195R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10010	((195R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10011	((195R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10100	((195R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10101	((195R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10110	((195R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10111	((195R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11000	((195R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11001	((195R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11010	((195R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11011	((195R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11100	((195R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11101	((195R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11110	((195R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11111	((195R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 13a: VinP/N6

Reference Voltage	Micro Adjustment value	VinP/N6 formula
VinP/N6	PKP/N6 4-0 = 00000	(159R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00001	((159R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00010	((159R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00011	((159R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00100	((159R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00101	((159R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00110	((159R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00111	((159R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01000	((159R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01001	((159R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01010	((159R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01011	((159R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01100	((159R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01101	((159R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01110	((159R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01111	((159R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10000	((159R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10001	((159R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10010	((159R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10011	((159R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10100	((159R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10101	((159R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10110	((159R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10111	((159R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11000	((159R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11001	((159R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11010	((159R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11011	((159R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11100	((159R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11101	((159R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11110	((159R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11111	((159R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 14: VinP/N7

Reference Voltage	Micro Adjustment value	VinP/N7 formula
VinP/N7	PKP/N3 4-0 = 00000	(123R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00001	((123R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00010	((123R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00011	((123R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00100	((123R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00101	((123R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00110	((123R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00111	((123R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01000	((123R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01001	((123R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01010	((123R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01011	((123R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01100	((123R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01101	((123R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01110	((123R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01111	((123R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10000	((123R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10001	((123R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10010	((123R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10011	((123R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10100	((123R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10101	((123R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10110	((123R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10111	((123R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11000	((123R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11001	((123R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11010	((123R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11011	((123R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11100	((123R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11101	((123R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11110	((123R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11111	((123R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 15: VinP/N9_2

Reference Voltage	Micro Adjustment value	VinP/N9_2 formula
VinP/N9_2	PKP/N4 4-0 = 00000	(31R / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00001	((31R -1R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00010	((31R -2R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00011	((31R -3R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00100	((31R -4R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00101	((31R -5R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00110	((31R -6R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00111	((31R -7R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01000	((31R -8R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01001	((31R -9R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01010	((31R -10R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01011	((31R -11R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01100	((31R -12R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01101	((31R -13R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01110	((31R -14R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01111	((31R -15R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10000	((31R -16R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10001	((31R -17R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10010	((31R -18R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10011	((31R -19R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10100	((31R -20R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10101	((31R -21R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10110	((31R -22R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10111	((31R -23R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11000	((31R -24R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11001	((31R -25R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11010	((31R -26R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11011	((31R -27R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11100	((31R -28R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11101	((31R -29R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11110	((31R -30R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11111	((31R -31R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10

Table 16: VinP/N9

Reference Voltage	Micro Adjustment value	VinP/N9 formula
VinP/N9	PKP/N5 4-0 = 00000	(31R / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00001	((31R -1R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00010	((31R -2R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00011	((31R -3R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00100	((31R -4R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00101	((31R -5R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00110	((31R -6R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00111	((31R -7R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01000	((31R -8R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01001	((31R -9R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01010	((31R -10R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01011	((31R -11R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01100	((31R -12R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01101	((31R -13R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01110	((31R -14R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01111	((31R -15R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10000	((31R -16R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10001	((31R -17R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10010	((31R -18R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10011	((31R -19R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10100	((31R -20R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10101	((31R -21R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10110	((31R -22R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10111	((31R -23R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11000	((31R -24R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11001	((31R -25R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11010	((31R -26R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11011	((31R -27R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11100	((31R -28R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11101	((31R -29R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11110	((31R -30R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11111	((31R -31R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10

Table 17:Positive polarity

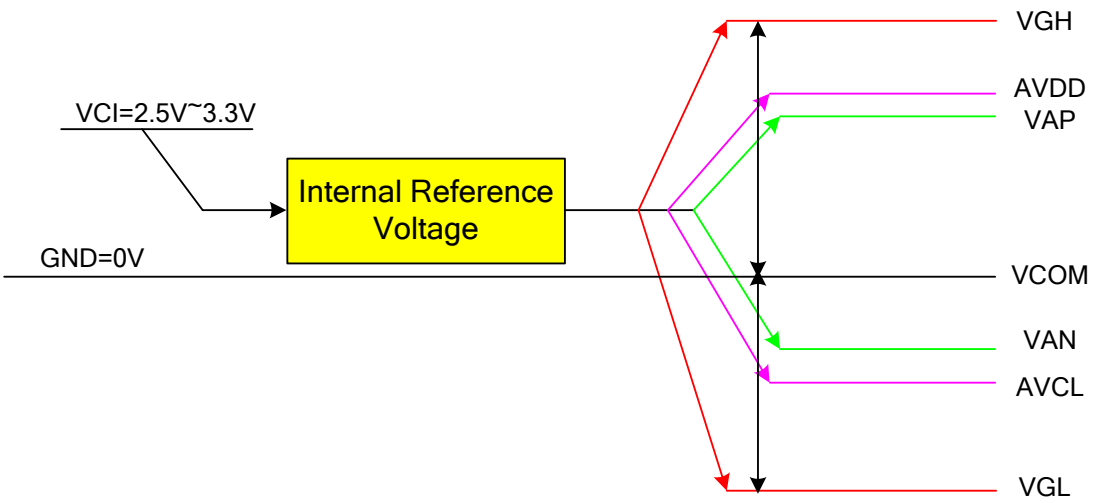
Grayscale voltage	Formula
v0	VinP0
v1	VinP1
v2	VinP2
v3	VinP3
v4	VinP3_2
v5	VinP4
v6	VinP5+(VinP4-VinP5)*(8R/10R)
v7	VinP5+(VinP4-VinP5)*(6R/10R)
v8	VinP5+(VinP4-VinP5)*(4R/10R)
v9	VinP5+(VinP4-VinP5)*(2R/10R)
v10	VinP5
v11	VinP6+(VinP5-VinP6)*(8R/10R)
v12	VinP6+(VinP5-VinP6)*(6R/10R)
v13	VinP6+(VinP5-VinP6)*(4R/10R)
v14	VinP6+(VinP5-VinP6)*(2R/10R)
v15	VinP6
v16	VinP7+(VinP6-VinP7)*(10R/12R)
v17	VinP7+(VinP6-VinP7)*(8R/12R)
v18	VinP7+(VinP6-VinP7)*(6R/12R)
v19	VinP7+(VinP6-VinP7)*(4R/12R)
v20	VinP7+(VinP6-VinP7)*(2R/12R)
v21	VinP7
v22	VinP8+(VinP7-VinP8)*(8R/10R)
v23	VinP8+(VinP7-VinP8)*(6R/10R)
v24	VinP8+(VinP7-VinP8)*(4R/10R)
v25	VinP8+(VinP7-VinP8)*(2R/10R)
v26	VinP8
v27	VinP9_2
v28	VinP9
v29	VinP10
v30	VinP11
v31	VinP12

Table 18: Negative polarity

Grayscale voltage	Formula
v31	VinN0
v30	VinN1
v29	VinN2
v28	VinN3
v27	VinN3_2
v26	VinN4
v25	VinN5+(VinN4-VinN5)*(8R/10R)
v24	VinN5+(VinN4-VinN5)*(6R/10R)
v23	VinN5+(VinN4-VinN5)*(4R/10R)
v22	VinN5+(VinN4-VinN5)*(2R/10R)
v21	VinN5
v20	VinN6+(VinN5-VinN6)*(8R/10R)
v19	VinN6+(VinN5-VinN6)*(6R/10R)
v18	VinN6+(VinN5-VinN6)*(4R/10R)
v17	VinN6+(VinN5-VinN6)*(2R/10R)
v16	VinN6
v15	VinN7+(VinN6-VinN7)*(10R/12R)
v14	VinN7+(VinN6-VinN7)*(8R/12R)
v13	VinN7+(VinN6-VinN7)*(6R/12R)
v12	VinN7+(VinN6-VinN7)*(4R/12R)
v11	VinN7+(VinN6-VinN7)*(2R/12R)
v10	VinN7
v9	VinN8+(VinN7-VinN8)*(8R/10R)
v8	VinN8+(VinN7-VinN8)*(6R/10R)
v7	VinN8+(VinN7-VinN8)*(4R/10R)
v6	VinN8+(VinN7-VinN8)*(2R/10R)
v5	VinN8
v4	VinN9_2
v3	VinN9
v2	VinN10
v1	VinN11
v0	VinN12

8.9 Voltage Generation

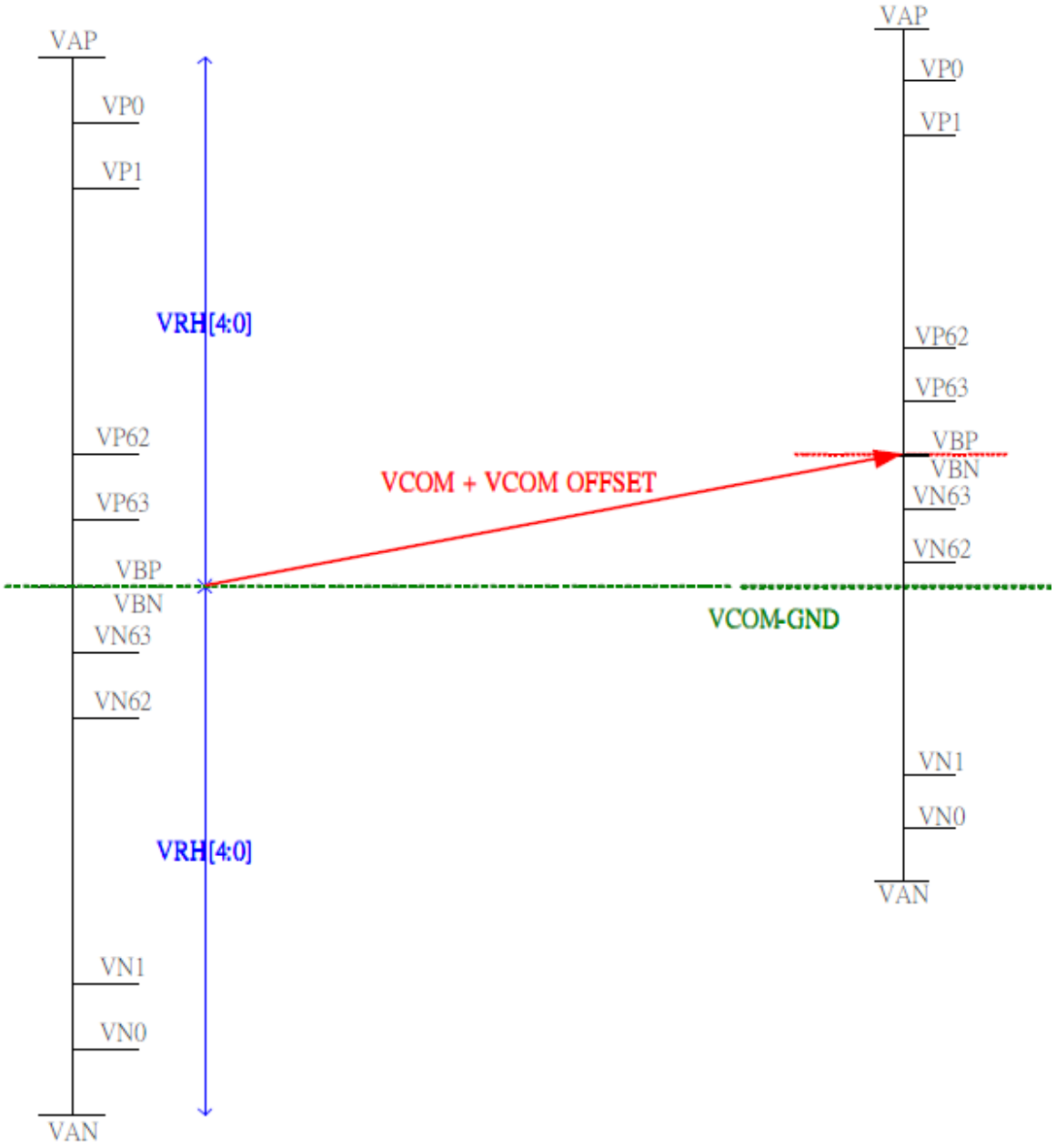
The following is the NV3029S analog voltage pattern diagram:



Power Booster Level

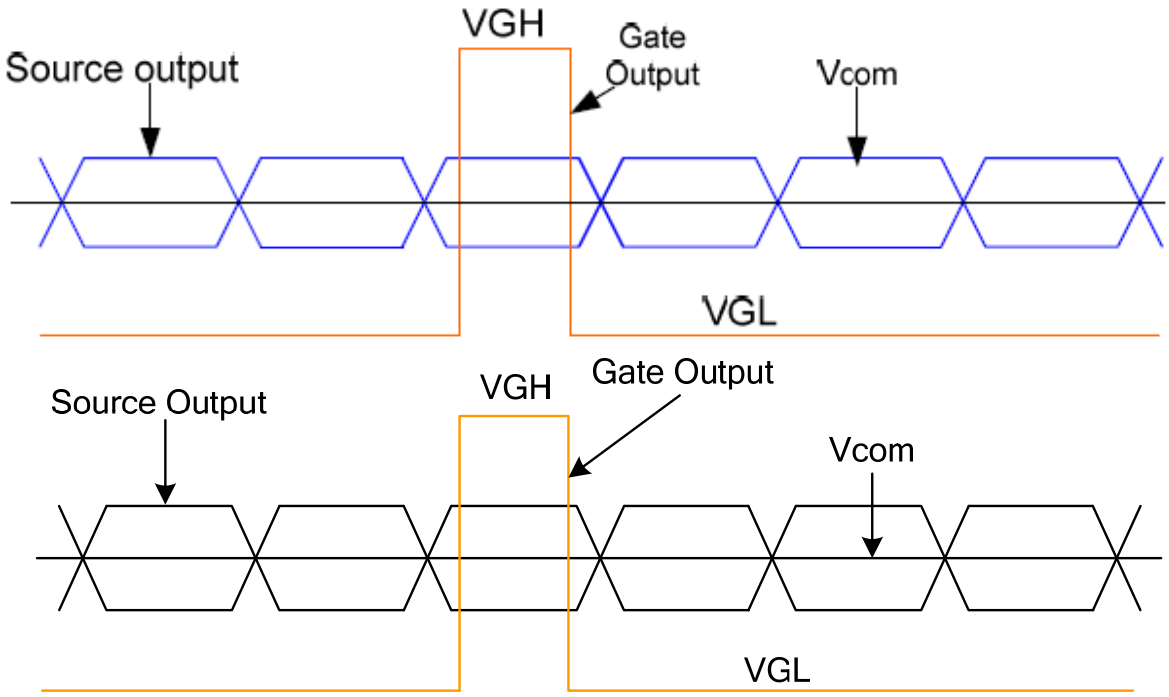
8.10 Relationship about source voltage

The relationship about source voltage is shown as below:



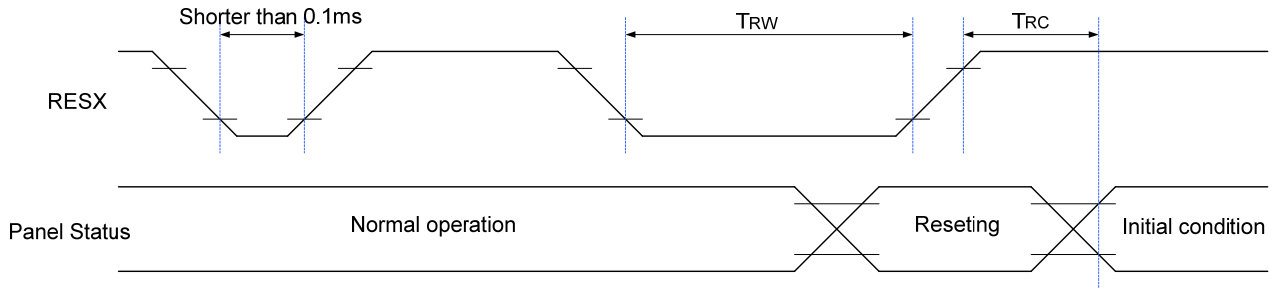
Relationship about source voltage

8.11 Applied Voltage to the TFT panel



Voltage Output to TFT LCD Panel

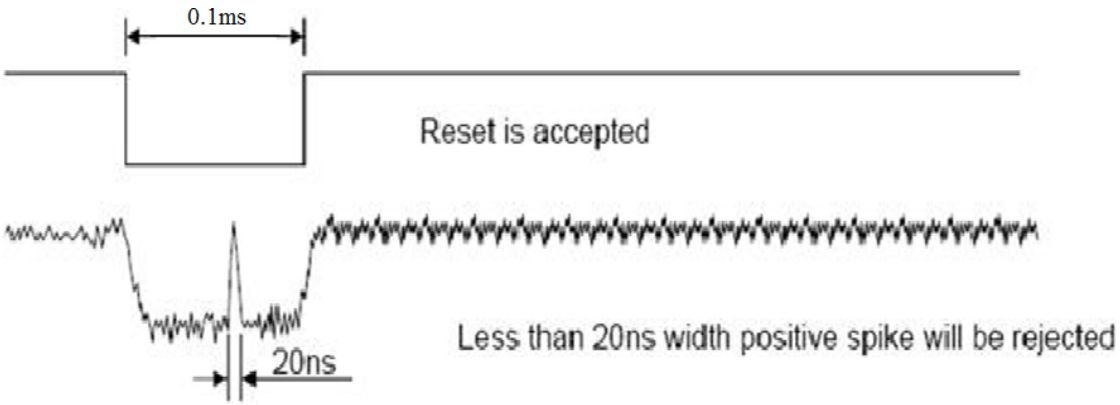
8.12 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	T_{RW}	RESX low pulse duration	0.1		ms
	T_{RC}	Reset cancel			ms

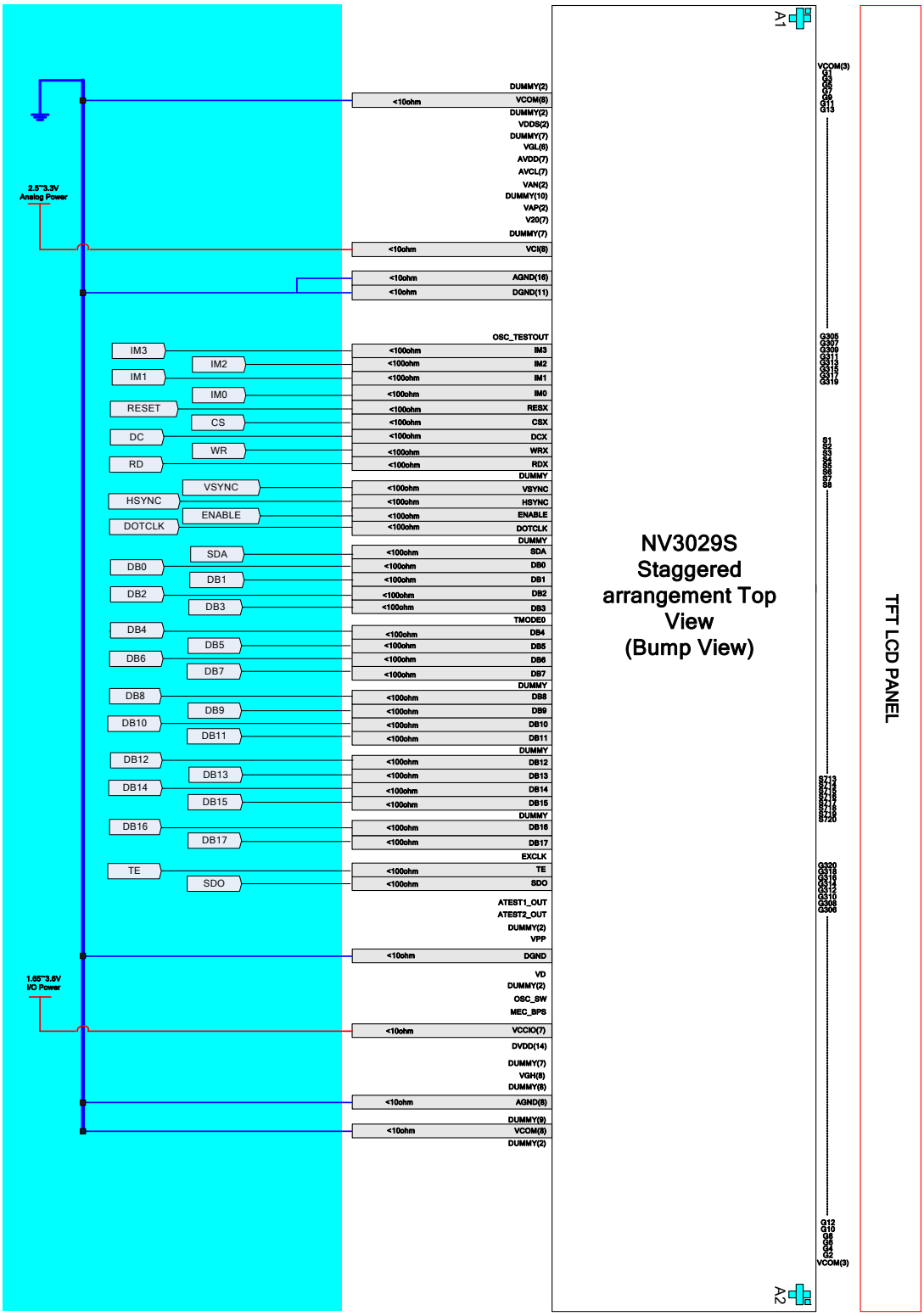
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time(RT) within 5ms after a rising edge of RESX.
2. Spice due to and electrostatic discharge on RESX line does not cause irregular system reset.
   When short than 0.1ms, reset rejected.
3. During the Resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in sleep in-mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

9. Application



10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Item	Symbol	Unit	Ratings	Notes
Power-supply voltage(1)	VCI,VCCIO	V	-0.3 to +3.6	1,2
Power-supply voltage(2)	VCI-AGND	V	-0.3 to +3.6	1,3
Power-supply voltage(3)	AVDD-AGND	V	-0.3 to +6.0	1,4
Power-supply voltage(4)	VGH-VGL	V	-0.3 to +30.0	1,4
Power-supply voltage(5)	AGND-VGL	V	+3.0 to +13.0	1,7
Power-supply voltage(6)	AVDD-VGL	V	+4.0 to +19.0	1,5
Power-supply voltage(7)	VCI-VGL	V	+3.0 to + 16.8	1,7
Input voltage	Vt	V	-0.3 to 3.9	1
Operating temperature	Topr	℃	-40 to +85	1
Storage temperature	Tstg	℃	-55 to +110	1

10.2 DC Characteristic

VCI = 2.5 ~ 3.3V, VCCIO = 1.65~3.6V, Ta = -40 ~ 85 °C

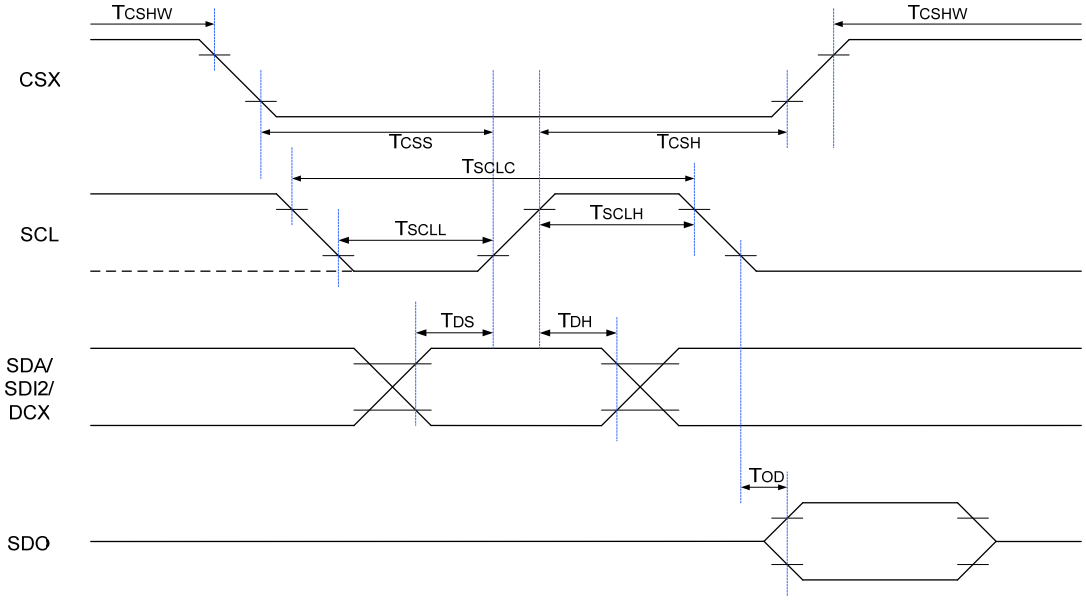
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VCCIO = 1.65V ~ 3.6 V	0.8* VCCIO	-	VCCIO	2,3
Input low voltage	V_{IL}	V	VCCIO = 1.65V ~ 3.6 V	– 0.3V	-	0.2* VCCIO	2,3
Output high voltage (D0-17 pins, FMARK)	V_{OH}	V	IOH = -0.1mA	0.8 * VCCIO	-	-	2
Output low voltage (D0-17 pins, FMARK)	V_{OL}	V	VCCIO = 1.65 ~ 3.6 V I_{OL} = 0.1mA	-	-	0.2* VCCIO	2
I/O leak current	Ili	µA	Vin = 0 ~ VCCIO	-1	-	1	4
Current consumption during normal operation (VCI-AGND)+(VCCIO-GND)	IOP(VCI)	mA	VCCIO=VCI=2.8V, Ta=25C, Fosc=6MHZ(320 Line)GRAM data =0000h, Frame rate=70HZ, REV=0, SAP=100,AP=100,DC0 =000,DC1=010,B/C=0, VC=001,VRH=0011, VCM=10011,VDV=100 00,VCOMG=1,CL=0, NO panel load	-	TBD	-	
Current consumption during standby operation (VCI-AGND)+(VCCIO-GND)	IOP(VCI)	µA		-	45		5,6

Notes:

1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI within the electrical characteristics conditions in normal operation. Exposure to a condition not within the electrical characteristics may affect reliability of the device.
2. Make sure VCI (high) ≥ GND (low) and VCCIO (high) ≥ GND (low).
3. Make sure VCI (high) ≥ AGND (low).
4. Make sure AVDD (high) ≥ AGND (low).
5. Make sure AVDD (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ AGND (low).
7. Make sure AGND (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

10.3 AC Characteristics

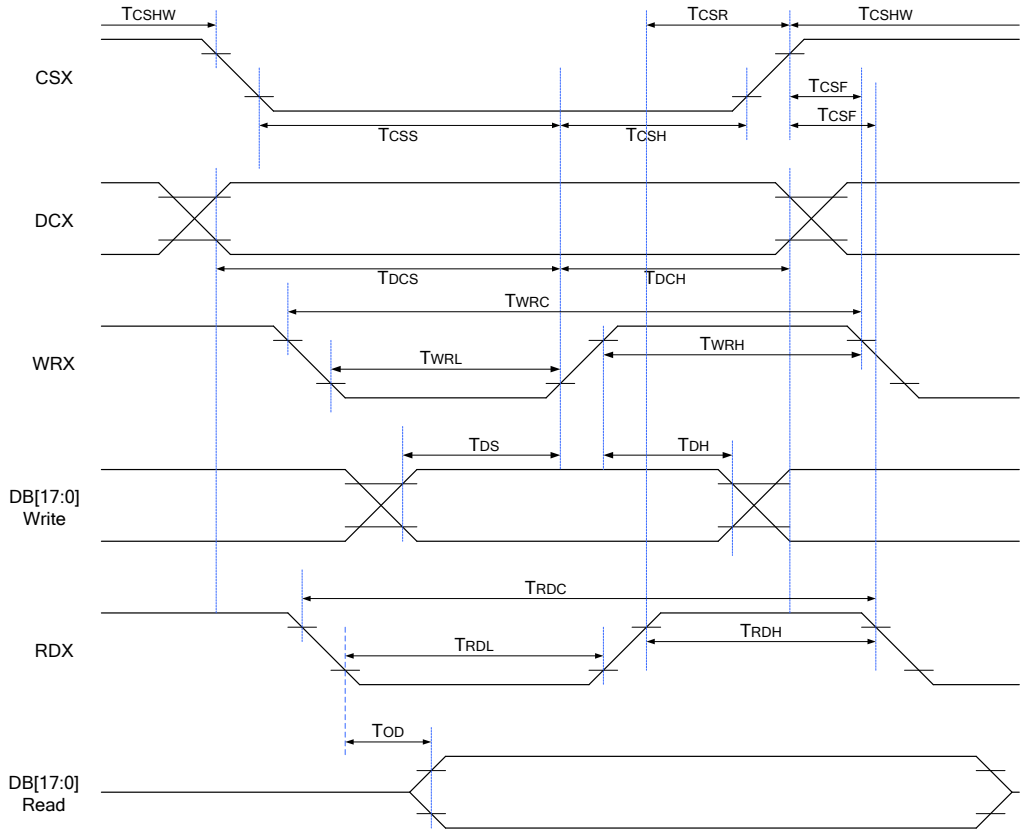
10.3.1 Serial Interface Timing Characteristics (3/4-wire SPI system)



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	7.7	-	ns	Write
	T_{CSH}	CSX hold time	7.7	-	ns	
	T_{CSHW}	CSX high level width	15.4	-	ns	
	T_{CSS}	CSX setup time	40	-	ns	Read
	T_{CSH}	CSX hold time	40	-	ns	
	T_{CSHW}	CSX high level width	80	-	ns	
SCL	T_{SCLC}	SCL cycle	15.4	-	ns	Write
	T_{SCLS}	SCL low pulse duration	6.16	-	ns	
	T_{SCLH}	SCL high pulse duration	6.16	-	ns	
	T_{SCLC}	SCL cycle	80	-	ns	Read
	T_{SCLS}	SCL low pulse duration	32	-	ns	
	T_{SCLH}	SCL high pulse duration	32	-	ns	
SDA/ SDI2/ DCX	T_{DS}	SDA/SDI2/DCX setup time	6.16	-	ns	Write
	T_{DH}	SDA/SDI2/DCX hold time	6.16	-	ns	
SDO	T_{OD}	Read data output dealy	-	24	ns	Read

Note: Ta=-30℃~70℃, VCCIO=1.65V to 3.6V, VCI=2.5V to 3.3V, AGND=DGND=0V.

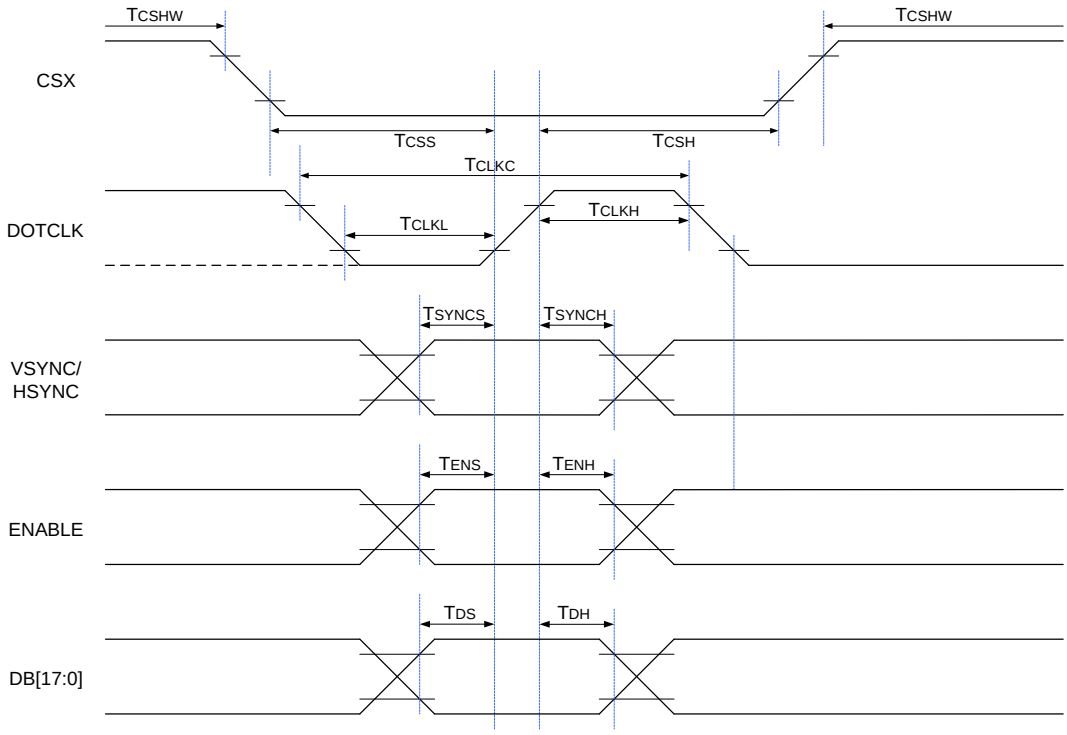
10.3.2 Parallel Interface Timing Characteristics(8080 series 8/9/16/18-Bit Parallel Interface)



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	15	-	ns	
	T_{CSH}	CSX hold time	15	-	ns	
	T_{CSF}	CSX falling edge before WRX/RDX falling edge	10	-	ns	
	T_{CSHW}	CSX high level width	0	-	ns	
	T_{CSR}	CSX rising edge after RDX rising edge	0	-	ns	
DCX	T_{DCS}	DCX setup time	10	-	ns	
	T_{DCH}	DCX hold time	10	-	ns	
WRX	T_{WRC}	WRX cycle	30	-	ns	
	T_{WRL}	WRX low pulse duration	10	-	ns	
	T_{WRH}	WRX high pulse duration	10	-	ns	
DB[17:0]	T_{DS}	Write data setup time	10	-	ns	Write
	T_{DH}	Write data hold time	10	-	ns	
RDX	T_{RDC}	RDX cycle	160	-	ns	
	T_{RDL}	RDX low pulse duration	48	-	ns	
	T_{RDH}	RDX high pulse duration	48	-	ns	
DB[17:0]	T_{OD}	Read data output delay	-	30	ns	Read

Note: Ta=-30℃~70℃, VCCIO=1.65V to 3.6V, VCI=2.5V to 3.3V, AGND=DGND=0V.

10.3.3 RGB Interface Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	16	-	ns	
	T_{CSH}	CSX hold time	16	-	ns	
	T_{CSHW}	CSX high level width	0	-	ns	
DOTCLK	T_{CLKC}	DOTCLK cycle	40	-	ns	
	T_{CLKL}	DOTCLK low pulse duration	16	-	ns	
	T_{CLKH}	DOTCLK high pulse duration	16	-	ns	
HSYNC/ VSYNC	T_{SYNCS}	HSYNC/VSYNC setup time	16	-	ns	
	T_{SYNCH}	HSYNC/VSYNC hold time	16	-	ns	
ENABLE	T_{ENS}	ENABLE setup time	16	-	ns	
	T_{ENH}	ENABLE hold time	16	-	ns	
DB[17:0]	T_{DS}	RGB data setup time	16	-	ns	
	T_{DH}	RGB data hold time	16	-	ns	

Note: Ta=-30℃~70℃, VCCIO=1.65V to 3.6V, VCI=2.5V to 3.3V, AGND=DGND=0V.

Revision history

Version No.	Date	Page	Introduction
0.1	2017-6-27	All	New build.
1.0	2017-8-25	P11	Update DB[0-17] pin description.
		P96	Change “bypass_mode”description in “B0h” register.
		P123	Update SRAM write mode drawing.