NV9510/12

HFQR Flyback Controller IC

Features

High Frequency QR Controller

- High efficiency across universal input and full load range by hybrid QR and CCM operation
- Wide VDD operating range from 6.5V to 78.5V
- Frequency hopping for better EMI performance
- Ultra-low standby power consumption (<20mW)
- Integrated over-voltage protection (OVP), under-voltage protection (UVP) and over-temperature protection (OTP)
- Adjustable thermal shut-down (SD) protection through external NTC thermistor
- Brown-in and brown-out protection
- Integrated high voltage (HV) startup & X-cap discharge
- Limit Power Source (LPS) with Power & Current Limit
- Cycle-by-cycle current limit (VCS_LIM)
- Current Sense Short Protection (CSSP)
- Secondary side diode short protection (SSSP)
- External depletion MOSFET startup (NV9512)
- Accurate auto-restart / latch / long auto-restart modes

High Power Density

- > 1W/cc achievable power density
- Small transformer size
- Low component count

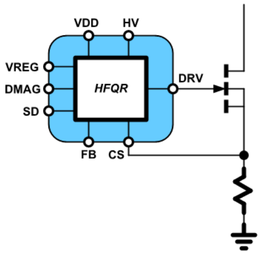
Product Reliability

- 20-year limited product warranty

Topologies / Applications

- USB PD/QC battery charger for portable devices
- High-efficiency AC/DC power adapter
- Power supply with fixed or variable output voltage

SOIC-10 Package



Simplified Schematic

Description

The NV9510/12 IC family are HFQR Flyback controllers that enable high-frequency operation, wide VDD range, high-voltage start-up, and multi-mode operation. The NV9510 IC family includes short-circuit, over-temperature and LPS protection features to make the devices well suited for a best-in-class reliable system with ultra-low part-count BOM. The devices, with less than 20mW standby power, are optimized for high power density AC/DC power supplies. The NV9510 IC family supports a wide VDD operating range to cover variable output applications with USB-PD/PPS and DP/DN protocol communication. Small footprint SOIC-10 packaging enables designers to achieve simple, quick and reliable solutions. Navitas' GaN IC and controller technologies enable high frequencies, high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

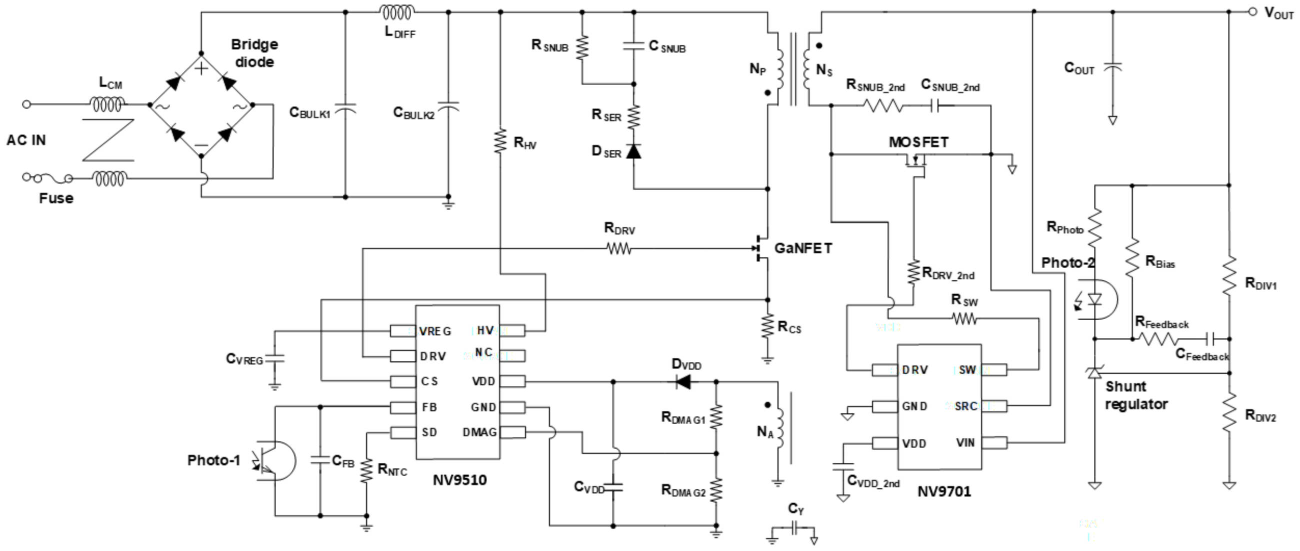


Figure 1. NV9510 Simplified HFQR Flyback Circuit Diagram

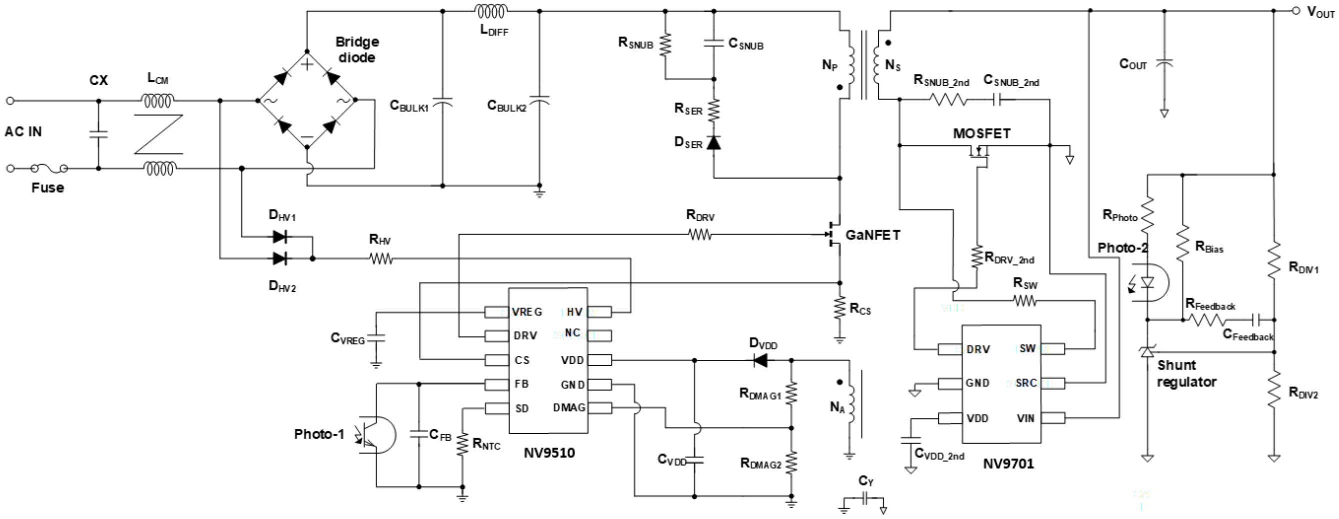


Figure 2. NV9510 Simplified Application Diagram (with X-cap Discharge Function)

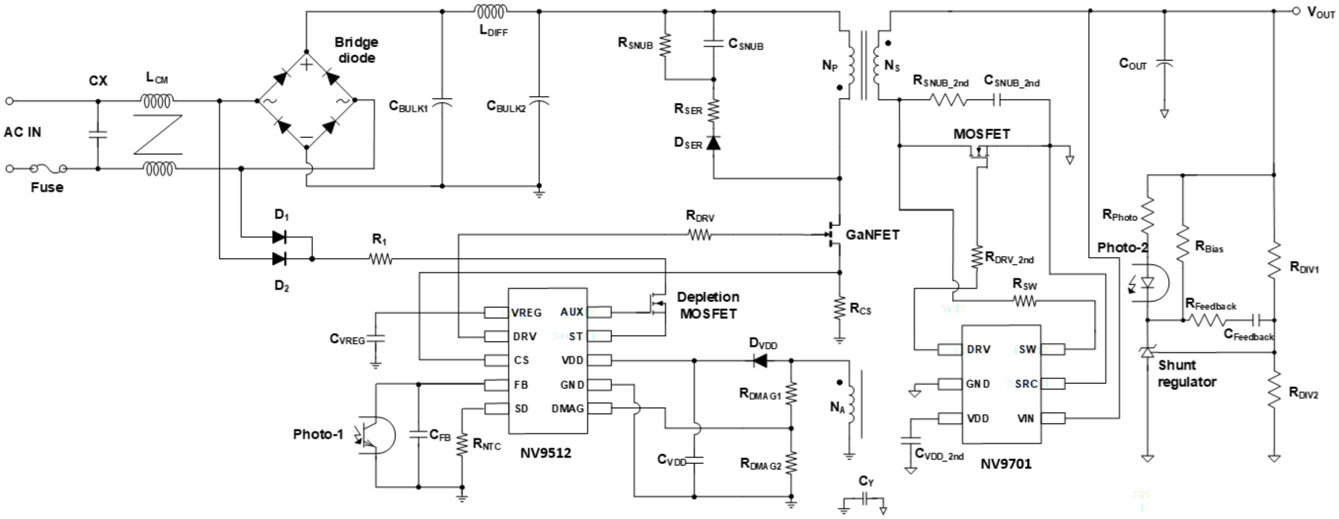


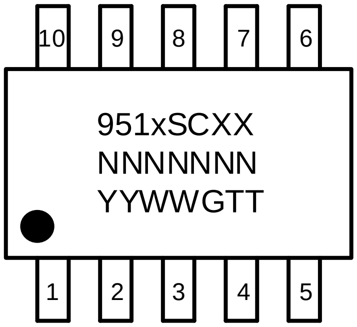
Figure 3. NV9512 Simplified Application Diagram

Ordering Information

Part Number	$f_{S\_BNK\_MAX}$	Key Function Descript	Operating Temperature Range	Package	Packing Method
NV9510SC02	129kHz	CCM / CC / GaNFET	-40°C to +125°C	10-Lead, SOIC	4K/Tape & Reel
NV9510SC06	129kHz	QR / PL+CC / GaNFET			
NV9510SC07	82kHz	CCM / CC / MOSFET			
NV9510SC14	225kHz	QR / PL+CC / MOSFET			
NV9510SC21	129kHz	QR / PL+CC / GaNFET / X-cap			
NV9512SC05	82kHz	CCM / CC / MOSFET			

**PL: Power Limit, CC: Constant Current (Current Limit)*

Pin Configuration and Marking Diagram



Symbol	Content
x	Device Code, 0=NV9510; 2=NV9512
SC	Package Code, SC=SOIC
XX	Trim Option Code
NNNNNNN	Lot Number
YY	Year Code
WW	Week Code
G	Manufacture Code
TT	Trace Code

Figure 4. Pin Configuration (Top View)

Pin Names and Descriptions

Pin No.	Name	Description
1	VDD	**Power Supply.** IC operation current is supplied through this pin. Typically, this pin is connected to external V_{DD} capacitor. The device starts to operate when V_{DD} exceeds 13.5V.
2	FB	**Feedback.** Input for the internal PWM comparator.
3	SD	**Shut Down.** Typically, this pin is connected to a NTC thermistor. The device enters the fault mode if the voltage on this pin is pulled below the fault thresholds.
4	GND	**Ground.**
5	DMAG	**Demagnetization Sense.** This pin is used to detect resonant valleys for QR switching. It also detects the output voltage information, as well as the input voltage information for Brown-in & Brown-out protection.
6	CS	**Current Sense.** This pin detects the GaN FET or MOSFET current cycle by cycle when connected to a current-sense resistor.
7	DRV	**Gate Drive Output.** This pin is connected to the gate to drive GaN FET or MOSFET.
8	VREG	**LDO Output.** Typically, this pin is connected to an external capacitor.
9	NC (NV9510)	**Not Connect.**
	AUX (NV9512)	**Auxiliary Control.** This pin is connected to gate of external depletion MOSFET.
10	HV (NV9510)	**High Voltage Startup.** This pin is the input for the high voltage startup. It can connect to X-cap for X-cap discharge function.
	ST (NV9512)	**High Voltage Startup.** This pin is connected to depletion MOSFET source terminal for current path to VDD.

Internal Functional Block Diagram

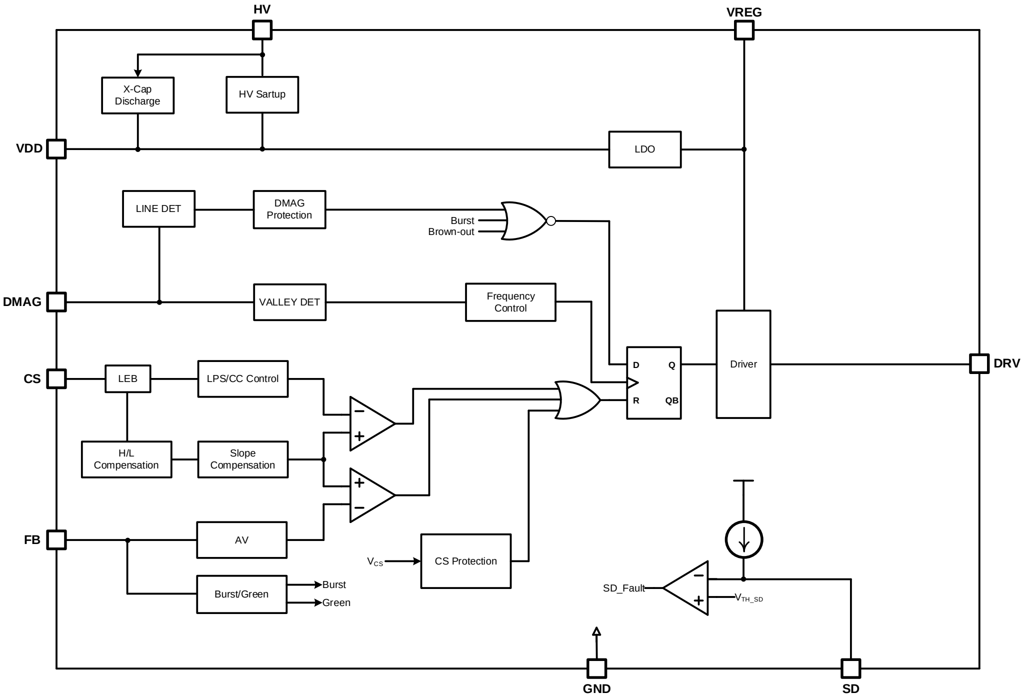


Figure 5. NV9510 Internal Function Block Diagram

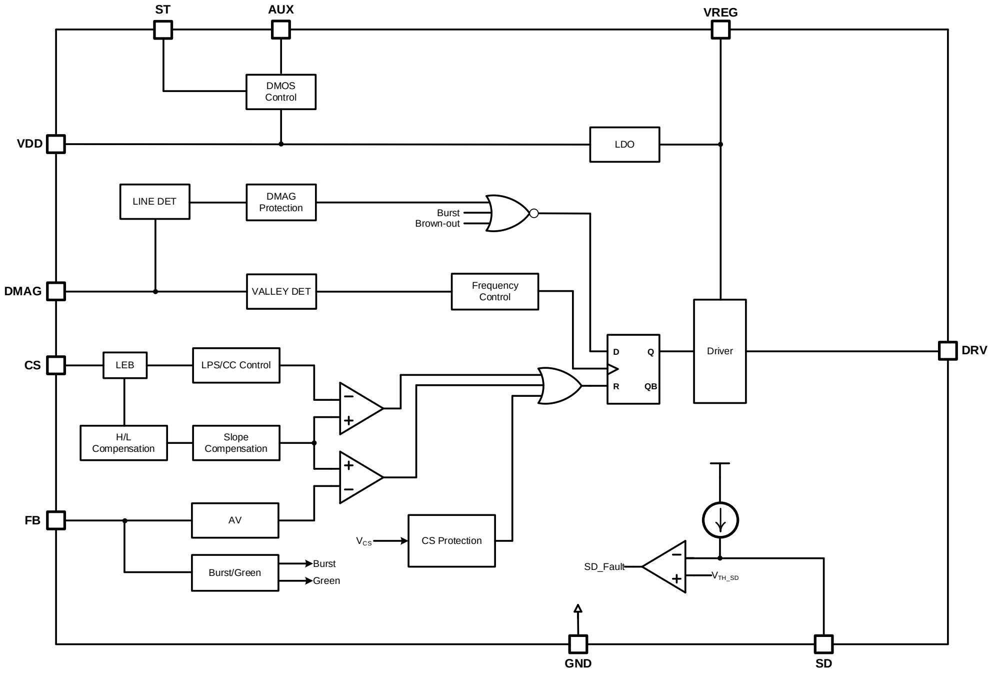


Figure 6. NV9512 Internal Function Block Diagram

Electrical Characteristics

Absolute Maximum Ratings (1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>V_{HV}</td><td colspan="2">HV Pin Input Voltage</td><td>-0.3</td><td>700</td><td>V</td></tr>
<tr><td>V_{AUX}</td><td colspan="2">AUX Pin Input Voltage</td><td>-0.3</td><td>30</td><td>V</td></tr>
<tr><td>V_{ST}</td><td colspan="2">ST Pin Input Voltage</td><td>-0.3</td><td>30</td><td>V</td></tr>
<tr><td>V_{VDD}</td><td colspan="2">VDD DC Supply Voltage</td><td>-0.3</td><td>80</td><td>V</td></tr>
<tr><td>V_{DRV}</td><td colspan="2">DRV Pin Output Voltage</td><td>-0.3</td><td>12</td><td>V</td></tr>
<tr><td>V_{CS}</td><td colspan="2">CS Pin Input Voltage</td><td>-0.3</td><td>5.5</td><td>V</td></tr>
<tr><td>V_{FB}</td><td colspan="2">FB Pin Input Voltage</td><td>-0.3</td><td>5.5</td><td>V</td></tr>
<tr><td>V_{DMAG}</td><td colspan="2">DMAG Pin Input Voltage</td><td>-0.3</td><td>5.5</td><td>V</td></tr>
<tr><td>V_{SD}</td><td colspan="2">SD Pin Input Voltage</td><td>-0.3</td><td>5.5</td><td>V</td></tr>
<tr><td>V_{REG}</td><td colspan="2">VREG Pin Output Voltage</td><td>-0.3</td><td>7</td><td>V</td></tr>
<tr><td>θ_{JA}</td><td colspan="2">Thermal Resistance (Junction-to-Ambient) SOIC-10</td><td>-</td><td>158.3</td><td>°C/W</td></tr>
<tr><td>θ_{JC}</td><td colspan="2">Thermal Resistance (Junction-to-Case) SOIC-10</td><td>-</td><td>95.6</td><td>°C/W</td></tr>
<tr><td>T_J</td><td colspan="2">Operating Junction Temperature</td><td>-40</td><td>150</td><td>°C</td></tr>
<tr><td>T_{STG}</td><td colspan="2">Storage Temperature Range</td><td>-40</td><td>150</td><td>°C</td></tr>
<tr><td>T_L</td><td colspan="2">Lead Temperature (Soldering) 10 Seconds</td><td>-</td><td>260</td><td>°C</td></tr>
<tr><td rowspan="2">ESD</td><td rowspan="2">Electrostatic Discharge Capability</td><td>Human Body Mode, ANSI/ESDA/JEDEC JS-001-2017 (Including All Pin)</td><td>-</td><td>2.0</td><td>kV</td></tr>
<tr><td>Charge Device Mode, ANSI/ESDA/JEDEC JS-001-2018</td><td>-</td><td>2.0</td><td>kV</td></tr>
</table>

Notes (1):

- *Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.*

Recommended Operating Conditions (2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Elevation does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{HV}	HV Pin Supply Voltage	-0.3	-	450	V
V_{VDD}	VDD Pin Supply Voltage	-0.3	-	75	V
V_{CS}	CS Pin Supply Voltage	-0.3	-	5	V
V_{FB}	FB Pin Supply Voltage	-0.3	-	5	V
V_{DMAG}	DMAG Pin Supply Voltage	-0.3	-	5	V
V_{SD}	SD Pin Supply Voltage	-0.3	-	5	V

Notes (2):

- *Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40°C to +125°C unless otherwise noted.*

Electrical Specifications

V_{DD} (Typ.) = 12V, T_A =-40°C to 125°C, and T_A (Typ.) =25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Type.	Max.	Unit
HV Section (NV9510)						
I_{HV}	Supply Current Drawn from HV Pin	V_{HV}=120V, V_{DD}=0V	5	-	20	mA
I_{HV_LC}	Leakage Current Drawn from HV Pin	V_{HV}=700V, V_{DD}=V_{DD_UVLO}+1V	-	-	3	μA
$t_{HV\_LINE\_Removal}$	Timer Duration for No Line Detection	X-cap Discharge Function	-	30	-	ms
t_{HV_DIS}	Discharge Timer Duration	X-cap Discharge Function	-	312	-	ms
VDD Section						
V_{DD_ON}	V_{DD} Turn-On Threshold Voltage	V_{DD} Rising	12.0	13.5	15.0	V
V_{DD_UVLO}	V_{DD} UVLO Threshold Voltage		6.2	6.5	6.8	V
I_{DD_ST}	Startup Current		0.5	2	5	μA
I_{DD_OP}	Operating Supply Current	No DRV Switching	0.40	0.65	0.90	mA
I_{DD_DPGN}	Operating Supply Current in Deep Green-Mode		200	300	400	μA
t_{D_DPGN}	Debounce Time to Enter Deep Green Mode		380	480	580	μs
V_{DD_OVP} (3)	V_{DD} Over-Voltage-Protection Threshold		77	78.5	-	V
t_{D_UVLO} (3)	UVLO De-bounce Time		-	10	-	μs
$t_{D\_VDD\_OVP}$ (3)	V_{DD} Over-Voltage-Protection De-bounce Time		-	32	-	μs
t_{VDD_LAR}	Long Auto-Restart Mode Time	Trim Option	2.08	2.64	3.20	s

Electrical Specifications

V_{DD} (Typ.) = 12V, T_A =-40°C to 125°C, and T_A (Typ.) =25°C, unless otherwise specified.

Parameter		**Test Conditions**	**Min.**	**Type.**	**Max.**	**Unit**
VREG Section						
V_{REG} (3)	VREG output voltage	GaNFET	-	6.25	-	V
		MOSFET	-	12	-	V
V_{REG_5mA} (3)	VREG with 5mA Load Current	I_{OUT} = 5mA	5.85	-	-	V
Oscillator Section						
$f_{S\_BNK\_MAX\_LL}$	Maximum Blanking Frequency at Low Line Input Voltage	$f_{S\_BNK\_MAX}$ = 82kHz	77	82	87	kHz
		$f_{S\_BNK\_MAX}$ = 129kHz	121	129	137	kHz
		$f_{S\_BNK\_MAX}$ = 225kHz	202	225	248	kHz
$f_{S\_BNK\_MAX\_HL}$	Maximum Blanking Frequency at High Line Input Voltage	$f_{S\_BNK\_MAX}$ = 82kHz	62	67	72	kHz
		$f_{S\_BNK\_MAX}$ = 129kHz	93	100	107	kHz
		$f_{S\_BNK\_MAX}$ = 225kHz	147	164	182	kHz
$f_{S\_BNK\_MAX\_CCM}$	Maximum Blanking Frequency in CCM	$f_{S\_BNK\_MAX}$ = 82kHz	62	67	72	kHz
		$f_{S\_BNK\_MAX}$ = 129kHz	93	100	107	kHz
f_{S_TMO}	Minimum Time-Out PWM Frequency		23	25	27	kHz
t_{ON_MAX}	Maximum PWM ON Time	$f_{S\_BNK\_MAX}$ = 82kHz & 129kHz	16.0	17.7	19.4	µs
		$f_{S\_BNK\_MAX}$ = 225kHz	9.5	10.5	11.5	µs
D_{MAX}	Maximum Duty Cycle		72	75	78	%
m_{slp} (3)	Slope Compensation		-	60	-	mv/µs
ΔV_{JIT} (3)	Current Sense Jitter Range	Except NV9510SC14	-	5.0	-	%
		NV9510SC14	-	10.0	-	%
T_{JIT}	Frequency Jitter Period		2.22	2.56	2.90	ms
Feedback Section						
V_{FB_OPEN}	FB Open Voltage		-	5.05	-	V
Z_{FB}	FB Pull Up Resistor		36	42	48	kΩ
A_{V_HV} (3)	FB Voltage Attenuation Factor at High Output Voltage	$f_{S\_BNK\_MAX}$ = 82kHz & 129kHz (V_{DMAG} > 1.75V)	-	0.225	-	V/V
A_{V_LV} (3)	FB Voltage Attenuation Factor at Low Output Voltage	$f_{S\_BNK\_MAX}$ = 82kHz & 129kHz (V_{DMAG}< 1.6V)	-	0.200	-	V/V
A_V (3)	FB Voltage Attenuation Factor	$f_{S\_BNK\_MAX}$ = 225kHz	-	0.175	-	V/V
$V_{FB\_BST\_ENT}$	FB Threshold for Burst Mode Entry		0.50	0.55	0.60	V
$V_{FB\_BST\_EXT}$	FB Threshold for Burst Mode Exit		0.55	0.60	0.65	V
$V_{FB\_BNK\_STR}$	Frequency Foldback Start Point	$f_{S\_BNK\_MAX}$ = 82kHz & 129kHz	-	2.300	-	V
		$f_{S\_BNK\_MAX}$ = 225kHz	-	2.563	-	V
$V_{FB\_BNK\_END\_L}$	Frequency Foldback End Point at Low Line Input Voltage	$f_{S\_BNK\_MAX}$ = 82kHz	-	1.519	-	V
		$f_{S\_BNK\_MAX}$ = 129kHz	-	1.394	-	V
		$f_{S\_BNK\_MAX}$ = 225kHz	-	1.313	-	V

Electrical Specifications

V_{DD} (Typ.) = 12V, T_A =-40°C to 125°C, and T_A (Typ.) =25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Type.	Max.	Unit
Feedback Section (Cont.)						
$V_{FB\_BNK\_END\_H}$	Frequency Foldback End Point at High Line Input Voltage	$f_{S\_BNK\_MAX}$ = 82kHz	-	1.597	-	V
		$f_{S\_BNK\_MAX}$ = 129kHz	-	1.456	-	V
		$f_{S\_BNK\_MAX}$ = 225kHz	-	1.372	-	V
$V_{FB\_CSMIN\_H}$ (3)	V_{CS_MIN} Foldback High Threshold Voltage	$f_{S\_BNK\_MAX}$ = 225kHz	-	1.500	-	V
$V_{FB\_CSMIN\_L}$ (3)	V_{CS_MIN} Foldback Low Threshold Voltage	$f_{S\_BNK\_MAX}$ = 225kHz	-	0.750	-	V
DMAG Section						
I_{DMAG_BRI}	Current Threshold for Brown-In		0.43	0.48	0.53	mA
N_{BRI} (3)	Debounce Cycle for Brown-In		-	4	-	Cycle
I_{DMAG_BRO}	Current Threshold for Brown-Out		0.31	0.36	0.41	mA
t_{D_BRO} (3)	Debounce Cycle for Brown-Out		-	16.5	-	ms
I_{DMAG_HL} (3)	Current Threshold for High Line		-	1.16	-	mA
N_{HL_ENT} (3)	Debounce Cycle for High Line Entry		-	4	-	Cycle
I_{DMAG_LL} (3)	Current Threshold for Low Line		-	1.04	-	mA
$t_{D\_LL\_ENT}$ (3)	Debounce Cycle for Low Line Entry		-	16.5	-	ms
$t_{DMAG\_BNK\_L}$ (3)	DMAG Sampling Blanking Time	(V_{FB} < 1.5V)	-	1.10	-	µs
$t_{DMAG\_BNK\_M}$ (3)	DMAG Sampling Blanking Time	(V_{FB} > 1.6V)	-	1.65	-	µs
V_{DMAG_HV}	V_{DMAG} Threshold for High Output		1.35	1.45	1.55	V
$V_{DMAG\_LV\_HYS}$ (3)	V_{DMAG} Hysteresis Threshold for Low Output		-	0.15	-	V
V_{DMAG_UVP}	V_{DMAG} Under-Voltage-Protection Threshold		0.350	0.425	0.500	V
N_{DMAG_UVP} (3)	Debounce Cycle for V_{DMAG_UVP}		-	4	-	Cycle
$t_{VDMAG\_UVP\_BNK}$	V_{DMAG_UVP} Blanking Time during Start-up		25	32	36	ms
V_{DMAG_OVP}	V_{DMAG} Over-Voltage-Protection Threshold		3.45	3.55	3.65	V
N_{DMAG_OVP} (3)	Debounce Cycle for V_{DMAG_OVP}		-	4	-	Cycle

Electrical Specifications

V_{DD} (Typ.) = 12V, T_A =-40°C to 125°C, and T_A (Typ.) =25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Type.	Max.	Unit
Current Sense Section						
V_{CS_LIM}	Maximum Current Sense Limit		0.620	0.650	0.680	V
$V_{CS\_MIN\_H}$	Minimum Current Sense Limit at High Output Voltage		0.195	0.225	0.255	V
$V_{CS\_MIN\_L}$	Minimum Current Sense Limit at Low Output Voltage		0.145	0.175	0.205	V
$V_{CS\_MIN\_FB\_STR\_LL\_H}$ (3)	Feedback of V_{CS_MIN} Foldback Start Point at Low Line and High Output Voltage	$f_{S\_BNK\_MAX}$ = 225kHz	-	0.425	-	V
$V_{CS\_MIN\_FB\_STR\_LL\_L}$ (3)	Feedback of V_{CS_MIN} Foldback Start Point at Low Line and Low Output Voltage	$f_{S\_BNK\_MAX}$ = 225kHz	-	0.375	-	V
$V_{CS\_MIN\_FB\_STR\_HL\_H}$ (3)	Feedback of V_{CS_MIN} Foldback Start Point at High Line and High Output Voltage	$f_{S\_BNK\_MAX}$ = 225kHz	-	0.525	-	V
$V_{CS\_MIN\_FB\_STR\_HL\_L}$ (3)	Feedback of V_{CS_MIN} Foldback Start Point at High Line and Low Output Voltage	$f_{S\_BNK\_MAX}$ = 225kHz	-	0.475	-	V
t_{LEB} (3)	Leading Edge Blanking Time	T_A =25°C	-	295	-	ns
t_{PD} (3)	Propagation Delay		-	50	-	ns
V_{CSSP}	CS Threshold for CS Short Circuit Protection		0.12	0.15	0.18	V
$t_{D\_CSSP\_MIN}$ (3)	Debounce Time for CSSP Trigger Minimum Period		-	2.2	-	µs
V_{CS_SSSP}	CS Threshold for SSSP		1.05	1.10	1.15	V
N_{CS_SSSP} (3)	Debounce Cycle for SSSP Protection Trigger		-	2	-	Cycle
t_{D_SSSP} (3)	Debounce Time for SSSP Protection Trigger	T_A =25°C	-	200	-	ns

Electrical Specifications

V_{DD} (Typ.) = 12V, T_A =-40°C to 125°C, and T_A (Typ.) =25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Type.	Max.	Unit
Gate Driver Section						
V_{CLAMP} (3)	Driver Output Clamping Voltage	V_{REG} = 6.25V	-	6	-	V
		V_{REG} = 12V	-	8	-	V
t_{R_DRV}	Driver Output Rising time from 10% to 90%		-	65	170	ns
t_{F_DRV}	Driver Output Falling time from 90% to 10%		-	20	40	ns
Over-Temperature Protection Section						
T_{OTP} (3)	Over-Temperature-Protection Threshold		-	140	-	°C
ΔT_{OTP} (3)	Over-Temperature-Protection Hysteresis		-	20	-	°C
Shut-Down Section						
V_{TH_SD}	Threshold Voltage for Shut-Down Trigger		0.95	1.00	1.05	V
$V_{TH\_SD\_STR}$	Threshold Voltage for Shut-Down Trigger at Start-up		1.05	1.10	1.15	V
I_{SD}	SD Pin Source Current		47.5	50.0	52.5	μA
t_{D_SD}	Debounce Time for Shut-Down Trigger		280	400	520	μs

Note (3):

- *Guaranteed by design*

Typical Performance Characteristics

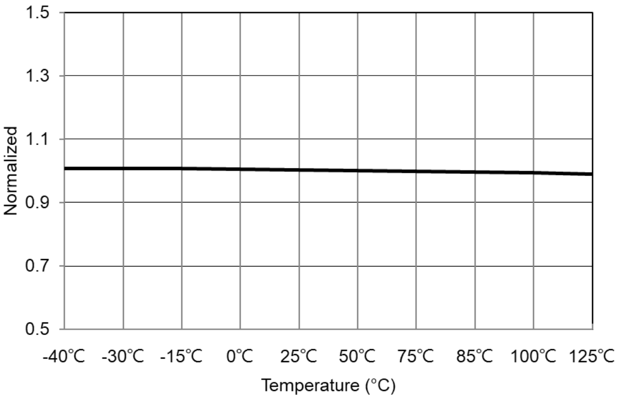


Figure 7. V_{DD_ON}

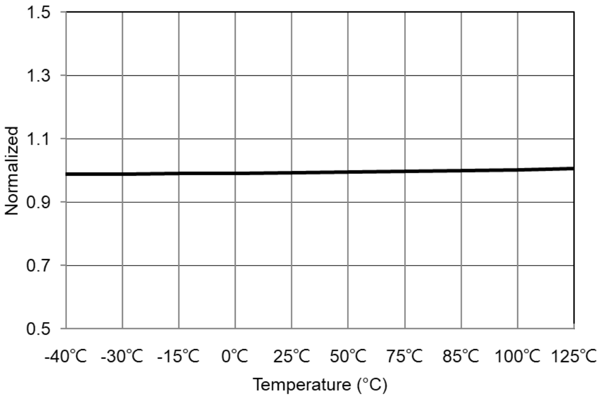


Figure 8. V_{DD_UVLO}

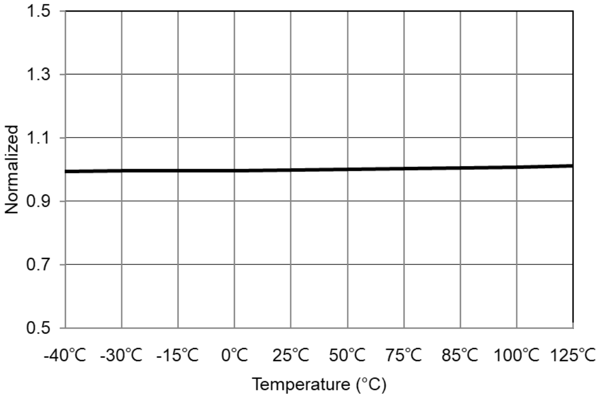


Figure 9. V_{DD_OVP}

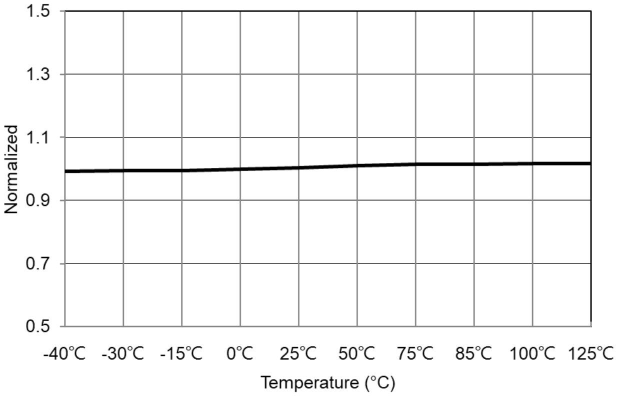


Figure 10. f_{S_TMO}

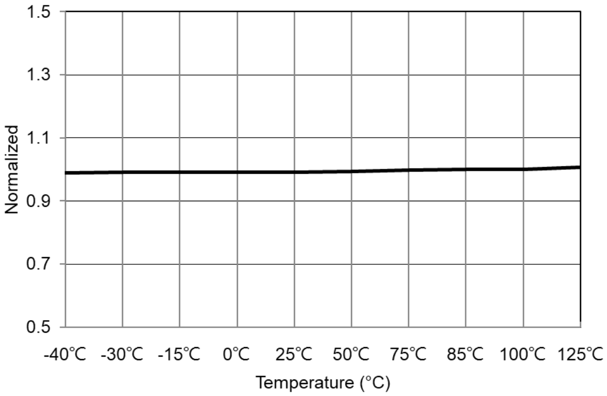


Figure 11. $V_{FB\_BST\_ENT}$

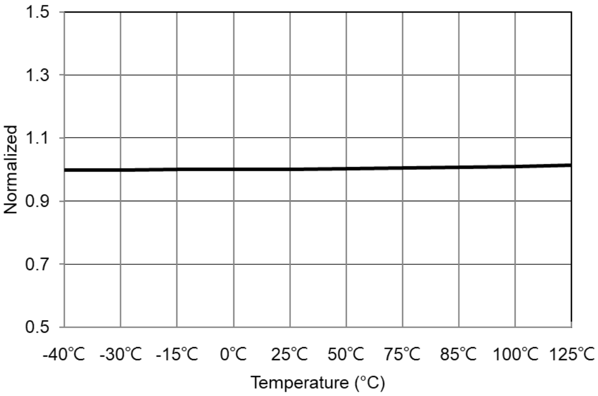


Figure 12. $V_{FB\_BST\_EXT}$

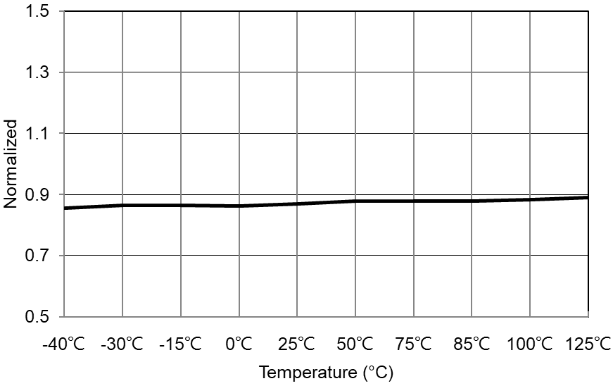


Figure 13. I_{DMAG_BRI}

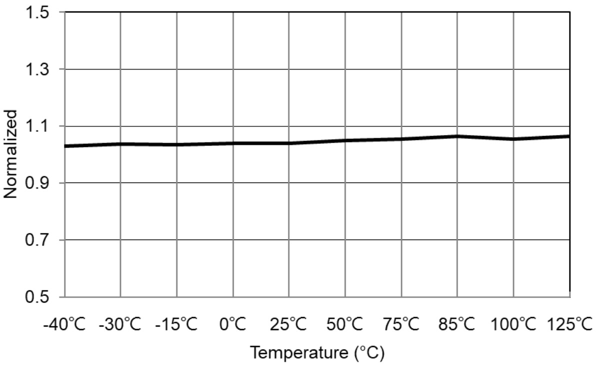


Figure 14. I_{DMAG_BRO}

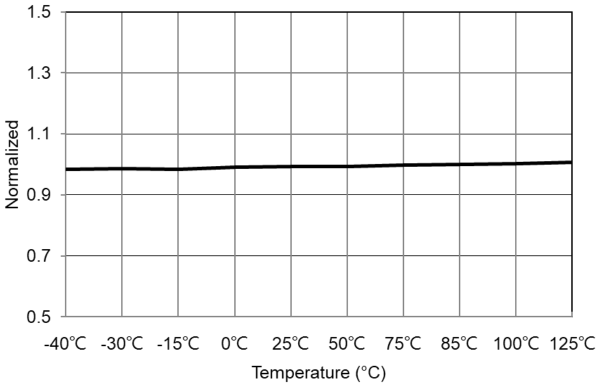


Figure 15. V_{DMAG_UVP}

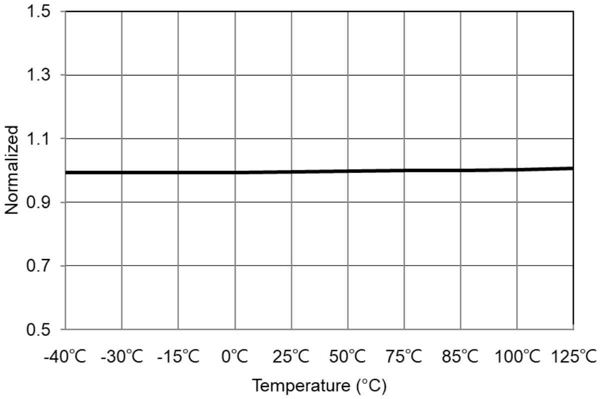


Figure 16. V_{DMAG_OVP}

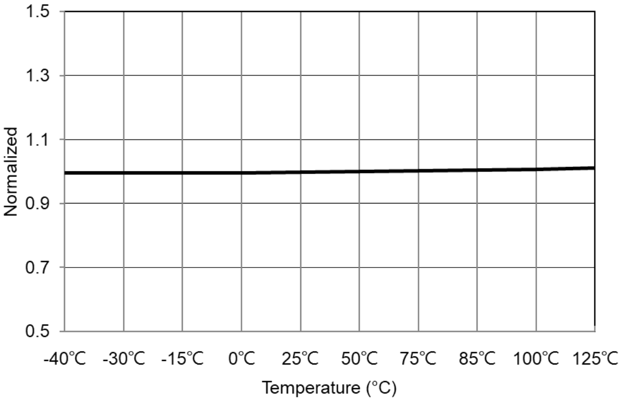


Figure 17. $V_{CS\_LIM\_H}$

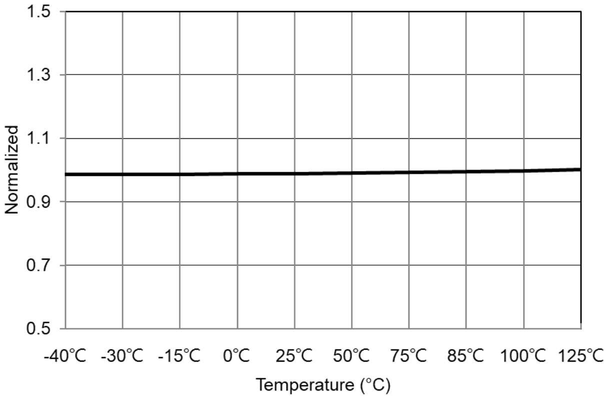


Figure 18. V_{TH_SD}

Detailed Function Description

Basic Operation

NV9510 family ICs are offline PWM Flyback regulator which operates in quasi-resonant (QR) mode to reduce switching losses and EMI (electromagnetic interference). It regulates the output based on the load condition through opto-coupler feedback circuitry.

The QR resonant frequency is determined by the the transformer magnetizing inductance (L_m) and the primary side FET effective output capacitance ($C_{oss\text{-}eff}$).

$$C_{oss-eff} = C_{oss-FET} + C_{parasitic} + C_{transformer} \quad \text{(Equation 1)}$$

$$t_{resonance} = 2\pi\sqrt{L_m \times C_{oss-eff}} \quad \text{(Equation 2)}$$

For the heavy load condition (e.g. 50%~100% of full load), the blanking time for the valley detection is fixed such that the switching time is between $1/f_{S\_BNK\_MAX\_LL(HL)}$ and $1/f_{S\_BNK\_MAX\_LL(HL)} + t_{resonance}$ as shown in Figure 19. The primary side peak current is modulated by the feedback voltage. For the medium load condition (e.g.25%~50% of full load), the blanking time is modulated as a function of load current such that the upper limit of the blanking frequency varies from $f_{S\_BNK\_MAX\_LL(HL)}$ as load decreases. The blanking frequency reduction stop point is f_{S_TMO}. For the light load condition (e.g.5%~25%), the blanking time is fixed such that the switching time is between $1/f_{S\_TMO}$ and $1/f_{S\_TMO} + t_{resonance}$ and the primary side peak current is modulated by the function of V_{CS_MIN} modulation, as shown in Figure 19.

NV9510 family ICs also have ability to operate in CCM. When the device enters CCM, the maximum blanking frequency is limited at $f_{S\_BNK\_MAX\_CCM}$.

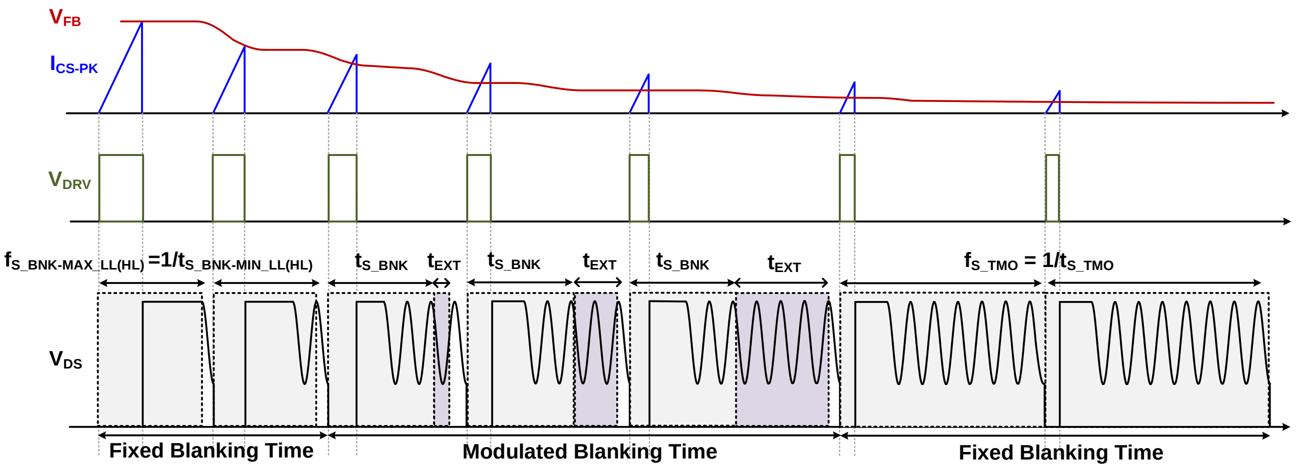


Figure 19 Frequency Fold-Back Operation

Burst Mode

As shown in Figure 20, when feedback voltage V_{FB} drops below $V_{FB\_BST\_ENT}$ at light load, the PWM output shuts off and the output voltage drops at a rate depending on the load current level. Thereafter, feedback voltage V_{FB} rises. Once V_{FB} exceeds $V_{FB\_BST\_EXT}$, NV9510 family products resume switching and the switch peak currents is limited by V_{CS_MIN}. If more power is delivered to the load than required, V_{FB} voltage will decrease. Once V_{FB} voltage is pulled below $V_{FB\_BNK\_ENT}$, switching stops again. In this manner, the burst mode operation alternately enables and disables switching of the FET to regulate the output and in the meanwhile reduce the switching losses.

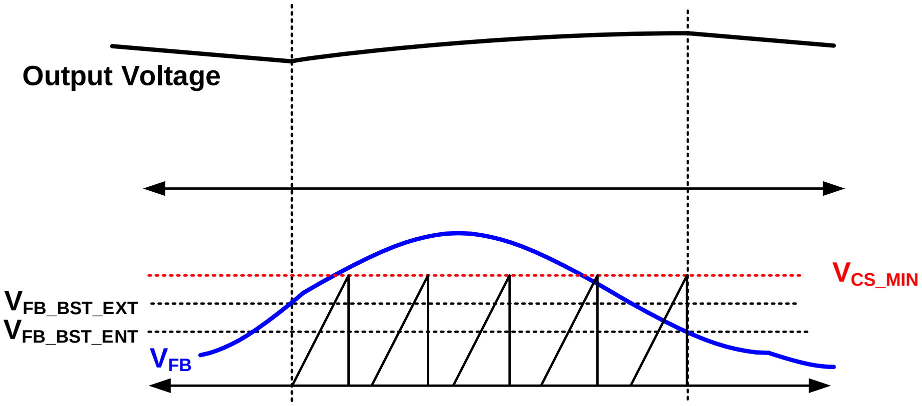


Figure 20 Burst Mode Operation

Deep Green Mode

NV9510 family ICs enter the deep green mode if V_{FB} voltage stays below $V_{FB\_BST\_ENT}$ for more than t_{D_DPGN} (480µs). In the deep green mode, the IC operating current is reduced to I_{DD_DPGN} (300µA) to minimize power consumption. IC resumes switching with normal operating current I_{DD_OP} once V_{FB} voltage rises above $V_{FB\_BST\_EXT}$.

Valley Detection

NV9510 family valley detection is achieved by monitoring V_{DMAG} voltage, which is the divided auxiliary winding voltage by R_{DMAG1} and R_{DMAG2} as shown in Figure 21. One ceramic capacitor (C_{DMAG}) less than 10 pF is recommended to filter out the noise if PCB noise coupling is observed.

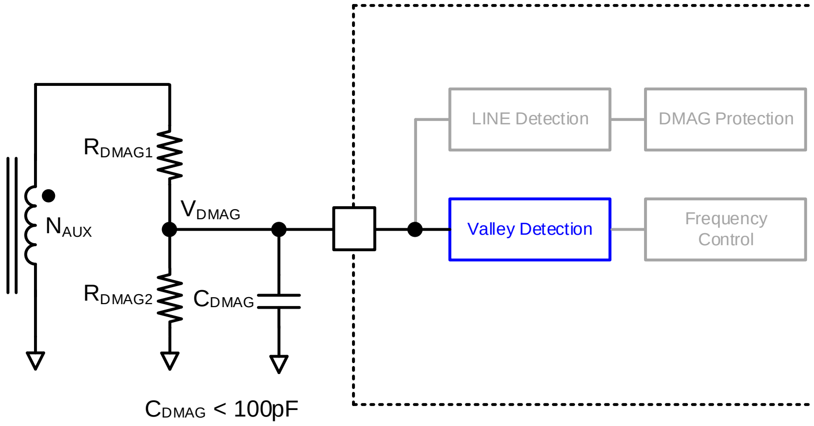


Figure 21 Valley Detection Circuit

Inherent Frequency Jitter

In flyback application, the DC ripple (∆VDC) of bulk capacitor at the low line application is larger than at the high line application as shown in Figure 22. This large DC ripple will result in switching frequency variation for a valley switched converter. The frequency variation scatters EMI noise over the nearby frequency band, allowing compliance with EMI requirement easily. Therefore, the EMI performance at the low line application is easy to comply with EMI limitation naturally. However, at the high line application, the DC ripple is relatively small and consequently the EMI performance may suffer. To maintain good EMI performance across over the universal input, a frequency jitter is implemented in the NV9510 family products.

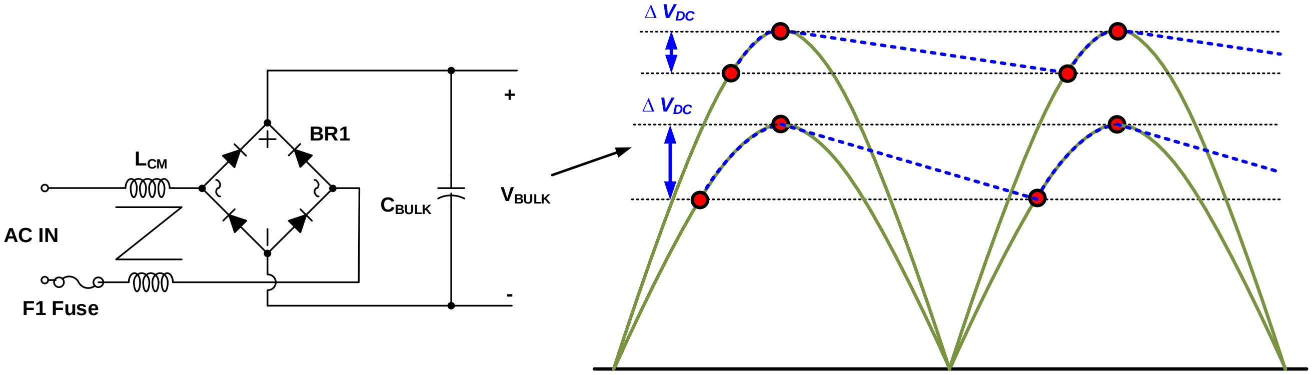


Figure 22 Inherent Frequency Jitter

Output Voltage Detection

Figure 23 shows the DMAG voltage ($V_{DMAG-S/H}$) is sampled at the end of t_{DMAG_BNK} to avoid sampling error. The DMAG voltage should be set based on the transformer turn ratio, the voltage divider resistors R_{DMAG2} & R_{DMAG1} and the specified IC parameter DMAG sampling normalization ratio, $Ratio_{DMAG}$ (0.16).

$$\mathrm{Ratio}_{\mathrm{DMAG}} = \frac{V_{\mathrm{DMAG-S/H}}}{V_O} = \frac{N_A}{N_S} \times \frac{R_{\mathrm{DMAG2}}}{R_{\mathrm{DMAG1}} + R_{\mathrm{DMAG2}}} = 0.16 \quad \text{(Equation 3)}$$

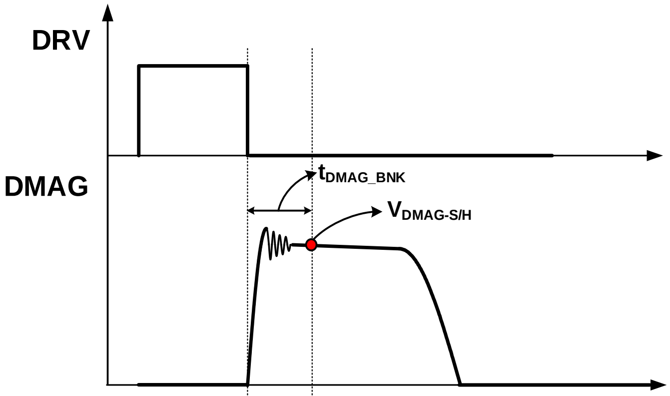


Figure 23 Output Voltage Detection

Line Voltage Detection

As illustrated in Figure 24, NV9510 family products indirectly senses the line voltage through DMAG pin during FET turn-on period. During the FET conduction time, the line voltage detector clamps DMAG pin voltage at 0V. The auxiliary winding voltage, V_{AUX}, is proportional to the input bulk capacitor voltage, V_{BLK}. So current I_{DMAG} flowing out of DMAG pin is expressed as:

$$I_{DMAG} = \frac{V_{BLK}}{R_{DMAG1}} \times \frac{N_A}{N_P} \qquad \text{(Equation 4)}$$

I_{DMAG} current, reflecting the line voltage information, is used for the brown-in and brown-out protection.

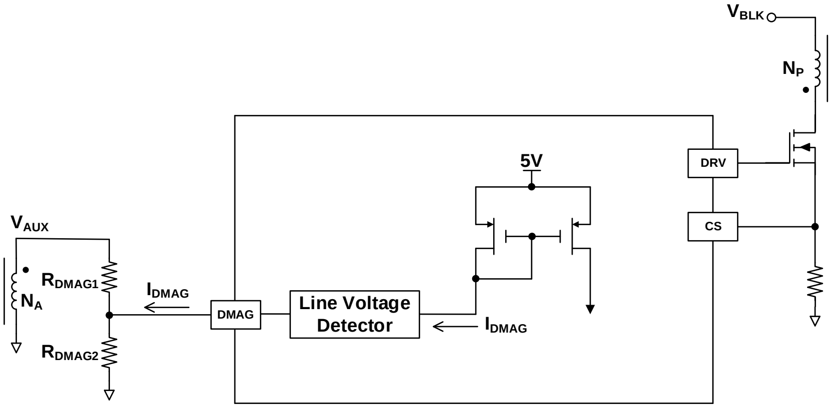


Figure 24 Line Voltage Detection Circuit

LPS Function

The NV9510 family products incorporates built-in power limit (PL) and current limit (CC) circuits to limit output power in the event of the protocol IC becoming malfunction. As Figure 25 shows, when output voltage is equal and lower than 11V, the LPS is controlled by CC; when higher than 11V, the LPS is controlled by PL and CC or CC only. The LPS can be adjusted by current sense resistance, it is recommended to have 10~15% margin.

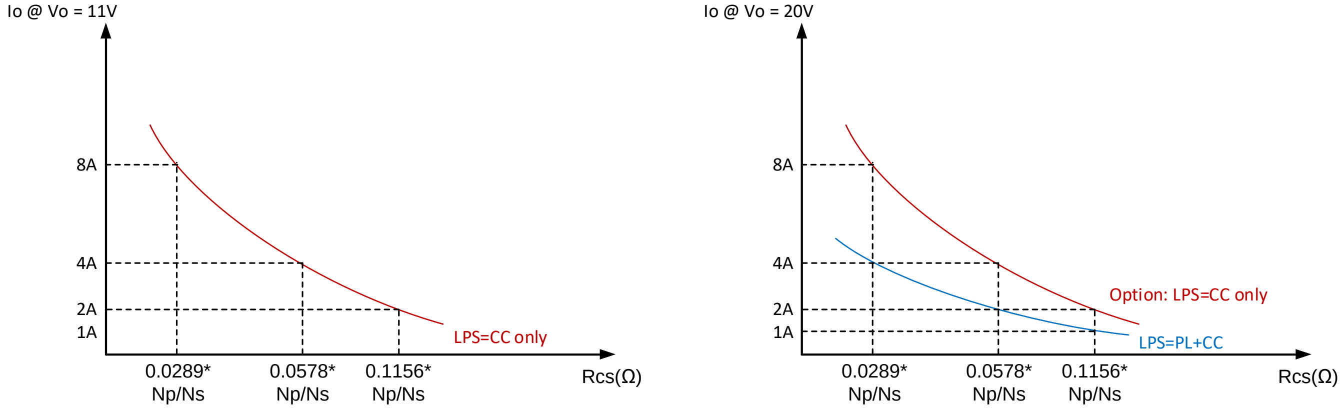


Figure 25 LPS vs. Rcs

HV Startup

During startup, the internal HV startup circuit is enabled and the bulk capacitor voltage supplies the current, I_{HV}, to charge hold-up capacitor C_{VDD} through R_{HV} (100kohm is recommended). When V_{DD} voltage reaches V_{DD_ON}, the HV startup circuit is disabled. The IC starts PWM switching and senses DMAG signal to check the brown-in condition. If the brown-in is not detected, the IC enters the auto-restart mode.

NV9510 integrates X-cap discharge function by connect one resistor from X-cap to HV pin as shown in Figure 26. The removal of line voltage (such as unplug) is detected by X-cap voltage detector. Once unplug detected, a debounce timer $t_{HV\_LINE\_Removal}$ (32ms) starts to make sure the unplug event is valid. After $t_{HV\_LINE\_Removal}$ (32ms) debounce timer, unplug event is confirmed and NV9510 enters protection. The PWM control block will be disabled, a built-in discharge path from X-cap through R_{HV} to HV pin will be enabled, and the discharge timer t_{HV_DIS} will keep 312ms to guarantee X-cap can be fully discharged.

NV9512 can use external depletion MOSFET for startup. AUX pin controls depletion MOSFET turn on and turn off, ST pin connects to source terminal of depletion MOSFET for current path to VDD. The recommended maximum rating of gate-source voltage at least ±20V.

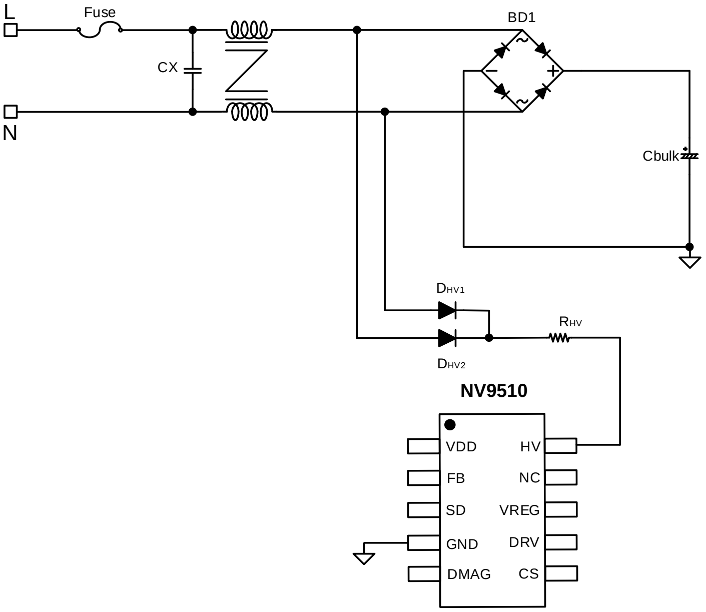


Figure 26 X-cap discharge circuit

Protection Description

NV9510 family products protection functions include VDD over-voltage protection (VDD-OVP), Brown-out protection, DMAG over-voltage protection (DMAG-OVP), DMAG under-voltage protection (DMAG-UVP), IC internal over-temperature protection (OTP), IC external thermal shut-down (SD). The brown-out protection is implemented with auto-restart mode. The VDD-OVP, DMAG-OVP and external SD protection can be configured with auto-restart or latch mode. The DMAG-UVP can be configured with auto-restart or long auto-restart mode.

When the long auto-restart mode protection is triggered, the DRV is turned off for a time period of t_{VDD_LAR} (2.64s). After t_{VDD_LAR}, if VDD rises above V_{DD_ON}, NV9510 family products resume normal operation as shown in Figure 27.

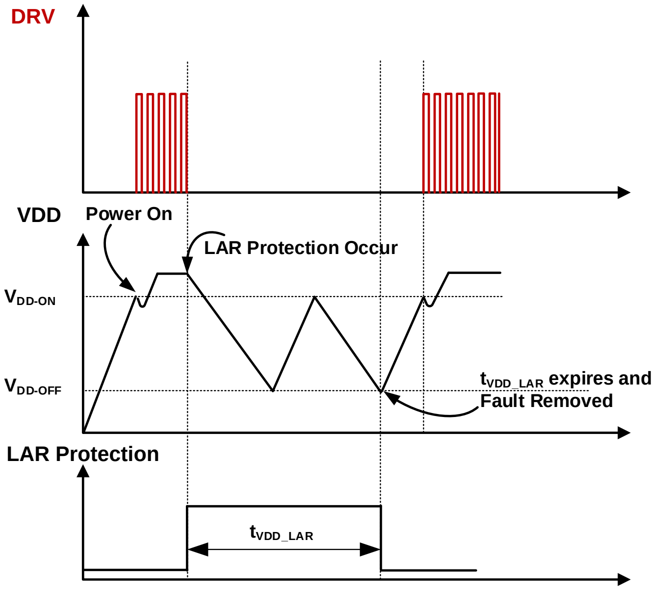


Figure 27 Auto-Restart Long AR Mode

VDD-OVP

VDD-OVP prevents IC damage from over voltage stress when abnormal system conditions occur. When VDD voltage exceeds V_{DD_OVP} (78.5V) for the debounce time $t_{D\_VDD\_OVP}$ (32μs), the VDD-OVP protection is triggered, the device enters the auto-restart mode or latch mode.

Brown-in & Brown-out

The sensed line voltage information is used for the brown-in and brown-out protection. During FET conduction time, when the current, I_{DMAG}, flowing out of DMAG pin is higher than 0.48mA for 4 debounce cycles, the brown-in is enabled. The input bulk capacitor voltage level to enable the brown-in is given as:

$$V_{BLK\_Brownin} = 0.48\text{mA} \times \frac{R_{DMAG1}}{N_A/N_P} \qquad \text{(Equation 5)}$$

When I_{DMAG} is lower than 0.36mA for longer than 16.5ms, the brown-out is triggered. The input bulk capacitor voltage level to trigger the brown-out protection is given as:

$$V_{BLK\_Brownout} = 0.36\text{mA} \times \frac{R_{DMAG1}}{N_A/N_P} \qquad \text{(Equation 6)}$$

IC Internal OTP

The internal temperature-sensing circuit disables the PWM output if the junction temperature exceeds 140°C (T_{OTP}), and the IC enters protection mode.

DMAG-OVP

DMAG-OVP prevents IC damage caused by the output over voltage. Figure 28 shows the internal circuit of DMAG-OVP. When abnormal system conditions occur and cause DMAG oltage to exceed V_{DMAG_OVP} (3.55V) for more than 4 consecutive switching cycles (N_{DMAG_OVP}), PWM pulses are disabled and the IC enters the auto-restart mode or the latch mode. Usually, DMAG over voltage protection is caused by an open circuit of the secondary side feedback network or a fault condition of the DMAG voltage divider resistors.

For DMAG voltage divider design, R_{DMAG1} is obtained from Equation 5, and R_{DMAG2} is determined by Equation 3. The output over voltage protection level, V_{O_OVP}, can be determined by Equation 7.

$$V_{O\_OVP} = \frac{N_S}{N_A} \times \left(1 + \frac{R_{DMAG1}}{R_{DMAG2}}\right) \times V_{DMAG\_OVP} \qquad \text{(Equation 7)}$$

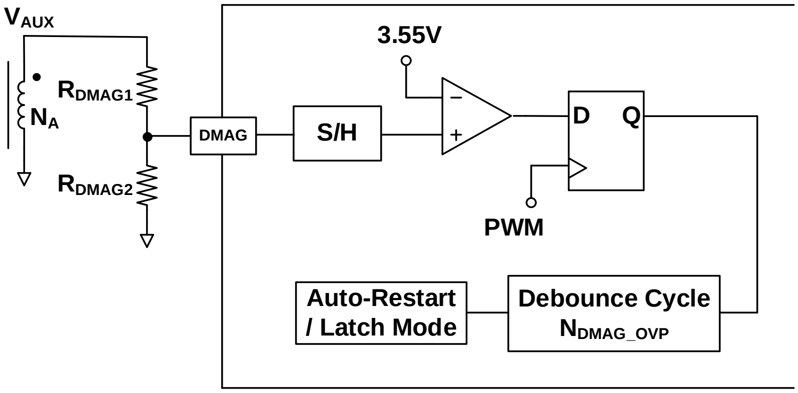


Figure 28 DMAG Over Voltage Protection Circuit

DMAG-UVP

In the event with shorted output, the output voltage will drop and the primary peak current will increase. To prevent operation for a long time under this condition, NV9510 family incorporate the under voltage protection through DMAG pin (DMAG-UVP). Figure 29 shows the internal circuit for DMAG-UVP. By sampling the auxiliary winding voltage on DMAG pin at the end of the secondary-side rectifier conduction time, the output voltage is indirectly sensed. When DMAG voltage is less than V_{DMAG_UVP} (0.425V) and longer than debounce cycles N_{DMAG_UVP}, DMAG UVP is triggered and the IC enters the auto-restart mode or the long auto-restart mode.

The output under voltage protection level, V_{O_UVP}, can be determined by Equation 8.

$$V_{O\_UVP} = \frac{N_S}{N_A} \times \left(1 + \frac{R_{DMAG1}}{R_{DMAG2}}\right) \times V_{DMAG\_UVP} \qquad \text{(Equation 8)}$$

To avoid DMAG-UVP triggering during the startup sequence, startup blanking time $t_{VDMAG\_UVP\_BNK}$ (32ms) is incorporated for system power on.

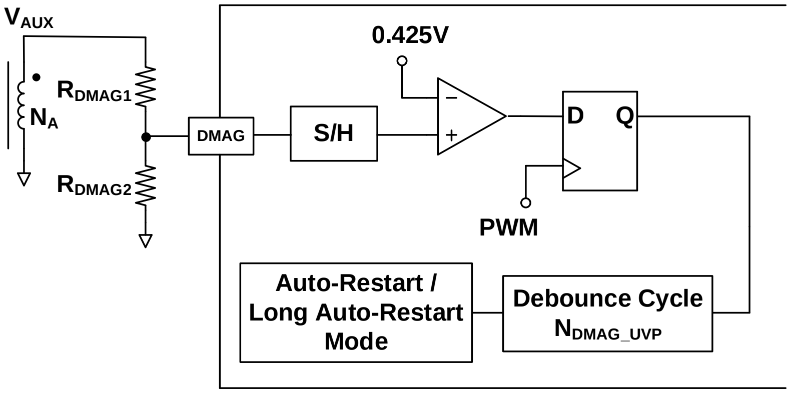


Figure 29 DMAG Under Voltage Protection Circuit

External Thermal Shut-down

During the startup, when VDD voltage reaches V_{DD_ON}, the shut-down trigger level is set at $V_{TH\_SD\_STR}$ (1.1V). After startup, the trigger level is changed to V_{TH_SD} (1.0V). By pulling down SD pin voltage below threshold voltage V_{TH_SD} (1.0V), the shut-down can be triggered externally and the IC will enter the auto-restart or the latch mode as shown in Figure 30. There is an internal constant current source I_{SD} (50µA) that is connected to SD pin. So an external OTP function can be implemented by connecting a NTC thermistor between SD pin and ground. The resistance of the NTC thermistor becomes smaller as the ambient temperature increases, therefore the voltage at SD pin will decrease. When the voltage is below the threshold voltage, V_{TH_SD} (1.0V), for debounce time of t_{D_SD} (400µs), the OTP protection is triggered. A capacitor may also be placed in parallel with the NTC thermistor to further improve the noise immunity.

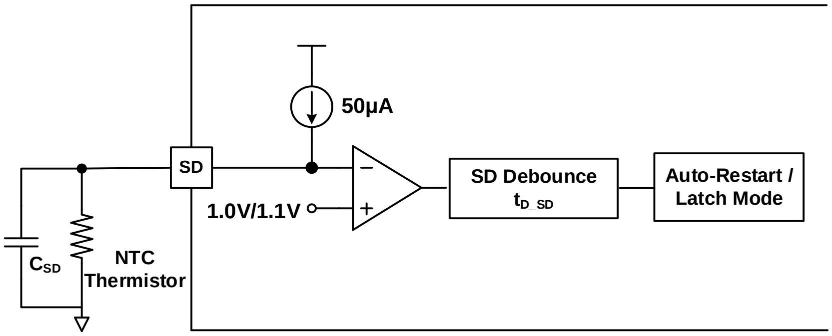


Figure 30 External OTP by SD Pin

Cycle by Cycle Current Limit

Under certain operation condition, such as the startup or the overload condition, the feedback control loop can be saturated and is unable to control the primary peak current. To limit the current under such conditions, NV9510 family products incorporate the cycle by cycle current limit protection which forces the DRV switch turn off when CS pin voltage reaches the current limit threshold, V_{CS_LIM}.

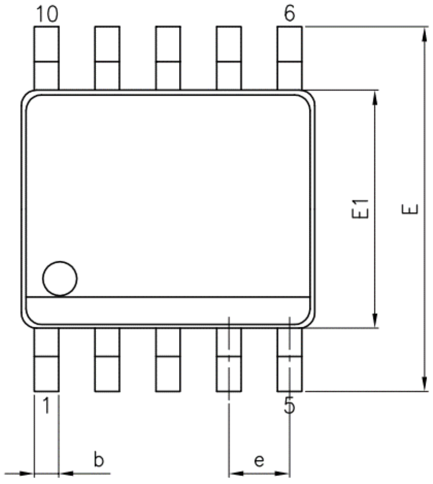
Current Sense Short Circuit Protection (CSSP)

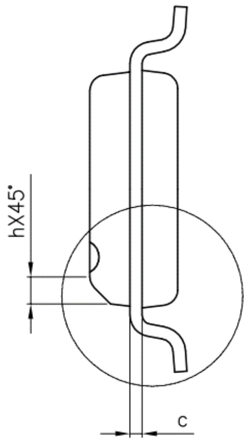
NV9510 family has CSSP function. When abnormal system conditions occur, In case after debounce time CS pin voltage is still lower than 0.15V ,DRV switch turn on time will be limited to limit output power.

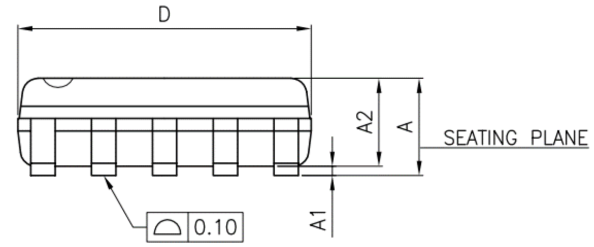
Secondary Side Diode Short Protection (SSSP)

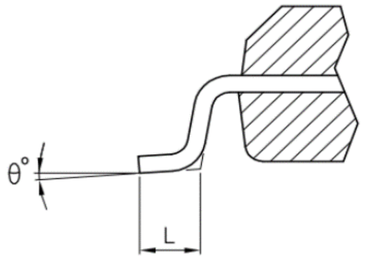
When the secondary-side rectifier is damaged, the primary-side switch current will increase dramatically within the leading-edge blanking time. To limit the switch current during such conditions, NV9510 family products incorporate SSSP function which forces the DRV Switch to turn off when CS pin voltage reaches 1.1V. After 2 switching cycle, the IC will enter the auto-restart mode.

Package Dimensions





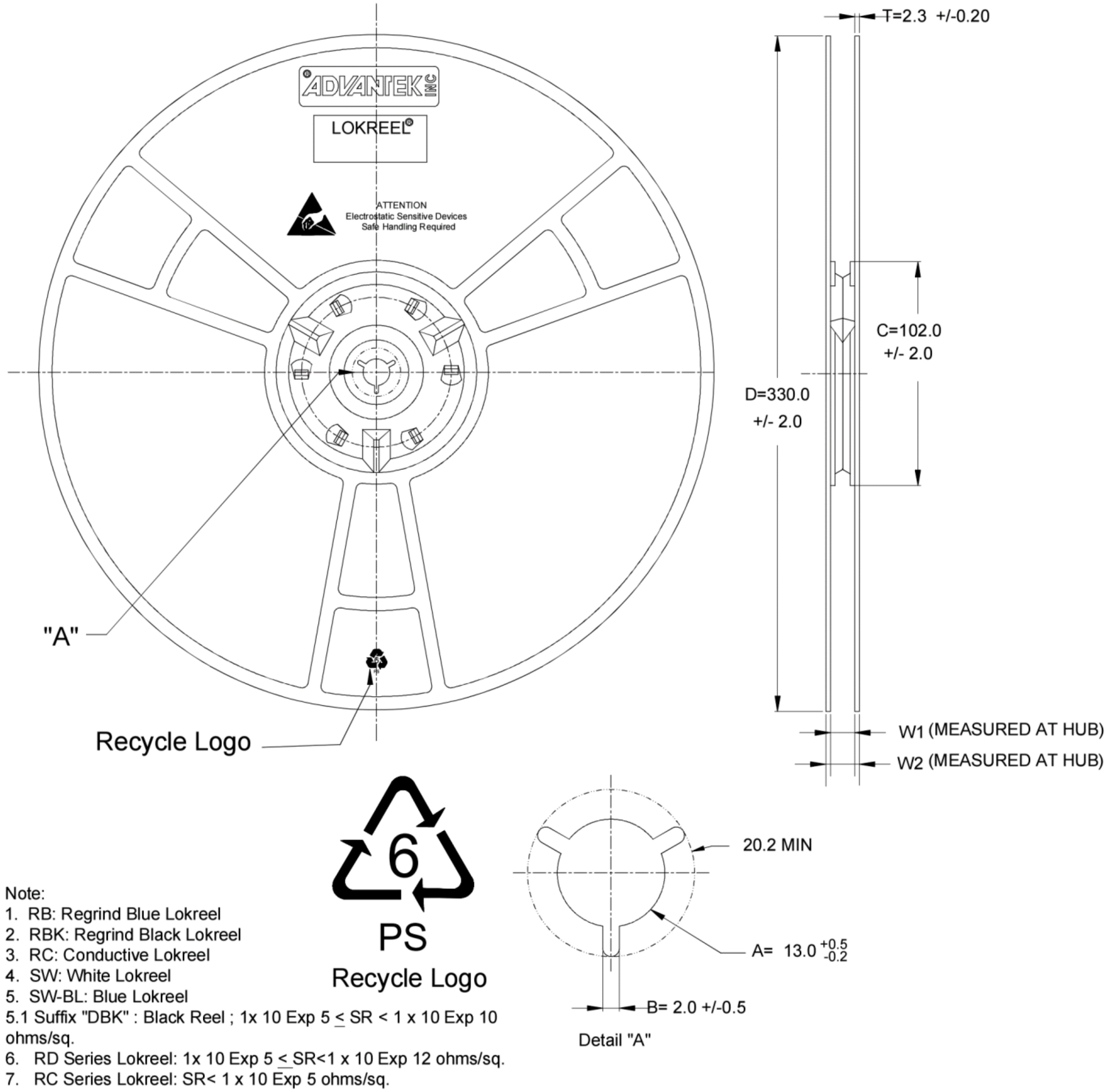




STMBOLS	STANDARD	
	MIN.	MAX.
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.30	0.45
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.00 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

VARIATIONS (ALL DIMENSIONS SHOW IN MM)

Tape and Reel Information



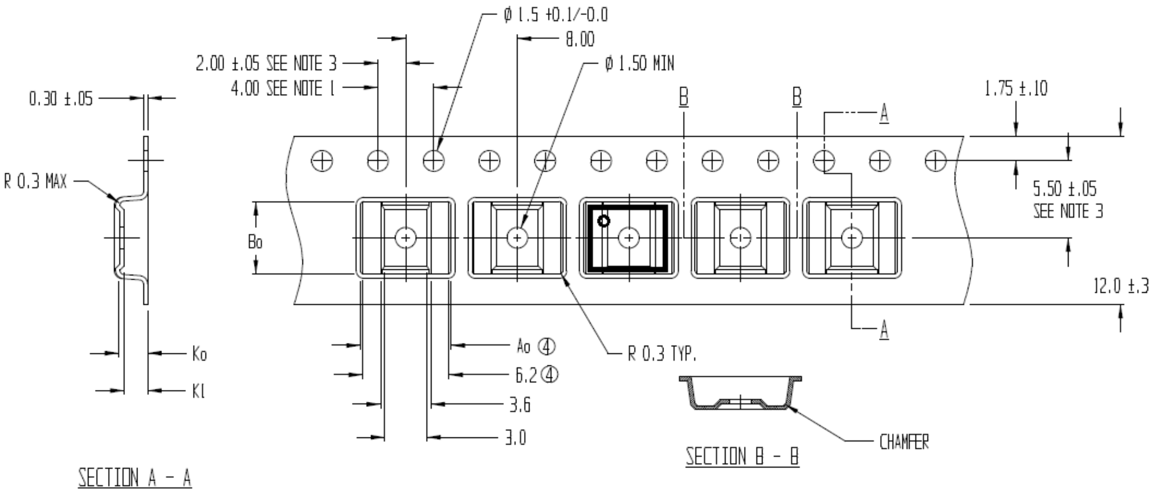
Note:

1. RB: Regrind Blue Lokreel
2. RBK: Regrind Black Lokreel
3. RC: Conductive Lokreel
4. SW: White Lokreel
5. SW-BL: Blue Lokreel

5.1 Suffix "DBK" : Black Reel ; 1x 10 Exp 5 ≤ SR < 1 x 10 Exp 10 ohms/sq.

6. RD Series Lokreel: 1x 10 Exp 5 ≤ SR<1 x 10 Exp 12 ohms/sq.
7. RC Series Lokreel: SR< 1 x 10 Exp 5 ohms/sq.

Nominal Hub Width	W1	W2 MAX
12mm	12.8mm +1.6 / -0.4	18.4mm



④① Ao = 6.50
Bo = 5.20
Ko = 2.10
K1 = 1.70

20-Year Limited Product Warranty

The 20-year limited warranty applies to all packaged Navitas GaNFast Power ICs, GaN Controller Co-pak ICs, and Controller ICs in mass production, subject to the terms and conditions of, Navitas' express limited product warranty, available at https://navitassemi.com/terms-conditions. The warranted specifications include only the MIN and MAX values only listed in Absolute Maximum Ratings and Electrical Characteristics sections of this datasheet. Typical (TYP) values or other specifications are not warranted.

Revision History

Date	Status	Notes
Feb. 24, 2023	PRELIMINARY	First publication

Additional Information

Contact info@navitassemi.com