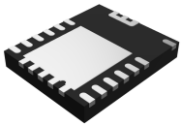
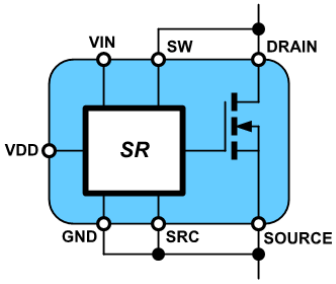
Flyback Sync Rect Controller & FET



QFN 5x6 Package



Simplified Schematic

Features

High Frequency SR Controller

- Integrated 12mΩ/100V MOSFET
- Compatibility of continuous conduction mode (CCM), quasi-resonant (QR) and discontinuous conduction mode (DCM) at low side applications.
- Wide input voltage ranges up to 26.5V
- Optimized SR gate turn-off threshold control
- Proprietary CCM SR turn-off control algorithm
- Minimized SR turn-on/off propagation delay
- SR MOSFET gate passive clamp
- Low power saving mode
- Highly efficient QFN 5x6 package

Topologies / Applications

- USB PD quick chargers for smart phones, feature phones and tablet PCs
- Power adaptor for portable device
- Flyback power supply with fixed or variable output voltage

Description

NV9750 is a secondary-side synchronous rectifier (SR) controller with integrated 100V Silicon MOSFET for isolated flyback converters. By implementing proprietary turn-off control algorithm, NV9750 can reliably support discontinuous conduction mode (DCM), quasi-resonant (QR) and continuous conduction mode (CCM) operation, which will help to design robust flyback converters. Small footprint QFN 5x6 package enables designers to achieve simple, quick and reliable solutions. Navitas' controller IC technologies enable high frequencies, high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

Simplified Application Diagram

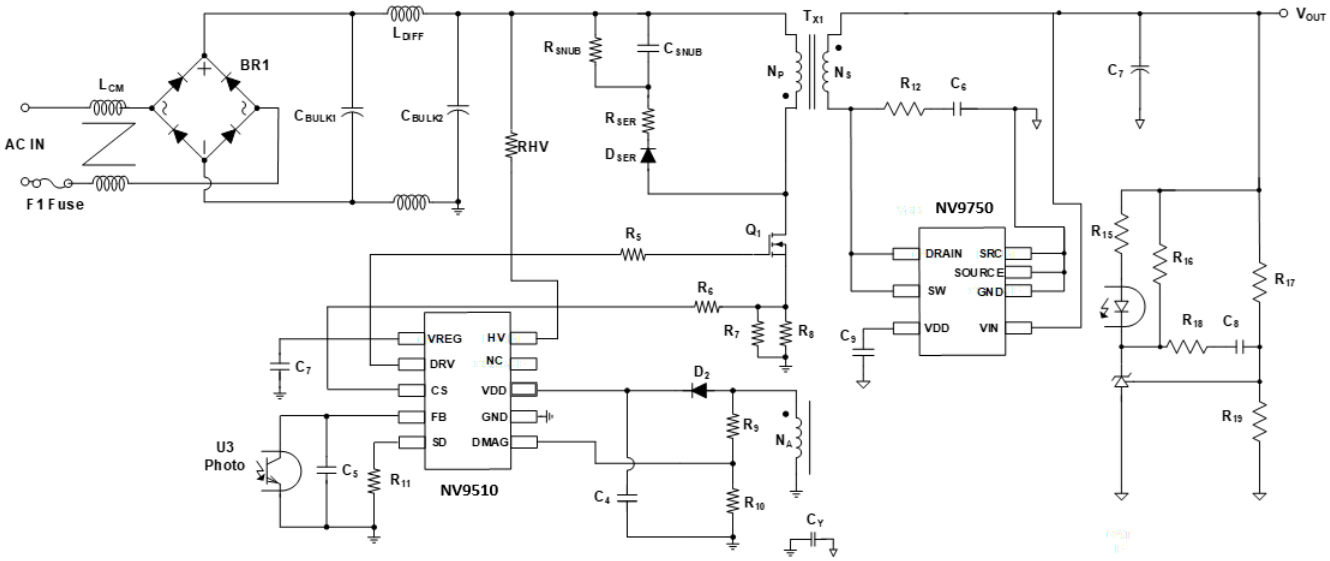


Figure 1. Low-Side SR Application Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
NV9750FN01	-40°C to +125°C	QFN5x6	5K/Tape & Reel

Pin Configuration and Marking Diagram

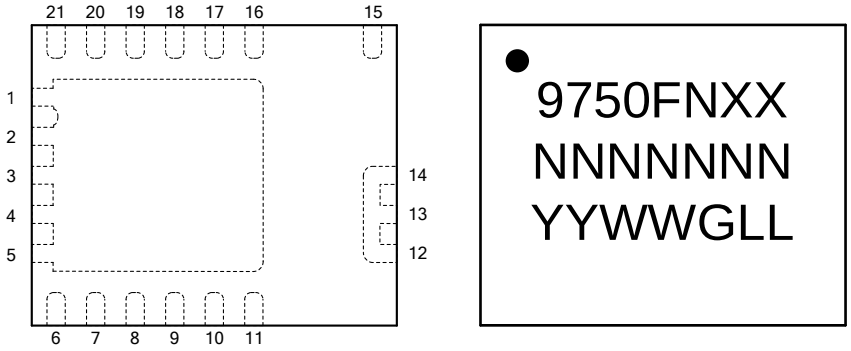


Figure 2. Pin Configuration & Marking Diagram (Top View)

Symbol	Content
9750	Device Code
FN	Package Code, FN=QFN 5x6
XX	Trim Option Code
NNNNNNN	Lot Number
YY	Year Code
WW	Week Code
G	Manufacture Code
LL	Trace Code

Pin Function

Pin No.	Name	Description
1, 2, 3, 4, 5, 11, 16	DRAIN	Connect to MOSFET Drain PAD.
6	SRC	Synchronous MOSFET source sense input.
7	VIN	Supports up to 26.5V operation, input of an integrated 5V LDO which generates the internal power supply for the low-voltage control circuitry.
8	GND	Ground Reference.
9	VDD	Internal regulator 5V output and gate driver power supply rail. Bypass with 1µF capacitor to GND.
10	NC	NC.
12, 13, 14	SOURCE	Connect to MOSFET Source PAD.
15	NC	NC.
17, 18, 19, 20	SOURCE	Connect to MOSFET Source PAD.
21	SW	Synchronous MOSFET drain sense input.
1, 2, 3, 4, 5, 11, 16	DRAIN	Connect to MOSFET Drain PAD.

Table 1. Pin Definition

Internal Function Block Diagram

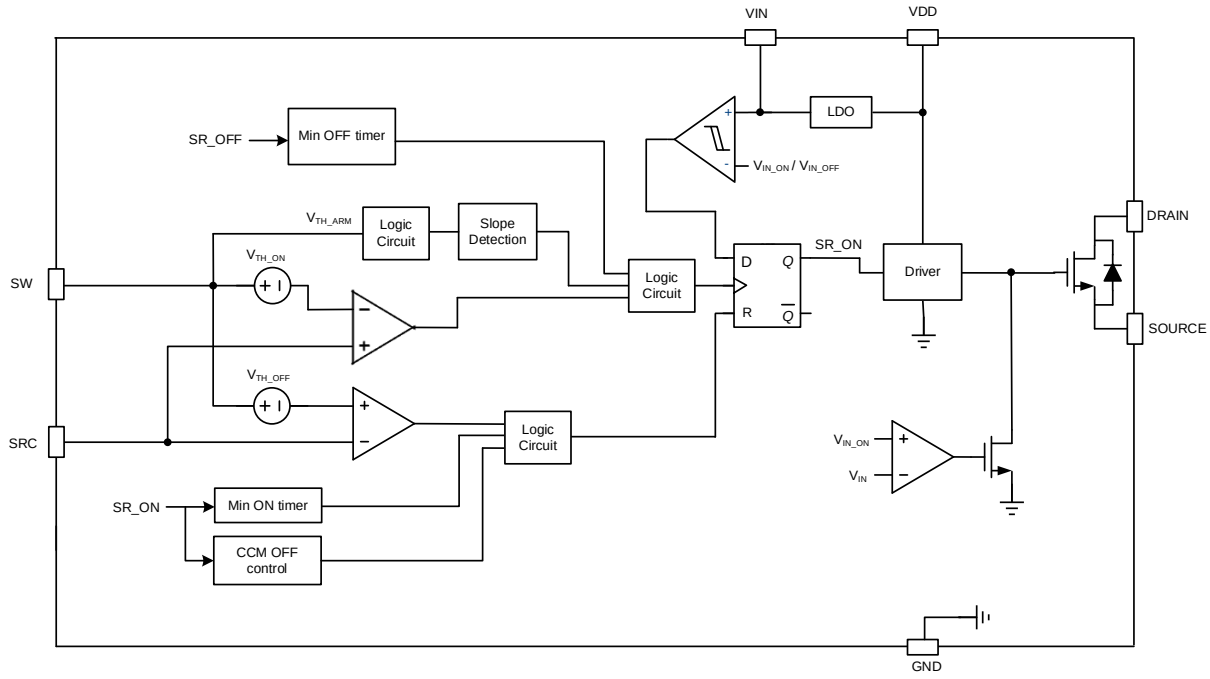


Figure 3. Internal Function Block Diagram

Electrical Characteristics

Absolute Maximum Ratings (1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VIN	Power Supply Input Pin Voltage		-0.3	28	V
SW	SW Sense Input Pin Voltage		-1.0	120	V
DRAIN	MOSFET Drain Pin		-	100	V
VDD	Internal Regulator Output Pin Voltage		-0.3	6.0	V
SOURCE	MOSFET Source Pin		-0.3	-	V
SRC	Source Sense Input Pin Voltage		-0.3	5.5	V
TJ	Operating Junction Temperature		-40	150	°C
TSTG	Storage Temperature Range		-60	150	°C
TL	Lead Soldering Temperature		-	260	°C
ESD	Electrostatic Discharge Capability	Human Body Mode, ANSI/ESDA/JEDEC JS-001-2017	-	2.0	kV
		Charge Device Mode, JED ANSI/ESDA/JEDEC JS-001-2018	-	2.0	kV

Notes (1):

- *Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.*
- *All voltage values are with respect to the GND pin*

Recommended Operating Conditions (2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Elevation does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Power Supply Input Pin Voltage	3.0	-	24	V
SW	SW Sense Input Pin Voltage	-1.0	-	120	V
DRAIN	MOSFET Drain Pin	-	-	100	V
VDD	Internal Regulator Output Pin Voltage	-0.3	-	5.5	V
SOURCE	MOSFET Source Pin	-0.3	-	-	V
SRC	Source Sense Input Pin Voltage	-0.3	-	-	V

Notes (2):

- *Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40°C to +85°C unless otherwise noted.*

Electrical Specifications

V_{IN} (Typ.) = V_{DD} (Typ.) = 5V, T_A =-40°C to 85°C, and T_A (Typ.) =25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Type.	Max.	Unit
Power Supply						
V_{IN_ON}	Turn-on Input Voltage	Vin Rising	2.0	2.2	2.4	V
V_{IN_OFF}	Turn off Input Voltage	Vin Falling	1.8	2.0	2.2	V
I_{IN_GREEN}	Quiescent Current	No DRV Switching	175	240	400	µA
T_{GREEN}(3)	Time Threshold for Power Save		-	100	-	µs
$I_{IN\_OP\_20kHz\_5V}$	Operating Current at 5V	F_{SW} = 20kHz, V_{IN} = 5V	495	710	805	µA
$I_{IN\_OP\_100kHz\_5V}$	Operating Current at 5V	F_{SW} = 100kHz, V_{IN} = 5V	1.5	2.0	2.5	mA
$I_{IN\_OP\_100kHz\_20V}$ (3)	Operating Current at 20V	F_{SW} = 100kHz, V_{IN} = 20V	-	2.0	-	mA
V_{DD_ON}	VDD Turn-on Threshold	V_{DD} Rising	2.7	2.9	3.1	V
V_{DD_OFF}	VDD Turn-off Threshold	V_{DD} Falling	2.5	2.7	2.9	V
V_{DD_0A}	VDD Regulation Voltage W/O Load	V_{IN}=12V I_{VDD}=0A	4.8	5.0	5.2	V
V_{DD_10mA}	VDD Regulation Voltage with 10mA Load	V_{IN}=12V I_{VDD}=10mA	4.7	4.9	5.1	V
SW Pin Sensing						
V_{TH_ON}	Turn-on Threshold		-405	-250	-95	mV
T_{ON_DLY} (3)	Turn-on Delay Time		-	10	-	ns
V_{TH_OFF}	Turn-off Threshold		0.01	-	0.8	mV
T_{OFF_DLY} (3)	Turn-off Delay Time		-	10	-	ns
SR Gate Control						
T_{ON_MIN}	SR Minimum ON-Time		295	350	420	ns
$T_{ON\_MIN\_H}$	T_{ON_MIN} at Heavy Load		565	650	735	ns
T_{OFF_MIN} (3)	SR Minimum OFF-Time		-	1.2	-	µs
MOSFET Section						
$V_{DS(CONT)}$	Drain-Source voltage		-	-	100	V
$R_{DS(ON)}$	Drain-Source resistance		-	12	16	mΩ

Note (3):

- *Guarantee by design*

Typical Performance Characteristics

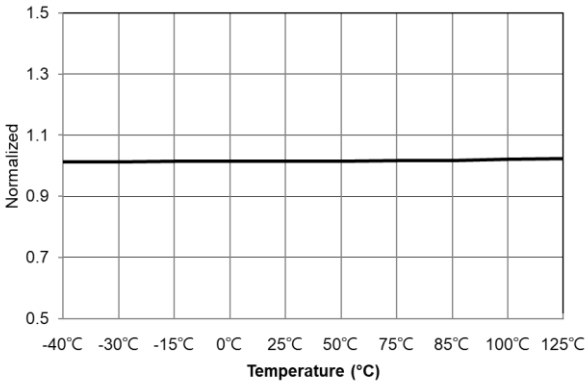


Figure 4 V_{IN_ON}

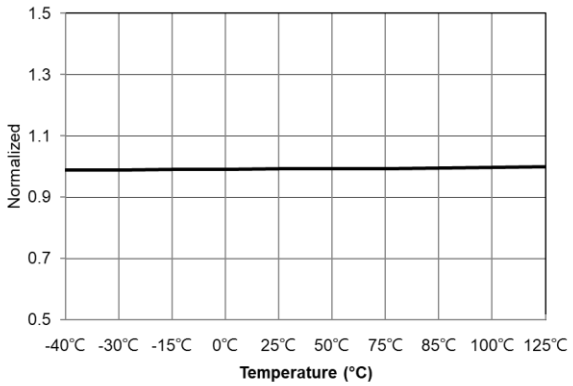


Figure 5 V_{IN_OFF}

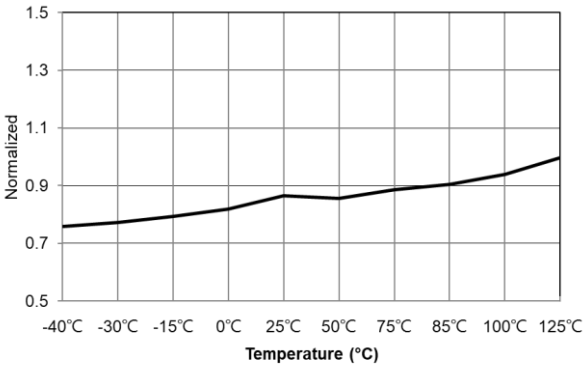


Figure 6 I_{IN_GREEN}

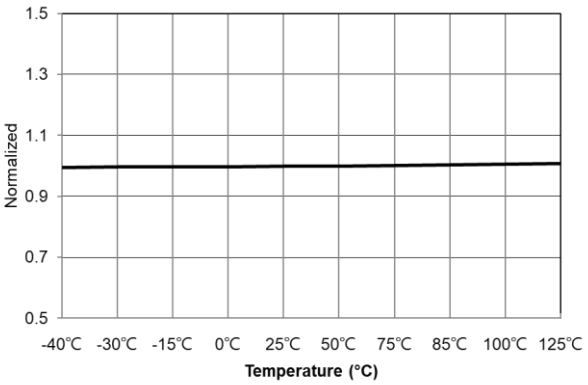


Figure 7 V_{DD_ON}

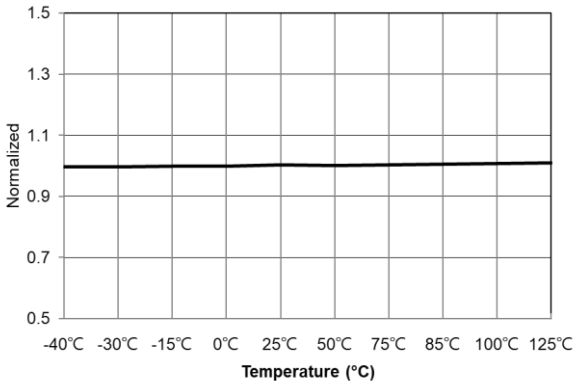


Figure 8 V_{DD_OFF}

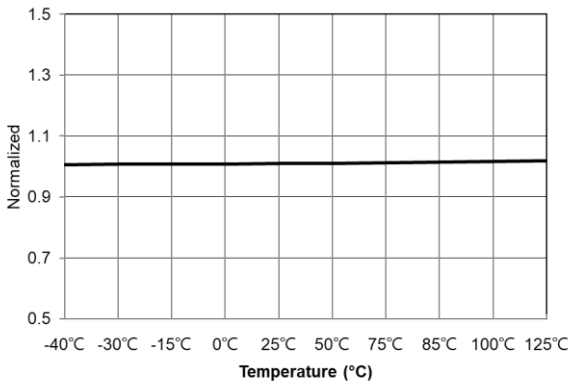


Figure 9 V_{DD_LDO}

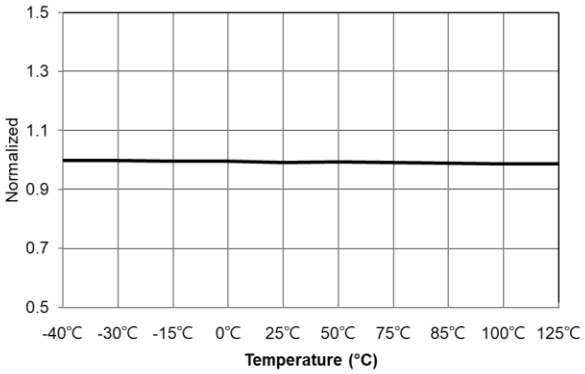


Figure 10 V_{LDO}

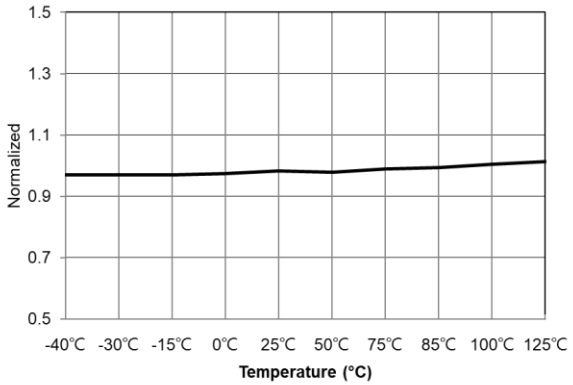


Figure 11 $I_{IN\_OP\_20kHz\_5V}$

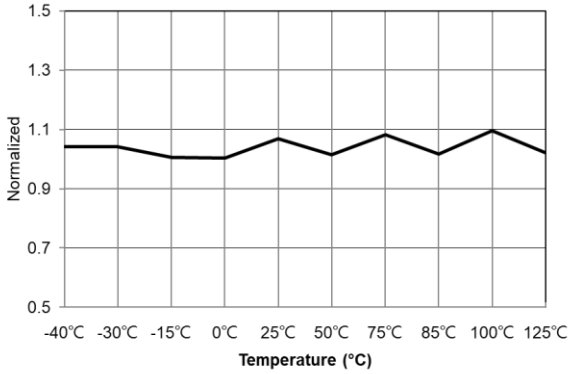


Figure 12 V_{TH_ON}

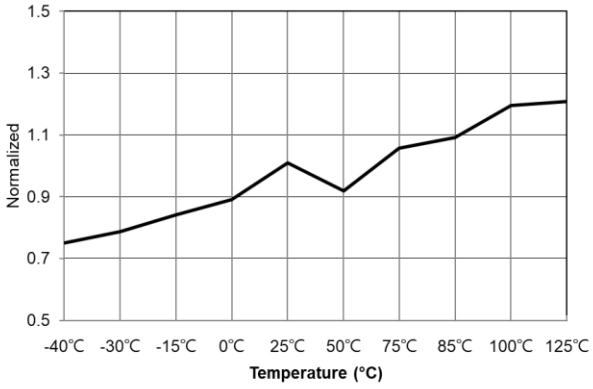


Figure 13 V_{TH_OFF}

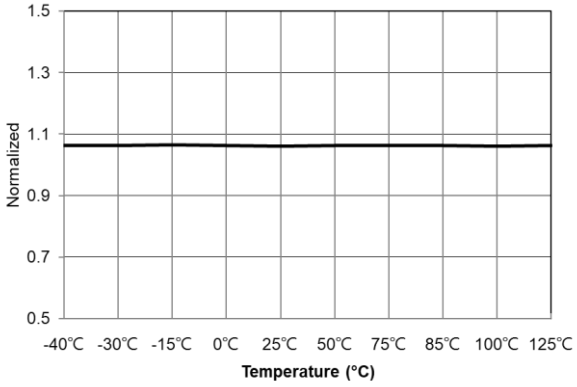


Figure 14 T_{ON_MIN}

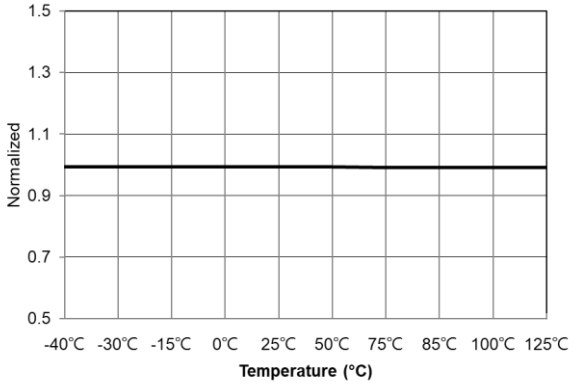
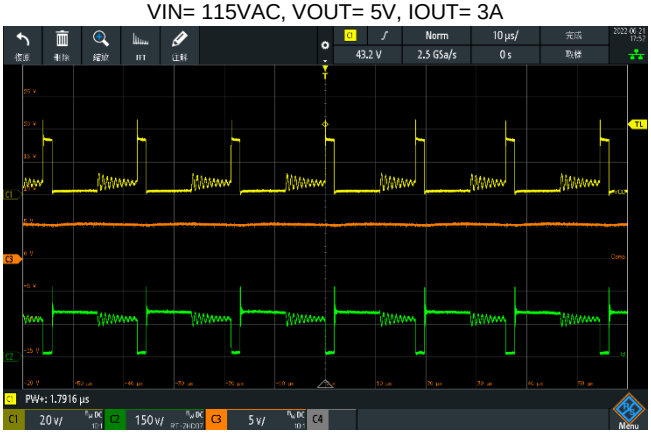


Figure 15 $T_{ON\_MIN\_H}$

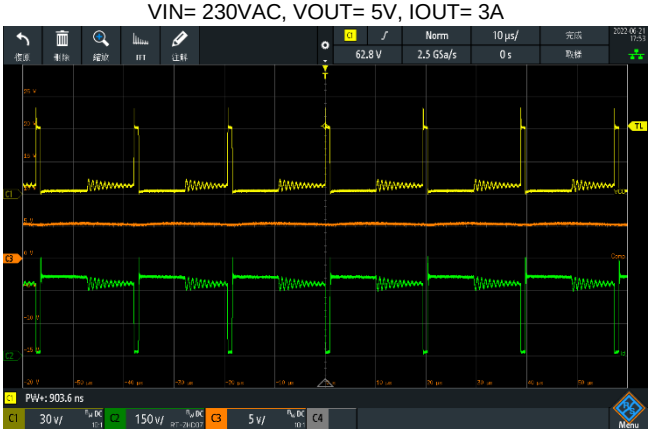
Typical Performance Characteristics *(Continued)*

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 5V, IOUT= 3A



CH1: VDS 20V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 5V, IOUT= 3A



CH1: VDS 30V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

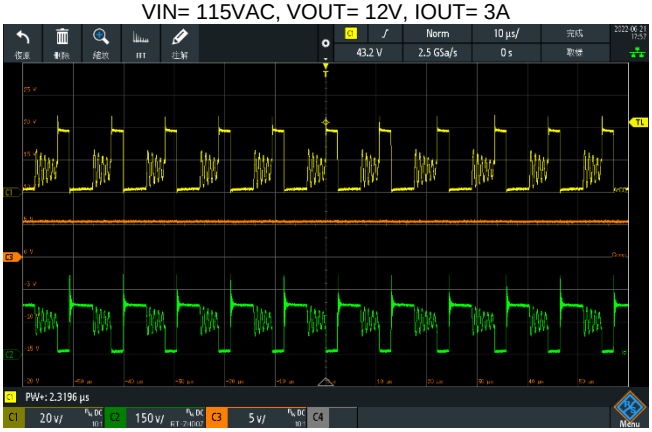
Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 9V, IOUT= 3A

CH1: VDS 20V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 9V, IOUT= 3A

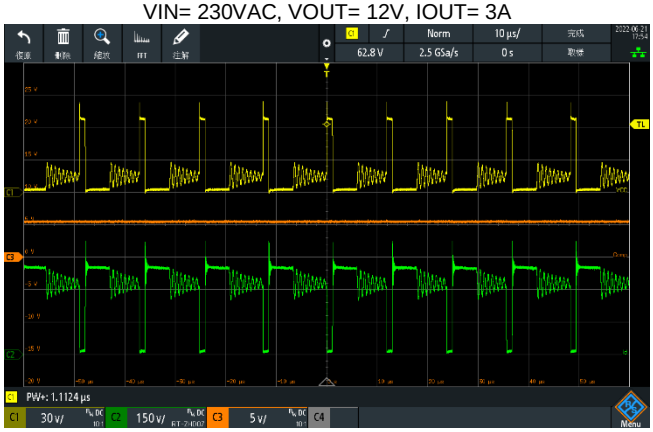
CH1: VDS 30V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 12V, IOUT= 3A



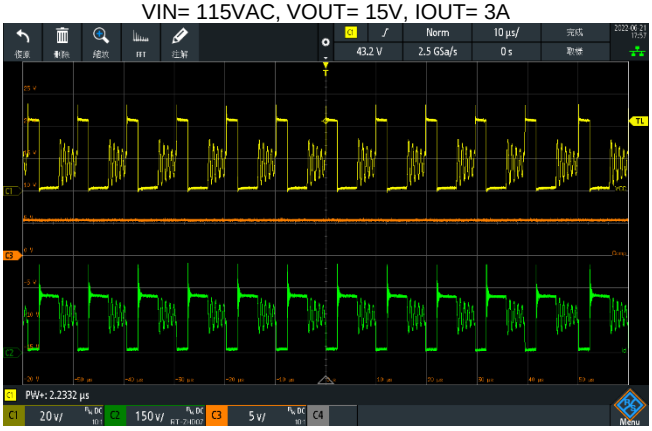
CH1: VDS 20V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 12V, IOUT= 3A



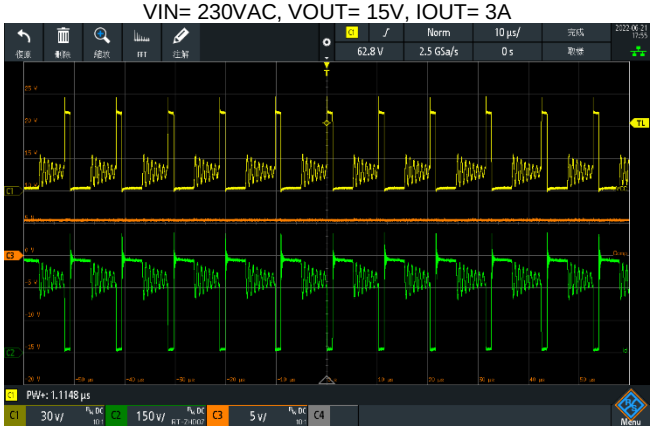
CH1: VDS 30V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 15V, IOUT= 3A



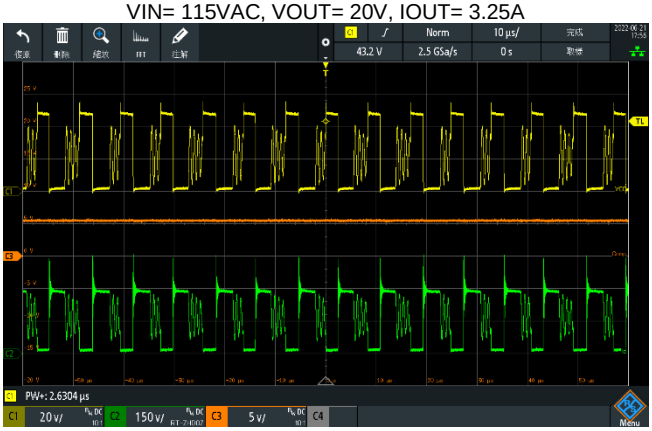
CH1: VDS 20V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 15V, IOUT= 3A



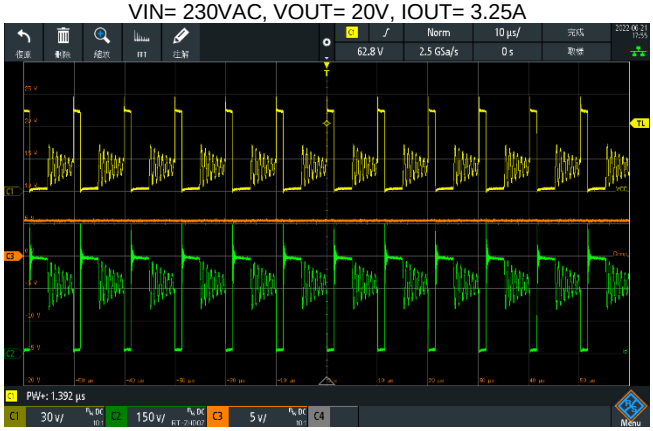
CH1: VDS 30V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 20V, IOUT= 3.25A



CH1: VDS 20V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 20V, IOUT= 3.25A



CH1: VDS 30V/div, CH2: Pri_VDS 150V/div, CH3: VDD 5V/div

Detailed Function Description

Operation

NV9750FN supports operation in discontinuous conduction mode (DCM), quasi-resonant (QR) and continuous conduction mode (CCM) flyback converters. The control circuitry controls the gate of synchronous rectification (SR) MOSFET on in forward mode and turn the gate off when the SR MOSFET current drops to certain value.

VDD Power Supply

VDD is the supply power for the NV9750FN, a bypass ceramic (typical 1µF) capacitor should be put closely from VDD to GND to guarantee the normal operation.

During startup, when V_{IN} rises above V_{IN_ON} (2.2V) and VDD rises to V_{DD_ON} (2.9V), NV9750FN starts to operate according to its internal logic. When VDD falls below V_{DD_OFF} (2.7V) or V_{IN} falls below V_{IN_OFF} (2.0V), then NV9750FN stops working right away.

SR Gate Turn-On Control

As shown in Figure 17, the turn-on of SR GATE is active when the SW sense voltage is lower than turn on threshold V_{TH_ON} (-250mV). To prevent the mis-trigger turn-on of SR MOSFET, a minimum off time T_{OFF_MIN} is used after SR MOSFET is turned off.

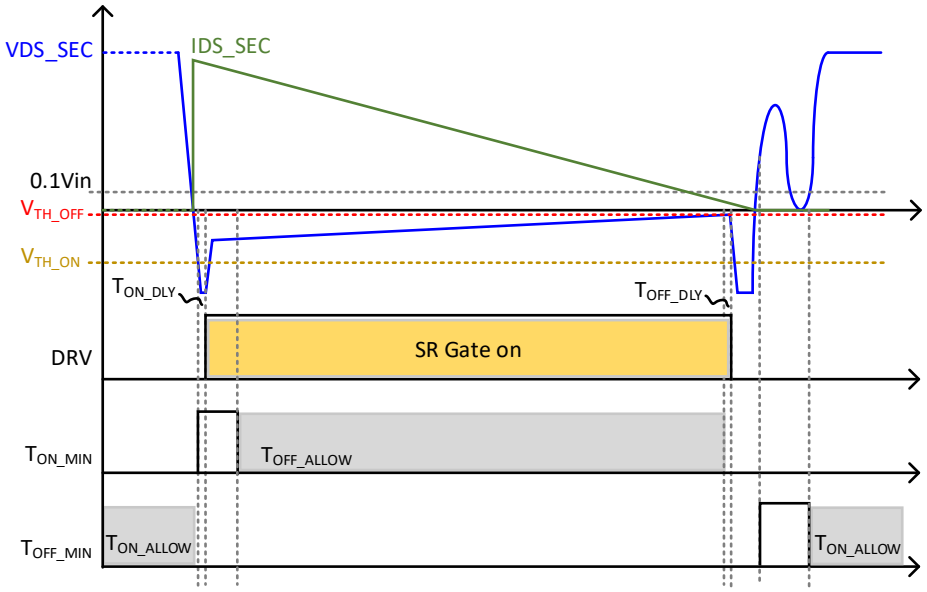


Figure 16. SR Turn-On Control Sequence

SR Gate Turn-Off Control

NV9750FN will detect the SW voltage, when it is higher than V_{TH_OFF} (0mV), the GATE will be turned off.

PCB Layout Guidelines

Optimized PCB layout is key for stable operation. Please refer to following layout guidelines to design your platform.

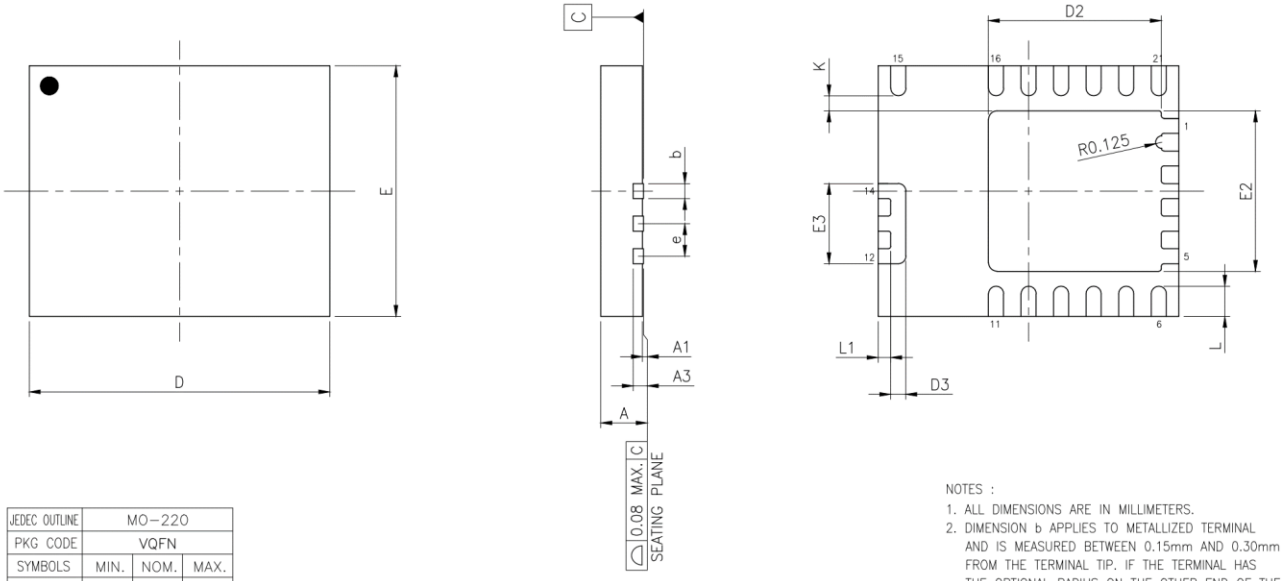
Sensing Loop for VSW and VSRC

- Make the sensing path of SW, SRC as short to Drain and Source as possible.
- Make two independent routing trace to Drain and Source directly.

Power Supply Loop

- Put a low ESR and low ESL decoupling ceramic capacitor from VDD to GND as close to NV9750FN as possible for stable power supply.
- The sensing loop (SRC and SW to the Source and Drain) is minimized and keep away from the switching power loop.

Package Dimensions



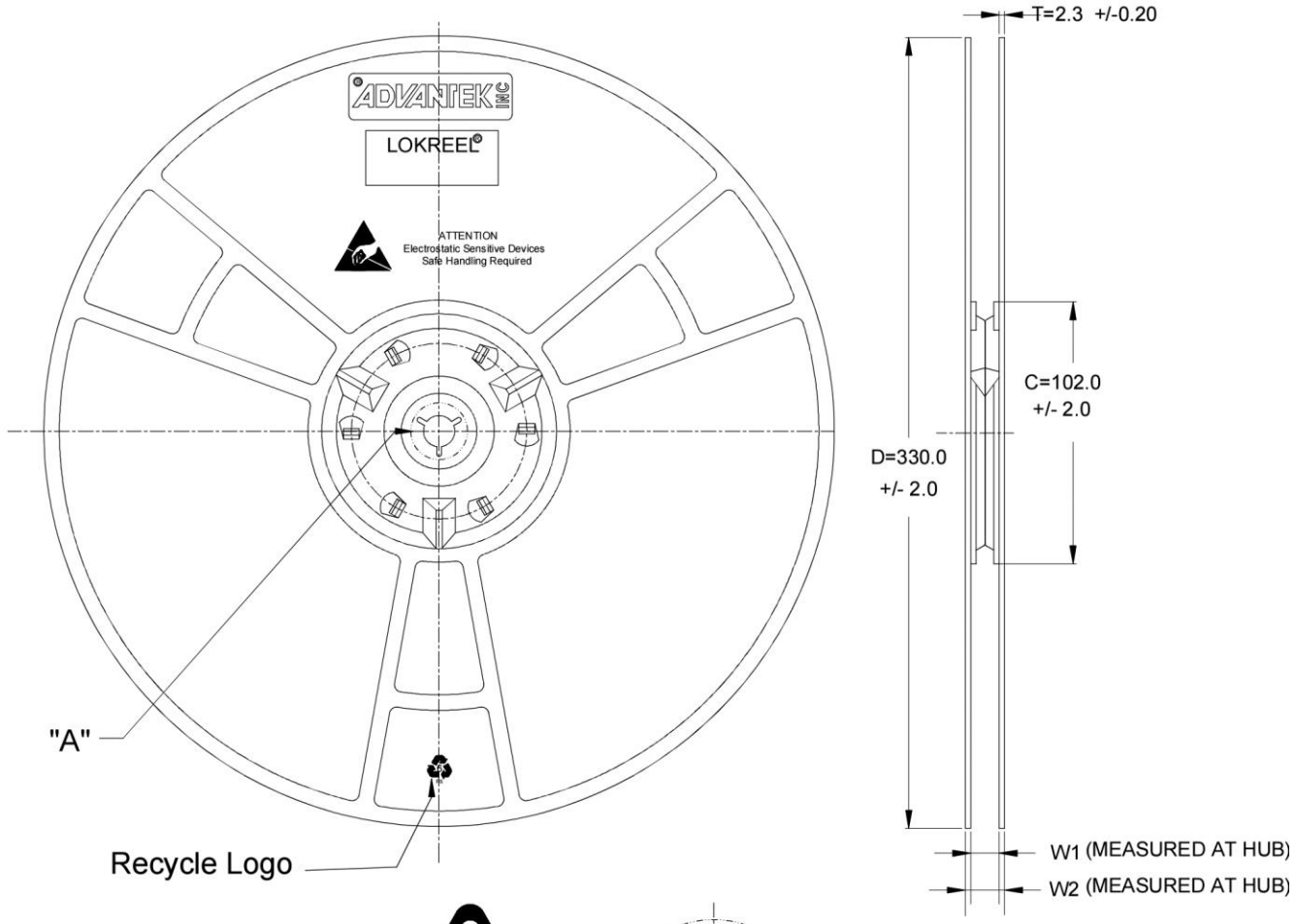
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.25	0.30	0.35
D	6.00 BSC		
E	5.00 BSC		
e	0.65 BSC		
L	0.55	0.60	0.65
L1	0.20	0.25	0.30
K	0.20	–	–

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			D3			E3			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
	3.40	3.45	3.50	3.15	3.20	3.25	0.25	0.30	0.35	1.55	1.60	1.65	X	V	N/A

Tape and Reel Information

-All Dimensions in Millimeters-

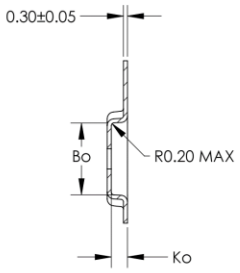


Note:
1. RB: Regrind Blue Lokreel
2. RBK: Regrind Black Lokreel
3. RC: Conductive Lokreel
4. SW: White Lokreel
5. SW-BL: Blue Lokreel

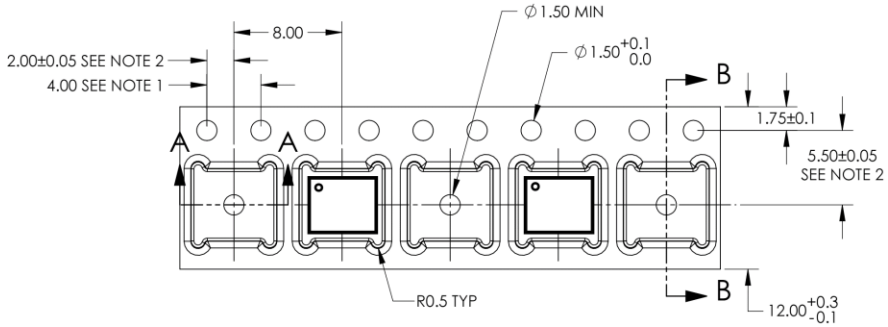
5.1 Suffix "DBK" : Black Reel ; 1x 10 Exp 5 ≤ SR < 1 x 10 Exp 10 ohms/sq.

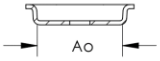
6. RD Series Lokreel: 1x 10 Exp 5 ≤ SR<1 x 10 Exp 12 ohms/sq.
7. RC Series Lokreel: SR< 1 x 10 Exp 5 ohms/sq.

Nominal Hub Width	W1	W2 MAX
12mm	12.8mm +1.6 / -0.4	1.84mm



SECTION B-B





SECTION A-A

SCALE 1:1

	DIM	±
Ao	6.30	0.1
Bo	5.30	0.1
Ko	1.20	0.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Revision History

Date	Status	Notes
May. 12, 2023	DATASHEET	First publication
May. 27, 2024		Remove high side application because it causes additional design effort to system cost and layout space.

Additional Information

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