

# MOSFET – Power, N-Channel, Automotive, SUPERFET® III, Easy-Drive

650 V, 25 mΩ

## NVCR8LS025N65S3A



### Features

- Typical  $R_{DS(on)} = 19.9 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$
- Typical  $Q_{g(tot)} = 236 \text{ nC}$  at  $V_{GS} = 10 \text{ V}$
- AEC-Q101 Qualified
- RoHS Compliant

### DIMENSION ( $\mu\text{m}$ )

Die Size	10830 x 7610
Die Size (Sawn)	10810 $\pm$ 30 x 7590 $\pm$ 30
Source Attach Area	(10155 x 3346) x 2
Gate Attach Area	406 x 618
Die Thickness	203.2 $\pm$ 25.4

Gate and Source : AlSiCu  
 Drain : Ti-NiV-Ag (back side of die)  
 Passivation : SiN  
 Wafer Diameter : 8 inch  
 Wafer sawn on UV Tape  
 Bad dice identified in Inking  
 Gross Die Count : 296

### ORDERING INFORMATION

Device	Package
NVCR8LS025N65S3A	Wafer Sawn on Foil

### RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40% to 66%

### ELECTRICAL CHARACTERISTICS

The Chip is 100% Probed to Meet the Conditions and Limits Specified at  $T_J = 25^\circ\text{C}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	650	–	–	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = +30 / -20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	$\pm 100$	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 3 \text{ mA}$	2.5	–	4.5	V
$*R_{DS(on)}$	Bare Die Drain to Source On Resistance	$I_D = 37.5 \text{ A}, V_{GS} = 10 \text{ V}$	–	19.9	25	$\text{m}\Omega$
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 37.5 \text{ V}$			1.2	V

\*Accurate  $R_{DS(on)}$  test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max  $R_{DS(on)}$  specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die  $R_{DS(on)}$  performance depends on the Source wire/ribbon bonding layout.

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## ABSOLUTE MAXIMUM RATINGS

in Reference to the NVHL025N65S3 electrical data in TO-247-3LD (  $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain to Source Voltage	650	V
$V_{GS}$	Gate to Source Voltage	DC Positive	30
		AC Positive, (f > 1Hz)	30
		AC Negative, (f > 1Hz)	-20
$I_D$	Continuous Drain Current	$T_C = 25^\circ\text{C}$	75
		$T_C = 100^\circ\text{C}$	65.8
$I_{DM}$	Pulsed Drain Current	Pulsed (Note 1)	300
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	2025	mJ
$E_{AR}$	Repetitive Avalanche (Note 1)	5.95	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
$P_D$	Power Dissipation $R_{\theta JC}$	$T_C = 25^\circ\text{C}$	595
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 15\text{ A}$ ,  $R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} < 75\text{ A}$ ,  $di/dt \leq 200\text{ A/ms}$ ,  $V_{DD} \leq BVDSS$ , starting  $T_J = 25^\circ\text{C}$

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.21	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	40	$^\circ\text{C/W}$

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## ELECTRICAL CHARACTERISTICS

in Reference to the NVHL025N65S3 electrical data in TO-247-3LD ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	650	-	-	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 520 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$	-	7.92	-	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = +30 \text{ V}$	-	-	+100	nA
		$V_{GS} = -20 \text{ V}$			-100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 3.0 \text{ mA}$	2.5		4.5	V	
$R_{DS(on)}$	Drain to Source On-Resistance	$I_D = 37.5 \text{ A},$ $V_{GS} = 10 \text{ V}$	$T_J = 25^\circ\text{C}$	-	19.9	25	$\text{m}\Omega$
			$T_J = 100^\circ\text{C}$	-	34.6	-	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 75 \text{ A}$		78.5		S	

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	7330	-	pF
$C_{oss}$	Output Capacitance		-	197	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	33.6	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0 \text{ V to } 400 \text{ V}, V_{GS} = 0 \text{ V}$		2062		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	$V_{DS} = 0 \text{ V to } 400 \text{ V}, V_{GS} = 0 \text{ V}$		285		pF
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 10 \text{ V}, V_{DS} = 400 \text{ V}, I_D = 75 \text{ A}$ (Note 4)	-	236	-	nC
$Q_{gs}$	Gate to Source Gate Charge		-	59.3	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	97.3	-	nC
$R_G$	Gate Resistance	$f = 1 \text{ MHz}$	-	0.818	-	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 75 \text{ A}, V_{GS} = 10 \text{ V},$ $R_G = 2 \Omega$ (Note 4)	-	43.3	-	ns
$t_r$	Rise Time		-	109	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	120	-	ns
$t_f$	Fall Time		-	107	-	ns

### DRAIN – SOURCE DIODE CHARACTERISTICS

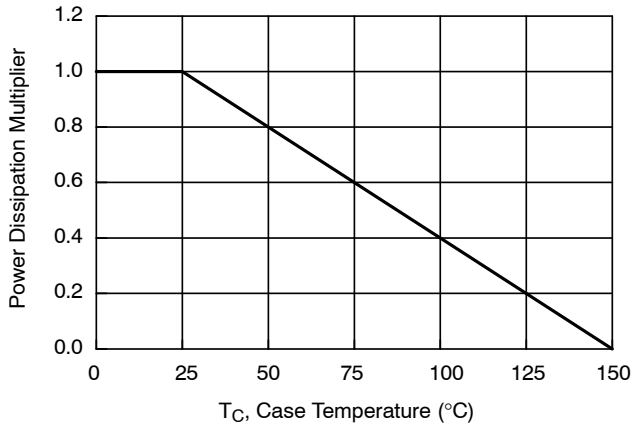
$I_S$	Maximum Continuous Drain to Source Diode Forward Current				75	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current				300	A
$V_{SD}$	Source to Drain Diode Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 37.5 \text{ A}, V_{GS} = 0 \text{ V}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 75 \text{ A}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}$	-	714	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	26.4	-	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

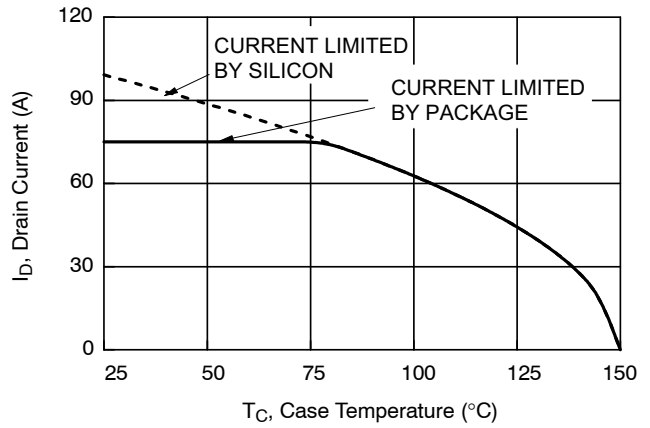
4. Essentially independent of operating temperature typical characteristics.

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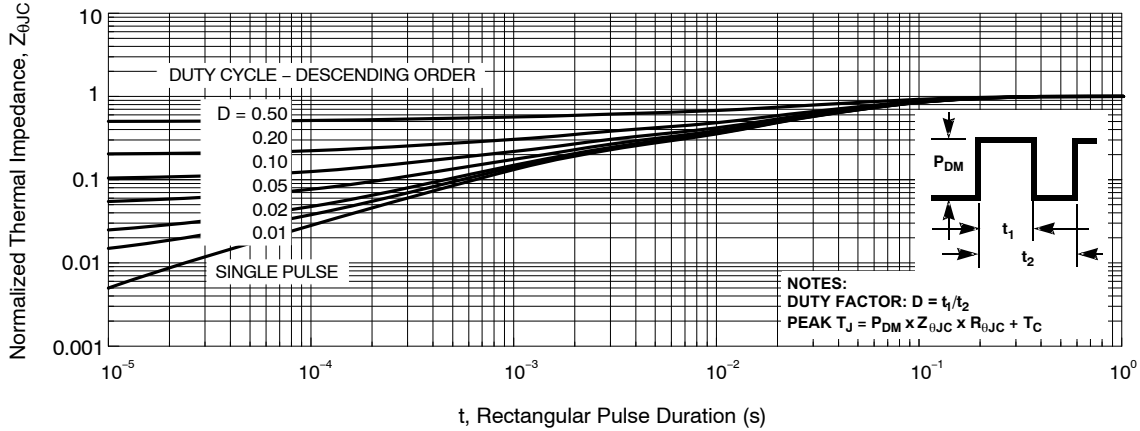
## TYPICAL CHARACTERISTICS



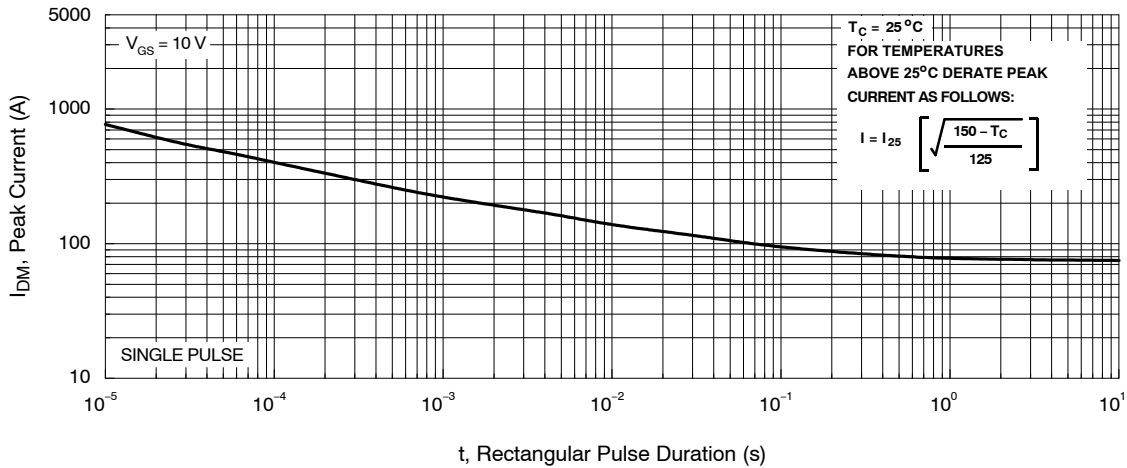
**Figure 1. Normalized Power Dissipation vs. Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**



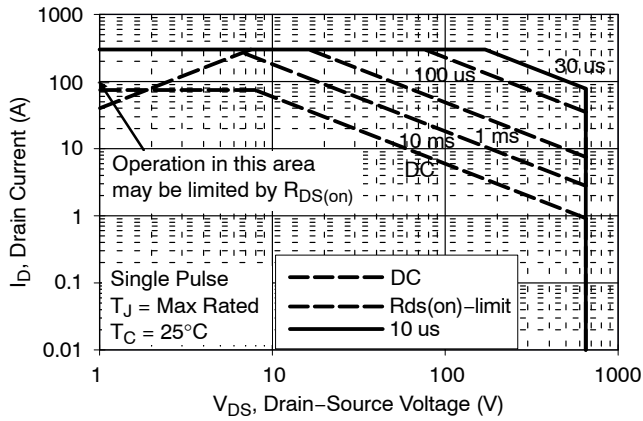
**Figure 3. Normalized Maximum Transient Thermal Impedance**



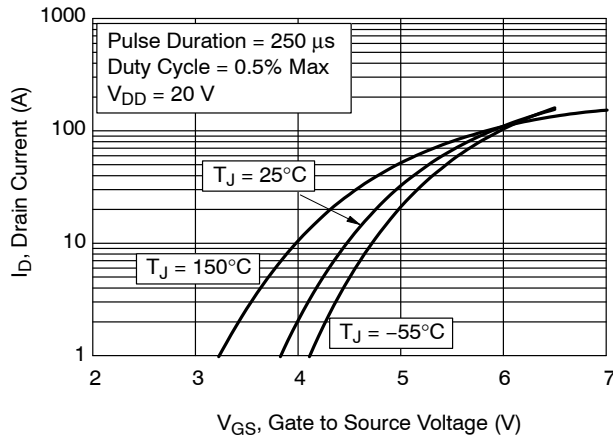
**Figure 4. Peak Current Capability**

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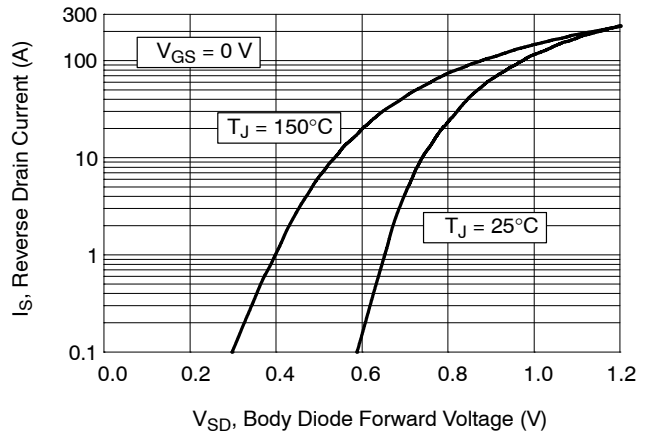
## TYPICAL CHARACTERISTICS (continued)



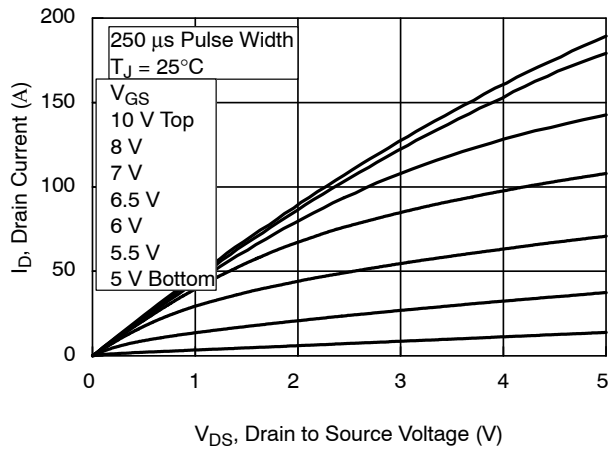
**Figure 5. Forward Bias Safe Operating Area**



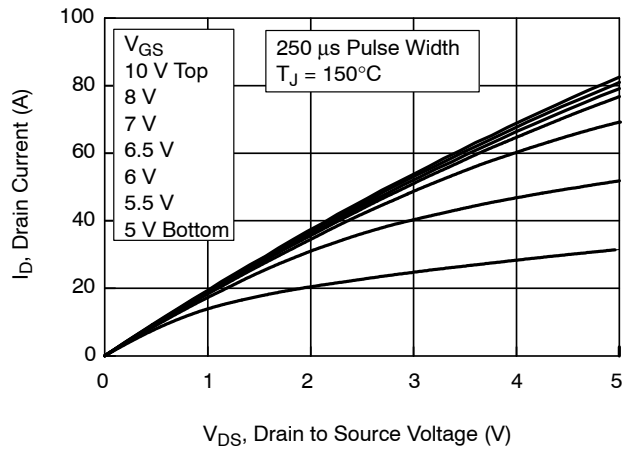
**Figure 6. Transfer Characteristic**



**Figure 7. Forward Diode Characteristics**



**Figure 8. Saturation Characteristics**



**Figure 9. Saturation Characteristics**

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## TYPICAL CHARACTERISTICS (continued)

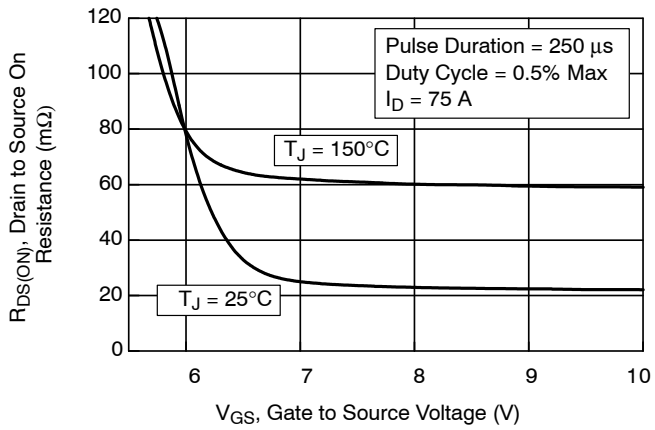


Figure 10.  $R_{DS(on)}$  vs. Gate Voltage

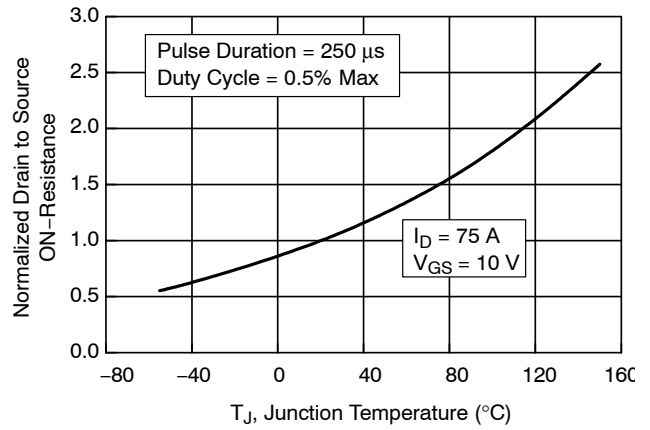


Figure 11. Normalized  $R_{DS(on)}$  vs. Junction Temperature

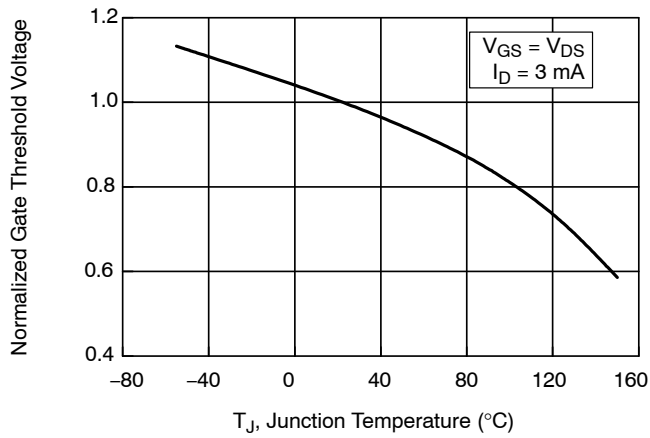


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

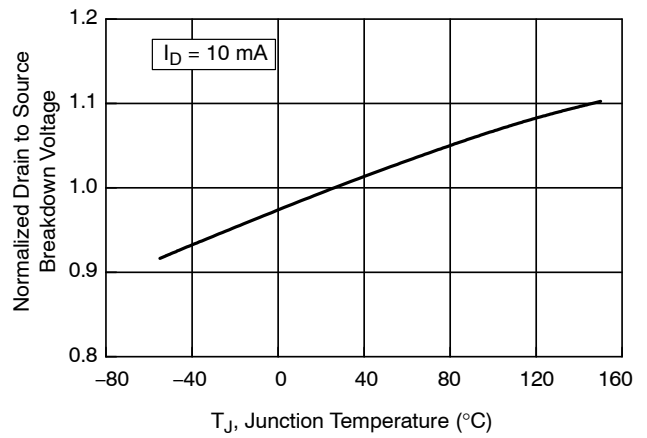


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

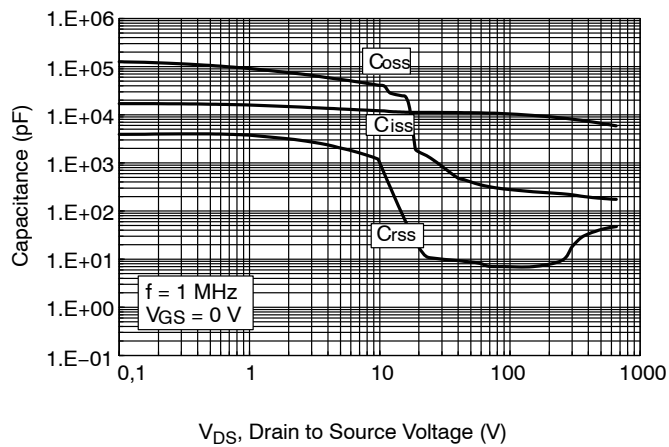


Figure 14. Capacitance vs. Drain to Source Voltage

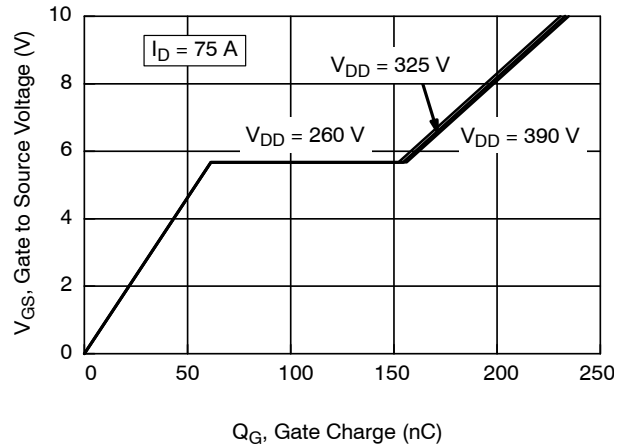


Figure 15. Gate Charge vs. Gate to Source Voltage

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## TYPICAL CHARACTERISTICS (continued)

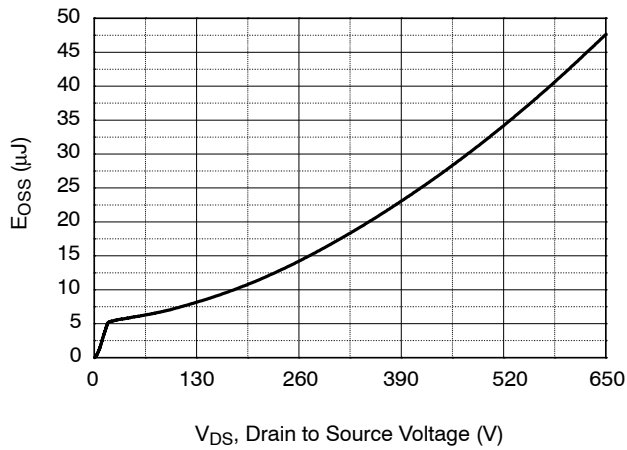


Figure 16. E<sub>OSS</sub> vs. Drain to Source Voltage

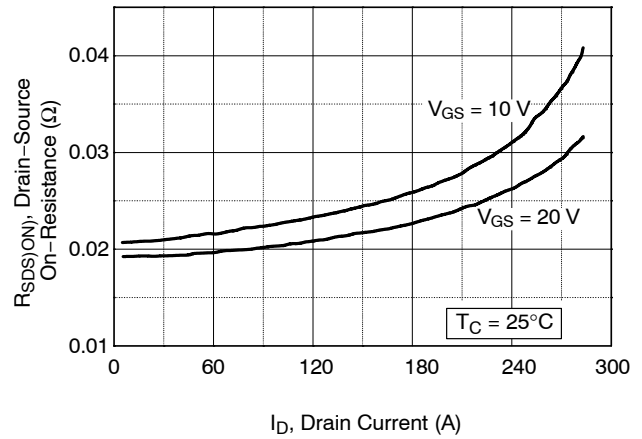


Figure 17. On-Resistance Variation vs. Drain Current and Gate Voltage

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