NVP2010 Data Sheet

CCD Image Signal Processor

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www.nextchip.com
2007.03.12
REV 0.0

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CCD Image Signal Processor

NVP2010 outputs CVBS or S-Video after receiving CFA patterns from the color-interlaced CCD, which are processed through an internal encoder and DAC. Equipped with built-in AE/AWB algorithms, timing generation module, NVP2010 can be operated without MICOM. NVP2010 can support high resolution output of 520 TV lines and has enhanced BLC function and motion detection function in 64 areas.

Features

-. Input : NTSC/PAL, 510H/760H CCD format
-. output : NTSC/PAL Analog S-Video or CVBS
-. 3-line color processing
-. Programmable GAMMA processing
-. H/V Aperture
-. Video adjustment (brightness, contrast, saturation and hue)
-. High quality color processing
-. Horizontal MIRROR
-. Blemish Compensation 32 points(Manual)
-. color rolling suppress.
-. Breathing suppress.
-. Support Horizontal Resolution 520TV Lines
-. Motion detection (64 area)
-. On-chip AE/AWB
-. On-chip CCD timing generator
-. On-chip NTSC/PAL video encoder
-. On-chip DAC(S-video or CVBS)
-. I^2C interface for EEPROM (MICOM less camera)
-. Serial interface for AFE
-. 3.3V operation

Ordering Information

Device	Package	Temperature Range
NVP2010	64-LQFP	0℃ ~ 70℃

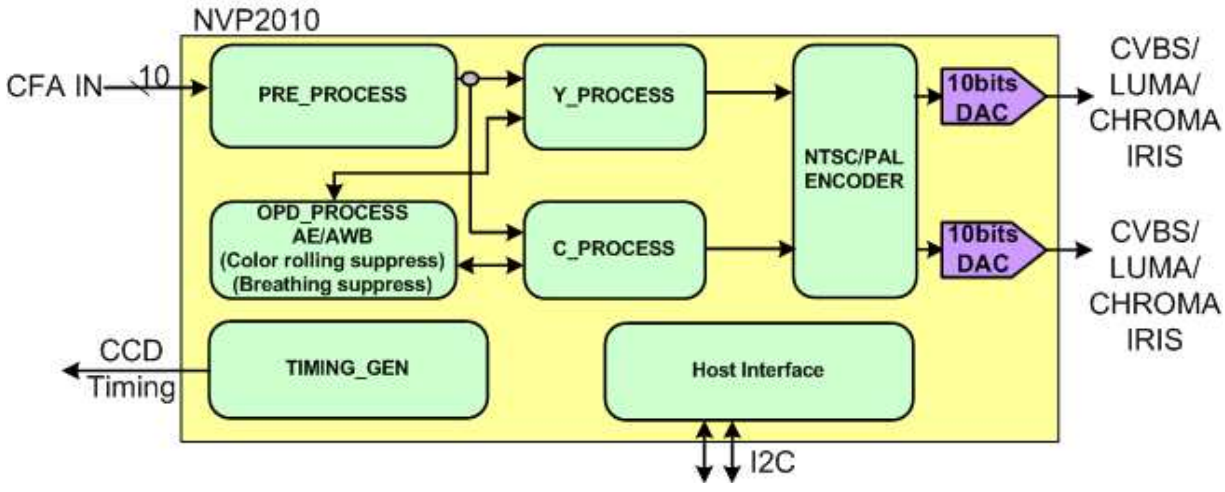
Applications

-. CCD Camera
-. Door Phone Camera
-. Video Phone Camera
-. Rear-view Monitoring Camera

Related Products

-. CCD : SONY, SHARP , PANASONIC CCD (510H/760H)
-. AFE : AD9806,AD9943 (Analog Device)
-. V-Driver : NVD2014 (NEXTCHIP)

Functional Block Diagram



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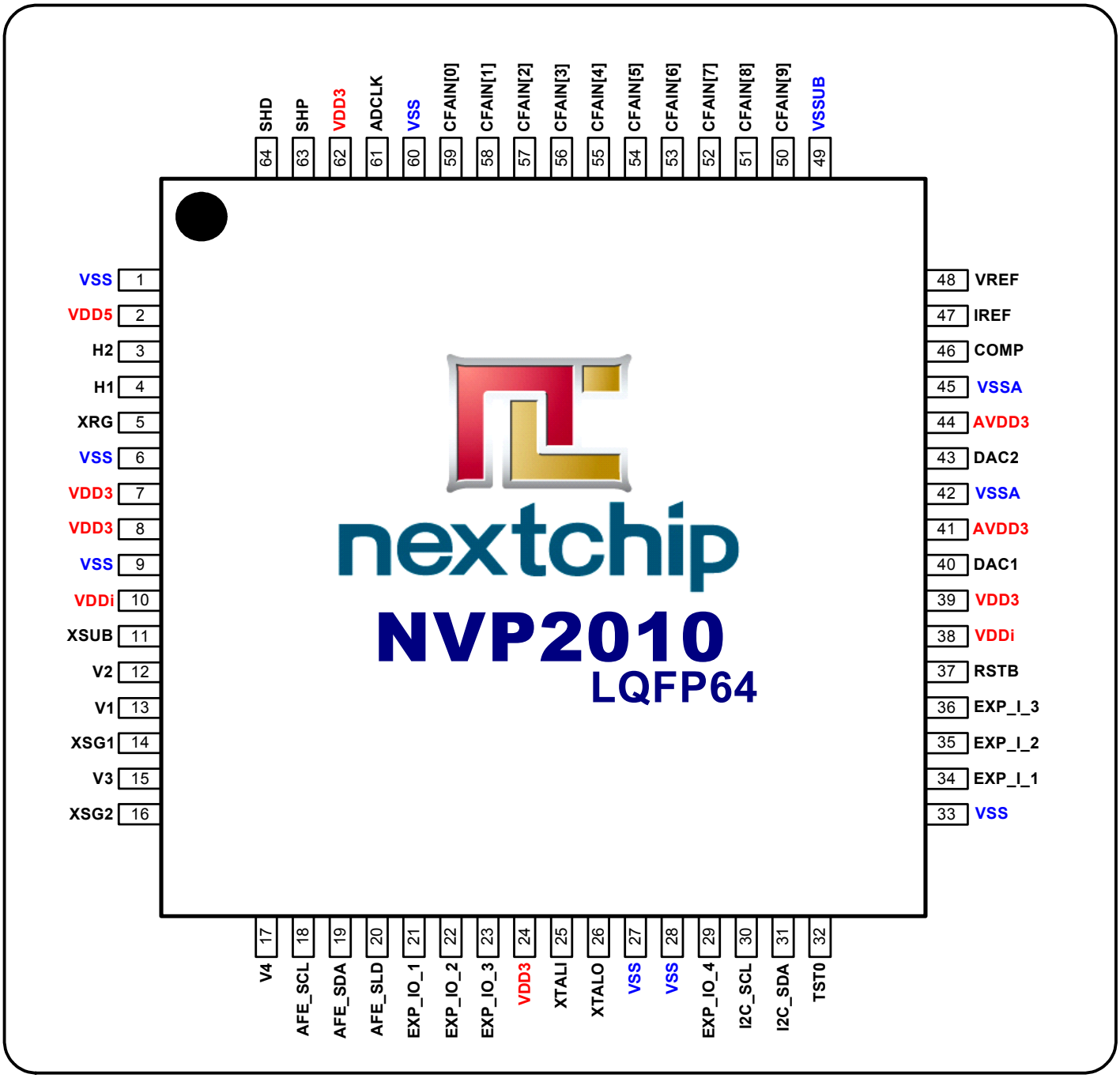
1. Pin Information

1.1 Pin Assignments



1.2 Pin Description

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	VSS	G	Digital Ground (for SHP, SHD)
2	VDD5	P	5V Digital Power (for XRG, H1, H2 pulse)
3	H2	O	CCD Horizontal Driving pulse 2
4	H1	O	CCD Horizontal Driving pulse 1
5	XRG	O	CCD Reset gate pulse
6	VSS	G	Digital Ground (for XRG, H1, H2 pulse)
7	VDD3	P	3.3V Digital Power
8	VDD3	P	3.3V Digital Power
9	VSS	G	Digital Ground
10	VDDi	P	1.8V Internal Core Power(Connect to VSS via external capacitor)
11	XSUB	O	CCD shutter speed control pulse
12	V2	O	CCD vertical driving pulse phase-2
13	V1	O	CCD vertical driving pulse phase-1
14	XSG1	O	CCD Read out pulse 1
15	V3	O	CCD vertical driving pulse phase-3
16	XSG2	O	CCD Read out pulse 2
17	V4	O	CCD vertical driving pulse phase-4
18	AFE_SCL	O	3-wire Serial interface clock output (for AFE control)
19	AFE_SDA	I/O	3-wire Serial data input/output (for AFE control)
20	AFE_SLD	O	3-wire Serial Enable output (for AFE control)
21	EXP_IO_1	I/O	External input/output control Pin
22	EXP_IO_2	I/O	External input/output control Pin
23	EXP_IO_3	I/O	External input/output control Pin
24	VDD3	P	3.3V Digital Power
25	XTALI	I	X-tal input(NTSC:28.6363MHz : PAL:28.375MHz)
26	XTALO	O	X-tal output
27	VSS	G	Digital Ground
28	VSS	G	Digital Ground
29	EXP_IO_4	I/O	External input/output control Pin
30	I2C_SCL	I/O	I2C Serial Clock (EEPROM/MICOM interface)
31	I2C_SDA	I/O	I2C Serial Data (EEPROM/MICOM interface)
32	TST0	I	Chip Test pin
33	VSS	G	Digital Ground
34	EXP_I_1	I	External input control Pin
35	EXP_I_2	I	External input control Pin
36	EXP_I_3	I	External input control Pin
37	RSTB	I	System Reset (active low)
38	VDDi	P	1.8V Internal Core Power(Connect to VSS via external capacitor)
39	VDD3	P	3.3V Digital Power
40	DAC1	O	DAC Output (LUMA/CHROMA/CVBS/IRIS/GND signal Output)
41	AVDD3	P	3.3V DAC Analog Power
42	VSSA	G	DAC Analog Ground
43	DAC2	O	DAC Output (LUMA/CHROMA/CVBS/IRIS/GND signal Output)
44	AVDD3	P	3.3V DAC Analog Power

PIN NO.	SYMBOL	I/O	DESCRIPTION
45	VSSA	G	DAC Analog Ground
46	COMP	-	DAC comparator reference
47	IREF	-	DAC current reference
48	VREF	-	DAC Voltage reference
49	VSSUB	G	DAC Analog Ground
50	CFAIN[9]	I	CCD CFA pattern input 9
51	CFAIN[8]	I	CCD CFA pattern input 8
52	CFAIN[7]	I	CCD CFA pattern input 7
53	CFAIN[6]	I	CCD CFA pattern input 6
54	CFAIN[5]	I	CCD CFA pattern input 5
55	CFAIN[4]	I	CCD CFA pattern input 4
56	CFAIN[3]	I	CCD CFA pattern input 3
57	CFAIN[2]	I	CCD CFA pattern input 2
58	CFAIN[1]	I	CCD CFA pattern input 1
59	CFAIN[0]	I	CCD CFA pattern input 0
60	VSS	G	Digital Ground
61	ADCLK	O	ADC sampling clock
62	VDD3	P	3.3V Digital Power (for SHP, SHD)
63	SHP	O	CDS sample & hold pulse for pre-charge
64	SHD	O	CDS sample & hold pulse for data

2. Register Information

2.1 Register Map

BANK 0										
ADDR		RESISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
-	0x00	0xAA								
-	0x01	0x55								
-	0x02	0xAA								
-	0x03	0x55								
0x00	0x04	H1_P	H2_P	H1_DELAY[5:0]						0x00
0x01	0x05	SHP_P	SHD_P	H2_DELAY[5:0]						0x00
0x02	0x06	RG_P	ADCLK_P	SHP_DELAY[5:0]						0x00
0x03	0x07	XSUB_P	PBLK_P	SHD_DELAY[5:0]						0x00
0x04	0x08	CLPOB_P	CLPDM_P	RG_DELAY[5:0]						0x00
0x05	0x09	NTSC	HIGH	ADCLK_DELAY[5:0]						0x80
0x06	0x0A	CCD_TYPE[1:0]		H1_WIDTH[2:0]			H2_WIDTH[2:0]			0x00
0x07	0x0B	1'b0	SEL_27M	SHD_WIDTH[2:0]			SHP_WIDTH[2:0]			0x00
0x08	0x0C	H1_HW	H2_HW	SHP_HW	SHD_HW	RG_HW	RG_WIDTH[2:0]			0x00
0x09	0x0D	AFE_00[15:8]								0x00
0x0A	0x0E	AFE_00[07:0]								0x20
0x0B	0x0F	AFE_01[15:8]								0x82
0x0C	0x10	AFE_01[07:0]								0x00
0x0D	0x11	AFE_02[15:8]								0x40
0x0E	0x12	AFE_02[07:0]								0x00
0x0F	0x13	AFE_03[15:8]								0xC0
0x10	0x14	AFE_03[07:0]								0x00
0x11	0x15	AFE_04[15:8]								0x00
0x12	0x16	AFE_04[07:0]								0x00
0x13	0x17	PGA_LENGTH[2:0]			PGA_DUMMY[1:0]		PGA_LOC[2:0]			0x04
0x14	0x18	CLAMP	AFE_PCON	PGA_ADDR[5:0]						0x70
0x15	0x19	CLAMP_REG[4:0]					DAY_IR_P	CLAMP_LEVEL[1:0]		0x43
0x16	0x1A	H_OFFSET								0x40
0x17	0x1B	BPF_SEL[1:0]		SHPD_TYPE	H_SIZE[3:0]				HP_DLL_EN	0x80
0x18	0x1C	Y_GAIN								0x4C
0x19	0x1D	H_EDGE_OFF	Y_CLIP[6:0]							0xB1
0x1A	0x1E	1'b0	DAY_EX[1:0]		1'b0	MIRROR_POS[3:0]				0x00
0x1B	0x1F	Y_GAMMA0								0x01
0x1C	0x20	Y_GAMMA1								0x10
0x1D	0x21	Y_GAMMA2								0x25
0x1E	0x22	Y_GAMMA3								0x41
0x1F	0x23	Y_GAMMA4								0x68
0x20	0x24	Y_GAMMA5								0x9E
0x21	0x25	Y_GAMMA6								0xE7
0x22	0x26	Y_GAMMA7								0xFF
0x23	0x27	HAP_SLICE1[3:0]				HAP_SLICE2[3:0]				0x45
0x24	0x28	VAP_SLICE[3:0]				VAP_GAIN[3:0]				0x45
0x25	0x29	8'b0								0x00
0x26	0x2A	PEAK_GAIN[2:0]			HAP_GAIN1[4:0]					0x0A
0x27	0x2B	1'b0	1'b0	1'b0	HAP_GAIN2[4:0]					0x09
0x28	0x2C	BF_DLY[3:0]				PEAK_SLICE[3:0]				0x63
0x29	0x2D	SUE_AGC_LEVEL								0x22
0x2A	0x2E	SUC_AGC_GAIN[3:0]				SUE_AGC_GAIN[3:0]				0x28
0x2B	0x2F	SUC_AGC_LEVEL								0x30
0x2C	0x30	SUC_HL_HLEVEL[3:0]				SUC_HL_LLEVEL[3:0]				0x90
0x2D	0x31	SUC_HL_GAIN[3:0]				SUC_EDGE_GAIN[3:0]				0x31
0x2E	0x32	C_GAMMA0								0x01

BANK 0										
ADDR		RESISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0x2F	0x33	C_GAMMA1								0x10
0x30	0x34	C_GAMMA2								0x25
0x31	0x35	C_GAMMA3								0x41
0x32	0x36	C_GAMMA4								0x68
0x33	0x37	C_GAMMA5								0x9E
0x34	0x38	C_GAMMA6								0xE7
0x35	0x39	C_GAMMA7								0xFF
0x36	0x3A	GAIN_RS1								0x80
0x37	0x3B	GAIN_RS2								0x80
0x38	0x3C	GAIN_BS1								0x80
0x39	0x3D	GAIN_BS2								0x80
0x3A	0x3E	CCY_GAIN								0x80
0x3B	0x3F	CCR_GAIN								0x80
0x3C	0x40	CCB_GAIN								0x80
0x3D	0x41	1'b0	CFIR_SEL	CLP_RS1[5:0]						0x3F
0x3E	0x42	CCRB_ID	S1_ID	CLP_RS2[5:0]						0xBF
0x3F	0x43	TEST_PATTERN[1:0]		CLP_BS1[5:0]						0xFF
0x40	0x44	YFIR_SEL[1:0]		CLP_BS2[5:0]						0x3F
0x41	0x45	CCORR								0xA0
0x42	0x46	CCORG								0x2E
0x43	0x47	CCORB								0x4E
0x44	0x48	CCOGR								0x6C
0x45	0x49	CCOGG								0x87
0x46	0x4A	CCOGB								0xAC
0x47	0x4B	CCOBR								0xC6
0x48	0x4C	CCOBG								0x52
0x49	0x4D	CCOBB								0xC4
0x4A	0x4E	RWB								0x5A
0x4B	0x4F	GWB								0x4A
0x4C	0x50	BWB								0x51
0x4D	0x51	RBLK								0x00
0x4E	0x52	GBLK								0x00
0x4F	0x53	BBLK								0x00
0x50	0x54	CR_GAIN								0x80
0x51	0x55	CB_GAIN								0x80
0x52	0x56	HUE1								0x00
0x53	0x57	HUE2								0x00
0x54	0x58	HUE3								0x00
0x55	0x59	HUE4								0x00
0x56	0x5A	HUE5								0x00
0x57	0x5B	HUE6								0x00
0x58	0x5C	UV_GAIN1								0x80
0x59	0x5D	UV_GAIN2								0x80
0x5A	0x5E	UV_GAIN3								0x80
0x5B	0x5F	UV_GAIN4								0x80
0x5C	0x60	UV_GAIN5								0x80
0x5D	0x61	UV_GAIN6								0x80
0x5E	0x62	BLC	BLC_AREA_VIEW	BLC_GAIN[5:0]						0x95
0x5F	0x63	MOTION_AGC[3:0]				MOTION_HIGH[3:0]				0x40
0x60	0x64	AE_LEVEL								0x54
0x61	0x65	BLC_LEVEL								0x40
0x62	0x66	MOTION_THL								0x0F
0x63	0x67	DAY_EXT_IN_P	1'b0	1'b0	1'b0	IRIS_LG_ON	IRIS_DAC_PORT	1'b0	1'b0	0x08
0x64	0x68	MAX1_AGC								0xD0
0x65	0x69	MAX2_AGC								0x00
0x66	0x6A	ESS_ZONE[3:0]				AED_ZONE[3:0]				0x75

BANK 0										
ADDR		RESISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0x67	0x6B	ESS_SDLY[3:0]				AGC_SDLY[3:0]				0x00
0x68	0x6C	AE_DG_REG[9:8]		AGC_REG[9:8]		AE_SPD[3:0]				0x4F
0x69	0x6D	AE_DG_REG[7:0]								0x00
0x6A	0x6E	AGC_REG[7:0]								0x00
0x6B	0x6F	AE_MODE[1:0]		SSM[2:0]			MOTION_TEST	IRIS_LENS[1:0]		0x42
0x6C	0x70	BTN_REPT_ON	1'b0	1'b0	ME_ESS[12:8]					0x80
0x6D	0x71	ME_ESS[7:0]								0x15
0x6E	0x72	R_MAX								0x8D
0x6F	0x73	B_MAX								0x43
0x70	0x74	R_MIN								0x64
0x71	0x75	B_MIN								0xCB
0x72	0x76	AWB_HIGH								0xF0
0x73	0x77	AWB_MODE[1:0]		AWB_DIP[1:0]		1'b0	1'b0	1'b0	1'b0	0x40
0x74	0x78	AWB_LOW								0x07
0x75	0x79	R_CLP[3:0]				B_CLP[3:0]				0xFF
0x76	0x7A	INTVAL_H[3:0]				INTVAL_L[3:0]				0x44
0x77	0x7B	AWB_SPD[3:0]				STA_ZONE[3:0]				0xF4
0x78	0x7C	STA_IN_LMT[3:0]				STA_OUT_LMT[3:0]				0x11
0x79	0x7D	8'b0								0x00
0x7A	0x7E	AWB_R0								0x40
0x7B	0x7F	AWB_R1								0x04
0x7C	0x80	AWB_R2								0x6D
0x7D	0x81	AWB_R3								0x42
0x7E	0x82	AWB_B0								0x40
0x7F	0x83	AWB_B1								0x00
0x80	0x84	AWB_B2								0xEE
0x81	0x85	AWB_B3								0x3C
0x82	0x86	AWB_R_OFFSET								0x10
0x83	0x87	AWB_B_OFFSET								0x08
0x84	0x88	DAY_NIGHT_START								0xC3
0x85	0x89	DAY_NIGHT_END								0x97
0x86	0x8A	DAY_ON[1:0]		DAY_DLY[5:0]						0x41
0x87	0x8B	SEL_EXPO_02[3:0]				SEL_EXPO_01[3:0]				0x00
0x88	0x8C	SEL_EXPO_04[3:0]				SEL_EXPO_03[3:0]				0x00
0x89	0x8D	8'b0								0x00
0x8A	0x8E	1'b0	1'b0	1'b0	SC_OFFSET[4:0]					0x00
0x8B	0x8F	DEF_M_SEL[4:0]				1'b0	DAY_EXT_IN_REG	1'b0		0x00
0x8C	0x90	HXV_OFFSET								0x00
0x8D	0x91	PRE_Y_GAIN								0x80
0x8E	0x92	EDGE_S[3:0]				EDGE_E[3:0]				0x02
0x8F	0x93	1'b0	MOTION_EN	M_VIEW_ON	DAY_BURST_ON	1'b0	1'b0	1'b0	1'b0	0x50
0x90	0x94	Fix '1'b0'								0x00
0x91	0x95									0x00
0x92	0x96									0x00
0x93	0x97									0x00
0x94	0x98									0x00
0x95	0x99									0x00
0x96	0x9A									0x00
0x97	0x9B									0x00
0x98	0x9C									0x00
0x99	0x9D									0x00
0x9A	0x9E									0x00
0x9B	0x9F									0x00
0x9C	0xA0									0x00
0x9D	0xA1									0x00
0x9E	0xA2									0x00

BANK 0										
ADDR		RESISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0x9F	0xA3	8'b0								0x00
0xA0	0xA4	POWER_FRE [1:0]		IRIS_P	HVAP_GAIN[4:0]					0x50
0xA1	0xA5	MOTION_TH_AREA[3:0]				SEL_IRIS_LENS[3:0]				0x00
0xA2	0xA6	8'b0								0x00
0xA3	0xA7	MIRROR	M_CURSOR_ON	M_CURSOR[5:0]						0x00
0xA4	0xA8	AWB_M_R								0x40
0xA5	0xA9	AWB_M_B								0x40
0xA6	0xAA	IRIS_LEVEL								0x40
0xA7	0xAB	IRIS_GAIN								0x80
0xA8	0xAC	BTN_DLY				1'b0	1'b0	1'b0	1'b0	0x50
0xA9	0xAD	Y_OFFSET								0x00
0xAA	0xAE	U_BURST[9:8]		SYNC_REG[5:0]						0xCE
0xAB	0xAF	V_BURST[9:8]		BLACK_REG[5:0]						0x15
0xAC	0xB0	U_BURST[7:0]								0x9F
0xAD	0xB1	V_BURST[7:0]								0x00
0xAE	0xB2	IRIS_DC[1:0]		IRIS_BLC_OFFSET[4:0]					DAC_P	0x09
0xAF	0xB3	DAC1_OUT[3:0]				DAC2_OUT[3:0]				0x00
0xB0	0xB4	MOTION_TH								0x22
0xB1	0xB5	MOTION_THF[3:0]				SLPF_SEL	AE_OUT_LMT[2:0]			0x08
0xB2	0xB6	MOTION_AREA[63:56]								0xFF
0xB3	0xB7	MOTION_AREA[55:48]								0xFF
0xB4	0xB8	MOTION_AREA[47:40]								0xFF
0XB5	0xB9	MOTION_AREA[39:32]								0xFF
0xB6	0xBA	MOTION_AREA[31:24]								0xFF
0xB7	0xBB	MOTION_AREA[23:16]								0xFF
0xB8	0xBC	MOTION_AREA[15:8]								0xFF
0xB9	0xBD	MOTION_AREA[7:0]								0xFF
0xBA	0xBE	BLC_AREA_SEL[63:56]								0xFF
0xBB	0xBF	BLC_AREA_SEL[55:48]								0xFF
0xBC	0xC0	BLC_AREA_SEL[47:40]								0xFF
0xBD	0xC1	BLC_AREA_SEL[39:32]								0xFF
0xBE	0xC2	BLC_AREA_SEL[31:24]								0xFF
0xBF	0xC3	BLC_AREA_SEL[23:16]								0xFF
0xC0	0xC4	BLC_AREA_SEL[15:8]								0xFF
0xC1	0xC5	BLC_AREA_SEL[7:0]								0xFF
0xC2	0xC6	SEL_DAY_EXT[3:0]				SEL_MIRROR[3:0]				0x00
0xC3	0xC7	SEL_BLC[3:0]				SEL_AGC[3:0]				0x00
0xC4	0xC8	SEL_AE1[3:0]				SEL_AE0[3:0]				0x00
0XC5	0xC9	SEL_SSM1[3:0]				SEL_SSM0[3:0]				0x00
0xC6	0xCA	4'b0				SEL_SSM2[3:0]				0x00
0xC7	0xCB	IRIS_GMAX[3:0]				IRIS_GMIN[3:0]				0x00
0xC8	0xCC	IR_GAIN[7:0]								0x00
0xC9	0xCD	Fix '1'b0'								0x00
0xCA	0xCE									0x00
0xCB	0xCF									0x00
0xCC	0xD0									0x00
0xCD	0xD1									0x00
0xCE	0xD2									0x00
0xCF	0xD3									0x00
0xD0	0xD4									0x00
0xD1	0xD5									0x00
0xD2	0xD6									0x00
0xD3	0xD7									0x00
0xD4	0xD8									0x00
0xD5	0xD9									0x00
0xD6	0xDA									0x00

BANK 0										
ADDR		RESISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0xD7	0xDB	Fix '1'b0'								0x00
0xD8	0xDC									0x00
0xD9	0xDD									0x00
0xDA	0xDE									0x00
0xDB	0xDF									0x00
0xDC	0xE0	MAX_AGC_SEL	1'b0	1'b0	Fix '1'b0'					0x80
0xDD	0xE1	DAY_MOTOR_P	DAY_PULSE_SEL[1:0]							0x80
0xDE	0xE2	1'b0	1'b0	1'b0						0x00
0xDF	0xE3	1'b0	BLK_TH[1:0]							0x00
0xE0	0xE4	NEGATIVE_IMG	BLK_GAIN[1:0]							0x00
0xE1	0xE5	HPF_SEL	HAP_CLIP1[1:0]							0xE0
0xE2	0xE6	1'b0	VAP_CLIP[1:0]							0x60
0xE3	0xE7	AWB_AE_DETECT	AWB_METHOD1[1:0]							0x80
0xE4	0xE8	AWB_TR_CLIP	AWB_METHOD2[1:0]							0xF0
0xE5	0xE9	AWB_METHOD3	AE_GMAX[1:0]							0x40
0xE6	0xEA	1'b0	1'b0	HAP_SUP_SEL						0x20
0xE7	0xEB	1'b0	1'b0	1'b0						0x00
0xE8	0xEC	AFE_DAC2_ON	1'b0	1'b0						0x00
0xE9	0xED	1'b0	1'b0	1'b0						0x00
0xEA	0xEE	1'b0	Y_CLIP_TH[1:0]							0x00
0xEB	0xEF	MOTION_DELAY[1:0]		1'b0						0x80
0xEC	0xF0	CLPOB_SIZE[3:0]				CLPOB_POS[3:0]				0x88
0xED	0xF1	Fix '1'b0'								0x00
0xEE	0xF2									0x00
0xEF	0xF3									0x00
0xF0	0xF4	AFE_DAC1_ON	IRIS_AFE_DC	INIT_SCR	ADC_SET	SLAVE_ADDR[3:0]				0x05
0xF1	0xF5	bank_reg								0x00
0xF2	0xF6	Fix '1'b0'								0x00
0xF3	0xF7									0x00
0xF4	0xF8									0x00
0xF5	0xF9									0x00
0xF6	0xFA									0x00
0xF7	0xFB									0x00
0xF8	0xFC	test1					DAC1_SL	DAC2_SL	1'b0	0x18
0xF9	0xFD	SD_H1[1:0]		SL_H1	SD_H2[1:0]		1'b0	SL_H2	1'b0	0x00
0xFA	0xFE	SD_RG[1:0]		SL_RG	HAP_SUPPRESS[4:0]					0x00

BANK 1										
ADDR		RESISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0x01	0x01	8'b0								0x00
0x02	0x02	COMPEN_START								0x00
0x03	0x03	Fix '1'b0'					1'b0	1'b0	1'b0	0x00
0x04	0x04						DEFECT_MANUAL	1'b0	1'b0	0x00
0x05	0x05						1'b0	1'b0	1'b0	0x00
0x08	0x08	DEF_V_00[9:8]		DEF_V_01[9:8]		DEF_V_02[9:8]		DEF_V_03[9:8]		0x00
0x09	0x09	DEF_H_00[7:0]								0x00
0x0A	0x0A	DEF_V_00[7:0]								0x00
0x0B	0x0B	DEF_H_00[9:8]		DEF_D_00[5:0]						0x00
0x0C	0x0C	DEF_H_01[7:0]								0x00
0x0D	0x0D	DEF_V_01[7:0]								0x00
0x0E	0x0E	DEF_H_01[9:8]		DEF_D_01[5:0]						0x00
0x0F	0x0F	DEF_H_02[7:0]								0x00
0x10	0x10	DEF_V_02[7:0]								0x00
0x11	0x11	DEF_H_02[9:8]		DEF_D_02[5:0]						0x00
0x12	0x12	DEF_H_03[7:0]								0x00
0x13	0x13	DEF_V_03[7:0]								0x00
0x14	0x14	DEF_H_03[9:8]		DEF_D_03[5:0]						0x00
0x15	0x15	DEF_V_04[9:8]		DEF_V_05[9:8]		DEF_V_06[9:8]		DEF_V_07[9:8]		0x00
0x16	0x16	DEF_H_04[7:0]								0x00
0x17	0x17	DEF_V_04[7:0]								0x00
0x18	0x18	DEF_H_04[9:8]		DEF_D_04[5:0]						0x00
0x19	0x19	DEF_H_05[7:0]								0x00
0x1A	0x1A	DEF_V_05[7:0]								0x00
0x1B	0x1B	DEF_H_05[9:8]		DEF_D_05[5:0]						0x00
0x1C	0x1C	DEF_H_06[7:0]								0x00
0x1D	0x1D	DEF_V_06[7:0]								0x00
0x1E	0x1E	DEF_H_06[9:8]		DEF_D_06[5:0]						0x00
0x1F	0x1F	DEF_H_07[7:0]								0x00
0x20	0x20	DEF_V_07[7:0]								0x00
0x21	0x21	DEF_H_07[9:8]		DEF_D_07[5:0]						0x00
0x22	0x22	DEF_V_08[9:8]		DEF_V_09[9:8]		DEF_V_10[9:8]		DEF_V_11[9:8]		0x00
0x23	0x23	DEF_H_08[7:0]								0x00
0x24	0x24	DEF_V_08[7:0]								0x00
0x25	0x25	DEF_H_08[9:8]		DEF_D_08[5:0]						0x00
0x26	0x26	DEF_H_09[7:0]								0x00
0x27	0x27	DEF_V_09[7:0]								0x00
0x28	0x28	DEF_H_09[9:8]		DEF_D_09[5:0]						0x00
0x29	0x29	DEF_H_10[7:0]								0x00
0x2A	0x2A	DEF_V_10[7:0]								0x00
0x2B	0x2B	DEF_H_10[9:8]		DEF_D_10[5:0]						0x00
0x2C	0x2C	DEF_H_11[7:0]								0x00
0x2D	0x2D	DEF_V_11[7:0]								0x00
0x2E	0x2E	DEF_H_11[9:8]		DEF_D_11[5:0]						0x00
0x2F	0x2F	DEF_V_12[9:8]		DEF_V_13[9:8]		DEF_V_14[9:8]		DEF_V_15[9:8]		0x00
0x30	0x30	DEF_H_12[7:0]								0x00
0x31	0x31	DEF_V_12[7:0]								0x00
0x32	0x32	DEF_H_12[9:8]		DEF_D_12[5:0]						0x00
0x33	0x33	DEF_H_13[7:0]								0x00
0x34	0x34	DEF_V_13[7:0]								0x00
0x35	0x35	DEF_H_13[9:8]		DEF_D_13[5:0]						0x00
0x36	0x36	DEF_H_14[7:0]								0x00
0x37	0x37	DEF_V_14[7:0]								0x00
0x38	0x38	DEF_H_14[9:8]		DEF_D_14[5:0]						0x00
0x39	0x39	DEF_H_15[7:0]								0x00
0x3A	0x3A	DEF_V_15[7:0]								0x00

BANK 1										
ADDR		RESISTER								DEF.
ISP	EEPROM	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0x3B	0x3B	DEF_H_15[9:8]		DEF_D_15[5:0]						0x00
0x3C	0x3C	DEF_V_16[9:8]		DEF_V_17[9:8]		DEF_V_18[9:8]		DEF_V_19[9:8]		0x00
0x3D	0x3D	DEF_H_16[7:0]								0x00
0x3E	0x3E	DEF_V_16[7:0]								0x00
0x3F	0x3F	DEF_H_16[9:8]		DEF_D_16[5:0]						0x00
0x40	0x40	DEF_H_17[7:0]								0x00
0x41	0x41	DEF_V_17[7:0]								0x00
0x42	0x42	DEF_H_17[9:8]		DEF_D_17[5:0]						0x00
0x43	0x43	DEF_H_18[7:0]								0x00
0x44	0x44	DEF_V_18[7:0]								0x00
0x45	0x45	DEF_H_18[9:8]		DEF_D_18[5:0]						0x00
0x46	0x46	DEF_H_19[7:0]								0x00
0x47	0x47	DEF_V_19[7:0]								0x00
0x48	0x48	DEF_H_19[9:8]		DEF_D_19[5:0]						0x00
0x49	0x49	DEF_V_20[9:8]		DEF_V_21[9:8]		DEF_V_22[9:8]		DEF_V_23[9:8]		0x00
0x4A	0x4A	DEF_H_20[7:0]								0x00
0x4B	0x4B	DEF_V_20[7:0]								0x00
0x4C	0x4C	DEF_H_20[9:8]		DEF_D_20[5:0]						0x00
0x4D	0x4D	DEF_H_21[7:0]								0x00
0x4E	0x4E	DEF_V_21[7:0]								0x00
0x4F	0x4F	DEF_H_21[9:8]		DEF_D_21[5:0]						0x00
0x50	0x50	DEF_H_22[7:0]								0x00
0x51	0x51	DEF_V_22[7:0]								0x00
0x52	0x52	DEF_H_22[9:8]		DEF_D_22[5:0]						0x00
0x53	0x53	DEF_H_23[7:0]								0x00
0x54	0x54	DEF_V_23[7:0]								0x00
0x55	0x55	DEF_H_23[9:8]		DEF_D_23[5:0]						0x00
0x56	0x56	DEF_V_24[9:8]		DEF_V_25[9:8]		DEF_V_26[9:8]		DEF_V_27[9:8]		0x00
0x57	0x57	DEF_H_24[7:0]								0x00
0x58	0x58	DEF_V_24[7:0]								0x00
0x59	0x59	DEF_H_24[9:8]		DEF_D_24[5:0]						0x00
0x5A	0x5A	DEF_H_25[7:0]								0x00
0x5B	0x5B	DEF_V_25[7:0]								0x00
0x5C	0x5C	DEF_H_25[9:8]		DEF_D_25[5:0]						0x00
0x5D	0x5D	DEF_H_26[7:0]								0x00
0x5E	0x5E	DEF_V_26[7:0]								0x00
0x5F	0x5F	DEF_H_26[9:8]		DEF_D_26[5:0]						0x00
0x60	0x60	DEF_H_27[7:0]								0x00
0x61	0x61	DEF_V_27[7:0]								0x00
0x62	0x62	DEF_H_27[9:8]		DEF_D_27[5:0]						0x00
0x63	0x63	DEF_V_28[9:8]		DEF_V_29[9:8]		DEF_V_30[9:8]		DEF_V_31[9:8]		0x00
0x64	0x64	DEF_H_28[7:0]								0x00
0x65	0x65	DEF_V_28[7:0]								0x00
0x66	0x66	DEF_H_28[9:8]		DEF_D_28[5:0]						0x00
0x67	0x67	DEF_H_29[7:0]								0x00
0x68	0x68	DEF_V_29[7:0]								0x00
0x69	0x69	DEF_H_29[9:8]		DEF_D_29[5:0]						0x00
0x6A	0x6A	DEF_H_30[7:0]								0x00
0x6B	0x6B	DEF_V_30[7:0]								0x00
0x6C	0x6C	DEF_H_30[9:8]		DEF_D_30[5:0]						0x00
0x6D	0x6D	DEF_H_31[7:0]								0x00
0x6E	0x6E	DEF_V_31[7:0]								0x00
0x6F	0x6F	DEF_H_31[9:8]		DEF_D_31[5:0]						0x00
0x70	0x70	AED_SPD	V_OFFSET[2:0]			1'b0	1'b0	1'b0	1'b0	0x30
0x71	0x71	SEL_IRISL[3:0]				SEL_IRISR[3:0]				0x00
0x72	0x72	1'b0	1'b0	1'b0	1'b0	SEL_MOTION[3:0]				0x00

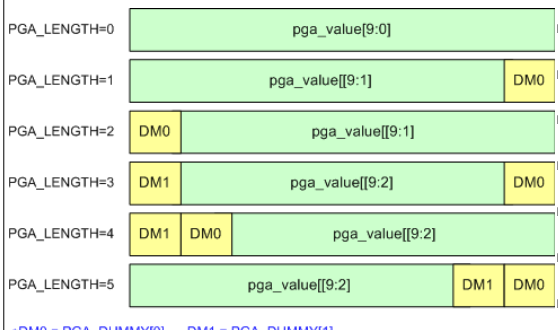
※ Read only register

BANK 0x81									
ADDR	RESISTER								DEF.
ISP	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0x81	ACC_BLC_MSB								-
0x82	ACC_BLC_LSB								-
0x83	ACC_NBLC_MSB								-
0x84	ACC_NBLC_LSB								-
0x85	AE_ES_MSB								-
0x86	AE_ES_LSB								-
0x87	AGC								-
0x88	AE_DIGT_GAIN								-
0x89	AE_ACC								-
0x8A	AWB_R								-
0x8B	AWB_B								-
0x8C	AWB_TARGET_R								-
0x8D	AWB_TARGET_B								-

2.2 Register Explanation

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x00	[7]	H1_P	· H1 pulse phase change · 0 : Normal 1: change	R/W	0x00
	[6]	H2_P	· H2 pulse phase change · 0 : Normal 1: change		
	[5:0]	H1_DELAY	· H1 pulse delay adjustment · range : 0 ~ 63ns		
0x01	[7]	SHP_P	· SHP pulse phase change · 0 : Normal 1: change	R/W	0x00
	[6]	SHD_P	· SHD pulse phase change · 0 : Normal 1: change		
	[5:0]	H2_DELAY	· H2 pulse delay adjustment · range : 0 ~ 63ns		
0x02	[7]	RG_P	· RG pulse phase change · 0 : Normal 1: change	R/W	0x00
	[6]	ADCLK_P	· ADCLK pulse phase change · 0 : Normal 1: change		
	[5:0]	SHP_DELAY	· SHP pulse delay adjustment · range : 0 ~ 63ns		
0x03	[7]	XSUB_P	· XSUB pulse phase change · 0 : Normal 1: change	R/W	0x00
	[6]	PBLK_P	· PBLK pulse phase change · 0 : Normal 1: change		
	[5:0]	SHD_DELAY	· SHD pulse delay adjustment · range : 0 ~ 63ns		
0x04	[7]	CLPOB_P	· CLPOB pulse phase change · 0 : Normal 1: change	R/W	0x00
	[6]	CLPDM_P	· CLPDM pulse phase change · 0 : Normal 1: change		
	[5:0]	RG_DELAY	· XRG pulse delay adjustment · range : 0 ~ 63ns		
0x05	[7]	NTSC	· NTSC · 0 : PAL 1: NTSC	R/W	0x80
	[6]	HIGH	· CCD resolution selection · 0 : NORMAL(270K) 1 : HI8(410K)		
	[5:0]	ADCLK_DELAY	· ADCLK pulse delay adjustment · range : 0 ~ 63ns		
0x06	[7:6]	CCD_TYPE	· CCD type selection · 0: SONY 1 : SHARP 2: PANASONIC	R/W	0x00
	[5:3]	H1_WIDTH	· H1 pulse width adjustment. · range : 0 ~ 7ns		
	[2:0]	H2_WIDTH	· H2 pulse width adjustment. · range : 0 ~ 7ns		

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x07	[7]	Fix	· Fix at 1'b0.	R/W	0x00
	[6]	SEL_27M	· System clock selection · 0 : CCD(NTSC :28.6363MHz or PAL :28.375MHz) 1 : 27MHz		
	[5:3]	SHD_WIDTH	· SHD pulse width adjustment (0 ~ 7ns)		
	[2:0]	SHP_WIDTH	· SHP pulse width adjustment (0 ~ 7ns)		
0x08	[7]	H1_HW	· Select H1 pulse width (0: High band 1: Low band)	R/W	0x00
	[6]	H2_HW	· Select H2 pulse width (0: High band 1: Low band)		
	[5]	SHP_HW	· Select SHP pulse width (0: High band 1: Low band)		
	[4]	SHD_HW	· Select SHD pulse width (0: High band 1: Low band)		
	[3]	RG_HW	· Select RG pulse width (0: High band 1: Low band)		
	[2:0]	RG_WIDTH	· RG pulse width adjustment (0 ~ 7ns)		
0x09		AFE_00[15:8]	· 1st AFE internal setting register	R/W	0x00
0x0A		AFE_00[07:0]		R/W	0x20
0x0B		AFE_01[15:8]	· 2nd AFE internal setting register	R/W	0x82
0x0C		AFE_01[07:0]		R/W	0x00
0x0D		AFE_02[15:8]	· 3rd AFE internal setting register	R/W	0x40
0x0E		AFE_02[07:0]		R/W	0x00
0x0F		AFE_03[15:8]	· 4th AFE internal setting register	R/W	0xC0
0x10		AFE_03[07:0]		R/W	0x00
0x11		AFE_04[15:8]	· 5th AFE internal setting register	R/W	0x00
0x12		AFE_04[07:0]		R/W	0x00
0x13	[2:0]	PGA_LENGTH	· Select PGA length.	R/W	0x04
	[1:0]	PGA_DUMMY	· Fill 1 or 2 bits if PGA is not 10 bits.		
	[2:0]	PGA_LOC	· Change address order of PGA.		
0x14	[7]	CLAMP	· Auto Clamp On/Off · 0 : OFF 1 : ON	R/W	0x70
	[6]	AFE_PCON	· Change the bit order of PGA.		
	[5:0]	PGA_ADDR	· Assign PGA address to each address.	R/W	



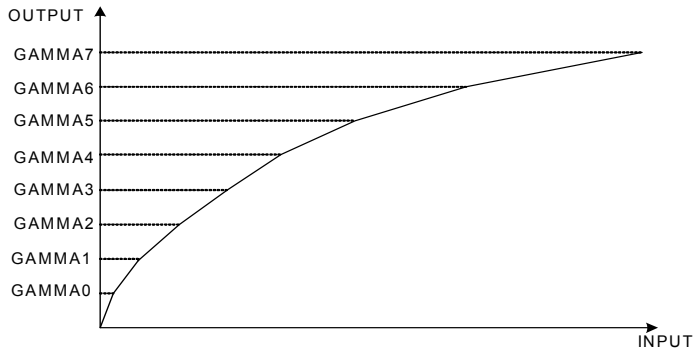
*DM0 = PGA_DUMMY[0], DM1 = PGA_DUMMY[1]

PGA_LOC=0	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	AD0	AD1	AD2	AD3	AD4	AD5
PGA_LOC=1	AD0	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	AD1	AD2	AD3	AD4	AD5
PGA_LOC=2	AD0	AD1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	AD2	AD3	AD4	AD5
PGA_LOC=3	AD0	AD1	AD2	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	AD3	AD4	AD5
PGA_LOC=4	AD0	AD1	AD2	AD3	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	AD4	AD5
PGA_LOC=5	AD0	AD1	AD2	AD3	AD4	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	AD5
PGA_LOC=6	AD0	AD1	AD2	AD3	AD4	AD5	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

* AD0 = PGA_ADDR[0], AD1 = PGA_ADDR[1], AD2 = PGA_ADDR[2]
AD3 = PGA_ADDR[3], AD4 = PGA_ADDR[4], AD5 = PGA_ADDR[5]

AFE_PCON=1	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
AFE_PCON=0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

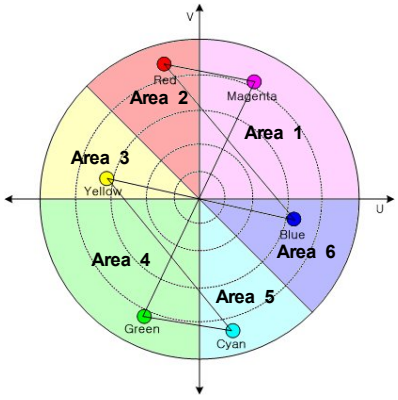
BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x15	[7:3]	CLAMP_REG	· Manual clamp value · Apply clamp with CLAMP_REG value if Auto Clamp is off.	R/W	0x43
	[2]	DAY_IR_P	· Day&Night output pulse phase change · 0 : Normal 1 : Change		
	[1:0]	CLAMP_LEVEL	· Set the weight of clamp value if Auto clamp is on.		
0x16	[7:0]	H_OFFSET	· Modify horizontal timing. (default : 0x00) · range : -128 ~ 127	R/W	0x40
0x17	[7:6]	BPF_SEL	· Band pass filter selection	R/W	0x80
	[5]	SHPD_TYPE	· Set the relation between SHP, SHD pulse and H1 pulse		
	[4:1]	H_SIZE	· Encoder horizontal active size control		
	[0]	HP_DLL_EN	· Pulse delay method selection · 0 : DELAY CELL 1 : ANALOG DLL		
0x18	[7:0]	Y_GAIN	· Second Y gain · Range : x0 ~ x2	R/W	0x4C
0x19	[7]	H_EDGE_OFF	· Remove Edge on right and left side of the screen. · 0 : Edge On 1: Edge Off	R/W	0xB1
	[6:0]	Y_CLIP	· Assign maximal Y value for output		
0x1A	[7]	Fix	· Fix at 1'b0.	R/W	0x00
	[6:5]	DAY_EX	· Select criteria for the control of day & night in the Day&Night function · 0 : Internal (Only AGC) 1 : External CDS input 2 : External CDS input + AGC		
	[4]	Fix	· Fix at 1'b0.		
	[3:0]	MIRROR_POS	· Horizontal position setting at time of mirror screen		
0x1B	[7:0]	Y_GAMMA0	· 1st Y GAMMA value	R/W	0x01
0x1C	[7:0]	Y_GAMMA1	· 2nd Y GAMMA vaue	R/W	0x10
0x1D	[7:0]	Y_GAMMA2	· 3rd Y GAMMA vlue	R/W	0x25
0x1E	[7:0]	Y_GAMMA3	· 4th Y GAMMA vlue	R/W	0x41
0x1F	[7:0]	Y_GAMMA4	· 5th Y GAMMA vlue	R/W	0x68
0x20	[7:0]	Y_GAMMA5	· 6th Y GAMMA vlue	R/W	0x9E
0x21	[7:0]	Y_GAMMA6	· 7th Y GAMMA vlue	R/W	0xE7
0x22	[7:0]	Y_GAMMA7	· 8th Y GAMMA vlue	R/W	0xFF



BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x23	[7:4]	HAP_SLICE1	· Low-frequency bandwidth horizontal aperture slice · Standard of the size of the edge that could become an aperture	R/W	0x45
	[3:0]	HAP_SLICE2	· High-frequency bandwidth horizontal aperture slice		
0x24	[7:4]	VAP_SLICE	· Vertical aperture slice	R/W	0x45
	[3:0]	VAP_GAIN	· Vertical aperture gain · Range : x0 ~ x2		
0x26	[7:5]	PEAK_GAIN	· Peaking filter gain · Range : x0 ~ x4	R/W	0x0A
	[4:0]	HAP_GAIN1	· Low-frequency bandwidth horizontal aperture gain · Range : x0 ~ x4		
0x27	[7:5]	Fix	· Fix at 1'b0.	R/W	0x09
	[4:0]	HAP_GAIN2	· High-frequency bandwidth horizontal aperture gain · Range : x0 ~ x4		
0x28	[7:4]	BF_DLY	· Adjust BURST position	R/W	0x63
	[3:0]	PEAK_SLICE	· Peaking slice.		
0x29	[7:0]	SUE_AGC_LEVEL	· Set AGC level for the start of edge suppress in low illumination · If AGC value is above the value set, edge suppress will be applied.	R/W	0x22
0x2A	[7:4]	SUC_AGC_GAIN	· Set ratio for color suppress in low illumination.	R/W	0x28
	[3:0]	SUE_AGC_GAIN	· Set ratio for edge suppress in low illumination.		
0x2B	[7:0]	SUC_AGC_LEVEL	· Set AGC level for the start of color suppress in low illumination	R/W	0x30
0x2C	[7:4]	SUC_HL_HLEVEL	· Set Y level for the start of highlight color suppress (bright range)	R/W	0x90
	[3:0]	SUC_HL_LLEVEL	· Set Y level for the start of highlight color suppress (dark range)		
0x2D	[7:4]	SUC_HL_GAIN	· Set ratio for highlight color suppress.	R/W	0x31
	[3:0]	SUC_EDGE_GAIN	· Set ratio for the suppression of color component at edge.		
0x2E	[7:0]	C_GAMMA0	· 1st C GAMMA value	R/W	0x01
0x2F	[7:0]	C_GAMMA1	· 2nd C GAMMA value	R/W	0x10
0x30	[7:0]	C_GAMMA2	· 3rd C GAMMA value	R/W	0x25
0x31	[7:0]	C_GAMMA3	· 4th C GAMMA value	R/W	0x41
0x32	[7:0]	C_GAMMA4	· 5th C GAMMA value	R/W	0x68
0x33	[7:0]	C_GAMMA5	· 6th C GAMMA value	R/W	0x9E
0x34	[7:0]	C_GAMMA6	· 7th C GAMMA value	R/W	0xE7
0x35	[7:0]	C_GAMMA7	· 8th C GAMMA value	R/W	0xFF
0x36	[7:0]	GAIN_RS1	· CCR = s2*GAIN_RS2-s1***GAIN_RS1** · Range : x0 ~ x2	R/W	0x80
0x37	[7:0]	GAIN_RS2	· CCR = s2***GAIN_RS2**-s1*GAIN_RS1 · Range : x0 ~ x2	R/W	0x80
0x38	[7:0]	GAIN_BS1	· CCB = s1***GAIN_BS1**-s2*GAIN_BS2 · Range : x0 ~ x2	R/W	0x80
0x39	[7:0]	GAIN_BS2	· CCB = s1*GAIN_BS1-s2***GAIN_BS2** · Range : x0 ~ x2	R/W	0x80

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x3A	[7:0]	CCY_GAIN	· CCY gain · Range : x0 ~ x2	R/W	0x80
0x3B	[7:0]	CCR_GAIN	· CCR gain · Range : x0 ~ x4	R/W	0x80
0x3C	[7:0]	CCB_GAIN	· CCB gain · Range : x0 ~ x4	R/W	0x80
0x3D	[7]	Fix	· Fix at 1'b0.	R/W	0x3F
	[6]	CFIR_SEL	· LPF selection on CHROMA path		
	[5:0]	CLP_RS1	· Clip of GAIN_RS1*s1		
0x3E	[7]	CCRB_ID	· Switch CCR and CCB lines at time of color calculation.	R/W	0xBF
	[6]	S1_ID	· Switch S1 and S2.		
	[5:0]	CLP_RS2	· CLIP of GAIN_RS2*s2		
0x3F	[7:6]	TEST_PATTERN	· Internal test pattern selection · 0 ~ 2 : Internal test Pattern 3 : CCD Input.	R/W	0xFF
	[5:0]	CLP_BS1	· Clip of GAIN_BS1*s1		
0x40	[7:6]	YFIR_SEL	· LPF selection on LUMA path	R/W	0x3F
	[5:0]	CLP_BS2	· Clip of GAIN_BS2*s2		
0x41	[7:0]	CCORR	· R' = CCR***CCORR**+CCY*CCORG+CCB*CCORB · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0xA0
0x42	[7:0]	CCORG	· R' = CCR*CCORR+CCY***CCORG**+CCB*CCORB · Gain range : -x0.5 ~ x0.5 (2's complement)	R/W	0x2E
0x43	[7:0]	CCORB	· R' = CCR*CCORR+CCY*CCORG+CCB***CCORB** · Gain range : -x0.5 ~ x0.5 (2's complement)	R/W	0x4E
0x44	[7:0]	CCOGR	· G' = CCY*CCOGG-(CCR***CCOGR**+CCB*CCOGB) · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x6C
0x45	[7:0]	CCOGG	· G' = CCY***CCOGG**-(CCR*CCOGR+CCB*CCOGB) · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x87
0x46	[7:0]	CCOGB	· G' = CCY*CCOGG-(CCR*CCOGR+CCB***CCOGB**) · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0xAC
0x47	[7:0]	CCOBR	· B' = CCR***CCOBR**+CCY*CCOBG+CCB*CCOBB · Gain range : -x0.5 ~ -x0.5 (2's complement)	R/W	0xC6
0x48	[7:0]	CCOBG	· B' = CCR*CCOBR+CCY***CCOBG**+CCB*CCOBB · Gain range : -x0.5 ~ -x0.5 (2's complement)	R/W	0x52
0x49	[7:0]	CCOBB	· B' = CCR*CCOBR+CCY*CCOBG+CCB***CCOBB** · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0xC4
0x4A	[7:0]	RWB	· RED gain · Gain range : x0(0x00) ~ x4(0xFF)	R/W	0x5A
0x4B	[7:0]	GWB	· GREEN gain · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x4A
0x4C	[7:0]	BWB	· BLUE gain · Gain range : x0(0x00) ~ x4(0xFF)	R/W	0x51
0x4D	[7:0]	RBLK	· RED offset · Gain range : -128 ~ 127 (2's complement)	R/W	0x00

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x4E	[7:0]	GBLK	· GREEN offset · Gain range : -128 ~ 127 (2's complement)	R/W	0x00
0x4F	[7:0]	BBLK	· BLUE offset · Gain range : -128 ~ 127 (2's complement)	R/W	0x00
0x50	[7:0]	CR_GAIN	· CR GAIN · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80
0x51	[7:0]	CB_GAIN	· CB GAIN · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80
0x52	[7:0]	HUE1	· 1st area HUE control · Data range : -45° ~ 45° (2's complement)	R/W	0x00
0x53	[7:0]	HUE2	· 2nd area HUE control · Data range : -45° ~ 45° (2's complement)	R/W	0x00
0x54	[7:0]	HUE3	· 3rd area HUE control · Data range : -45° ~ 45° (2's complement)	R/W	0x00
0x55	[7:0]	HUE4	· 4th area HUE control · Data range : -45° ~ 45° (2's complement)	R/W	0x00
0x56	[7:0]	HUE5	· 5th area HUE control · Data range : -45° ~ 45° (2's complement)	R/W	0x00
0x57	[7:0]	HUE6	· 6th area HUE control · Data range : -45° ~ 45° (2's complement)	R/W	0x00
0x58	[7:0]	UV_GAIN1	· 1st area UV gain · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80
0x59	[7:0]	UV_GAIN2	· 2nd area UV gain · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80
0x5A	[7:0]	UV_GAIN3	· 3rd area UV gain · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80
0x5B	[7:0]	UV_GAIN4	· 4th area UV gain · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80
0x5C	[7:0]	UV_GAIN5	· 5th area UV gain · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80
0x5D	[7:0]	UV_GAIN6	· 6th area UV gain · Gain range : x0(0x00) ~ x2(0xFF)	R/W	0x80



BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x5E	[7]	BLC	· BLC(Back Light Compensation) On/Off · 0 : OFF 1 : ON	R/W	0x95
	[6]	BLC_AREA_VIEW	· BLC AREA VIEW On/Off · 0 : OFF 1 : ON		
	[5:0]	BLC_GAIN	· Adjust ratio of screen brightness in the BLC area		
0x5F	[7:4]	MOTION_AGC	· Apply different motion threshold values for low illumination and general conditions so that motion can be detected. · Set the criteria of low illumination for motion detection.	R/W	0x40
	[3:0]	MOTION_HIGH	· Motion detection is not to be performed when the screen is as bright as it is set in the MOTION_HIGH or brighter		
0x60	[7:0]	AE_LEVEL	· Standard value for Auto Exposure when BLC is OFF	R/W	0x54
0x61	[7:0]	BLC_LEVEL	· Standard value for Auto Exposure when BLC is ON	R/W	0x40
0x62	[7:0]	MOTION_THL	· Low luminous motion threshold value	R/W	0x0F
0x63	[7]	DAY_EXT_IN_P	· Day&Night external input pulse phase change · 0 : Normal 1 : Change	R/W	0x08
	[6:4]	Fix	· Fix at 1'b0.		
	[3]	IRIS_LG_ON	· Select the iris level · 0 : IRIS_LEVEL 1 : IRIS_LEVEL*gain		
	[2]	IRIS_DAC_PORT	· Set DAC sleep mode register assign		
	[1:0]	Fix	· Fix at 1'b0.		
0x64	[7:0]	MAX1_AGC	· MAX AGC1	R/W	0xD0
0x65	[7:0]	MAX2_AGC	· MAX AGC2	R/W	0x00
0x66	[7:4]	ESS_ZONE	· Electronic shutter stable zone	R/W	0x75
	[3:0]	AED_ZONE	· Digital gain stable zone		
0x67	[7:4]	ESS_SDLY	· Delay time from when the AGC is operated until the electronic shutter works	R/W	0x00
	[3:0]	AGC_SDLY	· Delay time from when the electronic shutter is operated until the AGC functions		
0x68	[7:6]	AE_DG_REG[9:8]	· Manual digital gain MSB[9:8]	R/W	0x4F
	[5:4]	AGC_REG[9:8]	· Manual AGC MSB[9:0]		
	[3:0]	AE_SPD	· AE speed control · 0 : slow ~ 7 : fast		
0x69	[7:0]	AE_DG_REG[7:0]	· Manual digital gain LSB[7:0]	R/W	0x00
0x6A	[7:0]	AGC_REG[7:0]	· Manual AGC LSB[7:0]	R/W	0x00

<table>
<tr><th colspan="6">BANK 0</th></tr>
<tr><th>ADDR</th><th>bit</th><th>NAME</th><th>DESCRIPTION</th><th>status</th><th>default</th></tr>
<tr><td rowspan="4">0x6B</td><td>[7:6]</td><td>AE_MODE</td><td>· AE Mode selection
· 0 : Fixed(SSM) 1 : Auto 2 : Manual(256 steps) 3 : Manual</td><td rowspan="4">R/W</td><td rowspan="4">0x42</td></tr>
<tr><td>[5:3]</td><td>SSM</td><td>· Output predefined values of the electronic shutter.
<table>
<tr><th>SSM</th><th>NTSC</th><th>PAL</th></tr>
<tr><td>0</td><td>1/60</td><td>1/50</td></tr>
<tr><td>1</td><td>1/100</td><td>1/120</td></tr>
<tr><td>2</td><td>1/250</td><td>1/250</td></tr>
<tr><td>3</td><td>1/500</td><td>1/500</td></tr>
<tr><td>4</td><td>1/2,000</td><td>1/2,000</td></tr>
<tr><td>5</td><td>1/5,000</td><td>1/5,000</td></tr>
<tr><td>6</td><td>1/10,000</td><td>1/10,000</td></tr>
<tr><td>7</td><td>1/100,000</td><td>1/100,000</td></tr>
</table></td></tr>
<tr><td>[2]</td><td>MOTION_TEST</td><td>· Motion area view On/Off
· 0 : OFF 1 : ON</td></tr>
<tr><td>[1:0]</td><td>IRIS_LENS</td><td>· IRIS output type selection
· 0 : VIDEO 1 : DC else : Manual</td></tr>
<tr><td rowspan="3">0x6C</td><td>[7]</td><td>BTN_REPT_ON</td><td>· Select whether the button remained pressed is recognized as successive entry</td><td rowspan="3">R/W</td><td rowspan="3">0x80</td></tr>
<tr><td>[6:5]</td><td>Fix</td><td>· Fix at 1'b0.</td></tr>
<tr><td>[4:0]</td><td>ME_ESS[12:8]</td><td>· Manual ess value[12:8] (It functions only when the AE_MODE value is 3)</td></tr>
<tr><td>0x6D</td><td>[7:0]</td><td>ME_ESS[7:0]</td><td>· Manual ess value[7:0]</td><td>R/W</td><td>0x15</td></tr>
<tr><td>0x6E</td><td>[7:0]</td><td>R_MAX</td><td>· Set Maximal RED value in color temperature</td><td>R/W</td><td>0x8D</td></tr>
<tr><td>0x6F</td><td>[7:0]</td><td>B_MAX</td><td>· Set Maximal BLUE value in color temperature</td><td>R/W</td><td>0x43</td></tr>
<tr><td>0x70</td><td>[7:0]</td><td>R_MIN</td><td>· Set Minimal RED value in color temperature</td><td>R/W</td><td>0x64</td></tr>
<tr><td>0x71</td><td>[7:0]</td><td>B_MIN</td><td>· Set Minimal BLUE value in color temperature</td><td>R/W</td><td>0xCB</td></tr>
<tr><td>0x72</td><td>[7:0]</td><td>AWB_HIGH</td><td>· Maximal Y value for the operation of AWB</td><td>R/W</td><td>0xF0</td></tr>
<tr><td rowspan="3">0x73</td><td>[7:6]</td><td>AWB_MODE</td><td>· AWB / ATW / DIP mode selection
· 0 : AWB 1 : ATW 2: DIP 3 : MANUAL</td><td rowspan="3">R/W</td><td rowspan="3">0x40</td></tr>
<tr><td>[5:4]</td><td>AWB_DIP</td><td>· Select four color temperature predefined.</td></tr>
<tr><td>[3:0]</td><td>Fix</td><td>· Fix at 1'b0.</td></tr>
<tr><td>0x74</td><td>[7:0]</td><td>AWB_LOW</td><td>· Minimal Y value required for the operation of AWB</td><td>R/W</td><td>0x07</td></tr>
<tr><td rowspan="2">0x75</td><td>[7:4]</td><td>R_CLP</td><td>· CLIP maximal RED value in AWB tracking area.</td><td rowspan="2">R/W</td><td rowspan="2">0xFF</td></tr>
<tr><td>[3:0]</td><td>B_CLP</td><td>· CLIP maximal BLUE value in AWB tracking area.</td></tr>
<tr><td rowspan="2">0x76</td><td>[7:4]</td><td>INTVAL_H</td><td>· Set the size of upper section in the AWB tracking area.</td><td rowspan="2">R/W</td><td rowspan="2">0x44</td></tr>
<tr><td>[3:0]</td><td>INTVAL_L</td><td>· Set the size of lower section in the AWB tracking area.</td></tr>
<tr><td rowspan="2">0x77</td><td>[7:4]</td><td>AWB_SPD</td><td>· AWB tracking speed
· 0x00(slow) ~ 0x0F(fast)</td><td rowspan="2">R/W</td><td rowspan="2">0xF4</td></tr>
<tr><td>[3:0]</td><td>STA_ZONE</td><td>· Set the size of stabilization zone at time of AWB tracking.</td></tr>
<tr><td rowspan="2">0x78</td><td>[7:4]</td><td>STA_IN_LMT</td><td>· If the time in the STA_ZONE is higher than the value set when the AWB Tracking pointer is inside the STA_ZONE, no more AWB Tracking is to done.</td><td rowspan="2">R/W</td><td rowspan="2">0x11</td></tr>
<tr><td>[3:0]</td><td>STA_OUT_LMT</td><td>· Tracking is to done when white continues to exist in the area outside the STA_ZONE for a period longer than what is set.</td></tr>
</table>

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x7A	[7:0]	AWB_R0	· DIP_MODE == 0, AWB RED gain	R/W	0x40
0x7B	[7:0]	AWB_R1	· DIP_MODE == 1, AWB RED gain	R/W	0x04
0x7C	[7:0]	AWB_R2	· DIP_MODE == 2, AWB RED gain	R/W	0x6D
0x7D	[7:0]	AWB_R3	· DIP_MODE == 3, AWB RED gain	R/W	0x42
0x7E	[7:0]	AWB_B0	· DIP_MODE == 0, AWB BLUE gain	R/W	0x40
0x7F	[7:0]	AWB_B1	· DIP_MODE == 1, AWB BLUE gain	R/W	0x00
0x80	[7:0]	AWB_B2	· DIP_MODE == 2, AWB BLUE gain	R/W	0xEE
0x81	[7:0]	AWB_B3	· DIP_MODE == 3, AWB BLUE gain	R/W	0x3C
0x82	[7:0]	AWB_R_OFFSET	· AWB RED offset · Data range : -128 ~ 127 (2's complements)	R/W	0x10
0x83	[7:0]	AWB_B_OFFSET	· AWB BLUE offset · Data range : -128 ~ 127 (2's complements)	R/W	0x08
0x84	[7:0]	DAY_NIGHT_START	· Set the brightness level where the DAY & NIGHT function starts to operate	R/W	0xC3
0x85	[7:0]	DAY_NIGHT_END	· Set the brightness level where the DAY & NIGHT function stops operating	R/W	0x97
0x86	[7:6]	DAY_ON	· Set Day&Night function · 0 : B/W, 1: Color 2 : Auto	R/W	0x41
	[5:0]	DAY_DLY	· Delay time when the Day&Night function starts or stops · 0 sec ~ 15 sec		
0x87	[7:4]	SEL_EXPO_02	· Assign an output pulse to the pin number 22	R/W	0x00
	[3:0]	SEL_EXPO_01	· Assign an output pulse to the pin number 21		
0x88	[7:4]	SEL_EXPO_04	· Assign an output pulse to the pin number 29	R/W	0x00
	[3:0]	SEL_EXPO_03	· Assign an output pulse to the pin number 23		
※ output pulse 0 : none. 1 : day motor 2 : day IR 3 : power pulse 4 : motion detection 5 : IRIS_LENS[0] 6 : eeprom wr 7 : pblk 8 : clpdm 9 : clpob					
0x8A	[7:5]	Fix	· Fix at 1'b0.	R/W	0x00
	[4:0]	SC_OFFSET	· Scaler offset(only 27MHz)		
0x8B	[7:3]	DEF_M_SEL	· Manual defect point selection	R/W	0x00
	[2]	Fix	· Fix at 1'b0.		
	[1]	DAY_EXT_IN_REG	· Day&Night external enable signal		
	[0]	Fix	· Fix at 1'b0.		
0x8C	[7:0]	HXV_OFFSET	· Modify the pulse timing (at 27MHz) · Range : -128 ~ 127	R/W	0x00
0x8D	[7:0]	PRE_Y_GAiN	· First Y gain · Range : x0 ~ x2	R/W	0x80
0x8E	[7:4]	EDGE_S	· Remove noise generated on the left side of video	R/W	0x02
	[3:0]	EDGE_E	· Remove noise generated on the right side of video		

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0x8F	[7]	Fix	· Fix at 1'b0.	R/W	0x58
	[6]	MOTION_EN	· Motion detection On/Off · 0 : Off 1 : On		
	[5]	M_VIEW_ON	· Motion view On/Off (Display the motion area on the screen.) · 0 : Motion view Off 1 : Motion view On		
	[4]	DAY_BURST_ON	· BURST signal On/Off(Day&Night)		
	[3:0]	Fix	· Fix at 1'b0.		
0xA0	[7:6]	POWER_FRE	· Adjust the frequency of the power pulse.	R/W	0x50
	[5]	IRIS_P	· IRIS output phase change · 0 : Normal. 1 : Change.		
	[4:0]	HVAP_GAIN	· Sharpness gain		
0xA1	[7:4]	MOTION_TH_AREA	· Generate motion detection pulse when the number of areas where motions occur (out of 64 areas) is greater than what is set at MOTION_TH_AREA.	R/W	0x00
	[3:0]	SEL_IRIS_LENS	· Select the input pin for the IRIS_LENS signal		
0xA3	[7]	MIRROR	· MIRROR On/Off	R/W	0x00
	[6]	M_CURSOR_ON	· Set the cursor On/Off indicating one of the 64 areas at time of setting the MOTION AREA		
	[5:0]	M_CURSOR	· Set the cursor location indicating one of the 64 areas at time of setting the MOTION AREA		
0xA4	[7:0]	AWB_M_R	· AWB manual adjust RED gain	R/W	0x40
0xA5	[7:0]	AWB_M_B	· AWB manual adjust BLUE gain	R/W	0x40
0xA6	[7:0]	IRIS_LEVEL	· IRIS output level	R/W	0x40
0xA7	[7:0]	IRIS_GAIN	· IRIS output gain	R/W	0x80
0xA8	[7:4]	BTN_DLY	· Button input delay	R/W	0x05
	[3:0]	Fix	· Fix at 1'b0.		
0xA9	[7:0]	Y_OFFSET	· Adjust the Y offset · Range : -128 ~ +127(2's complement)	R/W	0x00
0xAA	[7:6]	U_BURST[9:8]	· U_BURST[9:8] value.	R/W	0xCE
	[5:0]	SYNC_REG	· Adjust the SYNC level of the video signal		
0xAB	[7:6]	V_BURST[9:8]	· V_BURST[9:8] value.	R/W	0x15
	[5:0]	BLACK_REG	· Adjust the BLACK level of the video signal		
0xAC	[7:0]	U_BURST[7:0]	· Set the U_BURST value.	R/W	0x9F
0xAD	[7:0]	V_BURST[7:0]	· Set the V_BURST value.	R/W	0x00
0xAE	[7:6]	IRIS_DC	· IRIS output selection · 0 : VIDEO 1 : DC else : MANUAL	R/W	0x09
	[5:1]	IRIS_BLC_OFFSET	· Set the offset value at time of MANUAL IRIS output		
	[0]	DAC_P	· DAC clock phase change · 0 : Normal 1: Change		
0xAF	[7:4]	DAC1_OUT	· DAC 1 output selection	R/W	0x00
	[3:0]	DAC2_OUT	· DAC 2 output selection		
※ DAC output mode 0 : CVBS 1 : LUMA 2 : CHROMA 3 : IRIS 4 : IRIS volume 5 : HIGH 6 : LOW					

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0xB0	[7:0]	MOTION_TH	· High luminous motion threshold value	R/W	0x22
0xB1	[7:4]	MOTION_THF	· Generate motion detection pulse when consecutive motions are detected as much as set at MOTION_THF or above.	R/W	0x08
	[3]	SLPF_SEL	· Encoder sync low pass filter On/Off · 0 : Off 1 : On		
	[2:0]	AE_OUT_LMT	· Start to operate AE after a certain time set at AE_OUT_LMT has passed once the brightness of input screen changes		
0xB2	[7:0]	MOTION_AREA[63:56]	· Set the MOTION area	R/W	0xFF
0xB3	[7:0]	MOTION_AREA[55:48]		R/W	0xFF
0xB4	[7:0]	MOTION_AREA[47:40]		R/W	0xFF
0xB5	[7:0]	MOTION_AREA[39:32]		R/W	0xFF
0xB6	[7:0]	MOTION_AREA[31:24]		R/W	0xFF
0xB7	[7:0]	MOTION_AREA[23:16]		R/W	0xFF
0xB8	[7:0]	MOTION_AREA[15:8]		R/W	0xFF
0xB9	[7:0]	MOTION_AREA[7:0]		R/W	0xFF
0xBA	[7:0]	BLC_AREA[63:56]	· Set the BLC area	R/W	0xFF
0xBB	[7:0]	BLC_AREA[55:48]		R/W	0xFF
0xBC	[7:0]	BLC_AREA[47:40]		R/W	0xFF
0xBD	[7:0]	BLC_AREA[39:32]		R/W	0xFF
0xBE	[7:0]	BLC_AREA[31:24]		R/W	0xFF
0xBF	[7:0]	BLC_AREA[23:16]		R/W	0xFF
0xC0	[7:0]	BLC_AREA[15:8]		R/W	0xFF
0xC1	[7:0]	BLC_AREA[7:0]		R/W	0xFF

AREA[0]	AREA[1]	AREA[2]	AREA[3]	AREA[4]	AREA[5]	AREA[6]	AREA[7]
AREA[8]	AREA[9]	AREA[10]	AREA[11]	AREA[12]	AREA[13]	AREA[14]	AREA[15]
AREA[16]	AREA[17]	AREA[18]	AREA[19]	AREA[20]	AREA[21]	AREA[22]	AREA[23]
AREA[24]	AREA[25]	AREA[26]	AREA[27]	AREA[28]	AREA[29]	AREA[30]	AREA[31]
AREA[32]	AREA[33]	AREA[34]	AREA[35]	AREA[36]	AREA[37]	AREA[38]	AREA[39]
AREA[40]	AREA[41]	AREA[42]	AREA[43]	AREA[44]	AREA[45]	AREA[46]	AREA[47]
AREA[48]	AREA[49]	AREA[50]	AREA[51]	AREA[52]	AREA[53]	AREA[54]	AREA[55]
AREA[56]	AREA[57]	AREA[58]	AREA[59]	AREA[60]	AREA[61]	AREA[62]	AREA[63]

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0xC2	[7:4]	SEL_DAY_EXT	· Select the input pin for the Day&Night external signal	R/W	0x00
	[3:0]	SEL_MIRROR	· Select the input pin for the MIRROR control signal		
0xC3	[7:4]	SEL_BLC	· Select the input pin for the BLC control signal	R/W	0x00
	[3:0]	SEL_AGC	· Select the input pin for the AGC control signal		
0xC4	[7:4]	SEL_AE1	· Select the input pin for the AE_MODE[1] signal	R/W	0x00
	[3:0]	SEL_AE0	· Select the input pin for the AE_MODE[0] signal		
0xC5	[7:4]	SEL_SSM1	· Select the input pin for the SSM[1] signal	R/W	0x00
	[3:0]	SEL_SSM0	· Select the input pin for the SSM[0] signal		
0xC6	[7:4]	Fix	· Fix at 1'b0.	R/W	0x00
	[3:0]	SEL_SSM2	· Select the input pin for the SSM[2] signal		
※ selection input pin 0x0 : none 0x1 : #34 0x2 : #35 0x3 : #36 0x4 :not use 0x5 :not use 0x6 :not use 0x7 :not use 0x8 :not use 0x9 : #21 0xA : #22 0xB : #23 0xC : #29					
0xC7	[7:4]	IRIS_GMAX	· Set the maximal value of IRIS_GAIN	R/W	0x00
	[3:0]	IRIS_GMIN	· Set the minimal value of IRIS_GAIN		
0xC8	[7:0]	IR_GAIN[7:0]	· Set the INFRARED gain value	R/W	0x00
0xDC	[7]	MAX_AGC_SEL	· MAX_AGC selection · 0 : MAX1_AGC 1 : MAX2_AGC	R/W	0x00
	[6:0]	Fix	· Fix at 1'b0.		
0xDD	[7]	DAY_MOTOR_P	· Day&Night motor control pulse phase change · 0 : Normal 1: Change	R/W	0x80
	[6:5]	DAY_PULSE_SEL	· Day&Night output pulse type selection · Adjust the brightness of IR · 0 : Maximum ~ 3 : Minimum		
	[4:0]	Fix	· Fix at 1'b0.		
0xDF	[7]	Fix	· Fix at 1'b0.	R/W	0x00
	[6:5]	BLK_TH	· Black level horizontal aperture threshold		
	[4:0]	Fix	· Fix at 1'b0.		
0xE0	[7]	NEGATIVE_IMG	· Negative image On/Off · 0 : Off 1 : On	R/W	0x00
	[6:5]	BLK_GAIN	· Black level horizontal aperture gain		
	[4:0]	Fix	· Fix at 1'b0.		
0xE1	[7]	HPF_SEL	· High frequence horizontal aperture filter selection	R/W	0xE0
	[6:5]	HAP_CLIP1	· Low frequence horizontal aperture clip		
	[4:0]	Fix	· Fix at 1'b0.		
0xE2	[7]	Fix	· Fix at 1'b0.	R/W	0x60
	[6:5]	VAP_CLIP	· Vertical aperture clip		
	[4:0]	Fix	· Fix at 1'b0.		
0xE3	[7]	AWB_AE_DETECT	· Set the point of starting AWB · 0 : Start AWB irrespective of AE 1 : Start AWB once AE gets stabilized	R/W	0x80
	[6:5]	AWB_METHOD1	· AWB method1 selection		
	[4:0]	Fix	· Fix at 1'b0.		

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0xE4	[7]	AWB_TR_CLIP	· Clip more than what is set as R_MAX/R_MIN, B_MAX/B_MIN in the AWB tracking area. · 0 : Clip Off 1 : Clip On	R/W	0xE0
	[6:5]	AWB_METHOD2	· AWB method2 selection		
	[4:0]	Fix	· Fix at 1'b0.		
0xE5	[7]	AWB_METHOD3	· AWB method3 selection	R/W	0x4C
	[6:5]	AE_GMAX	· AE digital gain maximum value selection		
	[4:0]	POS_CID	· OSD menu [CAMERA ID] item position(*OSD MENU)		
0xE6	[7:6]	Fix	· Fix at 1'b0.	R/W	0x20
	[5]	HAP_SUP_SEL	· Horizontal edge suppress mode selection		
	[4:0]	Fix	· Fix at 1'b0.		
0xE8	[7]	AFE_DAC2_ON	· AFE DAC2 output On/Off	R/W	0x00
	[6:0]	Fix	· Fix at 1'b0.		
0xEA	[7]	Fix	· Fix at 1'b0.	R/W	0x00
	[6:5]	Y_CLIP_TH	· Standards for processing when the output Y value is bigger than Y_CLIP. · 0 : clip 1: 1/8 2: 1/4 3 : 1/2		
	[4:0]	Fix	· Fix at 1'b0.		
0xEB	[7:6]	MOTION_DELAY	· Set the time for alarm signal of motion detection	R/W	0x80
	[5:0]	Fix	· Fix at 1'b0.		
0xEC	[7:4]	CLPOB_SIZE	· Set CLPOB pulse width	R/W	0x88
	[3:0]	CLPOB_POS	· Set CLPOB position		
0xF0	[7]	AFE_DAC1_ON	· AFE DAC1 output On/Off · 0 : OFF 1 : ON	R/W	0x05
	[6]	IRIS_AFE_DC	· Set the AFE DAC1 output value · 0: Internal register (IRIS_GAIN) 1 : Iris out		
	[5]	INIT_SCR	· Display initial screen (blue screen). 0 : Initial screen display Off 1: Initial screen display On		
	[4]	ADC_SET	· Set the Internal register of AFE. · The register saved at AFE_00 ~ AFE_03 is registered as the internal register of AFE when 0 is changed into 1.		
	[3:0]	SLAVE_ADDR	· Set I2C communication slave address		
0xF1	[7:0]	bank_reg	· Set internal register bank	R/W	0x00
0xF8	[7:3]	test1	· Test register	R/W	0x18
	[2]	DAC1_SL	· DAC1 sleep mode On/Off · 0 : Normal operation 1: Power down mode		
	[1]	DAC2_SL	· DAC2 sleep mode On/Off · 0 : Normal operation 1: Power down mode		
	[0]	Fix	· Fix at 1'b0.		

BANK 0					
ADDR	bit	NAME	DESCRIPTION	status	default
0xF9	[7:6]	SD_H1	· Driving option selection · 0 : 12mA 1 : 14mA 2 : 16mA 3 : 18mA	R/W	0x00
	[5]	SL_H1	· Slew rate selection · 0 : Fast 1 : Slow		
	[4:3]	SD_H2	· Driving option selection · 0 : 12mA 1 : 14mA 2 : 16mA 3 : 18mA		
	[2]	Fix	· Fix at 1'b0.		
	[1]	SL_H2	· Slew rate selection · 0 : Fast 1 : Slow		
	[0]	Fix	· Fix at 1'b0.		
0xFA	[7:6]	SD_RG	· Driving option selection · 0 : 12mA 1 : 14mA 2 : 16mA 3 : 18mA	R/W	0x00
	[5]	SL_RG	· Slew rate selection · 0 : Fast 1 : Slow		
	[4:0]	HAP_SUPPRESS	· Horizontal edge suppress		

BANK 1					
ADDR	bit	NAME	DESCRIPTION	status	default
0x02	[7:0]	COMPEN_START	· Starting point to correct a defect. · The higher the value, correction starts when the screen gets dark.	R/W	0x0A
0x04	[7:3]	Fix	· Fix at 1'b0.	R/W	0x00
	[2]	DEFECT_MANUAL	· Manually search for defect.		
	[1:0]	Fix	· Fix at 1'b0.		
0x08	[7:6]	DEF_V_00[9:8]	· 1st Vertical defect position	R/W	0x00
	[5:4}	DEF_V_01[9:8]	· 2nd Vertical defect position		
	[3:2]	DEF_V_02[9:8]	· 3rd Vertical defect position		
	[1:0]	DEF_V_03[9:8]	· 4th Vertical Defect Position		
0x09	[7:0]	DEF_H_00[7:0]	· 1st Horizontal defect position	R/W	0x00
0x0A	[7:0]	DEF_V_00[7:0]	· 1st Vertical defect position	R/W	0x00
0x0B	[7:6]	DEF_H_00[9:8]	· 1st Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_00[5:0]	· 1st Defect value		
0x0C	[7:0]	DEF_H_01[7:0]	· 2nd Horizontal defect position	R/W	0x00
0x0D	[7:0]	DEF_V_01[7:0]	· 2nd Vertical defect position	R/W	0x00
0x0E	[7:6]	DEF_H_01[9:8]	· 2nd Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_01[5:0]	· 2nd Defect value		
0x0F	[7:0]	DEF_H_02[7:0]	· 3rd Horizontal defect position	R/W	0x00
0x10	[7:0]	DEF_H_02[7:0]	· 3rd Vertical defect position	R/W	0x00
0x11	[7:6]	DEF_H_02[9:8]	· 3rd Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_02[5:0]	· 3rd Defect value		
0x12	[7:0]	DEF_H_03[7:0]	· 4th Horizontal defect position	R/W	0x00
0x13	[7:0]	DEF_V_03[7:0]	· 4th Vertical defect position	R/W	0x00
0x14	[7:6]	DEF_H_03[9:8]	· 4th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_03[5:0]	· 4th Defect value		
0x15	[7:6]	DEF_V_04[9:8]	· 5th Vertical defect position	R/W	0x00
	[5:4]	DEF_V_05[9:8]	· 6th Vertical defect position		
	[3:2]	DEF_V_06[9:8]	· 7th Vertical defect position		
	[1:0]	DEF_V_07[9:8]	· 8th Vertical defect position		
0x16	[7:0]	DEF_H_04[7:0]	· 5th Horizontal defect position	R/W	0x00
0x17	[7:0]	DEF_V_04[7:0]	· 5th Vertical defect position	R/W	0x00
0x18	[7:6]	DEF_H_04[9:8]	· 5th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_04[5:0]	· 5th Defect value		
0x19	[7:0]	DEF_H_05[7:0]	· 6th Horizontal defect position	R/W	0x00
0x1A	[7:0]	DEF_V_05[7:0]	· 6th Vertical defect position	R/W	0x00
0x1B	[7:6]	DEF_H_05[9:8]	· 6th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_05[5:0]	· 6th Defect value		
0x1C	[7:0]	DEF_H_06[7:0]	· 7th Horizontal defect position	R/W	0x00
0x1D	[7:0]	DEF_H_06[7:0]	· 7th Vertical defect position	R/W	0x00
0x1E	[7:6]	DEF_H_06[9:8]	· 7th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_06[5:0]	· 7th Defect value		

BANK 1					
ADDR	bit	NAME	DESCRIPTION	status	default
0x1F	[7:0]	DEF_H_07[7:0]	· 8th Horizontal defect position	R/W	0x00
0x20	[7:0]	DEF_V_07[7:0]	· 8th Vertical defect position	R/W	0x00
0x21	[7:6]	DEF_H_07[9:8]	· 8th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_07[5:0]	· 8th Defect value		
0x22	[7:6]	DEF_V_08[9:8]	· 9th Vertical defect position	R/W	0x00
	[5:4}	DEF_V_09[9:8]	· 10th Vertical defect position		
	[3:2]	DEF_V_10[9:8]	· 11th Vertical defect position		
	[1:0]	DEF_V_11[9:8]	· 12th Vertical defect position		
0x23	[7:0]	DEF_H_08[7:0]	· 9th Horizontal defect position	R/W	0x00
0x24	[7:0]	DEF_V_08[7:0]	· 9th Vertical defect position	R/W	0x00
0x25	[7:6]	DEF_H_08[9:8]	· 9th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_08[5:0]	· 9th Defect value		
0x26	[7:0]	DEF_H_09[7:0]	· 10th Horizontal defect position	R/W	0x00
0x27	[7:0]	DEF_V_09[7:0]	· 10th Vertical defect position	R/W	0x00
0x28	[7:6]	DEF_H_09[9:8]	· 10th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_09[5:0]	· 10th Defect value		
0x29	[7:0]	DEF_H_10[7:0]	· 11th Horizontal defect position	R/W	0x00
0x2A	[7:0]	DEF_H_10[7:0]	· 11th Vertical defect position	R/W	0x00
0x2B	[7:6]	DEF_H_10[9:8]	· 11th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_10[5:0]	· 11th Defect value		
0x2C	[7:0]	DEF_H_11[7:0]	· 12th Horizontal defect position	R/W	0x00
0x2D	[7:0]	DEF_V_11[7:0]	· 12th Vertical defect position	R/W	0x00
0x2E	[7:6]	DEF_H_11[9:8]	· 12th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_11[5:0]	· 12th Defect value		
0x2F	[7:6]	DEF_V_12[9:8]	· 13th Vertical defect position	R/W	0x00
	[5:4}	DEF_V_13[9:8]	· 14th Vertical defect position		
	[3:2]	DEF_V_14[9:8]	· 15th Vertical defect position		
	[1:0]	DEF_V_15[9:8]	· 16th Vertical defect position		
0x30	[7:0]	DEF_H_12[7:0]	· 13th Horizontal defect position	R/W	0x00
0x31	[7:0]	DEF_V_12[7:0]	· 13th Vertical defect position	R/W	0x00
0x32	[7:6]	DEF_H_12[9:8]	· 13th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_12[5:0]	· 13th Defect value		
0x33	[7:0]	DEF_H_13[7:0]	· 14th Horizontal defect position	R/W	0x00
0x34	[7:0]	DEF_V_13[7:0]	· 14th Vertical defect position	R/W	0x00
0x35	[7:6]	DEF_H_13[9:8]	· 14th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_13[5:0]	· 14th Defect value		
0x36	[7:0]	DEF_H_14[7:0]	· 15th Horizontal defect position	R/W	0x00
0x37	[7:0]	DEF_H_14[7:0]	· 15th Vertical defect position	R/W	0x00
0x38	[7:6]	DEF_H_14[9:8]	· 15th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_14[5:0]	· 15th Defect value		

BANK 1					
ADDR	bit	NAME	DESCRIPTION	status	default
0x39	[7:0]	DEF_H_15[7:0]	· 16th Horizontal defect position	R/W	0x00
0x3A	[7:0]	DEF_V_15[7:0]	· 16th Vertical defect position	R/W	0x00
0x3B	[7:6]	DEF_H_15[9:8]	· 16th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_15[5:0]	· 16th Defect value		
0x3C	[7:6]	DEF_V_16[9:8]	· 17th Vertical defect position	R/W	0x00
	[5:4}	DEF_V_17[9:8]	· 18th Vertical defect position		
	[3:2]	DEF_V_18[9:8]	· 19th Vertical defect position		
	[1:0]	DEF_V_19[9:8]	· 20th Vertical defect position		
0x3D	[7:0]	DEF_H_16[7:0]	· 17th Horizontal defect position	R/W	0x00
0x3E	[7:0]	DEF_V_16[7:0]	· 17th Vertical defect position	R/W	0x00
0x3F	[7:6]	DEF_H_16[9:8]	· 17th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_16[5:0]	· 17th Defect value		
0x40	[7:0]	DEF_H_17[7:0]	· 18th Horizontal defect position	R/W	0x00
0x41	[7:0]	DEF_V_17[7:0]	· 18th Vertical defect position	R/W	0x00
0x42	[7:6]	DEF_H_17[9:8]	· 18th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_17[5:0]	· 18th Defect value		
0x43	[7:0]	DEF_H_18[7:0]	· 19th Horizontal defect position	R/W	0x00
0x44	[7:0]	DEF_H_18[7:0]	· 19th Vertical defect position	R/W	0x00
0x45	[7:6]	DEF_H_18[9:8]	· 19th Horizontal defect position	R/W	0x00
	[7:0]	DEF_D_18[5:0]	· 19th Defect value		
0x46	[7:0]	DEF_H_19[7:0]	· 20th Horizontal defect position	R/W	0x00
0x47	[7:0]	DEF_V_19[7:0]	· 20th Vertical defect position	R/W	0x00
0x48	[7:6]	DEF_H_19[9:8]	· 20th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_19[5:0]	· 20th Defect value		
0x49	[7:6]	DEF_V_20[9:8]	· 21th Vertical defect position	R/W	0x00
	[5:4}	DEF_V_21[9:8]	· 22th Vertical defect position		
	[3:2]	DEF_V_22[9:8]	· 23th Vertical defect position		
	[1:0]	DEF_V_23[9:8]	· 24th Vertical defect position		
0x4A	[7:0]	DEF_H_20[7:0]	· 21th Horizontal defect position	R/W	0x00
0x4B	[7:0]	DEF_V_20[7:0]	· 21th Vertical defect position	R/W	0x00
0x4C	[7:6]	DEF_H_20[9:8]	· 21th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_20[5:0]	· 21th Defect value		
0x4D	[7:0]	DEF_H_21[7:0]	· 22th Horizontal defect position	R/W	0x00
0x4E	[7:0]	DEF_V_21[7:0]	· 22th Vertical defect position	R/W	0x00
0x4F	[7:6]	DEF_H_21[9:8]	· 22th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_21[5:0]	· 22th Defect value		
0x50	[7:0]	DEF_H_22[7:0]	· 23th Horizontal defect position	R/W	0x00
0x51	[7:0]	DEF_H_22[7:0]	· 23th Vertical defect position	R/W	0x00
0x52	[7:6]	DEF_H_22[9:8]	· 23th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_22[5:0]	· 23th Defect value		

BANK 1					
ADDR	bit	NAME	DESCRIPTION	status	default
0x53	[7:0]	DEF_H_23[7:0]	· 24th Horizontal defect position	R/W	0x00
0x54	[7:0]	DEF_V_23[7:0]	· 24th Vertical defect position	R/W	0x00
0x55	[7:6]	DEF_H_23[9:8]	· 24th Horizontal defect position	R/W	0x00
	[7:0]	DEF_D_23[5:0]	· 24th Defect value		
0x56	[7:6]	DEF_V_24[9:8]	· 25th Vertical defect position	R/W	0x00
	[5:4]	DEF_V_25[9:8]	· 26th Vertical defect position		
	[3:2]	DEF_V_26[9:8]	· 27th Vertical defect position		
	[1:0]	DEF_V_27[9:8]	· 28th Vertical defect position		
0x57	[7:0]	DEF_H_24[7:0]	· 25th Horizontal defect position	R/W	0x00
0x58	[7:0]	DEF_V_24[7:0]	· 25th Vertical defect position	R/W	0x00
0x59	[7:6]	DEF_H_24[9:8]	· 25th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_24[5:0]	· 25th Defect value		
0x5A	[7:0]	DEF_H_25[7:0]	· 26th Horizontal defect position	R/W	0x00
0x5B	[7:0]	DEF_V_25[7:0]	· 26th Vertical defect position	R/W	0x00
0x5C	[7:6]	DEF_H_25[9:8]	· 26th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_25[5:0]	· 26th Defect value		
0x5D	[7:0]	DEF_H_26[7:0]	· 27th Horizontal defect position	R/W	0x00
0x5E	[7:0]	DEF_H_26[7:0]	· 27th Vertical defect position	R/W	0x00
0x5F	[7:6]	DEF_H_26[9:8]	· 27th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_26[5:0]	· 27th Defect value		
0x60	[7:0]	DEF_H_27[7:0]	· 28th Horizontal defect position	R/W	0x00
0x61	[7:0]	DEF_V_27[7:0]	· 28th Vertical defect position	R/W	0x00
0x62	[7:6]	DEF_H_27[9:8]	· 28th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_27[5:0]	· 28th Defect value		
0x63	[7:6]	DEF_V_28[9:8]	· 29th Vertical defect position	R/W	0x00
	[5:4}	DEF_V_29[9:8]	· 30th Vertical defect position		
	[3:2]	DEF_V_30[9:8]	· 31th Vertical defect position		
	[1:0]	DEF_V_31[9:8]	· 32th Vertical defect position		
0x64	[7:0]	DEF_H_28[7:0]	· 29th Horizontal defect position	R/W	0x00
0x65	[7:0]	DEF_V_28[7:0]	· 29th Vertical defect position	R/W	0x00
0x66	[7:6]	DEF_H_28[9:8]	· 29th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_28[5:0]	· 29th Defect value		
0x67	[7:0]	DEF_H_29[7:0]	· 30th Horizontal defect position	R/W	0x00
0x68	[7:0]	DEF_V_29[7:0]	· 30th Vertical defect position	R/W	0x00
0x69	[7:6]	DEF_H_29[9:8]	· 30th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_29[5:0]	· 30th Defect value		
0x6A	[7:0]	DEF_H_30[7:0]	· 31th Horizontal defect position	R/W	0x00
0x6B	[7:0]	DEF_H_30[7:0]	· 31th Vertical defect position	R/W	0x00
0x6C	[7:6]	DEF_H_30[9:8]	· 31th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_30[5:0]	· 31th Defect value		

BANK 1					
ADDR	bit	NAME	DESCRIPTION	status	default
0x6D	[7:0]	DEF_H_31[7:0]	· 32th Horizontal defect position	R/W	0x00
0x6E	[7:0]	DEF_V_31[7:0]	· 32th Vertical defect position	R/W	0x00
0x6F	[7:6]	DEF_H_31[9:8]	· 32th Horizontal defect position	R/W	0x00
	[5:0]	DEF_D_31[5:0]	· 32th Defect value		
0x70	[7]	AED_SPD	· AE digital gain speed selection · 0 : Normal 1 : Fast	R/W	0x35
	[6:4]	V_OFFSET	· Encoder vertical direction offset		
	[3:0]	OSD_ROMRAM_POS	· Set delay for timing on font display		
0x71	[7:4]	SEL_IRISL	· Select the input pin for the IRIS control left button signal	R/W	0x00
	[3:0]	SEL_IRISR	· Select the input pin for the IRIS control right button signal		
0x72	[7:4]	Fix	· Fix at 1'b0.	R/W	0x00
	[3:0]	SEL_MOTION	· Select the input pin for the MOTION enable signal		

BANK 0x81					
ADDR	bit	NAME	DESCRIPTION	status	default
0x81	[5:0]	ACC_BLC_MSB	· Accumulated value at the BLC area	R	-
0x82	[7:0]	ACC_BLC_LSB		R	-
0x83	[5:0]	ACC_NBLC_LSB	· Accumulated value outside the Non-BLC area	R	-
0x84	[7:0]	ACC_NBLC_LSB		R	-
0x85	[4:0]	AE_ES_MSB	· Electronic shutter value	R	-
0x86	[7:0]	AE_ES_LSB		R	-
0x87	[7:0]	AGC	· AGC value	R	-
0x88	[7:0]	AE_DIGT_GAIN	· AE digital gain value	R	-
0x89	[7:0]	AE_ACC	· Average brightness of the input video	R	-
0x8A	[7:0]	AWB_R	· AWB R value	R	-
0x8B	[7:0]	AWB_B	· AWB B value	R	-
0x8C	[7:0]	AWB_TARGET_R	· Target R for AWB	R	-
0x8D	[7:0]	AWB_TARGET_B	· Target B for AWB	R	-

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power supply voltage	-0.5	6	V
Voltage on any 3.3V input pin	3.0	3.6	V
Voltage on any 5V input pin	4.5	5.5	V
Storage temperature	-40	125	℃

3.2. Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Digital power supply voltage	VDD3	3.0	3.3	3.6	V
3.3V Analog power supply voltage	AVDD3	3.0	3.3	3.6	V
5.0V Digital power supply voltage	VDD5	4.5	5.0	5.5	V
Commercial temperature range	T_A	0	-	70	℃
Industrial temperature range	T_A	-40	-	85	℃

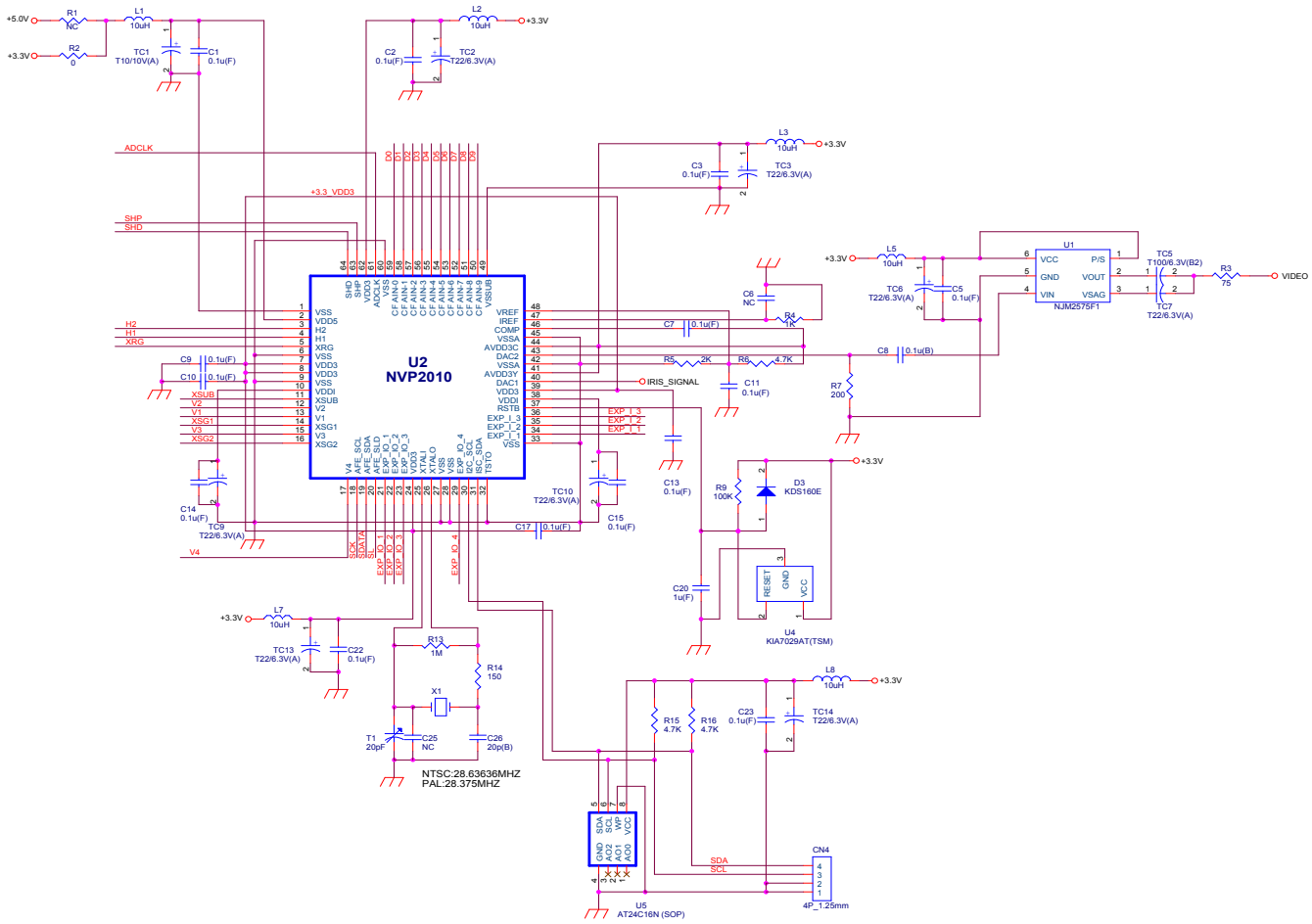
3.3. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Pins *Note1					
Input low voltage	V_{IL3}	V_{SS}-0.3	-	$0.3V_{DD3}$	V
Input high voltage	V_{IH3}	$0.7V_{DD3}$	-	V_{DD3}+0.3	V
Input low current (V_{IN3} = V_{SS})	I_{IL3}	-	-	-10	uA
Input high current (V_{IN3} = V_{DD3})	I_{IH3}	-	-	10	uA
Input capacitance (f = 1Mhz, V_{IN3}= 2.4V)	C_{IN}	-	-	10	pF
Output low voltage (I_{OH3} = 3.2mA)	V_{OL3}	-	-	0.4	V
Output high voltage (I_{OH3} = -400uA)	V_{OH3}	2.4	-	V_{DD3}	V
Output capacitance	C_{OUT}	-	-	10	pF
5.0V Pins *Note2					
Input low voltage	V_{IL5}	V_{SS}-0.5	-	0.8	V
Input high voltage	V_{IH5}	2.0	-	V_{DD5}+0.5	V
Input low current (V_{IN5} = V_{SS})	I_{IL5}	-	-	-10	uA
Input high current (V_{IN5} = V_{DD5})	I_{IH5}	-	-	10	uA
Input capacitance (f = 1Mhz, V_{IN5} = 2.4V)	C_{IN}	-	-	10	pF
Output low voltage (I_{OH5} = 3.2mA)	V_{OL5}	-	-	0.4	V
Output high voltage (I_{OH5} = -400uA)	V_{OH5}	2.4	-	V_{DD5}	V
Output capacitance	C_{OUT}	-	-	10	pF

*Note2 : 3.3V data pins
expect 5V data pins
*Note3 : 5V data pins
XRG, H1, H2 pins(#5, #4, #3)

4. System Application

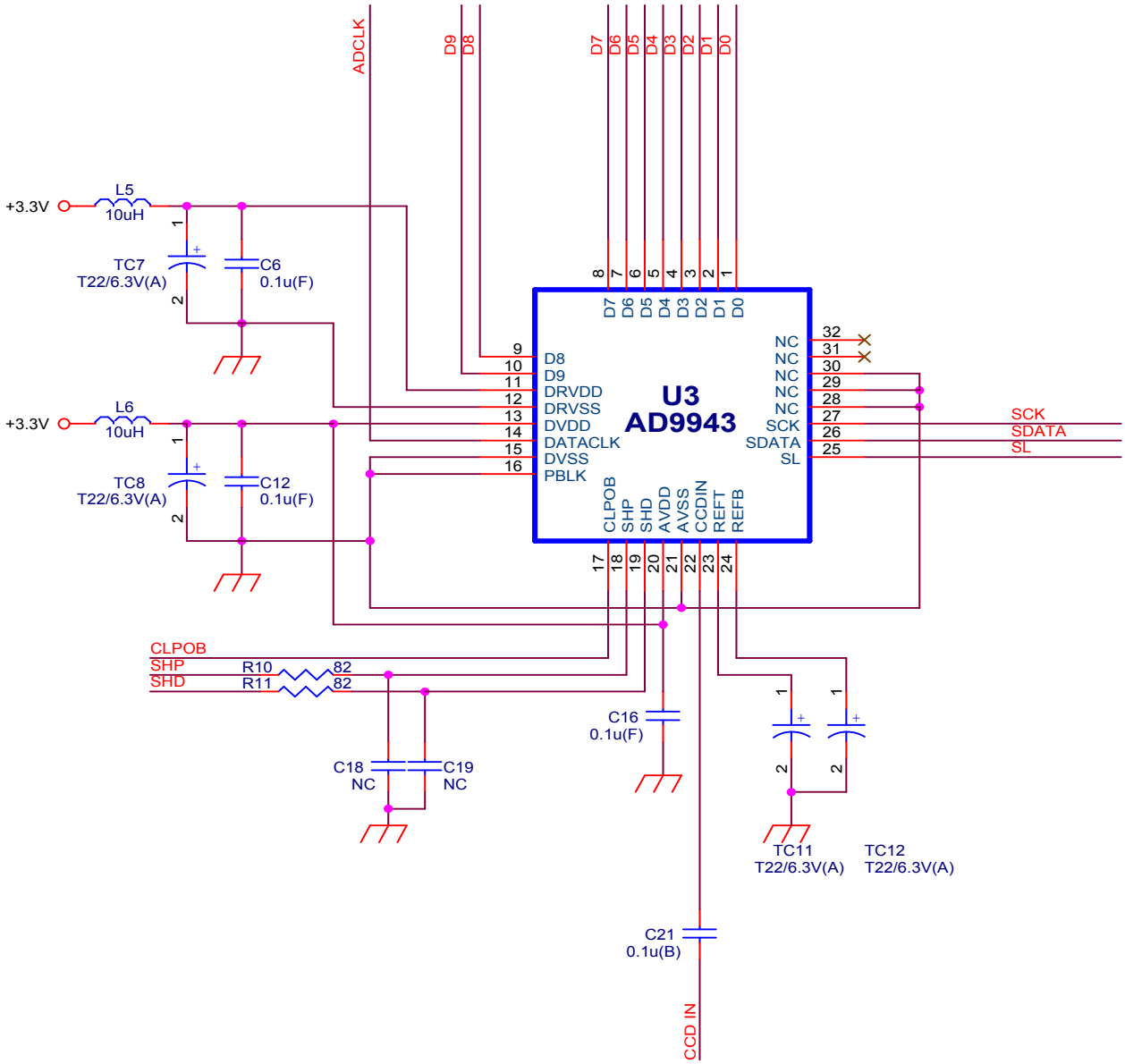
4.1.1 Circuit Guide (NVP2010)



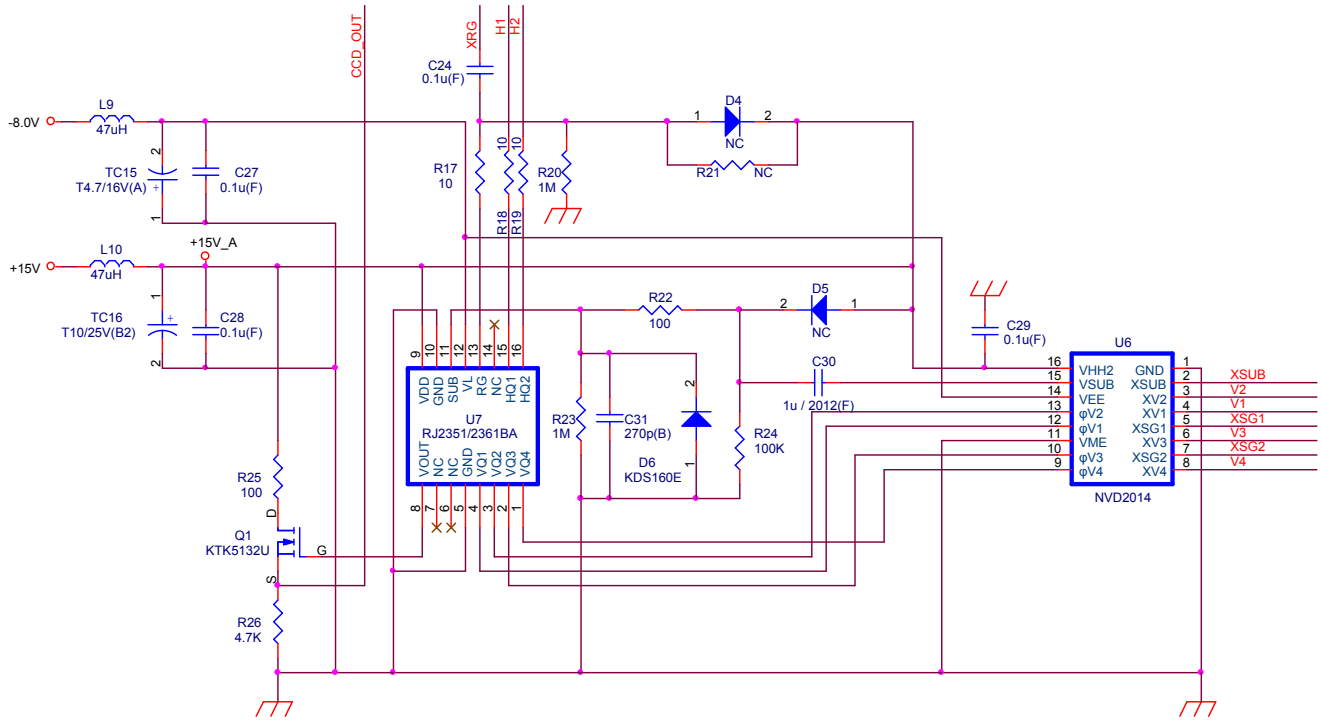
■ Circuit Guide

Ref. Desg.	Value	Maker	Stanrd	Type (Size)
L1~L8	10uH	TDK	NLFV25T-100K-PF	2520
			NLCV32T-100K-PF	3225
TC1~8	22/6.3V	Partsnic	TLMOJ226ASSR	3216
		SAMSUNG	TCSCSOJ226MA	3216
C1~C23	0.1uF	SAMSUNG	CL10F104ZB8	1608
R1~R23	10K ~	SAMSUNG	RC1608J103CS	1608

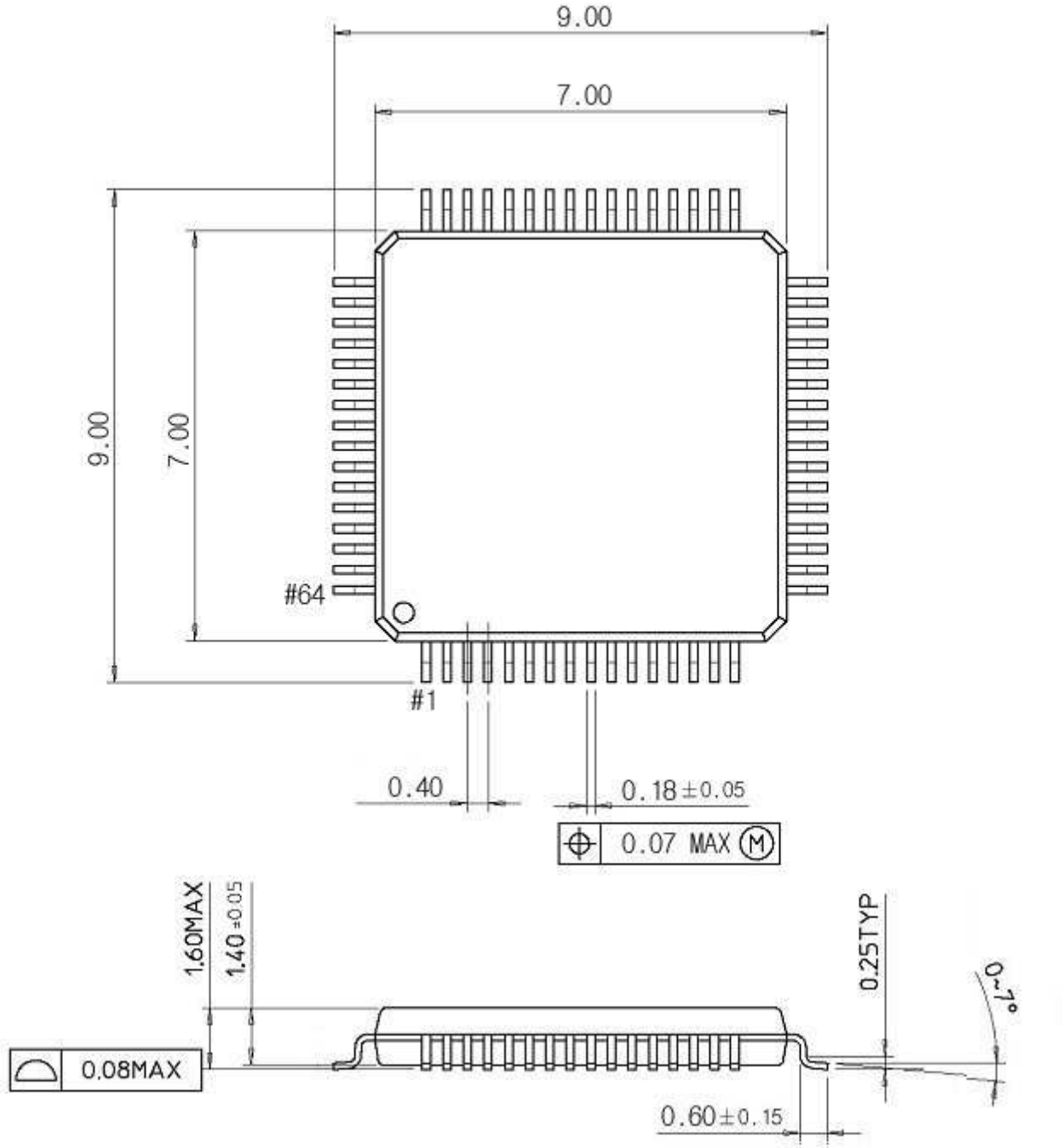
4.1.2 Circuit Guide (AD9943)



4.1.3 Circuit Guide (CCD)



4.2. Package Information



Package	Type	Pin pitch	Size(WxD)
	64 - LQFP	0.40mm	7x7mm

5. Revision History

REVISION	DATE	DESCRIPTION

6. Contact Information

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