Power MOSFET

40 V, 51 A, Single N-Channel, DPAK

Features

- Low R_{DS(on)}
- High Current Capability
- Avalanche Energy Specified
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- LED Backlight Driver
- CCFL Backlight
- DC Motor Control
- Power Supply Secondary Side Synchronous Rectification

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	40	V
Gate-to-Source Voltage - Continuous			V_{GS}	±20	V
Gate–to–Source Voltage – Non–Repetitive (t _p < 10 μS)			V_{GS}	±30	V
Continuous Drain	Steady State	T _C = 25°C	I _D	51	Α
Current (R _{θJC}) (Note 1)		T _C = 100°C		36	
Power Dissipation (R _{θJC}) (Note 1)		T _C = 25°C	P _D	47	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	85	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	°C
Source Current (Body Diode)			I _S	30	Α
Single Pulse Drain-to-Source Avalanche Energy (V_{DD} = 50 V, V_{GS} = 10 V, R_{G} = 25 Ω , $I_{L(pk)}$ = 40 A, L = 0.1 mH, V_{DS} = 40 V)			E _{AS}	80	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.2	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	107	

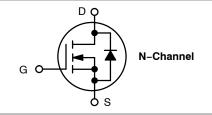
1. Surface-mounted on FR4 board using the minimum recommended pad size.



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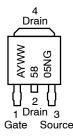
V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX	
40 V	16 m Ω @ 5.0 V	51 A	
	9.5 mΩ @ 10 V	51 A	





DPAK
CASE 369C
(Surface Mount)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location*

Y = Year

WW = Work Week

5805N = Device Code

G = Pb-Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

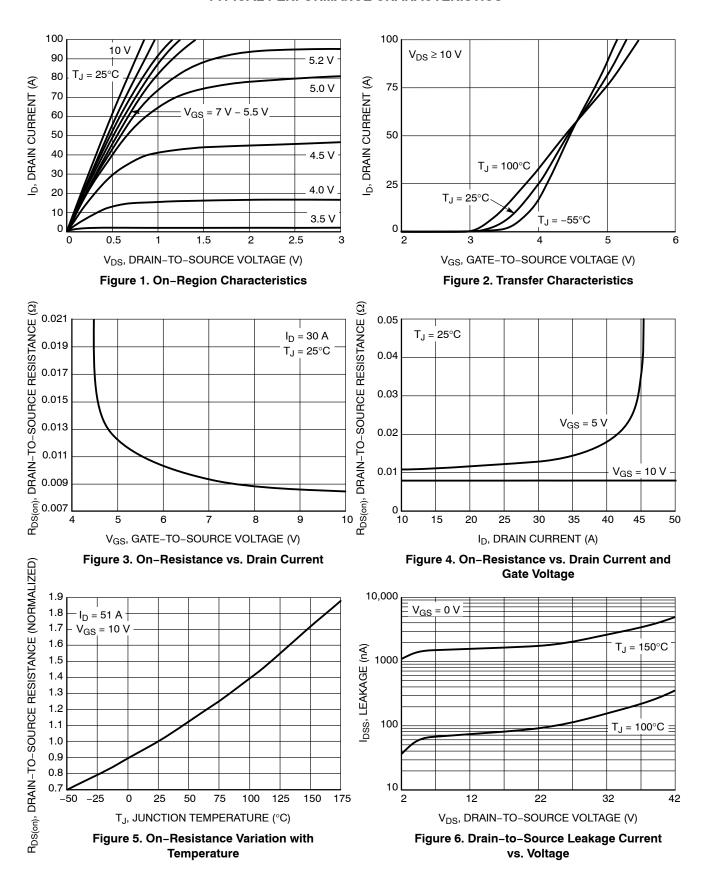
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•					•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				40.8		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	$V_{CC} = 0 \text{ V}$ $T_J = 25^{\circ}\text{C}$				1.0	μΑ
		$V_{GS} = 0 V$, $V_{DS} = 40 V$	T _J = 150°C			100	1
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	s = ±20 V			±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 250 μΑ	1.5		3.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				7.04		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _[₎ = 15 A		7.6	9.5	mΩ
		V _{GS} = 5.0 V, I	_O = 10 A		10.9	16	1
Forward Transconductance	gFS	V _{DS} = 15 V, I _E	₎ = 15 A		8.54		S
CHARGES, CAPACITANCES AND GA	TE RESISTANCE	ES .				•	
Input Capacitance	C _{iss}				1725		pF
Output Capacitance	C _{oss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			220		1 !
Reverse Transfer Capacitance	C _{rss}				160		1
Total Gate Charge	Q _{G(TOT)}				33	80	nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 10 \text{ V}, V_{DS} = 32 \text{ V},$ $I_{D} = 30 \text{ A}$			2.0		1
Gate-to-Source Charge	Q _{GS}				7.2		1
Gate-to-Drain Charge	Q_{GD}				9.8		1
SWITCHING CHARACTERISTICS (Not	e 3)					•	
Turn-On Delay Time	t _{d(on)}				10.2		ns
Rise Time	t _r	V _{GS} = 10 V, V _D	n = 32 V.		17.9		1
Turn-Off Delay Time	t _{d(off)}	$I_D = 30 \text{ A}, R_G$	= 2.5 Ω		22.9		1
Fall Time	t _f				4.5		1
DRAIN-SOURCE DIODE CHARACTER	RISTICS						
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C		0.83	1.2	V
			T _J = 150°C		0.65		7
Reverse Recovery Time	t _{RR}	V_{GS} = 0 V, dls/dt = 100 A/ μ s, I_{S} = 30 A			24.8		ns
Charge Time	ta				14.6		1
Discharge Time	tb				10.2		1
Reverse Recovery Charge	Q _{RR}				15.5		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

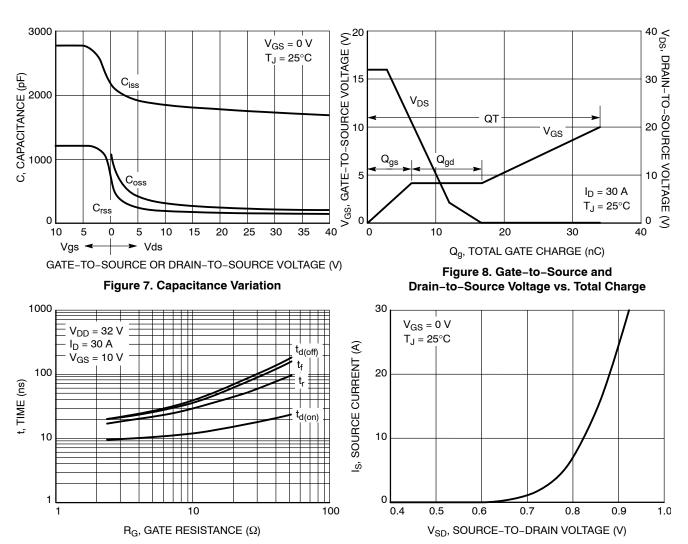


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

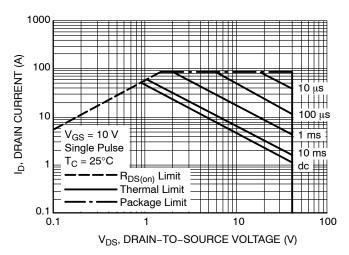


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CHARACTERISTICS

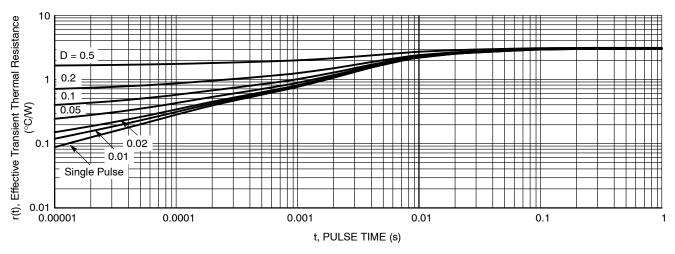


Figure 12. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NTD5805NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5805NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5805NT4G-VF01	DPAK (Pb-Free)	2500 / Tape & Reel

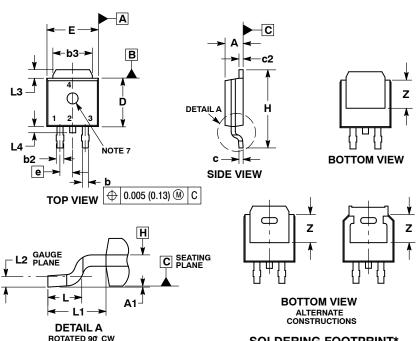
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging

Specifications Brochure, BRD8011/D.
*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)

CASE 369C **ISSUE F**



NOTES:

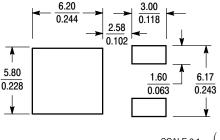
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES.
- 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-MENSIONS b3, L3 and Z.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD
- FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL
- NOT EXCEED 0.006 INCHES PER SIDE.
 5. DIMENSIONS D AND E ARE DETERMINED AT THE
- OUTERMOST EXTREMES OF THE PLASTIC BODY. 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIM	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.028	0.045	0.72	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
е	0.090	BSC	2.29	BSC	
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.114 REF		2.90	REF	
L2	0.020 BSC		0.51	BSC	
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

STYLE 2: PIN 1. GATE 2. DRAIN

- SOURCE

SOLDERING FOOTPRINT*



mm SCALE 3:1

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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