

MOSFET - Power, Single, N-Channel, TSOP-6

30 V, 7.0 A

NTGS4141N, NVGS4141N

Features

- Low $R_{DS(on)}$
- Low Gate Charge
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Pb-Free Package is Available

Applications

- Load Switch
- Notebook PC
- Desktop PC

MAXIMUM RATINGS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DS}	30	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	I_D	5.0	A
		$T_A = 85\text{ }^\circ\text{C}$		3.6	
	$t \leq 10\text{ s}$	$T_A = 25\text{ }^\circ\text{C}$		7.0	
Power Dissipation (Note 1)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	P_D	1.0	W
		$t \leq 10\text{ s}$		2.0	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	I_D	3.5	A
		$T_A = 85\text{ }^\circ\text{C}$		2.5	
Power Dissipation (Note 2)		$T_A = 25\text{ }^\circ\text{C}$	P_D	0.5	W
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}, V_{GS} = 10\text{ V}$	I_{DM}	45	A	
Pulsed Drain Current	$t_p = 30\text{ }\mu\text{s}, V_{GS} = 5\text{ V}$	I_D	30	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	2.0	A	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 30\text{ V}, I_L = 10.4\text{ A}, V_{GS} = 10\text{ V}, L = 1.0\text{ mH}, R_G = 25\text{ }\Omega$)		EAS	54	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

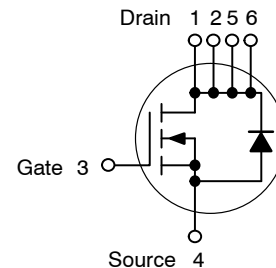
THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	248	

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0773 in sq).

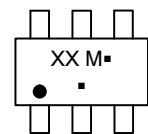
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	21.5 m Ω @ 10 V	7.0 A
	30 m Ω @ 4.5 V	

N-Channel



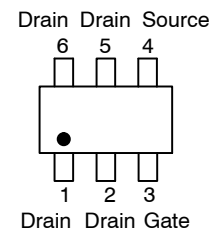
TSOP-6
CASE 318G
STYLE 1

MARKING DIAGRAM



- XX = Device Code
 - M = Date Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

NTGS4141N, NVGS4141N

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			18.4		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		1.0	μA
			$T_J = 125\text{ }^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.7		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.0\text{ A}$		21.5	25	mΩ
		$V_{GS} = 4.5\text{ V}, I_D = 6.0\text{ A}$		30	35	
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 7.0\text{ A}$		30		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 24\text{ V}$		560		pF
Output Capacitance	C_{OSS}			115		
Reverse Transfer Capacitance	C_{RSS}			75		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 7.0\text{ A}$		12		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.85		
Gate-to-Source Charge	Q_{GS}			1.9		
Gate-to-Drain Charge	Q_{GD}			3.0		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 7.0\text{ A}$		6.0		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.8		
Gate-to-Source Charge	Q_{GS}			1.85		
Gate-to-Drain Charge	Q_{GD}			3.0		
Gate Resistance	R_G			2.8		Ω

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 24\text{ V}, I_D = 7.0\text{ A}, R_G = 3.0\text{ }\Omega$		6.0		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(OFF)}$			18		
Fall Time	t_f			4.0		

DRAIN - SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$	$T_J = 25\text{ }^\circ\text{C}$		0.78	1.0	V
			$T_J = 125\text{ }^\circ\text{C}$		0.63		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 2.0\text{ A}$			15		ns
Charge Time	t_a				9.0		
Discharge Time	t_b				6.0		
Reverse Recovery Charge	Q_{RR}				8.0		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

NTGS4141N, NVGS4141N

TYPICAL PERFORMANCE CURVES

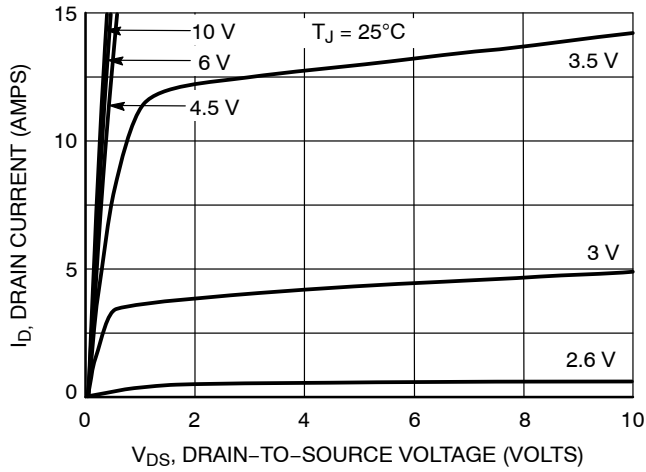


Figure 1. On-Region Characteristics

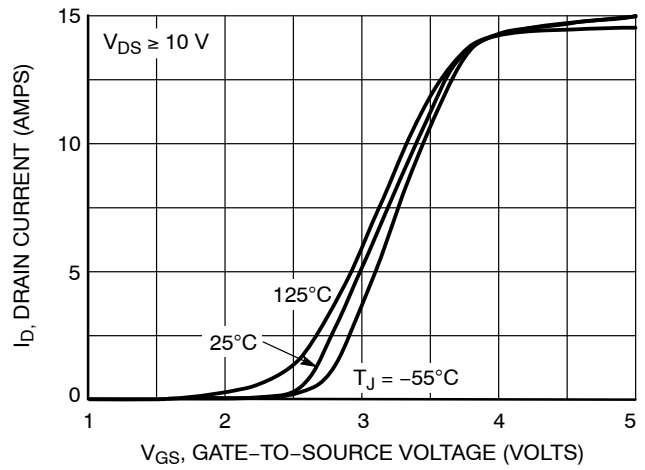


Figure 2. Transfer Characteristics

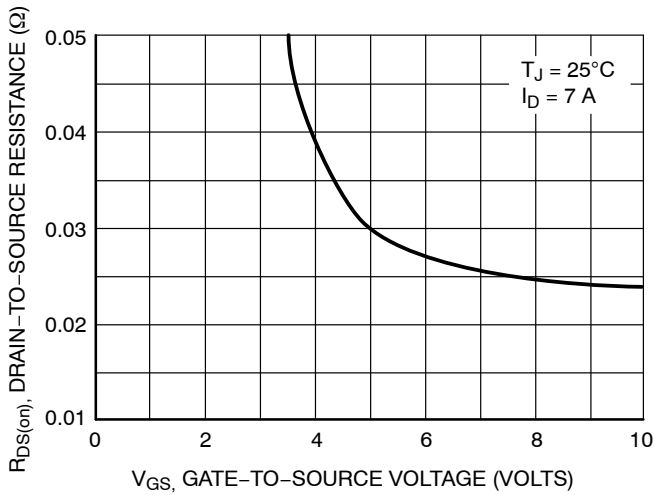


Figure 3. On-Resistance vs. Gate-to-Source Voltage

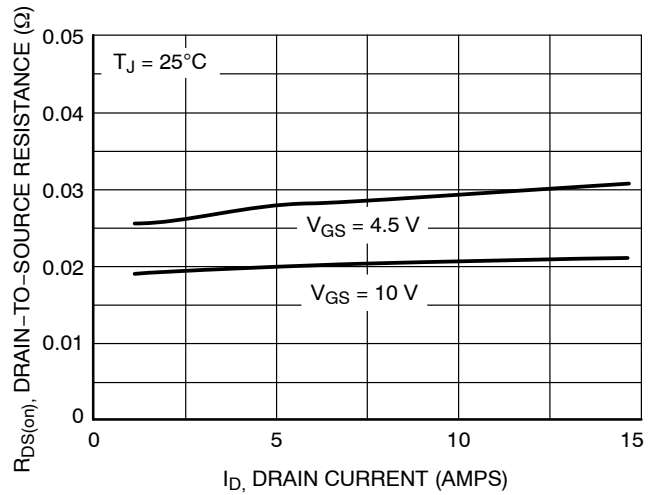


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

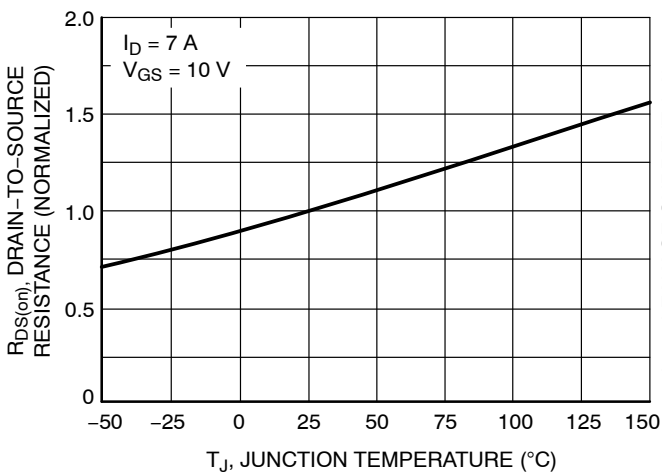


Figure 5. On-Resistance Variation with Temperature

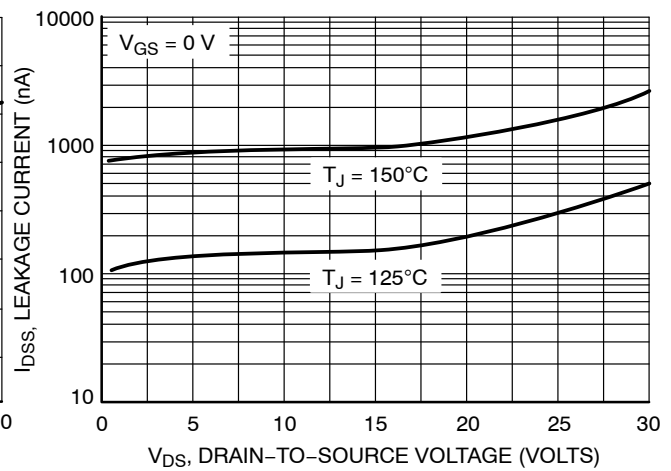
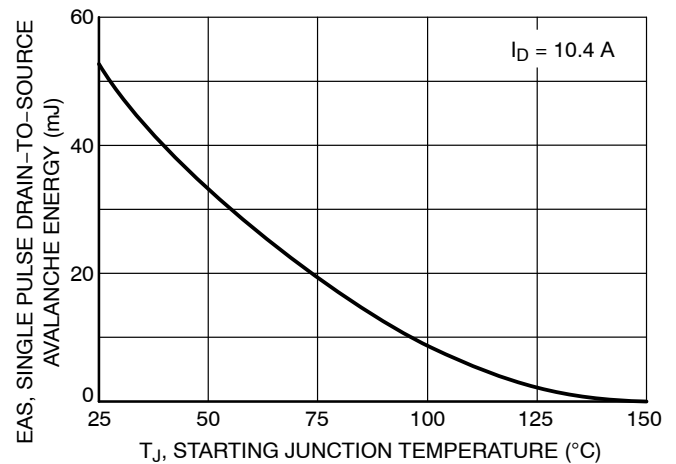
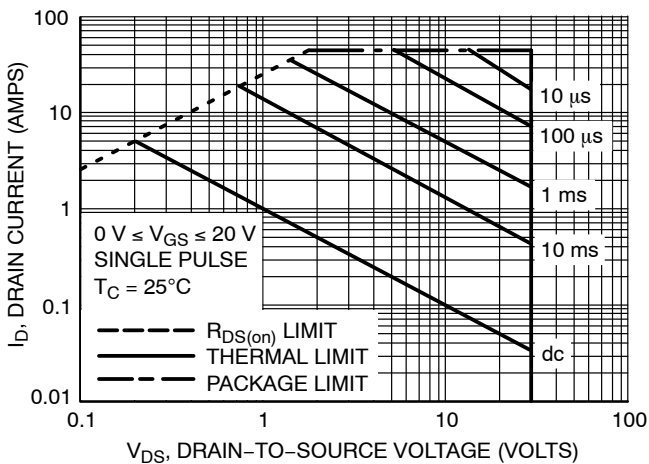
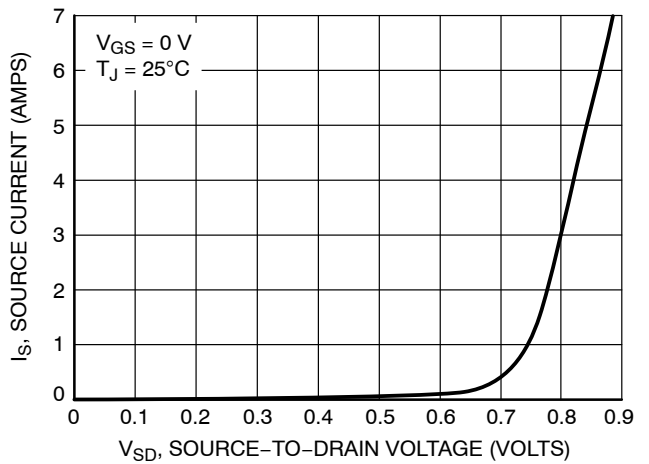
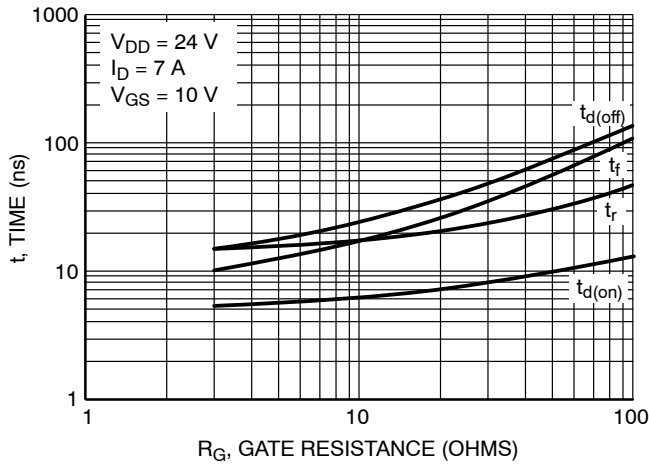
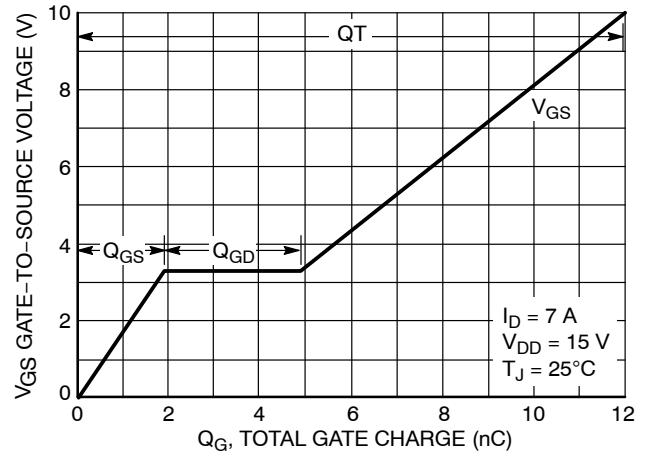
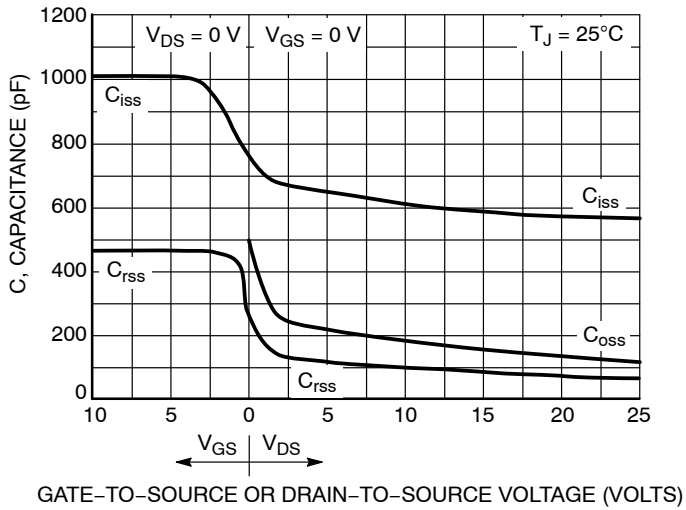


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTGS4141N, NVGS4141N

TYPICAL PERFORMANCE CURVES



NTGS4141N, NVGS4141N

TYPICAL PERFORMANCE CURVES

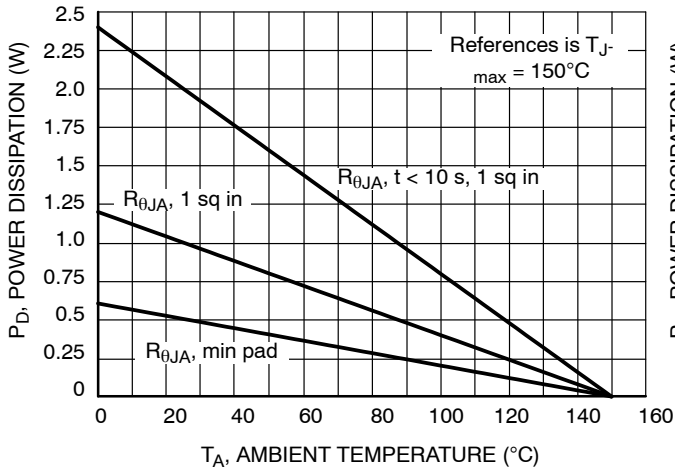


Figure 13. Maximum Power Derating Chart

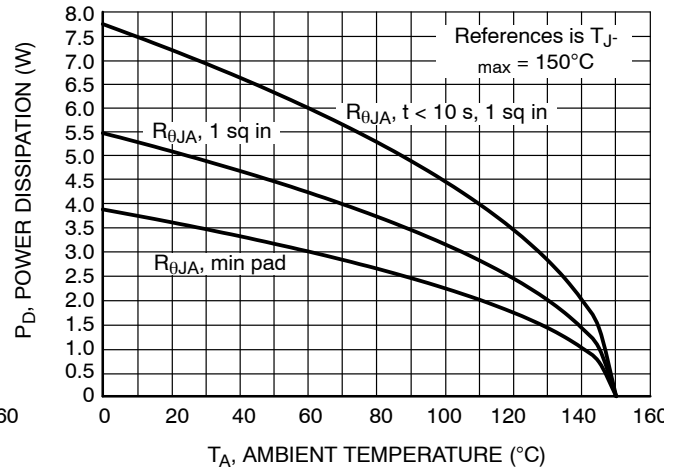


Figure 14. Current Derating Chart

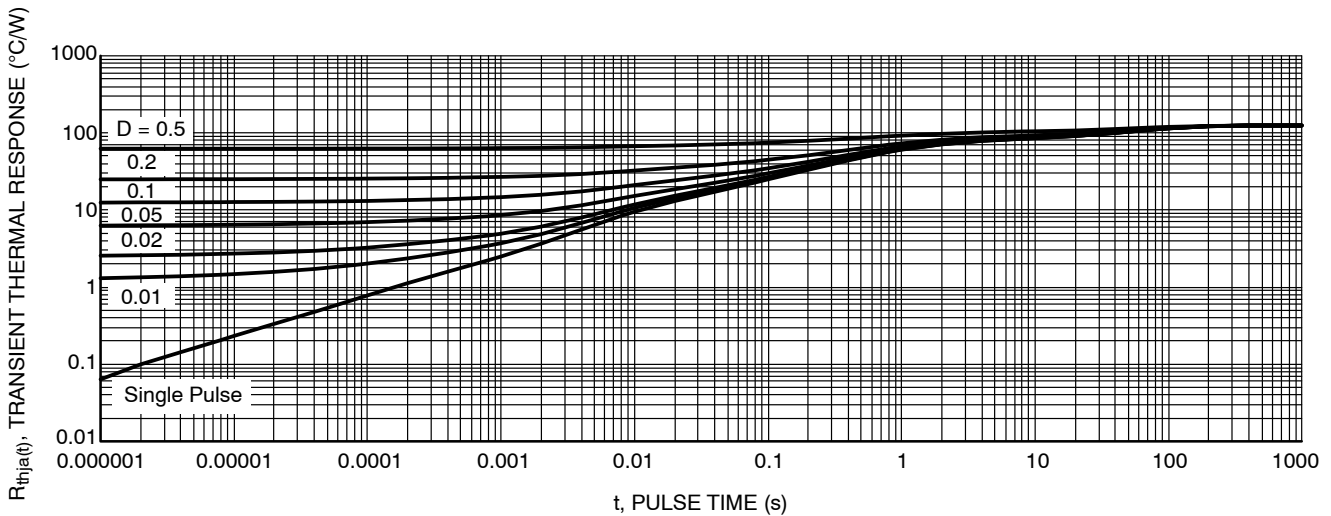


Figure 15. Thermal Response

Table 1. ORDERING INFORMATION

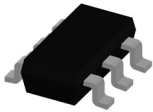
Part Number	Marking (XX)	Package	Shipping†
NTGS4141NT1G	S4	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NVGS4141NT1G	VS4	TSOP-6 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 5)

NTGS4141NT1	S4	TSOP-6	3000 / Tape & Reel
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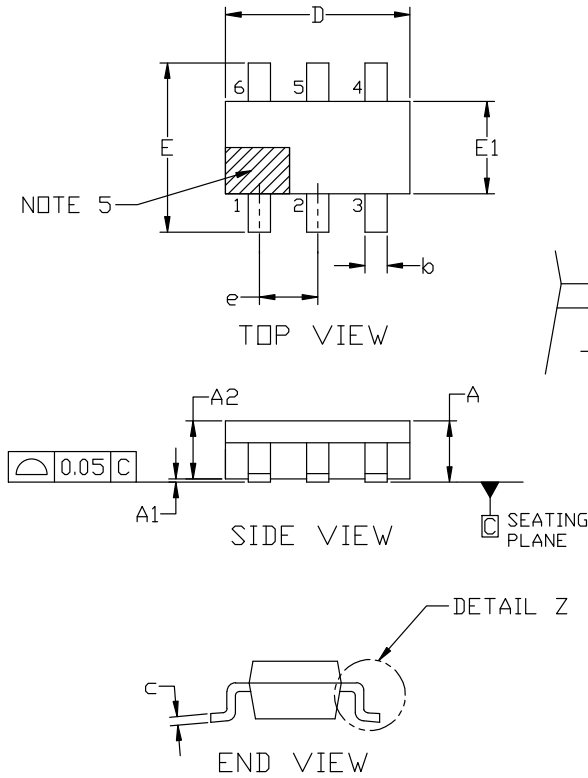
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



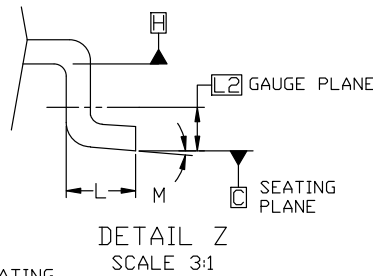
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

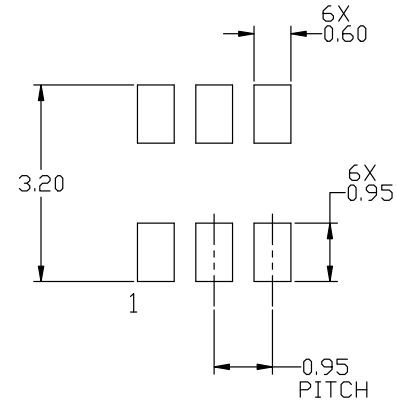


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

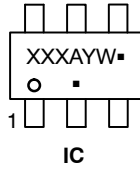
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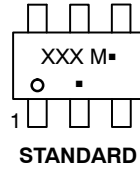
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

**GENERIC
MARKING DIAGRAM***



IC



STANDARD

XXX = Specific Device Code	XXX = Specific Device Code
A = Assembly Location	M = Date Code
Y = Year	▪ = Pb-Free Package
W = Work Week	
▪ = Pb-Free Package	

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | | |
|--|--|---|---|---|--|
| STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN | STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2 | STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out | STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD | STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2 | STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR |
| STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER | STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND | STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE | STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+ | STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2 | STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O |
| STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1 | STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN | STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE | STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE | STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR | |

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