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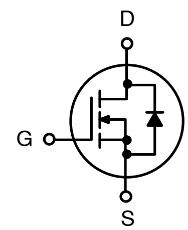
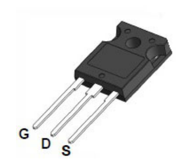
MOSFET – Power, N-Channel, Automotive SUPERFET® III, Easy-drive
650 V, 75 A, 25 mΩ

NVHL025N65S3

BV_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
650 V	25 mΩ @ 10 V	75 A

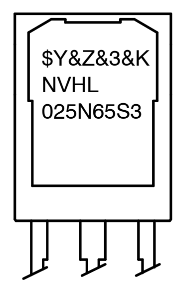


N-Channel MOSFET



TO−247−3LD
CASE 340CX

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
NVHL025N65S3	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

SuperFET III MOSFET is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss provide superior switching performance, and with−stand extreme dv/dt rate. Consequently, SuperFET III MOSFET Easy−drive series helps manage EMI issues and allows for easier design implementation.

Features

- AEC−Q101 Qualified
- Max Junction Temperature 150°C
- Typ. $R_{DS}(on)$ = 19.9 mΩ
- Ultra Low Gate Charge (Typ. Q_G = 236 nC)
- Low Effective Output Capacitance (Typ. C_{OSS}(eff.) = 2062 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Automotive PHEV−BEV DC−DC Converter
- Automotive Onboard Charger for PHEV−BEV

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC Positive	30	V
		AC Positive, (f > 1 Hz)	30	V
		AC Negative, (f > 1 Hz)	−20	V
I_D	Drain Current	Continuous (Tc = 25°C)	75	A
		Continuous (Tc = 100°C)	65.8	A
I_{DM}	Pulsed Drain Current	Pulsed (Note 1)	300	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		2025	mJ
E_{AR}	Repetitive Avalanche (Note 1)		5.95	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	V/ns
P_D	Power Dissipation	(Tc = 25°C)	595	W
		Derate Above 25°C	4.76	W/°C
T_J,T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 15 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} < 75 A, di/dt ≤ 200 A/ms, VDD ≤ BVDSS, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.21	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	40	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Shipping (Qty / Packing)
NVHL025N65S3	NVHL025N65S3	TO−247−3LD	Tube	30 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–to–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	713	–	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	650	755	–	V
ΔBVDSS / ΔTJ	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	0.34	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	0.30	1	μA
		V_{DS} = 520 V, V_{GS} = 0 V, Tc = 125°C	–	7.92	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = +30 V, V_{DS} = 0 V	–	5.27	+100	nA
		V_{GS} = −20 V, V_{DS} = 0 V	–	2.65	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 3.0 mA	2.5	3.56	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 37.5 A, T_J = 25°C	–	19.9	25	mΩ
		V_{GS} = 10 V, I_D = 37.5 A, T_J = 100°C	–	34.6	–	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 75 A	–	78.5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	7330	–	pF
C_{oss}	Output Capacitance		–	197	–	pF
C_{rss}	Reverse Transfer Capacitance		–	33.6	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	2062	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	285	–	pF
$Q_{g(tot)}$	Total Gate Charge	V_{DS} = 400 V, V_{GS} = 10 V, I_D = 75 A (Note 4)	–	236	–	nC
Q_{gs}	Gate to Source Gate Charge		–	59.3	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	97.3	–	nC
R_G	Gate Resistance	f = 1 MHz	–	0.818	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 400 V, I_D = 75 A, V_{GS} = 10 V, R_G = 2 Ω (Note 4)	–	43.3	–	ns
t_r	Turn–On Rise Time		–	109	–	ns
$t_{d(off)}$	Turn–Off Delay Time		–	120	–	ns
t_f	Fall Time		–	107	–	ns
DRAIN–SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	75	A
I_{SM}	Maximum Plused Drain to Source Diode Forward Current		–	–	300	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 37.5 A	–	0.88	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 75 A dI_F/dt = 100 A/μs	–	714	–	nS
Q_{rr}	Reverse Recovery Charge		–	26.4	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

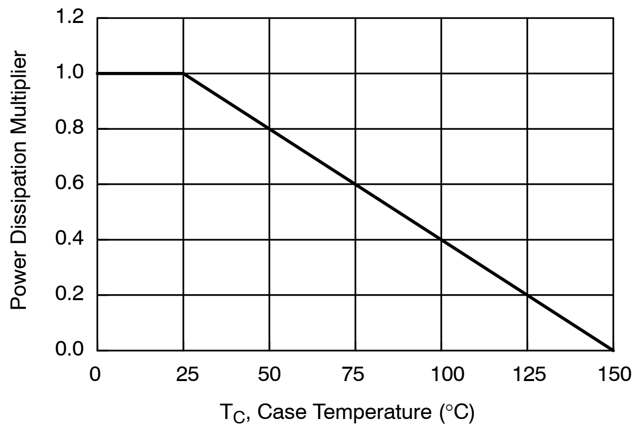


Figure 1. Normalized Power Dissipation vs. Case Temperature

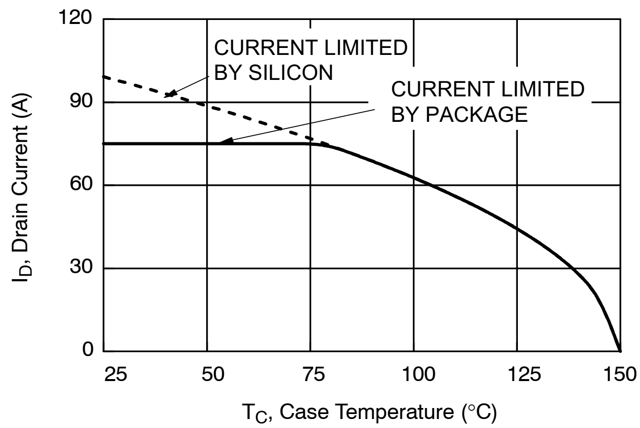


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

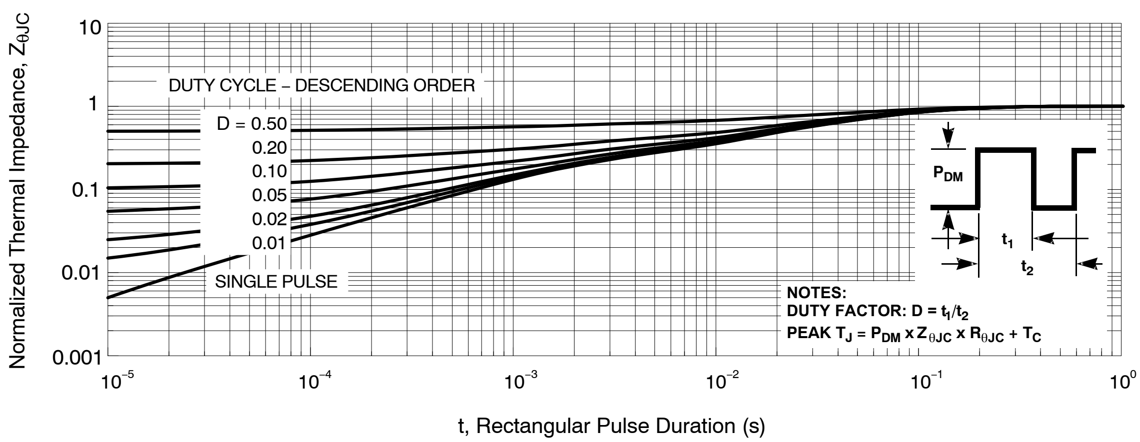


Figure 3. Normalized Maximum Transient Thermal Impedance

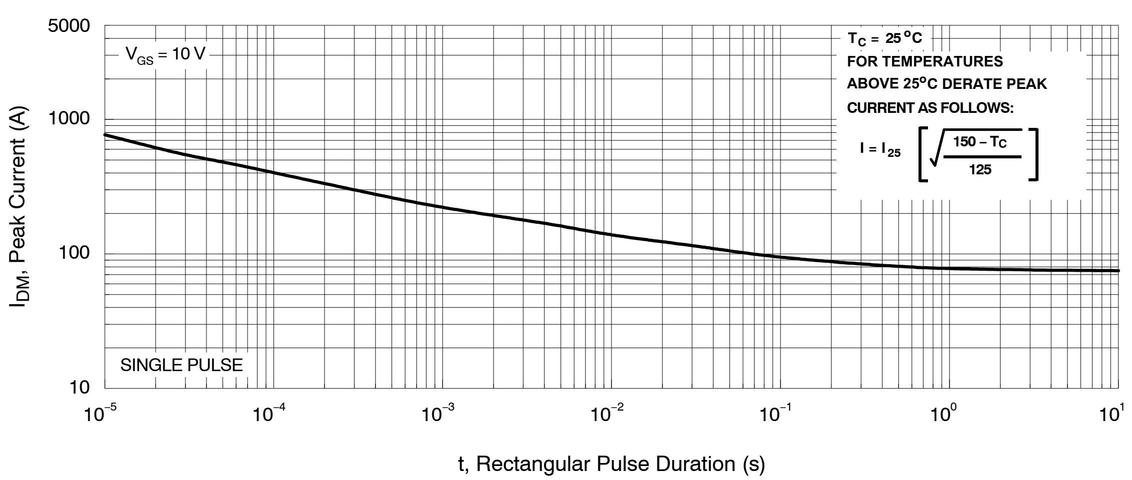


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

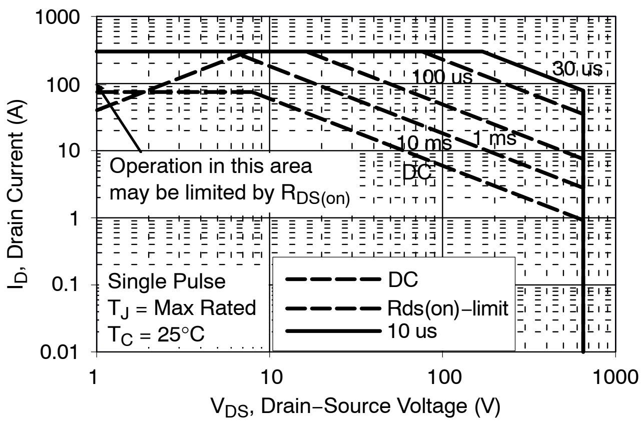


Figure 5. Forward Bias Safe Operating Area

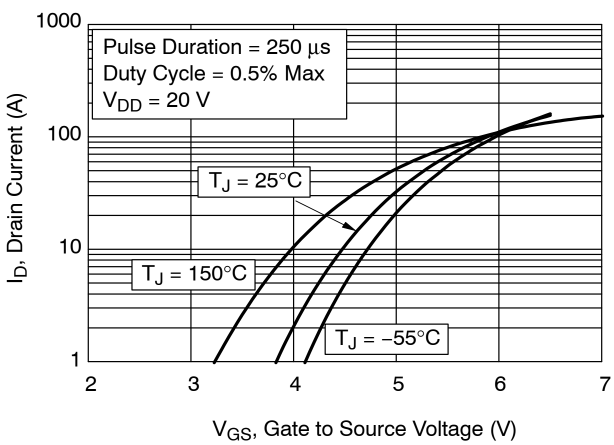


Figure 6. Transfer Characteristic

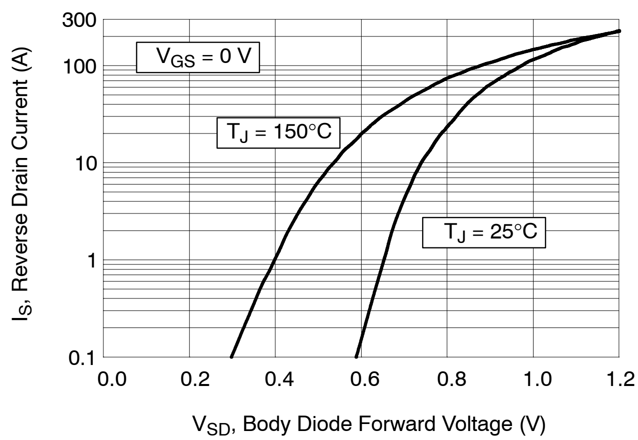


Figure 7. Forward Diode Characteristics

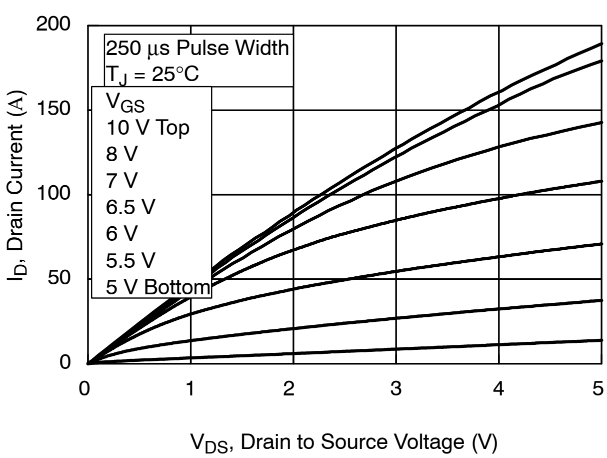


Figure 8. Saturation Characteristics

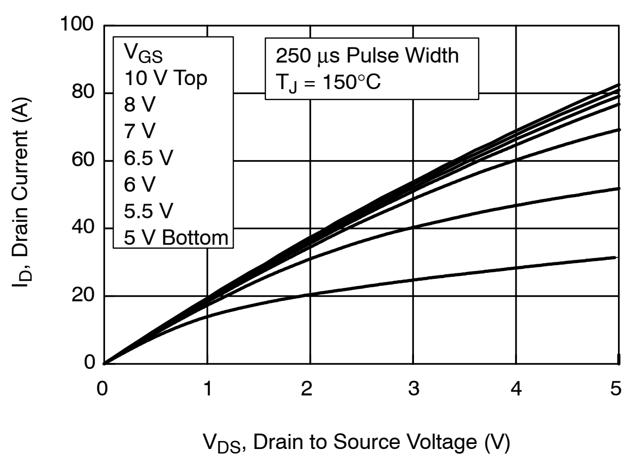


Figure 9. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

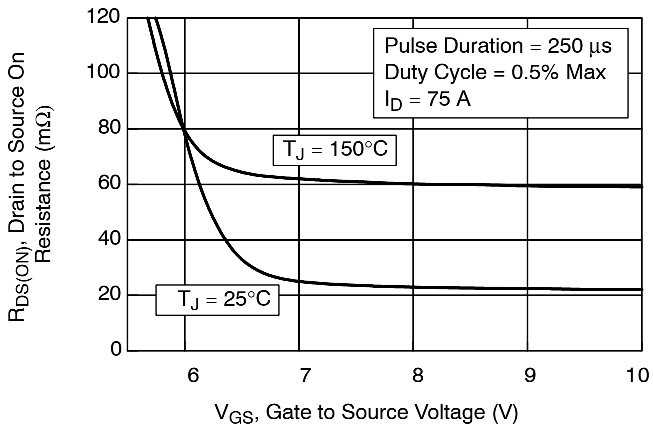


Figure 10. R_{DSON} vs. Gate Voltage

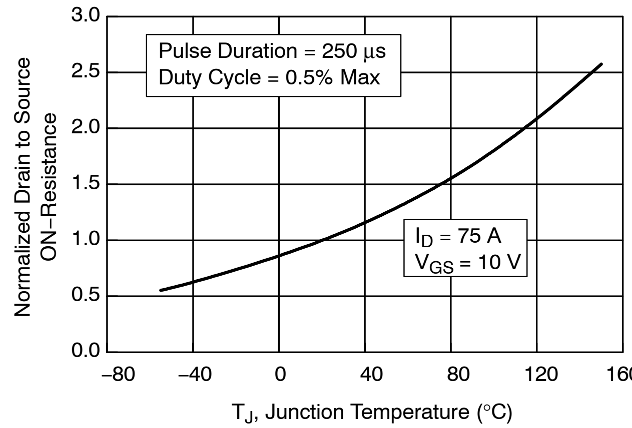


Figure 11. Normalized R_{DSON} vs. Junction Temperature

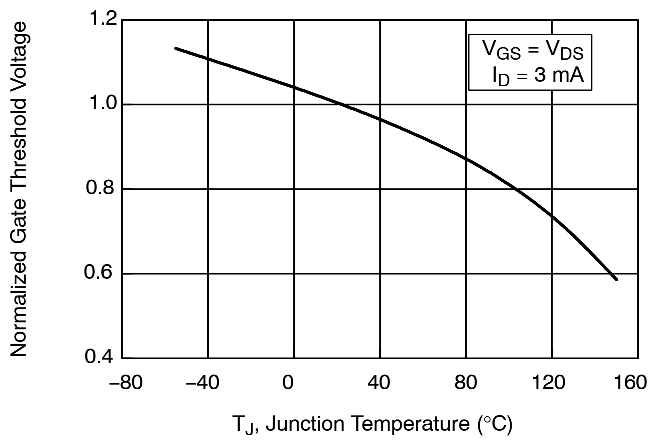


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

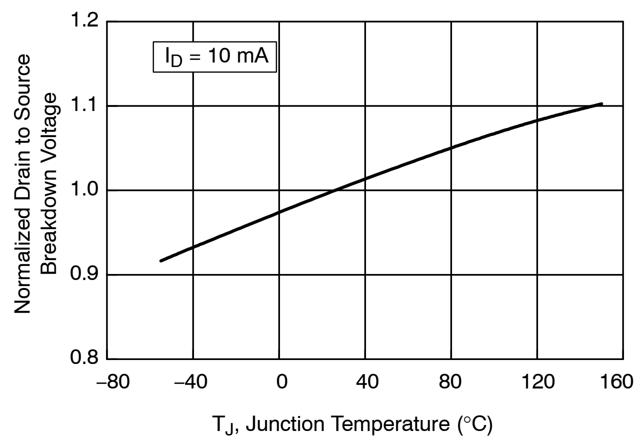


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

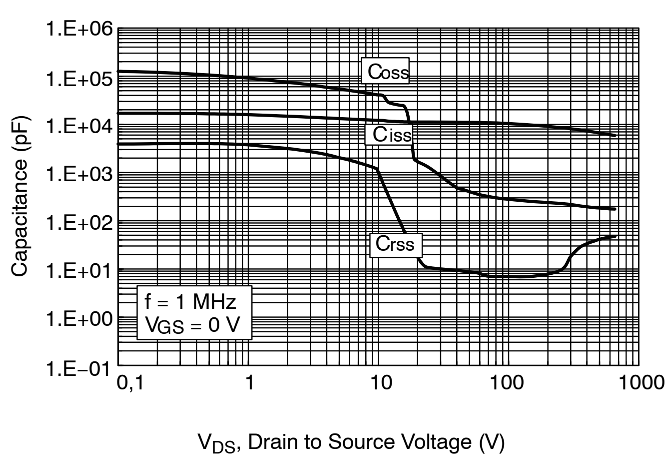


Figure 14. Capacitance vs. Drain to Source Volatage

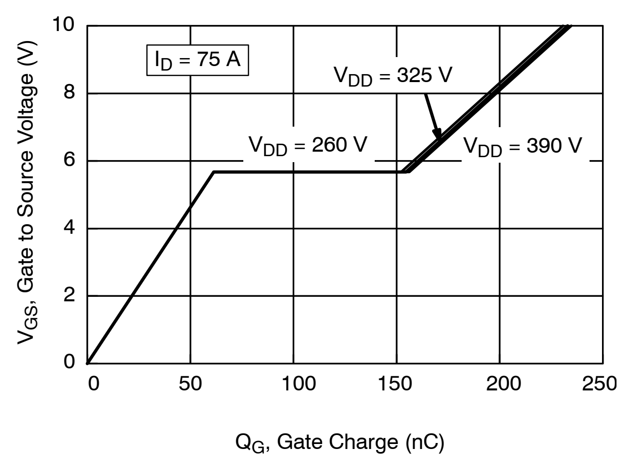


Figure 15. Gate Charge vs. Gate to Source Voltage

TYPICAL CHARACTERISTICS (continued)

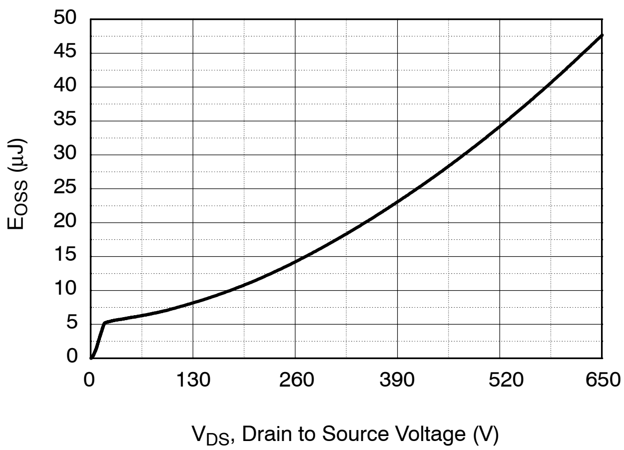


Figure 16. E_{OSS} vs. Drain to Source Voltage

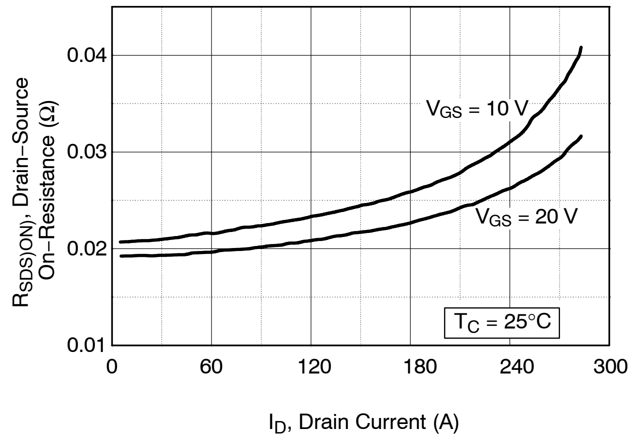


Figure 17. On−Resistance Variation vs. Drain Current and Gate Voltage

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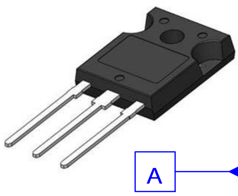
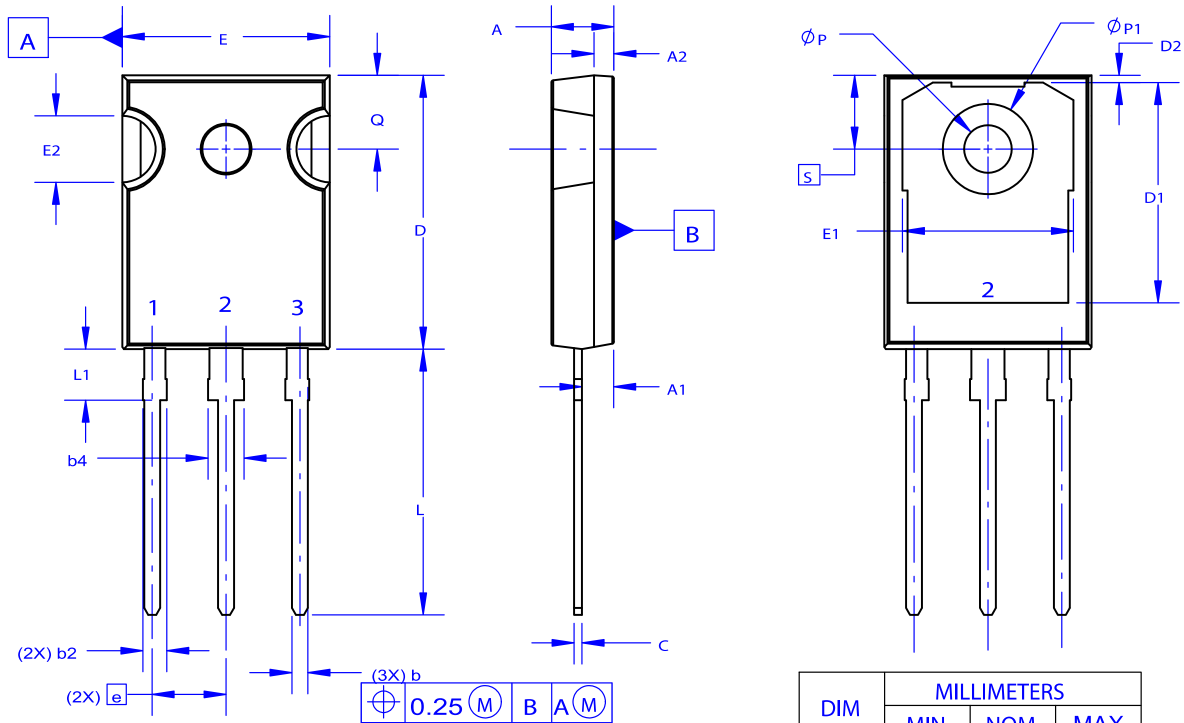


TO−247−3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020

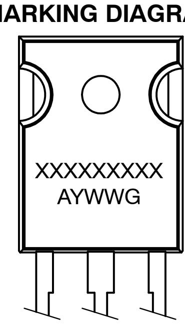


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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