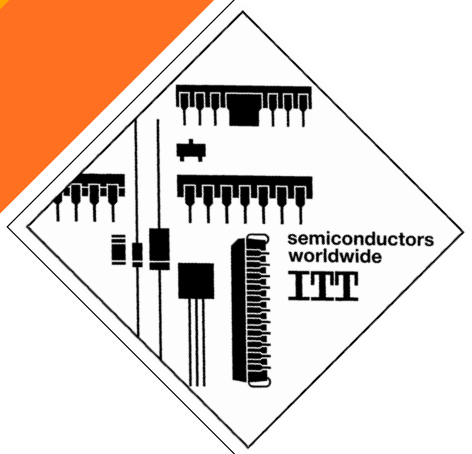

NVM 3060
4096-Bit EEPROM

Edition Feb. 14, 1990
6251-309-2/E

ITT Semiconductors

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4096-Bit EEPROM

1. Introduction

Electrically erasable programmable read-only memory (EEPROM) in N-channel floating-gate technology with a capacity of 512 words, 8 bits each.

The NVM 3060 is intended for use as a reprogrammable non-volatile memory in conjunction with the CCU 2030/2050/2070/3000 series Central Control Units or the SAA 12xx and TVPO 2066 Remote Control and Tuning ICs. It serves for storing the tuning information as well as several analog settings, further alignment information given in the factory when producing the TV set. The stored information remains stored even with the supply voltages switched off. Reading and programming operations are executed via the IM bus (see section 5.). Input and output signals are TTL level. An address option input provides the possibility to operate two memories in parallel, to obtain a total storage capacity of 8192 bits.

The device contains an on-chip charge pump for high programming voltage generation and an on-chip clock oscillator.

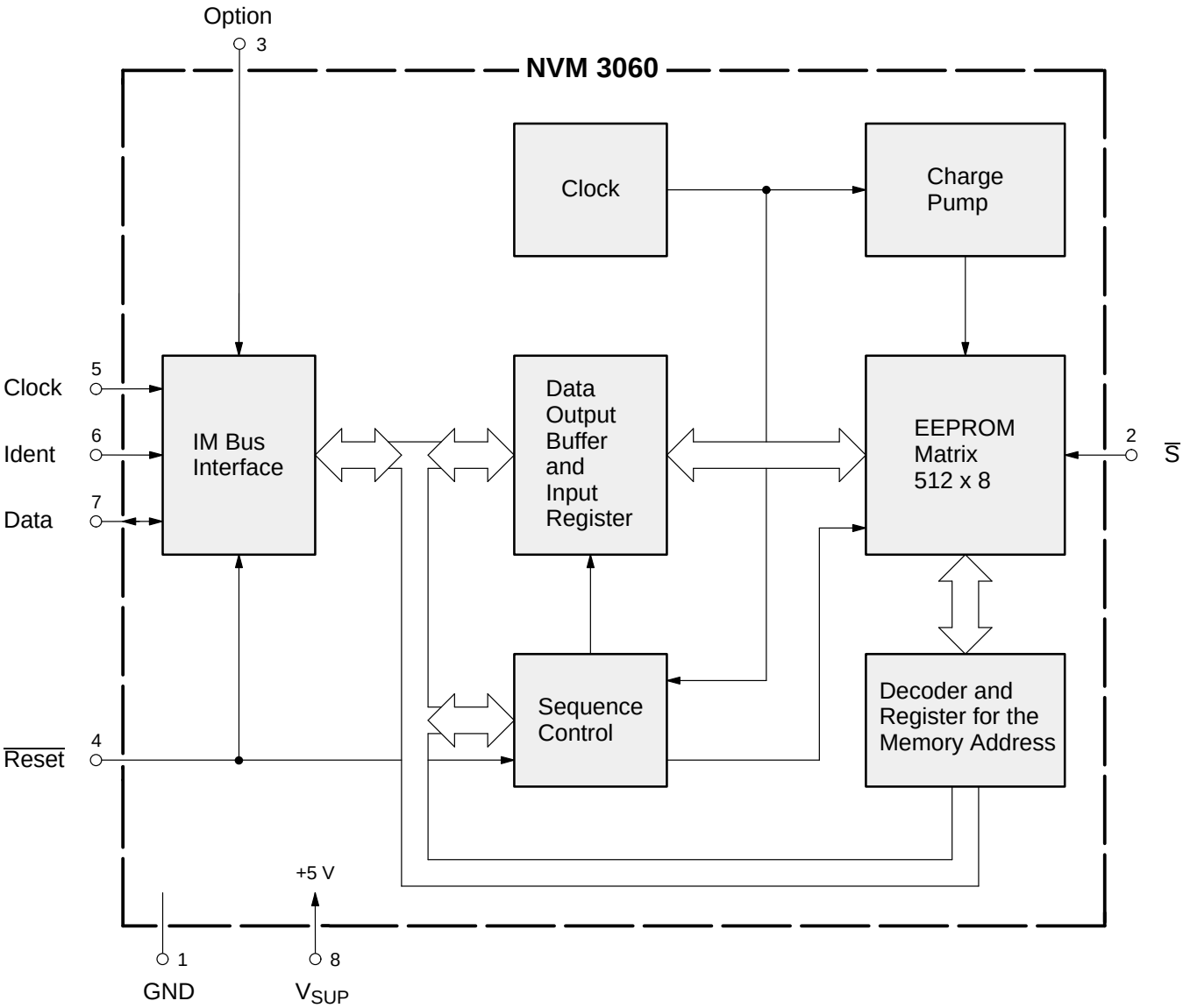


Fig. 1–1: Block diagram of the NVM 3060 EEPROM

2. Specifications

2.1. Outline Dimensions

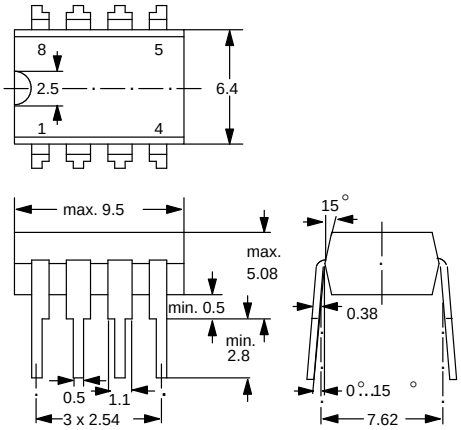


Fig. 2–1: NVM 3060 in 8-pin Dil Plastic Package 20 A 8 according to DIN 41870

Weight approx. 0.5 g Dimensions in mm

2.2. Pin Connections

1 Ground, 0

2 Safe Input $\overline{S}$

3 Option Input

4 $\overline{\text{Reset}}$ Input

5 IM Bus Clock Input

6 IM Bus Ident Input

7 IM Bus Data Input/Output

8 Supply Voltage V_{SUP}

2.3. Pin Descriptions

Pin 1 – Ground, 0
This pin must be connected to the negative of the supplies.

Pin 2 – Safe Input $\overline{S}$
Fig. 2–2 shows the internal configuration of this input. Normally, with pin 2 at ground potential (low), one portion of the programming matrix is protected so that this part of the memory cannot be reprogrammed inadvertently. Only when pin 2 receives high potential continuously, the protected portion of the memory matrix can be programmed. Pin 2 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pin 3 – Option Input Fig. 2–2 shows the internal configuration of this input. With pin 3 at ground potential (low) or floating, the NVM 3060 reacts upon the IM bus addresses 128,129 and 131. With pin 3 continuously at V_{SUP} potential (high), the NVM 3060 reacts upon this IM bus addresses 132,133 and 135 (see Fig.2–6). In this way, parallel operation of two NVM 3060 is permitted, to obtain 8192 bits of non-volatile storage directly accessible via the IM bus. Pin 3 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pin 4 – $\overline{\text{Reset}}$ Input
This input has a configuration as shown in Fig. 2–3. Via this input, the NVM 3060, together with the other circuits belonging to the system, receives the $\overline{\text{Reset}}$ signal which is derived from V_{SUP} via an external RC circuit. A low level is required during power-up and power-down procedures. Low level at pin 4 (max. 1.3 V) cancels a programming procedure and an IM bus operation in progress. The memory address register is not erased. During operation, pin 4 requires high level (min. 2.4 V).

Pins 5 to 7 – IM Bus Connections
These pins serve to connect the NVM 3060 EEPROM to the IM bus (see section 5.), via which it communicates with the CCU 2030/2050/2070/3000 Central Control Units or the SAA 12xx and TVPO 2066 Remote Control and Tuning ICs. Pins 5 (IM Bus Clock Input) and 6 (IM Bus Ident Input) are inputs as shown in Fig. 2–3 and pin 7 (IM Bus Data) is an input/output as shown in Fig. 2–4. The signal diagram for the IM bus is illustrated in Figs. 2–6 and Fig. 5–1. The required addresses which the NVM 3060 EEPROM receives from the microcomputer, are also shown in Fig. 2–6.

Pin 8 – Supply Voltage V_{SUP}
The supply voltage required is +5V (±5%), and the current consumption in active operation is approx. 30 mA. Inserting or removing the NVM 3060 from a live socket may alter programmed data!

2.4. Pin Circuits

The following figures show schematically the circuitry at the various pins. The integrated protection structures are not shown. The letter "E" means enhancement, the letter "D" depletion.

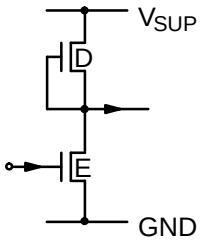


Fig. 2–3:
Pins 4, 5, and 6, Inputs

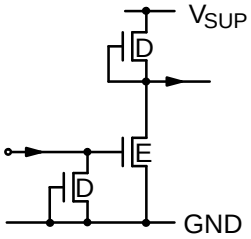


Fig. 2–2:
Pins 2 and 3, Input $\overline{S}$

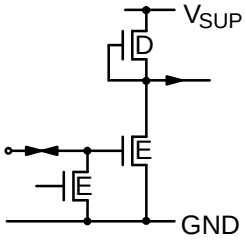


Fig. 2–4:
Pin 7, Input/Output

2.5. Electrical Characteristics

All Voltages are referred to ground.

2.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125*	°C
V_{SUP}	Supply Voltage	8	–0.5	+6	V
V_I	Input Voltage	2 to 7	–0.3 V	V_{SUP}	–
I_O	Output Current	7	–	5	mA

* Stored data may be affected by T_S above +85 °C

2.5.2. Recommended Operating Conditions

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	8	4.75	5.0	5.25	V
V_{IL}	Input Low Voltage	2, 3, 5 to 7	–	–	0.8	V
V_{IH}	Input High Voltage		2.4	–	–	V
V_{REIL}	$\overline{\text{Reset}}$ Input Low Voltage	4	–	–	1.3	V
V_{REIH}	$\overline{\text{Reset}}$ Input High Voltage		2.4	–	–	V
t_4	$V_{SUP} – V_{REI}$ Delay Time*	4, 8	0	–	–	ms
t_7	$V_{REI} – V_{SUP}$ Delay Time*		0	–	–	ms

*see Fig. 2–5

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{IMIL}	IM Bus Input Low Voltage	5 to 7	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	170	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs
t_{IM6}	ΦI Clock Input Setup Time before Ident End-Pulse Input		6.0	–	–	µs
t_{IM7}	IM Bus Input Delay Time after ΦI Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End-Pulse Low Time		3.0	–	–	µs

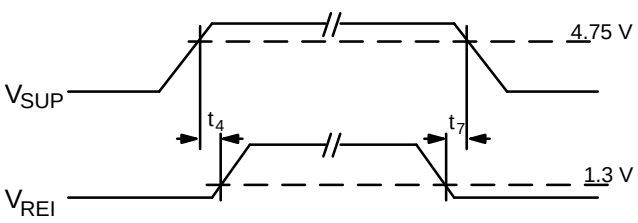
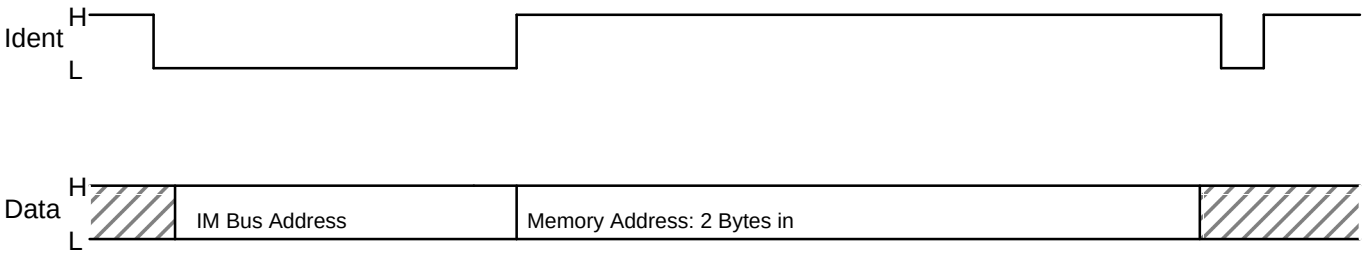


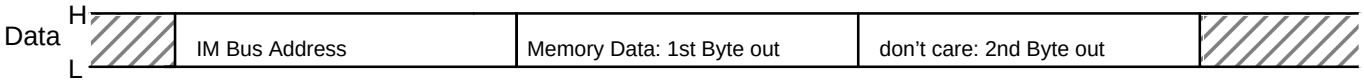
Fig. 2–5: Power on/off timing

2.5.3. Characteristics at V_{SUP} = 5 V, T_A= 25 °C

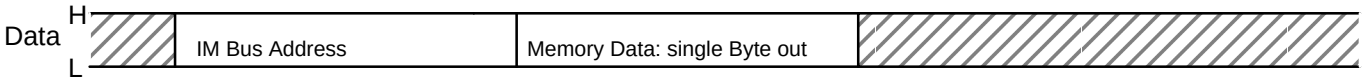
Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	8	17	35	60	mA	
I_{IH}	Input High Current	4 to 6	–	–	10	µA	V_{IH} = 5 V
V_{IMOL}	IM Bus Data Output Low Voltage	7	–	–	0.4	V	I_{IMO} = 3 mA
I_{IMOH}	IM Bus Data Output High Current		–	–	10	µA	V_{IMO} = 5 V
I_{IH}	Input Internal PUll-Down Current	2, 3	35	–	260	µA	V_{IH} = 5 V
t_P	Erase or Write Time		8	–	30	ms	



a) Entering memory address within a **16 Bit transfer**



b1) Reading data as first Byte within a **16 Bit transfer**



b2) Alternative to b1: Reading Data as a single Byte in an **8 Bit transfer**

c) Entering Data as first Byte within a **16 Bit transfer**

	IM Bus Address	
	Pin 3 Low	Pin 3 High
a) enter memory address:	128	132
b) reading:	129	133
c) programming:	131	135

Fig. 2–6: Signal diagram for the IM Bus

3. Functional Description

3.1. Memory Operation

The internal memory address space ranges from address 0 to address 511. Addresses 516 and 526 provide special functions.

To read a stored data word, the desired memory address has to be entered to the memory address register first. This is done by serially entering the IM bus address 128 (optionally 132) (during Ident = L), followed by the memory address (during Ident D = H) in a single IM bus operation.

With the memory address register set, the memory data may be read. This, in turn, is done by entering the IM bus address 129 (optionally 133) to the device (during Ident = L). Immediately after this, within the same IM bus operation (during Ident = H) the open-drain Data output will conduct to serially transmit the respective 8-bit memory data within a 16-bit word.

Reprogramming a memory location is done in two steps, a) and b), that are identical except for the data word to be entered. Step a) resets all bits to ″1″, and step b) programs the desired data into the selected memory location.

a) First, the desired memory address is entered in the way described above. Second, the actual programming is initiated by serially entering the IM bus address 131 (optionally 135) followed by the data word to be stored, which is 255 for step a). The device will now internally time its programming sequence. During this ″busy″ time all inputs are blocked from affecting the programming except for the $\overline{\text{Reset}}$ input. A $\overline{\text{Reset}}$ = L signal will immediately cancel any programming operation as well as any bus operation in progress.

The busy state may be interrogated by reading bit 1 of address location 526. A High level of this ″busy-bit″ indicates that programming is still under way. The IM bus operation for entering address 526 should always directly precede reading the busy-bit.

Reading any other address location during the busy state will produce erroneous data at the Data output. An address change operation during the busy state will not change the memory address register content. The intended start of another programming operation during the busy time will not be executed.

b) After time-out, normal operation may be resumed, e.g. by performing the second step of a programming sequence, i.e. by programming the desired 8-bit data word into the respective memory address location. This is done by restoring the proper memory address first, if necessary, and then by serially entering the IM bus address 131 (optionally 135) followed by the desired 8-bit data word as LSB in a 16-bit word. The device will again time its own programming sequence as described under a). After time-out the new data may be verified.

3.2. Testing

The NVM 3060 EEPROM contains circuitry designed to facilitate testing of the various functions. By programming data into address location 516, the device is switched to one or more of a number of test modes. A detailed description is given in section 4.

3.3. Protected Matrix

The programming matrix contains a protectable portion. Addresses 0 to 15, 64 to 79, 128 to 143, 192 to 207, 256 to 271, 320 to 335, 384 to 399 and 448 to 463 can only be programmed if the ″Safe″ input $\overline{\text{S}}$ (pin 2) is at high potential. In that way, this portion of the memory is protected against inadvertent reprogramming even if such false informations were received via the IM bus. The second part of the programming matrix is not protected.

3.4. Shipment

Parts are shipped with all bits set to ″1″.

7	6	5	4	3	2	1	0
Block programming enable	Read reference shift -0.3 V	Test Byte enable	Read reference shift -0.6V	Charge Pump disable	Read reference shift + 0.3 V		Read reference shift + 0.6 V

Fig. 4–1: Functions of the 8 bits in the test byte

4. Test Functions

This description of the test byte is not part of the specification. It contains no information necessary for normal (intended) use of the NVM 3060 memory. It is only intended as a description of the various functions of the test byte that are designed for factory use, but it does not specify such properties. The description is subject to change.

Address location 516 contains a test byte which governs test mode operation of the NVM 3060. The test byte is set by performing the IM bus operation for entering address 516, followed by an IM bus programming operation with the desired test data word. The test byte is valid during all following IM bus operations until changed or set to 0 by a $\overline{\text{Reset}}$ = L signal. The test byte shall not be changed during the busy time of a programming operation. Fig. 4–1 shows the bit arrangement of the test byte. Set bit 5 for activation of the test byte!

4.1. Block Programming

Three block program modes can be activated by the test byte, in conjunction with the memory address loaded into the memory address register:

memory address
9 8 7 6 5 4 3 2 1 0

1) all bytes are selected : 0 x x x x x x x 0 x (e.g. 0)

2) all even-numbered bytes are selected : 0 x x x x x x x 1 0 (e.g. 2)

3) all odd-numbered bytes are selected : 0 x x x x x x x 1 1 (e.g. 3)

Thus, programming all selected bytes with the same desired data is done within one programming sequence.

The complete sequence is:
Enter Address 516
Program Test byte (e.g. 160)
Enter Address 0, 2 or 3
Program Data

A checkerboard pattern is programmed with two programming operations after loading the test byte:

Enter Address 2
Program Data 85
Enter Address 3
Program Data 170

4.2. Read Reference Shifting

During read operations the memory cell threshold voltage is compared with a reference voltage. The comparator output then produces the logic one level for a cell threshold higher than the reference and the logic zero level for a cell threshold lower than the reference.

The test byte provides means to shift the reference voltage in positive or negative direction in three steps: ±0.3 V, ±0.6 V, and ±0.9 V.

During a read operation a positive-shifted reference voltage establishes a margin test for logic ones, whereas a negative-shifted reference does so for logic zeroes. This margin test is performed digitally by IM bus operations only, without the need to switch analog power supplies.

	7 6 5 4 3 2 1 0
+0.9V :	x 0 1 0 x 1 x 1
+0.6V :	x 0 1 0 x 0 x 1
+0.3V :	x 0 1 0 x 1 x 0
-0.3V :	x 1 1 0 x 0 x 0
-0.6V :	x 0 1 1 x 0 x 0
-0.9V :	x 1 1 1 x 0 x 0

4.3. Charge Pump Disable

Bit 3 of the test byte disables the high voltage charge pump.

5. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) has been designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with On-resistances of 150 Ω maximum. The 2.5 kΩ pull-up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 5–1. In The non-operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level as well to switch the first bit on the Data line. Thereafter eight address bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB.

The completion of the bus transaction is signalled by a short Low-state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

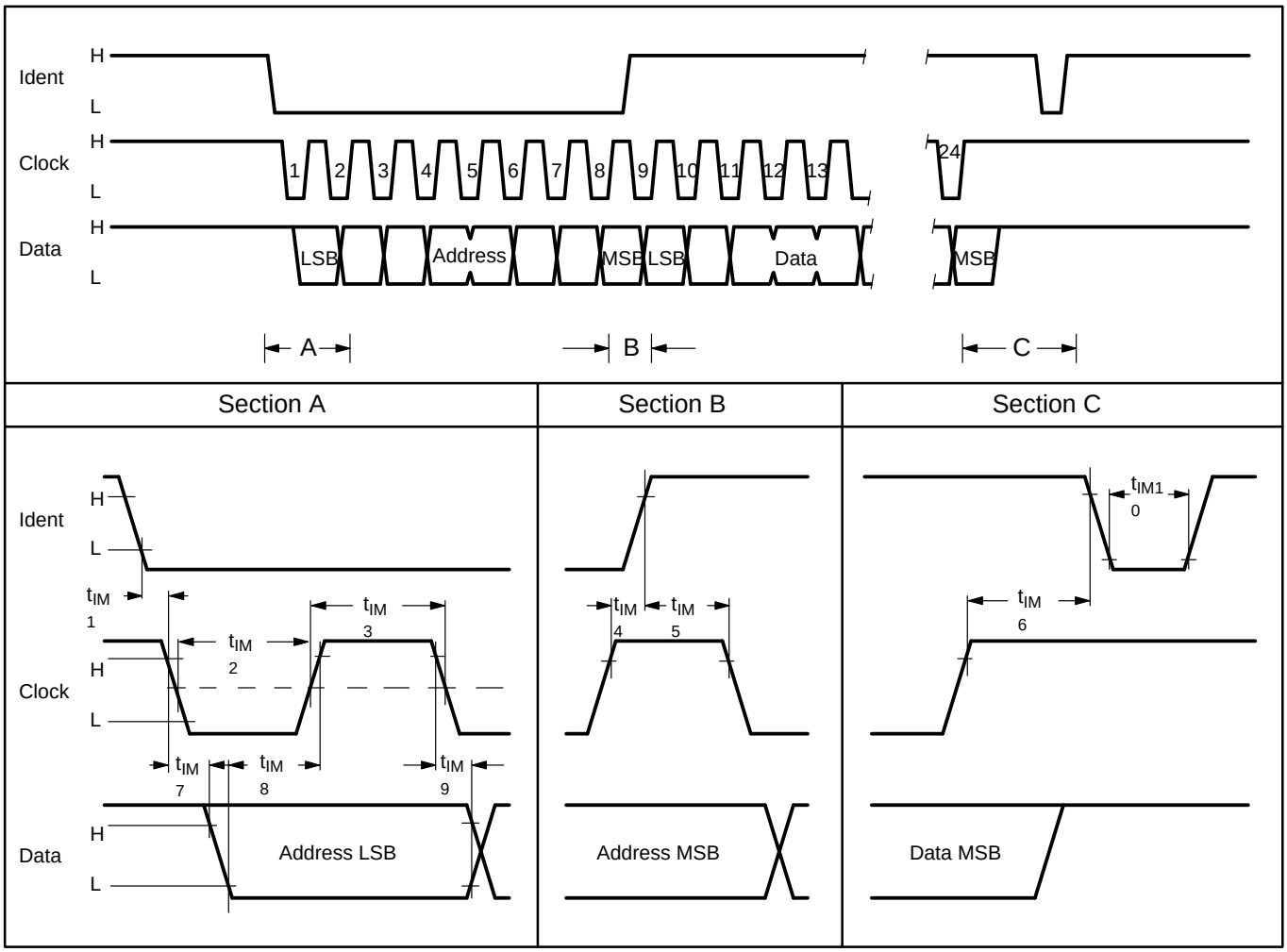


Fig. 5–1: IM bus waveforms

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