

NVMFD5489NL

MOSFET – Power, Dual N-Channel, Logic Level 60 V, 65 mΩ, 12 A



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Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- 175°C Operating Temperature
- NVMFD5489NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	60	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	$T_{mb} = 25^\circ\text{C}$	I_D 12	A
		$T_{mb} = 100^\circ\text{C}$	8.8	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	Steady State	$T_{mb} = 25^\circ\text{C}$	P_D 23.4	W
		$T_{mb} = 100^\circ\text{C}$	11.7	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3 & 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D 4.5	A
		$T_A = 100^\circ\text{C}$	3.2	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)	Steady State	$T_A = 25^\circ\text{C}$	P_D 3.0	W
		$T_A = 100^\circ\text{C}$	1.5	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM} 62	A	
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	22	A	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, I_{L(pk)} = 19.5 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	19	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

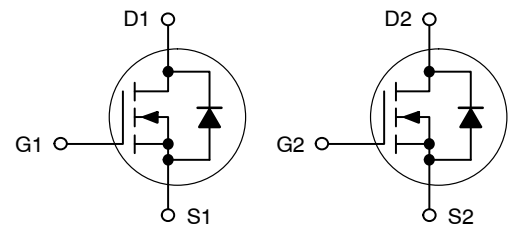
THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	6.4	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	50	
Junction-to-Ambient – Steady State (min footprint)		161	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.

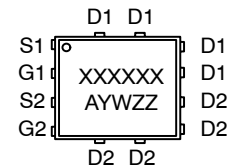
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	65 mΩ @ 10 V	12 A
	79 mΩ @ 4.5 V	

Dual N-Channel



DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



XXXXXX = 5489NL
(NVMFD5489NL) or
5489LW
(NVMFD5489NLWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFD5489NLT1G	DFN8 (Pb-Free)	1500/ Tape & Reel
NVMFD5489NLT3G	DFN8 (Pb-Free)	5000/ Tape & Reel
NVMFD5489NLWFT1G	DFN8 (Pb-Free)	1500/ Tape & Reel
NVMFD5489NLWFT3G	DFN8 (Pb-Free)	5000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	Reference to 25°C I _D = 250 μA		67		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V			1.0	μA
					10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.5		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	Reference to 25°C I _D = 250 μA		4.86		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		52	65	mΩ
		V _{GS} = 4.5 V, I _D = 7.5 A		66	79	

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		330		pF
Output Capacitance	C _{oss}		80			
Reverse Transfer Capacitance	C _{rss}		39			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 6 A		12.4		nC
Threshold Gate Charge	Q _{G(TH)}		0.31			
Gate-to-Source Charge	Q _{GS}		1.3			
Gate-to-Drain Charge	Q _{GD}		4.74			

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 6 A, R _G = 2.5 Ω		7		ns
Rise Time	t _r		11			
Turn-Off Delay Time	t _{d(off)}		31			
Fall Time	t _f		21			

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A		0.83	1.2	V
				0.71		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 10 A		24.2		ns
Charge Time	t _a		20.2			
Discharge Time	t _b		4.0			
Reverse Recovery Charge	Q _{RR}		26.5		nC	

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		0.93		nH
Drain Inductance	L _D		0.005			
Gate Inductance	L _G		1.84			
Gate Resistance	R _G		12		Ω	

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

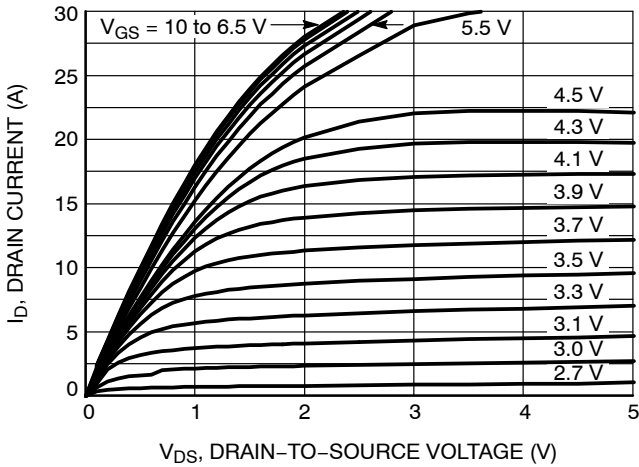


Figure 1. On-Region Characteristics

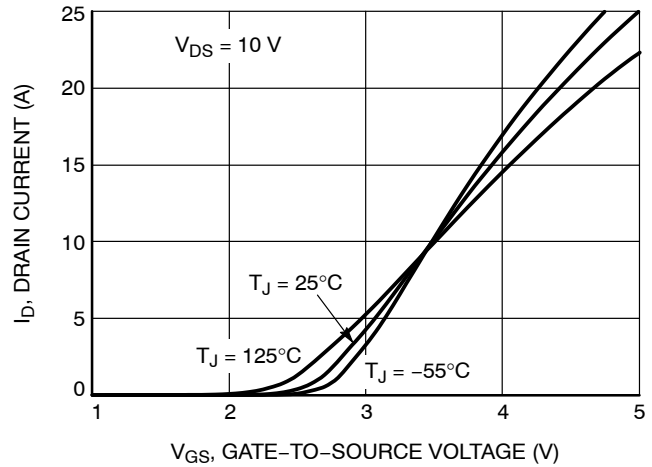


Figure 2. Transfer Characteristics

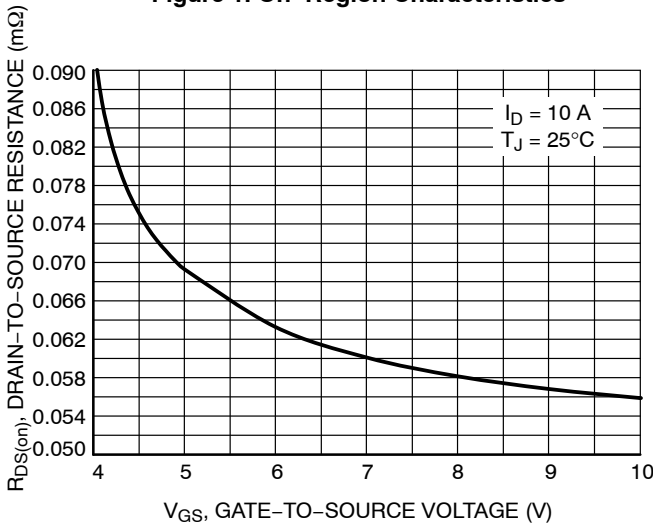


Figure 3. On-Resistance vs. V_{GS}

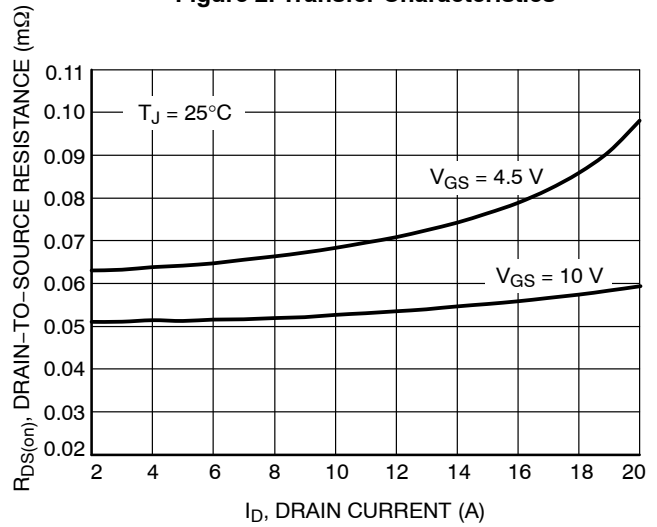


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

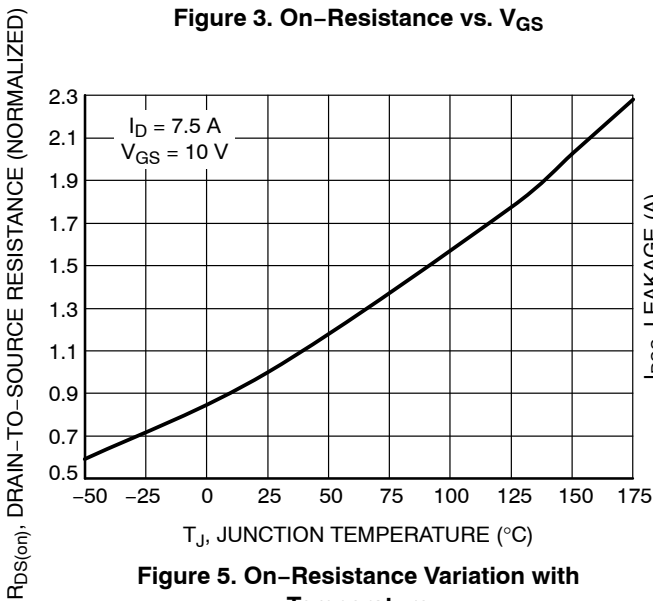


Figure 5. On-Resistance Variation with Temperature

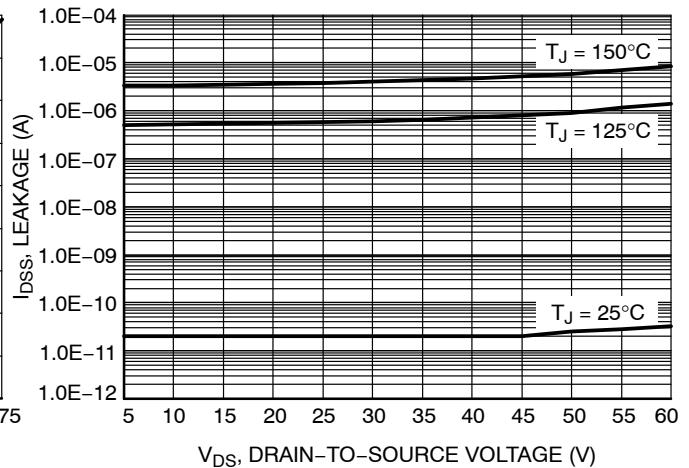


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

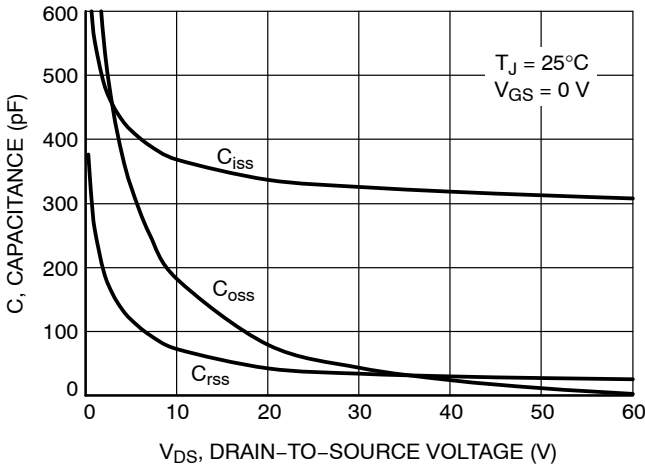


Figure 7. Capacitance Variation

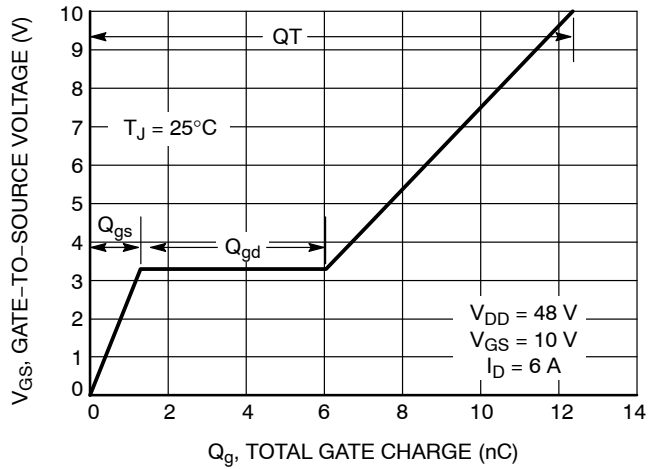


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

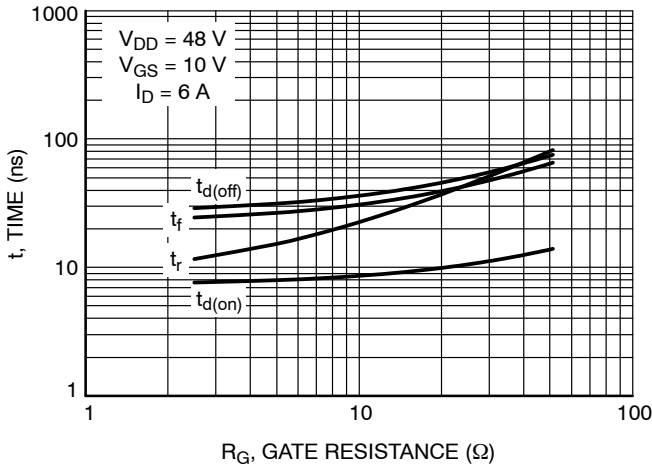


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

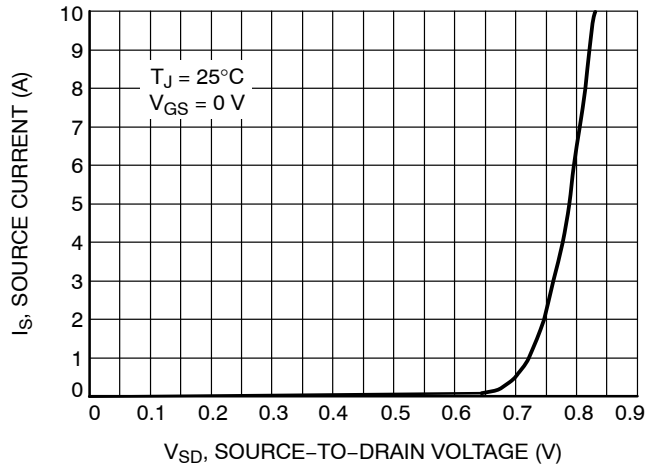


Figure 10. Diode Forward Voltage vs. Current

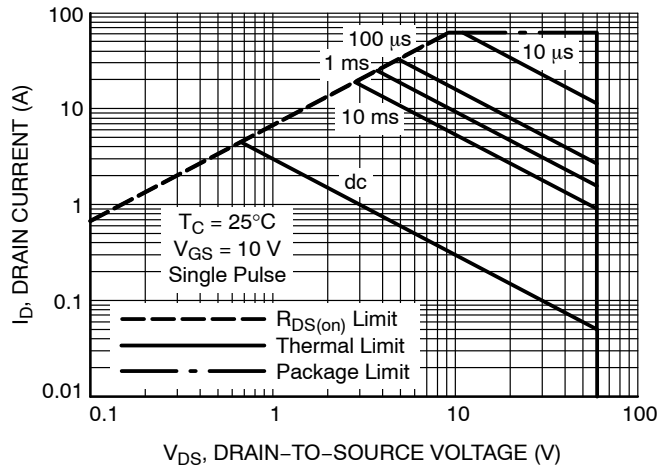


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

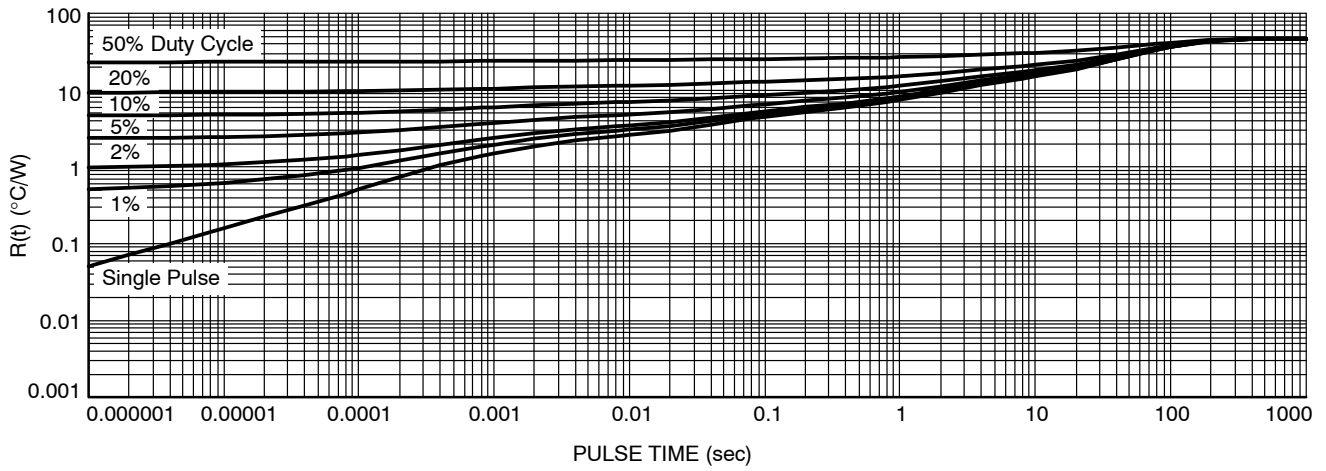


Figure 12. Thermal Response

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