

MOSFET – Power, Single, N-Channel, DFN5/DFNW5

40 V, 1.3 mΩ, 235 A

NVMFS5C426N

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C426NWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit	
V_{DSS}	Drain-to-Source Voltage	40	V	
V_{GS}	Gate-to-Source Voltage	± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State $T_C = 25^\circ\text{C}$	235	A
		$T_C = 100^\circ\text{C}$	166	
		$T_C = 25^\circ\text{C}$	128	W
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 100^\circ\text{C}$	64	
		$T_A = 25^\circ\text{C}$	41	A
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State $T_A = 25^\circ\text{C}$	41	A
		$T_A = 100^\circ\text{C}$	29	
		$T_A = 25^\circ\text{C}$	3.8	W
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	$T_A = 100^\circ\text{C}$	1.9	
		$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	900	A
I_{DM}	Pulsed Drain Current			
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$	
I_S	Source Current (Body Diode)	122	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 19 \text{ A}$)	739	mJ	
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$	

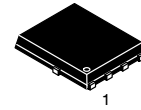
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

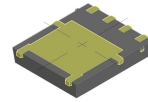
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	1.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

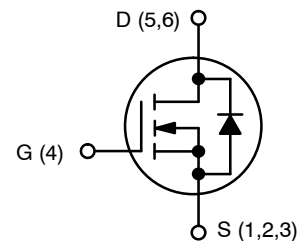
$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	1.3 mΩ @ 10 V	235 A



DFN5 (SO-8FL)
CASE 488AA

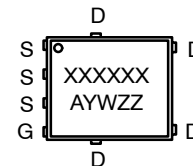


DFNW5
(FULL-CUT SO8FL WF)
CASE 507BA



N-CHANNEL MOSFET

MARKING DIAGRAM



XXXXXX = 5C426N
(NVMFS5C426N) or
426NWF
(NVMFS5C426NWF)
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

NVMFS5C426N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
V _{(BR)DSS} /T _J	Drain-to-Source Breakdown Voltage Temperature Coefficient			9.6		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 40 V			10	μA
					100	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 170 μA	2.5		3.5	V
V _{GS(TH)} /T _J	Threshold Temperature Coefficient			-8.6		mV/°C
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 50 A		1.1	1.3	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 50 A		145		S

CHARGES, CAPACITANCES & GATE RESISTANCE

C _{ISS}	Input Capacitance	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		4300		pF
C _{OSS}	Output Capacitance			2100		
C _{RSS}	Reverse Transfer Capacitance			59		
Q _{G(TOT)}	Total Gate Charge	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 50 A		65		nC
Q _{G(TH)}	Threshold Gate Charge	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 50 A		13		
Q _{GS}	Gate-to-Source Charge			20		
Q _{GD}	Gate-to-Drain Charge			12		
V _{GP}	Plateau Voltage			4.7		V

SWITCHING CHARACTERISTICS (Note 5)

t _{d(ON)}	Turn-On Delay Time	V _{GS} = 10 V, V _{DS} = 20 V, I _D = 50 A, R _G = 2.5 Ω		15		ns
t _r	Rise Time			47		
t _{d(OFF)}	Turn-Off Delay Time			36		
t _f	Fall Time			9.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 50 A	T _J = 25°C		0.82	1.2	V
			T _J = 125°C		0.68		
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A		63		ns	
t _a	Charge Time			34			
t _b	Discharge Time			29			
Q _{RR}	Reverse Recovery Charge				92		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

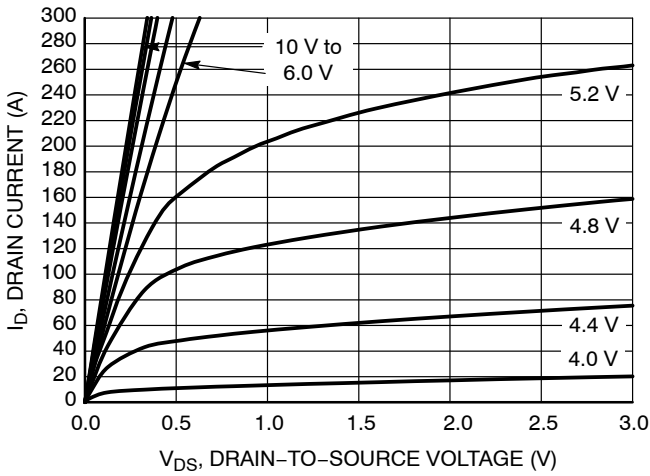


Figure 1. On-Region Characteristics

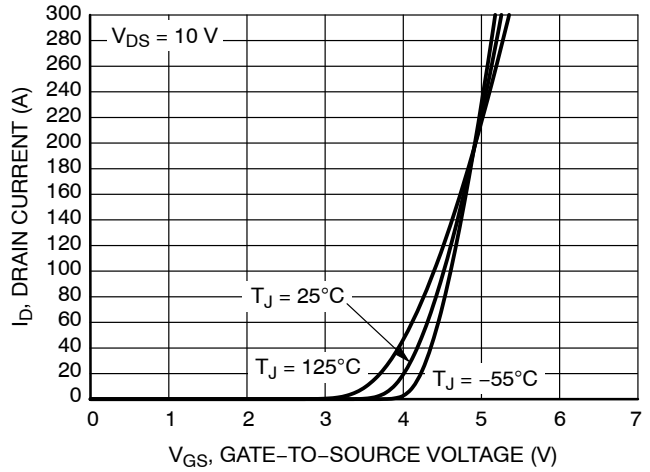


Figure 2. Transfer Characteristics

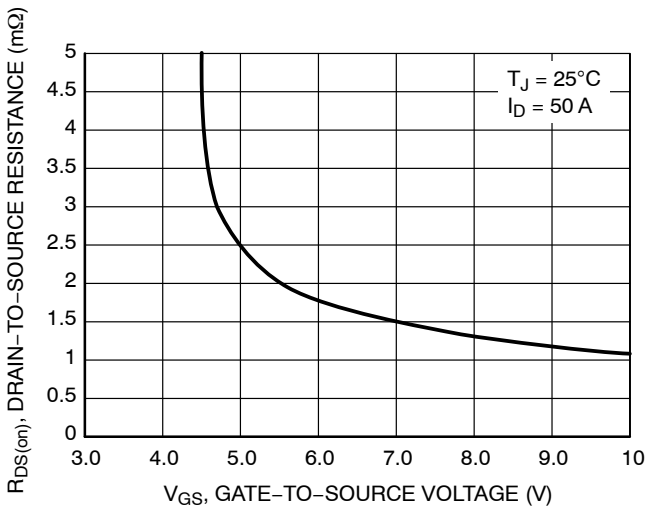


Figure 3. On-Resistance vs. Gate-to-Source Voltage

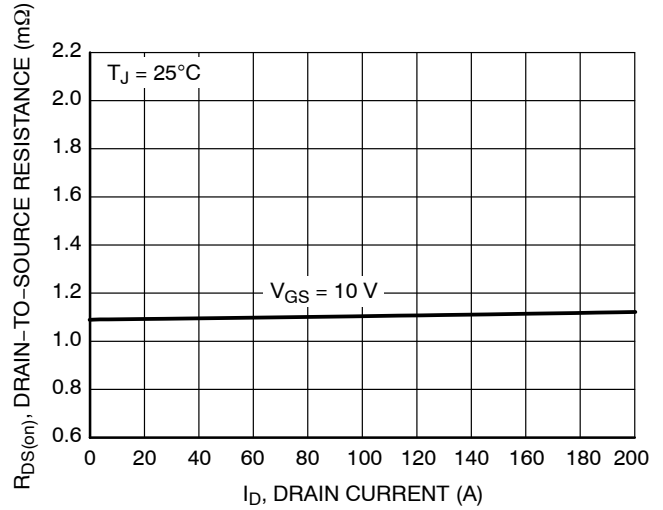


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

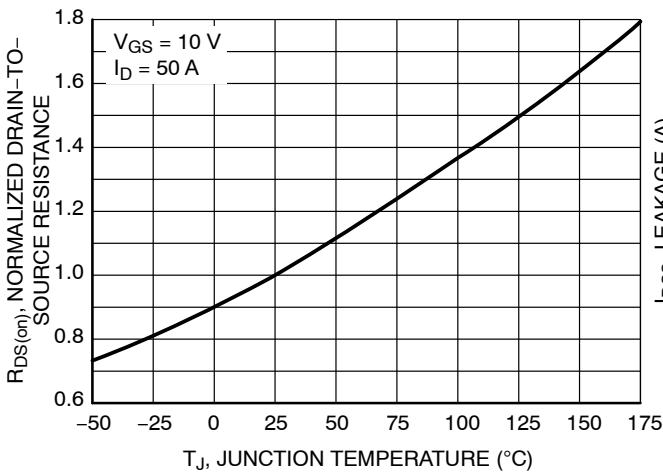


Figure 5. On-Resistance Variation with Temperature

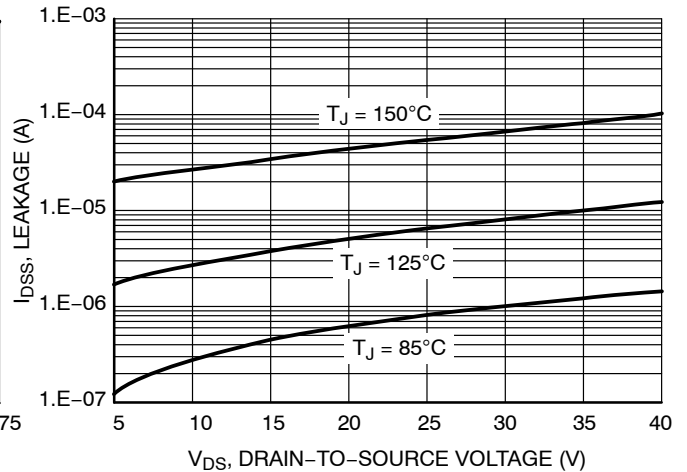


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

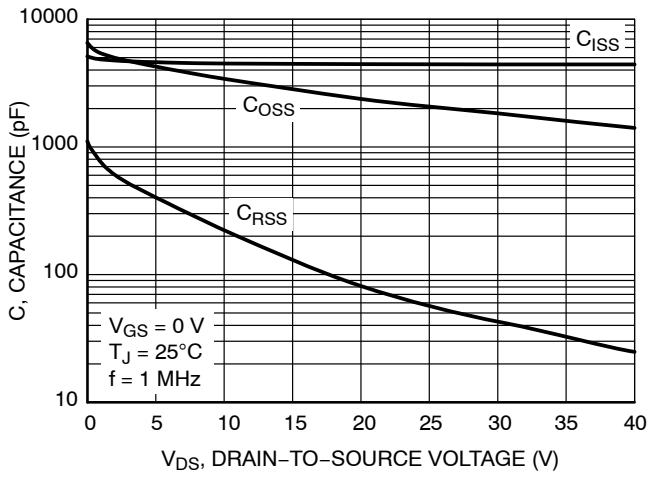


Figure 7. Capacitance Variation

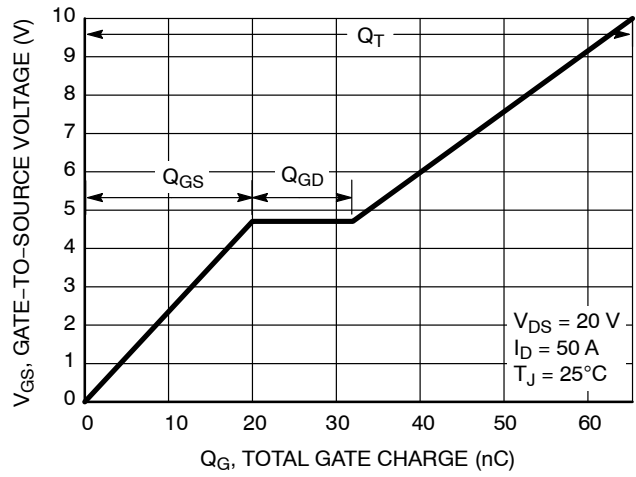


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

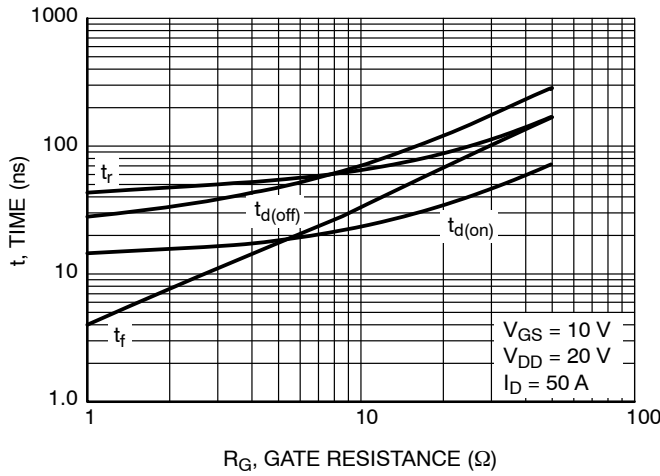


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

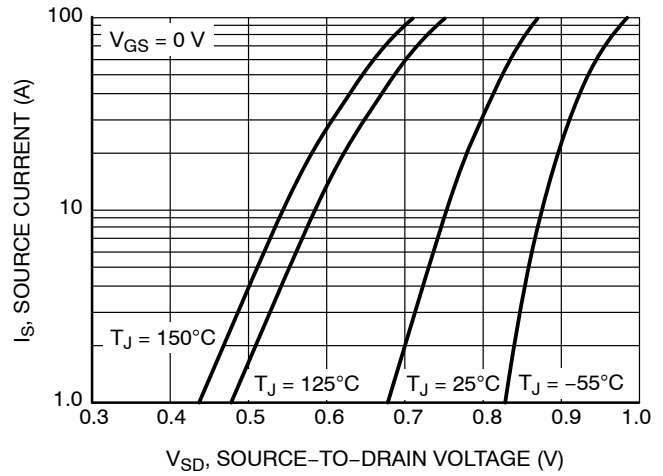


Figure 10. Diode Forward Voltage vs. Current

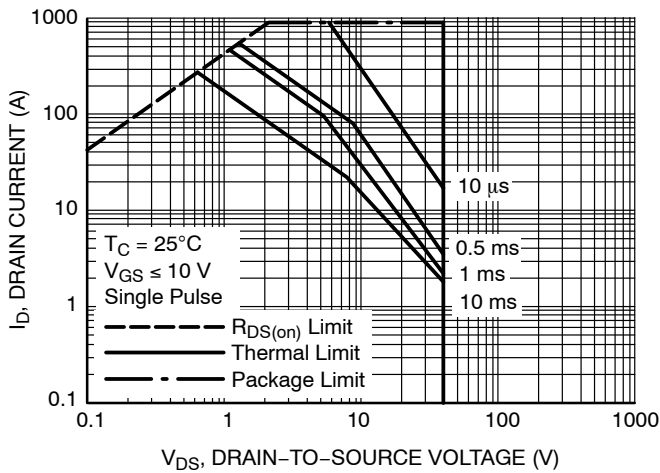


Figure 11. Safe Operating Area

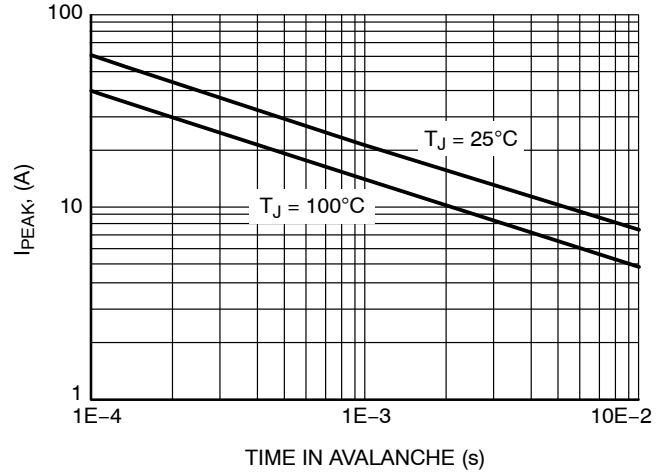


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFS5C426N

TYPICAL CHARACTERISTICS (continued)

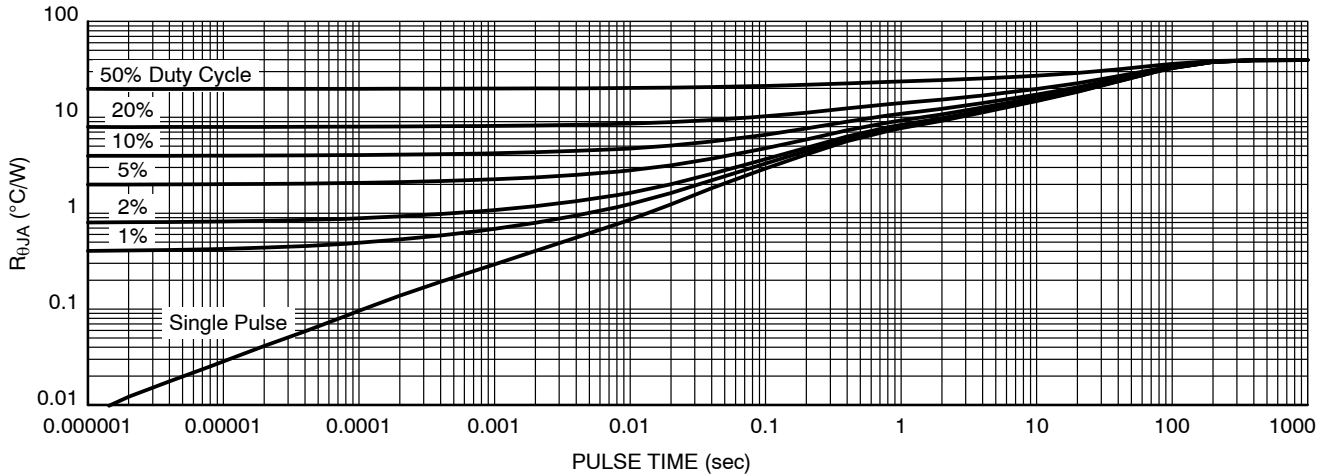


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

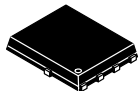
Device	Marking	Package	Shipping [†]
NVMFS5C426NT1G	5C426N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C426NET1G	5C426N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C426NET1G-YE	5C426N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C426NAFT1G	5C426N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C426NAFT1G-YE	5C426N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C426NWF1G	426NWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C426NWFET1G	426NWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

DISCONTINUED (Note 6)

NVMFS5C426NWF1G	426NWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C426NT3G	5C426N	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C426NWF3G	426NWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

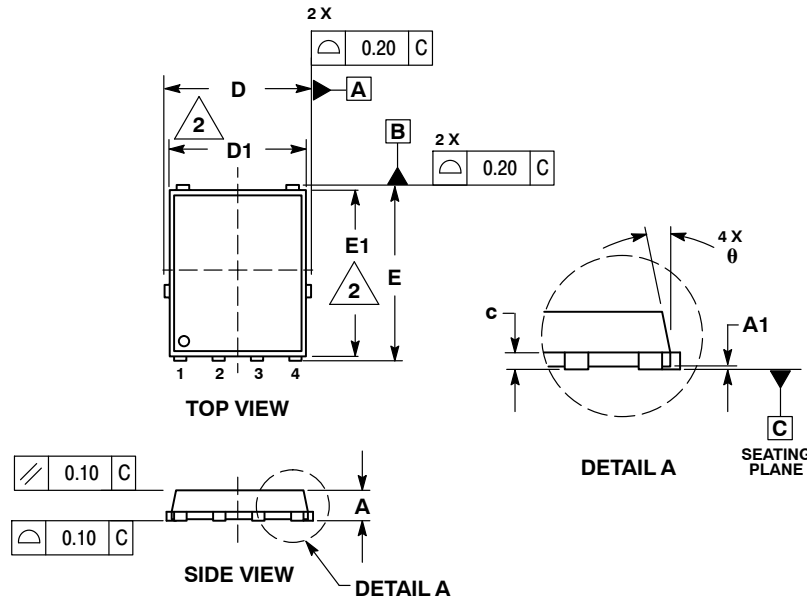
6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

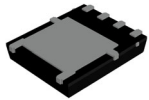


- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

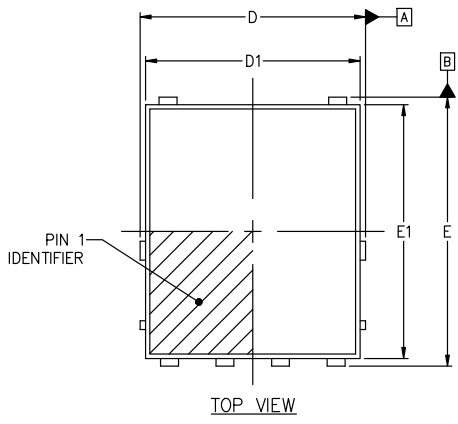
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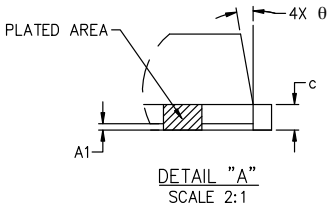


**DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C**

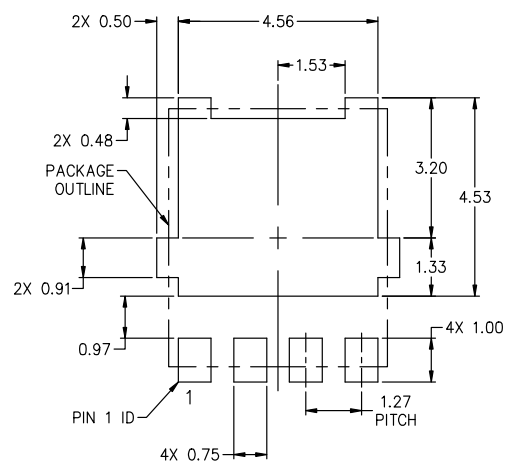
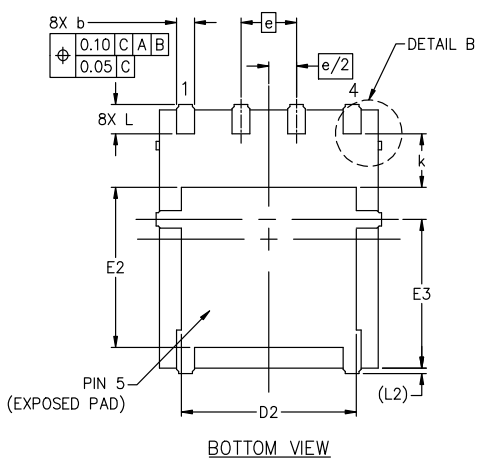
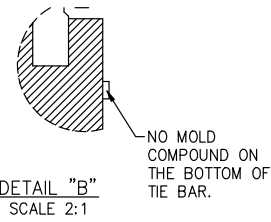
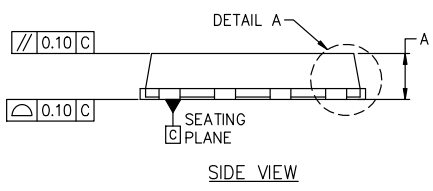
DATE 19 SEP 2024



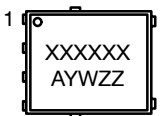
- NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
 2. ALL DIMENSIONS ARE IN MILLIMETERS.
 3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
theta	0°	6°	12°



GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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