

MOSFET – Power, Single N-Channel

60 V, 0.68 mΩ, 477 A

NVMTS0D7N06CL

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Power 88 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- Wettable Flank Option for Enhanced Optical Inspection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter		Value	Unit	
V _{DSS}	Drain-to-Source Voltage		60	V	
V _{GS}	Gate-to-Source Voltage		±20	V	
I _D	Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25 °C	477	A
			T _C = 100 °C	337.6	
P _D	Power Dissipation R _{θJC} (Note 1)		T _C = 25 °C	294.6	W
			T _C = 100 °C	147.3	
I _D	Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25 °C	62.2	A
			T _A = 100 °C	44.0	
P _D	Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25 °C	5.0	W
			T _A = 100 °C	2.5	
I _{DM}	Pulsed Drain Current	T _A = 25 °C, t _p = 10 µs	900	A	
T _J , T _{stg}	Operating Junction and Storage Temperature Range		-55 to +175	°C	
I _S	Source Current (Body Diode)		245.5	A	
E _{AS}	Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 40 A)		1754	mJ	
T _L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	°C	

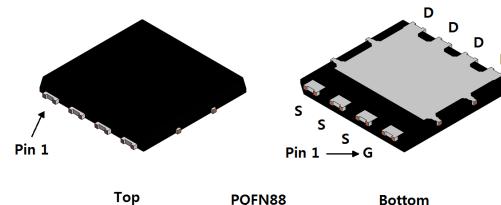
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

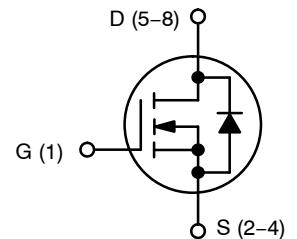
Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	R _{θJC}	0.5	°C/W
Junction-to-Ambient - Steady State (Note 2)	R _{θJA}	30	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V _{(BR)DSS}	R _{DS(ON) MAX}	I _D MAX
60 V	0.68 mΩ @ 10 V	477 A
	0.90 mΩ @ 4.5 V	

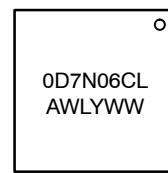


DFNW8
CASE 507AP



N-CHANNEL MOSFET

MARKING DIAGRAM



A = Assembly Location

WL = Wafer Lot Code

Y = Year Code

WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMTS0D7N06CL

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA		60	—	—	V
V _{(BR)DSS/T_J}	Drain-to-Source Breakdown Voltage Temperature Coefficient	I _D = 250 μA, ref to 25 °C		—	16.8	—	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25 °C	—	—	10	μA
			T _J = 125 °C	—	—	250	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V		—	—	100	nA

ON CHARACTERISTICS (Note 4)

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA		1.0	—	2.5	V
V _{GS(TH)/T_J}	Threshold Temperature Coefficient	I _D = 250 μA, ref to 25 °C		—	-5.63	—	mV/°C
R _{D(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V	I _D = 50 A	—	0.52	0.68	mΩ
		V _{GS} = 4.5 V	I _D = 50 A	—	0.69	0.90	
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 50 A		—	310	—	S

CHARGES, CAPACITANCES & GATE RESISTANCE

C _{ISS}	Input Capacitance	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V	—	1620	—	pF
C _{OSS}	Output Capacitance		—	8490	—	
C _{RSS}	Reverse Transfer Capacitance		—	270	—	
Q _{G(TOT)}	Total Gate Charge	V _{GS} = 4.5 V, V _{DS} = 30 V; I _D = 50 A	—	103	—	nC
Q _{G(TOT)}	Total Gate Charge		—	225	—	
Q _{G(TH)}	Threshold Gate Charge		—	21.6	—	
Q _{GS}	Gate-to-Source Charge		—	36.5	—	
Q _{GD}	Gate-to-Drain Charge		—	20.7	—	
V _{GP}	Plateau Voltage		—	2.46	—	V

SWITCHING CHARACTERISTICS (Note 5)

t _{d(ON)}	Turn-On Delay Time	V _{GS} = 10 V, V _{DS} = 30 V, I _D = 50 A, R _G = 2.5 Ω	—	35.3	—	ns
t _r	Rise Time		—	26.3	—	
t _{d(OFF)}	Turn-Off Delay Time		—	263	—	
t _f	Fall Time		—	60.7	—	

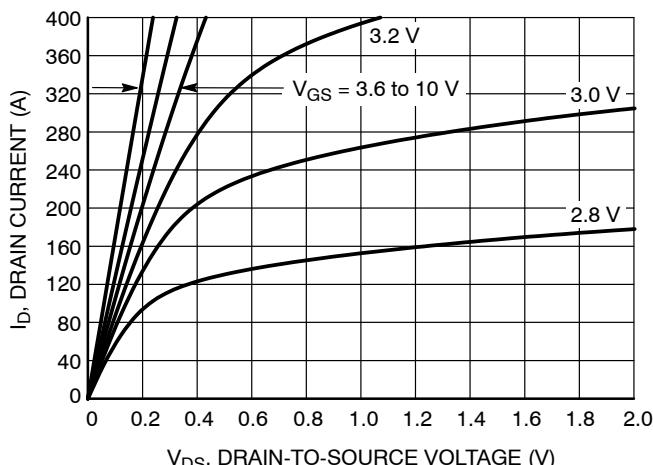
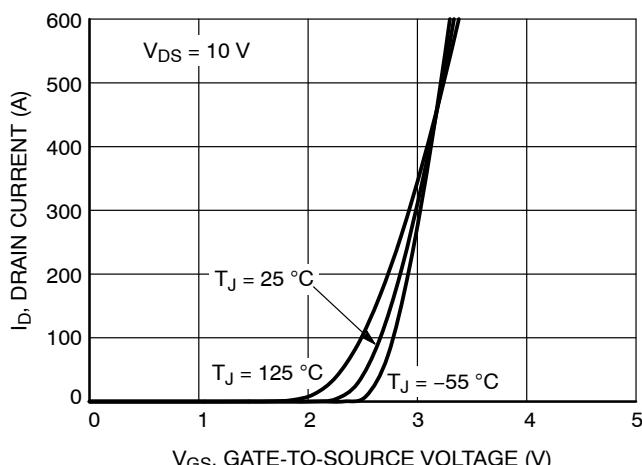
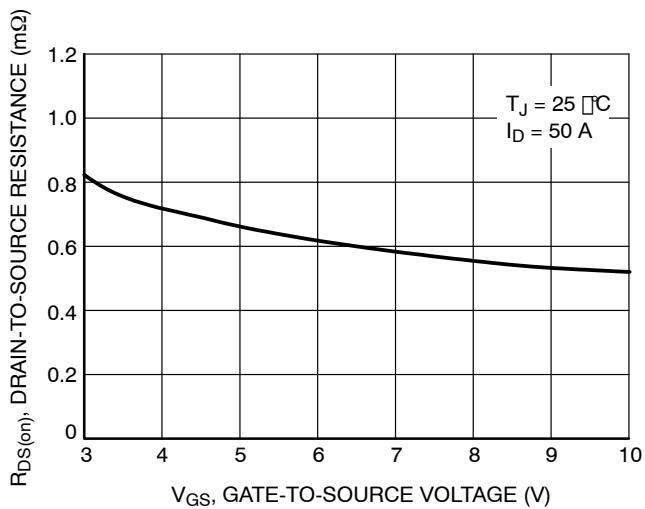
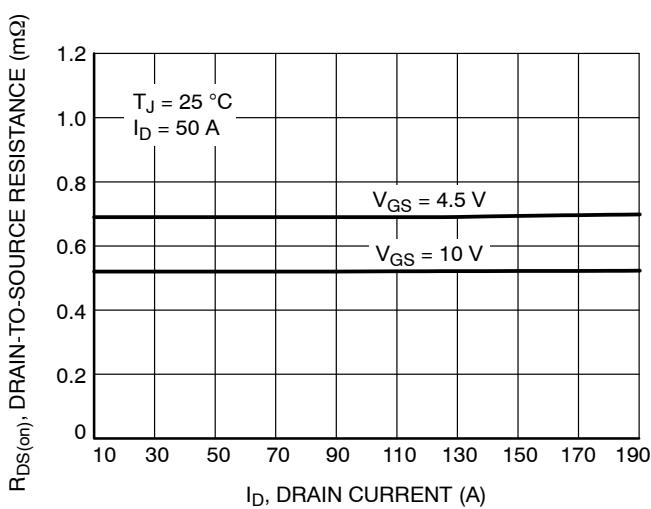
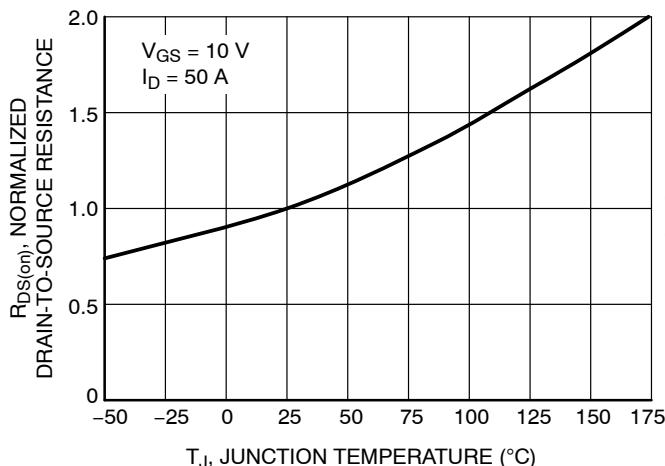
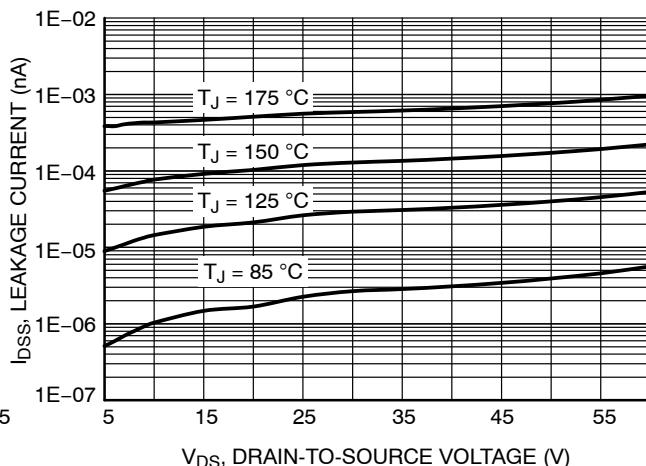
DRAIN-SOURCE DIODE CHARACTERISTICS

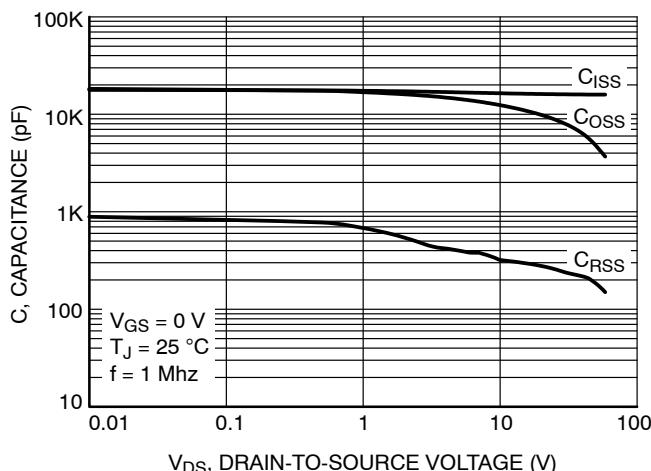
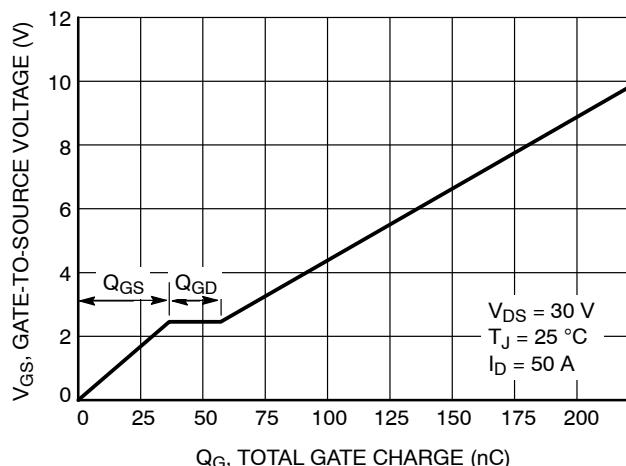
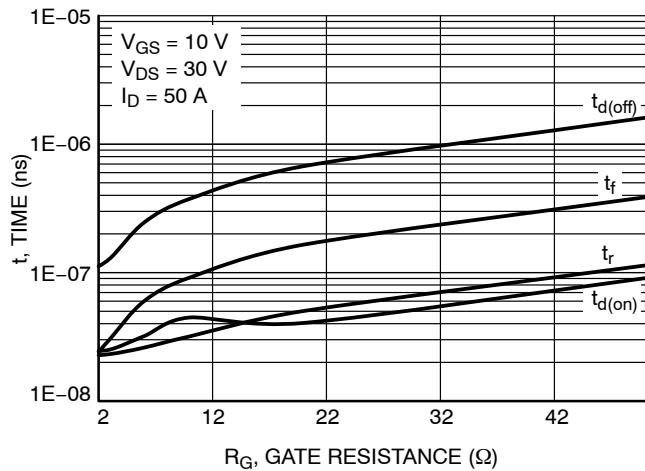
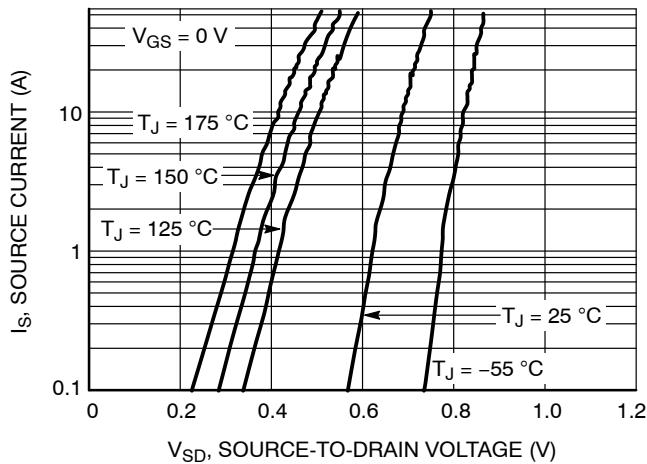
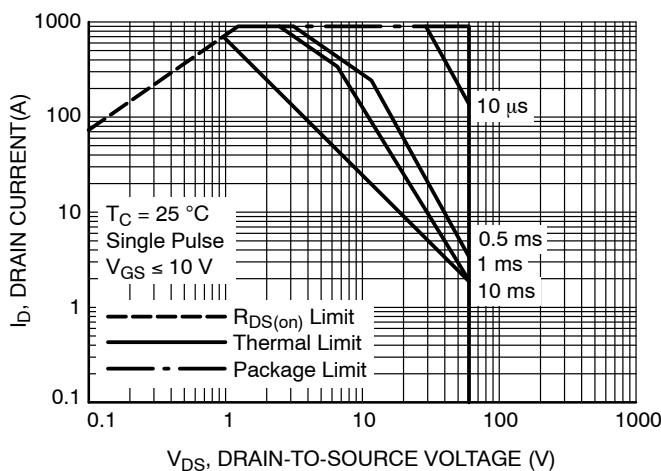
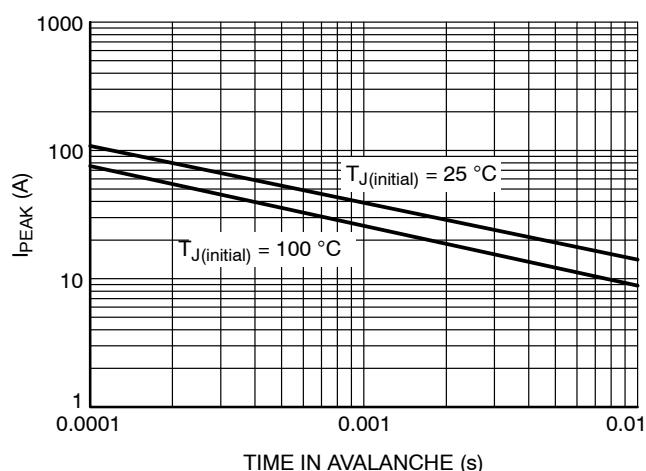
V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 50 A	T _J = 25 °C	—	0.67	1.2	V
			T _J = 125 °C	—	0.59	—	
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A	—	115	—	ns	
			—	70	—		
			—	45	—		
			—	307	—	nC	
t _a	Charge Time						
t _b	Discharge Time						
Q _{RR}	Reverse Recovery Charge						

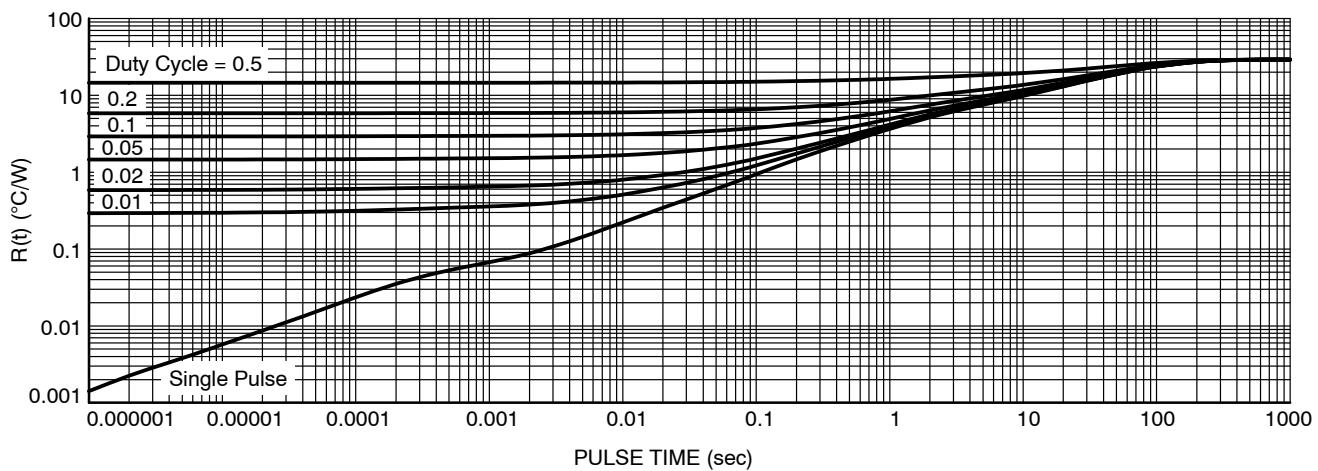
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage

Figure 5. On-Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source Voltage vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)**Figure 13. Thermal Characteristics****DEVICE ORDERING INFORMATION**

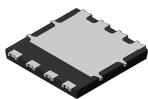
Device	Marking	Package	Shipping [†]
NVMTS0D7N06CLTXG	0D7N06CL	DFNW8 (Pb-Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

REVISION HISTORY

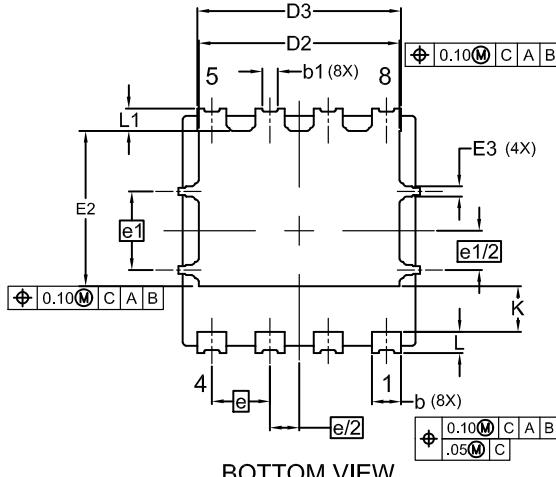
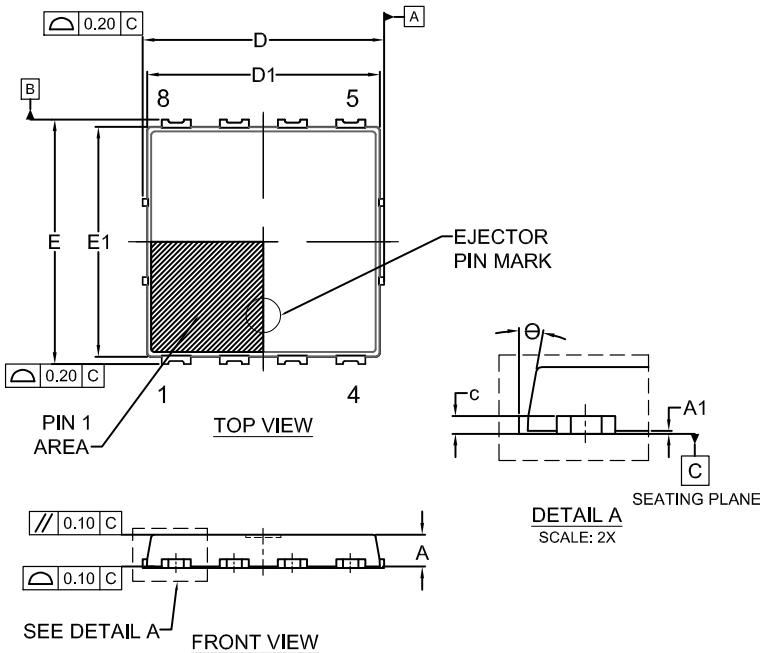
Revision	Description of Changes	Date
4	Rebranded the Data Sheet to onsemi format.	01/23/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

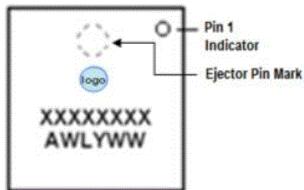


TDFNW8 8.30x8.40x1.10, 2.00P
CASE 507AP
ISSUE E

DATE 08 MAY 2024



**GENERIC
MARKING DIAGRAM***



XXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot Code

Y = Year Code

WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TDFNW8 8.30x8.40x1.10, 2.00P	PAGE 2 OF 2

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