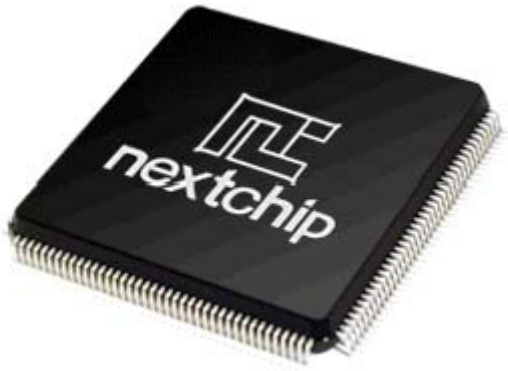
NVP1114A

4-Ch Video Decoder with 4-Ch Audio Codec, Video Encoder.



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4 Channel Video Decoder with 4-Ch Audio Codec, Video Encoder

: NVP1114A includes 4 Channel Video Decoder, 1 Channel Video Encoder and 4 Channel Audio Codec.

4 Channel Video Decoder delivers high quality images. It accepts separate 4 CVBS inputs from Camera, TV, VCR and the other video signal sources. It digitizes and decodes NTSC/PAL video signal into digital components video which represents 8-bit CCIR656 4:2:2 format with 27MHz, 54MHz and 108MHz multiplexed. **1 Channel Video Encoder** plays the roles of converting the digital ITU-R BT.656 format data into CVBS, Y and C in 10bit resolution. And there is 2-Ch DAC which is fed from the above video encoder. **4 Channel Audio Codec** has four ADC and one DAC. Built-in voice controller can generate digital outputs for recording/mixing and accepts digital input for playback.

Features

Video Decoder

-. 4-Ch Video Decoder which accepts 4-CVBS
-. Output in CCIR656 4:2:2 format with 27/54/108MHz
-. On Chip Analog CLAMP/AGC and Anti-aliasing Filter
-. Accepts NTSC-M/J/4.43, PAL-M/N/B/D/G/H/I/60
-. Robust Sync detection for weak, non-standard signal
-. High-performance 3H/5H 2D adaptive comb filter
-. White Peak Detection & Peak AGC
-. Programmable peaking filter for Luminance
-. Vertical Peaking filter
-. CTI (Chrominance Transient Improvement)
-. Color compensation for PAL
-. IF compensation filter
-. Robust No-video detection
-. Programmable brightness, contrast, saturation and hue
-. Motion Detection

Video Encoder

-. Supports NTSC/PAL
-. 2 Analog outputs
: 2*10bits DAC for generating 2*CVBS or S-Video(Y/C)
-. Supports Internal Color Bar Pattern Generator

Audio Codec

-. 4-Ch Voice Record, 1-Ch Playback
-. ΔΣ Modulator/Demodulator for ADC & DAC
-. Input/Output Analog Gain Control
-. 4 Channel PCM Voice Codec
: Linear PCM (8bits/16bits, 8K/16K)
: G.711 A-law/u-law (8bits, 8K/16K)
-. Input Mixing, Digital Volume, Mute Detection
-. I2S/SSP/DSP Interface (Master/Slave mode)
-. Cascade mode (up to 4 cascade support)

Applications

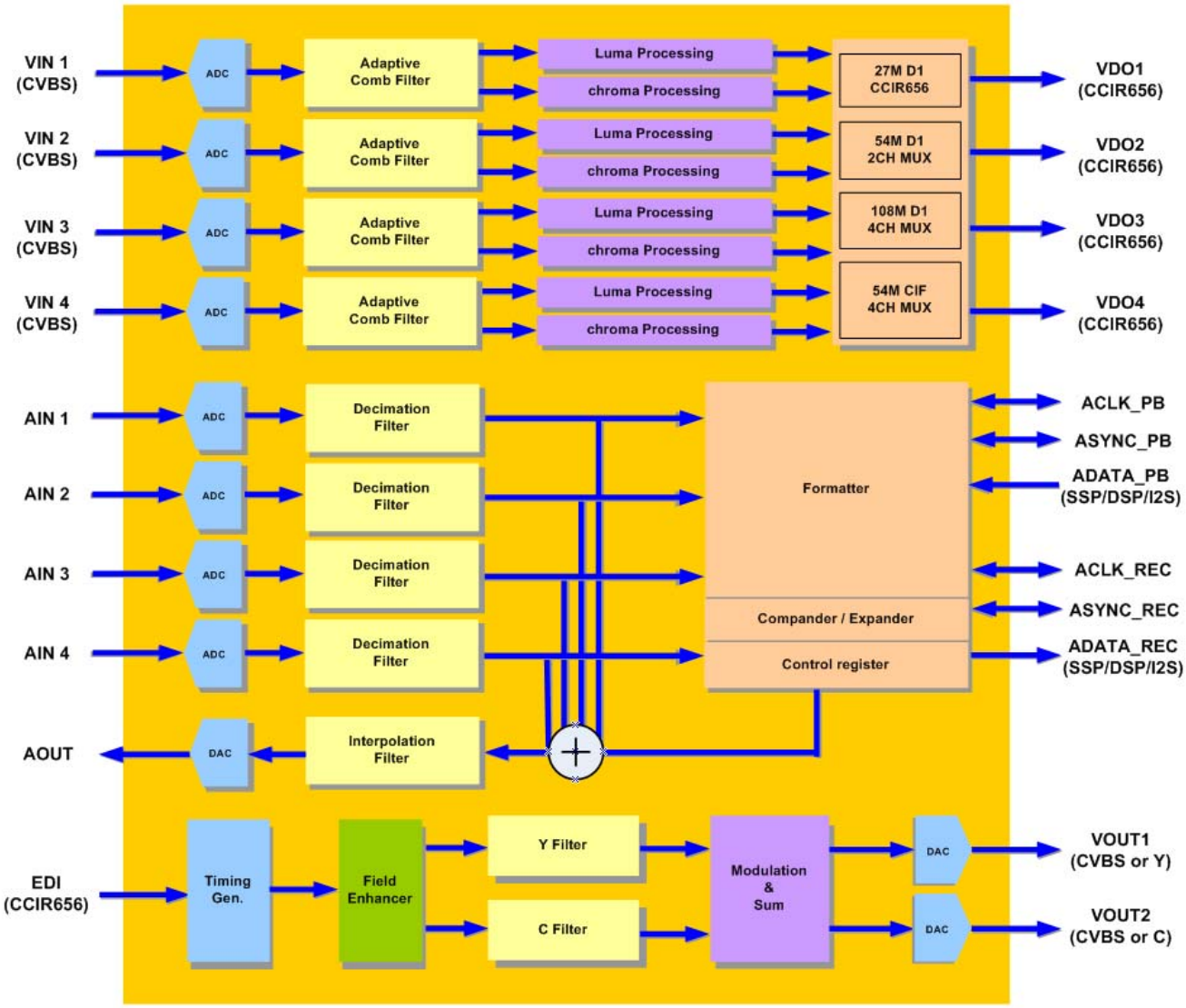
-. Video Security System

Related Products

-. NVS2200F
-. NVS3211
-. NVC1001
-. NVC1300/NVC1301
-. NVC1400/NVC1401
-. NVP3000
-. NVC1600

Ordering Information

Device	Package	Temperature Range
NVP1114A	128TQFP	-10 ~ 80℃


VIN 1 (CVBS)
VIN 2 (CVBS)
VIN 3 (CVBS)
VIN 4 (CVBS)
ADC
Adaptive Comb Filter
Luma Processing
chroma Processing
27M D1 CCIR656
54M D1 2CH MUX
108M D1 4CH MUX
54M CIF 4CH MUX
VDO1 (CCIR656)
VDO2 (CCIR656)
VDO3 (CCIR656)
VDO4 (CCIR656)
AIN 1
AIN 2
AIN 3
AIN 4
Decimation Filter
Formatter
Compander / Expander
Control register
ACLK_PB
ASYNC_PB
ADATA_PB (SSP/DSP/I2S)
ACLK_REC
ASYNC_REC
ADATA_REC (SSP/DSP/I2S)
AOUT
DAC
Interpolation Filter
EDI (CCIR656)
Timing Gen.
Field Enhancer
Y Filter
C Filter
Modulation & Sum
VOUT1 (CVBS or Y)
VOUT2 (CVBS or C)

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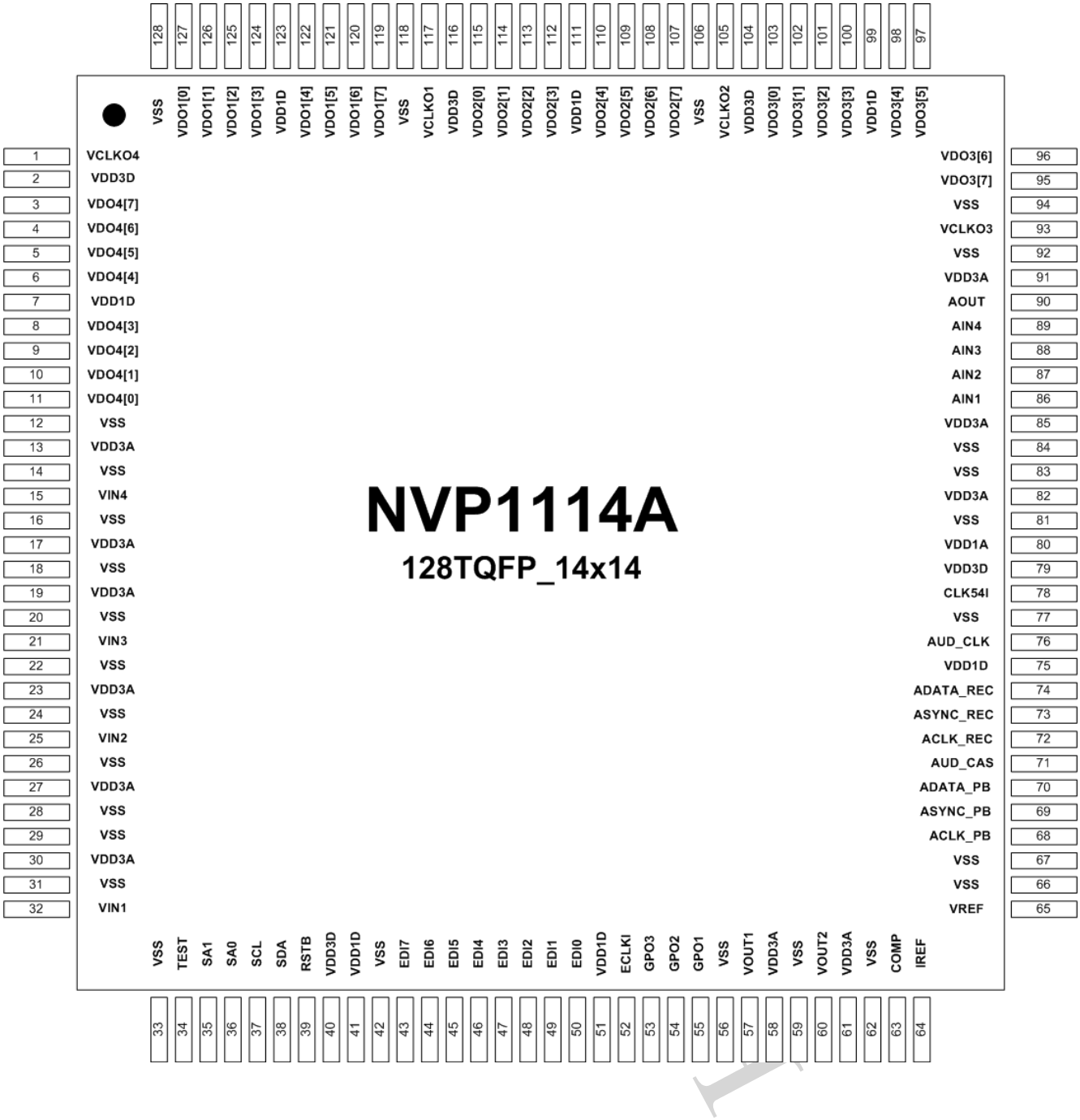
1. Pin Information

1.1. Pin Assignments



1.2. Pin Description

Pin name	Number	Type	Description
Video Interface			
CLK54I	78	I	Video decoder clock input.(54MHz)
VIN1, VIN2, VIN3, VIN4	32,25,21,15	I	Analog Video Input (1,2,3,4 Respectively)
VCLK01	117	O	Channel 1, Output Clock (27/54/108MHz)
VD01[7:0]	119,120,121,122,124,125,126,127	O	Channel 1, Output Data
VCLK02	105	O	Channel 2, Output Clock (27/54/108MHz)
VD02[7:0]	107,108,109,110,112,113,114,115	O	Channel 2, Output Data
VCLK03	93	O	Channel 3, Output Clock (27/54/108MHz)
VD03[7:0]	95,96,97,98,100,101,102,103	O	Channel 3, Output Data
VCLK04	1	O	Channel 4, Output Clock (27/54/108MHz)
VD04[7:0]	3,4,5,6,8,9,10,11	O	Channel 4, Output Data
ECLKI	52	I	Video Encoder Clock
EDI[7:0]	43,44,45,46,47,48,49,50	I	Video Encoder Data
VOUT1,VOUT2	57,60	O	Video Encoder Analog Output
COMP,IREF,VREF	63,64,65	-	Video Encoder Analog Reference
Audio Interface			
AUD_CLK	76	I	Audio Clock
AIN1, AIN2, AIN3, AIN4	86,87,88,89	I	Analog Audio Input (1,2,3,4 Respectively)
ACLK_REC	72	I/O	Clock for Record (M:Output, S:Input)
ASYNC_REC	73	I/O	Sync for Record (M:Output, S:Input)
ADATA_REC	74	O	Audio Digital Data for Record
AUD_CAS	71	I	Audio Digital Data for Cascade
ACLK_PB	68	I/O	Clock for Playback (M:Output,S:Input)
ASYNC_PB	69	I/O	Sync for Playback (M:Output,S:Input)
ADATA_PB	70	I	Audio Digital Data for Playback
AOUT	90	O	Audio Analog Output
I2C Interface			
SDA	38	I	I2C interface clock. (5V tolerant)
SCL	37	I/O	I2C interface R/W data. (5V tolerant)
SA1, SA0	35,36	I	Slave addresses. (5V tolerant)
ETC			
RSTB	39	I	System reset pin.
TEST	34	I	Test Pin.
GP01,GP02,GP03	55,54,53	O	Video loss, Motion, Mute, Alarm output
Power / Ground			
VSS	12,14,16,18,20,22,24,26,28, 29,31,33,42,56,59,62,66,67, 77,81,83,84,92,94,106,118,128	I	Ground
VDD3D	2,40,79,104,116	I	Digital Power (Digital 3.3V)
VDD1D	7,41,51,75,99,111,123	I	Digital Power (Digital 1.8V)
VDD3A	13,17,19,23,27,30,58,61,82,85,91	I	Analog Power (Analog 3.3V)
VDD1A	80	I	Analog Power (Analog 1.8V)
NVP1114A 128TQFP_14x14			

2. Video Decoder

: NVP1114A is Four Channel Video Decoder and delivers high quality images. It accepts separate 4 CVBS inputs from Camera, TV or VCR and so on. It digitizes and decodes NTSC/PAL video formats into digital components video which represents 8-bit CCIR656 4:2:2 format with 27MHz, 54MHz and 108MHz multiplexed.

: NVP1114A includes 4 channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. It shows the best picture quality adopted by high performance 2D adaptive comb filter and vertical peaking filter. It also support programmable Saturation, Hue, Brightness and Contrast and several function such as CTI, Programmable peaking filter, PAL compensation, IF compensation filter and White Peak Detect.

2.1. Functional Overview

: The role of video decoder is to separate luminance and chrominance signals from composite video signal. Fig 2.1 show the block diagram of the NVP1114A

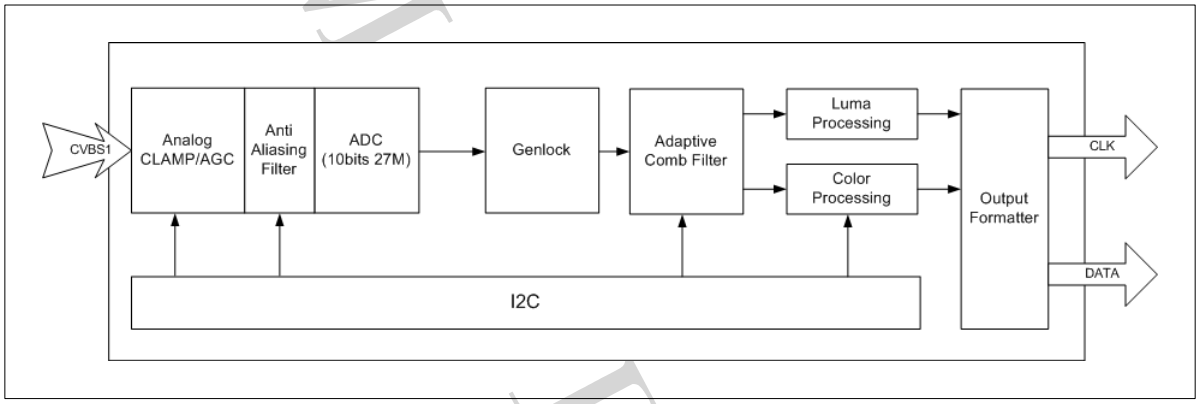


Figure 2.1. Video Decoder Data Flow of NVP1114A

The First step to decode composite video signals is to digitize the entire composite video signal using an A/D converter (ADC). NVP1114A uses the 10-bit ADC whose frequency is 27MHz. Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic. The video signal also is lowpass filtered to about 9MHz in Anti aliasing Filter to remove any high-frequency components that may result in aliasing.

Vertical sync and horizontal sync information are recovered in Genlock block. When composite video signal is decoded, the luminance and chrominance are separated by Adaptive Comb Filter. The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, 2D Adaptive Comb Filter is used.

The chrominance demodulator in color processing block accepts modulated chrominance data from Adaptive Comb Filter which generate Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sin and cos subcarrier data.

2.2. Video Input Formats

: NVP1114A supports all NTSC/PAL Video Standard. Table 2.1 show NTSC/PAL Video Standards and Register Setting Value (VIDEO FORMAT, BANK0, 0x20/30/40/50[4:0]) to support them.

VIDEO_FORMAT	FORMAT	LINE	HZ	Fsc(MHz)
0x00	NTSC-M,J	525	60	3.579545
0x11	NTSC-4.43	525	60	4.43361875
0x1D	PAL-B,D,G,H,I	625	50	4.43361875
0x16	PAL-M	525	60	3.57561149
0x1F	PAL-Nc	625	50	3.58205625
0x15	PAL-60	525	60	4.433619
% Don't use auto-detect mode in case of NRT (Non Real Time) operation				

Table 2.1. NVP1114A Input Video Image Formats

2.3. Analog Front End (CLAMP, AGC, Anti-aliasing Filter)

: NVP1114A includes 4 channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. Because its design is dedicated for video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for NVP1114A. Fig 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by Register (AFE_FIR_MODE, BANK0 0x61[0])

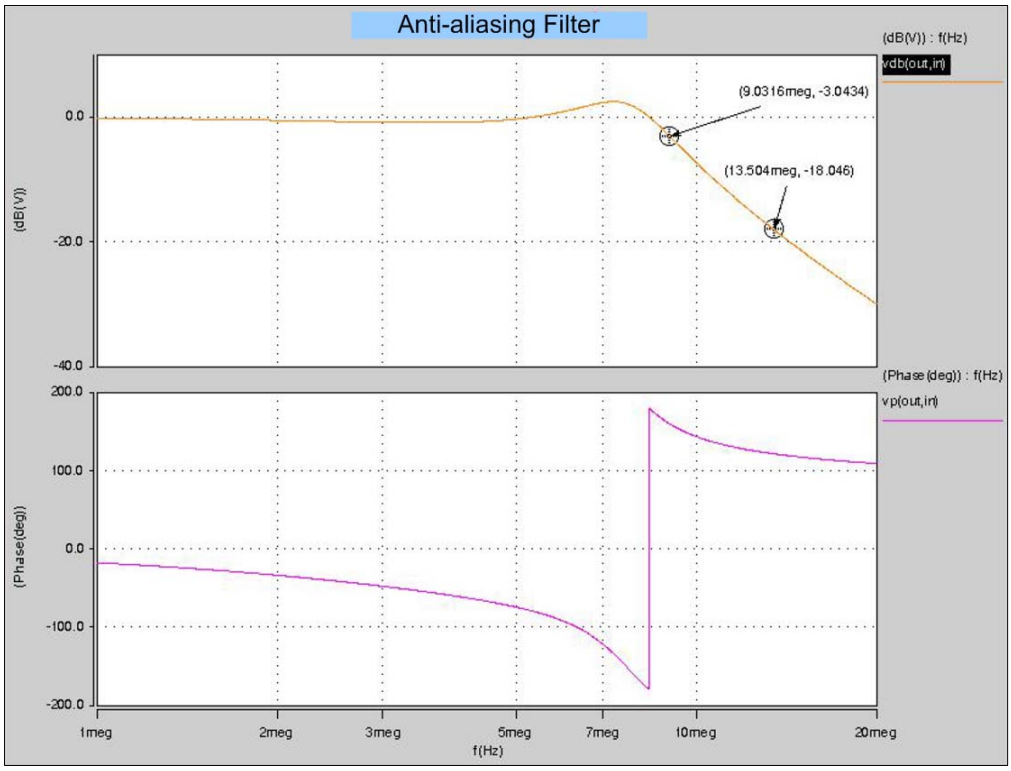


Figure 2.2 Anti-aliasing Filter characteristic

2.4. Genlock (Robust Sync Detection, Robust No-Video Detection)

: NVP1114A provides a fully digital GenLocking circuitry. The digital Genlocking Circuitry use the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier. NVP1114A uses the proprietary Genlock mechanism for video application system. That supports very Robust Sync Detection & Robust No-Video Detection, and it also showed reliable operation in Non-standard signal and Weak-signal.

2.5. Y/C separation (3H/5H Adaptive Comb Filter)

: An adaptive comb filter is used to separate Y and C signal from NTSC/PAL standard video signal. Therefore, The output image is sharper and clearer compared to other video decoder. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows the Chroma BSF which is controlled by Register (BSF_MODE, BANK0, 0x20/30/40/50[7:6]).

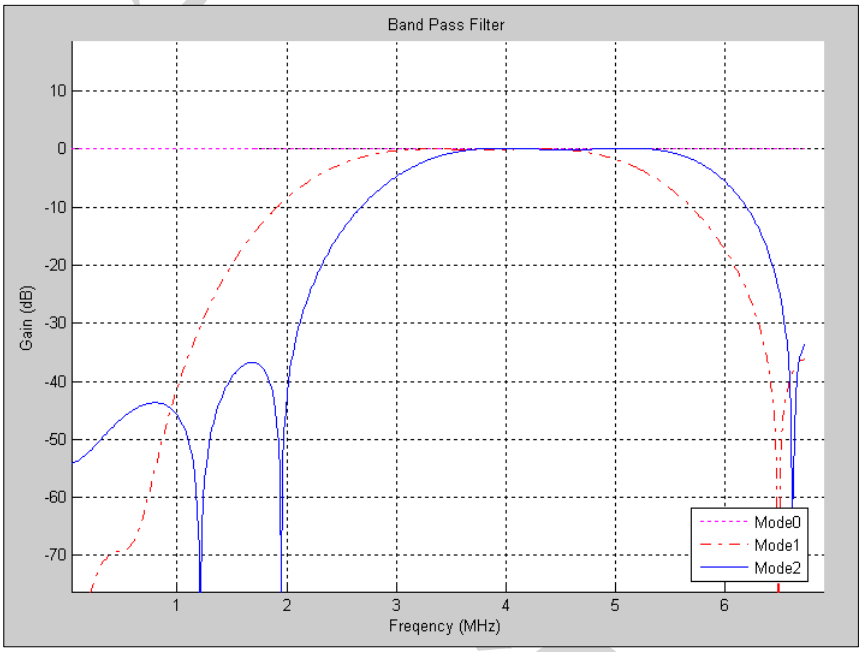


Figure 2.3. Band Split Filter Characteristic

NVP1114A can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the NVP1114A, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.6. Luma Processing

: The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

NVP1114A provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The luma filter is applied to this purpose and its characteristics can be controlled by register (Y_FIR_MODE, BANK0, 0x28/38/48/58[3:2]) via I2C interface.

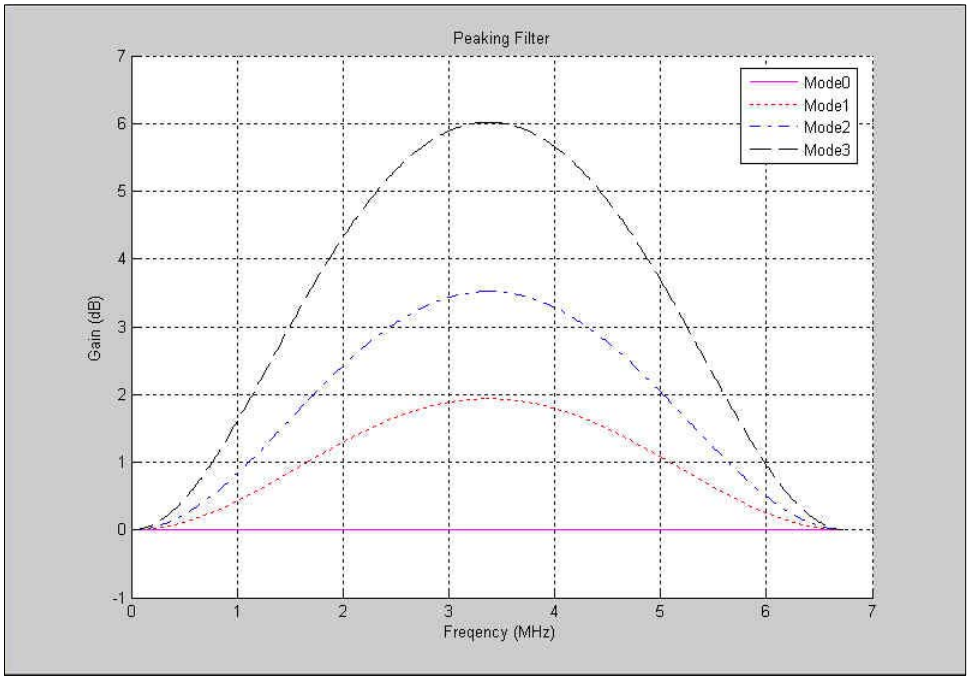


Figure 2.4. Peaking Filter Characteristic

2.7. Chroma Processing

: Chroma processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The chroma demodulator receives modulated chroma from YC separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts. Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6. Users can select the chroma filter through I2C interface (CLPF_SEL, BANK0, 0x7C[1:0]).

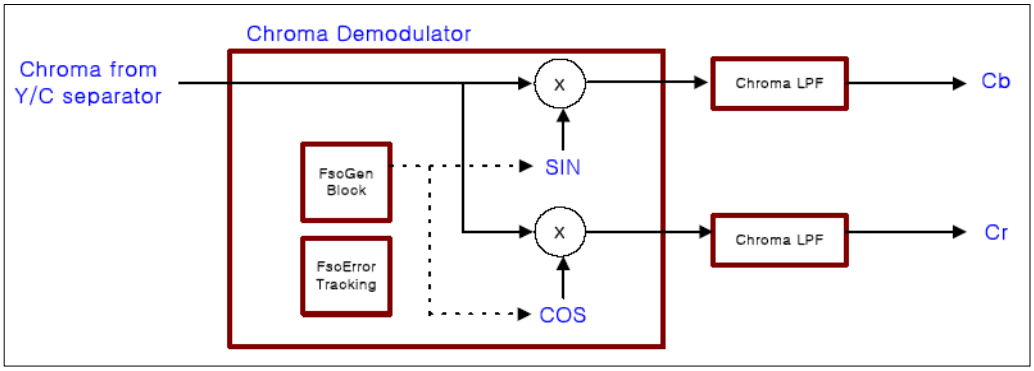


Figure 2.5. Chroma Process

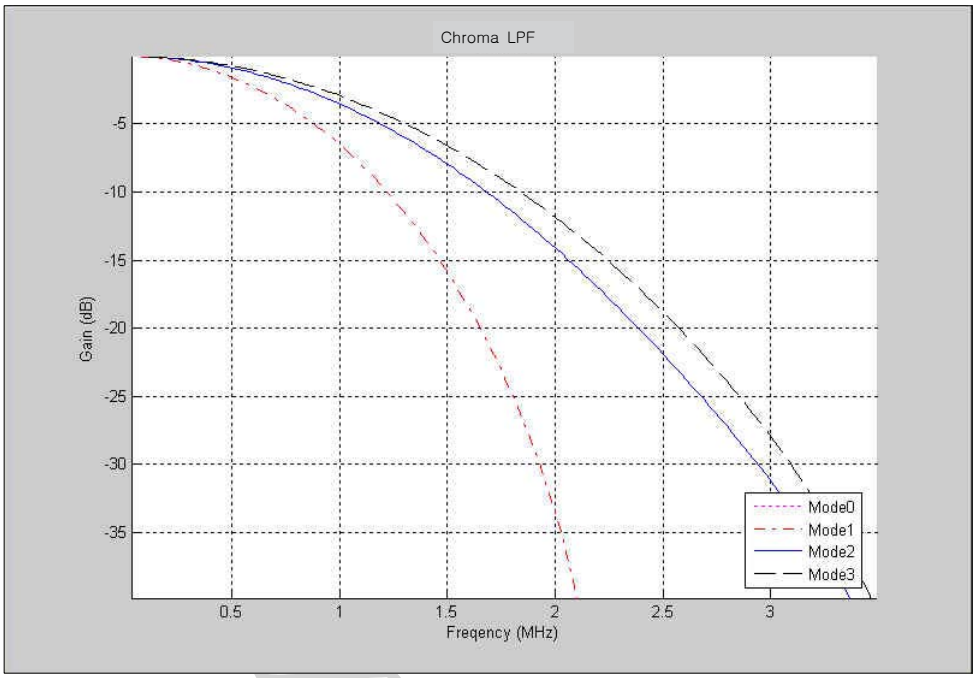


Figure 2.6. Chroma Low Pass filter Characteristic

2.8. White Peak Detector

: Out of the signals inputted from the Video Decoder, there are some signals whose ratio of the Sync Tip to the Video Ratio is not proportional due to the external factors such as Long Cable, Distributor...etc. as shown in Figure 2.7. In order to respond to such entry, NVP1114A supports White Peak Detect function that refers to the white peak information along with the Amplitude information of Sync Tip for the implementation of AGC to reach the Target Gain level. The "White Peak Detect function" can be set as follows depending on what the user needs as shown in Table 2.2.

In order to operate the White Peak Detector, the out of as seen in Figure 2.8 can be generated with the input like the one in Figure 2.7.

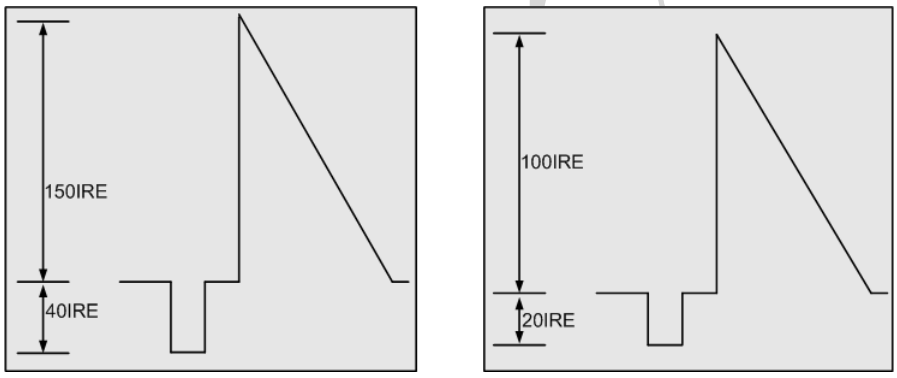


Figure 2.7. Input when the ratio of Sync Tip vs. Video Ratio is not proportional

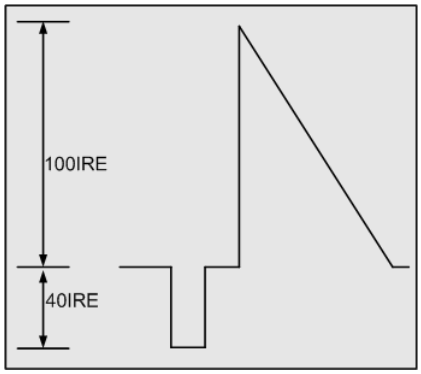


Figure 2.8. Outcome of the White peak Detector

Address	White Peak "On"	White Peak "Off"
BANK0, 0x99[1:0] [white peak threshold([9:8])]	0x51	0x51
BANK0, 0x9A [white peak threshold([7:0])]	0xB5	0xB5
BANK0, 0x9B [white peak on/off]	0x03	0x13
BANK0, 0x9C [white peak speed]	0x03	0x03
BANK0, 0x9D [white peak control]	0x22	0x22

Table 2.2 White Peak Detector-Driven Register Setting Value

2.9. Data Output Pin Order Control

: NVP1114A can change the order of the output pin in the 27MHz/54MHz/108MHz Output Mode as shown in Table 2.3. (OUT_DATA_INV, Bank0, 0x85[7:4])

Address		Data Output of Channel X
Bank0, 0x85, OUT_DATA_INV [3]	0	channel 4 out [7:0]
	1	channel 4 out [0:7]
Bank0, 0x85, OUT_DATA_INV [2]	0	channel 3 out [7:0]
	1	channel 3 out [0:7]
Bank0, 0x85, OUT_DATA_INV [1]	0	channel 2 out [7:0]
	1	channel 2 out [0:7]
Bank0, 0x85, OUT_DATA_INV [0]	0	channel 1 out [7:0]
	1	channel 1 out [0:7]

Table 2.3. Data Output Pin Order Control

2.10. Output Format

: NVP1114A supports a format of standard ITU-R BT.656. Channels of 4 is synchronized by each clock(VCLK01, VCLK02, VCLK03, VCLK04). Phase of clock is controlled by CH_CLK_SEL and CLK_DELAY_SEL of (BANK0, 0x2E, 0x3E, 0x4E, 0x5E).

2.10.1. ITU-R BT.656 Format

: Codes of SAV and EAV are injected into data stream of ITU-R BT.656 to indicate a start and a end of active. Note that a number of pixel for 1H Active line is always constant regardless of the actual incoming line length. Therefore, variance of analog input signal is applied to a blank section except codes of EAV and SAV. Fig 2.9 shows data stream of ITU-R BT.656 format. If length of 1H of analog input signal increase or decrease, number of pixel of 'A' increase or decrease.

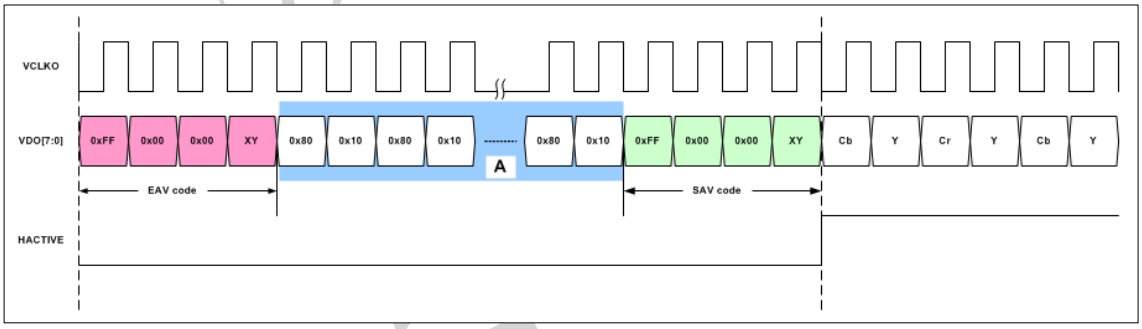


Figure 2.9. Region of active is constant

2.11. Output Mode

: When it comes to the transfer of the output to the back-end device, NVP1114A supports all the output of 27MHz/54MHz/108MHz Data Rate.

2.11.1. 27MHz D1 Data Output Mode

: Operated in the 27MHz D1 Data Out Mode, NVP1114A outputs VCLK01, VCLK02, VCLK03, VCLK04 and VD01[7:0],VD02[7:0], VD03[7:0], VD04[7:0] in the timing as shown in Figure 2.10. For VCLK01, VCLK02, VCLK03 and VCLK04 phase adjustment can be made against VD01~VD04 using "Clock delay control" Register. (CLK_DELAY_SEL, BANK0, 0x2E/3E/4E/5E[3:0])(CHx_OUT_SEL, BANK0, 0x2F/3F/4F/5F[2:0])

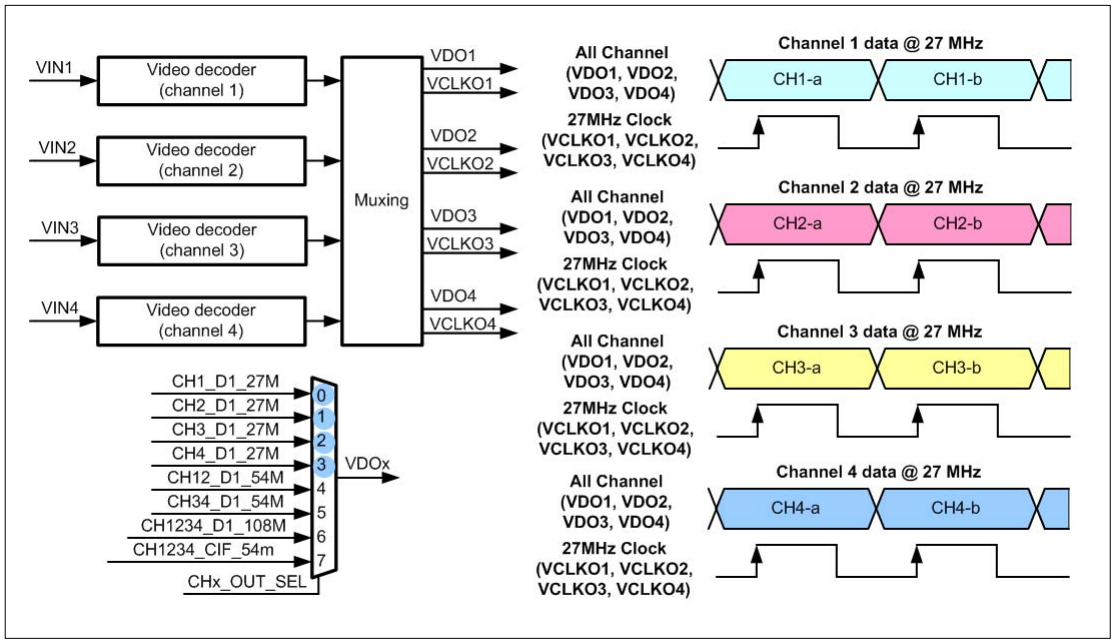


Figure 2.10. 27MHz D1 Data Output

2.11.2. 54MHz D1 Data Output Mode

: Operated in the 54MHz D1 Data Out Mode, NVP1114A outputs VCLK1, VCLK2 and VDO1[7:0], VDO2[7:0] in the timing as shown in Figure 2.11. Two channel Video data stream(720x480/720x576) represents 8bit ITU-BT.656 4:2:2 format with 54MHz multiplexed. For VCLK1 and VCLK2, phase adjustment can be made against VDO1,VDO2 using "clock delay control" Register.
(CLK_DELAY_SEL, BANK0, 0x2E/3E[3:0]), (CHx_OUT_SEL, BANK0, 0x2F/3F[2:0])

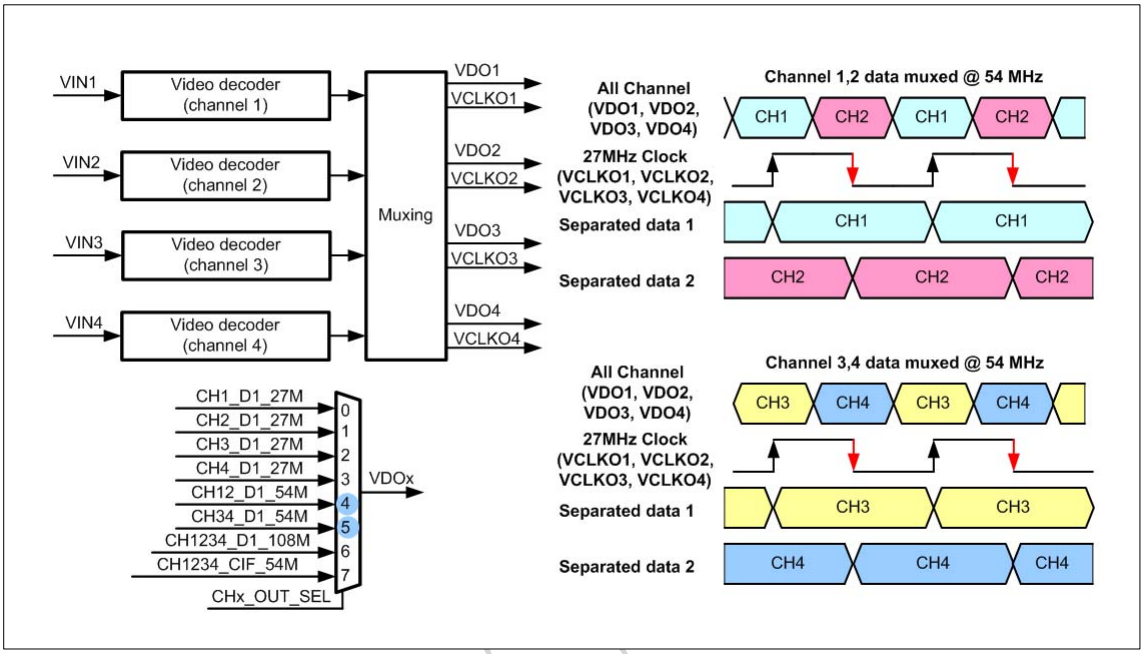


Figure 2.11. 54MHz D1 2Channel Data Output

2.11.3. 108MHz D1 Data Output Mode

: Operated in the 108MHz D1 Data Out Mode, NVP1114A outputs VCLK2 and VDO2[7:0] in the timing as shown in Figure 2.12. Four channel Video data stream(720x480/720x576) represents 8bit ITU-BT.656 4:2:2 format with 108MHz multiplexed. For VCLK2 phase adjustment can be made against VDO2 using "clock delay control" Register. (CLK_DELAY_SEL, BANK0, 0x3E[3:0]), (CHx_OUT_SEL, BANK0, 0x3F[2:0])

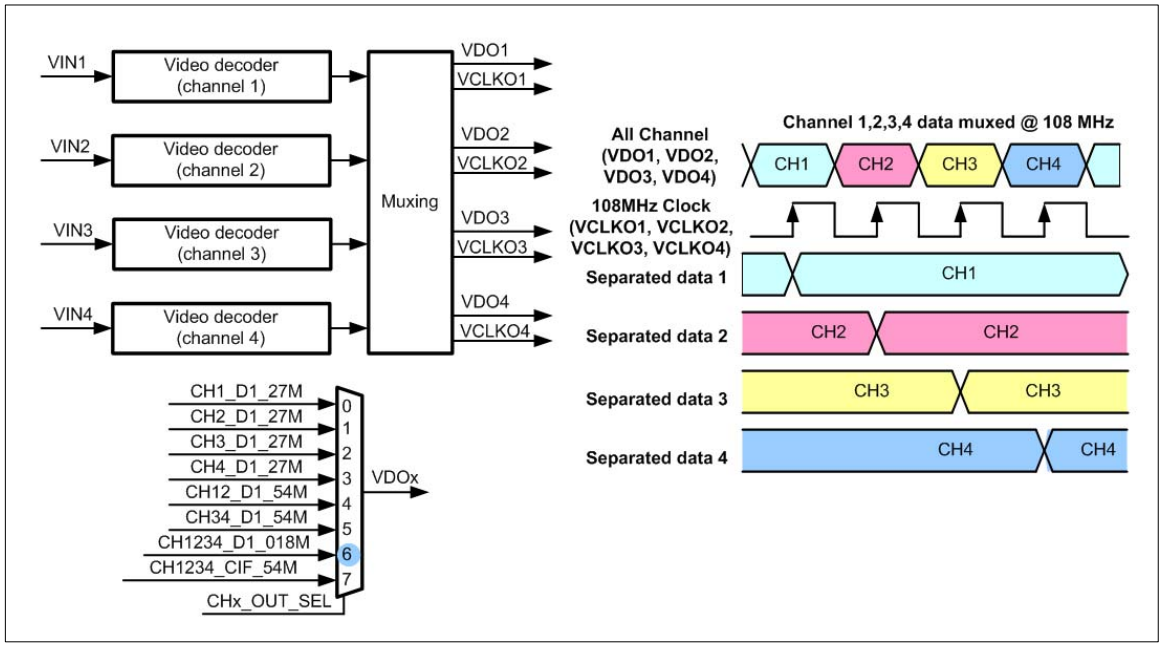
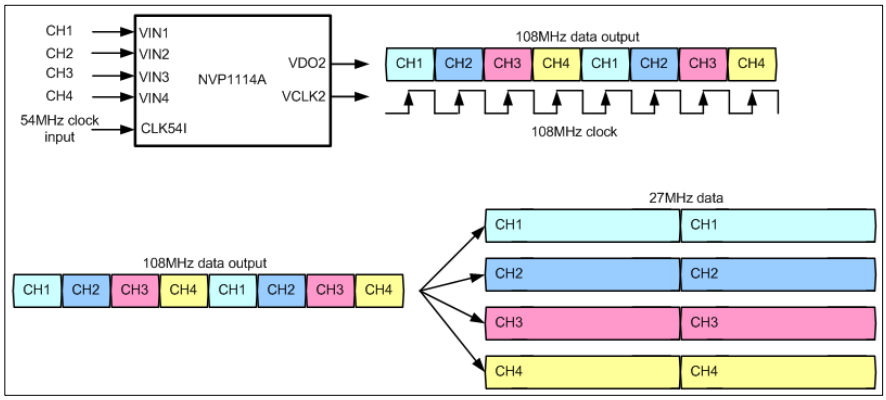


Figure 2.12.108Mhz D1 4Channel Data Output

■ Example of 108MHz D1 Data Output Mode with Channel ID

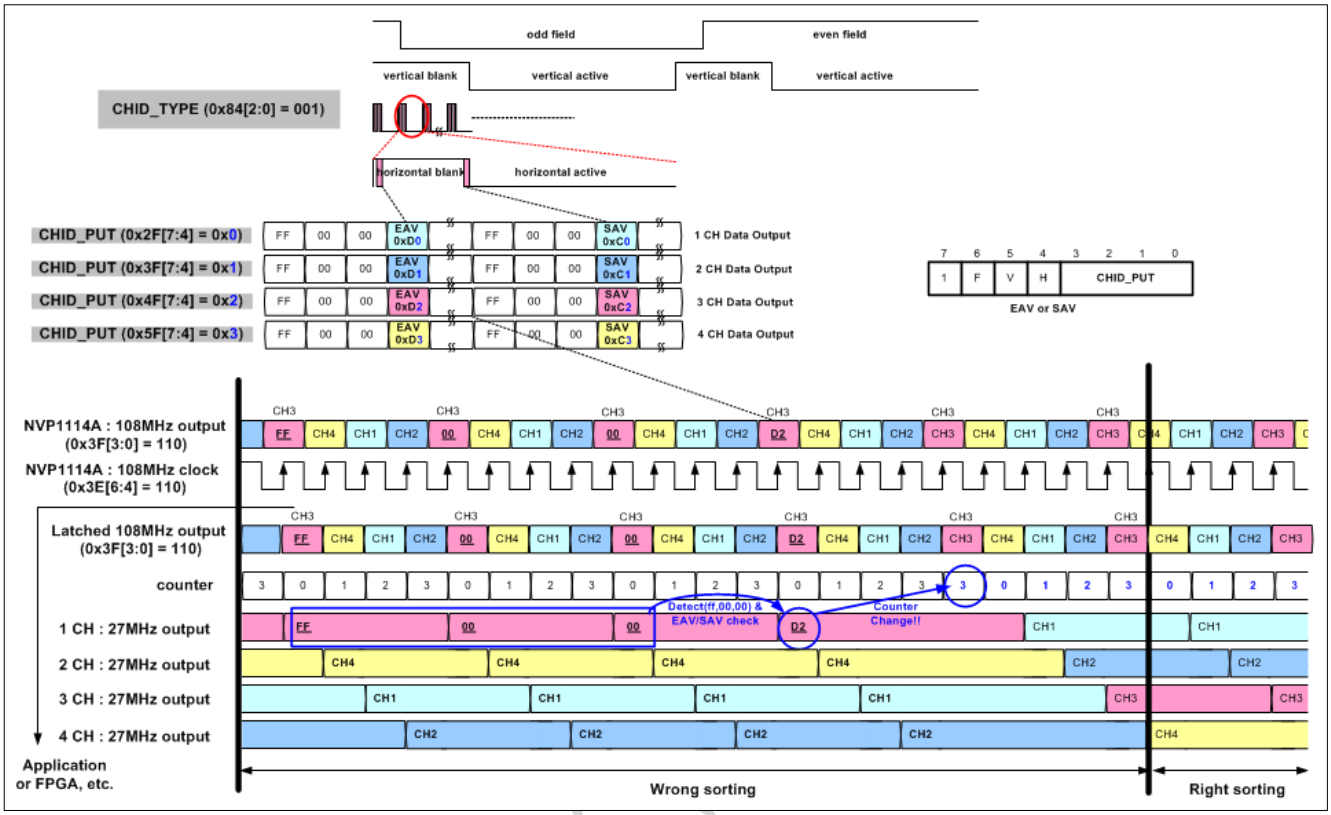
1. In case of VDO2 output port and VCLK2 output clock use.
2. Set VDO2 output(CH2_OUT_SEL, BANK0, 0x3F[2:0] = 0x6) and VCLK2 output(CH2_CLK_SEL, BANK0, 0x3E[6:4] = 0x6 or 0x7).
3. Set Channel ID Type (Refer to CHID_TYPE(0x84[2:0]) Register Description)
4. And then NVP1114A generate 108MHz clock and data output (Ex-Figure 1)

   If you want to confirm the 108MHz Data using FPGA or Other device, Execute 5~11 item in next page.



Ex-Figure 1

5. FPGA or equivalent devices which is input 108MHz time multiplexed data output, need to align with same channel data(27MHz 1,2,3,4 channel). EX-Figure 2 shows how to use Channel ID as a example.



Ex-Figure 2

6. CHID_TYPE(0x84[2:0]=001) mode described in top of Ex-Figure2
7. To generate 2bit digit, Design 2bit counter with VCLK2 (The 2bit digit means each channel).
8. Using 2bit digit, Convert from 108MHz Data to 27MHz Data (Wrong sorting part in Ex-Figure 2). and then Define the 2bit digit (0 : 1ch data, 1 : 2ch data, 2 : 3ch data, 3 : 4ch data). namely, 108MHz data output separate only with 27MHz, 4channel data, is not align with channel data where becomes mapping in counter value.
9. For mapping between separated each channel data and specified counter value, Select channel among separated each channel(1CH selected in Ex-Figure 2).
   If selected channel data become Right sorting condition, other 3 channel is sorted automatically.
10. Check the 1CH Data output when 2bit counter value is only '0' and then Search the EAV/SAV[3:0] after FF 00 00 Code.
11. If the EAV/SAV[3:0] is '2', make a counter reset to '3' (Refer to Blue color in Ex-Figure 2)
12. Become Right sorting part.

2.11.4. 54MHz CIF Data Output Mode

: Operated in the 54MHz CIF Data Out Mode, NVP1114A outputs VCLK2 and VDO2[7:0] in the timing as shown in Figure 2.13. Four channel Video data stream(360x480/360x576) represents 8bit ITU-BT.656 4:2:2 format with 54MHz multiplexed. For VCLK2 phase adjustment can be made against VDO2 using "clock delay control" Register. (CLK_DELAY_SEL, BANK0, 0x3E[3:0]), (CHx_OUT_SEL, BANK0, 0x3F[2:0])

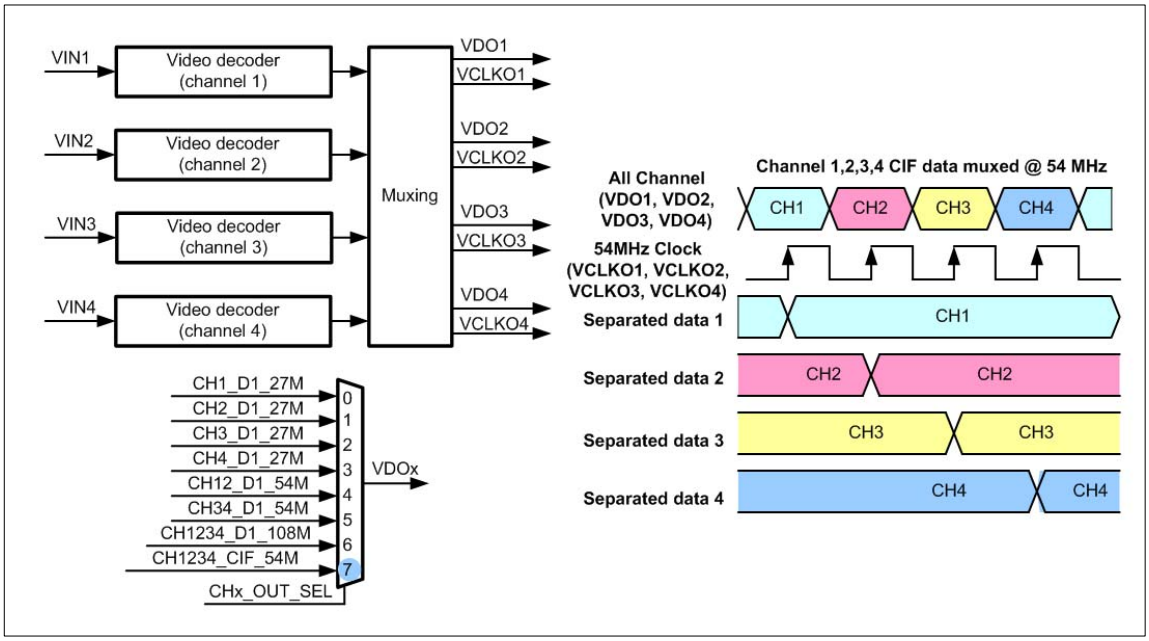


Figure 2.13. 54Mhz CIF 4Channel Data Output

2.12. Motion Detector

: NVP1114A supports motion detection function. It is designed in a way that using one Motion Detection module, the motion of the four channels can be detected in rotation. It also supports the output of the detected motion information on the screen. The function allows a screen such as the one shown in Figure 2.14. to be divided in 16 sections each of which can generate information on the motion detection information. For each section, motion detection can be controlled to be set at on/off. Once a motion is detected, the screen can be rendered dark or reversed in the unit of field to have the spot of the motion generated to be indicated in the screen.

2.12.1. How to Operate the Motion Detection Function

1). Set the Motion detection On (Bank1, 0xA1/A3/A5/A7[4]) - Set at low

2). Set the area for which to detect motion

: The screen is divided into 16 sections and each section is matched one to one.
(BANK1, 0xB0~0xB7 - Channel #1, Bank1, 0xB8~BF - Channel #2)
(BANK1, 0xC0~0xC7 - Channel #3, BANK1, 0xC8~CF - Channel #4)

3). Set the motion sensitivity 1 (Pixel Sensitivity: Set at BANK1 0xA9)

4). Set the motion sensitivity 2 (Temporal Sensitivity : Set at BANK1 0xA2/A4/A6/A8)

: When setting motion sensitivity, it is recommended to set the pixel sensitivity at "0x4B" and use the temporal sensitivity to send the sensitivity to situation.

5). Output of Motion Detection

: Motion information generated from each section is not to be generated separately through data interface. In other words, the motion information needs to be confirmed in the register or It is not included in the CCIR656 data.

: Motion information generated from each area can be displayed on the screen.
Display can be done through three approaches. This can be controlled using Motion_PIC (BANK1, 0xA1/A3/A5/A7[1:0]).

1-FIELD DATA

AREA 01	AREA 02	AREA 03	AREA 04	AREA 05	AREA 06	AREA 07	AREA 08
AREA 09	AREA 10	AREA 11	AREA 12	AREA 13	AREA 14	AREA 15	AREA 16
AREA 17	AREA 18	AREA 19	AREA 20	AREA 21	AREA 22	AREA 23	AREA 24
AREA 25	AREA 26	AREA 27	AREA 28	AREA 29	AREA 30	AREA 31	AREA 32
AREA 33	AREA 34	AREA 35	AREA 36	AREA 37	AREA 38	AREA 39	AREA 40
AREA 41	AREA 42	AREA 43	AREA 44	AREA 45	AREA 46	AREA 47	AREA 48
AREA 49	AREA 50	AREA 51	AREA 52	AREA 53	AREA 54	AREA 55	AREA 56
AREA 57	AREA 58	AREA 59	AREA 60	AREA 61	AREA 62	AREA 63	AREA 64

Figure 2.14 NVP1114A Motion Display

2.13. Scaler

: NVP1114A has 4 scalers. A Scaler plays a role to reduce input image size to the size user wants. Please refer to the figure as below.

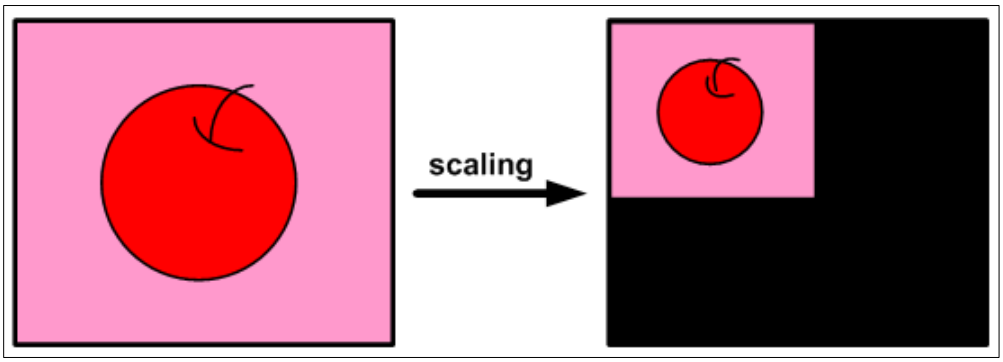


Figure 2.15 Function of Scaler

NVP1114A assigns each decoder to such channel. A User uses this scaler to control the size of input image by 1/32 for horizontal and vertical direction. H-direction's size can be controlled by the H_DTOx[19:0](0xC6~0xD1) register and V-direction's one by V_DTOx[19:0](0xCE~0xD9) register. The values of H_DTOx and V_DTOx is determined by following formula.

NTSC : H_DTOx[19:0] = (HP_scaled/720)×(2^19)
V_DTOx[19:0] = (VP_scaled/240)×(2^19)
PAL : H_DTOx[19:0] = (HP_scaled/720)×(2^19)
V_DTOx[19:0] = (VP_scaled/288)×(2^19)

Where, HP_scaled indicates horizontal pixel number or the size of the image which a user wants to get. VP_scaled does the same role as HP_scaled but for vertical direction.

For example of using this register, if you need 360x120 scaled image in NTSC, H_DTOx[19:0] shall have the value of (360/720)×2^19. Simply, H_DTOx[19:0] = 2^18. And V_DTOx[19:0] becomes (120/240)×2^19. Again, V_DTOx = 2^18

The table as below is register values for common scale sizes.

Registers	704x288	704x240	640x288	640x240	320x288	320x240	320x144	320x120
H_DTO1[19:16] (0xCE[3:0])	0x7	0x7	0x7	0x7	0x3	0x3	0x3	0x3
H_DTO1[15:8] (0xCA)	0xD2	0xD2	0x1C	0x1C	0x8E	0x8E	0x8E	0x8E
H_DTO1[7:0] (0xC6)	0x7D	0x7D	0x71	0x71	0x38	0x38	0x38	0x38
V_DTO1[19:16] (0xCE[7:4])	0x8	0x8	0x8	0x8	0x8	0x8	0x4	0x4
V_DTO1[15:8] (0xD6)	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
V_DTO1[7:0] (0xD2)	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

Table 2.4. Register Value for Scale used frequently

NVP1114A's scaler has two types of output as you can see in figure 2.16.
In mode1, the area which is not scaled is treated as blank. Therefore it can be longer than existing horizontal blank section. In this case, you should regard that in order to reduce the vertical size, it extend the horizontal blank section instead of using vertical blank. Hence, vertical blank section is able to have over 1 line range only for horizontal blank section under the standard status.(See the left side of Figure 2.16). Mode2 is output-way that let horizontal and vertical blank signals follow the standard and the section which is supposed to be blanked is changed to the value users define. Please refer to figure 2.16(right side). The blue section displays the result that users define as blue.

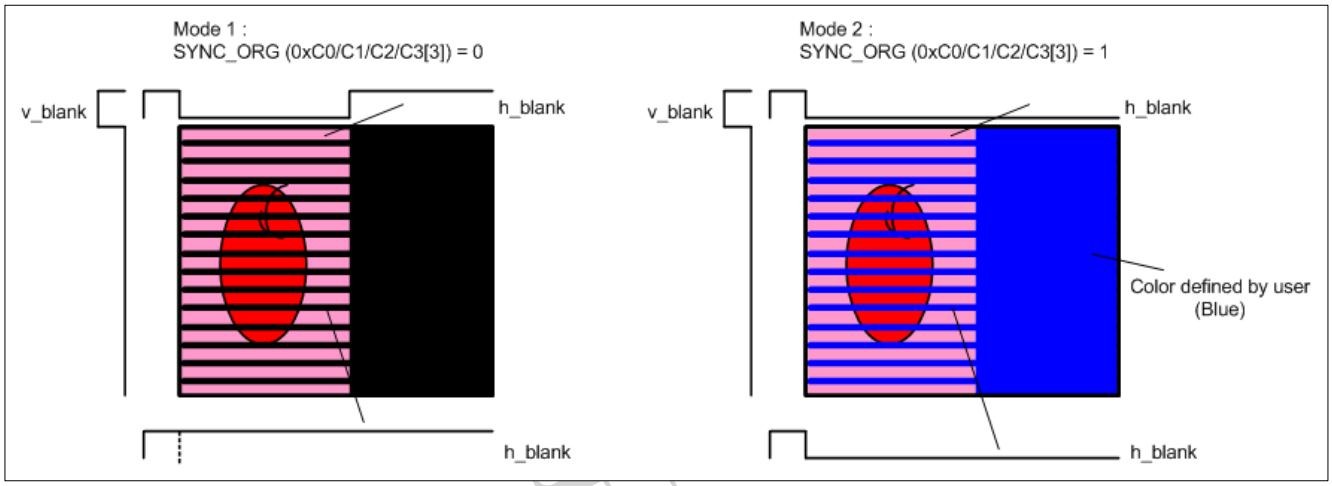


Figure 2.16 Function of Scaler

Figure 2.17 describes more detailed horizontal blank signal of Mode1. This is how scaled signal works in CCIR656 format. SAV packet(0xFF,0x00,0x00,SAV)is fixed, compared with input signal, and EAV packet takes a moving way.

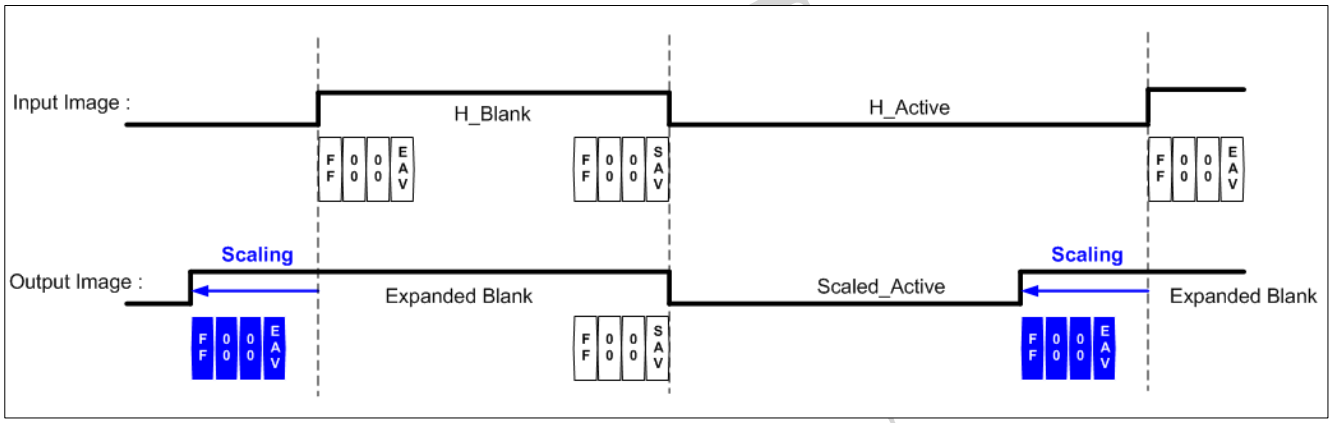


Figure 2.17 Scaled Horizontal Blank Signal of Mode 1

Figure 2.18 describes more detailed horizontal blank signal of Mode21. You might see in the figure that scaled signal is almost matched with horizontal blank signal's standard. But the rest section of the image that scaled signal is displayed is filled with the defined color(Blue) that users choose.

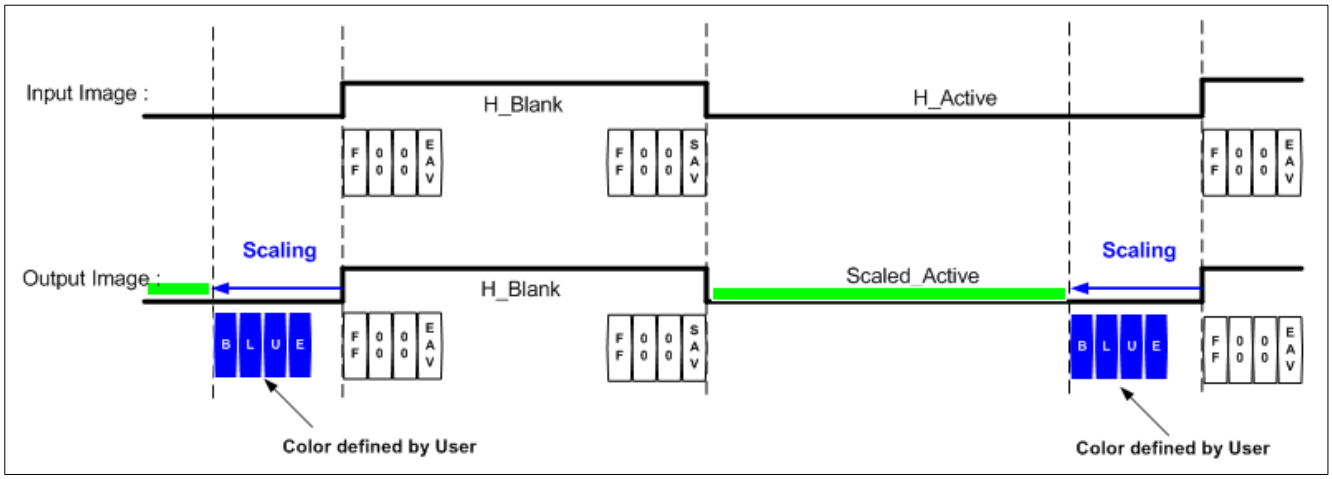


Figure 2.18 Scaled Horizontal Blank Signal of Mode 2

This scaler has a function to increase the 704 active pixel input to 720 size for horizontal direction. for using this function, there is the register to control start position in 16pixel range. That is H_DEL(0x24) (Figure 2.19)

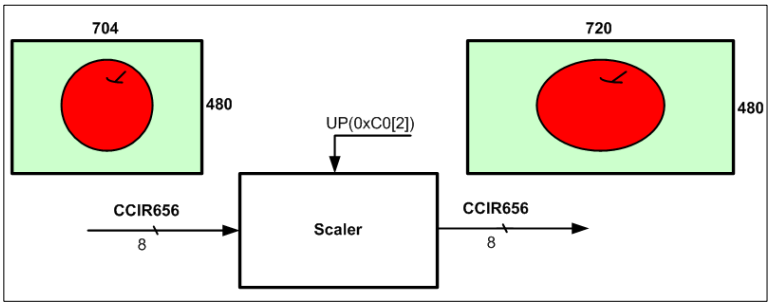


Figure 2.19 720 extension function

2.14. IRQ Pins (Interrupt Request Pins)

Generally, if MICOM or CPU checks the external status frequently, it makes its load heavier because they always works. Therefore, if there is any signal indicating the external status to let CPU know, it reduces CPU's burden. This signal which let CPU know the status of external inputs is called Interrupt and this interrupt signal is delivered to CPU through a pin.

NVP1114A has three interrupt pins. Those pins use GPO pin(#53,54,55) and through 0xE4/E5 registers, type

and phase of the signal can be changed. There are two modes to control the interrupt. Mode1 is CPU doesn't control the interrupt signal. In this mode, the result video decoder recognizes is directly delivered to CPU. In mode2, CPU controls the interrupt signal. For example, about no-video, video decoder let CPU knows the change of no-video(from Low to High) and make changed value(High) hold. And then CPU checks the status of no-video and handle it. After that, CPU initializes the changed value(High→Low)in order the video decoder to re-check no-video.

Please refer to figure 2.20 and 2.21. Those pictures describe the process of treating no-video of CH1 in Mode2. If CPU makes STA_CLEAR(0x0D[0]) high, interrupt signal becomes low. Therefore if input signal keeps in no-video status, interrupt signal is changed to low and gets back to high again. IF input signal is On when you make STA_CLEAR high, interrupt signal keeps in LOW.

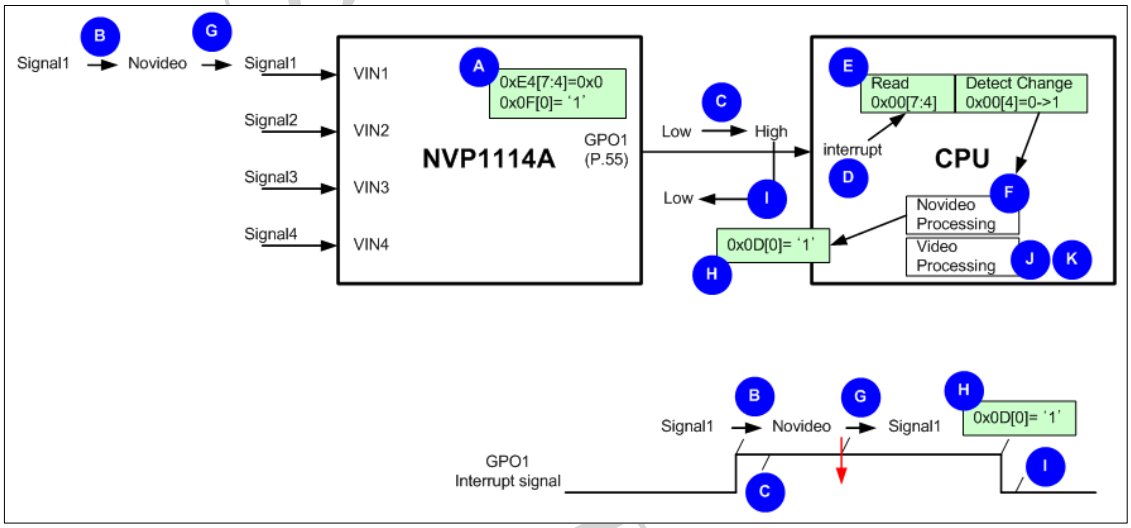


Figure 2.20 Usage example 1 for IRQ Pin

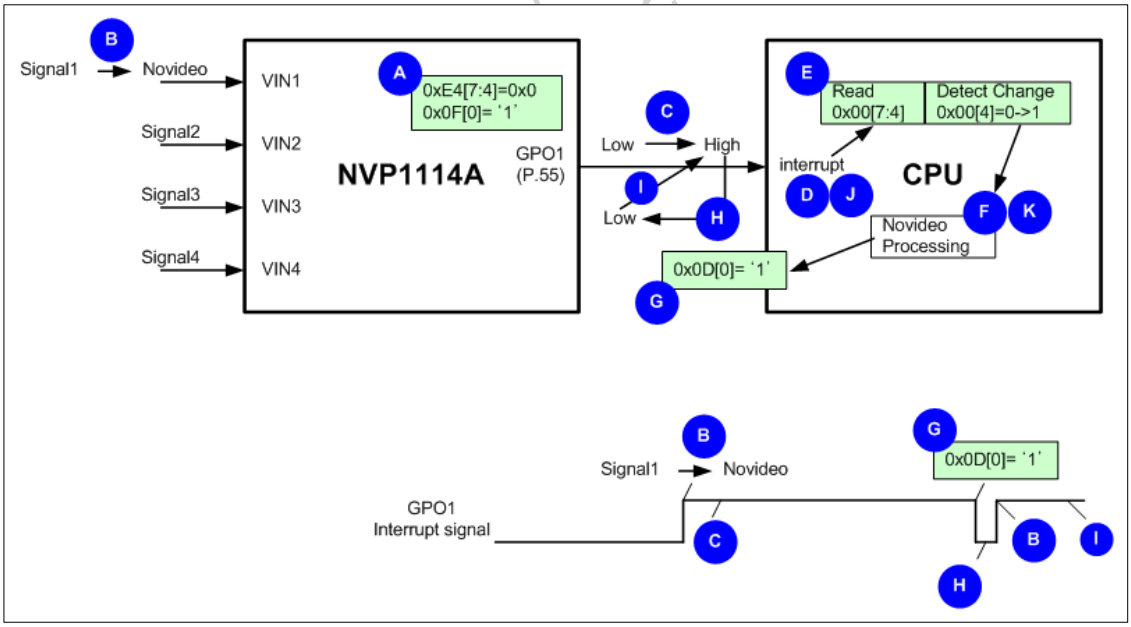


Figure 2.21 Usage example 2 for IRQ Pin

3. Audio Codec

3.1. Description

: NVP1114A outputs PCM digital audio signals converted from analog audio input signals and analog audio signals converted from PCM digital audio signals. NVP1114A has 4 channel ADCs and 1 channel DAC for audio signals.

Voice data convert to G.711 PCM and Linear PCM data, and these converted data is outputted via DSP/SSP/I2S interfaces. The output data will be saved at hard disk or any other storages. This process - to convert and save audio data into storage - is usually called as "Record Output".

The saved audio data is inputted to NVP1114A via DSP/SSP/I2S interfaces. The input audio data is outputted via audio DAC. This process is named as "Playback Output".

NVP1114A selects one audio input signal among four analog audio inputs and this audio is outputted through audio ADC and audio DAC. And it also supports directly mixed audio output signal which 4 analog audio inputs are mixed. This function usually is called by "Live Output".

In addition, NVP1114A supports audio mute detection and cascade function up to 4 chips - 16 audio channels.

3.2. Record Output

: Analog audio data is converted to PCM data and this data is outputted to the other NVP1114A or other IC via DSP/SSP/I2S interfaces. Record output is useful function to save compressed audio data into storage. Analog audio signal is finally outputted to ADATA_REC pin used for data of each channel.

PCM data is categorized based on sampling frequency, sampling data bit width and PCM method. G.711 (A-law/Mu-law) and linear PCM are supported. 8KHz/16KHz and 8bit/16bit are used for sampling frequency and sampling data bit width, respectively. Refer the following table when you set the register value.

	8K/8bit	8K/16bit	16K/8bit	16K/16bit
Linear PCM	Addr:0xA5[2], Val: 0 Addr:0xA5[1], Val: 1 Addr:0xA6[7:6] val: 00	Addr:0xA5[2], Val: 0 Addr:0xA5[1], Val: 0 Addr:0xA6[7:6] val: 00	Addr:0xA5[2], Val: 1 Addr:0xA5[1], Val: 1 Addr:0xA6[7:6] val: 00	Addr:0xA5[2], Val: 1 Addr:0xA5[1], Val: 0 Addr:0xA6[7:6] val: 00
G.711 U-law	Addr:0xA5[2], Val: 0 Addr:0xA5[1], Val: 1 Addr:0xA6[7:6] val: 10	Addr:0xA5[2], Val: 0 Addr:0xA5[1], Val: 0 Addr:0xA6[7:6] val: 10	Addr:0xA5[2], Val: 1 Addr:0xA5[1], Val: 1 Addr:0xA6[7:6] val: 10	Addr:0xA5[2], Val: 1 Addr:0xA5[1], Val: 0 Addr:0xA6[7:6] val: 10
G.711 A-law	Addr:0xA5[2], Val: 0 Addr:0xA5[1], Val: 1 Addr:0xA6[7:6] val: 11	Addr:0xA5[2], Val: 0 Addr:0xA5[1], Val: 0 Addr:0xA6[7:6] val: 11	Addr:0xA5[2], Val: 1 Addr:0xA5[1], Val: 1 Addr:0xA6[7:6] val: 11	Addr:0xA5[2], Val: 1 Addr:0xA5[1], Val: 0 Addr:0xA6[7:6] val: 11

Table 3.1. Sampling & PCM coding setting

DSP/SSP/I2S interfaces are supported as output data format. In addition, slave mode and master mode are also supported. At slave mode, input clock and synchronized signal come from external ICs, however Master mode generates clock and synchronized signal in itself.

3.2.1. Data Output Interface

: NVP1114A outputs "Record Output" using ACLK_REC, ASYNC_REC, ADATA_REC. ACLK_REC is a reference clock signal for Record Output Data and ASYNC_REC is a reference synchronization signal for Record Output Data. ADATA_REC is Record Output, data with reference clock and reference synchronized signal.

ACLK_REC is a reference clock of Record Output Data and ASYNC_REC is reference synchronized signal. ACLK_REC and ASYNC_REC signal support slave mode accepted external signals and master mode generating clock and synchronization signal in itself. And DSP/SSP/I2S interfaces are supported by configuration of these pins defined by internal register setting value.

	DSP	SSP	I2S
Master	Addr:0xA5[0], Val: 1 Addr:0xA5[5], Val: 0 Addr:0xA5[7], Val: 1	Addr:0xA5[0], Val: 1 Addr:0xA5[5], Val: 1 Addr:0xA5[7], Val: 1	Addr:0xA5[0], Val: 0 Addr:0xA5[5], Val: 0 Addr:0xA5[7], Val: 1
Slave	Addr:0xA5[0], Val: 1 Addr:0xA5[5], Val: 0 Addr:0xA5[7], Val: 0	Addr:0xA5[0], Val: 1 Addr:0xA5[5], Val: 1 Addr:0xA5[7], Val: 0	Addr:0xA5[0], Val: 0 Addr:0xA5[5], Val: 0 Addr:0xA5[7], Val: 0

Table 3.2. Record Output Interface configuration

Figure 3.1, 3.2, 3.3 shows timing diagram of I2S, DSP, and SSP mode, respectively. These figures show timing relation among ASYNC_REC, ACLK_REC and ADTA_REC. Polarity of ACLK_REC clock is changed by setting of internal register value [0xA5[3], RM_CLK].

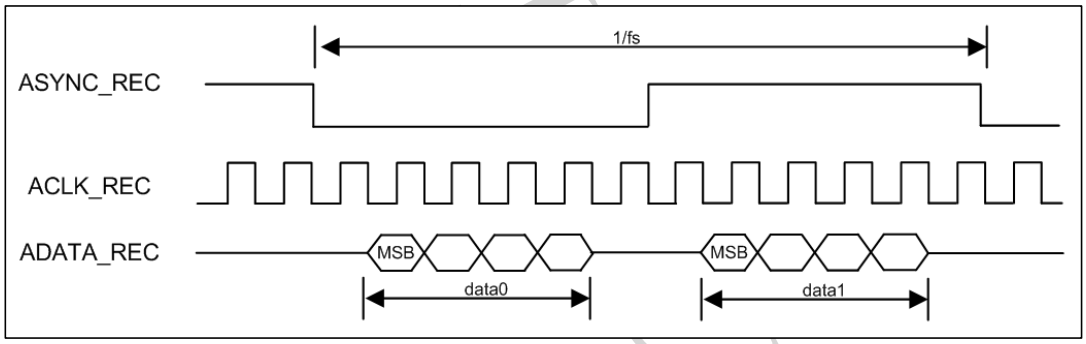


Figure 3.1. I2S mode

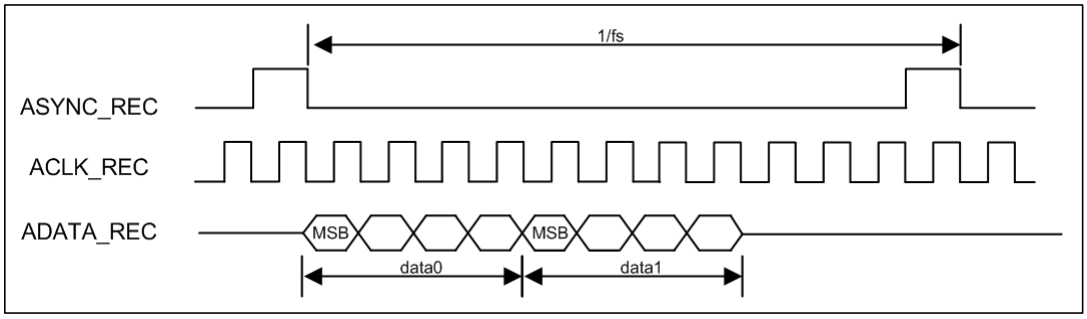


Figure 3.2. DSP mode

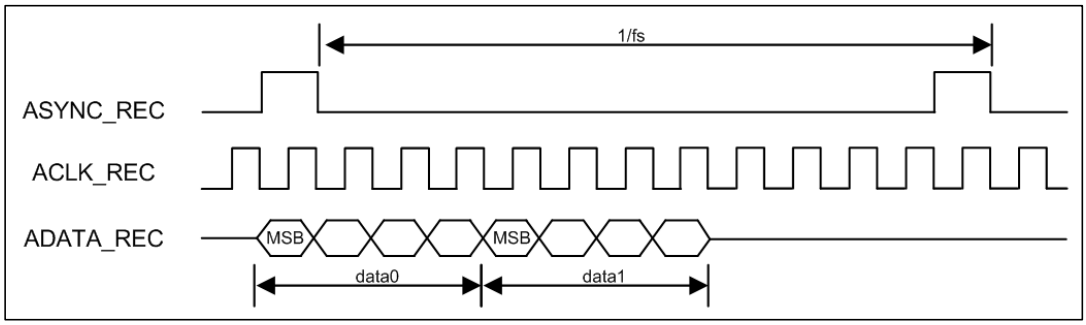


Figure 3.3. SSP mode

3.2.2. 2/4/8/16-Channel Data Output

: ADATA_REC supports up to 4 channel audio using single chip and up to 16 channel in cascade mode. The number of output channel is configured by internal register value [0xA6[1:0], R_MULTCH] and the order of output channel is configured by internal register value [0xA7 ~ 0xAE, R_SEQ]. Therefore, the order of audio output can be changed.

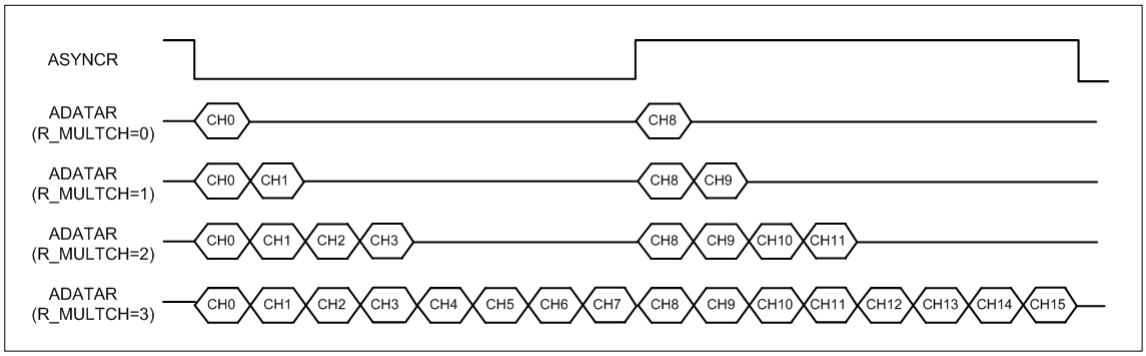


Figure 3.4. audio 2/4/8/16 channel data output <I2S mode>

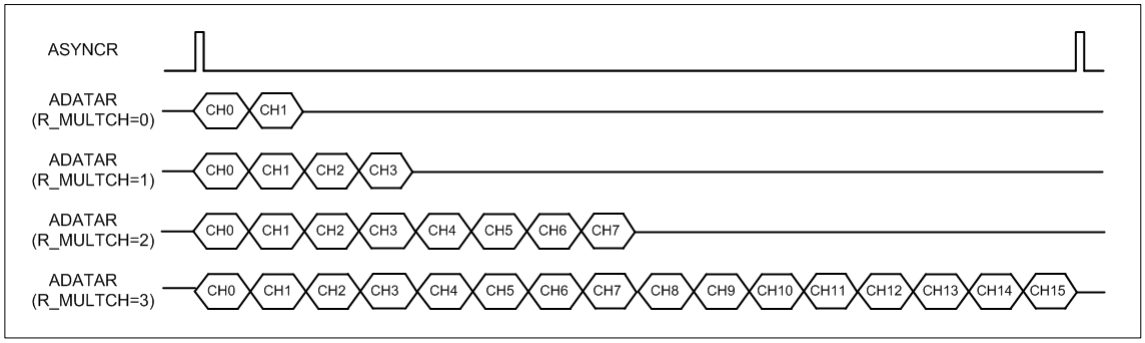


Figure 3.5. audio 2/4/8/16channel data output <DSP/SSP Mode>

3.3. Playback Output

: Playback is to output stored audio data to external device through DAC after internal processing.

NVP1114A gives and takes a clock and synchronization signal through ACLK_PB and ASYNC_PB pin. In this case, interface is the exactly same as Record data's interface. When multi-channel audio is supported, selective playback for intended channel is enable using register setting [0xB8[7:4], PB_SEL]. In case of single channel, PB_SEL should be set to "0000".

ACLK_PB and ASYNC_PB supports Master mode and Slave mode. In master mode, ACLK_PB and ASYNC_PB are outputted by NVP1114A, and clock and synchronization signal come from external devices at slave mode. Master/Slave mode is selected by setting internal register [0xAF[7], PB_MASTER].

ADATA_PB accepts an audio data synchronized with ACLK_PB and ASYNC_PB. ACLKP and ASYNCP accept I2S/DSP/SSP mode input and output, and I2S and DSP mode is set by internal register value [0xAF[0], PB_SYNC]. When DSP mode is selected, DSP/SSP mode is set by [0xAF[5], PB_SSP]. The relation of clock, synchronized signal and data are the exactly same as that of record/mix output. PB_CLK can be inverted for all modes using setting of register [0xAF[3], PB_CLK].

3.4. Audio detection

: NVP1114A has an audio mute detection block for individual 4 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the ADET_MODE and ADET_FILT (0xB5) register, and the detecting threshold values are defined by ADET_TH register (0xB6, 0xB7). According to this control bits and its result (audio detected), Interrupt is generated through the interrupt pins.

3.5. Cascade Operation

: NVP1114A supports cascade mode. Maximum 4 NVP1114A chips can be connected together for cascade mode and can be processed 16 channel voice encoding data. Cascade is enabled by setting register [0xA6[5:4], CHIP_STAGE]. The following figures show how to connect NVP1114A for each cascade modes. In this case, analog audio AOUT0 is assigned to AIN0-15,playback audio or all channel mixed audio as selected by MIX_OUTSEL.

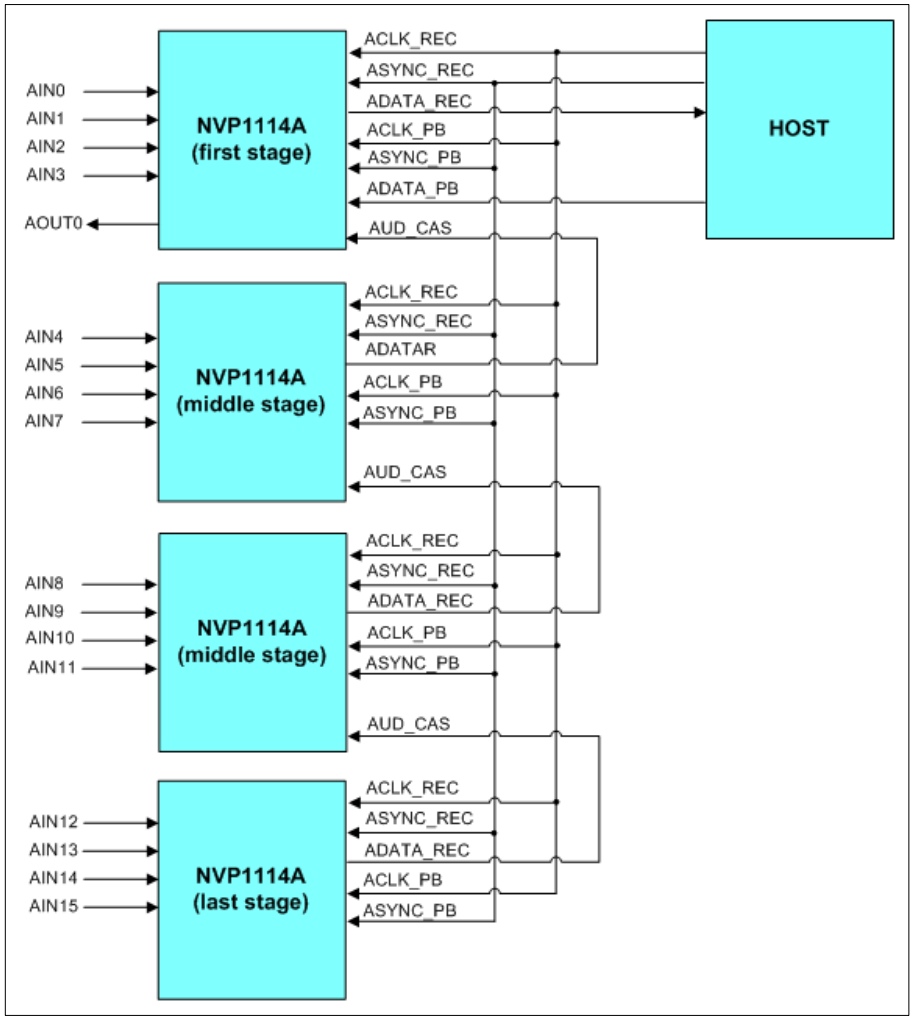


Figure 3.6. NVP1114A cascade mode

3.5.1. 16Channel Data Output

: Output of ADATA_REC supports up to 4 channels at single channel mode, and supports up to 16 channels at cascade mode. The number of output channels is set by register [0xA6[1:0], R_MULTCH]. The following figures show the output order of audio data and this order can be changed by setting register [0xA7 - 0xAE, R_SEQ].

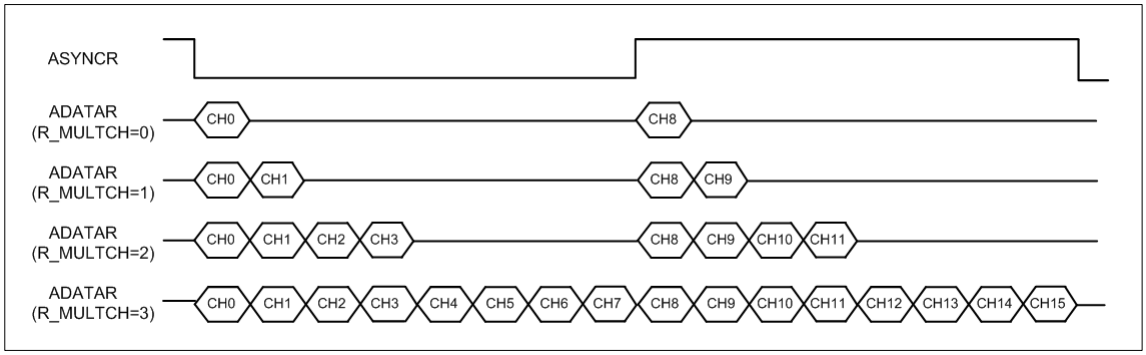


Figure 3.7. 16Channel Data output <I2S Mode>

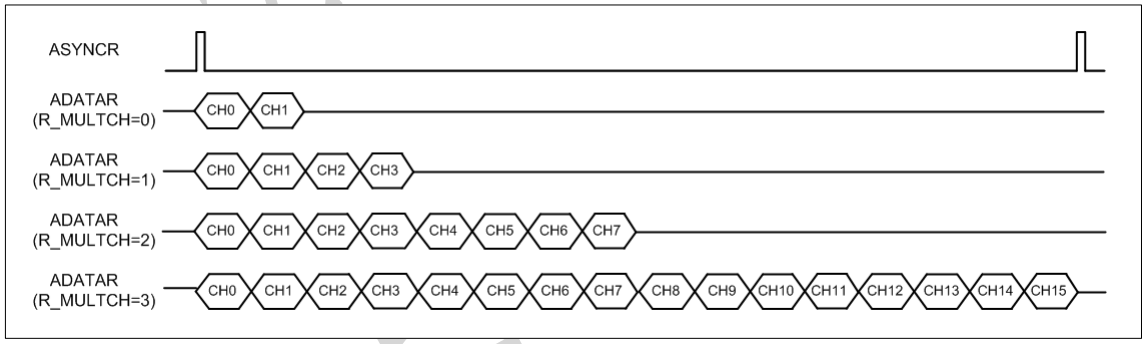


Figure 3.8. 16Channel Data Output <DSP/SSP Mode>

4. Video Encoder

4.1. Video Encoder Function Description

: NVP1114A has an independent video encoder that generates standard NTSC and PAL video signals. Video encoder receives digital video signal and generates analog video signal. The video encoder consists of Sync Separator, Pre-processing, Y/C low-pass filter, Modulation Part, Output Mux, and DAC (Digital-to-Analog Converter). DAC has a two-channel output and a 10-bit resolution. The video encoder works on 27 MHz and generates four analog video signals after receiving 8-bit CCIR656 data. The video signal generated at each channel is one of the following: CVBS, S-video(Y or C). A video encoder has an internal Color-Bar Generator for test purpose. Figure 4.1 shows a block diagram of a video encoder installed in NVP1114.

Video Encoder Feature

- -. Support NTSC/PAL and sub-standard format
- -. Accepts ITU-R.656 compatible 8bit video Input
- -. 27MHz Oscillator clock for Sub-carrier generation.
- -. Includes 2*10Bit DAC(Digital-to-Analog Converter) for generating CVBS, Y/C.
- -. Includes Color-Bar test pattern generator

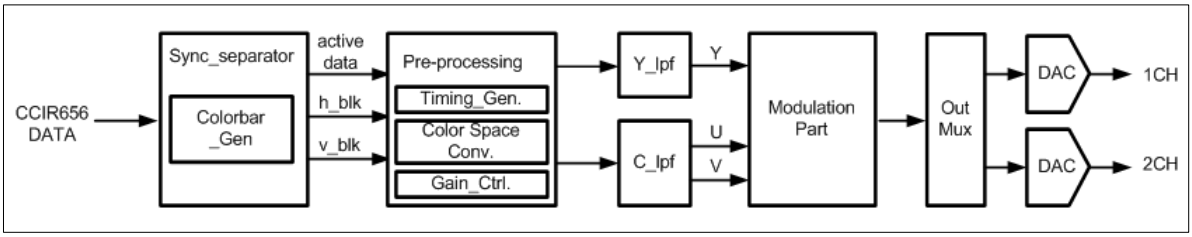


Figure 4.1. Video Encoder Data Flow of NVP1114A

4.2. Sync Separator

: Sync Separator extracts active data, horizontal blank and vertical blank from CCIR656 data. The information on the active data, horizontal blank, and vertical blank is present in EAV and SAV of CCIR656. In other words, they perform the job of separating video and timing signals that are included in digital video standard signals.

4.3. Pre-Processing

: Pre-processing block has three functions. First, it creates timing signals (Timing Generator). Second, it converts Y, Cb, Cr into Y, U, V (Color Space Conversion). Third, it controls the scale (Gain Control). The timing generator generates the Sync signal out of the Horizontal and Vertical Blank as well as various timing signals. As for the Color Space Conversion, the following formulas are used to convert Y, Cb, Cr into Y, U, V.

Standards	Y	U	V
NTSC (M), PAL (M, N),	0.591 (Y601 - 64)	0.504 (Cb - 512)	0.711 (Cr - 512)
NTSC (J)	0.639 (Y601 - 64)	0.545 (Cb - 512)	0.769 (Cr - 512)
PAL (B, D, G, H, I, Nc)	0.625 (Y601 - 64)	0.533 (Cb - 512)	0.752 (Cr - 512)

As for the gain control, Sync, Burst, Luma and Chroma can be adjusted in the scale from 0 to about 2. The increment in scale is 1/127. Figure 4.2 shows adjustments for each control.

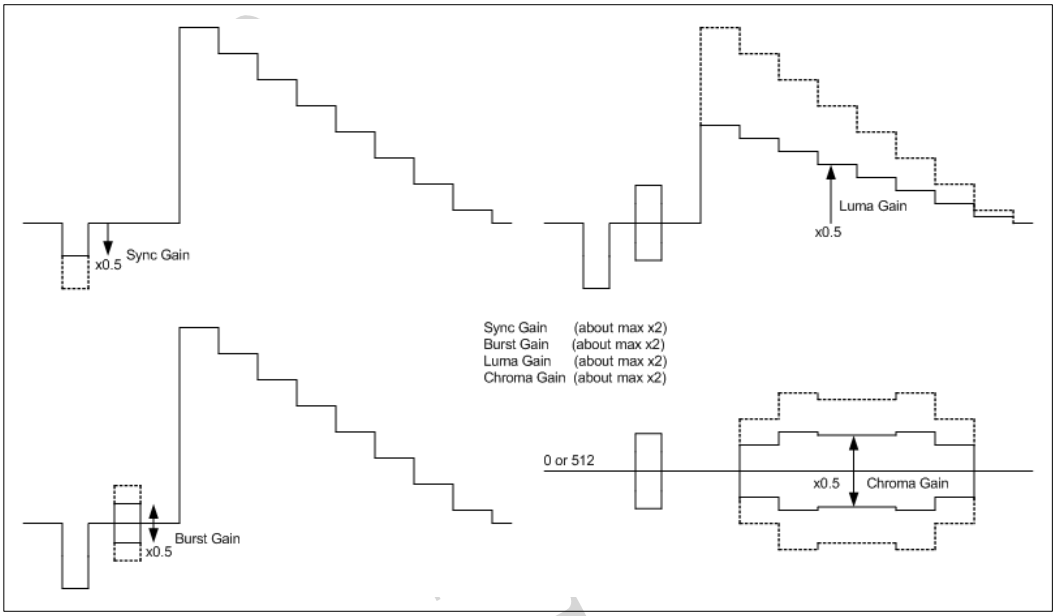


Figure 4.2. Gain Control for Burst, Sync, Luma, Chroma

4.4. Y/C low-pass filter

: Low-pass filtering at 6MHz is done in order to remove high frequency components that happen when Y is over-sampled. To eliminate aliases that may occur after modulation, low-pass filters of 0.6 MHz, 1 MHz, and 1.3 MHz are used according to frequency bandwidths of U and V.

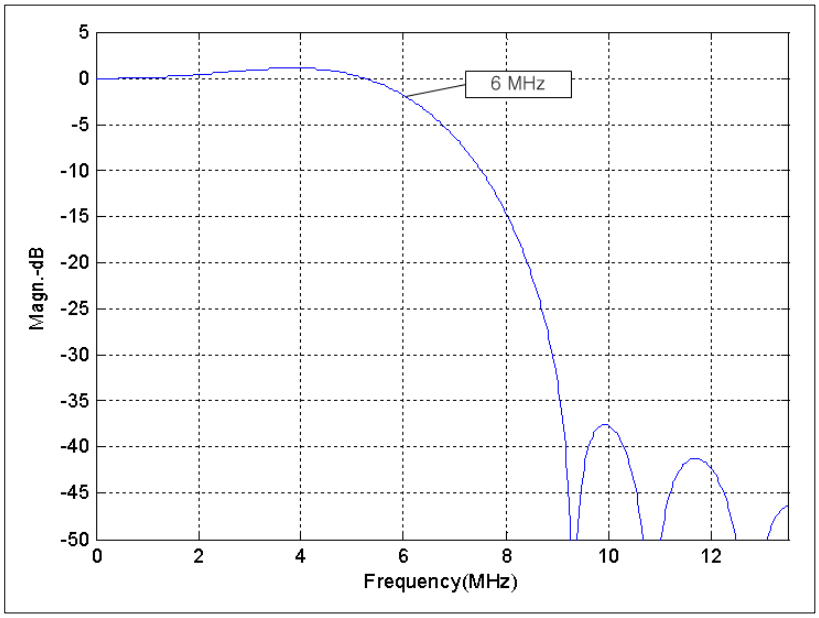


Figure 4.3. Frequency characteristic for luma filter

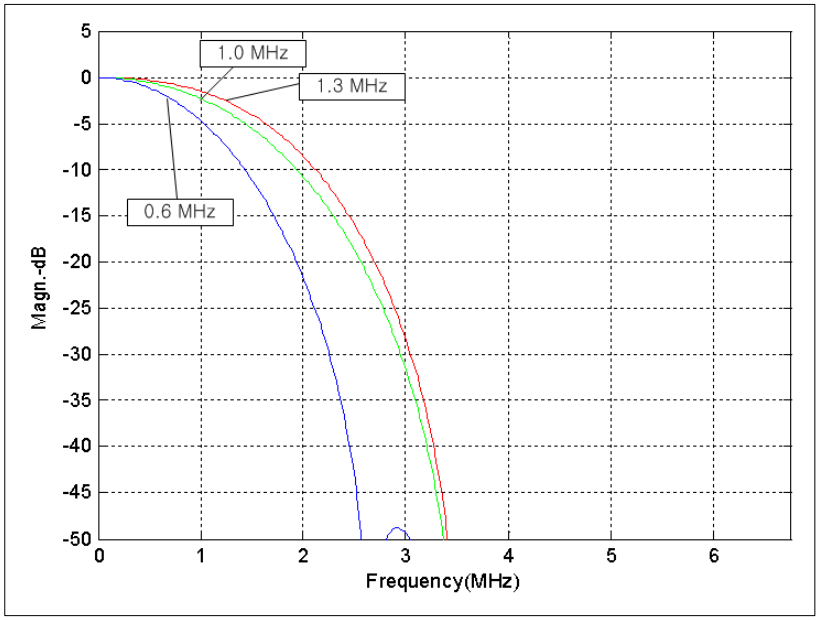


Figure 4.4. Frequency characteristic for chroma filter

4.5. Modulation Part

: The modulation block generates chroma signal through AM modulation. AM modulation is applied to NTSC and PAL. Figure 4.5 shows chroma formed by way of AM modulation for NTSC and PAL .

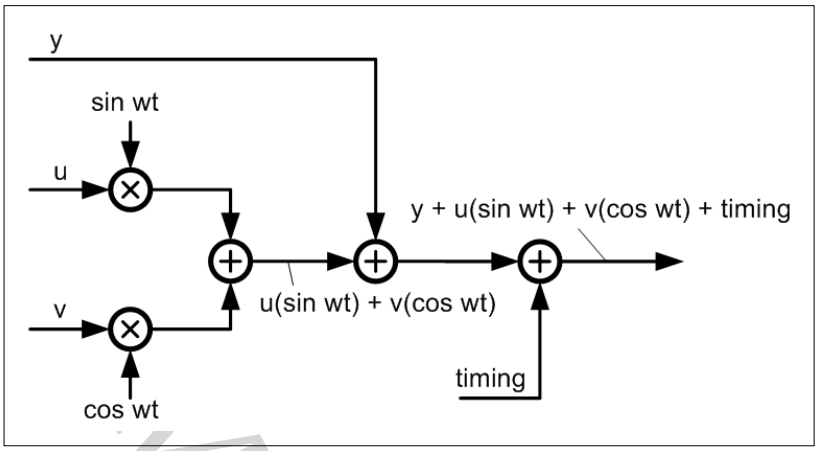


Figure 4.5. AM Modulation for NTSC and PAL

4.6. R/G/B & Y/Pb/Pr Processing

: This block performs color space conversion: it converts Y,Cb,Cr into R,G,B or Y,Pb,Pr. Low-pass filtering is performed after the conversion. The following represents the formulas for color space conversion.

For RGB,

when the pedestal level is present,

R' = 0.591 (Y601 - 64) + 0.810 (Cr - 512)

G' = 0.591 (Y601 - 64) - 0.413 (Cr - 512) - 0.199 (Cb - 512)

B' = 0.591 (Y601 - 64) + 1.025 (Cb - 512)

without pedestal level,

R' = 0.625 (Y601 - 64) + 0.857 (Cr - 512)

G' = 0.625 (Y601 - 64) - 0.437 (Cr - 512) - 0.210 (Cb - 512)

B' = 0.625 (Y601 - 64) + 1.084 (Cb - 512)

For YPbPr,

Y = ((800 - 252)/(940 - 64))(Y601 - 64)

Pb = ((800 - 16)/(940 - 64))(Cb - 64)

Pr = ((800 - 16)/(940 - 64))(Cr - 64)

Figure 4.6 and figure 4.7 show the frequency characteristics of the low-pass filters. Figure 4.6 shows the filter for G and Y, and figure 4.7 shows the filter for B/R or Pb/Pr.

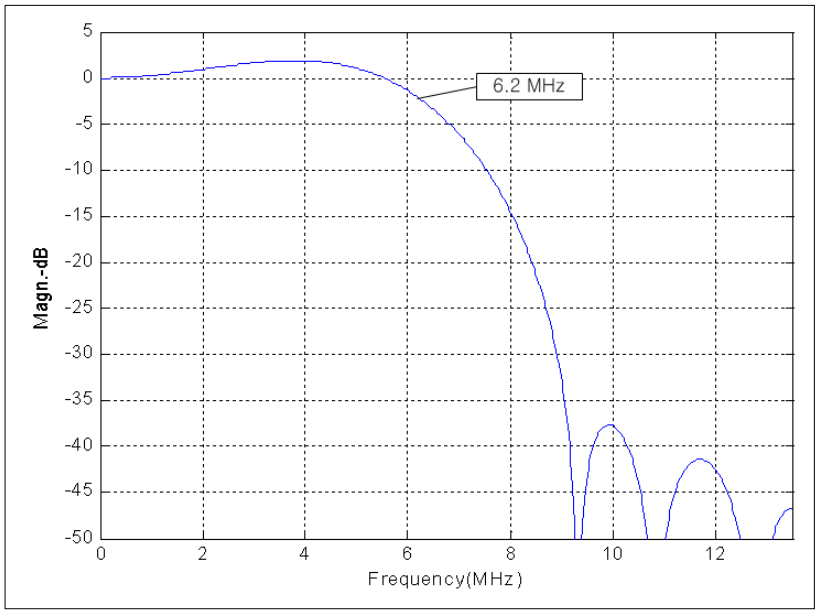


Figure 4.6. low-pass filter for G and Y

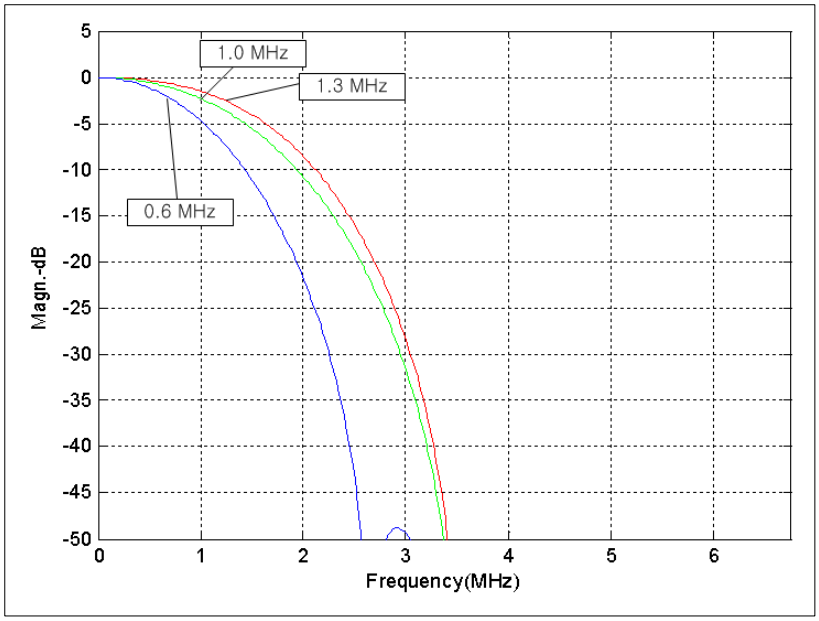


Figure 4.7. low-pass filter for B/R and Pb/Pr

4.7. Output Muxing

: Video Encoder has two channels for output. Each channel generates only one output out of three signals (CVBS, Y, C).

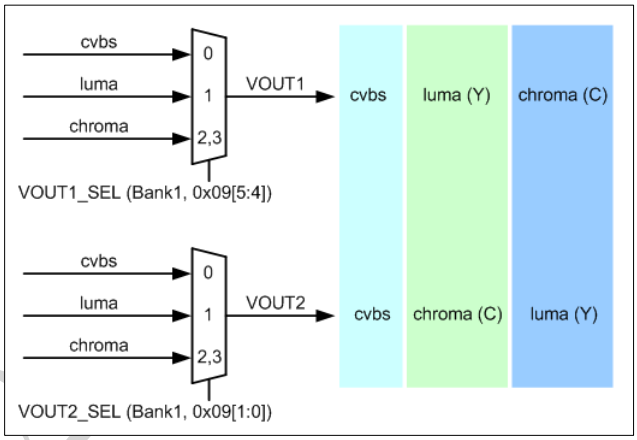


Figure 4.8. Output Muxing

4.8. Field Enhancer

: In DVR application area, a part of visual information from multi-channel is sometimes saved due to storage efficiency or limitation of compression device. In this case, saved images are not continuous fields but even field or odd field. Because stored images are not continuous fields, image quality is deteriorated when stored images are play-back. Field enhancer is used to overcome this problem. Fig. 4.9. shows operation pictures when field enhancer is on/off.

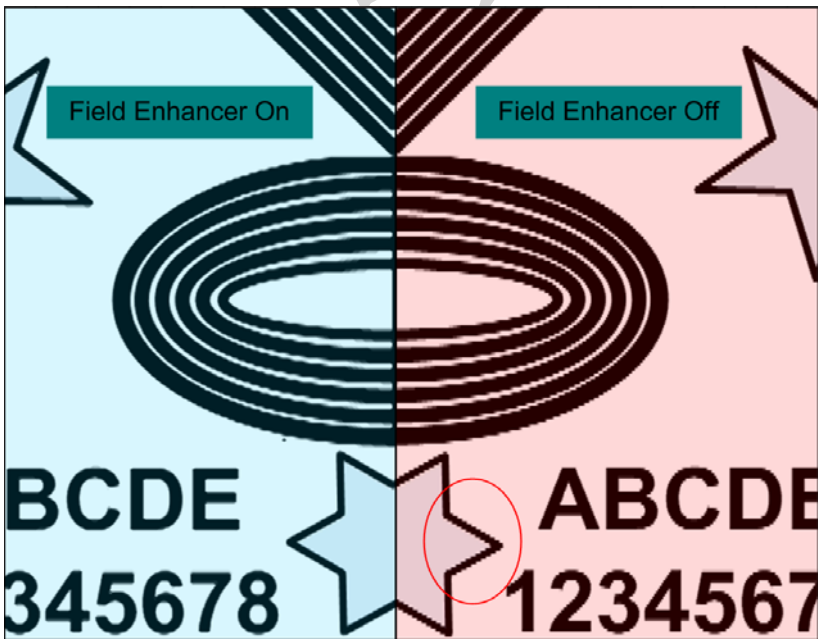


Figure 4.9. Field Enhancer Output

5. I2C Wire Interface

: I2C interface requires 2 wires, SCL (I2C clock) & SDA (I2C R/W data). NVP1114A provides special device ID as slave addresses (SA0,SA1). So any combination of 7 bit can be defined as slave address of NVP1114A. The Figure 5.1 shows read/write protocol of I2C interface. The 1-st byte transfers slave address and read/write information. For write mode, the 2nd byte transfers base register index and the 3rd byte transfers data to be written. For read mode, reading data is transferred during 2nd byte period. The brief I2C interface protocol is shown in Figure 5.2

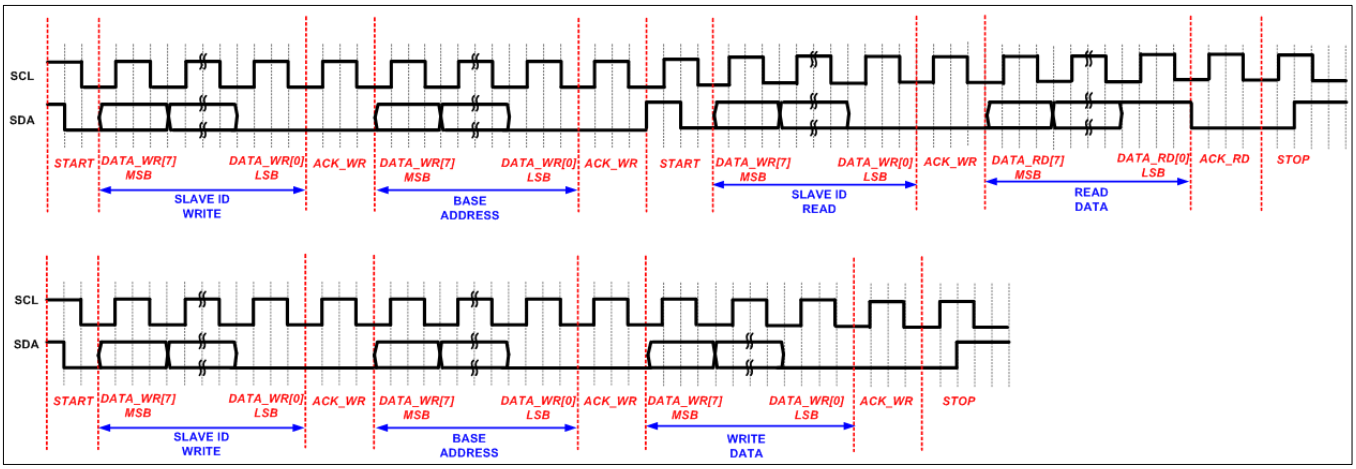


Figure 5.1. I2C Timing Diagram

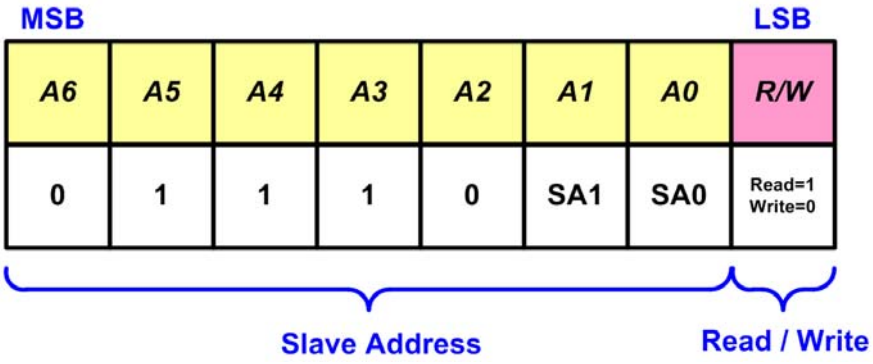


Figure 5.2. I2C Slave Address Configuration

5.1. Bank Operation

: The register bank of NVP1114A is divided into Bank0 and Bank1. The address of bank selector is 0xFF, and if the contents of this register is 0x00, Bank0 is accessible. On the other hand, if the contents of bank selector is 0x01, Bank1 is accessible. Notice that do not change fixed register value. If you change these values, you may suffer from unintended operation of NVP1114A.

6. Register Description

-Values in the box is fixed. Do not make them changed!

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0x00	NOVID_04	NOVID_03	NOVID_02	NOVID_01	MUTE_04	MUTE_03	MUTE_02	MUTE_01	READ ONLY
	0x01	ALARM_04	ALARM_03	ALARM_02	ALARM_01	MOTION_04	MOTION_03	MOTION_02	MOTION_01	READ ONLY
	0x02	BW_04	BW_03	BW_02	BW_01	FSCLOCK_04	FSCLOCK_03	FSCLOCK_02	FSCLOCK_01	READ ONLY
	0x03	AGCSTA_04	AGCSTA_03	AGCSTA_02	AGCSTA_01	CMPSTA_04	CMPSTA_03	CMPSTA_02	CMPSTA_01	READ ONLY
	0x04	LINENUM_04	LINENUM_03	LINENUM_02	LINENUM_01	FLD_04	FLD_03	FLD_02	FLD_01	READ ONLY
	0x05	VPORT1_SEQ2				VPORT1_SEQ1				0x10
	0x06	VPORT1_SEQ4				VPORT1_SEQ3				0x32
	0x07	VPORT2_SEQ2				VPORT2_SEQ1				0x10
	0x08	VPORT2_SEQ4				VPORT2_SEQ3				0x32
	0x09	VPORT3_SEQ2				VPORT3_SEQ1				0x10
	0x0A	VPORT3_SEQ4				VPORT3_SEQ3				0x32
	0x0B	VPORT4_SEQ2				VPORT4_SEQ1				0x10
	0x0C	VPORT4_SEQ4				VPORT4_SEQ3				0x32
	0x0D	0	0	0	STA_CLEAR_4	STA_CLEAR_3	STA_CLEAR_2	STA_CLEAR_1	STA_CLEAR_0	0x00
	0x0E	0	0	0	0	0	0	0	0	0x00
	0x0F	0	0	0	STA_MODE_4	STA_MODE_3	STA_MODE_2	STA_MODE_1	STA_MODE_0	0x00
	0x10	0	0	0	0	0	0	0	0	0x00
	0x11	1	1	1	0	1	1	1	1	0xEF
	0x12	1	1	1	1	1	1	1	1	0xFF
	0x13	1	1	1	1	1	1	1	1	0xFF
	0x14	1	1	1	1	1	1	1	1	0xFF
	0x19	0	0	0	0	0	0	0	0	0x00
	0x1A	0	0	0	0	0	0	0	0	0x00
	0x1B	DEV_ID								0x72
	0x1C	0	0	0	0	REV_ID				0x00
	0x1D	0	0	0	0	0	0	0	0	0x00
	0x1E	0	0	0	0	0	0	0	0	0x00
	0x1F	0	0	0	0	0	0	0	0	0x00

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0x20/30/40/50	BSF_MODE		AUTO	VIDEO FORMAT					0x60
0x21/31/41/51	BRIGHTNESS								0x00
0x22/32/42/52	CONTRAST								0xAB
0x23/33/43/53	HUE								0x02
0x24/34/44/54	SATURATION								0x90
0x25/35/45/55	U_GAIN								0x00
0x26/36/46/56	V_GAIN								0x00
0x27/37/47/57	U_OFFSET				V_OFFSET				0x00
0x28/38/48/58	0	0	0	0	Y_FIR_MODE				0x06
0x29/39/49/59	HSYNC_INV	VSYNC_INV	FLD_INV	Y_DELAY					0x10
0x2A/3A/4A/5A	H_DELAY								0x95
0x2B/3B/4B/5B	V_DELAY								0x00
0x2C/3C/4C/5C	HBLK_END								0x00
0x2D/3D/4D/5D	VBLK_END								0x8A
0x2E/3E/4E/5E	0	CH_CLK_SEL			CLK_DELAY_SEL				0x10
0x2F/3F/4F/5F	CHID_PUT				0	CH_OUT_SEL			0x00/11/22/33
0x60	1	1	0	1	0	0	0	0	0xD0
0x61	1	0	0	0	0	0	0	AFE_FIR_MODE	0x80
0x62	A_INP_GAIN_CTRL								0x40
0x63	0	1	1	1	1	1	0	0	0x7C
0x64	1	0	0	1	1	1	1	1	0x9F
0x65	0	0	0	0	0	0	0	0	0x00
0x66	0	0	1	0	0	0	0	0	0x20
0x67	0	1	0	0	0	0	0	0	0x40
0x68	1	0	0	0	0	0	0	0	0x80
0x69	0	1	0	1	0	0	0	0	0x50
0x6A	0	0	1	1	1	0	0	0	0x38
0x6B	0	0	0	0	1	1	1	1	0x0F
0x6C	0	0	0	0	1	1	0	0	0x0C
0x6D	0	0	0	0	COMB_MODE				0x01
0x6E	0	0	0	1	0	1	0	1	0x15
0x6F	0	0	0	0	1	0	1	0	0x0A

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0x70	1	0	0	0	0	0	0	0	0x80
	0x71	U_OFFSET2				V_OFFSET2				0x23
	0x72	1	0	0	0	1	0	0	0	0x88
	0x73	0	0	0	0	0	1	0	0	0x04
	0x74	0	0	1	0	1	0	1	0	0x2A
	0x75	FSC_LOCK_MODE				FSC_LOCK_SPD				0xCC
	0x76	1	1	1	1	0	0	0	0	0xF0
	0x77	ACC_OFF	0	1	0	ACC_GAIN_SPD				0x2F
	0x78	0	1	0	1	0	1	1	1	0x57
	0x79	FLD_DET_SPD		0	0	NOVID_MODE				0x43
	0x7A	0	0	NOVID_SPD						0x10
	0x7B	H_SHARPNESS				V_SHARPNESS				0x88
	0x7C	PAL_CM_OFF	IF_FIR_SEL			0	0	CLPF_SEL		0x82
	0x7D	0	1	CTI_GAIN		C_KILL				0x63
	0x7E	0	0	0	0	0	0	0	1	0x01
	0x7F	0	0	0	0	0	0	0	0	0x00
	0x80	1	0	0	0	0	0	0	0	0x80
	0x81	0	0	0	0	0	0	0	0	0x00
	0x82	0	0	0	0	0	0	0	0	0x00
	0x83	BGD_COL				DATA_OUT_MODE				0x81
	0x84	0	0	0	0	NOVID_INF_IN	CHID_TYPE			0x01
	0x85	OUT_DATA_INV				0	0	0	0	0x00
	0x86	0	0	0	0	0	0	0	0	0x00
	0x87	0	0	0	0	0	0	0	0	0x00
	0x88	0	0	0	0	0	0	0	VPLL_C	0x00
	0x89	VPLL_OD[3:0]				VPLL_OFF	VPLL_TST		VPLL_RST	0x20
	0x8A	VPLL_M[8]	VPLL_BP	VPLL_OE	VPLL_N					0x04
	0x8B	VPLL_M[7:0]								0x2E
	0x8C	0	0	0	0	0	0	0	0	0x00
	0x8D	0	0	1	1	0	0	0	0	0x30
	0x8E	1	0	1	1	1	0	0	0	0xB8
	0x8F	0	0	0	0	0	0	0	1	0x01

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0x90	0	0	0	0	0	1	1	0	0x06
	0x91	0	0	0	0	0	1	1	0	0x06
	0x92	0	0	0	1	0	0	0	1	0x11
	0x93	HPLL_OFF	0	1	1	1	0	0	1	0xB9
	0x94	1	0	1	1	0	0	1	0	0xB2
	0x95	0	0	0	0	0	1	0	1	0x05
	0x96	0	0	0	0	0	0	0	0	0x00
	0x97	0	0	1	0	1	0	0	0	0x28
	0x98	0	1	0	1	0	0	0	0	0x50
	0x99	0	1	0	1	0	0	WPD_MAX[9:8]		0x51
	0x9A	WPD_MAX[7:0]								0xB5
	0x9B	WPD_SEL								0x13
	0x9C	WPD_SPD								0x03
	0x9D	WPD_CTRL								0x22
	0x9E	1	1	1	1	1	1	1	1	0xFF
	0x9F	0	0	0	0	0	0	0	0	0x00
	0xA0	0	0	0	0	0	0	0	0	0x00
	0xA1	A_ADC_PW0	A_ADC_PW1	A_ADC_PW2	A_ADC_PW3	0	CAS_PB	RM_PB_PIN	PB_RM_PIN	0x00
	0xA2	A_ADC_PWDN	A_DAC_PWDN	1	0	TRANS_MODE	CAS_LINK	CAS_PIN	0	0x22
	0xA3	AIGAIN1				AIGAIN2				0x88
	0xA4	AIGAIN3				AIGAIN4				0x88
	0xA5	RM_MASTER	M_RLSWAP	RM_SSP	RM_BITRATE	RM_CLK	RM_SAMRATE	RM_BITWID	RM_SYNC	0x84
	0xA6	RM_LAW_SEL		CHIP_STAGE		CASCADE_MODE	R_ADATM	R_MULTCH		0x33
	0xA7	R_SEQ_0				R_SEQ_1				0x01
	0xA8	R_SEQ_2				R_SEQ_3				0x23
	0xA9	R_SEQ_4				R_SEQ_5				0x45
	0xAA	R_SEQ_6				R_SEQ_7				0x67
	0xAB	R_SEQ_8				R_SEQ_9				0x89
	0xAC	R_SEQ_A				R_SEQ_B				0xAB
	0xAD	R_SEQ_C				R_SEQ_D				0xCD
	0xAE	R_SEQ_E				R_SEQ_F				0xEF
	0xAF	PB_MASTER	0	PB_SSP	PB_BITRATE	PB_CLK	PB_SAMRATE	PB_BITWID	PB_SYNC	0x04

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0xB0	PB_LAW_SEL		MIX_GAIN_MODE	0	0	0	0	0	0x00
	0xB1	MIX_GAIN1				MIX_GAIN2				0x88
	0xB2	MIX_GAIN3				MIX_GAIN4				0x88
	0xB3	AOGAIN				MIX_GAINP				0x88
	0xB4	0	0	0	MIX_OUTSEL					0x14
	0xB5	ADET_MODE	ADET_FILT			ADET_0	ADET_1	ADET_2	ADET_3	0x0F
	0xB6	ADET_TH0				ADET_TH1				0xAA
	0xB7	ADET_TH2				ADET_TH3				0xAA
	0xB8	PB_SEL				MUX_DELAY		DC0		0x02
	0xB9	DC1								0x00
	0xBA	1	0	0	0	0	0	0	0	0x80
	0xBB	0	0	0	0	0	0	0	0	0x00
	0xBC	0	0	0	0	0	0	0	0	0x00
	0xBD	1	1	0	0	1	0	0	1	0xC9
	0xBE	0	0	0	0	1	1	1	1	0x0F
	0xBF	0	0	0	1	1	0	0	0	0x18
	0xC0	ID_ON1	BLK_OPER1	SUB_SAM1	SCALE_SEL1	SYNC_ORG1	UP1	HBYPASS1	VBYPASS1	0x13
	0xC1	ID_ON2	BLK_OPER2	SUB_SAM2	SCALE_SEL2	SYNC_ORG2	UP2	HBYPASS2	VBYPASS2	0x13
	0xC2	ID_ON3	BLK_OPER3	SUB_SAM3	SCALE_SEL3	SYNC_ORG3	UP3	HBYPASS3	VBYPASS3	0x13
	0xC3	ID_ON4	BLK_OPER4	SUB_SAM4	SCALE_SEL4	SYNC_ORG4	UP4	HBYPASS4	VBYPASS4	0x13
	0xC4	H_DEL1				H_DEL2				0x00
	0xC5	H_DEL3				H_DEL4				0x00
	0xC6	H_DTO1[7:0]								0x71
	0xC7	H_DTO2[7:0]								0x71
	0xC8	H_DTO3[7:0]								0x71
	0xC9	H_DTO4[7:0]								0x71
	0xCA	H_DTO1[15:8]								0x1C
	0xCB	H_DTO2[15:8]								0x1C
	0xCC	H_DTO3[15:8]								0x1C
	0xCD	H_DTO4[15:8]								0x1C
	0xCE	V_DTO1[19:16]				H_DTO1[19:16]				0x87
	0xCF	V_DTO2[19:16]				H_DTO2[19:16]				0x87

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0xD0	V_DTO3[19:16]				H_DTO3[19:16]				0x87
	0xD1	V_DTO4[19:16]				H_DTO4[19:16]				0x87
	0xD2	V_DTO1[7:0]								0x00
	0xD3	V_DTO2[7:0]								0x00
	0xD4	V_DTO3[7:0]								0x00
	0xD5	V_DTO4[7:0]								0x00
	0xD6	V_DTO1[15:8]								0x00
	0xD7	V_DTO2[15:8]								0x00
	0xD8	V_DTO3[15:8]								0x00
	0xD9	V_DTO4[15:8]								0x00
	0xDA	BLK_PKG[31:24]								0x80
	0xDB	BLK_PKG[23:16]								0x10
	0xDC	BLK_PKG[15:8]								0x80
	0xDD	BLK_PKG[7:0]								0x10
	0xDE	0	0	0	0	0	0	0	0	0x00
	0xDF	0	0	0	0	0	0	0	0	0x00
	0xE1	0	0	0	0	0	0	0	0	0x00
	0xE2	0	0	0	0	0	0	0	0	0x00
	0xE3	0	0	0	0	0	0	0	0	0x00
	0xE4	GPO1_INV	GPO1_OUT_SEL			GPO2_INV	GPO2_OUT_SEL			0x00
	0xE5	GPO3_INV	GPO3_OUT_SEL			0	0	0	0	0x00
	0xE6	0	0	0	0	0	0	0	0	0x00
	0xE7	0	0	0	0	0	0	0	0	0x00
	0xE8	0	0	0	1	0	0	0	0	0x10
	0xE9	0	0	0	1	0	0	0	1	0x11
	0xEA	0	0	0	0	0	0	0	1	0x01
	0xEB	0	1	0	0	0	0	0	0	0x40
	0xEC	0	0	0	0	0	0	0	0	0x00
	0xED	0	0	0	0	0	0	0	0	0x00
	0xEE	0	0	0	0	0	0	0	0	0x00
	0xEF	0	0	0	0	0	0	0	0	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0xF0	VAFE_PDN_04	VAFE_PDN_03	VAFE_PDN_02	VAFE_PDN_01	ENC_CLK_SEL		VDAC_CLK_SEL		0x00
	0xF1	0	0	0	0	0	0	0	0	0x00
	0xF2	DIV_SRC_SEL	DEC_27CLK_SEL			0	0	0	0	0xA0
	0xF3	AADC_CLK_SEL	0	0	ADAC_CLK_SEL	DEC_108CLK_SEL	AUD_54CLK_SEL			0x04
	0xF4	0	0	0	0	0	0	0	0	0x00
	0xF5	0	0	0	0	0	0	0	0	0x00
	0xF6	CLK108_PROCESS	0	VDO4_OEB	VDO1_OEB	VDO3_OEB	VDO2_OEB	VDAC1_OFF	VDAC2_OFF	0x80
	0xF7	0	1	0	1	1	0	0	0	0x58
	0xF8	0	1	1	1	1	0	1	1	0x7B
	0xF9	0	DATA_CATCH			0	0	0	0	0x20
	0xFA	0	0	0	0	0	0	0	0	0x00
	0xFB	1	0	0	0	0	0	0	0	0x80
	0xFC	1	0	0	0	0	0	0	0	0x80
	0xFD	0	1	0	0	1	0	0	1	0x49
	0xFE	0	0	1	1	0	1	1	1	0x37
	0xFF	0	0	0	0	0	0	0	BANK_SEL	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 1	0x00	BW_ON	CBAR_ON	PED	0	LNFMT	V_ALTER	FSC_SEL		0x00
	0x01	PATTERN_TYPE				1	0	CFIR_SEL		0x08
	0x02	HDELAY								0x00
	0x03	VDELAY								0x00
	0x04	BUST_GAIN								0x86
	0x05	SYNC_GAIN								0x7A
	0x06	LUMA_GAIN								0x7E
	0x07	CHMA_GAIN								0x7A
	0x08	0	0	0	FLD_ENH_ON	0	0	SYNC_FIR_SEL		0x00
	0x09	0	0	VOUT1_SEL		0	0	VOUT2_SEL		0x00
	0x10	FE_EN_WIN_HR_01								0x00
	0x11	FE_EN_WIN_HL_01								0x00
	0x12	FE_EN_WIN_VB_01								0x00
	0x13	FE_EN_WIN_VT_01								0x00
	0x14	FE_EN_WIN_HR_02								0x00
	0x15	FE_EN_WIN_HL_02								0x00
	0x16	FE_EN_WIN_VB_02								0x00
	0x17	FE_EN_WIN_VT_02								0x00
	0x18	FE_EN_WIN_HR_03								0x00
	0x19	FE_EN_WIN_HL_03								0x00
	0x1A	FE_EN_WIN_VB_03								0x00
	0x1B	FE_EN_WIN_VT_03								0x00
	0x1C	FE_EN_WIN_HR_04								0x00
	0x1D	FE_EN_WIN_HL_04								0x00
	0x1E	FE_EN_WIN_VB_04								0x00
	0x1F	FE_EN_WIN_VT_04								0x00
	0x20	FE_EN_WIN_HR_05								0x00
	0x21	FE_EN_WIN_HL_05								0x00
	0x22	FE_EN_WIN_VB_05								0x00
	0x23	FE_EN_WIN_VT_05								0x00
	0x24	FE_EN_WIN_HR_06								0x00
	0x25	FE_EN_WIN_HL_06								0x00
	0x26	FE_EN_WIN_VB_06								0x00
	0x27	FE_EN_WIN_VT_06								0x00
	0x28	FE_EN_WIN_HR_07								0x00
	0x29	FE_EN_WIN_HL_07								0x00
	0x2A	FE_EN_WIN_VB_07								0x00
	0x2B	FE_EN_WIN_VT_07								0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 1	0x2C	FE_EN_WIN_HR_08								0x00
	0x2D	FE_EN_WIN_HL_08								0x00
	0x2E	FE_EN_WIN_VB_08								0x00
	0x2F	FE_EN_WIN_VT_08								0x00
	0x30	FE_EN_WIN_HR_09								0x00
	0x31	FE_EN_WIN_HL_09								0x00
	0x32	FE_EN_WIN_VB_09								0x00
	0x33	FE_EN_WIN_VT_09								0x00
	0x34	FE_EN_WIN_HR_10								0x00
	0x35	FE_EN_WIN_HL_10								0x00
	0x36	FE_EN_WIN_VB_10								0x00
	0x37	FE_EN_WIN_VT_10								0x00
	0x38	FE_EN_WIN_HR_11								0x00
	0x39	FE_EN_WIN_HL_11								0x00
	0x3A	FE_EN_WIN_VB_11								0x00
	0x3B	FE_EN_WIN_VT_11								0x00
	0x3C	FE_EN_WIN_HR_12								0x00
	0x3D	FE_EN_WIN_HL_12								0x00
	0x3E	FE_EN_WIN_VB_12								0x00
	0x3F	FE_EN_WIN_VT_12								0x00
	0x40	FE_EN_WIN_HR_13								0x00
	0x41	FE_EN_WIN_HL_13								0x00
	0x42	FE_EN_WIN_VB_13								0x00
	0x43	FE_EN_WIN_VT_13								0x00
	0x44	FE_EN_WIN_HR_14								0x00
	0x45	FE_EN_WIN_HL_14								0x00
	0x46	FE_EN_WIN_VB_14								0x00
	0x47	FE_EN_WIN_VT_14								0x00
	0x48	FE_EN_WIN_HR_15								0x00
	0x49	FE_EN_WIN_HL_15								0x00
	0x4A	FE_EN_WIN_VB_15								0x00
	0x4B	FE_EN_WIN_VT_15								0x00
	0x4C	FE_EN_WIN_HR_16								0x00
	0x4D	FE_EN_WIN_HL_16								0x00
	0x4E	FE_EN_WIN_VB_16								0x00
	0x4F	FE_EN_WIN_VT_16								0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 1	0x50	FE_DIS_WIN_HR_01								0x00
	0x51	FE_DIS_WIN_HL_01								0x00
	0x52	FE_DIS_WIN_VB_01								0x00
	0x53	FE_DIS_WIN_VT_01								0x00
	0x54	FE_DIS_WIN_HR_02								0x00
	0x55	FE_DIS_WIN_HL_02								0x00
	0x56	FE_DIS_WIN_VB_02								0x00
	0x57	FE_DIS_WIN_VT_02								0x00
	0x58	FE_DIS_WIN_HR_03								0x00
	0x59	FE_DIS_WIN_HL_03								0x00
	0x5A	FE_DIS_WIN_VB_03								0x00
	0x5B	FE_DIS_WIN_VT_03								0x00
	0x5C	FE_DIS_WIN_HR_04								0x00
	0x5D	FE_DIS_WIN_HL_04								0x00
	0x5E	FE_DIS_WIN_VB_04								0x00
	0x5F	FE_DIS_WIN_VT_04								0x00
	0x60	FE_DIS_WIN_HR_05								0x00
	0x61	FE_DIS_WIN_HL_05								0x00
	0x62	FE_DIS_WIN_VB_05								0x00
	0x63	FE_DIS_WIN_VT_05								0x00
	0x64	FE_DIS_WIN_HR_06								0x00
	0x65	FE_DIS_WIN_HL_06								0x00
	0x66	FE_DIS_WIN_VB_06								0x00
	0x67	FE_DIS_WIN_VT_06								0x00
	0x68	FE_DIS_WIN_HR_07								0x00
	0x69	FE_DIS_WIN_HL_07								0x00
	0x6A	FE_DIS_WIN_VB_07								0x00
	0x6B	FE_DIS_WIN_VT_07								0x00
	0x6C	FE_DIS_WIN_HR_08								0x00
	0x6D	FE_DIS_WIN_HL_08								0x00
	0x6E	FE_DIS_WIN_VB_08								0x00
	0x6F	FE_DIS_WIN_VT_08								0x00
	0x70	FE_DIS_WIN_HR_09								0x00
	0x71	FE_DIS_WIN_HL_09								0x00
	0x72	FE_DIS_WIN_VB_09								0x00
	0x73	FE_DIS_WIN_VT_09								0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 1	0x74	FE_DIS_WIN_HR_10								0x00
	0x75	FE_DIS_WIN_HL_10								0x00
	0x76	FE_DIS_WIN_VB_10								0x00
	0x77	FE_DIS_WIN_VT_10								0x00
	0x78	FE_DIS_WIN_HR_11								0x00
	0x79	FE_DIS_WIN_HL_11								0x00
	0x7A	FE_DIS_WIN_VB_11								0x00
	0x7B	FE_DIS_WIN_VT_11								0x00
	0x7C	FE_DIS_WIN_HR_12								0x00
	0x7D	FE_DIS_WIN_HL_12								0x00
	0x7E	FE_DIS_WIN_VB_12								0x00
	0x7F	FE_DIS_WIN_VT_12								0x00
	0x80	FE_DIS_WIN_HR_13								0x00
	0x81	FE_DIS_WIN_HL_13								0x00
	0x82	FE_DIS_WIN_VB_13								0x00
	0x83	FE_DIS_WIN_VT_13								0x00
	0x84	FE_DIS_WIN_HR_14								0x00
	0x85	FE_DIS_WIN_HL_14								0x00
	0x86	FE_DIS_WIN_VB_14								0x00
	0x87	FE_DIS_WIN_VT_14								0x00
	0x88	FE_DIS_WIN_HR_15								0x00
	0x89	FE_DIS_WIN_HL_15								0x00
	0x8A	FE_DIS_WIN_VB_15								0x00
	0x8B	FE_DIS_WIN_VT_15								0x00
	0x8C	FE_DIS_WIN_HR_16								0x00
	0x8D	FE_DIS_WIN_HL_16								0x00
	0x8E	FE_DIS_WIN_VB_16								0x00
	0x8F	FE_DIS_WIN_VT_16								0x00
	0x90	0	0	0	INTP_MODE	0	0	FE_FLD_SEL	YC_CLIP	0x00
	0x91	FE_DIFF_REF								0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 1	0xA1	0	0	0	MOTION_OFF_01	0	0	MOTION_PIC_01		0x03
	0xA2	MOD_TSEN_01								0x6B
	0xA3	0	0	0	MOTION_OFF_02	0	0	MOTION_PIC_02		0x03
	0xA4	MOD_TSEN_02								0x6B
	0xA5	0	0	0	MOTION_OFF_03	0	0	MOTION_PIC_03		0x03
	0xA6	MOD_TSEN_03								0x6B
	0xA7	0	0	0	MOTION_OFF_04	0	0	MOTION_PIC_04		0x03
	0xA8	MOD_TSEN_04								0x6B
	0xA9	MOD_PSEN_01		MOD_PSEN_02		MOD_PSEN_03		MOD_PSEN_04		0xAA
	0xB0	CH1_MOD_01	CH1_MOD_02	CH1_MOD_03	CH1_MOD_04	CH1_MOD_05	CH1_MOD_06	CH1_MOD_07	CH1_MOD_08	0xFF
	0xB1	CH1_MOD_09	CH1_MOD_10	CH1_MOD_11	CH1_MOD_12	CH1_MOD_13	CH1_MOD_14	CH1_MOD_15	CH1_MOD_16	0xFF
	0xB2	CH1_MOD_17	CH1_MOD_18	CH1_MOD_19	CH1_MOD_20	CH1_MOD_21	CH1_MOD_22	CH1_MOD_23	CH1_MOD_24	0xFF
	0xB3	CH1_MOD_25	CH1_MOD_26	CH1_MOD_27	CH1_MOD_28	CH1_MOD_29	CH1_MOD_30	CH1_MOD_31	CH1_MOD_32	0xFF
	0xB4	CH1_MOD_33	CH1_MOD_34	CH1_MOD_35	CH1_MOD_36	CH1_MOD_37	CH1_MOD_38	CH1_MOD_39	CH1_MOD_40	0xFF
	0xB5	CH1_MOD_41	CH1_MOD_42	CH1_MOD_43	CH1_MOD_44	CH1_MOD_45	CH1_MOD_46	CH1_MOD_47	CH1_MOD_48	0xFF
	0xB6	CH1_MOD_49	CH1_MOD_50	CH1_MOD_51	CH1_MOD_52	CH1_MOD_53	CH1_MOD_54	CH1_MOD_55	CH1_MOD_56	0xFF
	0xB7	CH1_MOD_57	CH1_MOD_58	CH1_MOD_59	CH1_MOD_60	CH1_MOD_61	CH1_MOD_62	CH1_MOD_63	CH1_MOD_64	0xFF
	0xB8	CH2_MOD_01	CH2_MOD_02	CH2_MOD_03	CH2_MOD_04	CH2_MOD_05	CH2_MOD_06	CH2_MOD_07	CH2_MOD_08	0xFF
	0xB9	CH2_MOD_09	CH2_MOD_10	CH2_MOD_11	CH2_MOD_12	CH2_MOD_13	CH2_MOD_14	CH2_MOD_15	CH2_MOD_16	0xFF
	0xBA	CH2_MOD_17	CH2_MOD_18	CH2_MOD_19	CH2_MOD_20	CH2_MOD_21	CH2_MOD_22	CH2_MOD_23	CH2_MOD_24	0xFF
	0xBB	CH2_MOD_25	CH2_MOD_26	CH2_MOD_27	CH2_MOD_28	CH2_MOD_29	CH2_MOD_30	CH2_MOD_31	CH2_MOD_32	0xFF
	0xBC	CH2_MOD_33	CH2_MOD_34	CH2_MOD_35	CH2_MOD_36	CH2_MOD_37	CH2_MOD_38	CH2_MOD_39	CH2_MOD_40	0xFF
	0xBD	CH2_MOD_41	CH2_MOD_42	CH2_MOD_43	CH2_MOD_44	CH2_MOD_45	CH2_MOD_46	CH2_MOD_47	CH2_MOD_48	0xFF
	0xBE	CH2_MOD_49	CH2_MOD_50	CH2_MOD_51	CH2_MOD_52	CH2_MOD_53	CH2_MOD_54	CH2_MOD_55	CH2_MOD_56	0xFF
	0xBF	CH2_MOD_57	CH2_MOD_58	CH2_MOD_59	CH2_MOD_60	CH2_MOD_61	CH2_MOD_62	CH2_MOD_63	CH2_MOD_64	0xFF
	0xC0	CH3_MOD_01	CH3_MOD_02	CH3_MOD_03	CH3_MOD_04	CH3_MOD_05	CH3_MOD_06	CH3_MOD_07	CH3_MOD_08	0xFF
	0xC1	CH3_MOD_09	CH3_MOD_10	CH3_MOD_11	CH3_MOD_12	CH3_MOD_13	CH3_MOD_14	CH3_MOD_15	CH3_MOD_16	0xFF
	0xC2	CH3_MOD_17	CH3_MOD_18	CH3_MOD_19	CH3_MOD_20	CH3_MOD_21	CH3_MOD_22	CH3_MOD_23	CH3_MOD_24	0xFF
	0xC3	CH3_MOD_25	CH3_MOD_26	CH3_MOD_27	CH3_MOD_28	CH3_MOD_29	CH3_MOD_30	CH3_MOD_31	CH3_MOD_32	0xFF
	0xC4	CH3_MOD_33	CH3_MOD_34	CH3_MOD_35	CH3_MOD_36	CH3_MOD_37	CH3_MOD_38	CH3_MOD_39	CH3_MOD_40	0xFF
	0xC5	CH3_MOD_41	CH3_MOD_42	CH3_MOD_43	CH3_MOD_44	CH3_MOD_45	CH3_MOD_46	CH3_MOD_47	CH3_MOD_48	0xFF
	0xC6	CH3_MOD_49	CH3_MOD_50	CH3_MOD_51	CH3_MOD_52	CH3_MOD_53	CH3_MOD_54	CH3_MOD_55	CH3_MOD_56	0xFF
	0xC7	CH3_MOD_57	CH3_MOD_58	CH3_MOD_59	CH3_MOD_60	CH3_MOD_61	CH3_MOD_62	CH3_MOD_63	CH3_MOD_64	0xFF
	0xC8	CH4_MOD_01	CH4_MOD_02	CH4_MOD_03	CH4_MOD_04	CH4_MOD_05	CH4_MOD_06	CH4_MOD_07	CH4_MOD_08	0xFF
	0xC9	CH4_MOD_09	CH4_MOD_10	CH4_MOD_11	CH4_MOD_12	CH4_MOD_13	CH4_MOD_14	CH4_MOD_15	CH4_MOD_16	0xFF
	0xCA	CH4_MOD_17	CH4_MOD_18	CH4_MOD_19	CH4_MOD_20	CH4_MOD_21	CH4_MOD_22	CH4_MOD_23	CH4_MOD_24	0xFF
	0xCB	CH4_MOD_25	CH4_MOD_26	CH4_MOD_27	CH4_MOD_28	CH4_MOD_29	CH4_MOD_30	CH4_MOD_31	CH4_MOD_32	0xFF
	0xCC	CH4_MOD_33	CH4_MOD_34	CH4_MOD_35	CH4_MOD_36	CH4_MOD_37	CH4_MOD_38	CH4_MOD_39	CH4_MOD_40	0xFF
	0xCD	CH4_MOD_41	CH4_MOD_42	CH4_MOD_43	CH4_MOD_44	CH4_MOD_45	CH4_MOD_46	CH4_MOD_47	CH4_MOD_48	0xFF
	0xCE	CH4_MOD_49	CH4_MOD_50	CH4_MOD_51	CH4_MOD_52	CH4_MOD_53	CH4_MOD_54	CH4_MOD_55	CH4_MOD_56	0xFF
	0xCF	CH4_MOD_57	CH4_MOD_58	CH4_MOD_59	CH4_MOD_60	CH4_MOD_61	CH4_MOD_62	CH4_MOD_63	CH4_MOD_64	0xFF

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0x00	NOVID_04	NOVID_03	NOVID_02	NOVID_01	MUTE_04	MUTE_03	MUTE_02	MUTE_01	READ ONLY
	0x01	ALARM_04	ALARM_03	ALARM_02	ALARM_01	MOTION_04	MOTION_03	MOTION_02	MOTION_01	READ ONLY
	0x02	BW_04	BW_03	BW_02	BW_01	FSCLOCK_04	FSCLOCK_03	FSCLOCK_02	FSCLOCK_01	READ ONLY
	0x03	AGCSTA_04	AGCSTA_03	AGCSTA_02	AGCSTA_01	CMPSTA_04	CMPSTA_03	CMPSTA_02	CMPSTA_01	READ ONLY
	0x04	LINENUM_04	LINENUM_03	LINENUM_02	LINENUM_01	FLD_04	FLD_03	FLD_02	FLD_01	READ ONLY

■ Registers To Show Status (Read Only)

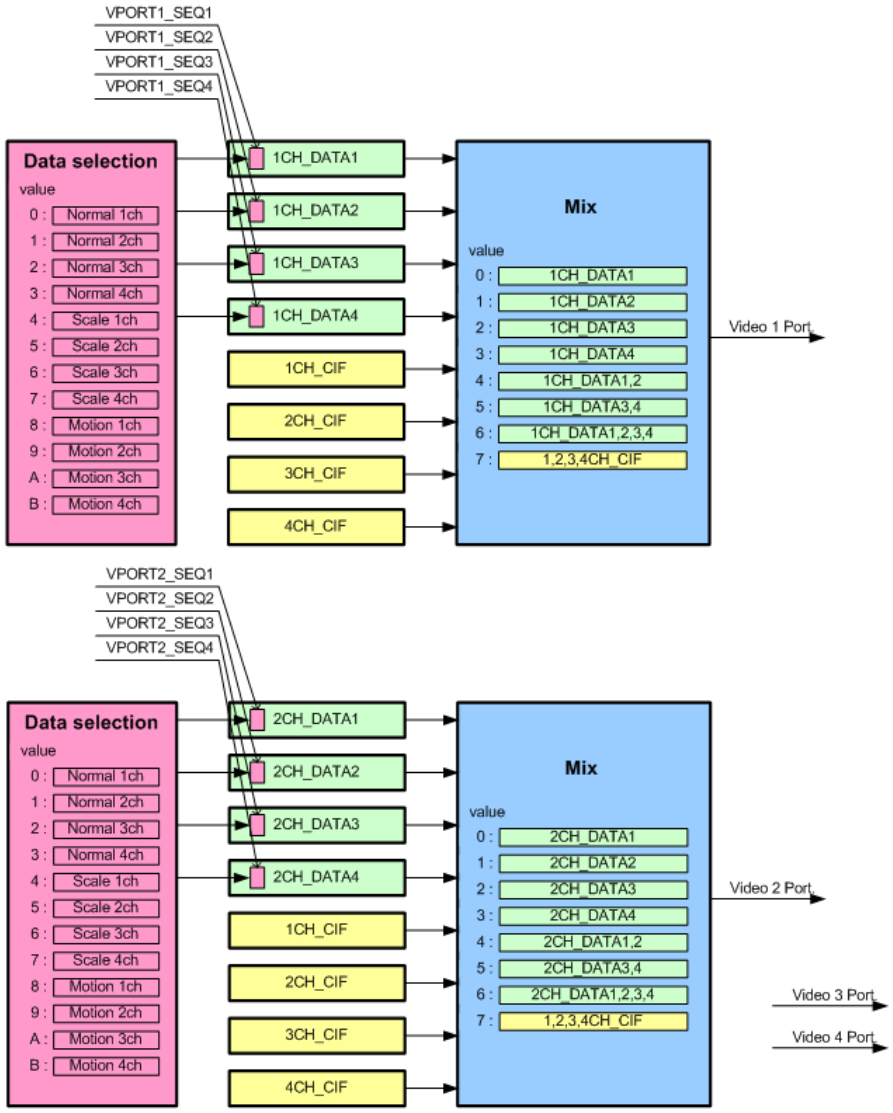
NOVID_0x	: No_video	(0:On Video	1:No Video)
MUTE_0x	: No_audio	(0:On Audio	1:No Audio)
ALARM_0x	: Alarm Status	(0:No Alarm	1:On Alarm)
Motion_0x	: Motion	(0:No Motion	1:On Motion)
BW_0x	: Black-White	(0:Color	1:B/W)
FSC_LOCK_0x	: Lock Status	(0:FSC Unlocked	1:Locked)
AGCSTA_0x	: AGC Stable	(0:AGC Unstable	1:AGC Stable)
CMP_STA_0x	: Clamp Stable	(0:Clamp Unstable	1:Clamp Stable)
LINE_NUM_0x	: Line number	(0:525line	1:625line)
FLD_0x	: Even field	(0:Odd field	1:Even field)

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0x05	VPORT1_SEQ2				VPORT1_SEQ1				0x10
	0x06	VPORT1_SEQ4				VPORT1_SEQ3				0x32
	0x07	VPORT2_SEQ2				VPORT2_SEQ1				0x10
	0x08	VPORT2_SEQ4				VPORT2_SEQ3				0x32
	0x09	VPORT3_SEQ2				VPORT3_SEQ1				0x10
	0x0A	VPORT3_SEQ4				VPORT3_SEQ3				0x32
	0x0B	VPORT4_SEQ2				VPORT4_SEQ1				0x10
	0x0C	VPORT4_SEQ4				VPORT4_SEQ3				0x32

■ Registers To Select Output

VPORTx_SEQx : Select the type of the output video signal through each output port(refer to the picture as below)

0	Normal 1 channel.	1	Normal 2 channel.
2	Normal 3 channel.	3	Normal 4 channel.
4	Scale 1 channel.	5	Scale 2 channel.
6	Scale 3 channel.	7	Scale 4 channel.
8	Motion 1 channel.	9	Motion 2 channel.
A	Motion 3 channel.	B	Motion 4 channel.



ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
BANK 0	0x0D	0	0	0	STA_CLEAR_4	STA_CLEAR_3	STA_CLEAR_2	STA_CLEAR_1	STA_CLEAR_0	0x00
	0x0E	0	0	0	0	0	0	0	0	0x00
	0x0F	0	0	0	STA_MODE_4	STA_MODE_3	STA_MODE_2	STA_MODE_1	STA_MODE_0	0x00
	0x1B	DEV_ID								0x72
	0x1C	0	0	0	0	REV_ID				0x00

■ Registers To Control Signals Of Interrupt

STA_CLEAR_x : Clear the interrupt signal

0 Continue 1 Clear

STA_Mode_x : Make the interrupt signal controlled by STA_CLEAR and STA_POL's registers.

0	No controlled	1	Controlled

DEV_ID : Device ID

REV_ID : Revision ID

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x20/30/40/50	BSF_MODE		AUTO	VIDEO FORMAT					0x60

■ Registers To Control Comb Filter and Video Format

BSF_MODE : Selects the filter to make primary separation of the brightness and color signals.

00	Test Mode	01	Mode1 (For NTSC)
10	Mode2 (For PAL)	11	Test Mode

AUTO : A register to set the Auto Detect Mode On/Off; When the AUTO mode has a high value, the LINE_NUM bit value of the STATUS Register(0x04[7:4]) is to be confirmed to distinguish NTSC-M/J and PAL-B/D/G/H standards. It does not support other standards, and when used in link with the DVR controller, it cannot be used in the NON_REAL_TIME mode.

0	Auto Detect Off	1	Auto Detect On

VIDEO_FORMAT[4:0] : A register to determine the video standards of the input signal

00000	NTSC-M,J	10001	NTSC-4.43
11101	PAL-B,D,G,H,I	10110	PAL-M
11111	PAL-Nc	10101	PAL-60
Others	None		

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x21/31/41/51	BRIGHTNESS								0x00
Bank0, 0x22/32/42/52	CONTRAST								0xAB

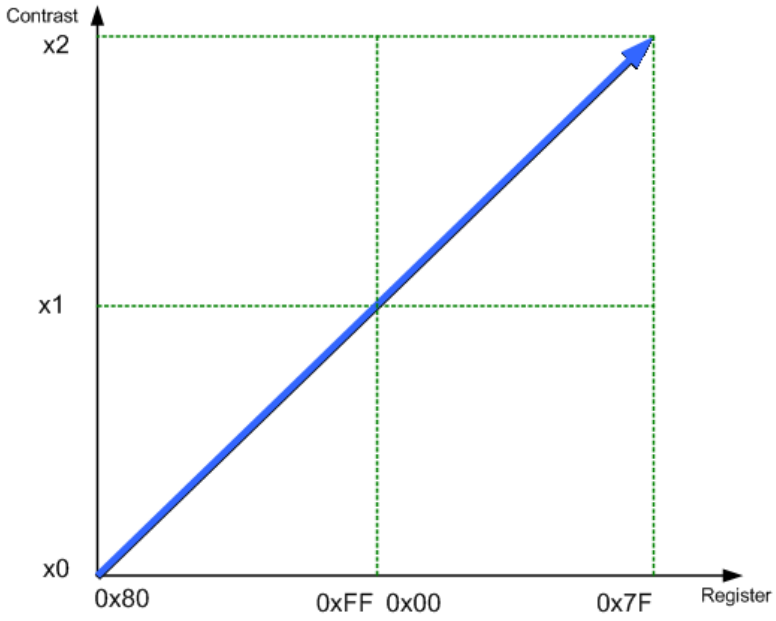
■ Registers To Control A Luminance

BRIGHTNESS : Brightness control; DC level of the Luma signal is adjustable up to -128 ~ +127.
BRIGHTNESS consists of 2's Complements.

00000001	+1	01111111	+127
10000000	-128	11111111	-1

CONTRAST : Contrast control, Gain level of the Luma signal is adjustable up to x2.
MSB represents an integral number while the rest the decimal fraction.

00000000	≒ x1	01111111	≒ x2
10000000	≒ x0	11000000	≒ x0.5



ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x23/33/43/53	HUE								0x02
Bank0, 0x24/34/44/54	SATURATION								0x90
Bank0, 0x25/35/45/55	U_GAIN								0x00
Bank0, 0x26/36/46/56	V_GAIN								0x00

■ Registers To Control A Chrominance

HUE : Color HUE Control Value (360°/256)

00000000	0°	01000000	90°
10000000	180°	11111111	360°

SATURATION : Color Gain Value (Adjustable up to x2)

00000000	≒ x0	10000000	≒ x1
11000000	≒ x1.5	11111111	≒ x2

U_GAIN : U Gain Value (Adjustable up to x2)

00000000	≒ x1	01111111	≒ x2
10000000	≒ x0	11000000	≒ x0.5

V_GAIN : V Gain Value (Adjustable up to x2)

00000000	≒ x1	01111111	≒ x2
10000000	≒ x0	11000000	≒ x0.5

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x27/37/47/57	U_OFFSET				V_OFFSET				0x00

■ Register To Control A Chrominance

U_OFFSET/V_OFFSET : U/V offset Value is adjustable up to ±7. U/V OFFSET consists of 2's Complements.

0001	+1	0111	+7
1000	-8	1111	-1

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x28/38/48/58	0	0	0	0	Y_FIR_MODE				0x06

■ Registers To Control A Sharpness

Y_FIR_MODE[3:2]: Peaking Filter control, Luma 3.5MHz frequency bandwidth amplification

00	bypass	01	2dB
10	3.5dB	11	6dB

Y_FIR_MODE[1:0]: Low Pass Filter control

00	bypass	01	4.2Mhz
10	5.6Mhz	11	7.2Mhz

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x29/39/49/59	HSYNC_INV	VSYNC_INV	FLD_INV	Y_DELAY					0x10

■ Registers To Control Luminance

HSYNC_INV: Horizontal Sync Signal Control, To inverse a phase of hsync.

VSYNC_INV: Vertical Sync Signal Control, To inverse a phase of vsync.

FLD_INV: Field Signal Control, To inverse a phase of even field signal.

Y_DELAY: Y_DELAY Control, controllable between 0 ~ 32.

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x2A/3A/4A/5A	H_DELAY								0x95
Bank0, 0x2B/3B/4B/5B	V_DELAY								0x00
Bank0, 0x2C/3C/4C/5C	HBLK_END								0x00
Bank0, 0x2D/3D/4D/5D	VBLK_END								0x8A

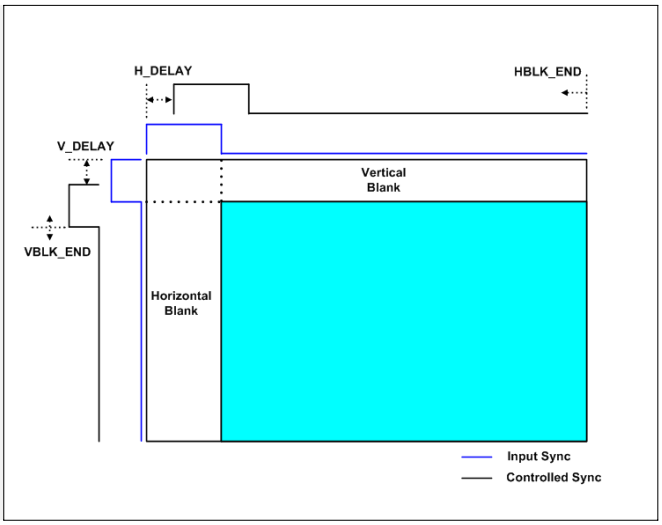
Registers To Control A Timing Of Output

H_DELAY :
Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal.

V_DELAY:
Register to determine the Vertical start position of output image to Vsync extracted in analog input signal.

HBLK_END:
Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed.

VBLK_END:
Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then the Active region is changed.



V_DELAY : signed operation
Reset V Counter(v_counter = 0)
NTSC : When it is 262 ± V_DELAY, V counter is reset.
PAL : When it is 312 ± V_DELAY, V counter is reset.

VBLK_END : vblk_end_old value.
VBLK_END[7:6] =0 : VBLK_END[5:0] + 6
VBLK_END[7:6] =1 : VBLK_END[5:0] + evenfld
VBLK_END[7:6] =2 : VBLK_END[5:0] + (!evenfld)
VBLK_END[7:6] =3 : When it is NTSC and evenfld is 1, if 0xE3[5] is 1, vblk_end_old value is 22 or 23
When it is NTSC and evenfld is 0, if 0xE3[5] is 0, vblk_end_old value is 23 or 22
When it is PAL and evenfld is 1, if 0xE3[5] is 1, vblk_end_old value is 24 or 25
When it is PAL and evenfld is 0, if 0xE3[5] is 1, vblk_end_old value is 25 or 24

If 0xEC[7] is 0, it is high if V counter value is smaller than vblk_end_old one.
If 0xEC[7] is 1, even though V counter is smaller than vblk_end_old, it is still high.
If V counter is bigger or same than (240(NTSC) or 288(PAL)) + vblk_end_old value, it is high. Except this condition, it is low.

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x2E/3E/4E/5E	0	CH_CLK_SEL			CLK_DELAY_SEL				0x10

■ Registers To Control Clock Of Output

CH_CLK_SEL: Select a clock of each channel.

000	27MHz clock with delay of 0 ns.	001	27MHz clock with delay of 9.25 ns
010	27MHz clock with delay of 18.5 ns	011	27MHz clock with delay of 27.75 ns
100	54MHz clock with delay of 0 ns	101	54MHz clock with delay of 18.5 ns
110	108MHz clock with delay of 0 ns	111	108MHz clock with delay of 9.25 ns

CLK_DELAY_SEL: Delay the output clock in the unit of ≒ 1ns. Can be delayed up to ≒ 15ns.

0000	≒ 1ns	0100	≒ 4ns
1000	≒ 7ns	1111	≒ 15ns

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x2F/3F/4F/5F	CHID_PUT				0	CH_OUT_SEL			0x00/11/22/33

■ Registers To Control A Data Of Output

CHID_PUT : Register to put channel id to distinguish channel. (0x0~0xF)

CH_OUT_SEL: Define the output form of the data generated in case that the system is not set at No Video.

000	27MHz CCIR656 data of ch 1	001	27MHz CCIR656 data of ch 2
010	27MHz CCIR656 data of ch 3	011	27MHz CCIR656 data of ch 4
100	54MHz time-mixed CCIR656 data of ch 1,2	101	54MHz time-mixed CCIR656 data of ch 3,4
110	108MHz time-mixed CCIR656 data of ch 1,2,3,4	111	54MHz time-mixed CIF data of ch 1,2,3,4

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x61	1	0	0	0	0	0	0	AFE_FIR_MODE	0x80

■ Registers To Control An Analog Front End

AFE_FIR_MODE : Off Anti-aliasing Filter in the AFE of NVP1114A

0	On	1	Off

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x62	A_INP_GAIN_CTRL								0x40

■ Register To Control An Analog Front End

A_INP_GAIN_CTRL : Gain Factor of Analog AGC in the AFE of NVP1114. When A_AGC_FZ is high, It's value is adopted to analog AGC.

0x40	x1	0x80	x2
0xC0	x3	0xF0	x4

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x6D	0	0	0	0	COMB_MODE				0x01

Register To Control Comb Filter

COMB_MODE : Selects the filter to separate the color and brightness information out of the input signal(CVBS)

0	Adaptive Comb + special condition	1	Adaptive Comb
2	2line comb (1,2 line)	3	2line comb (2,3 line)
4	3line comb (1,2,3 line)	5	notch filter
6	Adaptive comb + notch (auto select)		

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x71	U_OFFSET2				V_OFFSET2				0x23

Register To Control A Chrominance

U_OFFSET2/V_OFFSET2 : U/V offset Value is adjustable up to ±7. U/V OFFSET consists of 2's Complements.

0001	+1	0111	+7
1000	-8	1111	-1

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x75	FSC_LOCK_MODE				FSC_LOCK_SPD				0xCC

Registers To Control A Chrominance

FSC_LOCK_MODE : V-Alternation Signal generator

FSC_LOC_MODE[1:0] : Control the error size

0	Average of two lines	1	Error per line
2	Average of two lines	3	Average of two lines (one line is skipped)

FSC_LOC_MODE[3:2] : V-Alternation Signal generator

0	Original V-alternation Signal	1	If the number of V-alternation Signal error is 7,v-alternation signal toggles in section(8~25) of vertical blank.
2	If the number of V-alternation Signal error is 7,v-alternation signal toggles in section(8~9) of vertical blank.	3	If the number of V-alternation Signal error is 15, v-alternation signal toggles

FSC_LOCK_SPD : Locking speed control & Tracking Filter selection

0	Bypass	1	1/2 Cut
2	1/4 Cut	3	1/8 Cut
4	1/16 Cut	5	1/2 No Cut
6	1/4 No Cut	7	1/8 No Cut
8	1/16 No Cut	9	Fastest on Tracking Filter
10	Fast on Tracking Filter	11	Normal on Tracking Filter
12	Slow on Tracking Filter	13	Fastest on Tracking Filter

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x77	ACC_OFF	0	1	0	ACC_GAIN_SPD				0x2F

Register To Control A Chrominance

ACC_OFF : Continue to a constant gain value for chroma signal.

0 On 1 Off

ACC_GAIN_SPD : 1 step value applied to the ACC Gain Accumulator (ACC Accumulator 1 Step value = 4 * ACC_GAIN_SPD + 2)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x79	FLD_DET_SPD		0	0	NOVID_MODE				0x43

Registers To Control A Processing For No-Video

FLD_DET_SPD : Select the method to create the field information that will be externally output

00 Middle 01 Slow

10 Fast 11 Fastest

NOVID_MODE : Select Condition for No video detection, High Active

NOVID_MODE[0] If the input video is not detected sync, turn on the NOVID signal

NOVID_MODE[1] if Width of detected sync is narrower than video standard. turn on NOVID signal

NOVID_MODE[2] If Vertical sync don't exist, turn on the NOVID signal

NOVID_MODE[3] If the CLAMP is not stable, turn on the NOVID signal

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x7A	0	0	NOVID_SPD						0x10

Registers To Control A Processing For No-Video

NOVID_SPD : Sensitivity of the Novideo condition(Higher value, lower sensitivity)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x7B	H_Sharpness				V_Sharpness				0x88

Registers To Control A Sharpness

H_Sharpness : Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction.

0000 0 0100 x0.5

1000 x1 1111 x2

V_Sharpness : Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction.

0000	0	0100	x0.5
1000	x1	1111	x2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x7C	PAL_CM_OFF	IF_FIR_SEL			0	0	CLPF_SEL		0x82

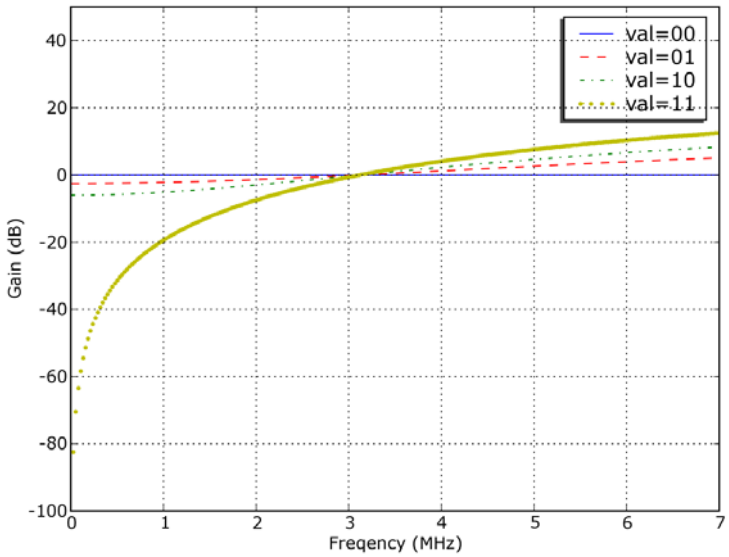
■ Registers To Control A Chrominance

PAL_CM_OFF : PAL Compensation On/Off

0	PAL Compensation applied	1	PAL Compensation not applied.

IF_FIR_SEL : IF Filter drive mode selected

000	bypass	001	mode1
010	mode2	others	mode3



CLPF_SEL : Color low pass filter applied mode applied after demodulation

00	Bypass	01	0.6M cutoff
10	1.0M cutoff	11	1.2M cutoff

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x7D	0	1	CTI_GAIN		C_KILL				0x63

■ Registers To Control A Chrominance

CTI_GAIN : Adjust gain level for CTI.

00	No Gain	11	More larger gain

C_KILL[3] : Color kill mode

0	Not Y/C separation	1	Color kill after Y/C separation

C_KILL[2:0] : color kill control

000	Burst Amplitude 10% Under & FSC Unlock	001	Burst Amplitude 5% Under & FSC Unlock
010	Burst Amplitude 10 % Under	011	Burst Amplitude 5% Under
100	Always color on	101	Always color on
110	Always color off	111	Always color off

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x83	BGD_COL				DATA_OUT_MODE				0x81

Register To Control A Data Of Output

BGD_COL : When No-Video, BackGround Color is used.

0000	Blue (75%)	1000	Black (75%)
0001	White (75%)	1001	Gray (75%)
0010	Yellow (75%)	1010	Red (NEXTCHIP*)
0011	Cyan (75%)	1011	Yellow (NEXTCHIP*)
0100	Green (75%)	1100	Magenta (NEXTCHIP*)
0101	Magenta (75%)	1101	Green (NEXTCHIP*)
0110	Red (75%)	1110	Blue (NEXTCHIP*)
0111	Blue (75%)	1111	Cyan (NEXTCHIP*)

* These color information is exactly same as controllers provided by NEXTCHIP

DATA_OUT_MODE : It limits a level of output data, can change signals of Cb and Cr each.

0000	Y(016~235), Cb(016~240), Cr(016~240)	0001	Y(001~254), Cb(001~254), Cr(001~254)
0010	Y(000~255), Cb(000~255), Cr(000~255)	0011	Cb/Cr Change, 016~235
0100	Cb/Cr Change, 001~254	0101	Cb/Cr Kill, 016~235
0110	Cb/Cr Kill, 001~254	Others	Background color output

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x84	0	0	0	0	NOVID_INF_IN	CHID_TYPE			0x01

Registers To Control An Output

NOVID_INF_IN : It can include a no-video information at MSB of EAV and SAV.

0	No information	1	Put no-video information in EAV or SAV

CHID_TYPE : It determines type of channel ID.

CHID_TYPE[2:0] = 0										
Condition			FVH			SAV / EAV Code Sequence				
Field	V	H	F	V	H	First	Second	Third	Fourth	
									NOVID_INF_IN = 0	NOVID_INF_IN = 1
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

CHID_TYPE[0] = 1																
Condition			FVH Value			SAV / EAV Code Sequence										
Field	V	H	F	V	H	First	Second	Third	Fourth							
									1CH	2CH	3CH	4CH	N_1CH	N_2CH	N_3CH	N_4CH
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3	0x70	0x71	0x72	0x73
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3	0x60	0x61	0x62	0x63
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3	0x50	0x51	0x52	0x53
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3	0x40	0x41	0x42	0x43
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3	0x30	0x31	0x32	0x33
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3	0x20	0x21	0x22	0x23
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93	0x10	0x11	0x12	0x13
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83	0x00	0x01	0x02	0x03

CHID_TYPE[1] = 1				
	Channel ID at Horizontal Blank			
	1CH	2CH	3CH	4CH
Y	0x10	0x11	0x12	0x13
Cb	0x80	0x81	0x82	0x83
Cr	0x80	0x81	0x82	0x83

CHID_TYPE[2] = 1				
	Channel ID at Horizontal Active in Vertical Blank			
	1CH	2CH	3CH	4CH
Y	0x10	0x11	0x12	0x13
Cb	0x80	0x81	0x82	0x83
Cr	0x80	0x81	0x82	0x83

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x85	OUT_DATA_INV				0	0	0	0	0x00

■ Registers To Control An Output

OUT_DATA_INV : It sorts output video data inversely. (0 : [7:0], 1 : [0:7])

OUT_DATA_INV[0]	Channel 1 output order control	OUT_DATA_INV[1]	Channel 2 output order control
OUT_DATA_INV[2]	Channel 3 output order control	OUT_DATA_INV[3]	Channel 4 output order control

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x88	0	0	0	0	0	0	0	VPLL_C	0x00

■ Register To Control A Video PLL

VPLL_C : Values(VPLL_OD, VPLL_M, VPLL_N) applied at PLL is permitted at a time.

0	Not applied	1	Applied

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x89	VPLL_OD[3:0]				VPLL_OFF	VPLL_TST		VPLL_RST	0x20
Bank0, 0x8A	VPLL_M[8]	VPLL_BP	VPLL_OE	VPLL_N					0x04
Bank0, 0x8B	VPLL_M[7:0]								0x2E

Registers To Control A Video PLL

VPLL_OFF : Power down control (Active high)

VPLL_TST : M and N divider test mode. (00 : N divider test and normal operation, 11 : M divider test)
Please fix PLL_TST = 00 in the normal Mode.

VPLL_RST : M and N divider reset for testability purpose. Please fix RESET=0 in the mormal PLL operation

VPLL_BP : Bypass the PLL, Active high

VPLL_OE : CLK_OUT enable signal, Active high

VPLL_M : Feedback 9-bit divider control pins, M[0] is LSB

VPLL_N : Input 5-bit divider control signal, N[0] is LSB

VPLL_OD : Output divider control signal

$$PLL\_OUT = Input\_Clock_{Frequency} \times \frac{VPLL\_M}{VPLL\_N} \times \frac{1}{VPLL\_OD} \times \frac{1}{2}$$

▶ VPLL_M = M[0]*1 + M[1]*2 + M[2]*4 + M[3]*8 + M[4]*16 + M[5]*32 + M[6]*64+ M[7]*128 + M[8]*256 + 2
▶ VPLL_N = N[0]*1 + N[1]*2 + N[2]*4 + N[3]*8 + N[4]*16 + 2
▶ VPLL_OD = OD[0]*1 + OD[1]*2 + OD[2]*4 + OD[3]*8

Where : PLL_OUT represents the output frequency.
▶ $INPUT\_CLOCK_{Freq}$ represents PLL input frequency
▶ VPLL_M represents feedback divider value
▶ VPLL_N represents input divider value
▶ VPLL_OD represents output divider value

※ Video PLL_OUT Frequency of NVP1114A must set 108MHz (54MHz x 2)
Please keep Bank0, 0x89 ~ 0x8B Address Default setting.

Attention : Please keep these conditions through usage
▶ 1MHz ≤ ($INPUT\_CLOCK_{Freq}$ / VPLL_N) ≤ 25MHz
▶ 100MHz ≤ PLL_OUT × VPLL_OD ≤ 250MHz
▶ VPLL_OD ≥ 1

※ For better understanding, ({0x8A[7],0x8B}+2) / [(0x8A[4:0]+2)×(0x89[7:4])×2] = V-PLL Gain

	0x89	0x8A	0x8B
x4	0x20	0x02	0x3E
x2	0x20	0x04	0x2E
x1	0x20	0x0A	0x2E

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x93	HPLL_OFF	0	1	1	1	0	0	1	0xB9

Registers To Control A HPLL

HPLL_OFF : HPLL ON/OFF (High Active)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0x99	0	1	0	1	0	0	WPD_MAX[9:8]		0x51
Bank0, 0x9A	WPD_MAX[7:0]								0xB5
Bank0, 0x9B	WPD_SEL								0x13
Bank0, 0x9C	WPD_SPD								0x03
Bank0, 0x9D	WPD_CTRL								0x22

■ Registers To Control A White Peak Detection

WPD_MAX : Digital value assigned to 110 IRE for the Normal 100% Color Bar (White Peak=100IRE) input
This digital value is applied to the gain table which is mapped by 255.

WPD_SEL[4] : White Peak Det. Function ON/OFF

0	About smaller White Peak value than WPD_MAX, WPD_MAX value is applied. About bigger one, Gain table which White peak value is applied to operates(WPD = ON)	1	Gain table with WPD_MAX value is applied (WPD = OFF)

WPD_SEL[3:0] : Set the stable boundary of White peak value. After this, if White peak value is over that boundary, white peak operates again.

WPD_SPD : Control the speed of White Peak Detect.

0 ~ 10	Bigger value, faster speed

WPD_CTRL[7:4] : Control counting the number which is out of the stable boundary of White peak value, compared with previous one.

0	32	1	16
2	8	3	4
4	2	5	1

WPD_CTRL[3:0] : Sampling the level of some % in the brightest section of the display, and comparing with WPD_MAX, white peak detection operates.

0	0.625 %	1	1.25 %
2	2.5 %	3	5 %
4	10 %	5	15 %
6	20 %	7	25 %

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xA1	A_ADC_PW0	A_ADC_PW1	A_ADC_PW2	A_ADC_PW3	0	CAS_PB	RM_PB_PIN	PB_RM_PIN	0x00
0xA2	A_DAC_PWDN	A_ADC_PWDN	1	0	ALINK_INV	ALINK_CLK	ALINK_CAS		0x22

■ Registers To Control AFE and Cascade Of Audio

A_ADC_PW0,1,2,3 : Power down for Analog Front-End circuit of Audio ADC0~3, reference voltage

0	Power On	1	Power Down

CAS_PB : The Usage of Playback Data when Cascade Mode

0	use multiple playback data, received through all stage	1	use single playback data, received through last stage

RM_PB_PIN : selection of clock and sync for ADATR, ADATM pin

0	use ACLK_REC and ASYNC_REC as clock and sync for ADATR, ADATM pin	1	use ACLK_PB and ASYNC_PB as clock and sync for ADATR, ADATM pin

PB_RM_PIN : selection of clock and sync for ADATR, ADATM pin

0	use ACLK_PB and ASYNC_PB as clock and sync for ADATR pin	1	use ACLK_REC and ASYNC_REC as clock and sync for ADATR pin

A_DAC_PWDN : Audio DAC power control

0	Power on	1	Power down

A_ADC_PWDN : Power down for analog front-end circuit of Audio ADC

0	Power on	1	Power down

ALINK_INV : Control the phase between transferred clock and cascade data

0	Same phase	1	Inverted phase

ALINK_CLK : Control the usage of ALINKI and ALINKO as clock transmitting

0	Don't Use	1	Use

ALINK_CAS : Control the usage of ALINKI and ALINKO as cascade transmitting

0	Don't Use	1	Use

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xA3	AIGAIN0				AIGAIN1				0x88
0xA4	AIGAIN2				AIGAIN3				0x88

■ Registers To Control An Audio Input Gain

AIGAIN : Control the gain of analog audio input AIN0 ~ 3

0	mute	1	0.25
2	0.31	3	0.38
4	0.5	5	0.63
6	0.75	7	0.88
8	1.0	9	1.25
10	1.5	11	1.75
12	2.0	13	2.25
14	2.5	15	2.75

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xA5	RM_MASTER	M_RLSWAP	RM_SSP	RM_BITRATE	RM_CLK	RM_SAMRATE	RM_BITWID	RM_SYNC	0x84

■ Registers To Control Record and Cascade Of Audio

RM_MASTER : Selection of master & slave mode of ACLK_REC and ASYNC_REC

0	Slave mode operation	1	Master mode operation

M_RLSWAP : Selection of data position for ADATA_MIX

0	mixing signal is assigned to left channel playback signal is assigned to right channel	1	mixing signal is assigned to right channel playback signal is assigned to left channel

RM_SSP : Selection of DSP mode and SSP mode for ADATA_REC pin, when ASYNC_REC is DSP mode

0	DSP mode	1	SSP mode

RM_BITRATE : Set the bitrate of audio signal outputted to ADATA_REC

0	256fs	1	384fs

RM_CLK : Set the relationship between audio signal outputted to ADATA_REC and clock outputted to ACLK_REC

0	inverted clock	1	non-inverted clock

RM_SAMRATE : Set the sampling rate of data outputted to ADATA_REC

0	8Khz	1	16Khz

RM_BITWID : Set the bit width of data outputted to ADATA_REC

0	16bits	1	8bits

RM_SYNC : Set the sync's mode inputted/outputted to ASYNC_REC.

0	I2S mode	1	DSP mode

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xA6	RM_LAW_SEL		CHIP_STAGE		CASCADE_MODE	R_ADATM	R_MULTCH		0x33

■ Registers To Control Record and Cascade Of Audio

RM_LAW_SEL : Define the data format outputed to ADATA_REC

0	linear PCM	1	None
2	u-law of G.711 format	3	a-law of G.711 format

CHIP_STAGE : Selection of chip state for cascade

0	middle stage	1	last stage
2	first stage	3	single chip operation

CASCADE_MODE : Set the chip position when it is cascaded.

0	NVP1114 type	1	NVP1104 type

R_ADATM : Selection of output data type for ADATA_MIX

0	Mixing data	1	Record Data

R_MULTCH : Selection of number of Channel for ADATA_REC

0	2ch channel	1	4ch channel
2	8ch channel	3	16ch channel

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xA7	R_SEQ_0				R_SEQ_1				0x01
0xA8	R_SEQ_2				R_SEQ_3				0x23
0xA9	R_SEQ_4				R_SEQ_5				0x45
0xAA	R_SEQ_6				R_SEQ_7				0x67
0xAB	R_SEQ_8				R_SEQ_9				0x89
0xAC	R_SEQ_A				R_SEQ_B				0xAB
0xAD	R_SEQ_C				R_SEQ_D				0xCD
0xAE	R_SEQ_E				R_SEQ_F				0xEF

■ Registers To Define Sequence of Record Data

R_SEQ : Sequence of Audio Data for ADATA_REC

0	channel 1 data	1	channel 2 data
2	channel 3 data	3	channel 4 data
4	channel 5 data	5	channel 6 data
6	channel 7 data	7	channel 8 data
8	channel 9 data	9	channel 10 data
10	channel 11 data	11	channel 12 data
12	channel 13 data	13	channel 14 data
14	channel 15 data	15	channel 16 data

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xAF	PB_MASTER	0	PB_SSP	PB_BITRATE	PB_CLK	PB_SAMRATE	PB_BITWID	PB_SYNC	0x04

■ Registers To Control A Playback

PB_MASTER : Set MASTER/SLAVE mode of ACLK_PB and ASYNC_PB.

0	Slave mode	1	Master mode

PB_SSP : Set the position of data and sync signals inputted to ADATA_PB, when ASYNC_PB is DSP mode.

0	DSP mode	1	SSP mode

PB_BITRATE : Set the bitrate of audio signal inputted to ADATA_PB.

0	256fs	1	384fs

PB_CLK : Set the relationship between audio signal inputted to ADATA_PB and clock inputted/outputed to ACLK_PB.

0	inverted clock	1	non-inverted clock

PB_SAMRATE : Set the sampling rate of data inputted to ADATA_PB.

0	8Khz	1	16Khz

PB_BITWID : Set the bit width of data inputted to ADATA_PB.

0	16bits	1	8bits

PB_SYNC : Set the sync's mode inputted/outputted to ASYNC_PB.

0	I2S mode	1	DSP mode

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xB0	PB_LAW_SEL		MIX_GAIN_MODE	0	0	0	0	0	0x00

Registers To Control A Playback

PB_LAW_SEL : Define the data format inputted to ADATA_PB.

0	linear PCM	1	None
2	G.711 format의 u-law	3	G.711 format의 a-law

MIX_GAIN_MODE : Selection of the mixing gain mode

0	Apply the mixing gain for MIX_GAIN0-P (0xB1~0xB3 Address) separately	1	Apply all mixing gain as the same gain(x1).

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xB1	MIX_GAIN0				MIX_GAIN1				0x88
0xB2	MIX_GAIN2				MIX_GAIN3				0x88
0xB3	AOGAIN				MIX_GAINP				0x88

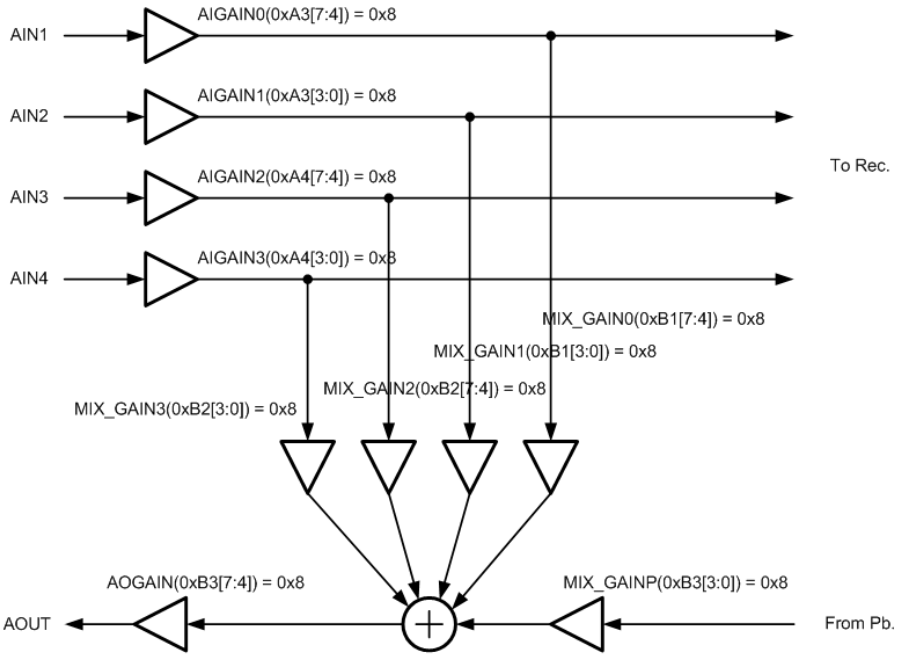
Registers To Control Mixing Of Audio And Gain Of DAC

MIX_GAINx, MIX_GAINP : Set the mixing gain for AIN0-3 and PLAYBACK

0	mute	1	0.25
2	0.31	3	0.38
4	0.5	5	0.63
6	0.75	7	0.88
8	1.0	9	1.25
10	1.5	11	1.75
12	2.0	13	2.25
14	2.5	15	2.75

AOGAIN : control the magnitude of output mixing signal

0	mute	1	0.25
2	0.31	3	0.38
4	0.5	5	0.63
6	0.75	7	0.88
8	1.0	9	1.25
10	1.5	11	1.75
12	2.0	13	2.25
14	2.5	15	2.75



※ This picture shows each position of Gain when it is mixed mode.
But if it is not Mixed but Live mode, MIX_GAIN(0xB2/B3[3:0]) becomes Bypass(gain=1)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xB4	0	0	0	MIX_OUTSEL					0x14

Register To Control A Mixing Of Audio

MIX_OUTSEL: select the audio output for analog mixing out.

0	Channel 0	1	Channel 1
2	Channel 2	3	Channel 3
4	Channel 4	5	Channel 5
6	Channel 6	7	Channel 7
8	Channel 8	9	Channel 9
10	Channel 10	11	Channel 11
12	Channel 12	13	Channel 13
14	Channel 14	15	Channel 15
16	playback audio (first stage playback audio)	17	middle stage playback audio
18	middle stage playback audio	19	last stage playback audio
20	mixed audio		

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xB5	ADET_MODE	ADET_FILT			ADET_0	ADET_1	ADET_2	ADET_3	0x0F

Registers For Audio Detection

ADET_MODE : Select the method to decide the existence of AIN0-3 audio signals.

0	Absolute amplitude detection mode	1	Differential amplitude detection mode

ADET_FILT : Set the time to decide the existence of AIN0-3 audio signals.

0	16 sec	1	15 sec
2	9 sec	3	5 sec
4	3 sec	5	1 sec
6	0.6 sec	7	0.5 sec

ADET_x : Enable bit audio signal existence checking function for AIN0-3.

0	don't use this function	1	Use this function

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xB6	ADET_TH0				ADET_TH1				0xAA
0xB7	ADET_TH2				ADET_TH3				0xAA

Register For Audio Detection

ADET_THx : Set the threshold value for audio signal existence of AIN0-3

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xB8	PB_SEL				MUX_DELAY		DC0		0x02
Bank0, 0xB9	DC1								0x00

Registers To Select An Audio Channel For Playback Input

PB_SEL: select the audio input channel for playback input

0	Channel 0	1	Channel 1
2	Channel 2	3	Channel 3
4	Channel 4	5	Channel 5
6	Channel 6	7	Channel 7
8	Channel 8	9	Channel 9
10	Channel 10	11	Channel 11
12	Channel 12	13	Channel 13
14	Channel 14	15	Channel 15

MUX_DELAY : Select the audio input pin

2	TW2864 pin to pin	3	TW2815 pin to pin

DC : set DC level of inputted audio signal through ADC

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xC0	ID_ON1	BLK_OPER1	SUB_SAM1	SCALE_SEL1	SYNC_ORG1	UP1	HBYPASS1	VBYPASS1	0x13
Bank0, 0xC1	ID_ON2	BLK_OPER2	SUB_SAM2	SCALE_SEL2	SYNC_ORG2	UP2	HBYPASS2	VBYPASS2	0x13
Bank0, 0xC2	ID_ON3	BLK_OPER3	SUB_SAM3	SCALE_SEL3	SYNC_ORG3	UP3	HBYPASS3	VBYPASS3	0x13
Bank0, 0xC3	ID_ON4	BLK_OPER4	SUB_SAM4	SCALE_SEL4	SYNC_ORG4	UP4	HBYPASS4	VBYPASS4	0x13

Registers To Control Scaler.

ID_ON : Decide if CH ID is inserted or not

0	CH ID is not inserted	1	CH ID is inserted.

BLK_OPER : Change data of the V or H Blank section. Existing 0x80, 0x10, 0x80 and 0x10 stream is changed to BLK_PKG register value as below.

0	Existing 0x80, 0x10 data stream.	1	Change to BLK_PKG (0xDA~0xDD register) value

SUB_SAM : When you scale under 0.5, select between average method and sampling one which is extracting one by one.
(But when you scale 0.5~1, set it only sampling(1))

0	Average	1	Sampling

SCALE_SEL : Decide to output between scale data and non-scale data which is same as bypass

0	bypass an input data.	1	output a scaled data

SYNC_ORG : Decide H blank length between standard and variable one based on scale ratio.

0	Changed by a scale ratio.	1	No changed by a scale ratio

UP : According to only 720 pixel input, stretch the display size to 720-size.

0	No expand	1	Expand

HBYPASS : According to H direction, decide if it is treated as cubic convolution or bypass.

0	Cubic Convolution	1	Bypass

VBYPASS : According to V direction, decide if it is treated as cubic convolution or bypass.

0	Cubic Convolution	1	Bypass

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xC4	H_DEL1				H_DEL2				0x00
Bank0, 0xC5	H_DEL3				H_DEL4				0x00

■ Registers To Control Scaler

H_DEL : When input is 704 pixel, decider H start position(0~15)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xC6	H_DTO1[7:0]								0x71
Bank0, 0xC7	H_DTO2[7:0]								0x71
Bank0, 0xC8	H_DTO3[7:0]								0x71
Bank0, 0xC9	H_DTO4[7:0]								0x71
Bank0, 0xCA	H_DTO1[15:8]								0x1C
Bank0, 0xCB	H_DTO2[15:8]								0x1C
Bank0, 0xCC	H_DTO3[15:8]								0x1C
Bank0, 0xCD	H_DTO4[15:8]								0x1C
Bank0, 0xCE	V_DTO1[19:16]				H_DTO1[19:16]				0x87
Bank0, 0xCF	V_DTO2[19:16]				H_DTO2[19:16]				0x87
Bank0, 0xD0	V_DTO3[19:16]				H_DTO3[19:16]				0x87
Bank0, 0xD1	V_DTO4[19:16]				H_DTO4[19:16]				0x87
Bank0, 0xD2	V_DTO1[7:0]								0x00
Bank0, 0xD3	V_DTO2[7:0]								0x00
Bank0, 0xD4	V_DTO3[7:0]								0x00
Bank0, 0xD5	V_DTO4[7:0]								0x00
Bank0, 0xD6	V_DTO1[15:8]								0x00
Bank0, 0xD7	V_DTO2[15:8]								0x00
Bank0, 0xD8	V_DTO3[15:8]								0x00
Bank0, 0xD9	V_DTO4[15:8]								0x00

■ Registers To Control Scaler

H_DTO : For Horizontal Direction, decide Ratio of Scale.

NTSC/PAL H scale = (H_DTO / 2^19) x 720

V_DTO : For Vertical Direction, decide Ratio of Scale.

NTSC V scale = (V_DTO / 2^19) x 240 PAL V scale = (V_DTO / 2^19) x 288

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xDA	BLK_PKG[31:24]								0x80
Bank0, 0xDB	BLK_PKG[23:16]								0x10
Bank0, 0xDC	BLK_PKG[15:8]								0x80
Bank0, 0xDD	BLK_PKG[7:0]								0x10

■ Registers To Control Scaler

BLK_PKG : data insertion in the section of H or V Blank.

[31:24] Cb [23:16] Y1

[15:8] Cr [7:0] Y2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xE4	GPO1_INV	GPO1_OUT_SEL			GPO2_INV	GPO2_OUT_SEL			0x00
Bank0, 0xE5	GPO3_INV	GPO3_OUT_SEL			0	0	0	0	0x00

■ Registers To Control Timings Of Output

MPPx_INV : Change the output signal's phase through GPOx pin.

0 Normal Phase 1 Reverse Phase

MPP1_OUT_SEL : Select the output signal through GP01

0	video loss	1	video loss or audio mute
2	Test Signals of Video Decoder #1 (0x86[3:0])	3	None
4	motion	5	video loss or audio mute or motion
6	video loss or audio mute or motion or alarm	7	mute

MPP2_OUT_SEL : Select the output signal through GP02

0	audio mute	1	video loss or audio mute
2	Test Signals of Video Decoder #1 (0x86[3:0])	3	Test Signals of Video Decoder #2 (0x86[7:4])
4	video loss	5	video loss or audio mute or motion
6	video loss or audio mute or motion or alarm	7	motion

MPP3_OUT_SEL :Select the output signal through GP03

0	motion	1	video loss or audio mute
2	Test Signals of Video Decoder #3 (0x87[3:0])	3	Test Signals of Video Decoder #4 (0x87[7:4])
4	audio mute	5	video loss or audio mute or motion
6	video loss or audio mute or motion or alarm	7	video loss

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xF0	VAFE_PDN_04	VAFE_PDN_03	VAFE_PDN_02	VAFE_PDN_01	ENC_CLK_SEL		VDAC_CLK_SEL		0x00

■ Registers To Control Power Down Of Video AFE

VAFE_PDN_04 : Power down for analog front-end circuit of video channel 4
VAFE_PDN_03 : Power down for analog front-end circuit of video channel 3
VAFE_PDN_02 : Power down for analog front-end circuit of video channel 2
VAFE_PDN_01 : Power down for analog front-end circuit of video channel 1

ENC_CLK_SEL : Select Video Encoder Clock

00	27MHz (ex_in_clk)	01	27MHz inverse (ex_in_clk_inv)
10	27MHz (inner clock, dec_27m_clk)	11	27MHz inverse (inner clock, dec_27m_clk_inv)

VDAC_CLK_SEL : Select Video DAC Clock

00	27MHz inverse (ex_in_clk_inv)	01	27MHz (ex_in_clk)
10	27MHz inverse (inner clock, dec_27m_clk_inv)	11	54MHz (PIN, inverse)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xF2	DIV_SRC_SEL	DEC_27CLK_SEL			0	0	0	0	0x00

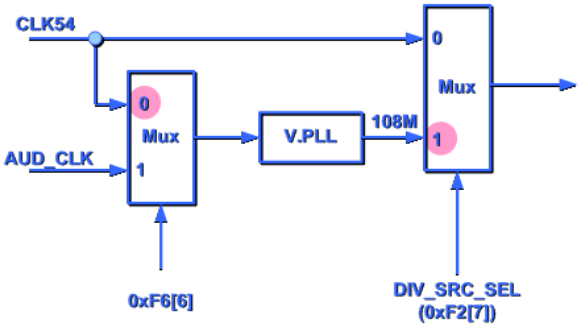
■ Registers To Control An AFE Of Audio

DIV_SRC_SEL : Select the main clock to operate the logic in a chip.(Cf. : assume that 54MHz Oscillator is connected to CLK54I pin)

0	54MHz coming to pin	1	108MHz passed through Video PLL

DEC_27CLK_SEL : Select the clock to operate Core of video decoder.(It should be operated with 27MHz. Assume that Osc.=54MHz, DIV_SRC_SEL(0xF2[7])=0)

0	27MHz Phase1 (div4)	1	27MHz Phase2 (div4)
2	27MHz Phase3 (div4)	3	27MHz Phase4 (div4)
4	54MHz Phase1 (div2)	5	54MHz Phase2 (div2)
6	108MHz (div_src_clk)	7	108MHz inverse (div_src_clk_inv)



NVP1114A	
Address	Value
0xF2	0xA0
0xF6	0x80

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xF3	AADC_CLK_SEL	0	0	ADAC_CLK_SEL	DEC_108CLK_SEL	AUD_54CLK_SEL			0x00

■ Registers To Control An AFE Of Audio

AADC_CLK_SEL : Select the input clock of Audio ADC

0	au_adc_clk	1	au_adc_clk_inv

ADAC_CLK_SEL : Select the input clock of Audio ADC

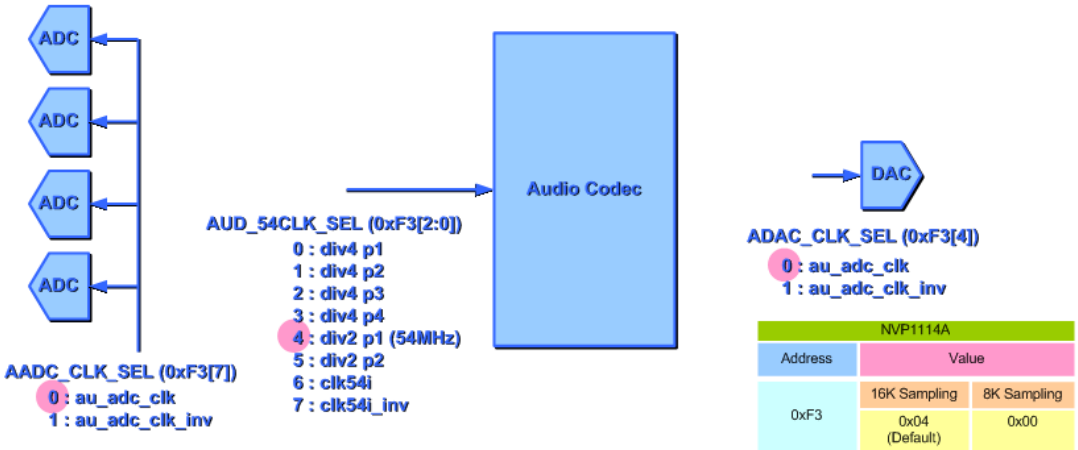
0	au_dac_clk	1	au_dac_clk_inv

DEC_108CLK_SEL : It is used in the block of data muxing which is operated with 108Mhz inside of video decoder.

0	108MHz (div_src_clk)	1	108MHz inverse (div_src_clk_inv)

AUD_54CLK_SEL : Select the clock to operate Audio Codec's logic(It should be 54MHz)

0	27MHz Phase1 (div4)	1	27MHz Phase2 (div4)
2	27MHz Phase3 (div4)	3	27MHz Phase4 (div4)
4	54MHz Phase1 (div2)	5	54MHz Phase2 (div2)
6	54MHz (clk54i)	7	54MHz inverse (clk54i_inv)



NVP1114A		
Address	Value	
0xF3	16K Sampling	8K Sampling
	0x04 (Default)	0x00

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xF6	CLK108_PROCESS	0	VDO4_OEB	VDO1_OEB	VDO3_OEB	VDO2_OEB	VDAC1_OFF	VDAC2_OFF	0x80

Registers To Control A Direction Of Video Data

CLK108_PROCESS : The mode to treat 108MHz signal(NVP1114A is always 1)

0 54MHz signal processing 1 108MHz signal processing

VDOx_OEB : Select Status(output or Hi-Z) of Video Output for X Port.

0 Output Status 1 Hi-Z

VDAC1_OFF : Power down for video DAC of channel 1
VDAC2_OFF : Power down for video DAC of channel 2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank0, 0xF9	0	DATA_CATCH			0	0	0	0	0x20

Register To Catch Data

DATA_CATCH : It can move a catch point to catch a stable data in each other frequency.

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
0xFF	0	0	0	0	0	0	0	BANK_SEL	0x00

Register To Select A Bank Of Registers

BANK_SEL : Select a Bank of Registers (Bank 0, Bank 1)

0 Bank 0 1 Bank 1

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x00	BW_ON	CBAR_ON	PED	0	LNFMT	V_ALTER	FSC_SEL		0x00

Registers To Video Standard Selection In Video Encoder

BW_ON : Generate Black/White only

0 Color 1 BW (Black / White)

CBAR_ON : Select to receive CCIR656 data coming out of the internal Color Bar Generator.

0 External CCIR656 Input 1 Internal CCIR656 Input (Default : Color Bar)

PED : Choose to add Pedestal to the Signal

0 Off 1 On

LNFMT : Select the field frequency (Fv) of Video Standard

0 60 Hz 1 50 Hz

V_ALTER : Add Phase Alternation

0	Off	1	On

FSCSEL : Determine the frequency for modulation

00	3.57954545 MHz	01	4.43361875 MHz
10	3.57561149 MHz	11	3.58205625 MHz

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x01	PATTERN_TYPE				1	0	CFIR_SEL		0x08

Registers To Select Internal Pattern & C-LPF In Video Encoder

PATTERN_TYPE : Determine the output pattern of the internal color bar generator

0000	Color Bar	0001	White
0010	Yellow	0011	Cyan
0100	Green	0101	Red
0110	Red	others	Color Bar

CFIR_SEL : Determine the cutoff frequency of the C low-pass filter

00	0.6 MHz cut-off	01	1.0 MHz cut-off
10	1.3 MHz cut-off	11	1.3 MHz cut-off

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x02	HDELAY								0x00
Bank1, 0x03	VDELAY								0x00

Registers To Move Position Of Output Image In Video Encoder

E_HDELAY : Move the output image in a horizontal direction.

0x00 ~ 0x7F	Delay to the right by 1 pixel. 0 means no delay.
0x80 ~ 0xFF	Delay to the left by 1 pixel. 8 means no delay.

E_VDELAY : Move the output image in a vertical direction.

0x00 ~ 0x7F	Delay upward by 1 line. 0 means no delay.
0x80 ~ 0xFF	Delay downward by 1 line. 8 means no delay.

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x04	BUST_GAIN								0x86
Bank1, 0x05	SYNC_GAIN								0x7A
Bank1, 0x06	LUMA_GAIN								0x7E
Bank1, 0x07	CHMA_GAIN								0x7A

■ Registers To Apply Gain For Output In Video Encoder

BUST_GAIN : Apply gain to Bursts of CVBS and S-video (0 ~ about two times)
Total gain = [7] + [6] + [5] + [4] + [3] + [2] + [1] + [0]
The bit that is not activated is zero.

[7]	×1	[6]	×(1/2)
[5]	x (1/4)	[4]	x (1/8)
[3]	x (1/16)	[2]	x (1/32)
[1]	x (1/64)	[0]	x (1/128)

SYNC_GAIN : Apply gain to Syncs of CVBS and S-video (0 ~ about two times)
Total gain = [7] + [6] + [5] + [4] + [3] + [2] + [1] + [0]
The bit that is not activated is zero.

[7]	×1	[6]	×(1/2)
[5]	x (1/4)	[4]	x (1/8)
[3]	x (1/16)	[2]	x (1/32)
[1]	x (1/64)	[0]	x (1/128)

LUMA_GAIN : Apply gain to Luma of CVBS and S-video (0 ~ about two times)
Total gain = [7] + [6] + [5] + [4] + [3] + [2] + [1] + [0]
The bit that is not activated is zero.

[7]	×1	[6]	×(1/2)
[5]	x (1/4)	[4]	x (1/8)
[3]	x (1/16)	[2]	x (1/32)
[1]	x (1/64)	[0]	x (1/128)

CHMA_GAIN : Apply gain to Chroma of CVBS and S-video (0 ~ about two times)
Total gain = [7] + [6] + [5] + [4] + [3] + [2] + [1] + [0]
The bit that is not activated is zero.

[7]	×1	[6]	×(1/2)
[5]	x (1/4)	[4]	x (1/8)
[3]	x (1/16)	[2]	x (1/32)
[1]	x (1/64)	[0]	x (1/128)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x08	0	0	0	FLD_ENH_ON	0	0	SYNC_FIR_SEL		0x00
Bank1, 0x09	0	0	ENC_OUT1_SEL		0	0	ENC_OUT2_SEL		0x00

■ Registers To Control Field Enhancement In Video Encoder

FLD_ENH_ON : Function for Field Enhancement is operated.

SYNC_FIR_SEL : Slope of Sync is changed.

ENC_OUTx_SEL : Output of Encoder is selected.

0	CVBS	1	Luminance
2	Chrominance	3	Chrominance

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x90	0	0	0	INTP_MODE	0	0	FE_FLD_SEL	YC_CLIP	0x00
Bank1, 0x91	FE_DIFF_REF								0x00

■ Register To Control Field Enhancement In Video Encoder

INTP_MODE : Interpolation mode is set.

0 Enhancement Method 1 Interpolation

FE_FLD_SEL : Field applied at Field Enhancement is defined.

0 odd field 1 even field

FE_DIFF_REF : If value is large, add weight value at vertical direction on interpolation.

YC_CLIP : Range of Y, C data is limited.

Y 16 ~ 235 C 16 ~ 240

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x10,0x14,0x18,0x1C, 0x20,0x24,0x28,0x2C, 0x30,0x34,0x38,0x3C, 0x40,0x44,0x48,0x4C	FE_EN_WIN_HR_x								0x00
Bank1, 0x11,0x15,0x19,0x1D, 0x21,0x25,0x29,0x2D, 0x31,0x35,0x39,0x3D, 0x41,0x45,0x49,0x4D	FE_EN_WIN_HL_x								0x00
Bank1, 0x12,0x16,0x1A,0x1E, 0x22,0x26,0x2A,0x2E, 0x32,0x36,0x3A,0x3E, 0x42,0x46,0x4A,0x4E	FE_EN_WIN_VB_x								0x00
Bank1, 0x13,0x17,0x1B,0x1F, 0x23,0x27,0x2B,0x2F, 0x33,0x37,0x3B,0x3F, 0x43,0x47,0x4B,0x4F	FE_EN_WIN_VT_x								0x00

■ Register To Control Field Enhancement In Video Encoder

: Window of 16 is created. therefore, each channel can be controled.

FE_EN_WIN_HR_x : Right Position of Horizontal direction of Area enabled Field Enhancement is changed.

FE_EN_WIN_HL_x : Left Position of Horizontal direction of Area enabled Field Enhancement is changed.

FE_EN_WIN_VB_x : Bottom Position of Vertical direction of Area enabled Field Enhancement is changed.

FE_EN_WIN_VT_x : Top Position of Vertical direction of Area enabled Field Enhancement is changed.

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0x50,0x54,0x58,0x5C, 0x60,0x64,0x68,0x6C, 0x70,0x74,0x78,0x7C, 0x80,0x84,0x88,0x8C	FE_DIS_WIN_HR_x								0x00
Bank1, 0x51,0x55,0x59,0x5D, 0x61,0x65,0x69,0x6D, 0x71,0x75,0x79,0x7D, 0x81,0x85,0x89,0x8D	FE_DIS_WIN_HL_x								0x00
Bank1, 0x52,0x56,0x5A,0x5E, 0x62,0x66,0x6A,0x6E, 0x72,0x76,0x7A,0x7E, 0x82,0x86,0x8A,0x8E	FE_DIS_WIN_VB_x								0x00
Bank1, 0x53,0x57,0x5B,0x5F, 0x63,0x67,0x6B,0x6F, 0x73,0x77,0x7B,0x7F, 0x83,0x87,0x8B,0x8F	FE_DIS_WIN_VT_x								0x00

■ Register To Control Field Enhancement In Video Encoder

: Window of 16 is created. therefore, each channel can be controled.

FE_DIS_WIN_HR_x : Right Position of Horizontal direction of Area disabled Field Enhancement is changed.

FE_DIS_WIN_HL_x : Left Position of Horizontal direction of Area disabled Field Enhancement is changed.

FE_DIS_WIN_VB_x : Bottom Position of Vertical direction of Area disabled Field Enhancement is changed.

FE_DIS_WIN_VT_x : Top Position of Vertical direction of Area disabled Field Enhancement is changed.

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0xA1/A3/A5/A7	MOTION_TIME_01			MOTION_OFF_01	0	0	MOTION_PIC_01		0x13

■ Registers To Detect Motion

MOTION_TIME : The time to happen Motion interrupt.

0~7 Bigger value, longer time

MOTION_OFF : Using NVP1114, it ensures that no motion information generated.

0 Motion detection on 1 Motion detection off

Note.)

1 Output Port :

- Only 1Ch. Motion (B1.0xA1=0x03, B0.0x05=0x18, B0.0x06=0x32, B0.0x2F[3:0]=0x0)
- Only 2Ch. Motion (B1.0xA3=0x03, B0.0x05=0x90, B0.0x06=0x32, B0.0x2F[3:0]=0x1)
- Only 3Ch. Motion (B1.0xA5=0x03, B0.0x05=0x10, B0.0x06=0x3A, B0.0x2F[3:0]=0x2)
- Only 4Ch. Motion (B1.0xA7=0x03, B0.0x05=0x10, B0.0x06=0xB2, B0.0x2F[3:0]=0x3)

2 Output Port :

- Only 1Ch. Motion (B1.0xA1=0x03, B0.0x07=0x18, B0.0x08=0x32, B0.0x3F[3:0]=0x0)
- Only 2Ch. Motion (B1.0xA3=0x03, B0.0x07=0x90, B0.0x08=0x32, B0.0x3F[3:0]=0x1)
- Only 3Ch. Motion (B1.0xA5=0x03, B0.0x07=0x10, B0.0x08=0x3A, B0.0x3F[3:0]=0x2)
- Only 4Ch. Motion (B1.0xA7=0x03, B0.0x07=0x10, B0.0x08=0xB2, B0.0x3F[3:0]=0x3)

3 Output Port :

- Only 1Ch. Motion (B1.0xA1=0x03, B0.0x09=0x18, B0.0x0A=0x32, B0.0x4F[3:0]=0x0)
- Only 2Ch. Motion (B1.0xA3=0x03, B0.0x09=0x90, B0.0x0A=0x32, B0.0x4F[3:0]=0x1)
- Only 3Ch. Motion (B1.0xA5=0x03, B0.0x09=0x10, B0.0x0A=0x3A, B0.0x4F[3:0]=0x2)
- Only 4Ch. Motion (B1.0xA7=0x03, B0.0x09=0x10, B0.0x0A=0xB2, B0.0x4F[3:0]=0x3)

4 Output Port :

- Only 1Ch. Motion (B1.0xA1=0x03, B0.0x0B=0x18, B0.0x0C=0x32, B0.0x5F[3:0]=0x0)
- Only 2Ch. Motion (B1.0xA3=0x03, B0.0x0B=0x90, B0.0x0C=0x32, B0.0x5F[3:0]=0x1)
- Only 3Ch. Motion (B1.0xA5=0x03, B0.0x0B=0x10, B0.0x0C=0x3A, B0.0x5F[3:0]=0x2)
- Only 4Ch. Motion (B1.0xA7=0x03, B0.0x0B=0x10, B0.0x0C=0xB2, B0.0x5F[3:0]=0x3)

MOTION_PIC : Indicates the type of processing made on the area where motion is generated.

0	EVEN_FLD (Luma - 32)	1	EVEN_FLD (Luma - 48)
2	ALL FLD (Luma - 48)	3	No processing made on the area where motion is generated.

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0xA2/A4/A6/A8	MOD_TSEN_01								0x6B

■ Registers To Detect Motion

MOD_TSEN : Motion Temporal Sensitivity.
: The value (the sum of the motion block) based on which it is determined whether motion is generated or not.
(0 -> 255 The greater the number, the less sensitive it gets)

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Default
Bank1, 0xA9	MOD_PSEN_01		MOD_PSEN_02		MOD_PSEN_03		MOD_PSEN_04		0xAA

■ Registers To Detect Motion

MOD_PSEN : Motion Pixel Sensitivity.
: Register that determines how much data input in the Motion block is used to search for motion

0	bypass	1	1/2
2	1/4	3	1/8

Bank1, 0xB0	CH1_MOD_01	CH1_MOD_02	CH1_MOD_03	CH1_MOD_04	CH1_MOD_05	CH1_MOD_06	CH1_MOD_07	CH1_MOD_08	0xFF
Bank1, 0xB1	CH1_MOD_09	CH1_MOD_10	CH1_MOD_11	CH1_MOD_12	CH1_MOD_13	CH1_MOD_14	CH1_MOD_15	CH1_MOD_16	0xFF
Bank1, 0xB2	CH1_MOD_17	CH1_MOD_18	CH1_MOD_19	CH1_MOD_20	CH1_MOD_21	CH1_MOD_22	CH1_MOD_23	CH1_MOD_24	0xFF
Bank1, 0xB3	CH1_MOD_25	CH1_MOD_26	CH1_MOD_27	CH1_MOD_28	CH1_MOD_29	CH1_MOD_30	CH1_MOD_31	CH1_MOD_32	0xFF
Bank1, 0xB4	CH1_MOD_33	CH1_MOD_34	CH1_MOD_35	CH1_MOD_36	CH1_MOD_37	CH1_MOD_38	CH1_MOD_39	CH1_MOD_40	0xFF
Bank1, 0xB5	CH1_MOD_41	CH1_MOD_42	CH1_MOD_43	CH1_MOD_44	CH1_MOD_45	CH1_MOD_46	CH1_MOD_47	CH1_MOD_48	0xFF
Bank1, 0xB6	CH1_MOD_49	CH1_MOD_50	CH1_MOD_51	CH1_MOD_52	CH1_MOD_53	CH1_MOD_54	CH1_MOD_55	CH1_MOD_56	0xFF
Bank1, 0xB7	CH1_MOD_57	CH1_MOD_58	CH1_MOD_59	CH1_MOD_60	CH1_MOD_61	CH1_MOD_62	CH1_MOD_63	CH1_MOD_64	0xFF

■ Registers To Detect Motion

CH_MOD_01 ~ CH_MOD_64
: Block enabler to detect motion.
: The entire screen is divided into 64 sections to each of which Enable is allocated.

CH_MOD_01	CH_MOD_02	CH_MOD_03	CH_MOD_04	CH_MOD_05	CH_MOD_06	CH_MOD_07	CH_MOD_08
CH_MOD_09	CH_MOD_10	CH_MOD_11	CH_MOD_12	CH_MOD_13	CH_MOD_14	CH_MOD_15	CH_MOD_16
CH_MOD_17	CH_MOD_18	CH_MOD_19	CH_MOD_20	CH_MOD_21	CH_MOD_22	CH_MOD_23	CH_MOD_24
CH_MOD_25	CH_MOD_26	CH_MOD_27	CH_MOD_28	CH_MOD_29	CH_MOD_30	CH_MOD_31	CH_MOD_32
CH_MOD_33	CH_MOD_34	CH_MOD_35	CH_MOD_36	CH_MOD_37	CH_MOD_38	CH_MOD_39	CH_MOD_40
CH_MOD_41	CH_MOD_42	CH_MOD_43	CH_MOD_44	CH_MOD_45	CH_MOD_46	CH_MOD_47	CH_MOD_48
CH_MOD_49	CH_MOD_50	CH_MOD_51	CH_MOD_52	CH_MOD_53	CH_MOD_54	CH_MOD_55	CH_MOD_56
CH_MOD_57	CH_MOD_58	CH_MOD_59	CH_MOD_60	CH_MOD_61	CH_MOD_62	CH_MOD_63	CH_MOD_64

7. Electrical characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
1.8V Digital Power Supply Voltage	V_{POWER1}	1.65	1.8	1.95	V
1.8V Analog Power Supply Voltage	V_{DDA1}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{POWER2}	3.0	3.3	3.6	V
3.3V Analog Power Supply Voltage	V_{DDA2}	3.0	3.3	3.6	V
Voltage on Any 1.8V input pins	V_{PIN1}	1.65	1.8	1.95	V
Voltage on Any 3.3V input pins	V_{PIN2}	3.0	3.3	3.6	V
Voltage on Any 5V input pins	V_{PIN5}	4.5	5	5.5	V
Storage Temperature	V_S	-40	-	125	℃
Junction Temperature	V_J	-40	-	125	℃
Vapor phase soldering (15 Sec)	V_{VSOL}	-	-	220	℃

7.2 Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
1.8V Digital Power Supply Voltage	V_{POWER1}	1.65	1.8	1.95	V
1.8V Analog Power Supply Voltage	V_{DDA1}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{POWER2}	3.0	3.3	3.6	V
3.3V Analog Power Supply Voltage	V_{DDA2}	3.0	3.3	3.6	V
Ambient operating temperature	V_A	-10	-	80	℃

7.3 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	VSSI-0.3	-	$0.3V_{POWER}$	V
Input High Voltage	V_{IH}	$0.7V_{POWER}$	-	V_{POWER}+0.3	V
Input Low Current (V_{IN} = VSS)	I_{IL}	-	-	-10	uA
Input High Current (VIN = V_{POWER})	I_{IH}	-	-	10	uA
Input Capacitance (f = 1MHz, V_{IN} = 2.4V)	C_{IN}	-	-	10	pF
Output Low Voltage (I_{OL} = 8.0mA)	V_{OL}	-	-	0.4	V
Output High Voltage (I_{OH} = 11.9mA)	V_{OH}	2.4	-	V_{POWER}	V
Three-State Current	I_{OZ}	-	-	10	uA
Output Capacitance	C_{OUT}	-	-	10	pF

7.4 AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current					
1.8V Supply Current	I_{DD1}	-	145	-	mA
3.3V Supply Current	I_{DD2}	-	137	-	mA
Clock Pin					
P_CLKIN frequency	f_{CLK54}	-	54.0	-	MHz
P_CLKIN duty cycle	f_{DUTY}	45	-	55	%
P_CLKIN pulse width low	t_{PWL_CLK54}	8.0	-	-	nsec
P_CLKIN pulse width high	t_{PWH_CLK54}	8.0	-	-	nsec
Host Interface Pins					
P_SCL frequency	f_{SCL}	-	-	6	P_CLKIN
P_SCL minimum pulse width low	t_{PWL_SCL}	6	-	-	P_CLKIN
P_SCL minimum pulse width high	t_{PWH_SCL}	4	-	-	P_CLKIN
P_SCL to P_SDA setup time	t_{IS_SDA}	2	-	-	P_CLKIN
P_SCL to P_SDA hold time	t_{IH_SDA}	2	-	-	P_CLKIN
P_SCL to P_SDA delay time	t_{OD_SDA}	-	-	6	P_CLKIN
P_SCL to P_SDA hold time	t_{OH_SDA}	3	-	-	P_CLKIN

8. System Application

8.1 Recommended Register

: For register values, always make sure to check and use updated values of recommendation.

8.1.1 Order for NTSC Recommended Register Setting

◆ Audio Master Mode Setting (Input clock : 54MHz) - 16KHz, 16bit, 16Channel, I2S, 4.096MHz

1

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xF0	0x00	0x00	0xA0	0x04	0x00	0x00	0x80	0x58	0x7B	0x20	0x00	0x80	0x80	0x49	0x37	0x00

2

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	Empty	0x00	0x22	0x88	0x88	0x84	0x33	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x80	0x00	0x00	0xC9	0x0F	0x18
Bank0, 0xC0	0x13	0x13	0x13	0x13	0x00	0x00	0x71	0x71	0x71	0x71	0x1C	0x1C	0x1C	0x1C	0x87	0x87
Bank0, 0xD0	0x87	0x87	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x80	0x10	0x80	0x10	0x00	0x00
Bank0, 0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x11	0x01	0x40	0x00	0x00	0x00	0x00

3

ADDRESS	0x00
Bank0, 0xA0	0x00

4

108MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x06
Bank0, 0x30	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x16
Bank0, 0x40	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x26
Bank0, 0x50	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x36
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x80	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x82	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xB8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xB5	0x13	0x03	0x22	0xFF	0x00

54MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x04
Bank0, 0x30	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x15
Bank0, 0x40	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x24
Bank0, 0x50	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x35
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x80	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x82	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xB8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xB5	0x13	0x03	0x22	0xFF	0x00

27MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x00
Bank0, 0x30	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x11
Bank0, 0x40	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x22
Bank0, 0x50	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x33
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x80	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x82	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xB8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xB5	0x13	0x03	0x22	0xFF	0x00

5

ADDRESS	0x08
Bank0, 0x80	0x00

6

ADDRESS	0x0F
Bank0, 0xF0	0x01

7

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank1, 0x00	0x00	0x08	0x00	0x00	0x86	0x7A	0x7E	0x7A	0x00	0x00	-	-	-	-	-	-
Bank1, 0x10 ~ 0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Bank1, 0x90	0x00	0x00	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Bank1, 0xA0	0x00	0x03	0x6B	0x03	0x6B	0x03	0x6B	0x03	0x6B	0xAA	0xFF	0x00	0x00	0x00	0x00	-

8

ADDRESS	0x0F
Bank0, 0xF0	0x00

9

ADDRESS	0x06
Bank0, 0xF0	0x80

10

ADDRESS	0x08
Bank0, 0x80	0x00

◆ Audio Master Mode Setting (Input clock : 54MHz) - 8KHz, 16bit, 16Channel, I2S, 2.048MHz

1

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xF0	0x00	0x00	0xA0	0x00	0x00	0x00	0x80	0x58	0x7B	0x20	0x00	0x80	0x80	0x49	0x37	0x00

2

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	Empty	0x00	0x22	0x88	0x88	0x84	0x33	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x80	0x00	0x00	0xC9	0x0F	0x18
Bank0, 0xC0	0x13	0x13	0x13	0x13	0x00	0x00	0x71	0x71	0x71	0x71	0x1C	0x1C	0x1C	0x1C	0x87	0x87
Bank0, 0xD0	0x87	0x87	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x80	0x10	0x80	0x10	0x00	0x00
Bank0, 0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x11	0x01	0x40	0x00	0x00	0x00	0x00

3

ADDRESS	0x00
Bank0, 0xA0	0x00

4

108MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x06
Bank0, 0x30	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x16
Bank0, 0x40	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x26
Bank0, 0x50	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x6C	0x36
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x80	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x82	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xB8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xB5	0x13	0x03	0x22	0xFF	0x00

54MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x04
Bank0, 0x30	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x15
Bank0, 0x40	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x24
Bank0, 0x50	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x40	0x35
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x80	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x82	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xB8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xB5	0x13	0x03	0x22	0xFF	0x00

27MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x00
Bank0, 0x30	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x11
Bank0, 0x40	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x22
Bank0, 0x50	0x60	0x00	0xAB	0x02	0x90	0x00	0x00	0x00	0x06	0x10	0x95	0x00	0x00	0x8A	0x10	0x33
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x80	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x82	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xB8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xB5	0x13	0x03	0x22	0xFF	0x00

5

ADDRESS	0x08
Bank0, 0x80	0x00

6

ADDRESS	0x0F
Bank0, 0xF0	0x01

7

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank1, 0x00	0x00	0x08	0x00	0x00	0x86	0x7A	0x7E	0x7A	0x00	0x00	-	-	-	-	-	-
Bank1, 0x10 ~ 0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Bank1, 0x90	0x00	0x00	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Bank1, 0xA0	0x00	0x03	0x6B	0x03	0x6B	0x03	0x6B	0x03	0x6B	0xAA	0xFF	0x00	0x00	0x00	0x00	-

8

ADDRESS	0x0F
Bank0, 0xF0	0x00

9

ADDRESS	0x06
Bank0, 0xF0	0x80

10

ADDRESS	0x08
Bank0, 0x80	0x00

8.1.2 Order for PAL Recommended Register Setting

◆ Audio Master Setting (Input clock : 54MHz) - 16KHz, 16bit, 16Channel, I2S, 4.096MHz

1

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xF0	0x00	0x00	0xA0	0x04	0x00	0x00	0x80	0x46	0x7B	0x20	0x00	0x80	0x80	0x49	0x37	0x00

2

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	Empty	0x00	0x22	0x88	0x88	0x84	0x33	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x80	0x00	0x00	0xC9	0x0F	0x18
Bank0, 0xC0	0x13	0x13	0x13	0x13	0x00	0x00	0x71	0x71	0x71	0x71	0x1C	0x1C	0x1C	0x1C	0x87	0x87
Bank0, 0xD0	0x87	0x87	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x80	0x10	0x80	0x10	0x00	0x00
Bank0, 0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x08	0x00	0x10	0x24	0x01	0x4B	0x00	0x00	0x00	0x00

3

ADDRESS	0x00
Bank0, 0xA0	0x00

4

108MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x06
Bank0, 0x30	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x16
Bank0, 0x40	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x26
Bank0, 0x50	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x36
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x08	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x89	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x01	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xD8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xA8	0x13	0x03	0x22	0xFF	0x00

54MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x04
Bank0, 0x30	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x15
Bank0, 0x40	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x24
Bank0, 0x50	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x35
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x08	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x89	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x01	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xD8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xA8	0x13	0x03	0x22	0xFF	0x00

27MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x00
Bank0, 0x30	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x11
Bank0, 0x40	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x22
Bank0, 0x50	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x33
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x08	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x89	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x01	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xD8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xA8	0x13	0x03	0x22	0xFF	0x00

5

ADDRESS	0x08
Bank0, 0x80	0x00

6

ADDRESS	0x0F
Bank0, 0xF0	0x01

7

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank1, 0x00	0x0D	0x08	0x00	0x01	0x90	0x70	0x7E	0x89	0x00	0x00	-	-	-	-	-	-
Bank1, 0x10 ~ 0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Bank1, 0x90	0x00	0x00	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Bank1, 0xA0	0x00	0x03	0x6B	0x03	0x6B	0x03	0x6B	0x03	0x6B	0xAA	0xFF	0x00	0x00	0x00	0x00	-

8

ADDRESS	0x0F
Bank0, 0xF0	0x00

9

ADDRESS	0x06
Bank0, 0xF0	0x80

10

ADDRESS	0x08
Bank0, 0x80	0x00

◆ Audio Master Setting (Input clock : 54MHz) - 8KHz, 16bit, 16Channel, I2S, 2.048MHz

1

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xF0	0x00	0x00	0xA0	0x00	0x00	0x00	0x80	0x46	0x7B	0x20	0x00	0x80	0x80	0x49	0x37	0x00

2

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	Empty	0x00	0x22	0x88	0x88	0x84	0x33	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x80	0x00	0x00	0xC9	0x0F	0x18
Bank0, 0xC0	0x13	0x13	0x13	0x13	0x00	0x00	0x71	0x71	0x71	0x71	0x1C	0x1C	0x1C	0x1C	0x87	0x87
Bank0, 0xD0	0x87	0x87	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x80	0x10	0x80	0x10	0x00	0x00
Bank0, 0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x08	0x00	0x10	0x24	0x01	0x4B	0x00	0x00	0x00	0x00

3

ADDRESS	0x00
Bank0, 0xA0	0x00

4

108MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x06
Bank0, 0x30	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x16
Bank0, 0x40	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x26
Bank0, 0x50	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x6C	0x36
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x08	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x89	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x01	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xD8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xA8	0x13	0x03	0x22	0xFF	0x00

54MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x04
Bank0, 0x30	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x15
Bank0, 0x40	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x24
Bank0, 0x50	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x44	0x35
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x08	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x89	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x01	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xD8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xA8	0x13	0x03	0x22	0xFF	0x00

27MHz Data Output of Video Decoder

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x10	0x32	0x10	0x32	0x10	0x32	0x00	0x00	0x00
Bank0, 0x10	0x00	0xEF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x72	0x00	0x00	0x00	0x00
Bank0, 0x20	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x00
Bank0, 0x30	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x11
Bank0, 0x40	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x22
Bank0, 0x50	0xBD	0x00	0xBE	0x00	0x7E	0x00	0x00	0x00	0x07	0x10	0xAC	0x00	0x00	0x0F	0x04	0x33
Bank0, 0x60	0xD0	0x80	0x40	0x7C	0x9F	0x00	0x20	0x40	0x80	0x50	0x08	0x0F	0x0C	0x01	0x15	0x0A
Bank0, 0x70	0x89	0x23	0x88	0x04	0x2A	0xCC	0xF0	0x2F	0x57	0x43	0x10	0x88	0x01	0x63	0x01	0x00
Bank0, 0x80	0x80	0x00	0x00	0x81	0x01	0x00	0x00	0x00	0x00	0x20	0x04	0x2E	0x00	0x30	0xD8	0x01
Bank0, 0x90	0x06	0x06	0x11	0xB9	0xB2	0x05	0x00	0x28	0x50	0x51	0xA8	0x13	0x03	0x22	0xFF	0x00

5

ADDRESS	0x08
Bank0, 0x80	0x00

6

ADDRESS	0x0F
Bank0, 0xF0	0x01

7

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank1, 0x00	0x0D	0x08	0x00	0x01	0x90	0x70	0x7E	0x89	0x00	0x00	-	-	-	-	-	-
Bank1, 0x10 ~ 0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Bank1, 0x90	0x00	0x00	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Bank1, 0xA0	0x00	0x03	0x6B	0x03	0x6B	0x03	0x6B	0x03	0x6B	0xAA	0xFF	0x00	0x00	0x00	0x00	-

8

ADDRESS	0x0F
Bank0, 0xF0	0x00

9

ADDRESS	0x06
Bank0, 0xF0	0x80

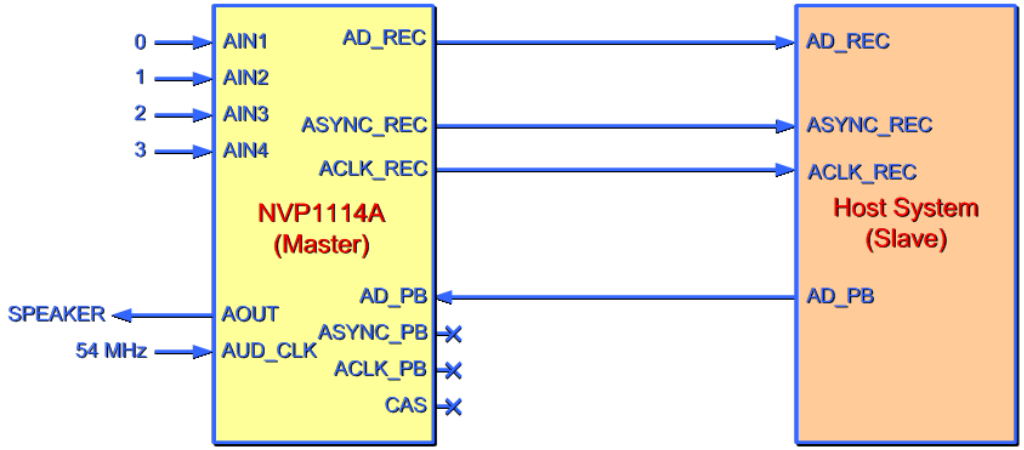
10

ADDRESS	0x08
Bank0, 0x80	0x00

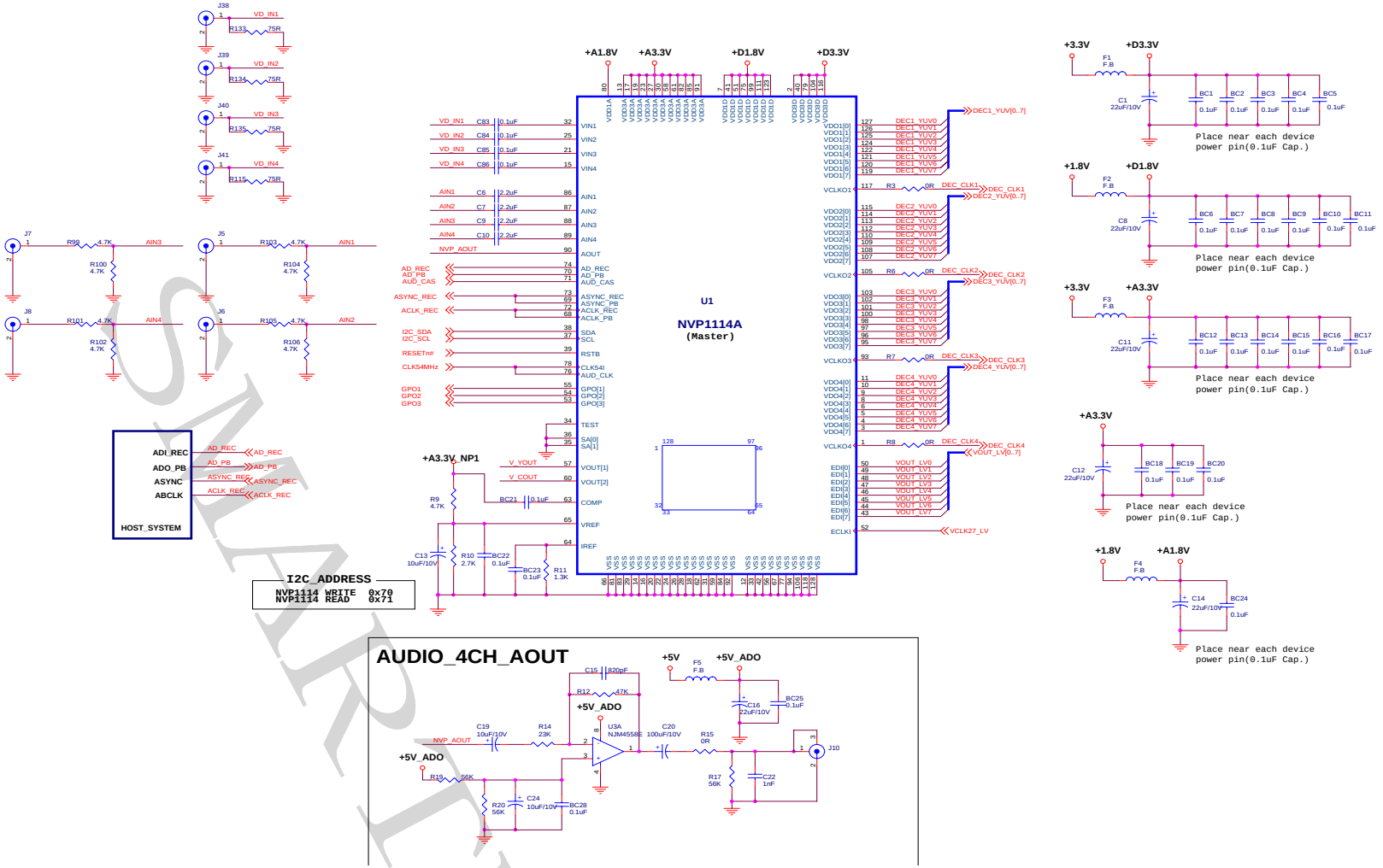
8.2 Index of System Application

8.3 4 Channel, Master Mode

8.3.1 Block Diagram (4 Channel, I²S Master Mode)

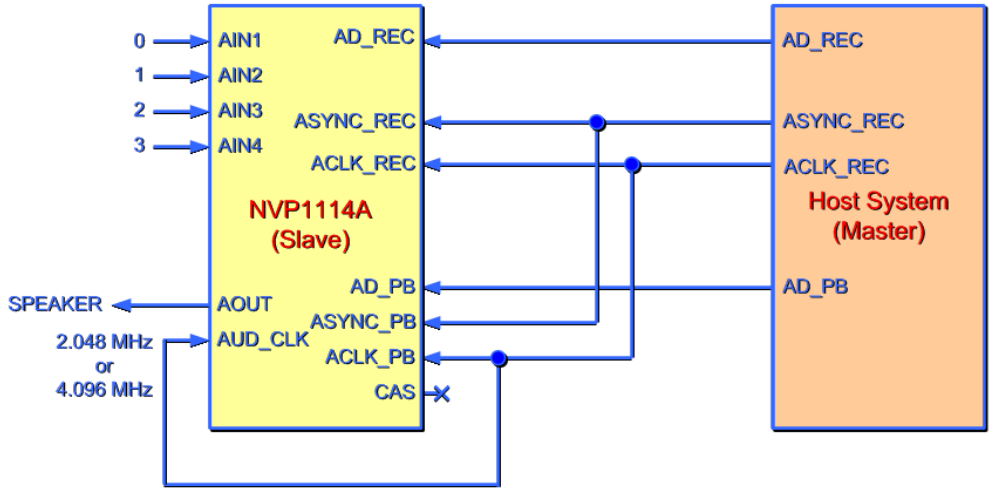


8.3.2 Circuit Configuration (4 Channel, I²S Master Mode)

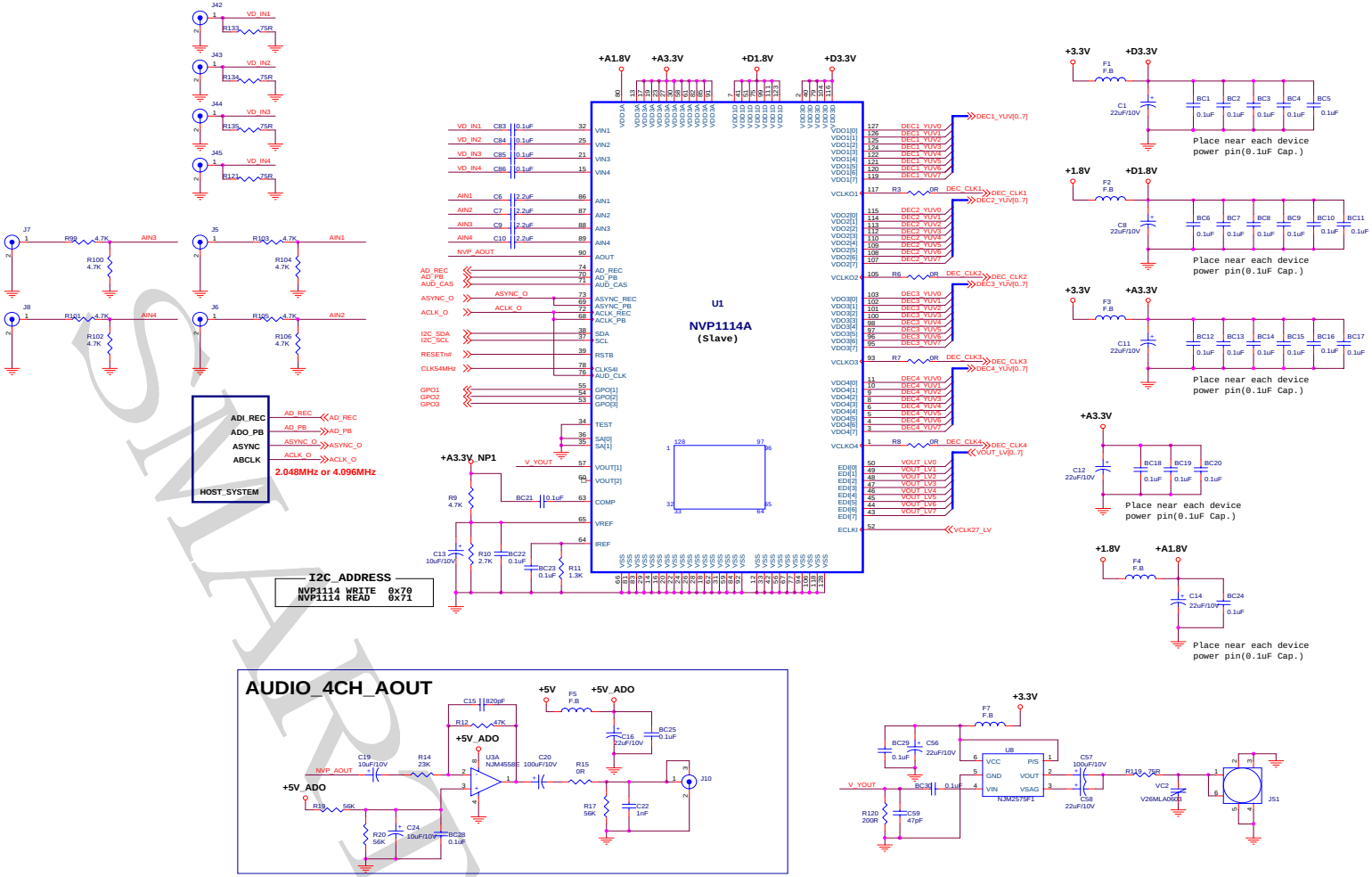


8.4 4 Channel, Slave Mode

8.4.1 Block Diagram (4 Channel, I²S Slave Mode)



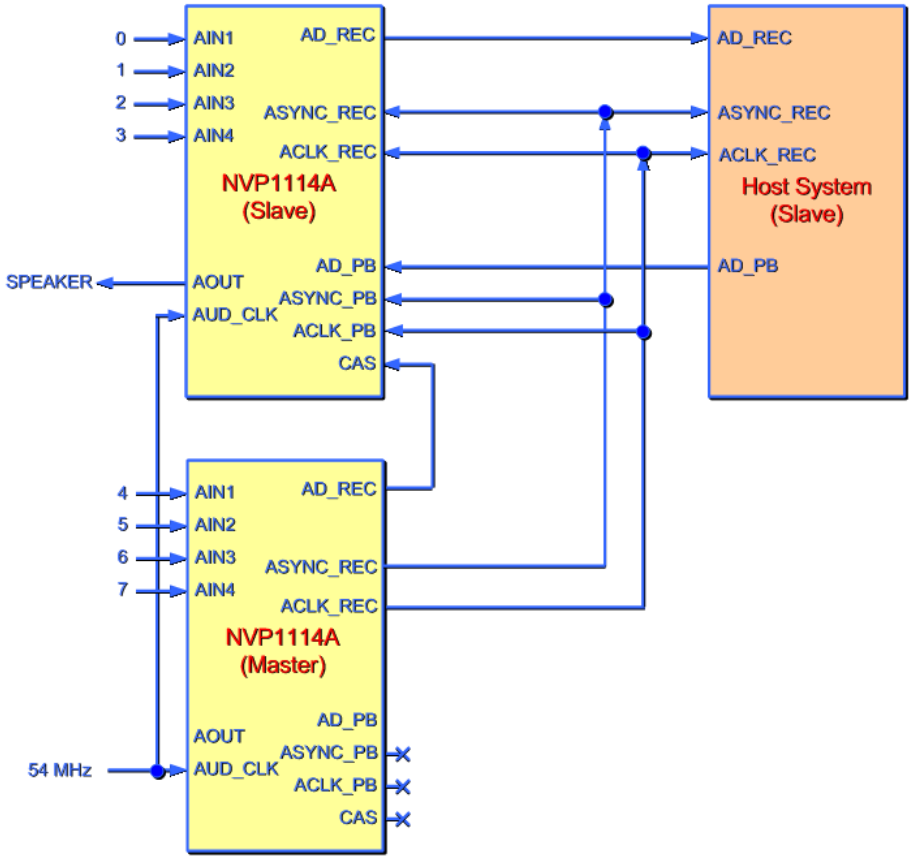
8.4.2 Circuit Configuration (4 Channel, I²S Slave Mode)



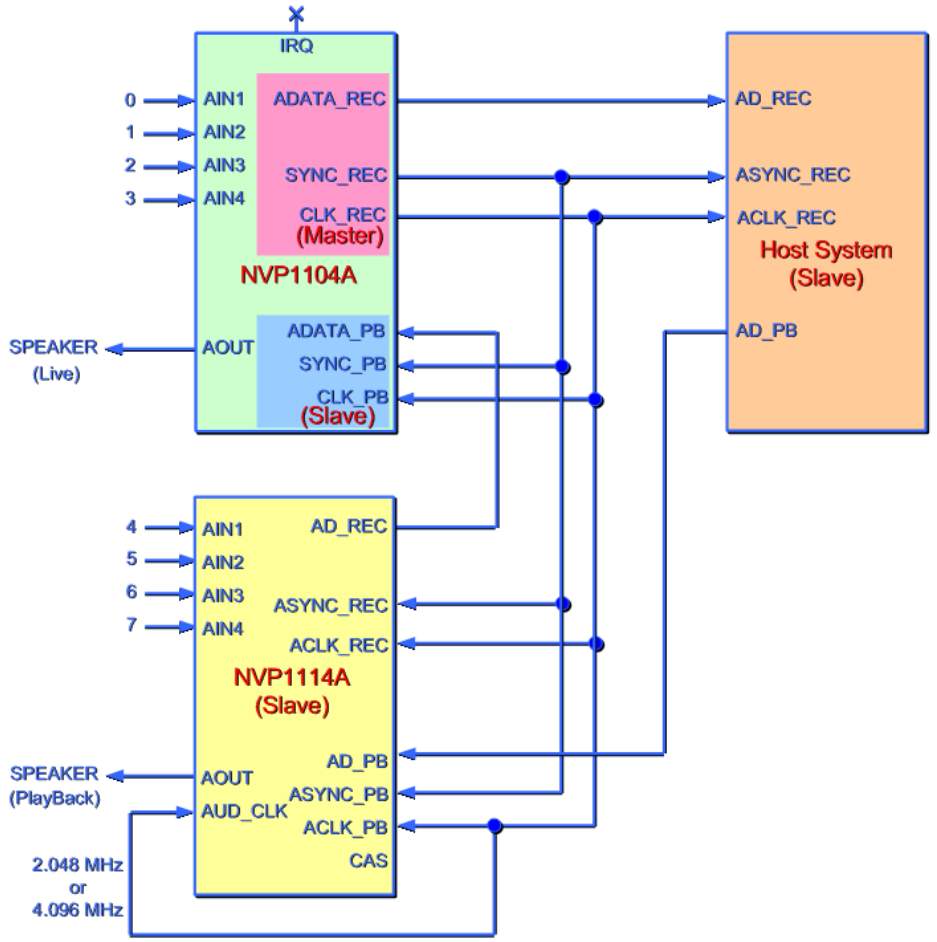
8.5 8 Channel, Master Mode

8.5.1 Block Diagram

8.5.1.1 NVP1114A Only (8 Channel, I²S Master Mode)

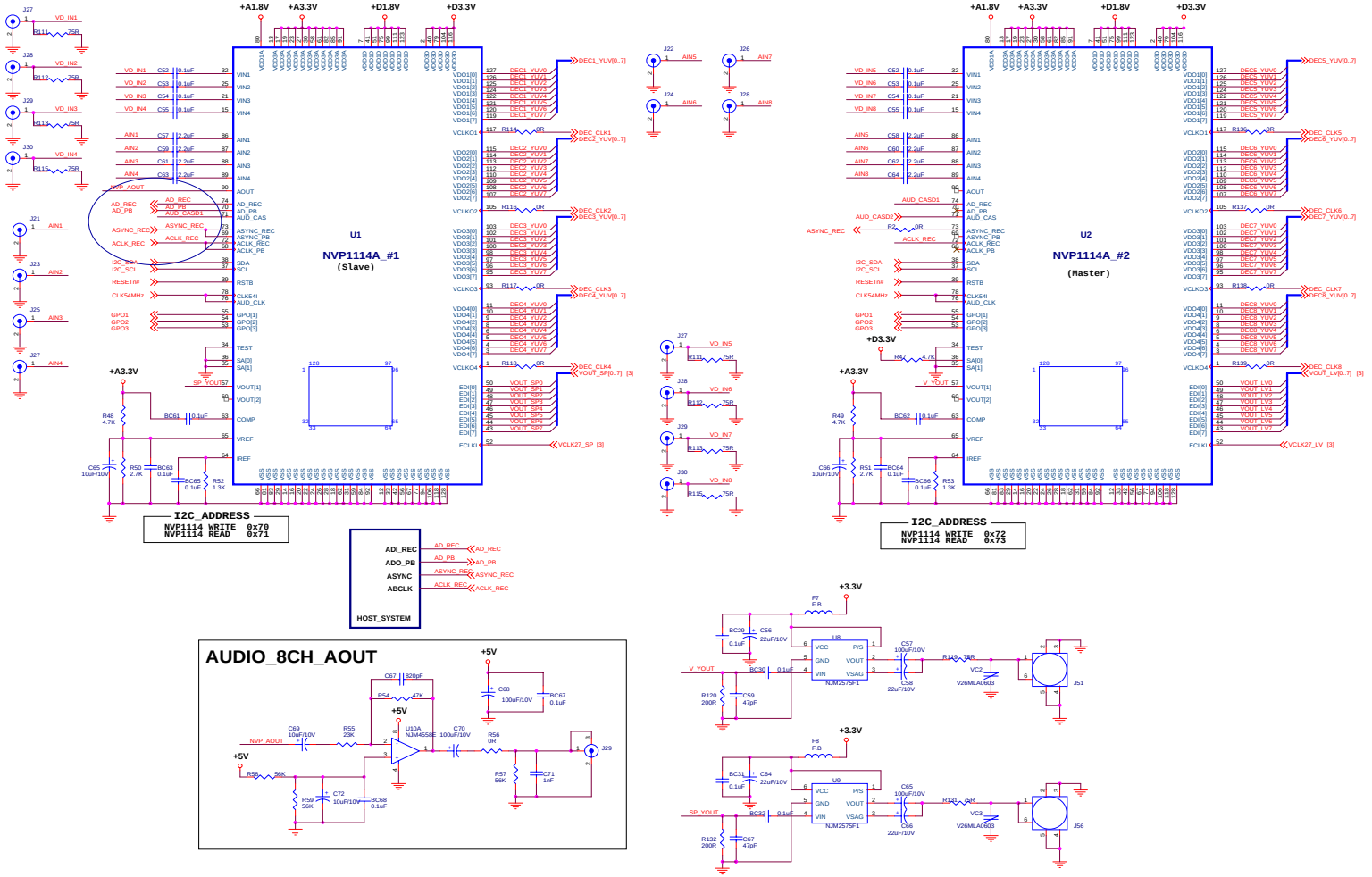


8.5.1.2 NVP1114A + NVP1104A (8 Channel, I²S Master Mode)

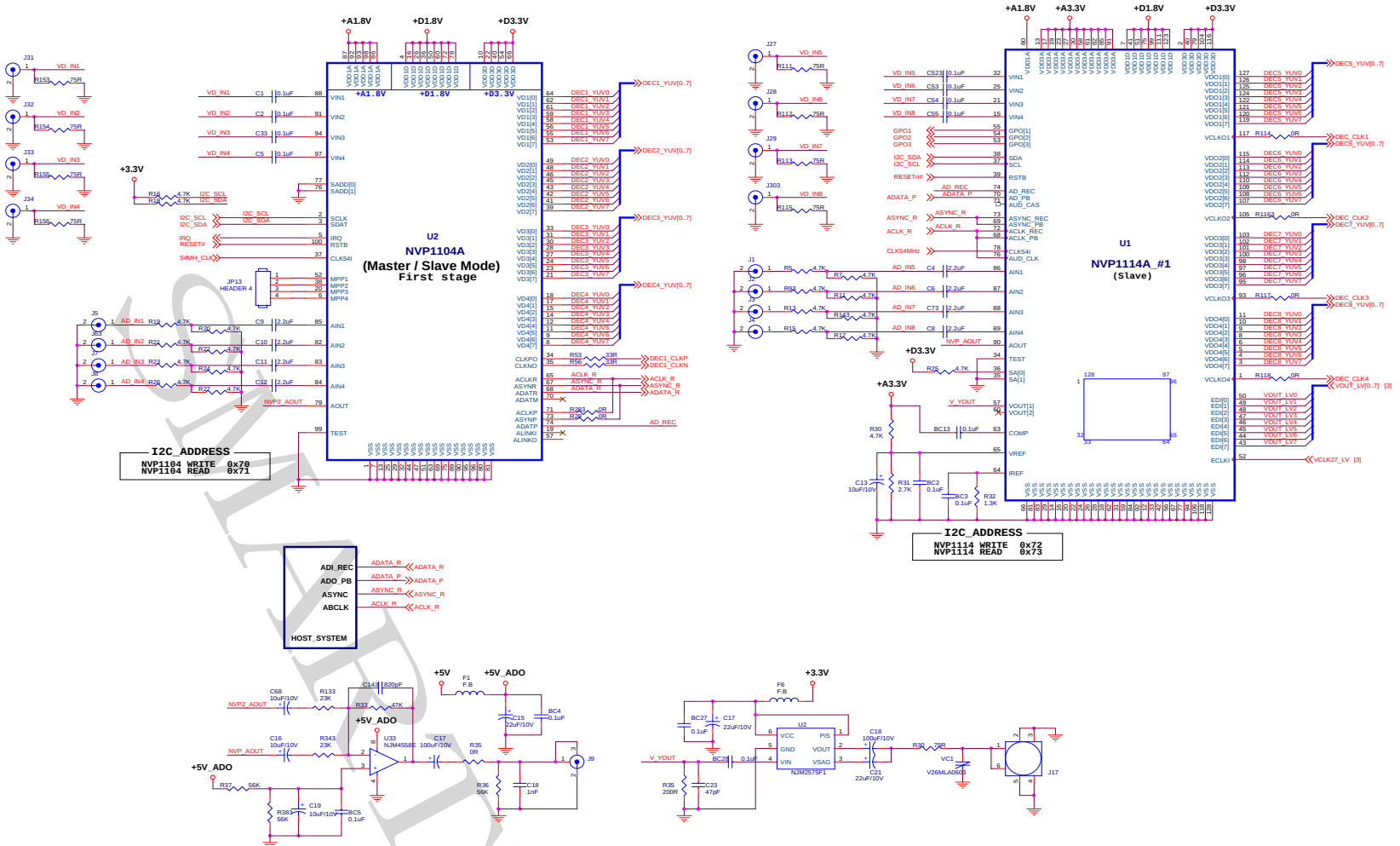


8.5.2 Circuit Configuration

8.5.2.1 NVP1114A Only (8 Channel, I²S Master Mode)



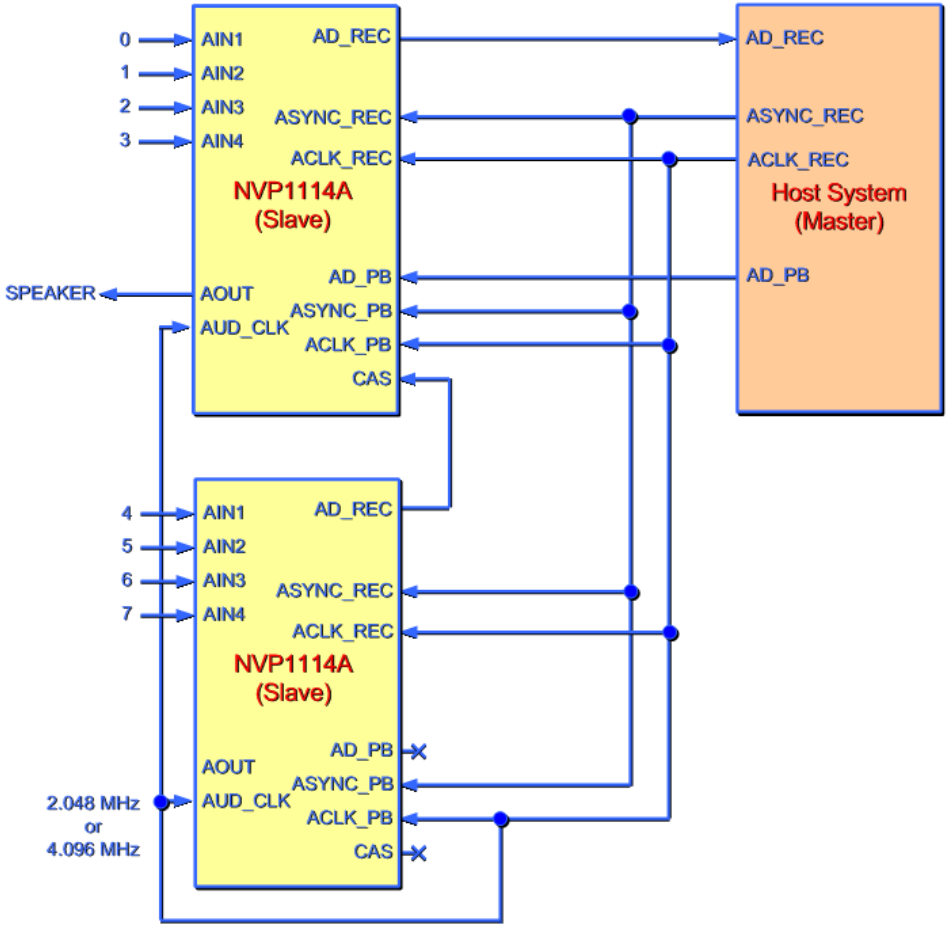
8.5.2.2 NVP1114A + NVP1104A (8 Channel, I²S Master Mode)



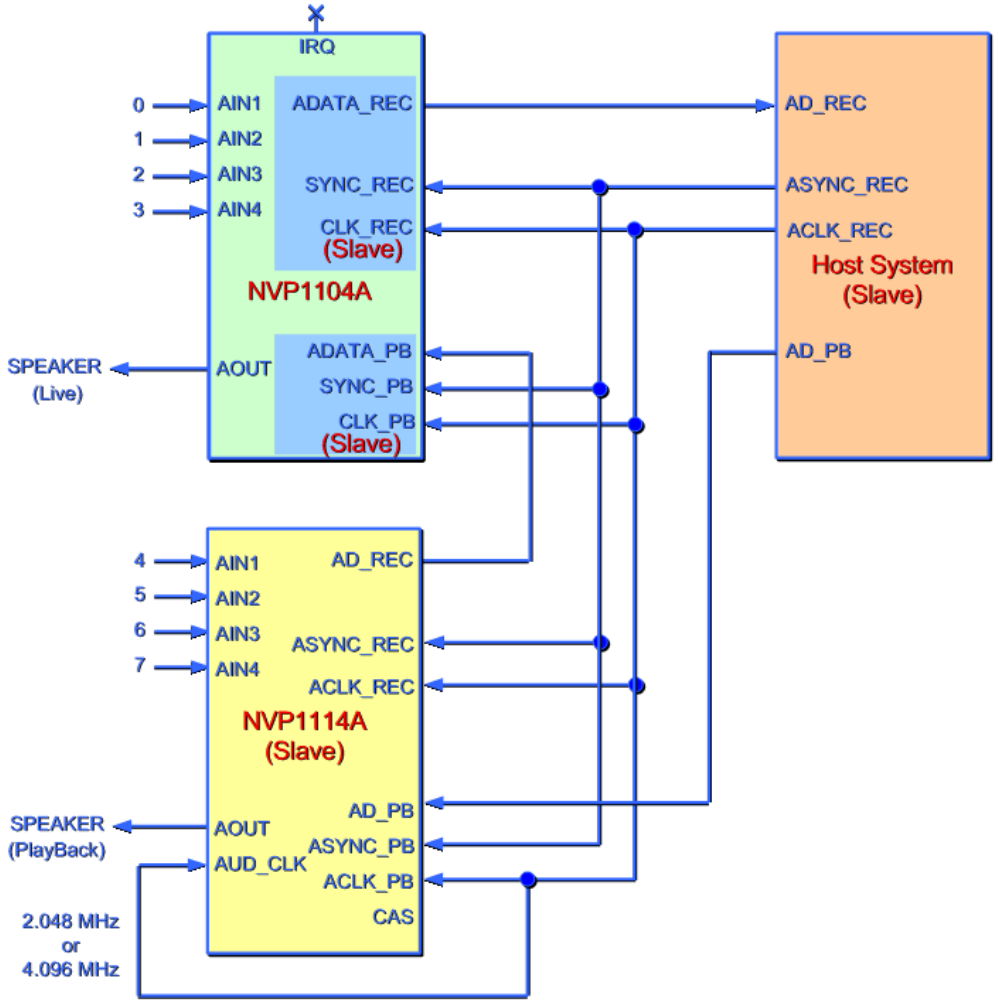
8.6 8 Channel, Slave Mode

8.6.1 Block Diagram

8.6.1.1 NVP1114A Only (8 Channel, I^2S Slave Mode)

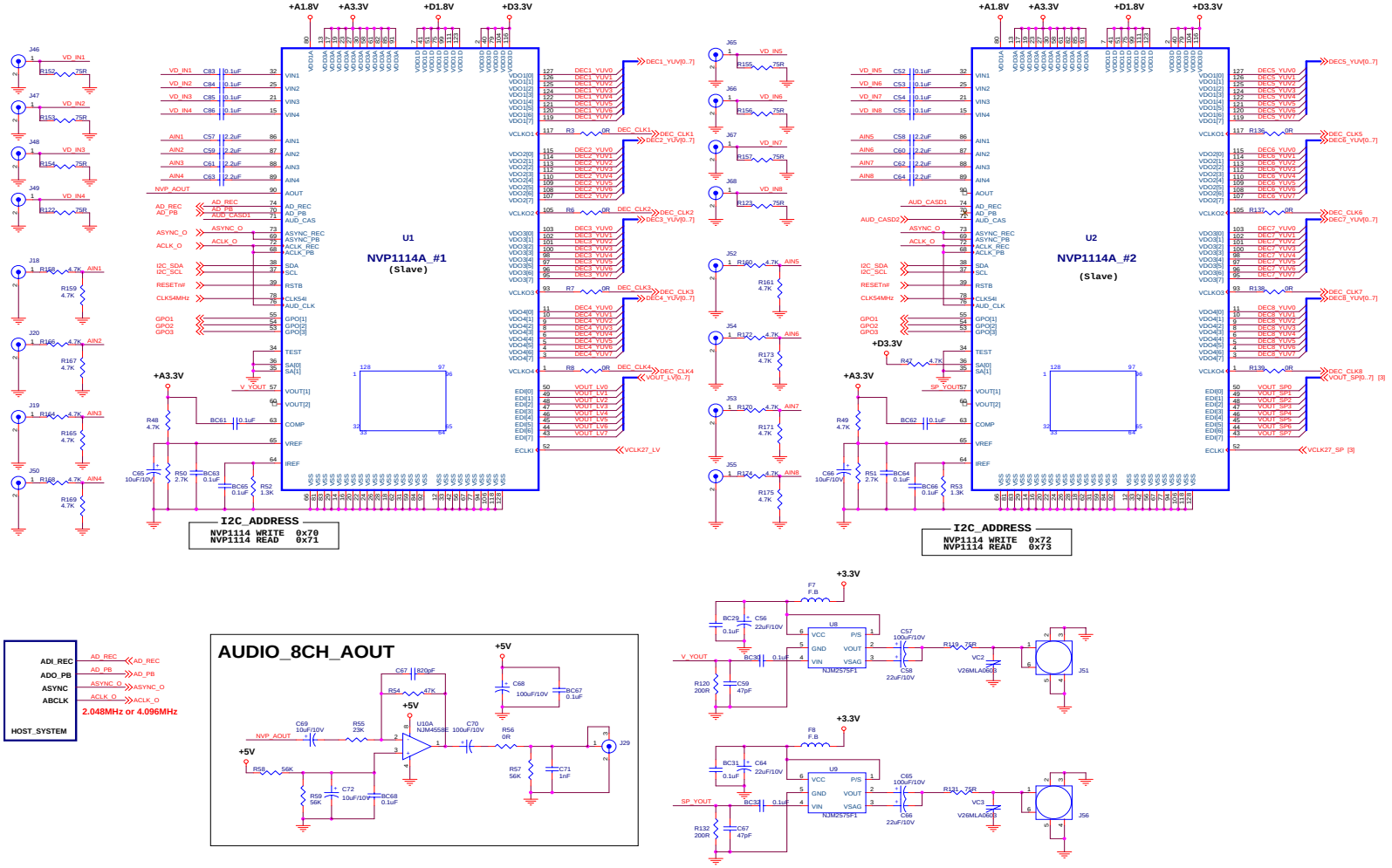


8.6.1.2 NVP1114A + NVP1104A (8 Channel, I²S Slave Mode)

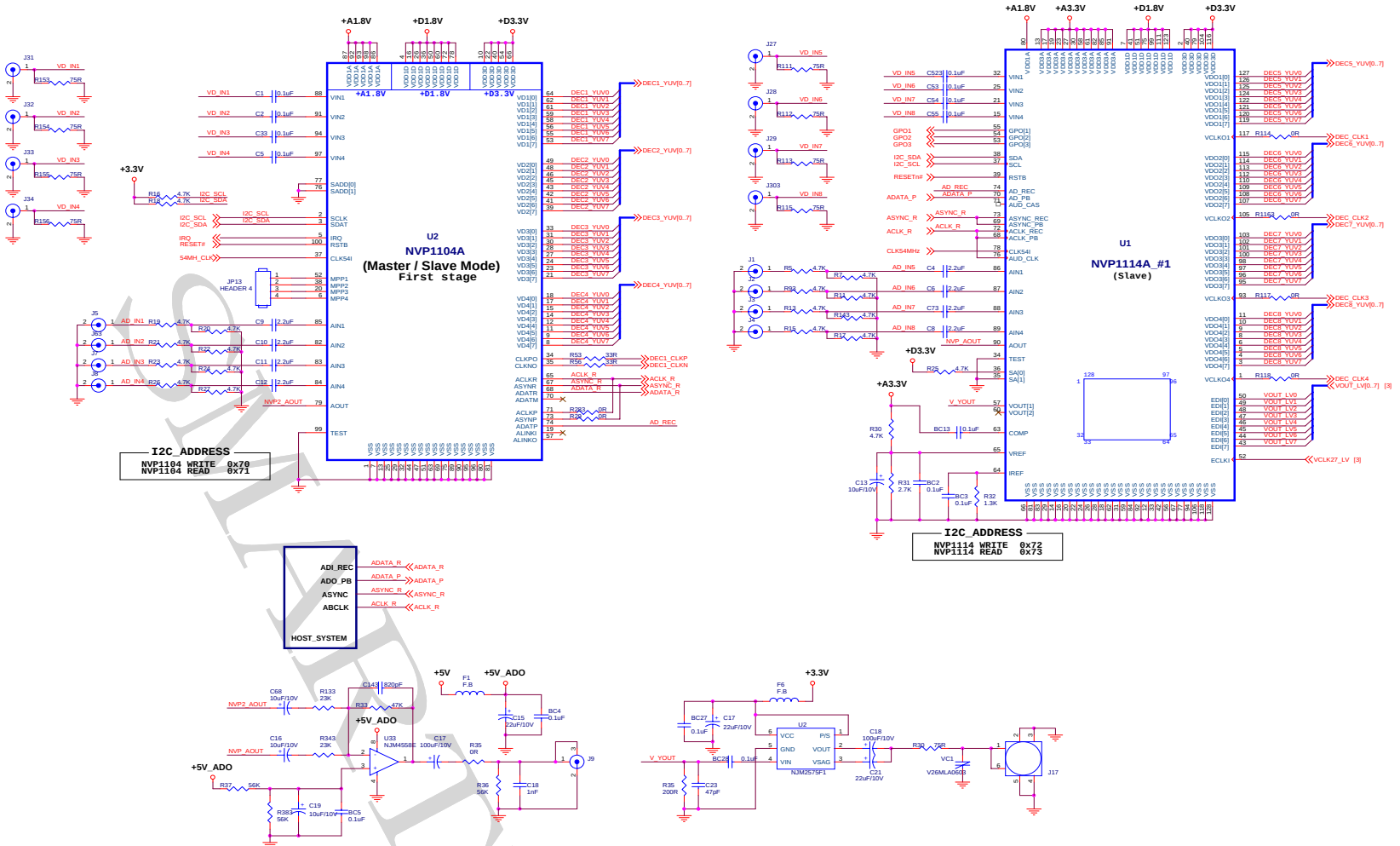


8.6.2 Circuit Configuration

8.6.2.1 NVP1114A Only (8 Channel, I²S Slave Mode)



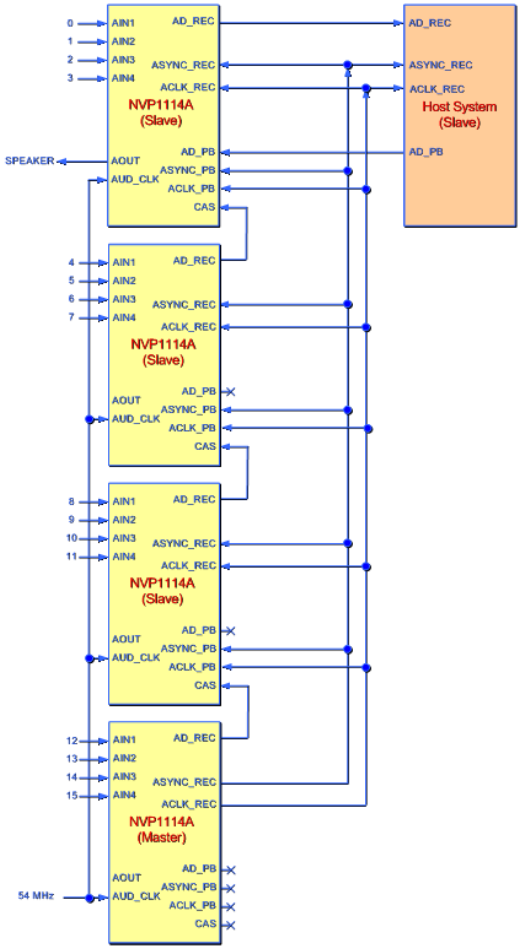
8.6.2.2 NVP1114A + NVP1104A (8 Channel, I²S Slave Mode)



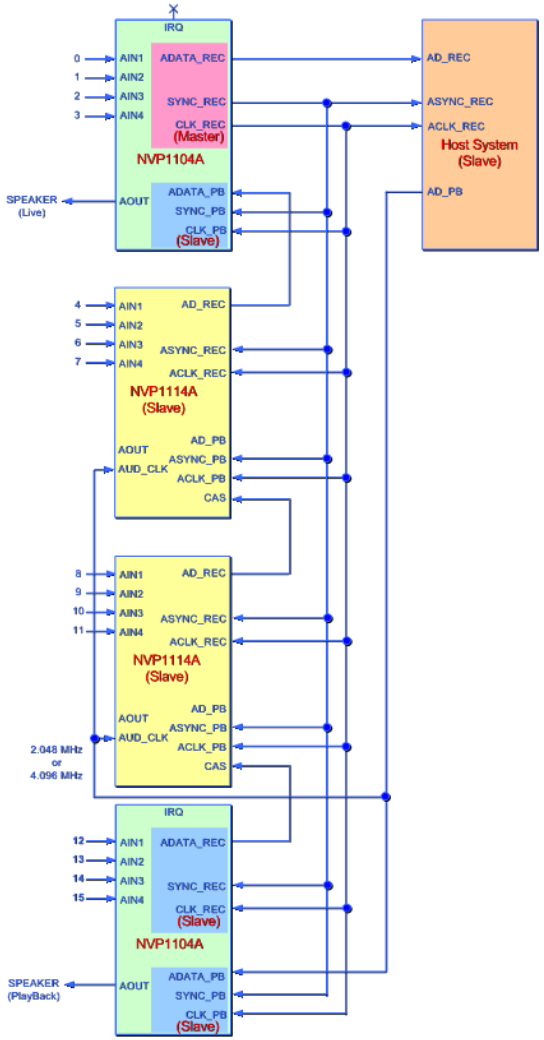
8.7 16 Channel, Master Mode

8.7.1 Block Diagram

8.7.1.1 NVP1114A Only (16 Channel, I²S Master Mode)

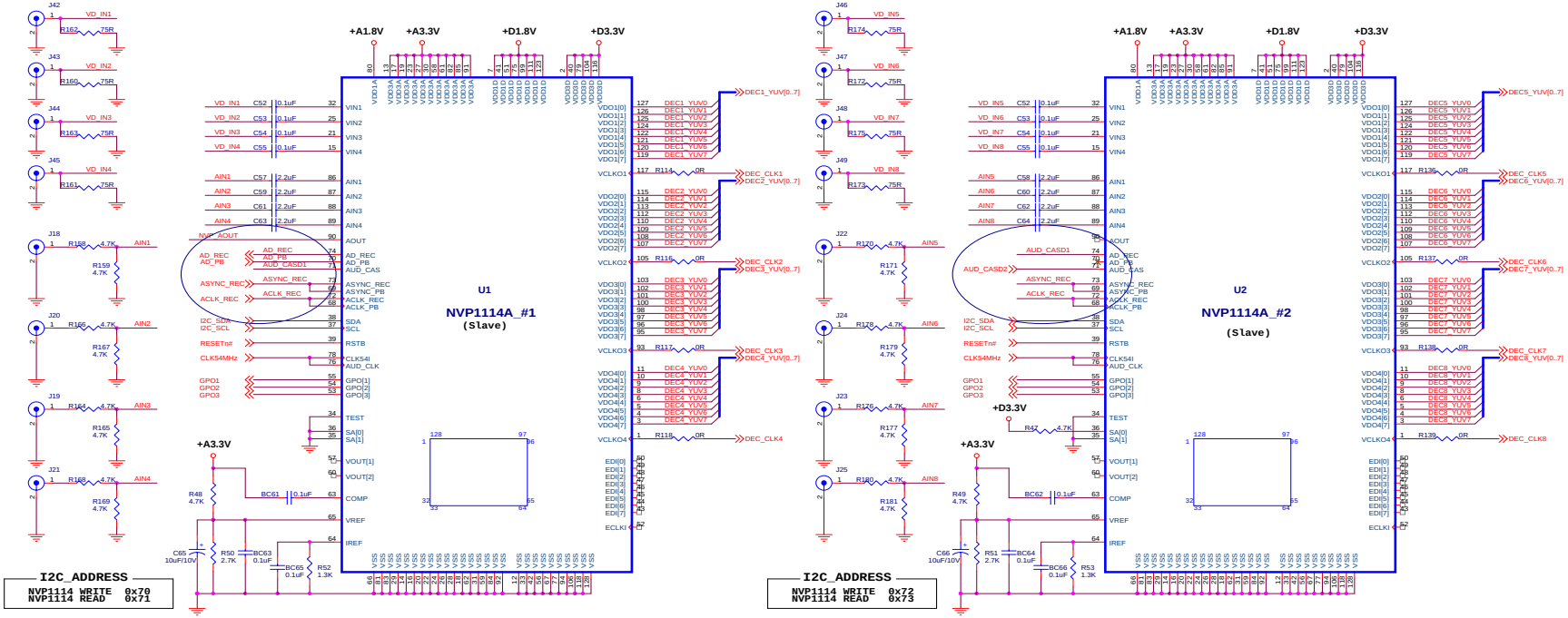


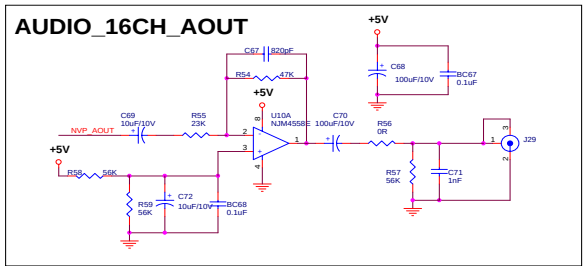
8.7.1.2 NVP1114A + NVP1104A (16 Channel, I²S Master Mode)

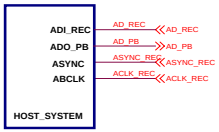


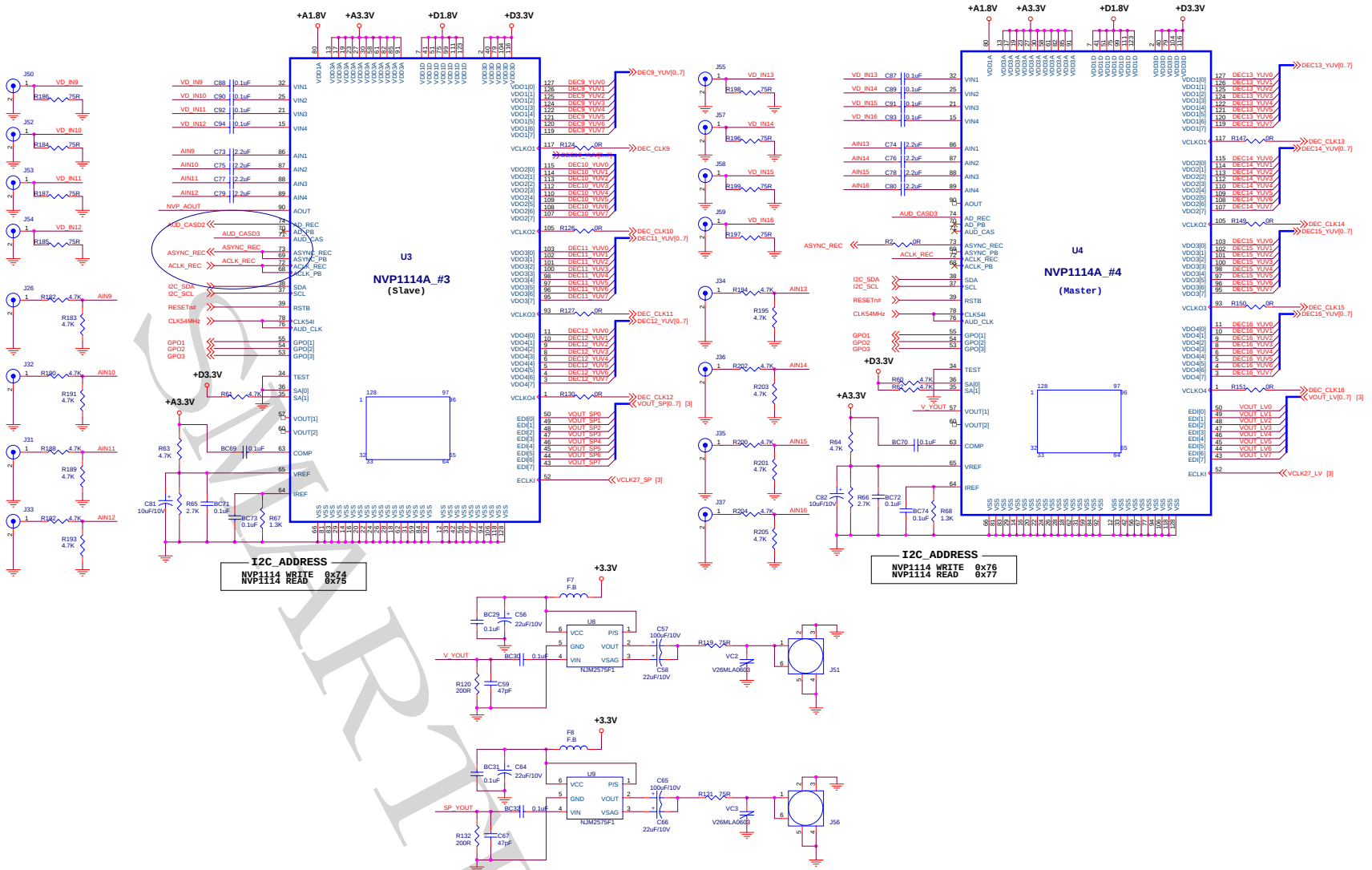
8.7.2 Circuit Configuration

8.7.2.1 NVP1114A Only (16 Channel, I²S Master Mode)

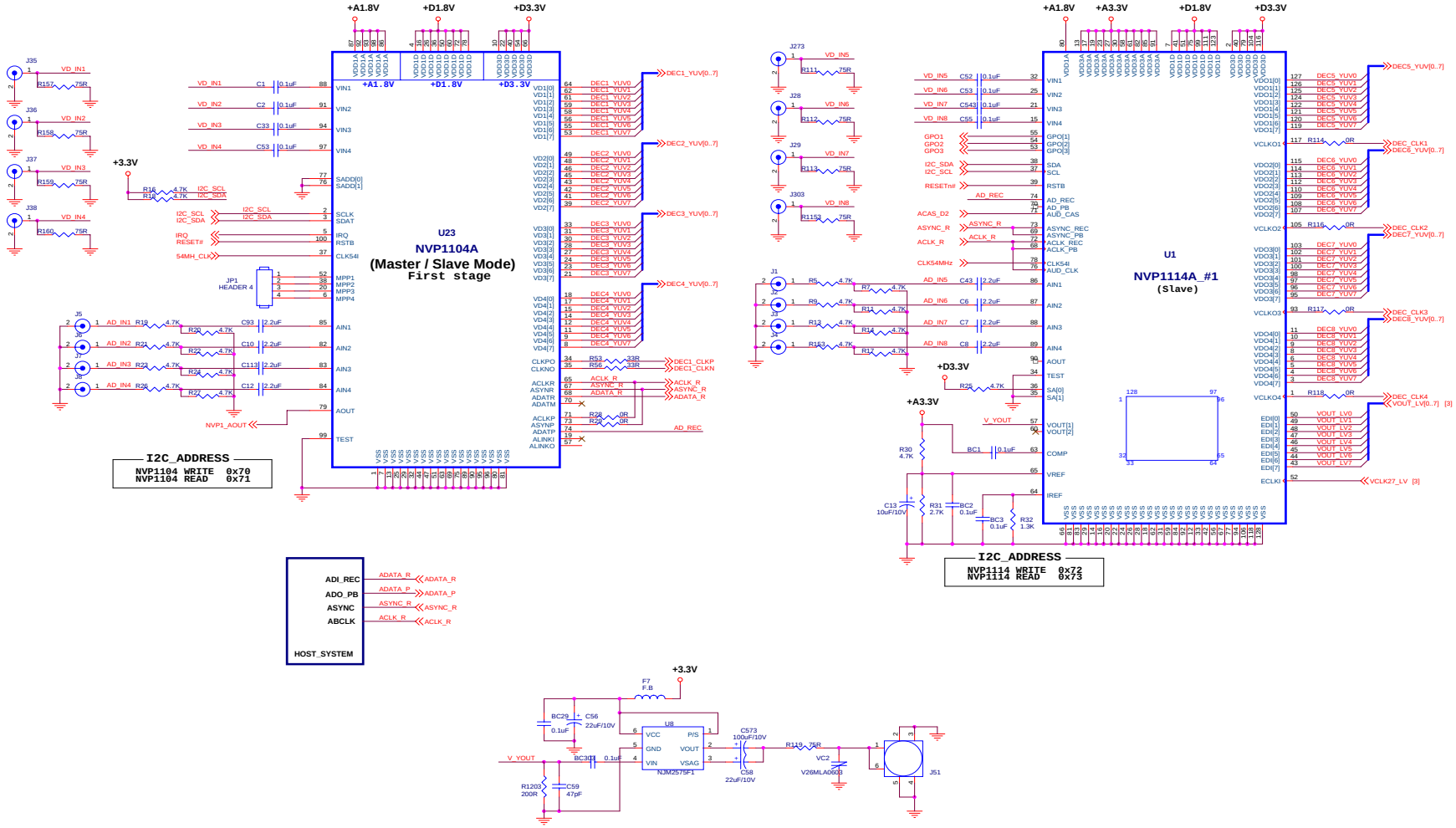


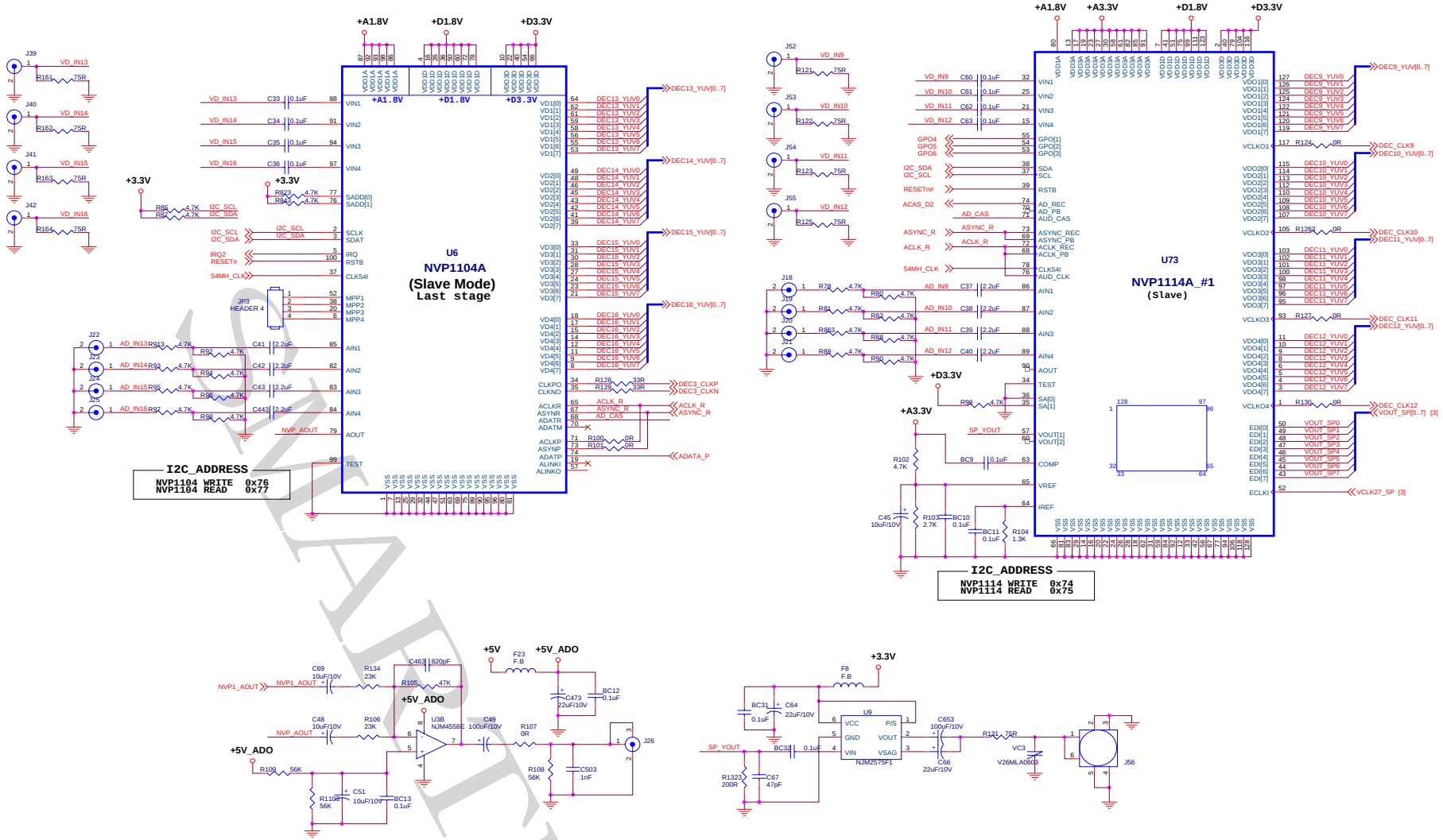





U3
NVP1114A_#3
(Slave)
U4
NVP1114A_#4
(Master)
I2C_ADDRESS
NVP1114 WRITE 0x74
NVP1114 READ 0x75
I2C_ADDRESS
NVP1114 WRITE 0x76
NVP1114 READ 0x77
+A1.8V
+A3.3V
+D1.8V
+D3.3V
NJM2575F1

8.7.2.2 NVP1114A + NVP1104A (16 Channel, I²S Master Mode)

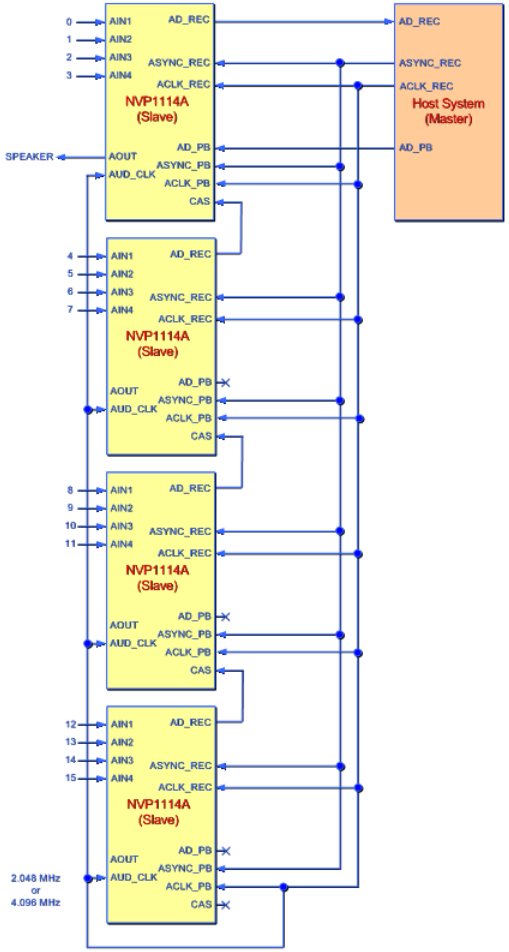



U6
NVP1104A
(Slave Mode)
Last stage
I2C_ADDRESS
NVP1104 WRITE 0x76
NVP1104 READ 0x77
U73
NVP1114A_#1
(Slave)
I2C_ADDRESS
NVP1114 WRITE 0x74
NVP1114 READ 0x75
+A1.8V
+D1.8V
+D3.3V
+A3.3V
+3.3V
+5V
+5V_ADO

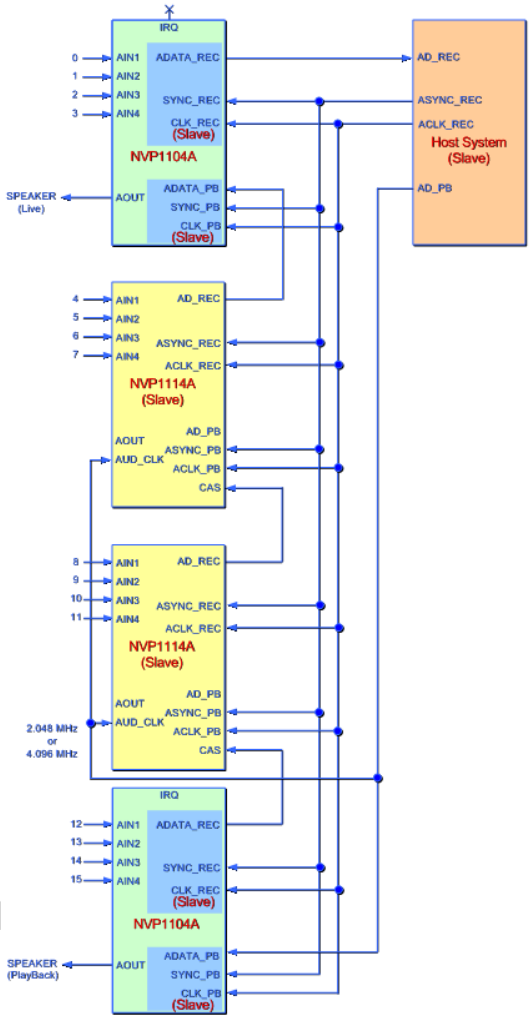
8.8 16 Channel, Slave Mode

8.8.1 Block Diagram

8.8.1.1 NVP1114A Only (16 Channel, I²S Slave Mode)

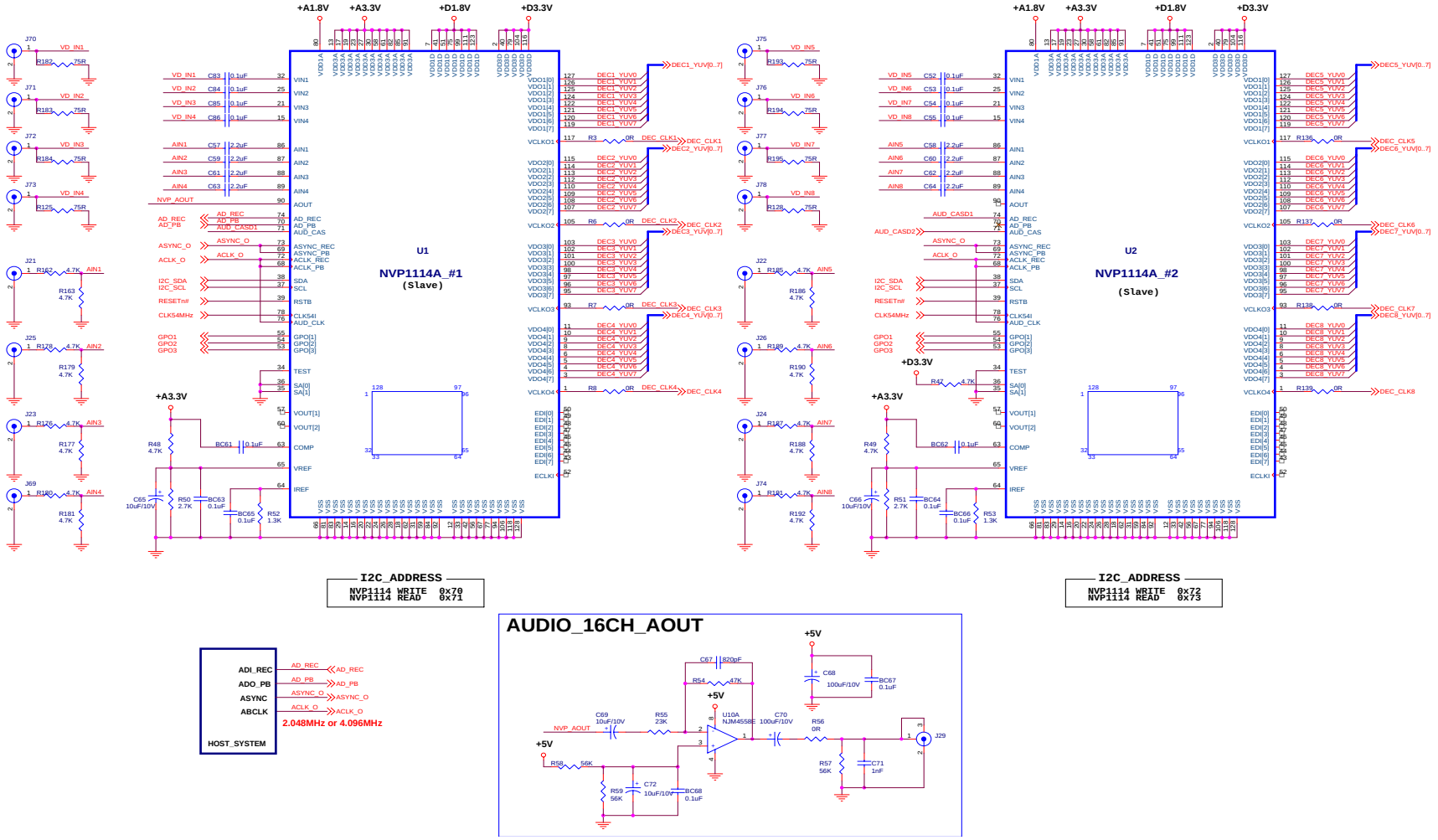


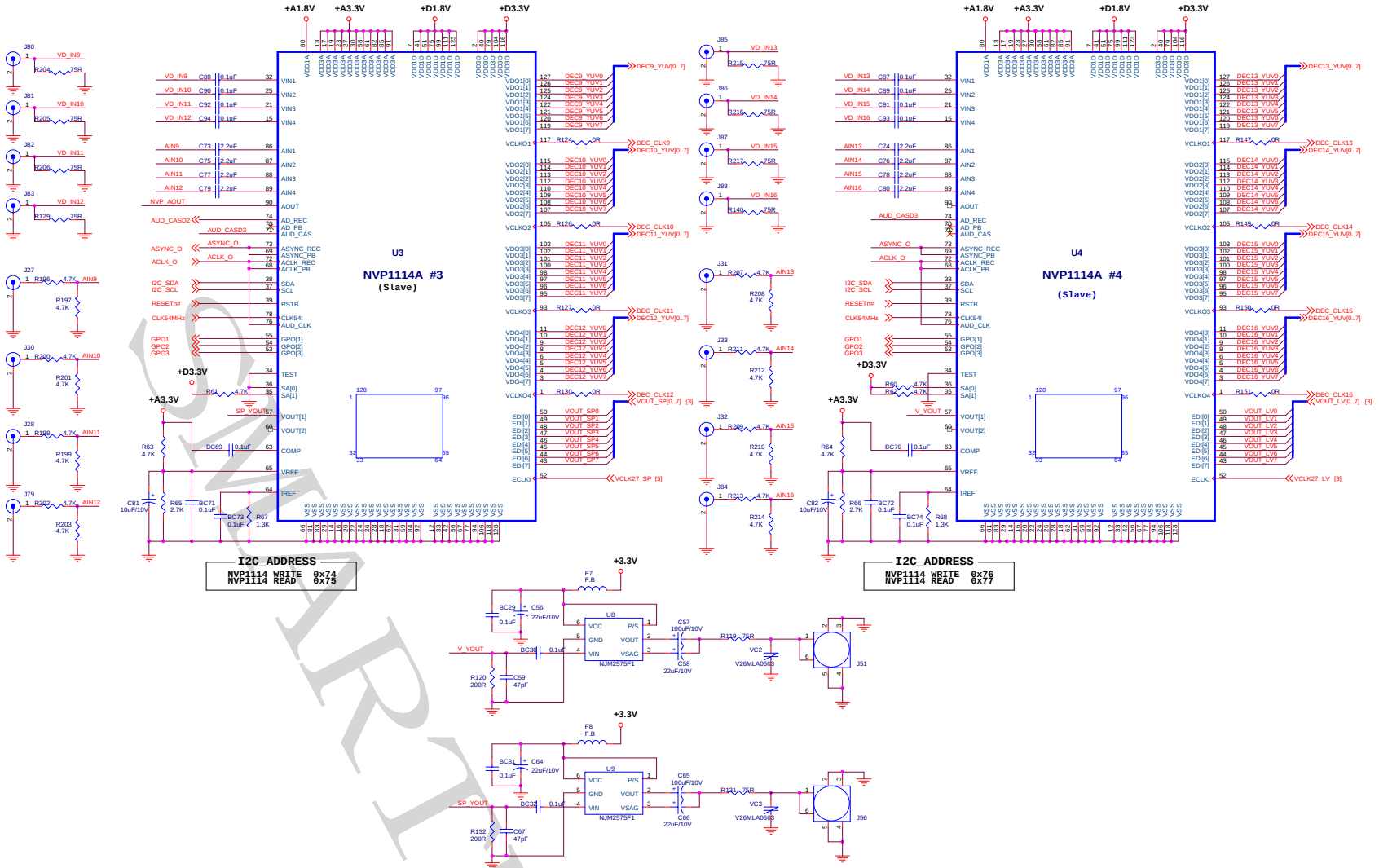
8.8.1.2 NVP1114A + NVP1104A (16 Channel, I²S Slave Mode)



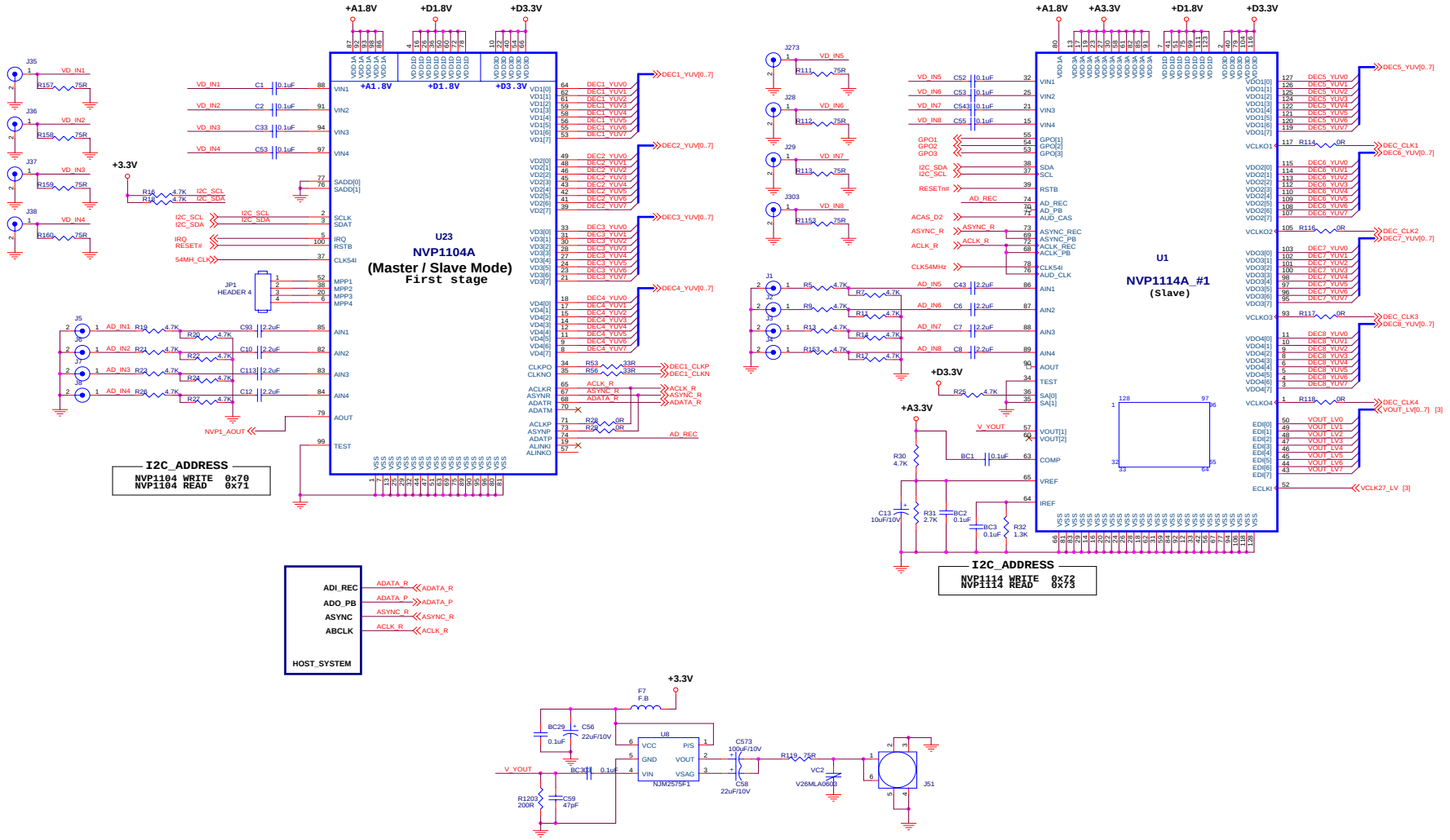
8.8.2 Circuit Configuration

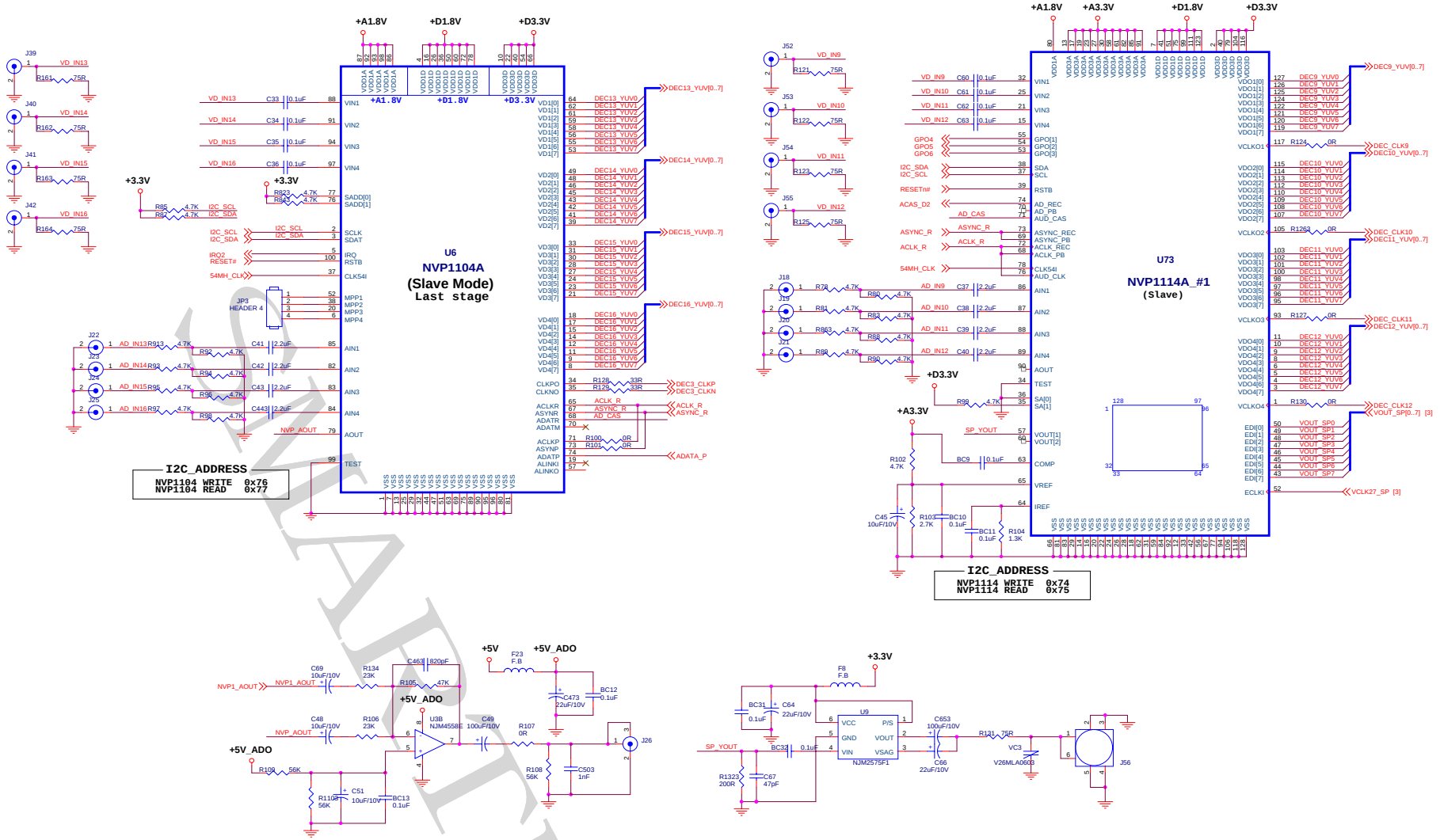
8.8.2.1 NVP1114A Only (16 Channel, I²S Slave Mode)




+A1.8V
+A3.3V
+D1.8V
+D3.3V
U3
NVP1114A_#3
(Slave)
U4
NVP1114A_#4
(Slave)
I2C_ADDRESS
NVP1114 WRITE 0x74
NVP1114 READ 0x75
I2C_ADDRESS
NVP1114 WRITE 0x76
NVP1114 READ 0x77
+3.3V
NJM2575F1

8.8.2.2 NVP1114A + NVP1104A (16 Channel, I²S Slave Mode)




U6
NVP1104A
(Slave Mode)
Last stage
I2C_ADDRESS
NVP1104 WRITE 0x76
NVP1104 READ 0x77
U73
NVP1114A_#1
(Slave)
I2C_ADDRESS
NVP1114 WRITE 0x74
NVP1114 READ 0x75
+A1.8V
+D1.8V
+D3.3V
+A3.3V
+5V
+5V_ADO
+3.3V

8.9 Register Setting

8.9.1 16 Channel, 16bit@16KHz, I2S Master/Slave Mode (NVP1114A Only)

◆ Master Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x04	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x84	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x04	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x04	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x04	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x04	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.9.2 16 Channel, 8bit@16KHz, I2S Master/Slave Mode (NVP1114A Only)

◆ Master Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x06	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x86	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x06	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x06	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x06	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x06	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.9.3 16 Channel, 16bit@8KHz, I2S Master/Slave Mode (NVP1114 Only)

◆ Master Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x00	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x80	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x00	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x00	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x00	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x00	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.9.4 16 Channel, 8bit@8KHz, I2S Master/Slave Mode (NVP1114A Only)

◆ Master Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1114A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.9.5 16 Channel, 16bit@16KHz, I2S Master/Slave Mode (NVP1114A + NVP1104A)

◆ Master Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x84	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x04	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x04	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x04	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x04	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x04	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x04
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.9.6 16 Channel, 8bit@16KHz, I2S Master/Slave Mode (NVP1114A + NVP1104A)

◆ Master Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x86	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x06	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x06	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x06	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x06	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x06	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x06
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.9.7 16 Channel, 16bit@8KHz, I2S Master/Slave Mode (NVP1114A + NVP1104A)

◆ Master Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x80	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x00	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x00	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x00	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x00	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A middle stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x00	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x00
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.9.8 16 Channel, 8bit@8KHz, I2S Master/Slave Mode (NVP1114A + NVP1104A)

◆ Master Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x82	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x02	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

◆ Slave Mode

NVP1104A first stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x02	0x23	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

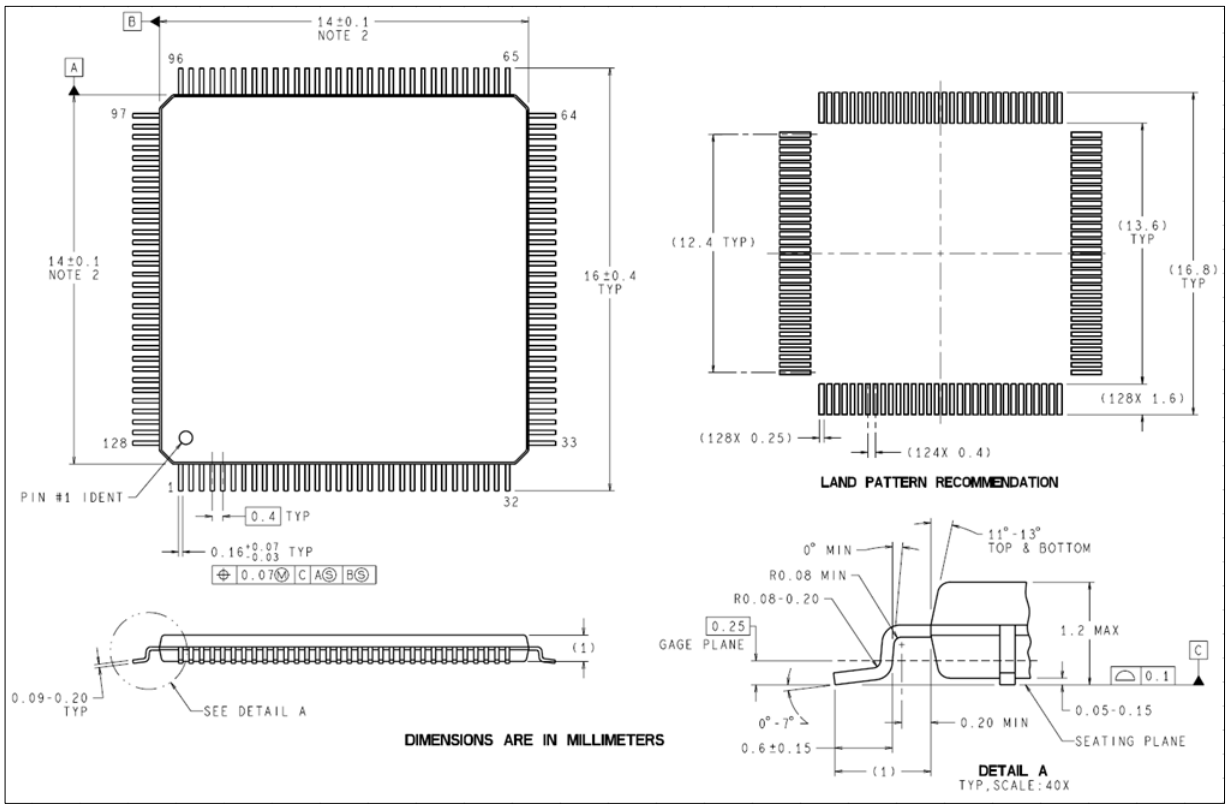
NVP1104A last stage Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x04	0x20	0x00	0x00	0x02	0x13	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x10	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0x49	0x3F	0x17

NVP1114A Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Bank0, 0xA0	-	0x00	0x22	0x00	0x00	0x02	0x03	0x01	0x23	0x45	0x67	0x89	0xAB	0xCD	0xEF	0x02
Bank0, 0xB0	0x00	0x88	0x88	0x88	0x14	0x0F	0xAA	0xAA	0x02	0x00	0x00	0x00	0x00	0xC9	0x0F	0x18

8.10 Package Information



9. Revision History

REV	Date	Description
Preliminary 0.0	2009.05.12.	Generated
Preliminary 1.0	2009.07.17.	Add information about scaler and explanation for registers

10. Contact Information

-. www.nextchip.com

-. sales@nextchip.com (82-2-3460-4702), Gideon Park.