NVP1918

8-CH 960H Video Decoders and Audio Codecs with Video Encoder

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REV 0.0

[주]넥스트칩 nextchip

Revision History

VERSION	DATE	DESCRIPTION	NOTE
REV 0.0	2012-04-23	- Initial Draft	

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8 CH 960H Video Decoders and Audio Codecs with Video Encoder

NVP1918 includes 8-Channel 720H/960H Video Decoders and 10-Channel Audio Codecs with 720H/960H Video Encoder. 8-Channel 720H/960H Video Decoder delivers high quality images. It accepts separate 8 CVBS inputs from Camera, TV, DVD and the other video signal sources. It digitizes and decodes NTSC/PAL video signal into digital video components which represents 8-bit BT.1302 4:2:2 format with 36MHz or 72MHz/144MHz multiplexed. **NVP1918** includes Clock PLL, so 72/144MHz time multiplexed function available.

720H/960H Video Encoder plays the roles of converting the 8bit BT.656/BT.1302 format data into CVBS or S-Video in 10bit resolution. And there is 2 Channel DAC which is fed from the above Video Encoder.

10-Channel Audio Codec is 8-Channel Voice/2-Channel Mic PCM Codec which handles voice band signals(300Hz~3400Hz) with 8bit/16bit linear PCM, 8bit G.711(u-law, A-law) PCM. Built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

8-Channel Coaxial Communication Protocol communicates between controller(DVR) and camera on the video signal through coaxial cable.

Features

Video Decoder

-. 8-Ch Video Decoder which accepts 8-CVBS
-. Output in BT.1302 4:2:2 format with 36/72/144MHz
-. Each Video Output Port 720H/960H Selectable
-. On Chip Analog CLAMP/PGA and Anti-aliasing Filter
-. Accepts NTSC-M/J/4.43, PAL-B/D/G/H/I/K/L/M/N/60
-. Robust Sync detection for weak, non-standard signals
-. High-performance 3H/5H 2D adaptive comb filter and Notch Filter
-. Programmable H/V Peaking filter for Luminance
-. CTI (Chrominance Transient Improvement)
-. Color compensation for PAL
-. IF compensation filter
-. Robust No-video detection
-. Programmable Brightness, Contrast, Saturation and Hue
-. Programmable Picture Quality Control
-. Black/White Detection

Audio Codec

-. 8-Ch Voice / 2-Ch Mic Record, 1-Ch Playback
-. 10bit pipe-line ADC / ΔΣ DAC
-. Input / Output Analog Gain Control
-. Linear PCM (8bit/16bit, 8K/16K/32K)
-. G.711 a-law/u-law (8bits, 8K/16K/32K)
-. Input Mixing, Digital Volume, Mute Detection
-. SSP/DSP/I2S Interface (Master/Slave mode)
-. Cascade mode (up to 2 cascade support)
  - 16Channel recording (with 4channel mic recording), mixing output, playback

Video Encoder

-. Support NTSC/PAL 960H/720H Encoding
-. BT.656 / BT.1302 Input
-. 2 Analog Outputs
  - 2 * 10bit DAC for generating 2 * CVBS or S-Video(Y/C)
-. Support Internal Pattern (ColorBar/MultiBurst) Generator

MISC

-. Built in Clock PLL
-. Single 27M Crystal for 720H/960H all video standards
-. Built in 8-Ch Motion/Black/White Detector
-. Motion information at VBI region
-. Support Coaxial Protocols up to 5C-2V(Coaxial Cable) 200M.
-. Support Each Channel MPP Pin and IRQ Pin
-. Support 4 Video Output Clocks
-. Support I2C serial Interface
-. 1.2V / 1.8V / 3.3V Supply Voltage
-. 128 LQFP, 14X14, 0.4p

Application

-. Video Security System

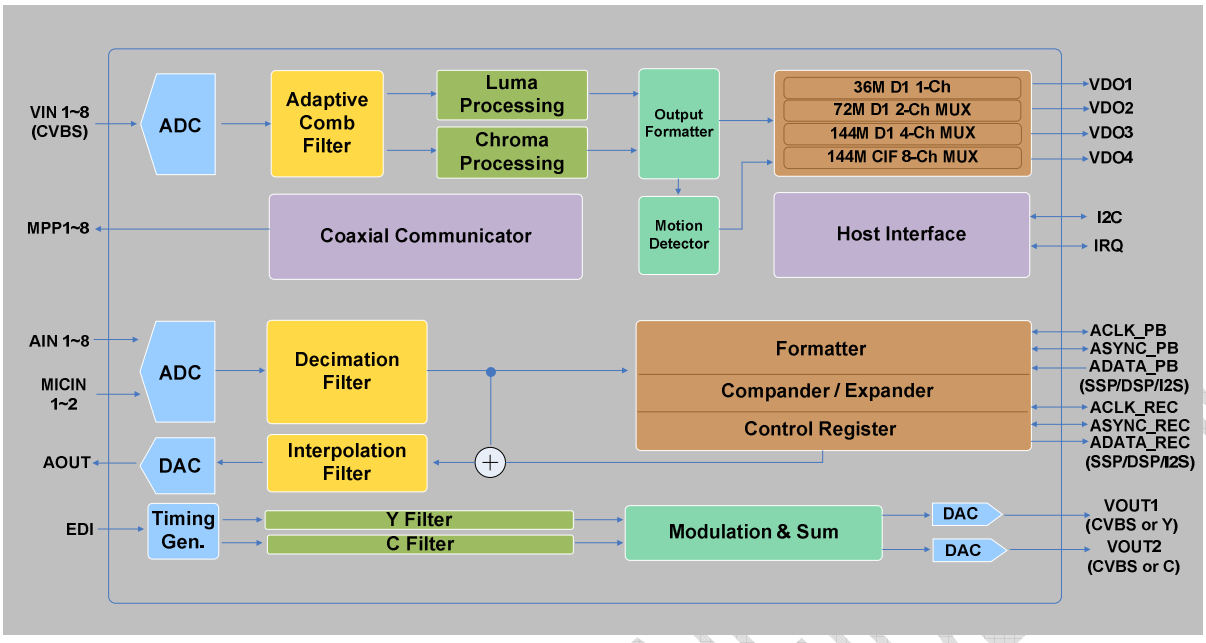
Ordering Information

Device	Package	Temperature Range
NVP1918	128LQFP	0 ~ 70℃

Related Products

-. NVC1600
-. NVC1700
-. NVS3260
-. HI3515/20/31

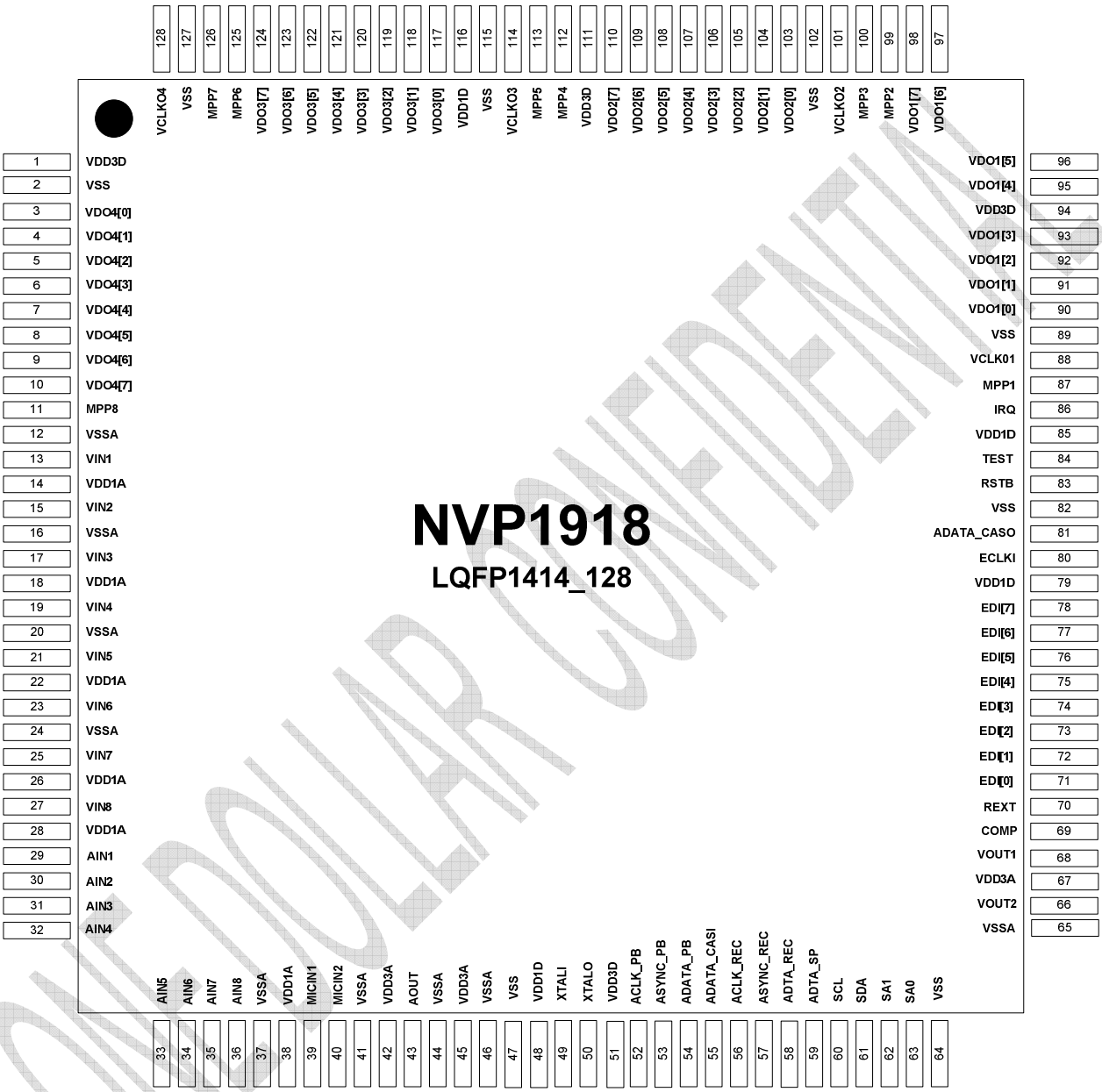
Functional Block Diagram



Contents

1. Pin Information

1.1 Pin Assignments



1.2 Pin Description

Name	Pin number	Type	Descriptions
System Clock / Reset			
RSTB	83	DI	System Reset (Active low)
XTALO	50	DO	Crystal Out
XTALI	49	DI	Crystal Input (27MHz)
Analog Video Input/output Interface			
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7, VIN8	13, 15, 17, 19, 21, 23, 25, 27	AI	Analog Video Input (1 ~ 8 Respectively)
VOUT1, VOUT2	68, 66	AO	Analog Video Output (1 ~ 2 Respectively)
COMP	69	A	Video DAC Compensation pin.
REXT	70	A	Video DAC external resistor pin
Analog Audio Input/output Interface			
AIN1, AIN2, AIN3, AIN4 AIN5, AIN6, AIN7, AIN8	29, 30, 31, 32 33, 34, 35, 36	AI	Analog Voice Input (1 ~ 8 Respectively)
MICIN1,MICIN2	39, 40	AI	Speaker Input (1 ~ 2 Respectively)
AOUT	43	AO	Analog Voice Output
Digital Video Interface			
VDO1[7:0]	98, 97, 96, 95, 93, 92, 91, 90	O	Video Port 1 Output
VDO2[7:0]	110, 109, 108, 107, 106, 105, 104, 103	O	Video Port 2 Output
VDO3[7:0]	124, 123, 122, 121 120, 119, 118, 117	O	Video Port 3 Output
VDO4[7:0]	10, 9, 8, 7, 6, 5, 4, 3	O	Video Port 4 Output
VCLK01, VCLK02, VCLK03, VCLK04	88, 101, 114, 128	O	Video Clock Output (1 ~ 4 Respectively)
ECLKI	80	I	Video Encoder Clock Input
EDI[7:0]	78, 77, 76, 75, 74, 73, 72 , 71	I	Video Encoder Digital Input
ETC			
TEST	84	I	Test Pin (Connect to Ground)
IRQ	86	O	Interrupt Request Output
MPP1,MPP2,MPP3,MPP4, MPP5,MPP6,MPP7,MPP8	87,99,100,112, 113,125,126,11	O	Multi-Purpose Pin Output

Name	Pin Number	Type	Descriptions
Digital Audio Interface			
ACLK_REC	56	B	Clock for Record (M:output, S:Input)
ASYNC_REC	57	B	Sync for Record(M:output, S:Input)
ADATA_REC	58	O	Audio Digital Data for Record
ADATA_SP	59	O	Audio Digital Data for Speaker
ADATA_CASO	81	O	Audio Digital Data for Cascade Output
ADATA_CASI	55	I	Audio Digital Data for Cascade Input
ACLK_PB	52	B	Clock for Playback (M:output, S:Input)
ASYNC_PB	53	B	Sync for Playback (M:output, S:Input)
ADATA_PB	54	I	Audio Digital Data for Playback
I2C Interface			
SDA	61	B	I2C Interface R/W Data (5V tolerant)
SCL	60	I	I2C Interface Clock (5V tolerant)
SA1, SA0	62, 63	I	Slave Address (5V tolerant)
Power/Ground			
VDD1D	48, 79, 85,116	P	Digital Power (Digital 1.2V)
VDD3D	1, 51, 94, 111,	P	Digital Power (Digital 3.3V)
VDD1A	14, 18, 22, 26 28, 38	P	Analog Power (Analog 1.8V)
VDD3A	42,45,67	P	Analog Power (Analog 3.3V)
VSS	2, 47, 64, 82, 89,102,115,127	G	Digital Ground
VSSA	12, 16, 20, 24, 37, 41, 44, 46, 65	G	Analog Ground

2. Video Decoder

NVP1918 is 8 Channel Video Decoder and delivers high quality images. It accepts separates 8 CVBS inputs from Camera, TV, or DVD and so on. It digitizes and decodes NTSC/PAL video formats into digital components video which represents 8-bit CCIR656 4:2:2 format with 36MHz, 72MHz and 144MHz multiplexed. 72/144MHz multiplexed function will be available, because It built in Clock PLL.

NVP1918 includes 8 channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. It shows the best picture quality adopted by high performance 2D adaptive comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness and Contrast and several function such as CTI, Programmable peaking filter, PAL compensation and IF compensation filter.

2.1. Functional Overview

The role of video decoder is to separate luminance and chrominance signals from composite video signal. Figure 2.1 show the block diagram of the **NVP1918**

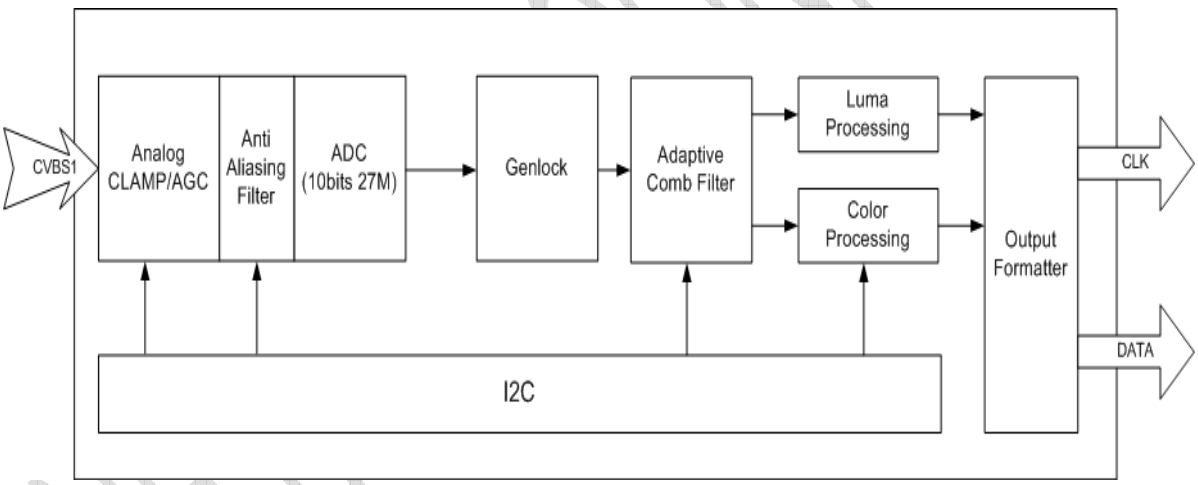


Figure 2.1. Video Decoder DATA FLOW of NVP1918

The First step to decode composite video signals is to digitize the entire composite video signal using an A/D converter (ADC). **NVP1918** uses the 10-bit ADC. Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic. The video signal also is low-pass filtered to about 9MHz in Anti aliasing Filter to remove any high-frequency components that may result in aliasing.

Vertical sync and horizontal sync information are recovered in Genlock block. When composite video signal is decoded, the luminance and chrominance are separated by Adaptive Comb Filter.

The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, 2D Adaptive Comb Filter is used.

The chrominance demodulator in color processing block accepts modulated chrominance data from Adaptive Comb Filter which generate Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sin and cos subcarrier data.

2.2. Video Input Formats

NVP1918 supports all NTSC/PAL Video Standard. Table 2.1 show NTSC/PAL Video Standards and Register Setting Value (VIDEO_FORMAT, 0x08~0B[4:0]/0x88~8B[4:0], Bank0) to support them.

Table 2.1. NVP1918 Input Video Image Formats

VIDEO_FORMAT	FORMAT	LINE	HZ	Fsc(MHz)
0x00	NTSC-M,J	525	60	3.579545
0x11	NTSC-4.43	525	60	4.43361875
0x1D	PAL-B,D,G,H,I	625	50	4.43361875
0x16	PAL-M	525	60	3.57561149
0x1F	PAL-Nc	625	50	3.58205625
0x15	PAL-60	525	60	4.433619
▪ Don't use auto-detect mode in case of NRT (Non Real Time) operation				

2.3. Analog Front End (CLAMP, PGA, Anti-aliasing Filter)

NVP1918 includes 8 channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. Because its design is dedicated for video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for **NVP1918** . Figure 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by Register (BAND_SEL, 0x01[0], Bank3)

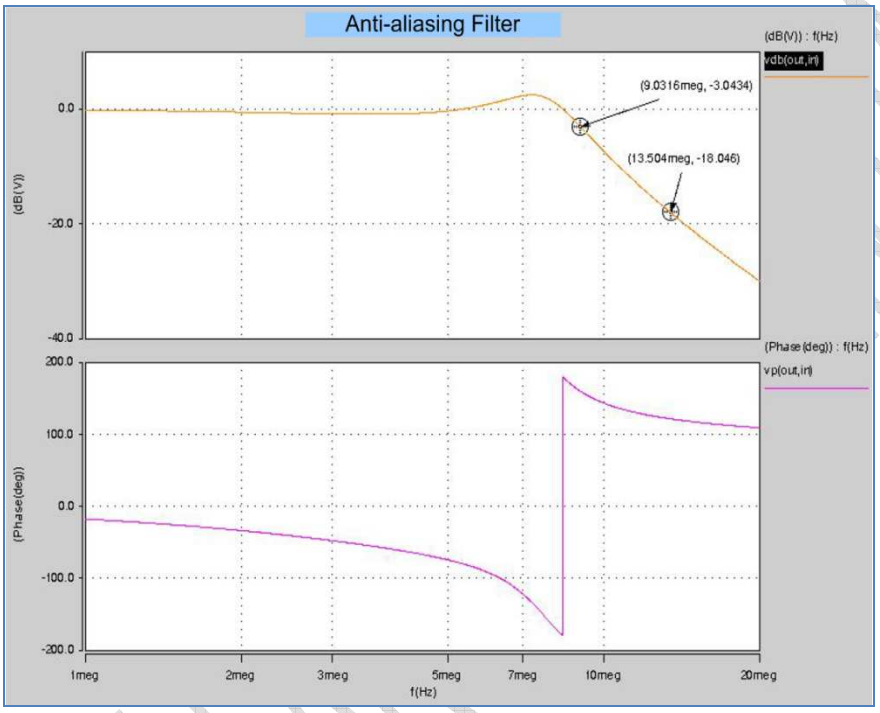


Figure 2.2. Anti-aliasing Filter characteristic

2.4. Genlock (Robust Sync Detection, Robust No-Video Detection)

NVP1918 provides a fully digital GenLocking circuitry. The digital Genlocking Circuitry use the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier.

NVP1918 uses the proprietary Genlock mechanism for video application system.
It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

2.5. Y/C separation (3H/5H Adaptive Comb Filter)

An adaptive comb filter is used to separate Y and C signal from NTSC/PAL standard video signal. Therefore, The output image is sharper and clearer compared to other video decoder. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows the Chroma BSF which is controlled by Register(BSF_MODE, 0x08~0B[6:5]/0x88~8B, Bank0).

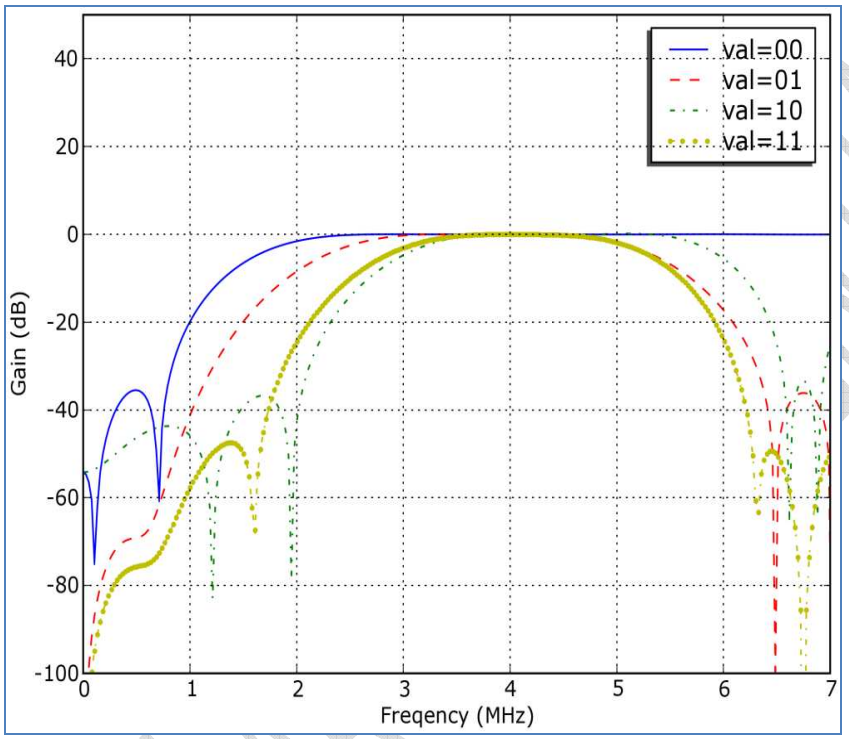


Figure 2.3. Band Split Filter Characteristic

NVP1918 can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the **NVP1918**, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.6. Luma Processing

The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

Figure 2.5. shows Peaking Filter Characteristic. **NVP1918** provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The Peaking filter is applied to this purpose and its characteristics can be controlled by register (Y_PEAK_MODE, 0x1A[1:0] / 0x1A[5:4] / 0x1B[1:0] / 0x1B[5:4] / 0x9A[1:0] / 0x9A[5:4] / 0x9B[1:0] / 0x9B[5:4], Bank0) via I2C interface.

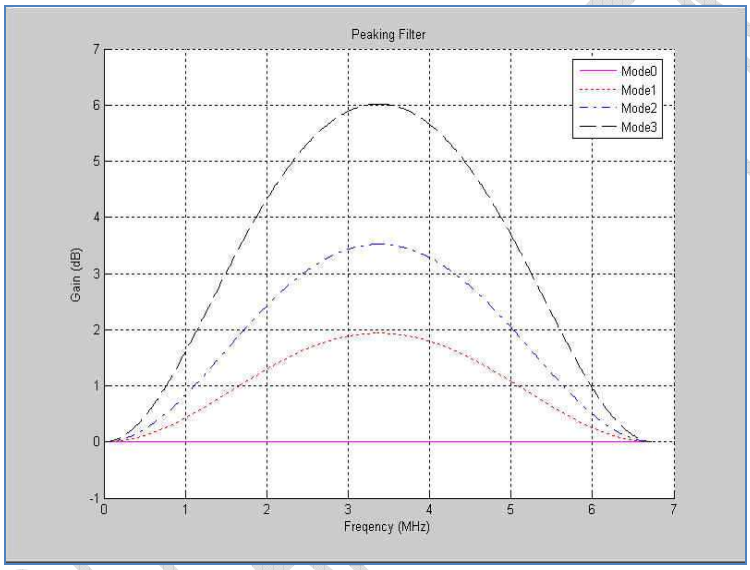


Figure 2.4. Peaking Filter Characteristic

2.7. Chroma Processing

Chroma processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The chroma demodulator receives modulated chroma from YC separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6.

Users can select the chroma filter through I2C interface (CLPF_SEL, 0x35/B5[1:0], Bank0).

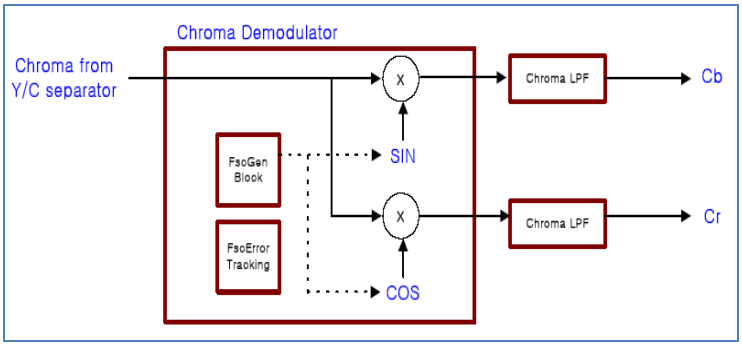


Figure 2.5. Chroma Process

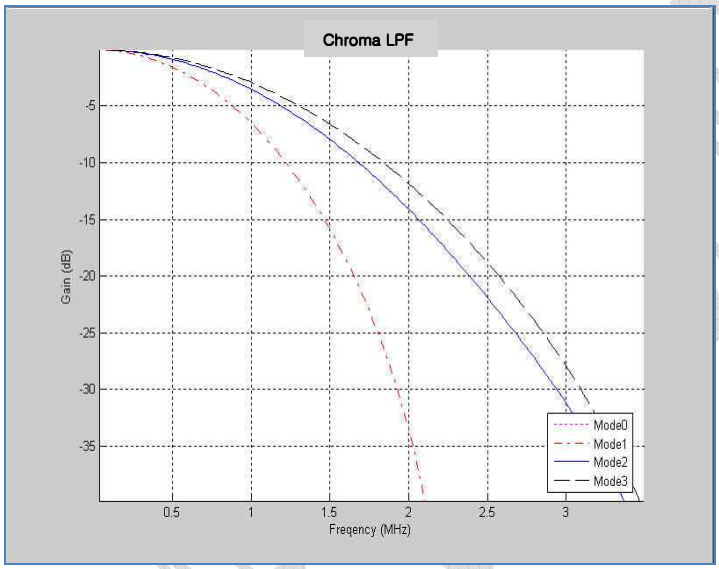


Figure 2.6. Chroma Low Pass filter Characteristic

2.8. Data Output Pin Order Control

NVP1918 can change the order of the output pin in the 36MHz/72MHz/144MHz Output Mode as shown in Table 2.2. (OUT_DATA_INV, 0xD0[3:0], Bank1)

Table 2.2. Data Output Pin Order Control

Address	*state*	Data Output of Port X
0xD0, OUT_DATA_INV [3]	0	VDO4 [7:0]
	1	VDO4 [0:7]
0xD0, OUT_DATA_INV [2]	0	VDO3 [7:0]
	1	VDO3 [0:7]
0xD0, OUT_DATA_INV [1]	0	VDO2 [7:0]
	1	VDO2 [0:7]
0xD0, OUT_DATA_INV [0]	0	VDO1 [7:0]
	1	VDO1 [0:7]

2.9. Output Format

NVP1918 supports a format of standard ITU-R BT.1302. Ports of 4 is synchronized by each output clock(VCLK_01~VCLK_04). Phase of clock is controlled by VCLK_SEL and VCLK_DLY_SEL of (BANK1, 0xCC~0xCF).

2.9.1. ITU-R BT.1302 Format

Codes of SAV and EAV are injected into data stream of ITU-R BT.1302 to indicate a start and a end of active. Note that a number of pixel for 1H Active line is always constant regardless of the actual incoming line length. Therefore, variance of analog input signal is applied to a blank section except codes of EAV and SAV. Figure 2.7 shows data stream of ITU-R BT.1302 format. If length of 1H of analog input signal increase or decrease, number of pixel of 'A' increase or decrease.

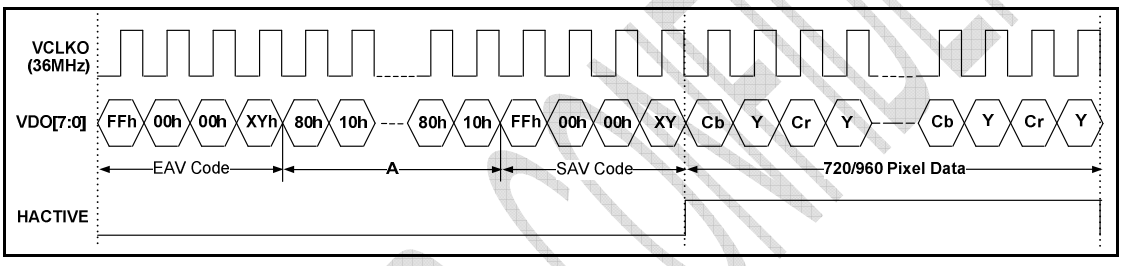


Figure 2.7. Region of active is constant

2.10. Output Mode

When it comes to the transfer of the output to the back-end device, **NVP1918** supports all the output of 36MHz/72MHz/144MHz Data Rate.

2.10.1 36MHz 720H/960H 1-CH D1 Data Output Mode

Operated in the 36MHz D1 Data Out Mode, NVP1918 outputs VCLK01, VCLK02, VCLK03, VCLK04 and VDO1[7:0], VDO2[7:0], VDO3[7:0], VDO4[7:0] in the timing as shown in Figure 2.8. For VCLK01, VCLK02, VCLK03 and VCLK04, phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC / CD / CE / CF[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC / CD / CE / CF[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4] / 0xC8[3:0] / 0xC9[7:4] / 0xC9[3:0], Bank1)

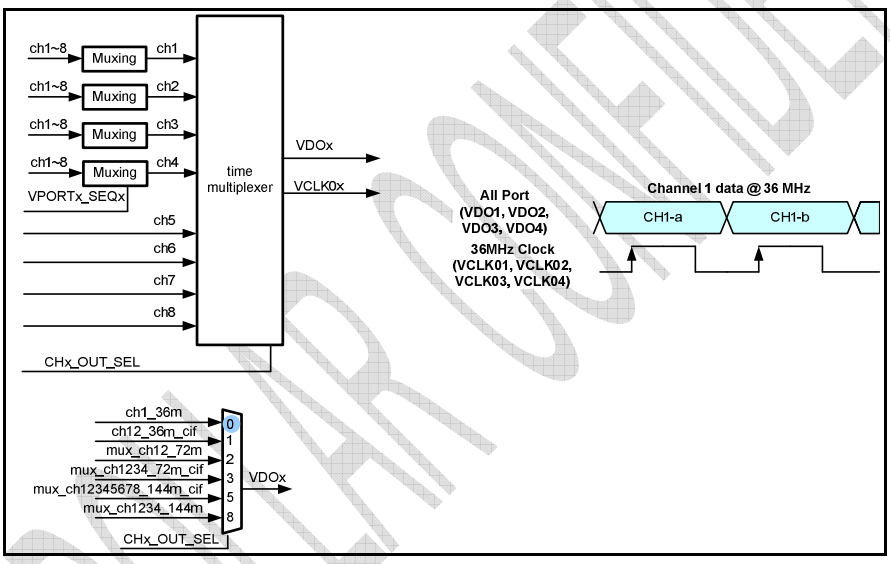


Figure 2.8. 36MHz D1 1Channel Data Output

2.10.2 72MHz 720H/960H 2-Ch D1 Data Output Mode

Operated in the 72MHz D1 Data Out Mode, **NVP1918** outputs VCLK01, VCLK02, VCLK03, VCLK04 and VDO1[7:0], VDO2[7:0], VDO3[7:0], VDO4[7:0] in the timing as shown in Figure 2.9. Two channel video data stream represents 8bit BT.1302 4:2:2 format with 72MHz multiplexed. For VCLK01, VCLK02, VCLK03 and VCLK04, phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC / CD / CE / CF[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC / CD / CE / CF[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4] / 0xC8[3:0] / 0xC9[7:4] / 0xC9[3:0], Bank1)

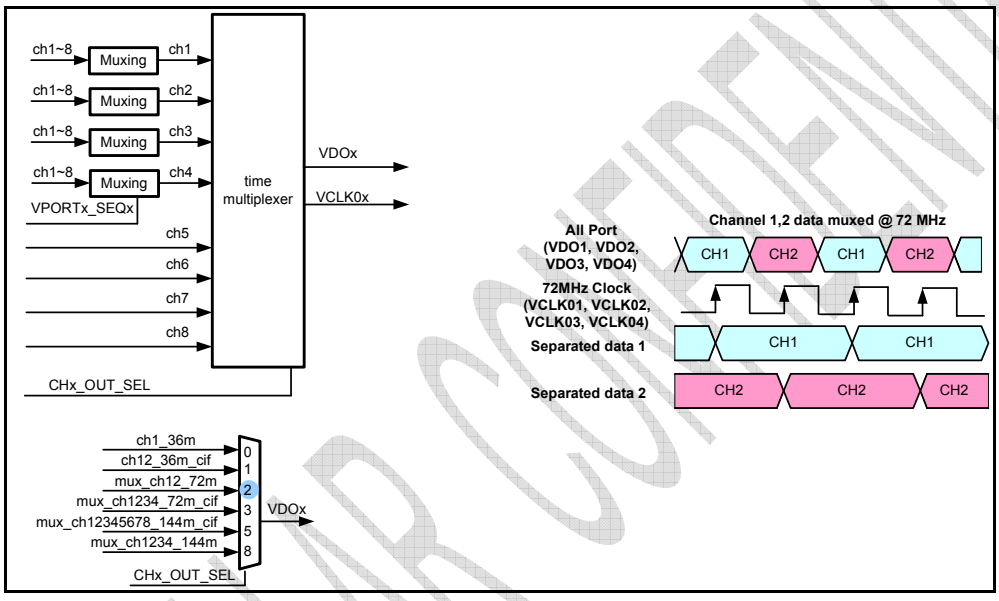


Figure 2.9. 72MHz D1 2Channel Data Output

2.10.3. 108MHz 720H/960H 4-Ch D1 Data Output Mode

Operated in the 144MHz D1 Data Out Mode, **NVP1918** outputs VCLK01, VCLK02, VCLK03, VCLK04 and VDO1[7:0], VDO2[7:0], VDO3[7:0], VDO4[7:0] in the timing as shown in Figure 2.10. Four channel Video data stream represents 8bit BT.1302 4:2:2 format with 144MHz multiplexed. For VCLK01, VCLK02, VCLK03 and VCLK04, phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC / CD / CE / CF[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC / CD / CE / CF[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4] / 0xC8[3:0] / 0xC9[7:4] / 0xC9[3:0], Bank1)

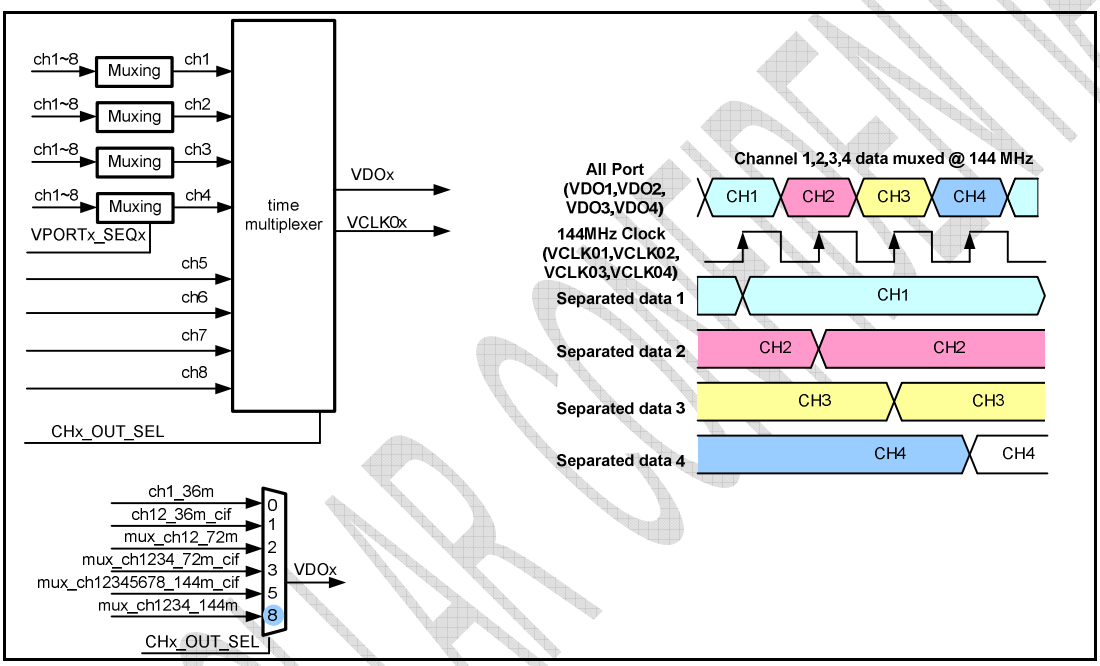


Figure 2.10. 144MHz D1 4Channel Data Output

- Example of 144MHz D1 Data Output Mode with Channel ID

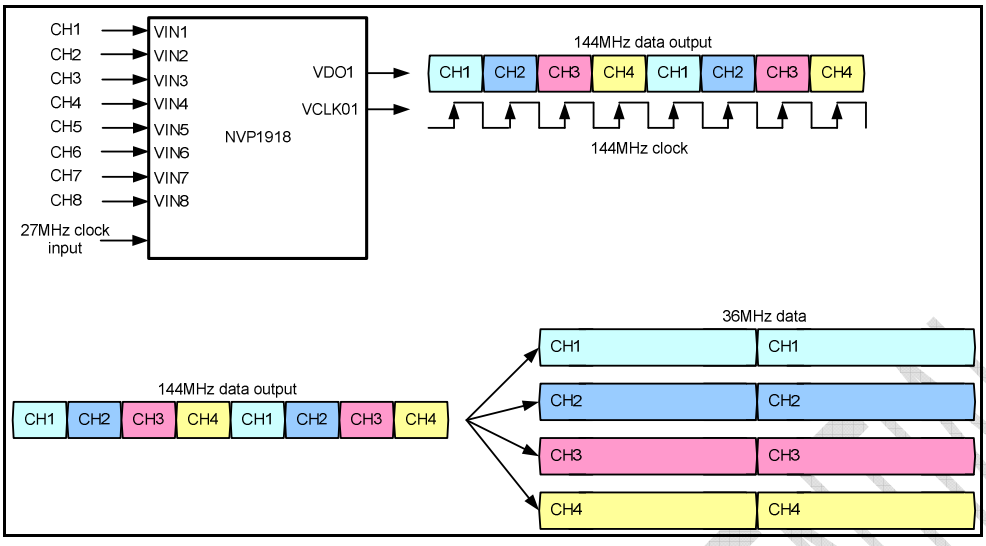
1. In case of VDO1 output port and VCLK01 output clock use.

2. Set VDO1 output(CH_OUT_SEL1,BANK1,0xC8[3:0] = 0x8) and VCLK01 output (VCLK01_SEL, BANK1,0xCC[6:4] = 0x6 or 0x7) .

3. Set Channel ID Type (Refer to CHID_TYPE(0x54/D4[2:0],BANK0) Register Description)

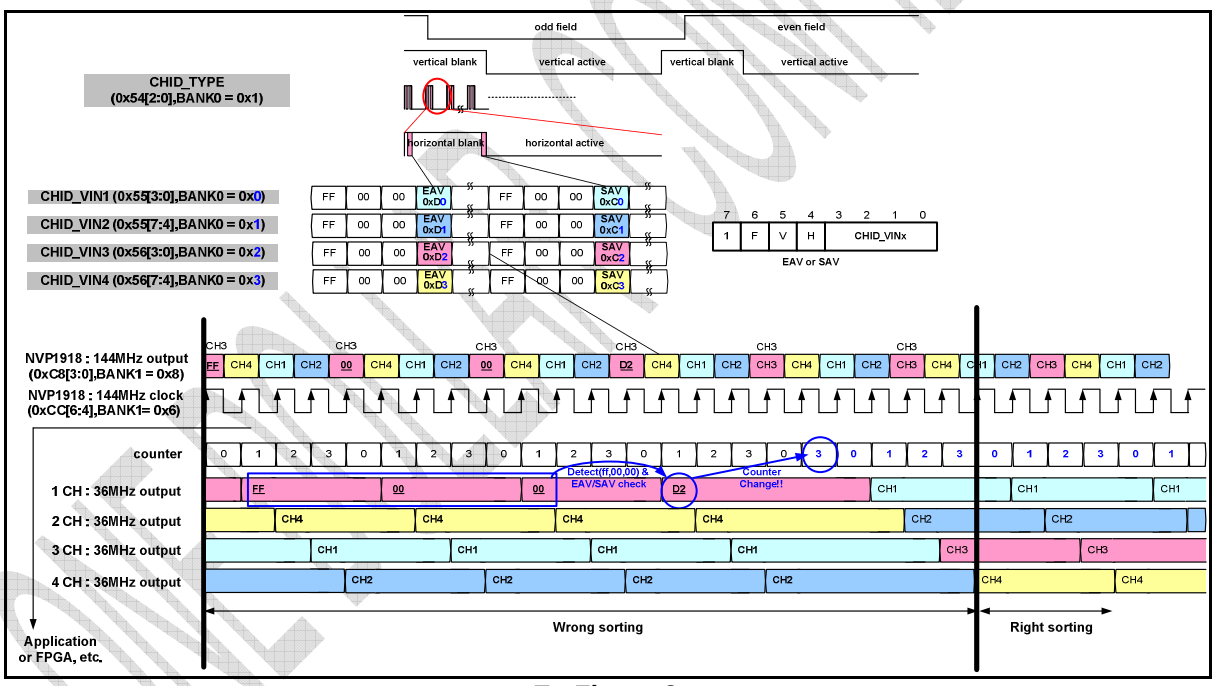
4. And then NVP1918 generate 144MHz clock and data output (Ex-Figure 1)

If you want to confirm the 144MHz Data using FPGA or Other device, Execute 5~11 item in next page.



Ex-figure 1

5. FPGA or equivalent devices which is input 144MHz time multiplexed data output, need to align with same channel data(36MHz 1,2,3,4 channel). EX-Figure 2 shows how to use Channel ID as a example.



Ex-Figure 2

6. CHID_TYPE(BANK0, 0x54[2:0]=001) mode described in top of Ex-Figure2

7. To generate 2bit digit, Design 2bit counter with VCLK01 (The 2bit digit means each channel).

8. Using 2bit digit, Convert from 144MHz Data to 36MHz Data (Wrong sorting part in Ex-Figure 2). and then Define the 2bit digit (**0** : 1ch data, **1** : 2ch data, **2** : 3ch data, **3** : 4ch data).
namely, 144MHz data output separate only with 36MHz, 4channel data, is not align with channel data where becomes mapping in counter value.

9. For mapping between separated each channel data and specified counter value, Select channel among separated each channel(1CH selected in Ex-Figure 2).
If selected channel data become Right sorting condition, other 3 channel is sorted automatically.

10. Check the 1ch data output when 2bit counter value is only '0' and then Search the EAV/SAV[3:0] after FF 00 00 Code.

11. If the EAV/SAV[3:0] is '2', make a counter reset to '3' (Refer to Blue color in Ex-Figure 2)

12. Become Right sorting part.

2.10.4. 36MHz 2-Ch CIF Data Output Mode

Operated in the 36MHz CIF Data Out Mode, **NVP1918** outputs VCLK01, VCLK02, VCLK03, VCLK04 and VDO1[7:0], VDO2[7:0], VDO3[7:0], VDO4[7:0] in the timing as shown in Figure 2.11. Two channel CIF data stream represents 8bit BT.1302 4:2:2 format with 36MHz multiplexed.

For VCLK01, VCLK02, VCLK03 and VCLK04, phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC/CD/CE/CF[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC/CD/CE/CF[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4]/0xC8[3:0]/0xC9[7:4]/0xC9[3:0], Bank1)

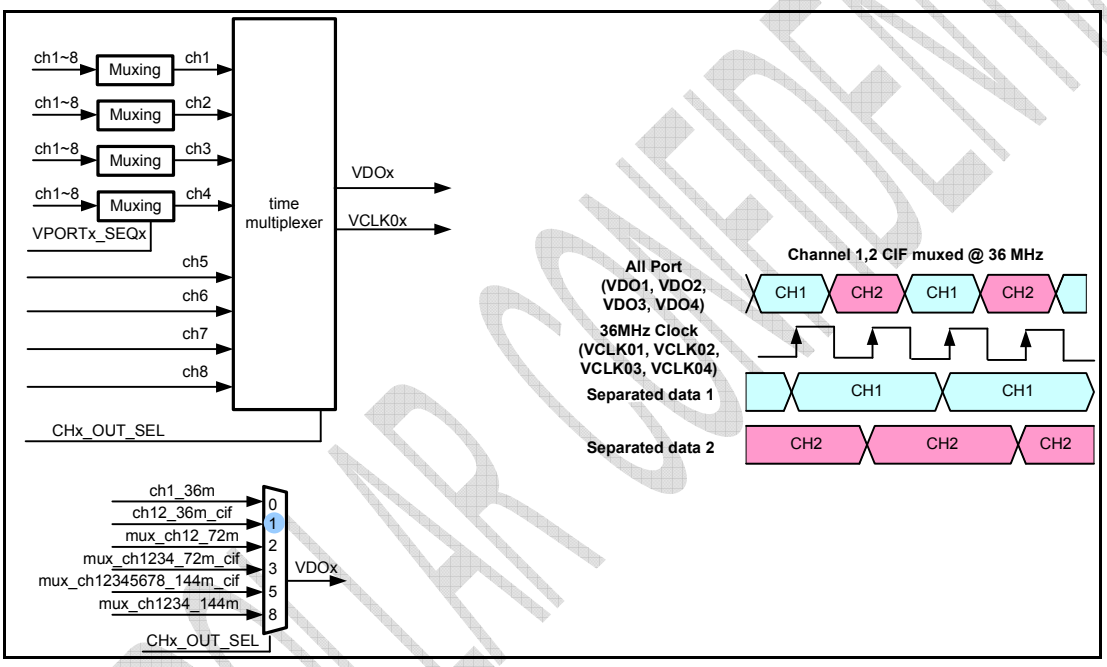


Figure 2.11. 36MHz CIF 2Channel Data Output

2.10.5. 72MHz 4-Ch CIF Data Output Mode

Operated in the 72MHz CIF Data Out Mode, **NVP1918** outputs VCLK01, VCLK02, VCLK03, VCLK04 and VDO1[7:0],VDO2[7:0],VDO3[7:0],VDO4[7:0] in the timing as shown in Figure 2.12. Four channel CIF data stream represents 8bit BT.1302 4:2:2 format with 72MHz multiplexed.

For VCLK01, VCLK02, VCLK03 and VCLK04, phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC/CD/CE/CF[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC/CD/CE/CF[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4]/0xC8[3:0]/0xC9[7:4]/0xC9[3:0], Bank1)

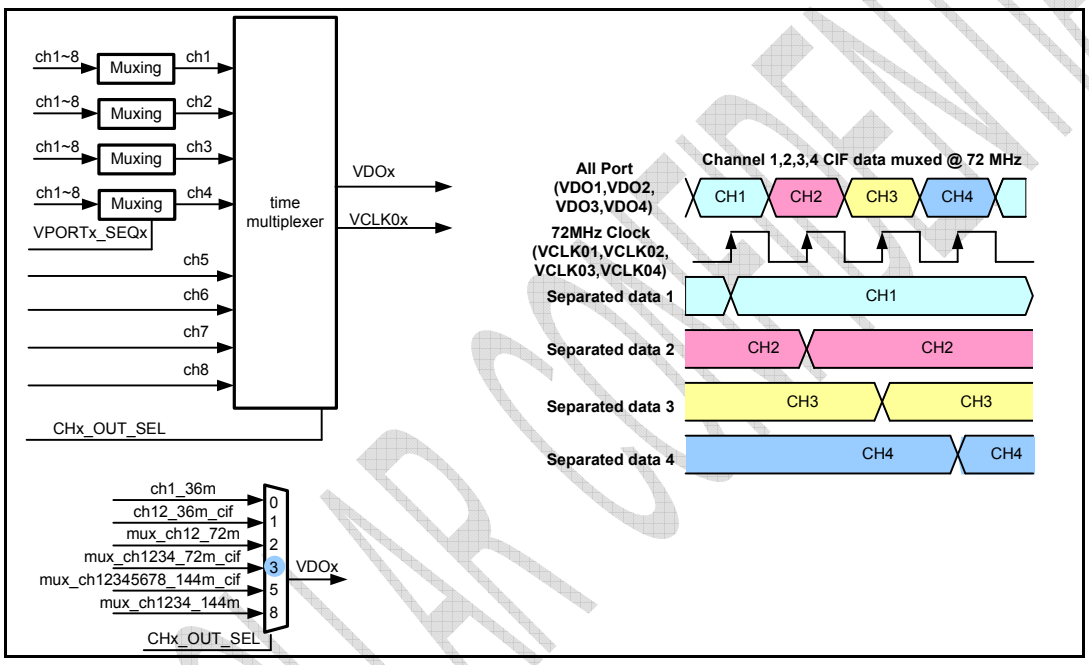


Figure 2.12 72MHz CIF 4Channel Data Output

2.10.6. 144MHz 8-Ch CIF Data Output Mode

Operated in the 144MHz CIF Data Out Mode, **NVP1918** outputs VCLK01, VCLK02, VCLK03, VCLK04 and VDO1[7:0], VDO2[7:0], VDO3[7:0], VDO4[7:0] in the timing as shown in Figure 2.13. Eight channel CIF data stream represents 8bit BT.1302 4:2:2 format with 144MHz multiplexed.

For VCLK01, VCLK02, VCLK03 and VCLK04, phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC/CD/CE/CF[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC/CD/CE/CF[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4]/0xC8[3:0]/0xC9[7:4]/0xC9[3:0], Bank1)

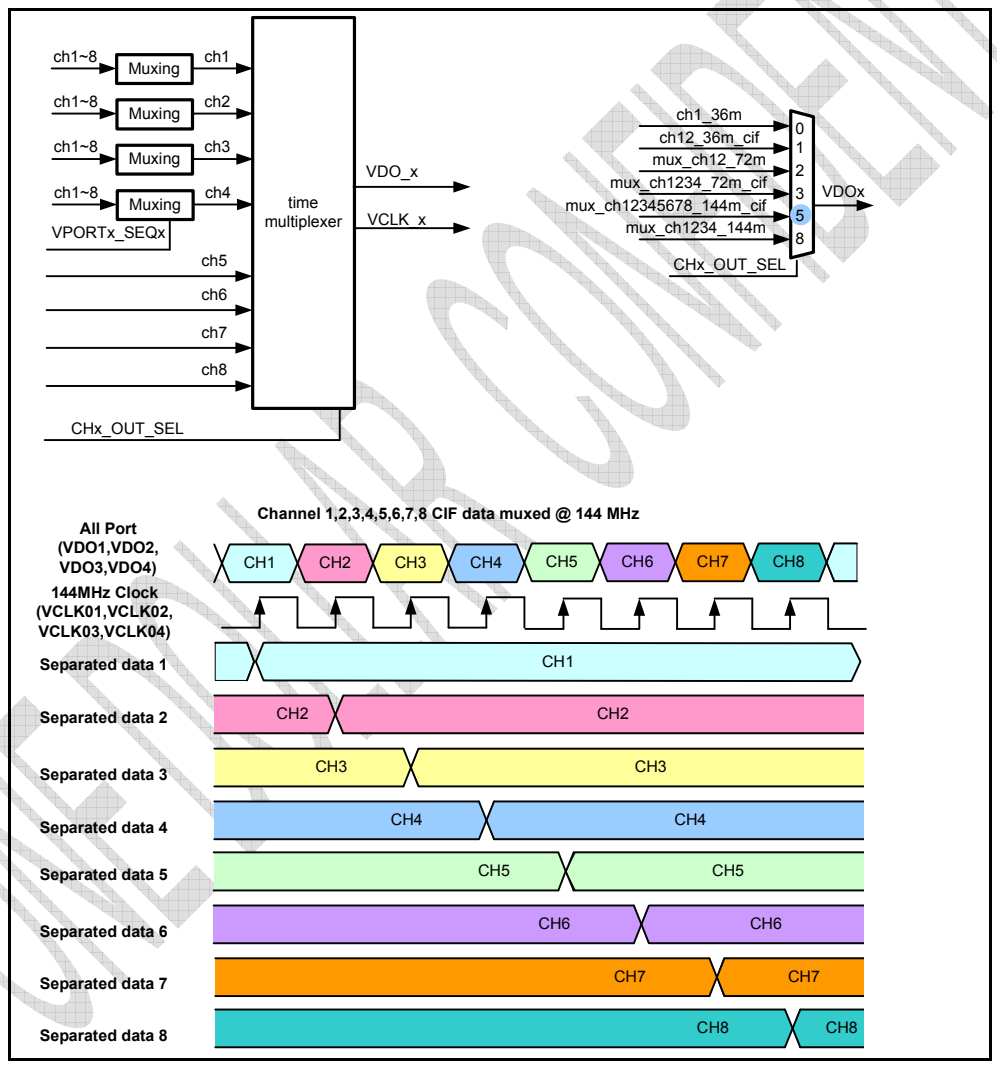


Figure 2.13. 144MHz CIF 8Channel Data Output

2.11. Motion Detector

NVP1918 supports 8 channel motion detection function. It supports the output of the detected motion information on the screen. The function allows a screen such as the one shown in Figure 2.14. to be divided in 192 sections each of which can generate information on the motion detection information.

For each section, motion detection can be controlled to be set at on/off. Once a motion is detected, the screen can be rendered dark or reversed in the unit of field to have the spot of the motion generated to be indicated in the screen.

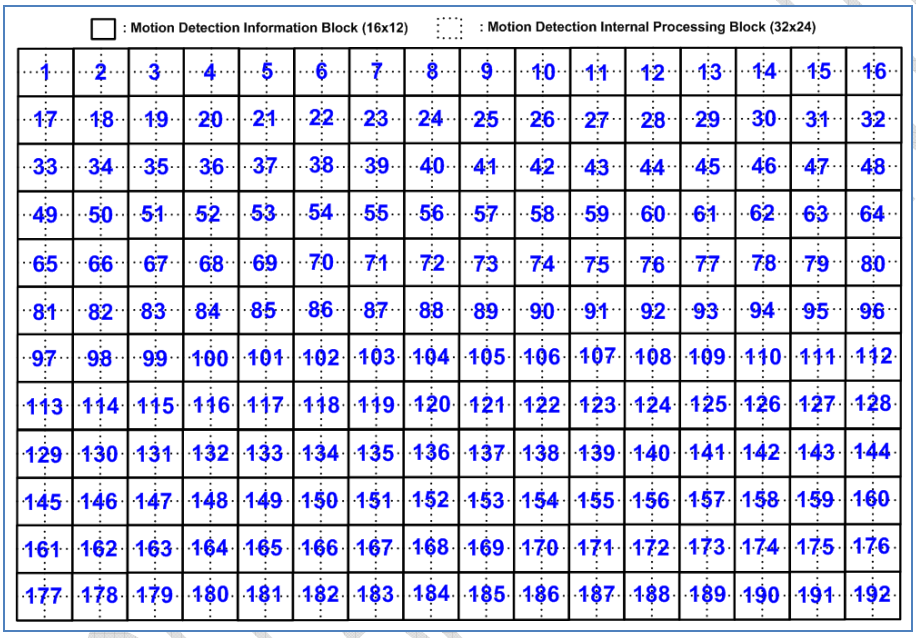


Figure 2.14. Motion Block Mapping

2.11.1. How to Operate the Motion Detection Function

1). Set the Motion detection On (Bank2, 0x00/02/04/06/08/0A/0C/0E[4]) - Set at low

2). Set the area for which to detect motion

: The screen is divided into 192 sections and each section is matched one to one.

- (BANK2, 0x20~0x37 - Channel 1, Bank3, 0x38~4F - Channel 2)
- (BANK2, 0x50~0x67 - Channel 3, Bank3, 0x68~7F - Channel 4)
- (BANK2, 0x80~0x97 - Channel 5, Bank3, 0x98~AF - Channel 6)
- (BANK2, 0xB0~0xC7 - Channel 7, Bank3, 0xC8~DF - Channel 8)

3). Set the motion sensitivity 1 (Pixel Sensitivity: Set at BANK2, 0x10/11)

4). Set the motion sensitivity 2 (Temporal Sensitivity : Set at BANK2 0x01/03/05/07/09/0B/0D/0F)

: When setting motion sensitivity, it is recommended to set the pixel sensitivity at “0x60” and use the temporal sensitivity to send the sensitivity to situation.

5). Output of Motion Detection

: Motion information generated from each section is not to be generated separately through data interface. In other words, the motion information needs to be confirmed in the register or It is not included in the BT.1302 data.

: Motion information generated from each area can be displayed on the screen.

Display can be done through three approaches. This can be controlled using MOTION_PIC (BANK2, 0x00/02/04/06/08/0A/0C/0E[1:0]).

3. Audio Codec

3.1. Description

NVP1918 outputs PCM digital audio signals converted from analog audio input signals and analog audio signals converted from PCM digital audio signals. **NVP1918** has 10 channel ADCs and 1 channel DAC for audio signals.

Voice data convert to G.711 PCM and Linear PCM data, and these converted data is outputted via DSP/SSP/I2S interfaces. The output data will be saved at hard disk or any other storages. This process - to convert and save audio data into storage - is usually called as "Record Output".

The saved audio data is inputted to **NVP1918** via DSP/SSP/I2S interfaces. The input audio data is outputted via audio DAC. This process is named as "Playback Output".

NVP1918 selects one audio input signal among ten analog audio inputs(8-Ch voice/2-Ch mic) and this audio is outputted through audio ADC and audio DAC. And it also supports directly mixed audio output signal which 10 analog audio inputs are mixed. This function usually is called by "Live Output".

In addition, **NVP1918** supports audio mute detection and cascade function up to 2 chips - 20 audio channels(16-Ch voice/4-Ch mic)

3.2. Record Output

Analog audio data is converted to PCM data and this data is outputted to the other **NVP1918** or other IC via DSP/SSP/I2S interfaces. Record output is useful function to save compressed audio data into storage. Analog audio signal is finally outputted to ADATA_REC pin used for data of each channel and ADATA_SP pin used for one mixed signal of each channel's data. The output data from ADATA_SP pin is either same data of ADATA_REC pin or mixed signal of each channel's data.

PCM data is categorized based on sampling frequency, sampling data bit width and PCM method. G.711 (A-law/Mu-law), unsigned linear PCM and linear PCM are supported. 8KHz / 16KHz and 8bit/16bit are used for sampling frequency and sampling data bit width, respectively. Refer the following table when you set the register value.

Table 3.1. Sampling & PCM coding setting

	BANK1											
	8K/8bit		8K/16bit		16K/8bit		16K/16bit		32K/8bit		32K/16bit	
	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE
Linear PCM	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 0 1 00	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 0 0 00	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 1 1 00	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 1 0 00	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	1 1 1 00	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	1 1 0 00
Unsigned Linear PCM	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 0 1 01	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 0 0 01	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 1 1 01	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	0 1 0 01	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	1 1 1 01	0x00[0] 0x07[3] 0x07[2] 0x09[7:6]	1 1 0 01
G.711 U-law	0x00[0] 0x07[3] 0x07[2] 0x09[7:6] 0x09[3]	0 0 1 10 0	0x00[0] 0x07[3] 0x07[2] 0x09[7: 0x09[3]	0 0 0 10 0	0x00[0] 0x07[3] 0x07[2] 0x09[7:6] 0x09[3]	0 1 1 10 0	0x00[0] 0x07[3] 0x07[2] 0x09[7:6] 0x09[3]	0 1 0 10 0	0x00[0] 0x07[3] 0x07[2] 0x09[7:6] 0x09[3]	1 1 1 10 0	0x00[0] 0x07[3] 0x07[2] 0x09[7:6] 0x09[3]	1 1 0 10 0
G.711 A-law	0x00[0] 0x37[3] 0x37[2] 0x39[7:6] 0x39[3]	0 0 1 10 1	0x00[0] 0x37[3] 0x37[2] 0x39[7:6] 0x39[3]	0 0 0 10 1	0x00[0] 0x37[3] 0x37[2] 0x39[7:6] 0x39[3]	0 1 1 10 1	0x00[0] 0x37[3] 0x37[2] 0x39[7:6] 0x39[3]	0 1 0 10 1	0x00[0] 0x37[3] 0x37[2] 0x39[7:6] 0x39[3]	1 1 1 10 1	0x00[0] 0x37[3] 0x37[2] 0x39[7:6] 0x39[3]	1 1 0 10 1

DSP / SSP / I2S interfaces are supported as output data format. In addition, slave mode and master mode are also supported. At slave mode, input clock and synchronized signal come from external ICs, however Master mode generates clock and synchronized signal in itself.

3.2.1 Data Output Interface

NVP1918 outputs "Record Output" using ACLK_REC, ASYNC_REC, ADATA_REC and ADATA_SP. ACLK_REC is a reference clock signal for Record Output Data and ASYNC_REC is a reference synchronization signal for Record Output Data. ADATA_REC and ADATA_SP are synchronized Record Output, data with reference clock and reference synchronized signal.

Table 3.2 Record Output Interface configuration

	BANK1					
	DSP		SSP		I2S	
	ADDR	*VALUE*	*ADDR*	*VALUE*	*ADDR*	*VALUE*
Master	0x07[0] 0x07[1] 0x07[7]	1 0 1	0x07[0] 0x07[1] 0x07[7]	1 1 1	0x07[0] 0x07[1] 0x07[7]	0 0 1
Slave	0x07[0] 0x07[1] 0x07[7]	1 0 0	0x07[0] 0x07[1] 0x07[7]	1 1 0	0x07[0] 0x07[1] 0x07[7]	0 0 0

ACLK_REC is a reference clock of Record Output Data and ASYNC_REC is reference synchronized signal. ACLK_REC and ASYNC_REC signal support slave mode accepted

external signals and master mode generating clock and synchronization signal in itself. And DSP/SSP/I2S interfaces are supported by configuration of these pins defined by internal register setting value.

Figure 3.1, 3.2, 3.3 shows timing diagram of I2S, DSP, and SSP mode, respectively.

These figures show timing relation among ASYNC_REC, ACLK_REC and ADTA_REC, and ADATA_SP is outputted using same interface method of ADATA_REC. Polarity of ACLK_REC clock is changed by setting of internal register value [0x37[6], RM_CLK].

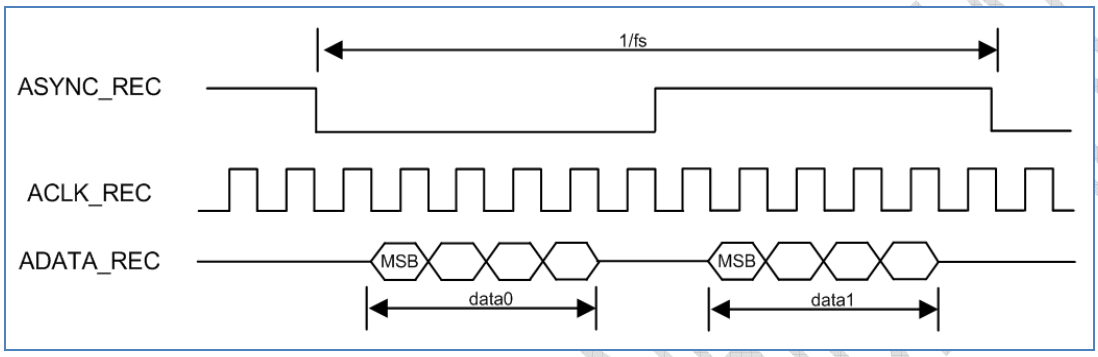


figure 3.1 I2S mode

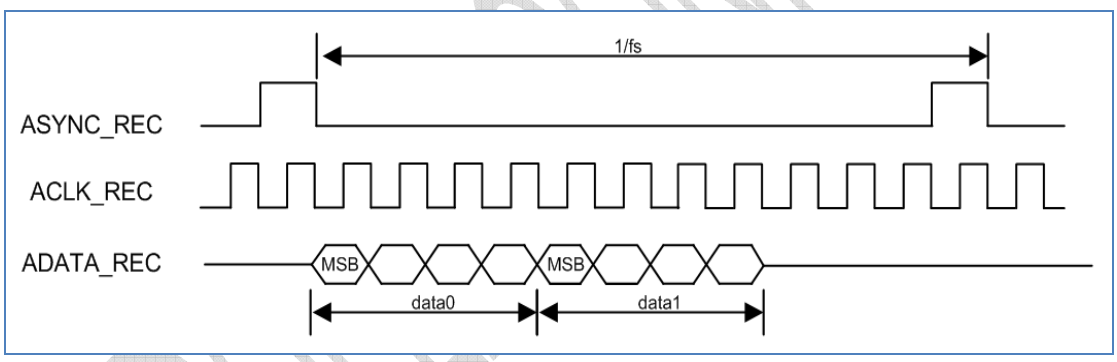


figure 3.2 DSP mode

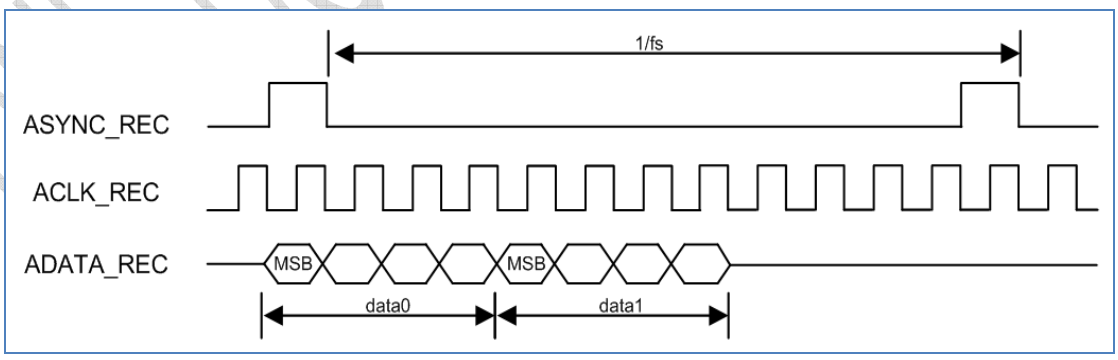


figure 3.3 SSP mode

3.2.2. 2/4/8/16-Channel Data Output(256 fs)

ADATA_REC supports up to 8 channel audio(8-Ch voice) using single chip and up to 16 channel(16-Ch voice) in cascade mode. In this case, the bitrate of the audio signal should be 256 fs([0x37[5:4], RM_BITRATE). The number of output channel is configured by internal register value [0x38[1:0], R_MULTCH] and the order of output channel is configured by internal register value [0x3A ~ 0x41, R_SEQ]. Therefore, the order of audio output can be changed.

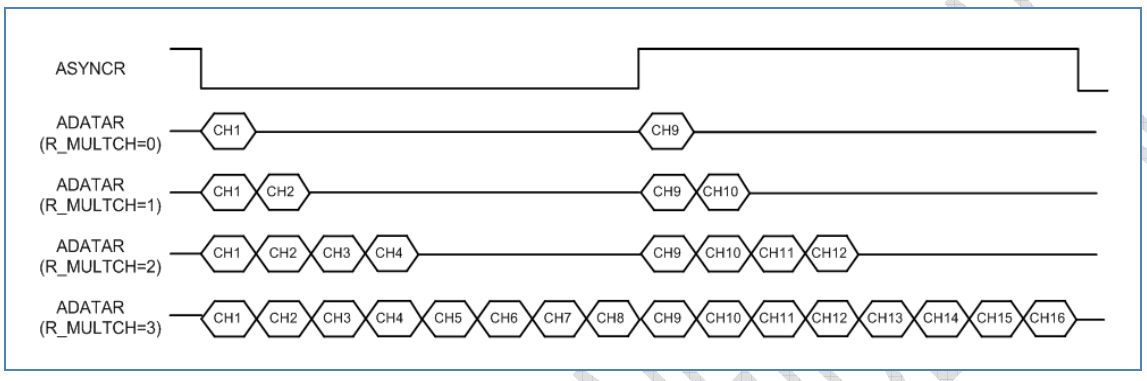


figure 3.4. audio 2/4/8/16 channel data output <I2S mode, 256fs>

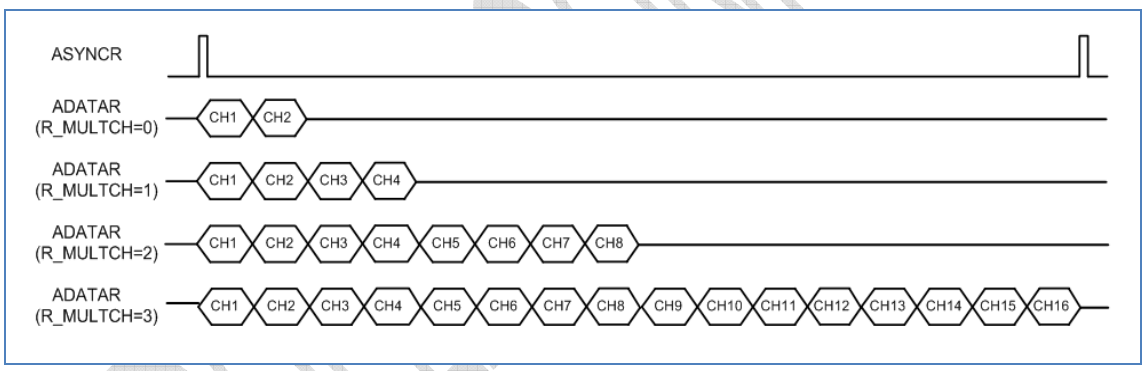


figure 3.5. audio 2/4/8/16channel data output <DSP/SSP mode, 256fs>

3.2.3. 2/4/8/16-Channel Voice Data Output with 4-Channel Mic Data(320 fs)

ADATA_REC supports up to 10 channel audio(8-Ch voice/2-Ch mic) using single chip and up to 20 channel(16-Ch voice/4-Ch mic) in cascade mode. In this case, the bitrate of the audio signal should be 320 fs([0x37[5:4], RM_BITRATE). The number of output channel is configured by internal register value [0x38[1:0], R_MULTCH] and the order of output channel is configured by internal register value [0x3A ~ 0x41, R_SEQ / 0x42, MIC_SEQ]. Therefore, the order of audio output can be changed.

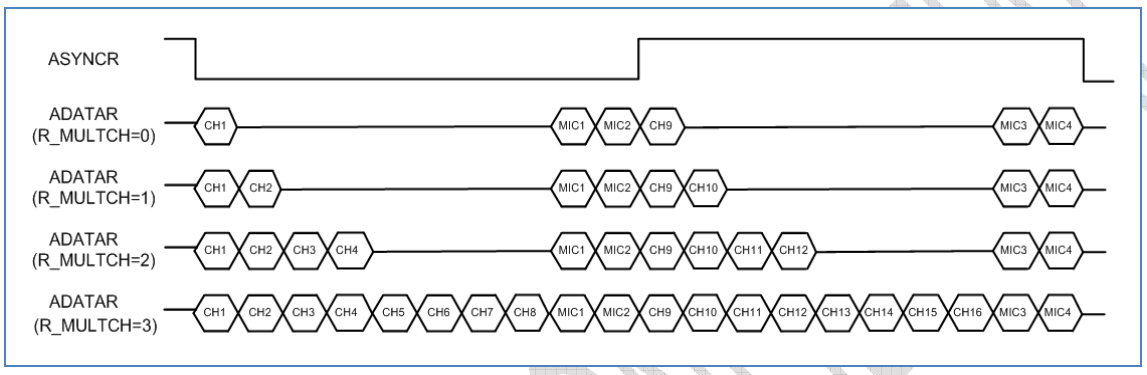


figure 3.6 audio 2/4/6/8/16 channel data output(with 4 channel mic) <I2S mode, 320fs>

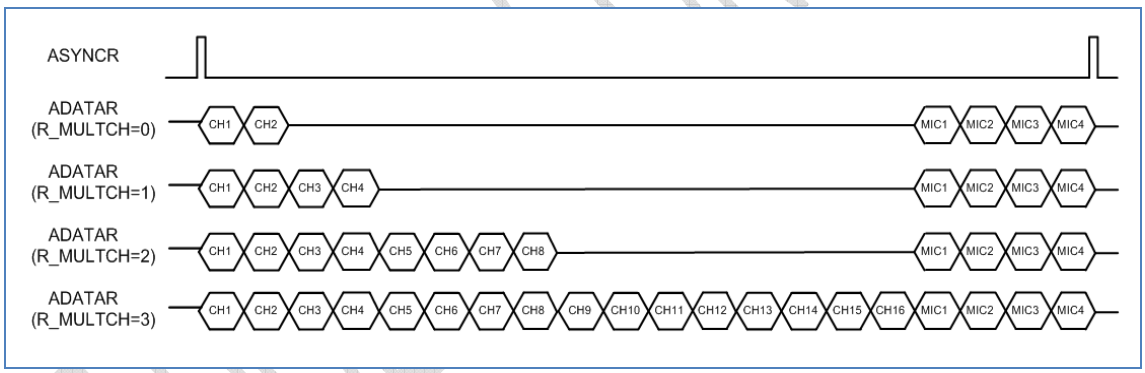


figure 3.7. audio 2/4/8/16 channel data output(with 4 channel mic) <DSP/SSP mode, 320fs>

3.2.4. ADATA_SP Output

ADATA_SP supports 3 kinds of output method. Firstly, the output data of ADATA_SP pin is the exactly same as those of ADATA_REC except output data sequence. The order of output data is opposite. If the output data order of ADATA_REC is "CH1, CH2, CH9, CH10", the output data order of ADATA_SP is "CH16, CH15, CH8, CH7". That is to say, two output pin - ADATA_SP and ADATA_REC are complement relationship. Secondly, one of input signals is selected as output signal of ADATA_SP. The selectable input signal ranges from analog input signal to ADATA_PB signal. Lastly, mixed data of input signal is selected as the output signal of ADATA_SP. The mixing gain of each channel's input signal is determined by internal register setting value[0x46 ~ 0x51, MIX_RATIO].

The output configuration of ADATA_SP is determined by internal register setting. First and second configuration are determined by [0x38[2],R_ADATSP], and second and third configuration are determined by [0x54[4:0],L_CH_OUTSEL] and [0x55[4:0],R_CH_OUTSEL]. In this case, L_CH_OUTSEL and R_CH_OUTSEL select one of input channels or mixed data.

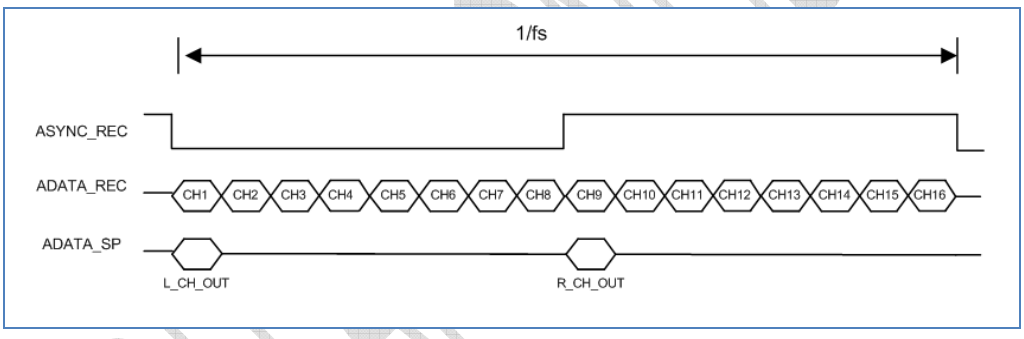


figure 3.8 ADATA_SP Output <I2S mode>

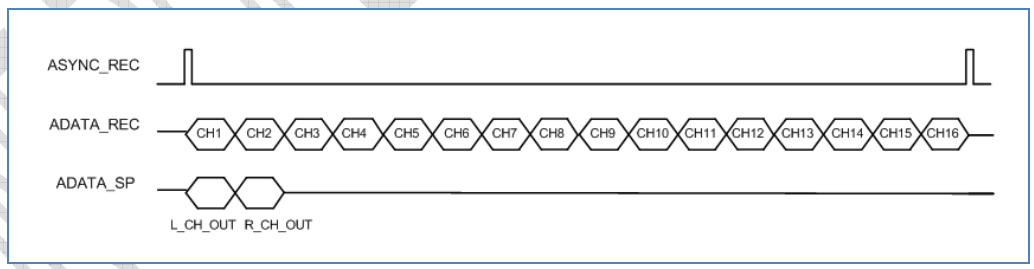


figure 3.9 ADATA_SP Output <DSP/SSP mode>

3.3. Playback Output

Playback is to output stored audio data to external device through DAC after internal processing.

NVP1918 gives and takes a clock and synchronization signal through ACLK_PB and ASYNC_PB pin. In this case, interface is the exactly same as Record data's interface. When multi-channel audio is supported, selective playback for intended channel is enable using register setting [0x44[4:0], PB_SEL]. In case of single channel, PB_SEL should be set to "00000".

ACLK_PB and ASYNC_PB supports Master mode and Slave mode. In master mode, ACLK_PB and ASYNC_PB are outputted by **NVP1918** , and clock and synchronization signal come from external devices at slave mode. Master/Slave mode is selected by setting internal register [0x43[7], PB_MASTER].

ADATA_PB accepts an audio data synchronized with ACLK_PB and ASYNC_PB. ACLK_PB and ASYNCP accept I2S/DSP/SSP mode input and output, and I2S and DSP mode is set by internal register value [0x43[0], PB_SYNC]. When DSP mode is selected, DSP/SSP mode is set by [0x43[1], PB_SSP]. The relation of clock, synchronized signal and data are the exactly same as that of record/mix output. PB_CLK can be inverted for all modes using setting of register [0x43[6], PB_CLK].

3.4. Audio Detection

NVP1918 has an audio mute detection block for individual 10 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the ADET_MODE and ADET_FILT (0x59) register, and the detecting threshold values are defined by ADET_TH register (0x5C ~ 0x60). According to this control bits and its result (audio detected), Interrupt is generated through the interrupt pins.

3.5. Cascade Operation

NVP1918 supports cascade mode. Maximum 2 **NVP1918** chips can be connected together for cascade mode and can be processed 20 channel audio encoding data(16-Ch voice/4-Ch mic). Cascade is enabled by setting register [0x36[1:0], CHIP_STAGE]. Figure 3.10 shows how to connect **NVP1918** for the cascade mode. In this case, analog audio AOUT1 is assigned to AIN1-16 and MICIN1-4. 1 channel audio or all channel mixed audio signal is selected as output signal set by MIX_OUTSEL.

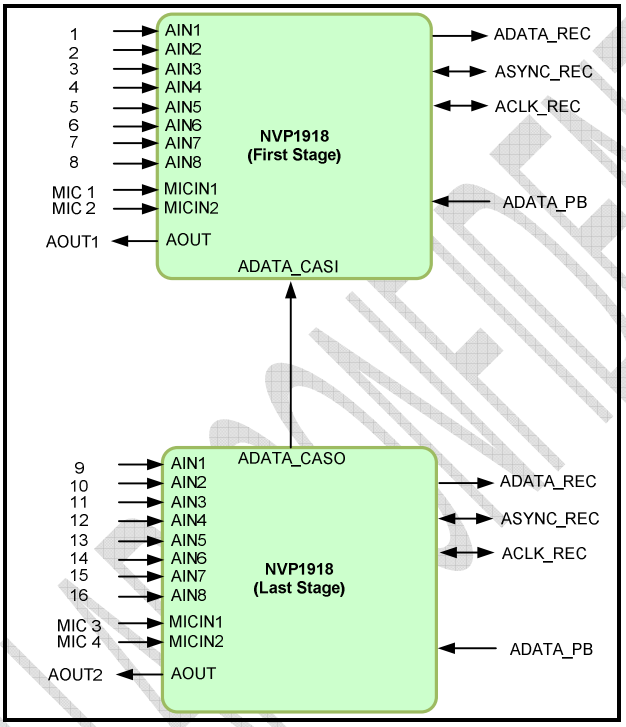


figure 3. 10. NVP1918 & NVP1918 Cascade mode

4. Video Encoder

4.1. Video Encoder Function Description

NVP1918 has an independent 720H/960H video encoder that generates standard NTSC and PAL 720H/960H video signals. Video encoder receives digital video signal and generates analog video signal. The video encoder consists of Sync Separator, Pre-processing, Y/C low-pass filter, Modulation Part, Output Mux, and DAC (Digital-to-Analog Converter). DAC has a two-channel output and a 10-bit resolution.

The video encoder works on 27/36 MHz and generates analog video signals after receiving 8-bit BT.656(720H)/BT.1302(960H) data. The video signal generated at each channel is one of the following: CVBS, S-video(Y or C). A video encoder has an internal Pattern Generator for test purpose. Figure 4.1 shows a block diagram of a video encoder installed in **NVP1918**.

Video Encoder Feature

-. Support 720H/960H NTSC/PAL and sub-standard format
-. Accepts BT.656/BT.1302 compatible 8bit video Input
-. 27/36MHz Clock for Sub-carrier generation.
-. Includes 2*10Bit DAC(Digital-to-Analog Converter) for generating 2*CVBS or Y/C.
-. Includes ColorBar/MultiBurst test pattern generator

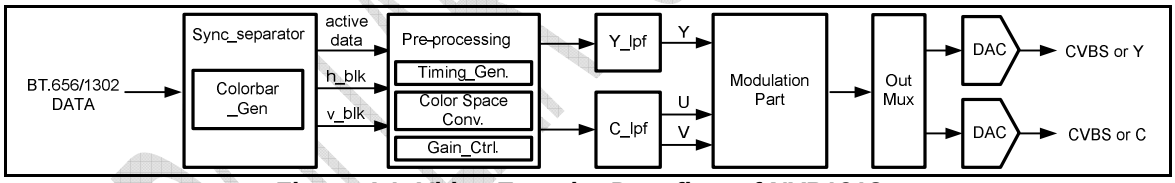


Figure 4.1. Video Encoder Data flow of NVP1918

4.2. Video Encoder Function Description

Sync Separator extracts active data, horizontal blank and vertical blank from BT.656/1302 data. The information on the active data, horizontal blank, and vertical blank is present in EAV and SAV of BT.656/1302. In other words, they perform the job of separating video and timing signals that are included in digital video standard signals.

4.3. Pre-Processing

Pre-processing block has three functions. First, it creates timing signals (Timing Generator). Second, it converts Y, Cb, Cr into Y, U, V (Color Space Conversion). Third, it controls the scale (Gain Control). The timing generator generates the Sync signal out of the Horizontal and Vertical Blank as well as various timing signals. As for Table 4.1, the following formulas are used to convert Y, Cb, Cr into Y, U, V.

Table 4.1. Color Space Conversion (YCbCr to YUV)

Standards	Y	U	V
NTSC	0.591 (Y601 - 64)	0.504 (Cb - 512)	0.711 (Cr - 512)
PAL	0.625 (Y601 - 64)	0.533 (Cb - 512)	0.752 (Cr - 512)

As for the gain control, Sync, Burst, Luma and Chroma can be adjusted in the scale from 0 to about 2. The increment in scale is 1/127. Figure 4.2 shows adjustments for each control.

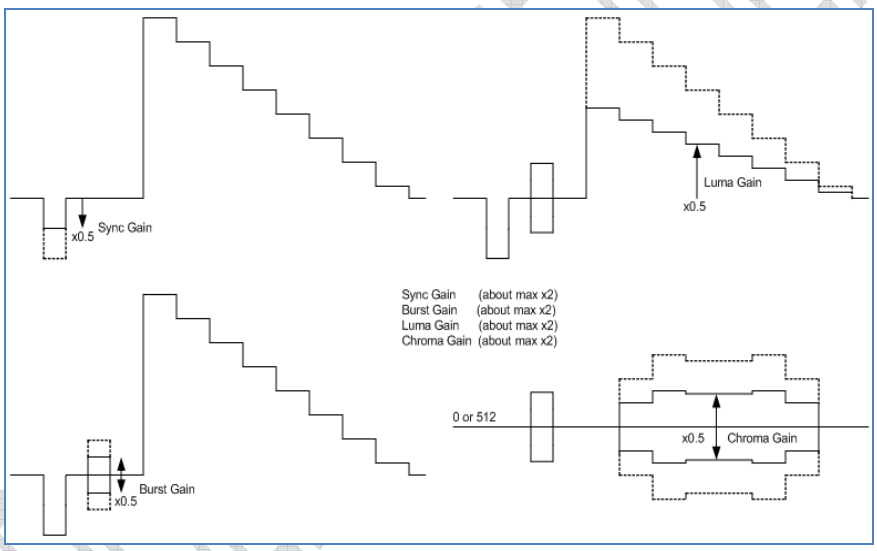


Figure 4.2. Gain Control for Burst, Sync, Luma, Chroma

4.4. Y/C low pass filter

Y Low-pass filtering is done in order to remove high frequency components that happen when Y is over-sampled. To eliminate aliases that may occur after modulation, C Low-pass filters are used according to frequency bandwidths of U and V.

4.5. Modulation Part

The modulation block generates chroma signal through AM modulation. AM modulation is applied to NTSC and PAL. Figure 4.3 shows chroma formed by way of AM modulation for NTSC and PAL .

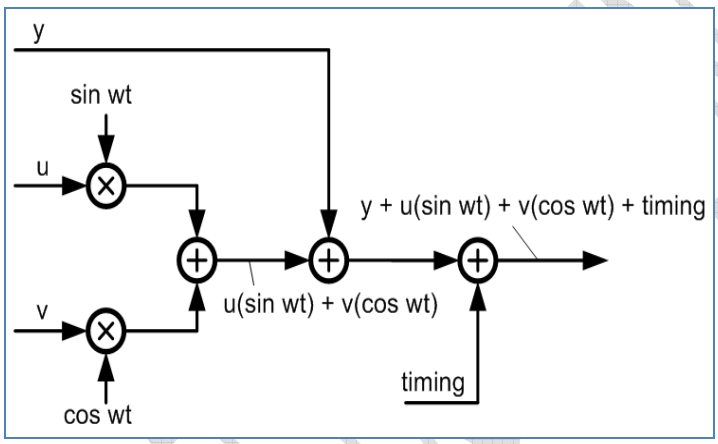


Figure 4.3. AM Modulation for NTSC and PAL

4.6. Output Muxing

Video Encoder has two channels for output. Each channel generates only one output out of three signals (CVBS, Y, C).

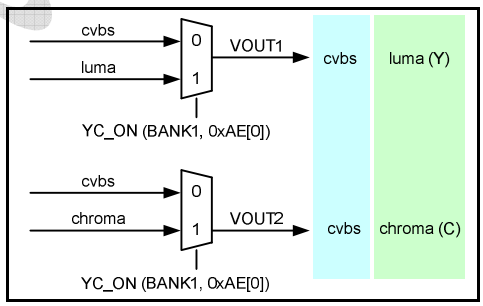


Figure 4.4. Output Muxing

5. Coaxial Protocol

NVP1918 includes Coaxial Protocol generator that sends control signal from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal. **NVP1918** supports Pelco Protocol up to 5C-2V(coaxial cable) 200M. It depends on Coaxial Cable impedance characteristic. This document presents the concept of Coaxial Protocol. Coaxitron is Pelco's name for a method of sending control signaling from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal (Known as "Up The Coax" or "UTC").

There are two types of Coaxitron command structures. One type, Standard Coaxitron,. is a series of 15 pulses, or data bits, that are sent within video line 18 of a video field. The other type, Extended Coaxitron, is a series of 32 pulses, where 16 pulses are sent in line 18 and 16 pulses in line 19 of a video field. Refer to Figure 5.1. No pulses are sent when the system is in an idle state

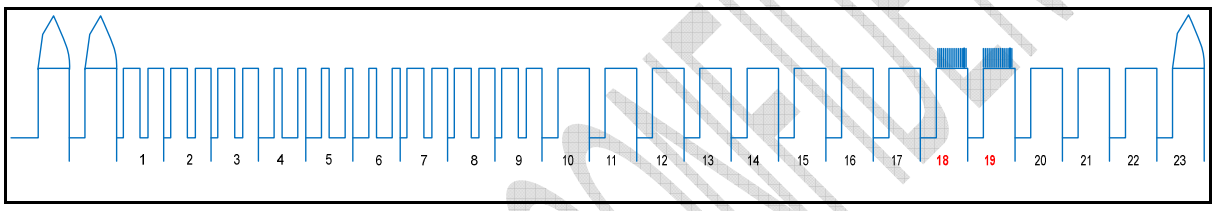


Figure 5.1. Coaxitron Active line

Coaxitron is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 2us pulse represents a one(1) and a 1us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 5.2. and Figure 5.3.

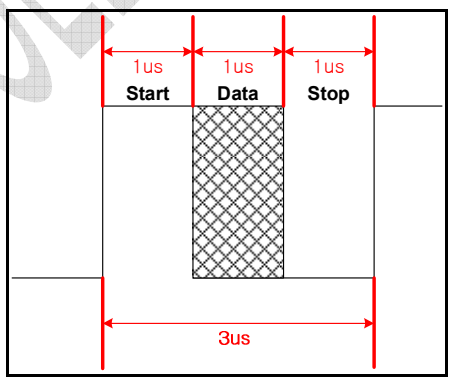


Figure 5.2. Description of One Coaxitron Bit

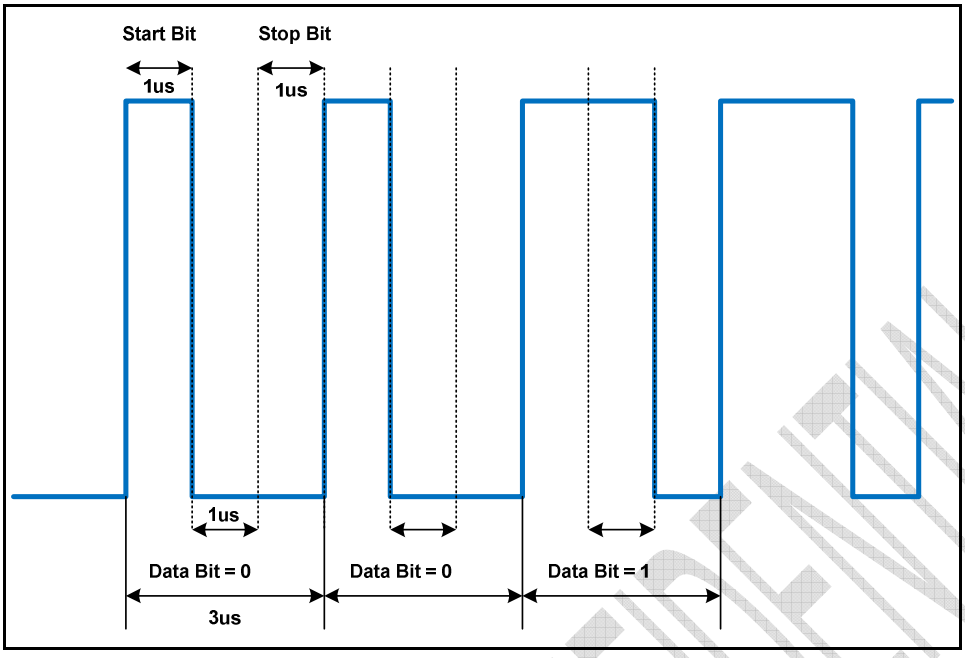


Figure 5.3. Coaxitron Bit Timing

NVP1918 is able to control coaxitron timing format on the video signal. Start Active line of Coaxitron (BL_TXST_01,0x53, BANK1) is 18th line on VBI. Pulse width of Coaxitron (BAUD, 0x52, BANK1) is fixed 1us. The size of Coaxial Data (PELCO_TXDAT_01~04, 0x70 ~ 0x73, BANK1) is 4 bytes. Refer to Figure 5.4.

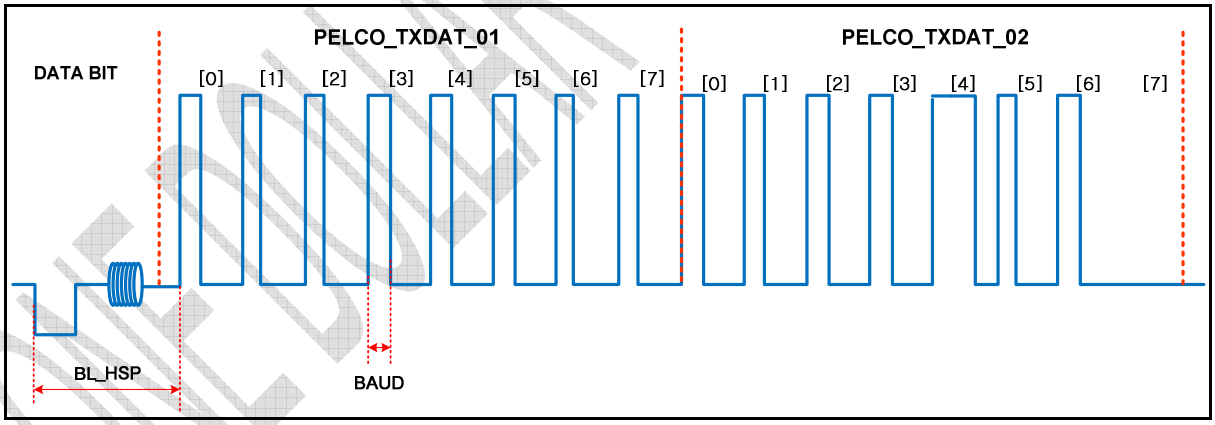


Figure 5.4. Data Structure of Coaxitron Origins (VBI 18th)

6. I2C Interface

I2C interface requires 2 wires, SCL (I2C clock) & SDA (I2C R/W data). **NVP1918** provides special device ID as slave addresses (SA0,SA1). So any combination of 7 bit can be defined as slave address of **NVP1918**. The Figure 6.1 shows read/write protocol of I2C interface. The 1st byte transfers slave address and read/write information. For write mode, the 2nd byte transfers base register index and the 3rd byte transfers date to be written.

For read mode, reading data is transferred during 2nd byte period. The brief I2C interface protocol is shown in Figure 6.2.

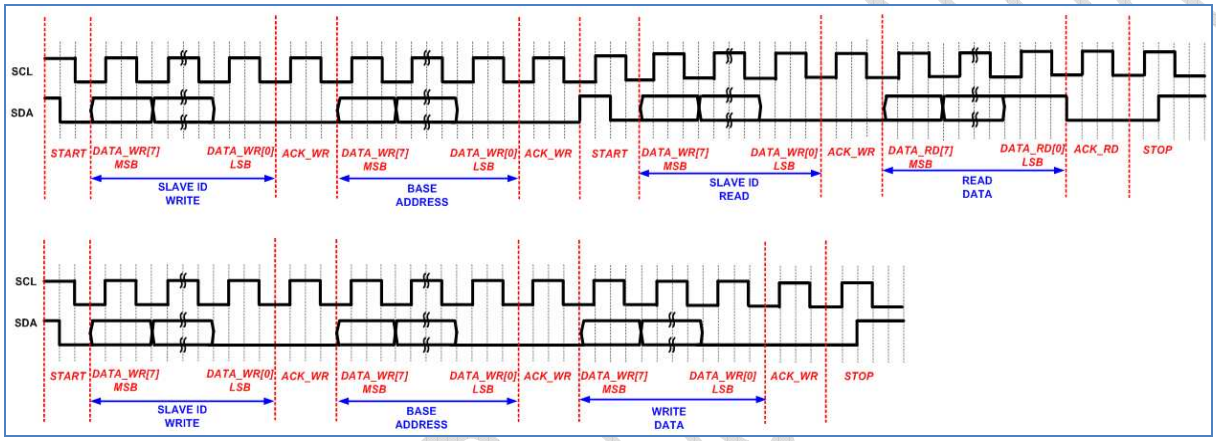


Figure 6.1. I2C Timing Diagram

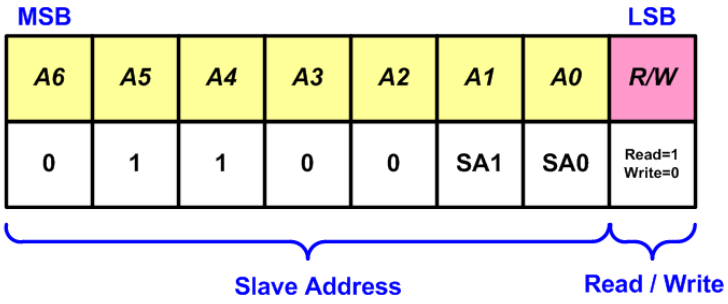


Figure 6.2. I2C Slave Address Configuration

7. Register Description

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK 0	0x00	*RESERVED*								0x11	0x11	0x11
	0x01	*RESERVED*								0x11	0x11	0x11
	0x02	PD_VDAC	PD_VDAC_Y	PD_VDAC_C	-	PD_VCH4	PD_VCH3	PD_VCH2	PD_VCH1	0x10	0x00	0x00
	0x03	-								0x00	0x00	0x00
	0x04	*RESERVED*								0x00	0x00	0x00
	0x05	*RESERVED*								0x00	0x00	0x00
	0x06	RESERVED								0xAF	0xAF	0xAF
	0x07	-								0x00	0x00	0x00
	0x08	AUTO_1	BSF_MODE_1		VIDEO_FORMAT_1					0xDD	0xA0	0xDD
	0x09	AUTO_2	BSF_MODE_2		VIDEO_FORMAT_2					0xDD	0xA0	0xDD
	0x0A	AUTO_3	BSF_MODE_3		VIDEO_FORMAT_3					0xDD	0xA0	0xDD
	0x0B	AUTO_4	BSF_MODE_4		VIDEO_FORMAT_4					0xDD	0xA0	0xDD
	0x0C	BRIGHTNESS_1								0x00	0xF8	0xF8
	0x0D	BRIGHTNESS_2								0x00	0xF8	0xF8
	0x0E	BRIGHTNESS_3								0x00	0xF8	0xF8
	0x0F	BRIGHTNESS_4								0x00	0xF8	0xF8
	0x10	CONTRAST_1								0x80	0x80	0x80
	0x11	CONTRAST_2								0x80	0x80	0x80
	0x12	CONTRAST_3								0x80	0x80	0x80
	0x13	CONTRAST_4								0x80	0x80	0x80
	0x14	H_SHARPNESS_1				V_SHARPNESS_1				0x80	0x80	0x80
	0x15	H_SHARPNESS_2				V_SHARPNESS_2				0x80	0x80	0x80
	0x16	H_SHARPNESS_3				V_SHARPNESS_3				0x80	0x80	0x80
	0x17	H_SHARPNESS_4				V_SHARPNESS_4				0x80	0x80	0x80
	0x18	Y_FIR_MODE_2				Y_FIR_MODE_1				0x33	0x00	0x00
	0x19	Y_FIR_MODE_4				Y_FIR_MODE_3				0x33	0x00	0x00
	0x1A	Y_PEAK_MODE_2				Y_PEAK_MODE_1				0x11	0x11	0x11
	0x1B	Y_PEAK_MODE_4				Y_PEAK_MODE_3				0x11	0x11	0x11
	0x1C	*RESERVED*	PED_ON_1	*RESERVED*						0x04	0x8F	0x8F
	0x1D	*RESERVED*	PED_ON_2	*RESERVED*						0x04	0x8F	0x8F
	0x1E	*RESERVED*	PED_ON_3	*RESERVED*						0x04	0x8F	0x8F
	0x1F	*RESERVED*	PED_ON_4	*RESERVED*						0x04	0x8F	0x8F

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK0	0x20	*RESERVED*								0x00	0x00	0x00
	0x21	*RESERVED*								0x00	0x00	0x00
	0x22	*RESERVED*								0x00	0x00	0x00
	0x23	*RESERVED*								0x00	0x00	0x00
	0x24	*RESERVED*								0x00	0x00	0x00
	0x25	*RESERVED*								0x00	0x00	0x00
	0x26	*RESERVED*								0x00	0x00	0x00
	0x27	*RESERVED*								0x00	0x00	0x00
	0x28	*RESERVED*								0x00	0x00	0x00
	0x29	*RESERVED*								0x00	0x00	0x00
	0x2A	*RESERVED*								0x00	0x00	0x00
	0x2B	*RESERVED*								0x00	0x00	0x00
	0x2C	*RESERVED*								0x00	0x00	0x00
	0x2D	*RESERVED*								0x00	0x00	0x00
	0x2E	*RESERVED*								0x00	0x00	0x00
	0x2F	*RESERVED*								0x00	0x00	0x00
	0x30	*RESERVED*			Y_DELAY_1					0x08	0x08	0x08
	0x31	*RESERVED*			Y_DELAY_2					0x08	0x08	0x08
	0x32	*RESERVED*			Y_DELAY_3					0x08	0x08	0x08
	0x33	*RESERVED*			Y_DELAY_4					0x08	0x08	0x08
	0x34	ACC_OFF_14	*RESERVED*			ACC_GAIN_SPD_14				0x2F	0x2F	0x2F
	0x35	PAL_CM_OFF_14	IF_FIR_SEL_14			CLPF_SEL_14				0x01	0x82	0x02
	0x36	COLOROFF_4	COLOROFF_3	COLOROFF_2	COLOROFF_1	C_KILL_14				0x0B	0x0B	0x0B
	0x37	FLD_DET_SPD_14		*RESERVED*		NOVID_MODE_14				0x43	0x43	0x43
	0x38	CTI_GAIN_1								0x0F	0x08	0x08
	0x39	CTI_GAIN_2								0x0F	0x08	0x08
	0x3A	CTI_GAIN_3								0x0F	0x08	0x08
	0x3B	CTI_GAIN_4								0x0F	0x08	0x08
	0x3C	SATURATION_1								0x80	0x80	0x80
	0x3D	SATURATION_2								0x80	0x80	0x80
	0x3E	SATURATION_3								0x80	0x80	0x80
	0x3F	SATURATION_4								0x80	0x80	0x80

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK0	0x40	HUE_1								0x00	0x01	0x00
	0x41	HUE_2								0x00	0x01	0x00
	0x42	HUE_3								0x00	0x01	0x00
	0x43	HUE_4								0x00	0x01	0x00
	0x44	U_GAIN_1								0x00	0x00	0x00
	0x45	U_GAIN_2								0x00	0x00	0x00
	0x46	U_GAIN_3								0x00	0x00	0x00
	0x47	U_GAIN_4								0x00	0x00	0x00
	0x48	V_GAIN_1								0x03	0x00	0x00
	0x49	V_GAIN_2								0x03	0x00	0x00
	0x4A	V_GAIN_3								0x03	0x00	0x00
	0x4B	V_GAIN_4								0x03	0x00	0x00
	0x4C	U_OFFSET_1								0x04	0x00	0x04
	0x4D	U_OFFSET_2								0x04	0x00	0x04
	0x4E	U_OFFSET_3								0x04	0x00	0x04
	0x4F	U_OFFSET_4								0x04	0x00	0x04
	0x50	V_OFFSET_1								0x04	0x00	0x04
	0x51	V_OFFSET_2								0x04	0x00	0x04
	0x52	V_OFFSET_3								0x04	0x00	0x04
	0x53	V_OFFSET_4								0x04	0x00	0x04
	0x54	FLD_INV_4	FLD_INV_3	FLD_INV_2	FLD_INV_1	NOVID_INF_IN_14	CHID_TYPE_14			0x01	0xF1	0x01
	0x55	CHID_VIN2				CHID_VIN1				0x10	0x10	0x10
	0x56	CHID_VIN4				CHID_VIN3				0x32	0x32	0x32
	0x57	-								0x00	0x00	0x00
	0x58	H_DELAY_1								0x29	0xB2	0xB2
	0x59	H_DELAY_2								0x29	0xB2	0xB2
	0x5A	H_DELAY_3								0x29	0xB2	0xB2
	0x5B	H_DELAY_4								0x29	0xB2	0xB2
	0x5C	V_DELAY_1								0x1E	0x1E	0x1E
	0x5D	V_DELAY_2								0x1E	0x1E	0x1E
	0x5E	V_DELAY_3								0x1E	0x1E	0x1E
	0x5F	V_DELAY_4								0x1E	0x1E	0x1E

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK0	0x60	HBLK_END_1								0x00	0x00	0x00
	0x61	HBLK_END_2								0x00	0x00	0x00
	0x62	HBLK_END_3								0x00	0x00	0x00
	0x63	HBLK_END_4								0x00	0x00	0x00
	0x64	VBLK_END_1								0x0D	0x08	0x0D
	0x65	VBLK_END_2								0x0D	0x08	0x0D
	0x66	VBLK_END_3								0x0D	0x08	0x0D
	0x67	VBLK_END_4								0x0D	0x08	0x0D
	0x68	H_CROP_S_1								0x00	0x00	0x00
	0x69	H_CROP_S_2								0x00	0x00	0x00
	0x6A	H_CROP_S_3								0x00	0x00	0x00
	0x6B	H_CROP_S_4								0x00	0x00	0x00
	0x6C	H_CROP_E_1								0x00	0x00	0x00
	0x6D	H_CROP_E_2								0x00	0x00	0x00
	0x6E	H_CROP_E_3								0x00	0x00	0x00
	0x6F	H_CROP_E_4								0x00	0x00	0x00
	0x70	V_CROP_S_1								0x00	0x00	0x00
	0x71	V_CROP_S_2								0x00	0x00	0x00
	0x72	V_CROP_S_3								0x00	0x00	0x00
	0x73	V_CROP_S_4								0x00	0x00	0x00
	0x74	V_CROP_E_1								0x00	0x00	0x00
	0x75	V_CROP_E_2								0x00	0x00	0x00
	0x76	V_CROP_E_3								0x00	0x00	0x00
	0x77	V_CROP_E_4								0x00	0x00	0x00
	0x78	BGDCOL_2				BGDCOL_1				0x88	0x88	0x88
	0x79	BGDCOL_4				BGDCOL_3				0x88	0x88	0x88
	0x7A	DATA_OUT_MODE_2				DATA_OUT_MODE_1				0x11	0x11	0x11
	0x7B	DATA_OUT_MODE_4				DATA_OUT_MODE_3				0x11	0x11	0x11
	0x7C	-								0x00	0x00	0x00
	0x7D	-								0x00	0x00	0x00
	0x7E	-								0x00	0x00	0x00
	0x7F	-								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK0	0x80	*RESERVED*								0x11	0x11	0x11
	0x81	*RESERVED*								0x11	0x11	0x11
	0x82	-				PD_VCH8	PD_VCH7	PD_VCH6	PD_VCH5	0x00	0x00	0x00
	0x83	-								0x00	0x00	0x00
	0x84	*RESERVED*								0x00	0x00	0x00
	0x85	*RESERVED*								0x00	0x00	0x00
	0x86	*RESERVED*								0xAF	0xAF	0xAF
	0x87	-								0x00	0x00	0x00
	0x88	AUTO_5	BSF_MODE_5		VIDEO_FORMAT_5					0xDD	0xA0	0xDD
	0x89	AUTO_6	BSF_MODE_6		VIDEO_FORMAT_6					0xDD	0xA0	0xDD
	0x8A	AUTO_7	BSF_MODE_7		VIDEO_FORMAT_7					0xDD	0xA0	0xDD
	0x8B	AUTO_8	BSF_MODE_8		VIDEO_FORMAT_8					0xDD	0xA0	0xDD
	0x8C	BRIGHTNESS_5								0x00	0xF8	0xF8
	0x8D	BRIGHTNESS_6								0x00	0xF8	0xF8
	0x8E	BRIGHTNESS_7								0x00	0xF8	0xF8
	0x8F	BRIGHTNESS_8								0x00	0xF8	0xF8
	0x90	CONTRAST_5								0x80	0x80	0x80
	0x91	CONTRAST_6								0x80	0x80	0x80
	0x92	CONTRAST_7								0x80	0x80	0x80
	0x93	CONTRAST_8								0x80	0x80	0x80
	0x94	H_SHARPNESS_5				V_SHARPNESS_5				0x80	0x80	0x80
	0x95	H_SHARPNESS_6				V_SHARPNESS_6				0x80	0x80	0x80
	0x96	H_SHARPNESS_7				V_SHARPNESS_7				0x80	0x80	0x80
	0x97	H_SHARPNESS_8				V_SHARPNESS_8				0x80	0x80	0x80
	0x98	Y_FIR_MODE_6				Y_FIR_MODE_5				0x33	0x00	0x00
	0x99	Y_FIR_MODE_8				Y_FIR_MODE_7				0x33	0x00	0x00
	0x9A	Y_PEAK_MODE_6				Y_PEAK_MODE_5				0x11	0x11	0x11
	0x9B	Y_PEAK_MODE_8				Y_PEAK_MODE_7				0x11	0x11	0x11
	0x9C	*RESERVED*	PED_ON_5		*RESERVED*					0x04	0x8F	0x8F
	0x9D	*RESERVED*	PED_ON_6		*RESERVED*					0x04	0x8F	0x8F
	0x9E	*RESERVED*	PED_ON_7		*RESERVED*					0x04	0x8F	0x8F
	0x9F	*RESERVED*	PED_ON_8		*RESERVED*					0x04	0x8F	0x8F

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK0	0xA0	*RESERVED*								0x00	0x00	0x00
	0xA1	*RESERVED*								0x00	0x00	0x00
	0xA2	*RESERVED*								0x00	0x00	0x00
	0xA3	*RESERVED*								0x00	0x00	0x00
	0xA4	*RESERVED*								0x00	0x00	0x00
	0xA5	*RESERVED*								0x00	0x00	0x00
	0xA6	*RESERVED*								0x00	0x00	0x00
	0xA7	*RESERVED*								0x00	0x00	0x00
	0xA8	*RESERVED*								0x00	0x00	0x00
	0xA9	*RESERVED*								0x00	0x00	0x00
	0xAA	*RESERVED*								0x00	0x00	0x00
	0xAB	*RESERVED*								0x00	0x00	0x00
	0xAC	*RESERVED*								0x00	0x00	0x00
	0xAD	*RESERVED*								0x00	0x00	0x00
	0xAE	*RESERVED*								0x00	0x00	0x00
	0xAF	*RESERVED*								0x00	0x00	0x00
	0xB0	*RESERVED*			Y_DELAY_5					0x08	0x08	0x08
	0xB1	*RESERVED*			Y_DELAY_6					0x08	0x08	0x08
	0xB2	*RESERVED*			Y_DELAY_7					0x08	0x08	0x08
	0xB3	*RESERVED*			Y_DELAY_8					0x08	0x08	0x08
	0xB4	ACC_OFF_58	*RESERVED*			ACC_GAIN_SPD_58				0x2F	0x2F	0x2F
	0xB5	PAL_CM_OFF_58	IF_FIR_SEL_58			CLPF_SEL_58				0x01	0x82	0x02
	0xB6	COLOROFF_8	COLOROFF_7	COLOROFF_6	COLOROFF_5	C_KILL_58				0x03	0x0B	0x0B
	0xB7	FLD_DET_SPD_58		*RESERVED*		NOVID_MODE_58				0x43	0x43	0x43
	0xB8	CTI_GAIN_5								0x0F	0x08	0x08
	0xB9	CTI_GAIN_6								0x0F	0x08	0x08
	0xBA	CTI_GAIN_7								0x0F	0x08	0x08
	0xBB	CTI_GAIN_8								0x0F	0x08	0x08
	0xBC	SATURATION_5								0x80	0x80	0x80
	0xBD	SATURATION_6								0x80	0x80	0x80
	0xBE	SATURATION_7								0x80	0x80	0x80
	0xBF	SATURATION_8								0x80	0x80	0x80

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK0	0xC0	HUE_5								0x00	0x01	0x00
	0xC1	HUE_6								0x00	0x01	0x00
	0xC2	HUE_7								0x00	0x01	0x00
	0xC3	HUE_8								0x00	0x01	0x00
	0xC4	U_GAIN_5								0x00	0x00	0x00
	0xC5	U_GAIN_6								0x00	0x00	0x00
	0xC6	U_GAIN_7								0x00	0x00	0x00
	0xC7	U_GAIN_8								0x00	0x00	0x00
	0xC8	V_GAIN_5								0x03	0x00	0x00
	0xC9	V_GAIN_6								0x03	0x00	0x00
	0xCA	V_GAIN_7								0x03	0x00	0x00
	0xCB	V_GAIN_8								0x03	0x00	0x00
	0xCC	U_OFFSET_5								0x04	0x00	0x04
	0xCD	U_OFFSET_6								0x04	0x00	0x04
	0xCE	U_OFFSET_7								0x04	0x00	0x04
	0xCF	U_OFFSET_8								0x04	0x00	0x04
	0xD0	V_OFFSET_5								0x04	0x00	0x04
	0xD1	V_OFFSET_6								0x04	0x00	0x04
	0xD2	V_OFFSET_7								0x04	0x00	0x04
	0xD3	V_OFFSET_8								0x04	0x00	0x04
	0xD4	FLD_INV_8	FLD_INV_7	FLD_INV_6	FLD_INV_5	NOVID_INF_IN_14	CHID_TYPE_58			0x01	0xF1	0x01
	0xD5	CHID_VIN6				CHID_VIN5				0x54	0x54	0x54
	0xD6	CHID_VIN8				CHID_VIN7				0x76	0x76	0x76
	0xD7	-								0x00	0x00	0x00
	0xD8	H_DELAY_5								0x29	0xB2	0xB2
	0xD9	H_DELAY_6								0x29	0xB2	0xB2
	0xDA	H_DELAY_7								0x29	0xB2	0xB2
	0xDB	H_DELAY_8								0x29	0xB2	0xB2
	0xDC	V_DELAY_5								0x1E	0x1E	0x1E
	0xDD	V_DELAY_6								0x1E	0x1E	0x1E
	0xDE	V_DELAY_7								0x1E	0x1E	0x1E
	0xDF	V_DELAY_8								0x1E	0x1E	0x1E

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK0	0xE0	HBLK_END_5								0x00	0x00	0x00
	0xE1	HBLK_END_6								0x00	0x00	0x00
	0xE2	HBLK_END_7								0x00	0x00	0x00
	0xE3	HBLK_END_8								0x00	0x00	0x00
	0xE4	VBLK_END_5								0x0D	0x08	0x0D
	0xE5	VBLK_END_6								0x0D	0x08	0x0D
	0xE6	VBLK_END_7								0x0D	0x08	0x0D
	0xE7	VBLK_END_8								0x0D	0x08	0x0D
	0xE8	H_CROP_S_5								0x00	0x00	0x00
	0xE9	H_CROP_S_6								0x00	0x00	0x00
	0xEA	H_CROP_S_7								0x00	0x00	0x00
	0xEB	H_CROP_S_8								0x00	0x00	0x00
	0xEC	H_CROP_E_5								0x00	0x00	0x00
	0xED	H_CROP_E_6								0x00	0x00	0x00
	0xEE	H_CROP_E_7								0x00	0x00	0x00
	0xEF	H_CROP_E_8								0x00	0x00	0x00
	0xF0	V_CROP_S_5								0x00	0x00	0x00
	0xF1	V_CROP_S_6								0x00	0x00	0x00
	0xF2	V_CROP_S_7								0x00	0x00	0x00
	0xF3	V_CROP_S_8								0x00	0x00	0x00
	0xF4	V_CROP_E_5								0x00	0x00	0x00
	0xF5	V_CROP_E_6								0x00	0x00	0x00
	0xF6	V_CROP_E_7								0x00	0x00	0x00
	0xF7	V_CROP_E_8								0x00	0x00	0x00
	0xF8	BGDCOL_6				BGDCOL_5				0x88	0x88	0x88
	0xF9	BGDCOL_8				BGDCOL_7				0x88	0x88	0x88
	0xFA	DATA_OUT_MODE_6				DATA_OUT_MODE_5				0x11	0x11	0x11
	0xFB	DATA_OUT_MODE_8				DATA_OUT_MODE_7				0x11	0x11	0x11
	0xFC	-								0x00	0x00	0x00
	0xFD	-								0x00	0x00	0x00
	0xFE	-								0x00	0x00	0x00
	0xFF	-				BANK_SEL				0x00	0x00	0x00

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK1	0x00	PD_AAL	PD_AAM	-	PD_AD	RM_PB_PIN	PB_RM_PIN	FILTER_ON	EN_32K_ MODE	0x02	0x02	0x02
	0x01	AIGAIN_02				AIGAIN_01				0x00	0x88	0x88
	0x02	AIGAIN_04				AIGAIN_03				0x00	0x88	0x88
	0x03	AIGAIN_06				AIGAIN_05				0x00	0x88	0x88
	0x04	AIGAIN_08				AIGAIN_07				0x00	0x88	0x88
	0x05	MIGAIN_02				MIGAIN_01				0x00	0x88	0x88
	0x06	CAS_PB	TRANS_MODE	-	CAS_PIN	CASCADE_ MODE	PB_MODE	CHIP_STAGE		0x1B	0x1B	0x1B
	0x07	RM_MASTER	RM_CLK	RM_BITRATE		RM_SAMRATE	RM_BITWID	RM_SSP	RM_SYNC	0xC8	0xC8	0xC8
	0x08	RM_BIT_ SWAP	-			R_ADATSP2	R_ADATSP	R_MULTCH		0x03	0x03	0x03
	0x09	RM_FORMAT		-		RM_LAW_SEL	-			0x00	0x00	0x00
	0x0A	R_SEQ_02				R_SEQ_01				0x10	0x10	0x10
	0x0B	R_SEQ_04				R_SEQ_03				0x32	0x32	0x32
	0x0C	R_SEQ_06				R_SEQ_05				0x54	0x54	0x54
	0x0D	R_SEQ_08				R_SEQ_07				0x76	0x76	0x76
	0x0E	R_SEQ_10				R_SEQ_09				0x98	0x98	0x98
	0x0F	R_SEQ_12				R_SEQ_11				0Xba	0xBA	0xBA
	0x10	R_SEQ_14				R_SEQ_13				0Xdc	0xDC	0xDC
	0x11	R_SEQ_16				R_SEQ_15				0xFE	0xFE	0xFE
	0x12	MIC_SEQ_04		MIC_SEQ_03		MIC_SEQ_02		MIC_SEQ_01		0xE4	0xE4	0xE4
	0x13	PB_MASTER	PB_CLK	PB_BITRATE		PB_SAMRATE	PB_BITWID	PB_SSP	PB_SYNC	0x08	0x08	0x08
	0x14	PB_BIT_ SWAP	-			PB_SEL				0x00	0x00	0x00
	0x15	PB_FORMAT		-		PB_ LAW_SEL	--			0x00	0x00	0x00
	0x16	MIX_RATIO_02				MIX_RATIO_01				0x88	0x88	0x88
	0x17	MIX_RATIO_04				MIX_RATIO_03				0x88	0x88	0x88
	0x18	MIX_RATIO_06				MIX_RATIO_05				0x88	0x88	0x88
	0x19	MIX_RATIO_08				MIX_RATIO_07				0x88	0x88	0x88
	0x1A	MIX_RATIO_10				MIX_RATIO_09				0x88	0x88	0x88
	0x1B	MIX_RATIO_12				MIX_RATIO_11				0x88	0x88	0x88
	0x1C	MIX_RATIO_14				MIX_RATIO_13				0x88	0x88	0x88
	0x1D	MIX_RATIO_16				MIX_RATIO_15				0x88	0x88	0x88
	0x1E	MIX_RATIO_M2				MIX_RATIO_M1				0x88	0x88	0x88
	0x1F	MIX_RATIO_M4				MIX_RATIO_M3				0x88	0x88	0x88

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK1	0x20	MIX_RATIO_P2				MIX_RATIO_P1				0x88	0x88	0x88
	0x21	MIX_RATIO_P4				MIX_RATIO_P3				0x88	0x88	0x88
	0x22	AOGAIN				-				0x80	0x80	0x80
	0x23	-		MIX_DERATIO		MIX_OUTSEL				0x19	0x19	0x19
	0x24	-				L_CH_OUTSEL				0x18	0x18	0x18
	0x25	-				R_CH_OUTSEL				0x16	0x16	0x16
	0x26	MIX_MUTE_08	MIX_MUTE_07	MIX_MUTE_06	MIX_MUTE_05	MIX_MUTE_04	MIX_MUTE_03	MIX_MUTE_02	MIX_MUTE_01	0x00	0x00	0x00
	0x27	MIX_MUTE_16	MIX_MUTE_15	MIX_MUTE_14	MIX_MUTE_13	MIX_MUTE_12	MIX_MUTE_11	MIX_MUTE_10	MIX_MUTE_09	0x00	0x00	0x00
	0x28	MIX_MUTE_M4	MIX_MUTE_M3	MIX_MUTE_M2	MIX_MUTE_M1	MIX_MUTE_P4	MIX_MUTE_P3	MIX_MUTE_P2	MIX_MUTE_P1	0x00	0x00	0x00
	0x29	*RESERVED*				ADET_MODE	ADET_FILT			0x88	0x88	0x88
	0x2A	ADET_08	ADET_07	ADET_06	ADET_05	ADET_04	ADET_03	ADET_02	ADET_01	0xFF	0xFF	0xFF
	0x2B	ADET_M2	ADET_M1	-						0xC0	0xC0	0xC0
	0x2C	ADET_TH_02				ADET_TH_01				0xAA	0xAA	0xAA
	0x2D	ADET_TH_04				ADET_TH_03				0xAA	0xAA	0xAA
	0x2E	ADET_TH_06				ADET_TH_05				0xAA	0xAA	0xAA
	0x2F	ADET_TH_08				ADET_TH_07				0xAA	0xAA	0xAA
	0x30	ADET_TH_M2				ADET_TH_M1				0xAA	0xAA	0xAA
	0x31	*RESERVED*						DCA0		0x02	0x02	0x02
	0x32	DCA1								0x00	0x00	0x00
	0x33	*RESERVED*						DCB0		0x02	0x02	0x02
	0x34	DCB1								0x00	0x00	0x00
	0x35	-								0x02	0x00	0x00
	0x36	-								0x00	0x00	0x00
	0x37	REC_8K		PB_8K		*RESERVED*				0x00	0x00	0x00
	0x38	*RESERVED*			AUD_SW_RST	-				0x00	0x00	0x00
	0x39	RM_DELAY	PB_DELAY	*RESERVED*						0x05	0x05	0x05
	0x3A	*RESERVED*								0xA1	0xA1	0xA1
	0x3B	*RESERVED*								0x10	0x10	0x10
	0x3C	*RESERVED*								0x10	0x10	0x10
	0x3D	*RESERVED*								0x00	0x00	0x00
	0x3E	*RESERVED*								0x07	0x08	0x08
	0x3F	*RESERVED*								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK1	0x40	-								0x00	0x00	0x00
	0x41	-								0x00	0x00	0x00
	0x42	-								0x00	0x00	0x00
	0x43	-								0x00	0x00	0x00
	0x44	*RESERVED*								0x11	0x14	0x14
	0x45	*RESERVED*								0x00	0x01	0x01
	0x46	*RESERVED*								0x11	0x00	0x00
	0x47	*RESERVED*								0x20	0x00	0x00
	0x48	*RESERVED*							**VPLL_C**	0x60	0x60	0x60
	0x49	-			**PLL_OFF**	-		**PLL_BP**	**PLL_RST**	0x00	0x00	0x00
	0x4A	-		**OD**		**N**				0x22	0x22	0x22
	0x4B	**M**								0x20	0x20	0x20
	0x4C	*RESERVED*								0x00	0x00	0x00
	0x4D	*RESERVED*								0x00	0x00	0x00
	0x4E	*RESERVED*								0x00	0x00	0x00
	0x4F	-								0x00	0x00	0x00
	0x50	**BAUD**								0x37	0x37	0x37
	0x51	**RBAUD**								0x37	0x37	0x37
	0x52	**PELCO_BAUD**								0x1B	0x1B	0x1B
	0x53	**BL_TXST_01**								0x05	0x05	0x05
	0x54	-				**BL_TXST_02**				0x00	0x00	0x00
	0x55	**BL_RXST_01**								0x07	0x07	0x07
	0x56	-				**BL_RXST_02**				0x00	0x00	0x00
	0x57	**PELCO_TXST_01**								0x09	0x09	0x09
	0x58	-				**PELCO_TXST_02**				0x00	0x00	0x00
	0x59	-							**TX_START**	0x00	0x00	0x00
	0x5A	-			**TX_BYTE_LENGTH**					0x08	0x08	0x08
	0x5B	-					**PACKET_MODE**			0x06	0x06	0x06
	0x5C	-							**PELCO_CTEN**	0x00	0x00	0x00
	0x5D	**BL_HSP_01**								0x46	0x46	0x46
	0x5E	-			**BL_HSP_02**					0x00	0x00	0x00
	0x5F	-							**PELCO_SHOT**	0x00	0x00	0x00

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK1	0x60	TX_DATA_01								0xAA	0xAA	0xAA
	0x61	TX_DATA_02								0x1B	0x1C	0x1C
	0x62	TX_DATA_03								0x00	0x18	0x18
	0x63	TX_DATA_04								0x00	0xFF	0xFF
	0x64	TX_DATA_05								0xAA	0xAA	0xAA
	0x65	TX_DATA_06								0x3B	0x3C	0x3C
	0x66	TX_DATA_07								0x00	0xFF	0xFF
	0x67	TX_DATA_08								0x1F	0xFF	0xFF
	0x68	TX_DATA_09								0xAA	0xAA	0xAA
	0x69	TX_DATA_10								0x1C	0x1B	0x1B
	0x6A	TX_DATA_11								0x18	0x00	0x00
	0x6B	TX_DATA_12								0xFF	0x00	0x00
	0x6C	TX_DATA_13								0xAA	0xAA	0xAA
	0x6D	TX_DATA_14								0x3C	0x3B	0x3B
	0x6E	TX_DATA_15								0xFF	0x00	0x00
	0x6F	TX_DATA_16								0xFF	0x00	0x00
	0x70	PELCO_TXDAT_01								0xFF	0x00	0x00
	0x71	PELCO_TXDAT_02								0x00	0x00	0x00
	0x72	PELCO_TXDAT_03								0xFF	0x00	0x00
	0x73	PELCO_TXDAT_04								0x00	0x00	0x00
	0x74	RX_DATA_01								R	R	R
	0x75	RX_DATA_02								R	R	R
	0x76	RX_DATA_03								R	R	R
	0x77	RX_DATA_04								R	R	R
	0x78	RX_DATA_05								R	R	R
	0x79	RX_DATA_06								R	R	R
	0x7A	RX_DATA_07								R	R	R
	0x7B	RX_DATA_08								R	R	R
	0x7C	VSO_INV								0x00	0x00	0x00
	0x7D	HSO_INV								0x00	0x00	0x00
	0x7E	RX_THRESHOLD								0x80	0x80	0x80
	0x7F	Hidden_Even_line_modification								0x01	0x01	0x01

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK 1	0x80	*RESERVED*								0x00	0x00	0x00
	0x81	*RESERVED*								0xFF	0xFF	0xFF
	0x82	*RESERVED*								0x00	0x00	0x00
	0x83	*RESERVED*								0x00	0x00	0x00
	0x84	*RESERVED*								0x00	0x00	0x00
	0x85	*RESERVED*								0x00	0x00	0x00
	0x86	*RESERVED*								0x06	0x00	0x00
	0x87	*RESERVED*								0x01	0x00	0x00
	0x88	*RESERVED*								0x00	0x00	0x00
	0x89	*RESERVED*								0x00	0x00	0x00
	0x8A	*RESERVED*								0x00	0x00	0x00
	0x8B	-					DEVICE_SEL			0x00	0x00	0x00
	0x8C	COAX_OUT_SEL_2				COAX_OUT_SEL_1				0x10	0x10	0x10
	0x8D	COAX_OUT_SEL_4				COAX_OUT_SEL_3				0x32	0x32	0x32
	0x8E	COAX_OUT_SEL_6				COAX_OUT_SEL_5				0x54	0x54	0x54
	0x8F	COAX_OUT_SEL_8				COAX_OUT_SEL_7				0x76	0x76	0x76
	0x90	-							CLEAN	0x00	0x00	0x00
	0x91	-								0x00	0x00	0x00
	0x92	-								0x00	0x00	0x00
	0x93	-								0x00	0x00	0x00
	0x94	*RESERVED*								0x00	0x00	0x00
	0x95	-								0x00	0x00	0x00
	0x96	-								0x00	0x00	0x00
	0x97	-								0x00	0x00	0x00
	0x98	-								0x00	0x00	0x00
	0x99	-								0x00	0x00	0x00
	0x9A	-								0x00	0x00	0x00
	0x9B	-								0x00	0x00	0x00
	0x9C	-								0x00	0x00	0x00
	0x9D	-								0x00	0x00	0x00
	0x9E	-								0x00	0x00	0x00
	0x9F	-								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK1	0xA0	BW	CCIR656	PATTERN_ON	BLANK_ON	LNFMT	V_ALTER	FSC_SEL		0x2D	0x00	0x0D
	0xA1	*RESERVED*								0x00	0x00	0x00
	0xA2	-	BURST_RST	-		PAT_NO				0x47	0x47	0x47
	0xA3	CBYPASS	-	CFIR_NO		-	YFIL_NO			0x35	0x35	0x35
	0xA4	Y_GAIN								0x80	0x8D	0x89
	0xA5	U_GAIN								0x80	0x85	0x95
	0xA6	V_GAIN								0x80	0x88	0x95
	0xA7	SYNC_GAIN								0x80	0x80	0x80
	0xA8	BURST_GAIN								0x80	0x8C	0x93
	0xA9	PED_GAIN								0x80	0x80	0x80
	0xAA	BLANK_LVL								0x80	0x80	0x80
	0xAB	PHASE_TURN								0x80	0x80	0x80
	0xAC	H_DELAY								0x00	0x00	0x00
	0xAD	V_DELAY								0x00	0x00	0x00
	0xAE	-							YC_ON	0x00	0x01	0x01
	0xAF	-								0x00	0x00	0x00
	0xB0	-								0x00	0x00	0x00
	0xB1	-								0x00	0x00	0x00
	0xB2	-								0x00	0x00	0x00
	0xB3	-								0x00	0x00	0x00
	0xB4	*RESERVED*								0x00	0x40	0x40
	0xB5	*RESERVED*								0x00	0x30	0x30
	0xB6	*RESERVED*								0x00	0x40	0x40
	0xB7	*RESERVED*								0x00	0x30	0x30
	0xB8	*RESERVED*								0x00	0x40	0x40
	0xB9	*RESERVED*								0x00	0x30	0x30
	0xBA	*RESERVED*								0x00	0x40	0x40
	0xBB	*RESERVED*								0x00	0x30	0x30
	0xBC	MPP_SEL2				MPP_SEL1				0x00	0x00	0x00
	0xBD	MPP_SEL4				MPP_SEL3				0x00	0x00	0x00
	0xBE	MPP_SEL6				MPP_SEL5				0x00	0x00	0x00
	0xBF	MPP_SEL8				MPP_SEL7				0x00	0x00	0x00

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK1	0xC0	VPORTA_SEQ2				VPORTA_SEQ1				0x10	0x10	0x10
	0xC1	VPORTA_SEQ4				VPORTA_SEQ3				0x10	0x10	0x10
	0xC2	VPORTB_SEQ2				VPORTB_SEQ1				0x32	0x32	0x32
	0xC3	VPORTB_SEQ4				VPORTB_SEQ3				0x32	0x32	0x32
	0xC4	VPORTC_SEQ2				VPORTC_SEQ1				0x54	0x54	0x54
	0xC5	VPORTC_SEQ4				VPORTC_SEQ3				0x54	0x54	0x54
	0xC6	VPORTD_SEQ2				VPORTD_SEQ1				0x76	0x76	0x76
	0xC7	VPORTD_SEQ4				VPORTD_SEQ3				0x76	0x76	0x76
	0xC8	CH_OUT_SELB				CH_OUT_SELA				0x22	0x22	0x22
	0xC9	CH_OUT_SELD				CH_OUT_SELC				0x22	0x22	0x22
	0xCA	-				VDO_4_EN	VDO_3_EN	VDO_2_EN	VDO_1_EN	0x00	0x0F	0x0F
	0xCB	MPP_INV8	MPP_INV7	MPP_INV6	MPP_INV5	MPP_INV4	MPP_INV3	MPP_INV2	MPP_INV1	0x00	0x00	0x00
	0xCC	VCLK_1_SEL				VCLK_1_DLY_SEL				0x30	0x30	0x30
	0xCD	VCLK_2_SEL				VCLK_2_DLY_SEL				0x10	0x30	0x30
	0xCE	VCLK_3_SEL				VCLK_3_DLY_SEL				0x30	0x30	0x30
	0xCF	VCLK_4_SEL				VCLK_4_DLY_SEL				0x10	0x30	0x30
	0xD0	*RESERVED*				OUT_DATA_INV				0x00	0x00	0x00
	0xD1	*RESERVED*								0x00	0x00	0x00
	0xD2	-								0x00	0x00	0x00
	0xD3	-								0x00	0x00	0x00
	0xD4	*RESERVED*								0x00	0x00	0x00
	0xD5	-							S_CLK_ON	0x00	0x00	0x00
	0xD6	MPP8_DIR	MPP7_DIR	MPP6_DIR	MPP5_DIR	MPP4_DIR	MPP3_DIR	MPP2_DIR	MPP1_DIR	0x00	0x00	0x00
	0xD7	-								0x00	0x00	0x00
	0xD8	NOVID_08	NOVID_07	NOVID_06	NOVID_05	NOVID_04	NOVID_03	NOVID_02	NOVID_01	R	R	R
	0xD9	MOTION_08	MOTION_07	MOTION_06	MOTION_05	MOTION_04	MOTION_03	MOTION_02	MOTION_01	R	R	R
	0xDA	BLACK_08	BLACK_07	BLACK_06	BLACK_05	BLACK_04	BLACK_03	BLACK_02	BLACK_01	R	R	R
	0xDB	WHITE_08	WHITE_07	WHITE_06	WHITE_05	WHITE_04	WHITE_03	WHITE_02	WHITE_01	R	R	R
	0xDC	MUTE_08	MUTE_07	MUTE_06	MUTE_05	MUTE_04	MUTE_03	MUTE_02	MUTE_01	R	R	R
	0xDD	MUTE_16	MUTE_15	MUTE_14	MUTE_13	MUTE_12	MUTE_11	MUTE_10	MUTE_09	R	R	R
	0xDE	-				MUTEMIC_04	MUTEMIC_03	MUTEMIC_02	MUTEMIC_01	R	R	R
	0xDF	-								0x00	0x00	0x00

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK1	0xE0	NOVID_08B	NOVID_07B	NOVID_06B	NOVID_05B	NOVID_04B	NOVID_03B	NOVID_02B	NOVID_01B	R	R	R
	0xE1	MOTION_08B	MOTION_07B	MOTION_06B	MOTION_05B	MOTION_04B	MOTION_03B	MOTION_02B	MOTION_01B	R	R	R
	0xE2	BLACK_08B	BLACK_07B	BLACK_06B	BLACK_05B	BLACK_04B	BLACK_03B	BLACK_02B	BLACK_01B	R	R	R
	0xE3	WHITE_08B	WHITE_07B	WHITE_06B	WHITE_05B	WHITE_04B	WHITE_03B	WHITE_02B	WHITE_01B	R	R	R
	0xE4	MUTE_08B	MUTE_07B	MUTE_06B	MUTE_05B	MUTE_04B	MUTE_03B	MUTE_02B	MUTE_01B	R	R	R
	0xE5	MUTE_16B	MUTE_15B	MUTE_14B	MUTE_13B	MUTE_12B	MUTE_11B	MUTE_10B	MUTE_09B	R	R	R
	0xE6	-				MUTEMIC_04B	MUTEMIC_03B	MUTEMIC_02B	MUTEMIC_01B	R	R	R
	0xE7	-								0x00	0x00	0x00
	0xE8	RD_STATE_CLR	-		STATE_HOLD	-				0x90	0x90	0x90
	0xE9	-				IRQ_INV	IRQ_SEL			0x00	0x00	0x00
	0xEA	-								0x00	0x00	0x00
	0xEB	-								0x00	0x00	0x00
	0xEC	AGC_LOCK_08	AGC_LOCK_07	AGC_LOCK_06	AGC_LOCK_05	AGC_LOCK_04	AGC_LOCK_03	AGC_LOCK_02	AGC_LOCK_01	R	R	R
	0xED	CMP_LOCK_08	CMP_LOCK_07	CMP_LOCK_06	CMP_LOCK_05	CMP_LOCK_04	CMP_LOCK_03	CMP_LOCK_02	CMP_LOCK_01	R	R	R
	0xEE	H_LOCK_08	H_LOCK_07	H_LOCK_06	H_LOCK_05	H_LOCK_04	H_LOCK_03	H_LOCK_02	H_LOCK_01	R	R	R
	0xEF	Auto_NT_04		Auto_NT_03		Auto_NT_02		Auto_NT_01		R	R	R
	0xF0	Auto_NT_08		Auto_NT_07		Auto_NT_06		Auto_NT_05		R	R	R
	0xF1	FLD_04		FLD_03		FLD_02		FLD_01		R	R	R
	0xF2	FLD_07		FLD_06		FLD_05		FLD_04		R	R	R
	0xF3	BW_08	BW_07	BW_06	BW_05	BW_04	BW_03	BW_02	BW_08	R	R	R
	0xF4	DEV_ID(0x80)								R	R	R
	0xF5	*RESERVED(0x0)*				REV_ID(0x0)				R	R	R
	0xF6	CMP_VALUE								R	R	R
	0xF7	AGC_VALUE								R	R	R
	0xF8	-				CMP_AGC_CH				0x00	0x00	0x00
	0xF9	-								0x00	0x00	0x00
	0xFA	-								0x00	0x00	0x00
	0xFB	-								0x00	0x00	0x00
	0xFC	-								0x00	0x00	0x00
	0xFD	-								0x00	0x00	0x00
	0xFE	-								0x00	0x00	0x00
	0xFF	-				BANK_SEL				0x00	0x00	0x00

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0x00	*RESERVED*			MOTION_OFF 01	*RESERVED*		MOTION_PIC_01		0X03	0X03	0X03
	0x01	MOD_TSEN_01								0X60	0X60	0X60
	0x02	*RESERVED*			MOTION_OFF 02	*RESERVED*		MOTION_PIC_02		0X03	0X03	0X03
	0x03	MOD_TSEN_02								0X60	0X60	0X60
	0x04	*RESERVED*			MOTION_OFF 03	*RESERVED*		MOTION_PIC_03		0X03	0X03	0X03
	0x05	MOD_TSEN_03								0X60	0X60	0X60
	0x06	*RESERVED*			MOTION_OFF 04	*RESERVED*		MOTION_PIC_04		0X03	0X03	0X03
	0x07	MOD_TSEN_04								0X60	0X60	0X60
	0x08	*RESERVED*			MOTION_OFF 05	*RESERVED*		MOTION_PIC_05		0X03	0X03	0X03
	0x09	MOD_TSEN_05								0X60	0X60	0X60
	0x0A	*RESERVED*			MOTION_OFF 06	*RESERVED*		MOTION_PIC_06		0X03	0X03	0X03
	0x0B	MOD_TSEN_06								0X60	0X60	0X60
	0x0C	*RESERVED*			MOTION_OFF 07	*RESERVED*		MOTION_PIC_07		0X03	0X03	0X03
	0x0D	MOD_TSEN_07								0X60	0X60	0X60
	0x0E	*RESERVED*			MOTION_OFF 08	*RESERVED*		MOTION_PIC_08		0X03	0X03	0X03
	0x0F	MOD_TSEN_08								0X60	0X60	0X60
	0x10	MOD_PSEN_01		MOD_PSEN_02		MOD_PSEN_03		MOD_PSEN_04		0x00	0x00	0x00
	0x11	MOD_PSEN_05		MOD_PSEN_06		MOD_PSEN_07		MOD_PSEN_08		0x00	0x00	0x00
	0x12	H960_CH8	H960_CH7	H960_CH6	H960_CH5	H960_CH4	H960_CH3	H960_CH2	H960_CH1	0x00	0x00	0x00
	0x13	*RESERVED*								0x00	0x00	0x00
	0x14	*RESERVED*								0x00	0xC0	0xC0
	0x15	-								0x00	0x00	0x00
	0x16	-								0x00	0x00	0x00
	0x17	-								0x00	0x00	0x00
	0x18	-								0x00	0x00	0x00
	0x19	-								0x00	0x00	0x00
	0x1A	-								0x00	0x00	0x00
	0x1B	-								0x00	0x00	0x00
	0x1C	-								0x00	0x00	0x00
	0x1D	-								0x00	0x00	0x00
	0x1E	-								0x00	0x00	0x00
	0x1F	-								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0x20	CH1_MOD_01	CH1_MOD_02	CH1_MOD_03	CH1_MOD_04	CH1_MOD_05	CH1_MOD_06	CH1_MOD_07	CH1_MOD_08	0xFF	0xFF	0xFF
	0x21	CH1_MOD_09	CH1_MOD_10	CH1_MOD_11	CH1_MOD_12	CH1_MOD_13	CH1_MOD_14	CH1_MOD_15	CH1_MOD_16	0xFF	0xFF	0xFF
	0x22	CH1_MOD_17	CH1_MOD_18	CH1_MOD_19	CH1_MOD_20	CH1_MOD_21	CH1_MOD_22	CH1_MOD_23	CH1_MOD_24	0xFF	0xFF	0xFF
	0x23	CH1_MOD_25	CH1_MOD_26	CH1_MOD_27	CH1_MOD_28	CH1_MOD_29	CH1_MOD_30	CH1_MOD_31	CH1_MOD_32	0xFF	0xFF	0xFF
	0x24	CH1_MOD_33	CH1_MOD_34	CH1_MOD_35	CH1_MOD_36	CH1_MOD_37	CH1_MOD_38	CH1_MOD_39	CH1_MOD_40	0xFF	0xFF	0xFF
	0x25	CH1_MOD_41	CH1_MOD_42	CH1_MOD_43	CH1_MOD_44	CH1_MOD_45	CH1_MOD_46	CH1_MOD_47	CH1_MOD_48	0xFF	0xFF	0xFF
	0x26	CH1_MOD_49	CH1_MOD_50	CH1_MOD_51	CH1_MOD_52	CH1_MOD_53	CH1_MOD_54	CH1_MOD_55	CH1_MOD_56	0xFF	0xFF	0xFF
	0x27	CH1_MOD_57	CH1_MOD_58	CH1_MOD_59	CH1_MOD_60	CH1_MOD_61	CH1_MOD_62	CH1_MOD_63	CH1_MOD_64	0xFF	0xFF	0xFF
	0x28	CH1_MOD_65	CH1_MOD_66	CH1_MOD_67	CH1_MOD_68	CH1_MOD_69	CH1_MOD_70	CH1_MOD_71	CH1_MOD_72	0xFF	0xFF	0xFF
	0x29	CH1_MOD_73	CH1_MOD_74	CH1_MOD_75	CH1_MOD_76	CH1_MOD_77	CH1_MOD_78	CH1_MOD_79	CH1_MOD_80	0xFF	0xFF	0xFF
	0x2A	CH1_MOD_81	CH1_MOD_82	CH1_MOD_83	CH1_MOD_84	CH1_MOD_85	CH1_MOD_86	CH1_MOD_87	CH1_MOD_88	0xFF	0xFF	0xFF
	0x2B	CH1_MOD_89	CH1_MOD_90	CH1_MOD_91	CH1_MOD_92	CH1_MOD_93	CH1_MOD_94	CH1_MOD_95	CH1_MOD_96	0xFF	0xFF	0xFF
	0x2C	CH1_MOD_97	CH1_MOD_98	CH1_MOD_99	CH1_MOD_100	CH1_MOD_101	CH1_MOD_102	CH1_MOD_103	CH1_MOD_104	0xFF	0xFF	0xFF
	0x2D	CH1_MOD_105	CH1_MOD_106	CH1_MOD_107	CH1_MOD_108	CH1_MOD_109	CH1_MOD_110	CH1_MOD_111	CH1_MOD_112	0xFF	0xFF	0xFF
	0x2E	CH1_MOD_113	CH1_MOD_114	CH1_MOD_115	CH1_MOD_116	CH1_MOD_117	CH1_MOD_118	CH1_MOD_119	CH1_MOD_120	0xFF	0xFF	0xFF
	0x2F	CH1_MOD_121	CH1_MOD_122	CH1_MOD_123	CH1_MOD_124	CH1_MOD_125	CH1_MOD_126	CH1_MOD_127	CH1_MOD_128	0xFF	0xFF	0xFF
	0x30	CH1_MOD_129	CH1_MOD_130	CH1_MOD_131	CH1_MOD_132	CH1_MOD_133	CH1_MOD_134	CH1_MOD_135	CH1_MOD_136	0xFF	0xFF	0xFF
	0x31	CH1_MOD_137	CH1_MOD_138	CH1_MOD_139	CH1_MOD_140	CH1_MOD_141	CH1_MOD_142	CH1_MOD_143	CH1_MOD_144	0xFF	0xFF	0xFF
	0x32	CH1_MOD_145	CH1_MOD_146	CH1_MOD_147	CH1_MOD_148	CH1_MOD_149	CH1_MOD_150	CH1_MOD_151	CH1_MOD_152	0xFF	0xFF	0xFF
	0x33	CH1_MOD_153	CH1_MOD_154	CH1_MOD_155	CH1_MOD_156	CH1_MOD_157	CH1_MOD_158	CH1_MOD_159	CH1_MOD_160	0xFF	0xFF	0xFF
	0x34	CH1_MOD_161	CH1_MOD_162	CH1_MOD_163	CH1_MOD_164	CH1_MOD_165	CH1_MOD_166	CH1_MOD_167	CH1_MOD_168	0xFF	0xFF	0xFF
	0x35	CH1_MOD_169	CH1_MOD_170	CH1_MOD_171	CH1_MOD_172	CH1_MOD_173	CH1_MOD_174	CH1_MOD_175	CH1_MOD_176	0xFF	0xFF	0xFF
	0x36	CH1_MOD_177	CH1_MOD_178	CH1_MOD_179	CH1_MOD_180	CH1_MOD_181	CH1_MOD_182	CH1_MOD_183	CH1_MOD_184	0xFF	0xFF	0xFF
	0x37	CH1_MOD_185	CH1_MOD_186	CH1_MOD_187	CH1_MOD_188	CH1_MOD_189	CH1_MOD_190	CH1_MOD_191	CH1_MOD_192	0xFF	0xFF	0xFF
	0x38	CH2_MOD_01	CH2_MOD_02	CH2_MOD_03	CH2_MOD_04	CH2_MOD_05	CH2_MOD_06	CH2_MOD_07	CH2_MOD_08	0xFF	0xFF	0xFF
	0x39	CH2_MOD_09	CH2_MOD_10	CH2_MOD_11	CH2_MOD_12	CH2_MOD_13	CH2_MOD_14	CH2_MOD_15	CH2_MOD_16	0xFF	0xFF	0xFF
	0x3A	CH2_MOD_17	CH2_MOD_18	CH2_MOD_19	CH2_MOD_20	CH2_MOD_21	CH2_MOD_22	CH2_MOD_23	CH2_MOD_24	0xFF	0xFF	0xFF
	0x3B	CH2_MOD_25	CH2_MOD_26	CH2_MOD_27	CH2_MOD_28	CH2_MOD_29	CH2_MOD_30	CH2_MOD_31	CH2_MOD_32	0xFF	0xFF	0xFF
	0x3C	CH2_MOD_33	CH2_MOD_34	CH2_MOD_35	CH2_MOD_36	CH2_MOD_37	CH2_MOD_38	CH2_MOD_39	CH2_MOD_40	0xFF	0xFF	0xFF
	0x3D	CH2_MOD_41	CH2_MOD_42	CH2_MOD_43	CH2_MOD_44	CH2_MOD_45	CH2_MOD_46	CH2_MOD_47	CH2_MOD_48	0xFF	0xFF	0xFF
	0x3E	CH2_MOD_49	CH2_MOD_50	CH2_MOD_51	CH2_MOD_52	CH2_MOD_53	CH2_MOD_54	CH2_MOD_55	CH2_MOD_56	0xFF	0xFF	0xFF
	0x3F	CH2_MOD_57	CH2_MOD_58	CH2_MOD_59	CH2_MOD_60	CH2_MOD_61	CH2_MOD_62	CH2_MOD_63	CH2_MOD_64	0xFF	0xFF	0xFF

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0x40	CH2_MOD_65	CH2_MOD_66	CH2_MOD_67	CH2_MOD_68	CH2_MOD_69	CH2_MOD_70	CH2_MOD_71	CH2_MOD_72	0xFF	0xFF	0xFF
	0x41	CH2_MOD_73	CH2_MOD_74	CH2_MOD_75	CH2_MOD_76	CH2_MOD_77	CH2_MOD_78	CH2_MOD_79	CH2_MOD_80	0xFF	0xFF	0xFF
	0x42	CH2_MOD_81	CH2_MOD_82	CH2_MOD_83	CH2_MOD_84	CH2_MOD_85	CH2_MOD_86	CH2_MOD_87	CH2_MOD_88	0xFF	0xFF	0xFF
	0x43	CH2_MOD_89	CH2_MOD_90	CH2_MOD_91	CH2_MOD_92	CH2_MOD_93	CH2_MOD_94	CH2_MOD_95	CH2_MOD_96	0xFF	0xFF	0xFF
	0x44	CH2_MOD_97	CH2_MOD_98	CH2_MOD_99	CH2_MOD_100	CH2_MOD_101	CH2_MOD_102	CH2_MOD_103	CH2_MOD_104	0xFF	0xFF	0xFF
	0x45	CH2_MOD_105	CH2_MOD_106	CH2_MOD_107	CH2_MOD_108	CH2_MOD_109	CH2_MOD_110	CH2_MOD_111	CH2_MOD_112	0xFF	0xFF	0xFF
	0x46	CH2_MOD_113	CH2_MOD_114	CH2_MOD_115	CH2_MOD_116	CH2_MOD_117	CH2_MOD_118	CH2_MOD_119	CH2_MOD_120	0xFF	0xFF	0xFF
	0x47	CH2_MOD_121	CH2_MOD_122	CH2_MOD_123	CH2_MOD_124	CH2_MOD_125	CH2_MOD_126	CH2_MOD_127	CH2_MOD_128	0xFF	0xFF	0xFF
	0x48	CH2_MOD_129	CH2_MOD_130	CH2_MOD_131	CH2_MOD_132	CH2_MOD_133	CH2_MOD_134	CH2_MOD_135	CH2_MOD_136	0xFF	0xFF	0xFF
	0x49	CH2_MOD_137	CH2_MOD_138	CH2_MOD_139	CH2_MOD_140	CH2_MOD_141	CH2_MOD_142	CH2_MOD_143	CH2_MOD_144	0xFF	0xFF	0xFF
	0x4A	CH2_MOD_145	CH2_MOD_146	CH2_MOD_147	CH2_MOD_148	CH2_MOD_149	CH2_MOD_150	CH2_MOD_151	CH2_MOD_152	0xFF	0xFF	0xFF
	0x4B	CH2_MOD_153	CH2_MOD_154	CH2_MOD_155	CH2_MOD_156	CH2_MOD_157	CH2_MOD_158	CH2_MOD_159	CH2_MOD_160	0xFF	0xFF	0xFF
	0x4C	CH2_MOD_161	CH2_MOD_162	CH2_MOD_163	CH2_MOD_164	CH2_MOD_165	CH2_MOD_166	CH2_MOD_167	CH2_MOD_168	0xFF	0xFF	0xFF
	0x4D	CH2_MOD_169	CH2_MOD_170	CH2_MOD_171	CH2_MOD_172	CH2_MOD_173	CH2_MOD_174	CH2_MOD_175	CH2_MOD_176	0xFF	0xFF	0xFF
	0x4E	CH2_MOD_177	CH2_MOD_178	CH2_MOD_179	CH2_MOD_180	CH2_MOD_181	CH2_MOD_182	CH2_MOD_183	CH2_MOD_184	0xFF	0xFF	0xFF
	0x4F	CH2_MOD_185	CH2_MOD_186	CH2_MOD_187	CH2_MOD_188	CH2_MOD_189	CH2_MOD_190	CH2_MOD_191	CH2_MOD_192	0xFF	0xFF	0xFF
	0x50	CH3_MOD_01	CH3_MOD_02	CH3_MOD_03	CH3_MOD_04	CH3_MOD_05	CH3_MOD_06	CH3_MOD_07	CH3_MOD_08	0xFF	0xFF	0xFF
	0x51	CH3_MOD_09	CH3_MOD_10	CH3_MOD_11	CH3_MOD_12	CH3_MOD_13	CH3_MOD_14	CH3_MOD_15	CH3_MOD_16	0xFF	0xFF	0xFF
	0x52	CH3_MOD_17	CH3_MOD_18	CH3_MOD_19	CH3_MOD_20	CH3_MOD_21	CH3_MOD_22	CH3_MOD_23	CH3_MOD_24	0xFF	0xFF	0xFF
	0x53	CH3_MOD_25	CH3_MOD_26	CH3_MOD_27	CH3_MOD_28	CH3_MOD_29	CH3_MOD_30	CH3_MOD_31	CH3_MOD_32	0xFF	0xFF	0xFF
	0x54	CH3_MOD_33	CH3_MOD_34	CH3_MOD_35	CH3_MOD_36	CH3_MOD_37	CH3_MOD_38	CH3_MOD_39	CH3_MOD_40	0xFF	0xFF	0xFF
	0x55	CH3_MOD_41	CH3_MOD_42	CH3_MOD_43	CH3_MOD_44	CH3_MOD_45	CH3_MOD_46	CH3_MOD_47	CH3_MOD_48	0xFF	0xFF	0xFF
	0x56	CH3_MOD_49	CH3_MOD_50	CH3_MOD_51	CH3_MOD_52	CH3_MOD_53	CH3_MOD_54	CH3_MOD_55	CH3_MOD_56	0xFF	0xFF	0xFF
	0x57	CH3_MOD_57	CH3_MOD_58	CH3_MOD_59	CH3_MOD_60	CH3_MOD_61	CH3_MOD_62	CH3_MOD_63	CH3_MOD_64	0xFF	0xFF	0xFF
	0x58	CH3_MOD_65	CH3_MOD_66	CH3_MOD_67	CH3_MOD_68	CH3_MOD_69	CH3_MOD_70	CH3_MOD_71	CH3_MOD_72	0xFF	0xFF	0xFF
	0x59	CH3_MOD_73	CH3_MOD_74	CH3_MOD_75	CH3_MOD_76	CH3_MOD_77	CH3_MOD_78	CH3_MOD_79	CH3_MOD_80	0xFF	0xFF	0xFF
	0x5A	CH3_MOD_81	CH3_MOD_82	CH3_MOD_83	CH3_MOD_84	CH3_MOD_85	CH3_MOD_86	CH3_MOD_87	CH3_MOD_88	0xFF	0xFF	0xFF
	0x5B	CH3_MOD_89	CH3_MOD_90	CH3_MOD_91	CH3_MOD_92	CH3_MOD_93	CH3_MOD_94	CH3_MOD_95	CH3_MOD_96	0xFF	0xFF	0xFF
	0x5C	CH3_MOD_97	CH3_MOD_98	CH3_MOD_99	CH3_MOD_100	CH3_MOD_101	CH3_MOD_102	CH3_MOD_103	CH3_MOD_104	0xFF	0xFF	0xFF
	0x5D	CH3_MOD_105	CH3_MOD_106	CH3_MOD_107	CH3_MOD_108	CH3_MOD_109	CH3_MOD_110	CH3_MOD_111	CH3_MOD_112	0xFF	0xFF	0xFF
	0x5E	CH3_MOD_113	CH3_MOD_114	CH3_MOD_115	CH3_MOD_116	CH3_MOD_117	CH3_MOD_118	CH3_MOD_119	CH3_MOD_120	0xFF	0xFF	0xFF
	0x5F	CH3_MOD_121	CH3_MOD_122	CH3_MOD_123	CH3_MOD_124	CH3_MOD_125	CH3_MOD_126	CH3_MOD_127	CH3_MOD_128	0xFF	0xFF	0xFF

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0x60	CH3_MOD_129	CH3_MOD_130	CH3_MOD_131	CH3_MOD_132	CH3_MOD_133	CH3_MOD_134	CH3_MOD_135	CH3_MOD_136	0xFF	0xFF	0xFF
	0x61	CH3_MOD_137	CH3_MOD_138	CH3_MOD_139	CH3_MOD_140	CH3_MOD_141	CH3_MOD_142	CH3_MOD_143	CH3_MOD_144	0xFF	0xFF	0xFF
	0x62	CH3_MOD_145	CH3_MOD_146	CH3_MOD_147	CH3_MOD_148	CH3_MOD_149	CH3_MOD_150	CH3_MOD_151	CH3_MOD_152	0xFF	0xFF	0xFF
	0x63	CH3_MOD_153	CH3_MOD_154	CH3_MOD_155	CH3_MOD_156	CH3_MOD_157	CH3_MOD_158	CH3_MOD_159	CH3_MOD_160	0xFF	0xFF	0xFF
	0x64	CH3_MOD_161	CH3_MOD_162	CH3_MOD_163	CH3_MOD_164	CH3_MOD_165	CH3_MOD_166	CH3_MOD_167	CH3_MOD_168	0xFF	0xFF	0xFF
	0x65	CH3_MOD_169	CH3_MOD_170	CH3_MOD_171	CH3_MOD_172	CH3_MOD_173	CH3_MOD_174	CH3_MOD_175	CH3_MOD_176	0xFF	0xFF	0xFF
	0x66	CH3_MOD_177	CH3_MOD_178	CH3_MOD_179	CH3_MOD_180	CH3_MOD_181	CH3_MOD_182	CH3_MOD_183	CH3_MOD_184	0xFF	0xFF	0xFF
	0x67	CH3_MOD_185	CH3_MOD_186	CH3_MOD_187	CH3_MOD_188	CH3_MOD_189	CH3_MOD_190	CH3_MOD_191	CH3_MOD_192	0xFF	0xFF	0xFF
	0x68	CH4_MOD_01	CH4_MOD_02	CH4_MOD_03	CH4_MOD_04	CH4_MOD_05	CH4_MOD_06	CH4_MOD_07	CH4_MOD_08	0xFF	0xFF	0xFF
	0x69	CH4_MOD_09	CH4_MOD_10	CH4_MOD_11	CH4_MOD_12	CH4_MOD_13	CH4_MOD_14	CH4_MOD_15	CH4_MOD_16	0xFF	0xFF	0xFF
	0x6A	CH4_MOD_17	CH4_MOD_18	CH4_MOD_19	CH4_MOD_20	CH4_MOD_21	CH4_MOD_22	CH4_MOD_23	CH4_MOD_24	0xFF	0xFF	0xFF
	0x6B	CH4_MOD_25	CH4_MOD_26	CH4_MOD_27	CH4_MOD_28	CH4_MOD_29	CH4_MOD_30	CH4_MOD_31	CH4_MOD_32	0xFF	0xFF	0xFF
	0x6C	CH4_MOD_33	CH4_MOD_34	CH4_MOD_35	CH4_MOD_36	CH4_MOD_37	CH4_MOD_38	CH4_MOD_39	CH4_MOD_40	0xFF	0xFF	0xFF
	0x6D	CH4_MOD_41	CH4_MOD_42	CH4_MOD_43	CH4_MOD_44	CH4_MOD_45	CH4_MOD_46	CH4_MOD_47	CH4_MOD_48	0xFF	0xFF	0xFF
	0x6E	CH4_MOD_49	CH4_MOD_50	CH4_MOD_51	CH4_MOD_52	CH4_MOD_53	CH4_MOD_54	CH4_MOD_55	CH4_MOD_56	0xFF	0xFF	0xFF
	0x6F	CH4_MOD_57	CH4_MOD_58	CH4_MOD_59	CH4_MOD_60	CH4_MOD_61	CH4_MOD_62	CH4_MOD_63	CH4_MOD_64	0xFF	0xFF	0xFF
	0x70	CH4_MOD_65	CH4_MOD_66	CH4_MOD_67	CH4_MOD_68	CH4_MOD_69	CH4_MOD_70	CH4_MOD_71	CH4_MOD_72	0xFF	0xFF	0xFF
	0x71	CH4_MOD_73	CH4_MOD_74	CH4_MOD_75	CH4_MOD_76	CH4_MOD_77	CH4_MOD_78	CH4_MOD_79	CH4_MOD_80	0xFF	0xFF	0xFF
	0x72	CH4_MOD_81	CH4_MOD_82	CH4_MOD_83	CH4_MOD_84	CH4_MOD_85	CH4_MOD_86	CH4_MOD_87	CH4_MOD_88	0xFF	0xFF	0xFF
	0x73	CH4_MOD_89	CH4_MOD_90	CH4_MOD_91	CH4_MOD_92	CH4_MOD_93	CH4_MOD_94	CH4_MOD_95	CH4_MOD_96	0xFF	0xFF	0xFF
	0x74	CH4_MOD_97	CH4_MOD_98	CH4_MOD_99	CH4_MOD_100	CH4_MOD_101	CH4_MOD_102	CH4_MOD_103	CH4_MOD_104	0xFF	0xFF	0xFF
	0x75	CH4_MOD_105	CH4_MOD_106	CH4_MOD_107	CH4_MOD_108	CH4_MOD_109	CH4_MOD_110	CH4_MOD_111	CH4_MOD_112	0xFF	0xFF	0xFF
	0x76	CH4_MOD_113	CH4_MOD_114	CH4_MOD_115	CH4_MOD_116	CH4_MOD_117	CH4_MOD_118	CH4_MOD_119	CH4_MOD_120	0xFF	0xFF	0xFF
	0x77	CH4_MOD_121	CH4_MOD_122	CH4_MOD_123	CH4_MOD_124	CH4_MOD_125	CH4_MOD_126	CH4_MOD_127	CH4_MOD_128	0xFF	0xFF	0xFF
	0x78	CH4_MOD_129	CH4_MOD_130	CH4_MOD_131	CH4_MOD_132	CH4_MOD_133	CH4_MOD_134	CH4_MOD_135	CH4_MOD_136	0xFF	0xFF	0xFF
	0x79	CH4_MOD_137	CH4_MOD_138	CH4_MOD_139	CH4_MOD_140	CH4_MOD_141	CH4_MOD_142	CH4_MOD_143	CH4_MOD_144	0xFF	0xFF	0xFF
	0x7A	CH4_MOD_145	CH4_MOD_146	CH4_MOD_147	CH4_MOD_148	CH4_MOD_149	CH4_MOD_150	CH4_MOD_151	CH4_MOD_152	0xFF	0xFF	0xFF
	0x7B	CH4_MOD_153	CH4_MOD_154	CH4_MOD_155	CH4_MOD_156	CH4_MOD_157	CH4_MOD_158	CH4_MOD_159	CH4_MOD_160	0xFF	0xFF	0xFF
	0x7C	CH4_MOD_161	CH4_MOD_162	CH4_MOD_163	CH4_MOD_164	CH4_MOD_165	CH4_MOD_166	CH4_MOD_167	CH4_MOD_168	0xFF	0xFF	0xFF
	0x7D	CH4_MOD_169	CH4_MOD_170	CH4_MOD_171	CH4_MOD_172	CH4_MOD_173	CH4_MOD_174	CH4_MOD_175	CH4_MOD_176	0xFF	0xFF	0xFF
	0x7E	CH4_MOD_177	CH4_MOD_178	CH4_MOD_179	CH4_MOD_180	CH4_MOD_181	CH4_MOD_182	CH4_MOD_183	CH4_MOD_184	0xFF	0xFF	0xFF
	0x7F	CH4_MOD_185	CH4_MOD_186	CH4_MOD_187	CH4_MOD_188	CH4_MOD_189	CH4_MOD_190	CH4_MOD_191	CH4_MOD_192	0xFF	0xFF	0xFF

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0x80	CH5_MOD_01	CH5_MOD_02	CH5_MOD_03	CH5_MOD_04	CH5_MOD_05	CH5_MOD_06	CH5_MOD_07	CH5_MOD_08	0xFF	0xFF	0xFF
	0x81	CH5_MOD_09	CH5_MOD_10	CH5_MOD_11	CH5_MOD_12	CH5_MOD_13	CH5_MOD_14	CH5_MOD_15	CH5_MOD_16	0xFF	0xFF	0xFF
	0x82	CH5_MOD_17	CH5_MOD_18	CH5_MOD_19	CH5_MOD_20	CH5_MOD_21	CH5_MOD_22	CH5_MOD_23	CH5_MOD_24	0xFF	0xFF	0xFF
	0x83	CH5_MOD_25	CH5_MOD_26	CH5_MOD_27	CH5_MOD_28	CH5_MOD_29	CH5_MOD_30	CH5_MOD_31	CH5_MOD_32	0xFF	0xFF	0xFF
	0x84	CH5_MOD_33	CH5_MOD_34	CH5_MOD_35	CH5_MOD_36	CH5_MOD_37	CH5_MOD_38	CH5_MOD_39	CH5_MOD_40	0xFF	0xFF	0xFF
	0x85	CH5_MOD_41	CH5_MOD_42	CH5_MOD_43	CH5_MOD_44	CH5_MOD_45	CH5_MOD_46	CH5_MOD_47	CH5_MOD_48	0xFF	0xFF	0xFF
	0x86	CH5_MOD_49	CH5_MOD_50	CH5_MOD_51	CH5_MOD_52	CH5_MOD_53	CH5_MOD_54	CH5_MOD_55	CH5_MOD_56	0xFF	0xFF	0xFF
	0x87	CH5_MOD_57	CH5_MOD_58	CH5_MOD_59	CH5_MOD_60	CH5_MOD_61	CH5_MOD_62	CH5_MOD_63	CH5_MOD_64	0xFF	0xFF	0xFF
	0x88	CH5_MOD_65	CH5_MOD_66	CH5_MOD_67	CH5_MOD_68	CH5_MOD_69	CH5_MOD_70	CH5_MOD_71	CH5_MOD_72	0xFF	0xFF	0xFF
	0x89	CH5_MOD_73	CH5_MOD_74	CH5_MOD_75	CH5_MOD_76	CH5_MOD_77	CH5_MOD_78	CH5_MOD_79	CH5_MOD_80	0xFF	0xFF	0xFF
	0x8A	CH5_MOD_81	CH5_MOD_82	CH5_MOD_83	CH5_MOD_84	CH5_MOD_85	CH5_MOD_86	CH5_MOD_87	CH5_MOD_88	0xFF	0xFF	0xFF
	0x8B	CH5_MOD_89	CH5_MOD_90	CH5_MOD_91	CH5_MOD_92	CH5_MOD_93	CH5_MOD_94	CH5_MOD_95	CH5_MOD_96	0xFF	0xFF	0xFF
	0x8C	CH5_MOD_97	CH5_MOD_98	CH5_MOD_99	CH5_MOD_100	CH5_MOD_101	CH5_MOD_102	CH5_MOD_103	CH5_MOD_104	0xFF	0xFF	0xFF
	0x8D	CH5_MOD_105	CH5_MOD_106	CH5_MOD_107	CH5_MOD_108	CH5_MOD_109	CH5_MOD_110	CH5_MOD_111	CH5_MOD_112	0xFF	0xFF	0xFF
	0x8E	CH5_MOD_113	CH5_MOD_114	CH5_MOD_115	CH5_MOD_116	CH5_MOD_117	CH5_MOD_118	CH5_MOD_119	CH5_MOD_120	0xFF	0xFF	0xFF
	0x8F	CH5_MOD_121	CH5_MOD_122	CH5_MOD_123	CH5_MOD_124	CH5_MOD_125	CH5_MOD_126	CH5_MOD_127	CH5_MOD_128	0xFF	0xFF	0xFF
	0x90	CH5_MOD_129	CH5_MOD_130	CH5_MOD_131	CH5_MOD_132	CH5_MOD_133	CH5_MOD_134	CH5_MOD_135	CH5_MOD_136	0xFF	0xFF	0xFF
	0x91	CH5_MOD_137	CH5_MOD_138	CH5_MOD_139	CH5_MOD_140	CH5_MOD_141	CH5_MOD_142	CH5_MOD_143	CH5_MOD_144	0xFF	0xFF	0xFF
	0x92	CH5_MOD_145	CH5_MOD_146	CH5_MOD_147	CH5_MOD_148	CH5_MOD_149	CH5_MOD_150	CH5_MOD_151	CH5_MOD_152	0xFF	0xFF	0xFF
	0x93	CH5_MOD_153	CH5_MOD_154	CH5_MOD_155	CH5_MOD_156	CH5_MOD_157	CH5_MOD_158	CH5_MOD_159	CH5_MOD_160	0xFF	0xFF	0xFF
	0x94	CH5_MOD_161	CH5_MOD_162	CH5_MOD_163	CH5_MOD_164	CH5_MOD_165	CH5_MOD_166	CH5_MOD_167	CH5_MOD_168	0xFF	0xFF	0xFF
	0x95	CH5_MOD_169	CH5_MOD_170	CH5_MOD_171	CH5_MOD_172	CH5_MOD_173	CH5_MOD_174	CH5_MOD_175	CH5_MOD_176	0xFF	0xFF	0xFF
	0x96	CH5_MOD_177	CH5_MOD_178	CH5_MOD_179	CH5_MOD_180	CH5_MOD_181	CH5_MOD_182	CH5_MOD_183	CH5_MOD_184	0xFF	0xFF	0xFF
	0x97	CH5_MOD_185	CH5_MOD_186	CH5_MOD_187	CH5_MOD_188	CH5_MOD_189	CH5_MOD_190	CH5_MOD_191	CH5_MOD_192	0xFF	0xFF	0xFF
	0x98	CH6_MOD_01	CH6_MOD_02	CH6_MOD_03	CH6_MOD_04	CH6_MOD_05	CH6_MOD_06	CH6_MOD_07	CH6_MOD_08	0xFF	0xFF	0xFF
	0x99	CH6_MOD_09	CH6_MOD_10	CH6_MOD_11	CH6_MOD_12	CH6_MOD_13	CH6_MOD_14	CH6_MOD_15	CH6_MOD_16	0xFF	0xFF	0xFF
	0x9A	CH6_MOD_17	CH6_MOD_18	CH6_MOD_19	CH6_MOD_20	CH6_MOD_21	CH6_MOD_22	CH6_MOD_23	CH6_MOD_24	0xFF	0xFF	0xFF
	0x9B	CH6_MOD_25	CH6_MOD_26	CH6_MOD_27	CH6_MOD_28	CH6_MOD_29	CH6_MOD_30	CH6_MOD_31	CH6_MOD_32	0xFF	0xFF	0xFF
	0x9C	CH6_MOD_33	CH6_MOD_34	CH6_MOD_35	CH6_MOD_36	CH6_MOD_37	CH6_MOD_38	CH6_MOD_39	CH6_MOD_40	0xFF	0xFF	0xFF
	0x9D	CH6_MOD_41	CH6_MOD_42	CH6_MOD_43	CH6_MOD_44	CH6_MOD_45	CH6_MOD_46	CH6_MOD_47	CH6_MOD_48	0xFF	0xFF	0xFF
	0x9E	CH6_MOD_49	CH6_MOD_50	CH6_MOD_51	CH6_MOD_52	CH6_MOD_53	CH6_MOD_54	CH6_MOD_55	CH6_MOD_56	0xFF	0xFF	0xFF
	0x9F	CH6_MOD_57	CH6_MOD_58	CH6_MOD_59	CH6_MOD_60	CH6_MOD_61	CH6_MOD_62	CH6_MOD_63	CH6_MOD_64	0xFF	0xFF	0xFF

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0xA0	CH6_MOD_65	CH6_MOD_66	CH6_MOD_67	CH6_MOD_68	CH6_MOD_69	CH6_MOD_70	CH6_MOD_71	CH6_MOD_72	0xFF	0xFF	0xFF
	0xA1	CH6_MOD_73	CH6_MOD_74	CH6_MOD_75	CH6_MOD_76	CH6_MOD_77	CH6_MOD_78	CH6_MOD_79	CH6_MOD_80	0xFF	0xFF	0xFF
	0xA2	CH6_MOD_81	CH6_MOD_82	CH6_MOD_83	CH6_MOD_84	CH6_MOD_85	CH6_MOD_86	CH6_MOD_87	CH6_MOD_88	0xFF	0xFF	0xFF
	0xA3	CH6_MOD_89	CH6_MOD_90	CH6_MOD_91	CH6_MOD_92	CH6_MOD_93	CH6_MOD_94	CH6_MOD_95	CH6_MOD_96	0xFF	0xFF	0xFF
	0xA4	CH6_MOD_97	CH6_MOD_98	CH6_MOD_99	CH6_MOD_100	CH6_MOD_101	CH6_MOD_102	CH6_MOD_103	CH6_MOD_104	0xFF	0xFF	0xFF
	0xA5	CH6_MOD_105	CH6_MOD_106	CH6_MOD_107	CH6_MOD_108	CH6_MOD_109	CH6_MOD_110	CH6_MOD_111	CH6_MOD_112	0xFF	0xFF	0xFF
	0xA6	CH6_MOD_113	CH6_MOD_114	CH6_MOD_115	CH6_MOD_116	CH6_MOD_117	CH6_MOD_118	CH6_MOD_119	CH6_MOD_120	0xFF	0xFF	0xFF
	0xA7	CH6_MOD_121	CH6_MOD_122	CH6_MOD_123	CH6_MOD_124	CH6_MOD_125	CH6_MOD_126	CH6_MOD_127	CH6_MOD_128	0xFF	0xFF	0xFF
	0xA8	CH6_MOD_129	CH6_MOD_130	CH6_MOD_131	CH6_MOD_132	CH6_MOD_133	CH6_MOD_134	CH6_MOD_135	CH6_MOD_136	0xFF	0xFF	0xFF
	0xA9	CH6_MOD_137	CH6_MOD_138	CH6_MOD_139	CH6_MOD_140	CH6_MOD_141	CH6_MOD_142	CH6_MOD_143	CH6_MOD_144	0xFF	0xFF	0xFF
	0xAA	CH6_MOD_145	CH6_MOD_146	CH6_MOD_147	CH6_MOD_148	CH6_MOD_149	CH6_MOD_150	CH6_MOD_151	CH6_MOD_152	0xFF	0xFF	0xFF
	0xAB	CH6_MOD_153	CH6_MOD_154	CH6_MOD_155	CH6_MOD_156	CH6_MOD_157	CH6_MOD_158	CH6_MOD_159	CH6_MOD_160	0xFF	0xFF	0xFF
	0xAC	CH6_MOD_161	CH6_MOD_162	CH6_MOD_163	CH6_MOD_164	CH6_MOD_165	CH6_MOD_166	CH6_MOD_167	CH6_MOD_168	0xFF	0xFF	0xFF
	0xAD	CH6_MOD_169	CH6_MOD_170	CH6_MOD_171	CH6_MOD_172	CH6_MOD_173	CH6_MOD_174	CH6_MOD_175	CH6_MOD_176	0xFF	0xFF	0xFF
	0xAE	CH6_MOD_177	CH6_MOD_178	CH6_MOD_179	CH6_MOD_180	CH6_MOD_181	CH6_MOD_182	CH6_MOD_183	CH6_MOD_184	0xFF	0xFF	0xFF
	0xAF	CH6_MOD_185	CH6_MOD_186	CH6_MOD_187	CH6_MOD_188	CH6_MOD_189	CH6_MOD_190	CH6_MOD_191	CH6_MOD_192	0xFF	0xFF	0xFF
	0xB0	CH7_MOD_01	CH7_MOD_02	CH7_MOD_03	CH7_MOD_04	CH7_MOD_05	CH7_MOD_06	CH7_MOD_07	CH7_MOD_08	0xFF	0xFF	0xFF
	0xB1	CH7_MOD_09	CH7_MOD_10	CH7_MOD_11	CH7_MOD_12	CH7_MOD_13	CH7_MOD_14	CH7_MOD_15	CH7_MOD_16	0xFF	0xFF	0xFF
	0xB2	CH7_MOD_17	CH7_MOD_18	CH7_MOD_19	CH7_MOD_20	CH7_MOD_21	CH7_MOD_22	CH7_MOD_23	CH7_MOD_24	0xFF	0xFF	0xFF
	0xB3	CH7_MOD_25	CH7_MOD_26	CH7_MOD_27	CH7_MOD_28	CH7_MOD_29	CH7_MOD_30	CH7_MOD_31	CH7_MOD_32	0xFF	0xFF	0xFF
	0xB4	CH7_MOD_33	CH7_MOD_34	CH7_MOD_35	CH7_MOD_36	CH7_MOD_37	CH7_MOD_38	CH7_MOD_39	CH7_MOD_40	0xFF	0xFF	0xFF
	0xB5	CH7_MOD_41	CH7_MOD_42	CH7_MOD_43	CH7_MOD_44	CH7_MOD_45	CH7_MOD_46	CH7_MOD_47	CH7_MOD_48	0xFF	0xFF	0xFF
	0xB6	CH7_MOD_49	CH7_MOD_50	CH7_MOD_51	CH7_MOD_52	CH7_MOD_53	CH7_MOD_54	CH7_MOD_55	CH7_MOD_56	0xFF	0xFF	0xFF
	0xB7	CH7_MOD_57	CH7_MOD_58	CH7_MOD_59	CH7_MOD_60	CH7_MOD_61	CH7_MOD_62	CH7_MOD_63	CH7_MOD_64	0xFF	0xFF	0xFF
	0xB8	CH7_MOD_65	CH7_MOD_66	CH7_MOD_67	CH7_MOD_68	CH7_MOD_69	CH7_MOD_70	CH7_MOD_71	CH7_MOD_72	0xFF	0xFF	0xFF
	0xB9	CH7_MOD_73	CH7_MOD_74	CH7_MOD_75	CH7_MOD_76	CH7_MOD_77	CH7_MOD_78	CH7_MOD_79	CH7_MOD_80	0xFF	0xFF	0xFF
	0xBA	CH7_MOD_81	CH7_MOD_82	CH7_MOD_83	CH7_MOD_84	CH7_MOD_85	CH7_MOD_86	CH7_MOD_87	CH7_MOD_88	0xFF	0xFF	0xFF
	0xBB	CH7_MOD_89	CH7_MOD_90	CH7_MOD_91	CH7_MOD_92	CH7_MOD_93	CH7_MOD_94	CH7_MOD_95	CH7_MOD_96	0xFF	0xFF	0xFF
	0xBC	CH7_MOD_97	CH7_MOD_98	CH7_MOD_99	CH7_MOD_100	CH7_MOD_101	CH7_MOD_102	CH7_MOD_103	CH7_MOD_104	0xFF	0xFF	0xFF
	0xBD	CH7_MOD_105	CH7_MOD_106	CH7_MOD_107	CH7_MOD_108	CH7_MOD_109	CH7_MOD_110	CH7_MOD_111	CH7_MOD_112	0xFF	0xFF	0xFF
	0xBE	CH7_MOD_113	CH7_MOD_114	CH7_MOD_115	CH7_MOD_116	CH7_MOD_117	CH7_MOD_118	CH7_MOD_119	CH7_MOD_120	0xFF	0xFF	0xFF
	0xBF	CH7_MOD_121	CH7_MOD_122	CH7_MOD_123	CH7_MOD_124	CH7_MOD_125	CH7_MOD_126	CH7_MOD_127	CH7_MOD_128	0xFF	0xFF	0xFF

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0xC0	CH7_MOD_129	CH7_MOD_130	CH7_MOD_131	CH7_MOD_132	CH7_MOD_133	CH7_MOD_134	CH7_MOD_135	CH7_MOD_136	0xFF	0xFF	0xFF
	0xC1	CH7_MOD_137	CH7_MOD_138	CH7_MOD_139	CH7_MOD_140	CH7_MOD_141	CH7_MOD_142	CH7_MOD_143	CH7_MOD_144	0xFF	0xFF	0xFF
	0xC2	CH7_MOD_145	CH7_MOD_146	CH7_MOD_147	CH7_MOD_148	CH7_MOD_149	CH7_MOD_150	CH7_MOD_151	CH7_MOD_152	0xFF	0xFF	0xFF
	0xC3	CH7_MOD_153	CH7_MOD_154	CH7_MOD_155	CH7_MOD_156	CH7_MOD_157	CH7_MOD_158	CH7_MOD_159	CH7_MOD_160	0xFF	0xFF	0xFF
	0xC4	CH7_MOD_161	CH7_MOD_162	CH7_MOD_163	CH7_MOD_164	CH7_MOD_165	CH7_MOD_166	CH7_MOD_167	CH7_MOD_168	0xFF	0xFF	0xFF
	0xC5	CH7_MOD_169	CH7_MOD_170	CH7_MOD_171	CH7_MOD_172	CH7_MOD_173	CH7_MOD_174	CH7_MOD_175	CH7_MOD_176	0xFF	0xFF	0xFF
	0xC6	CH7_MOD_177	CH7_MOD_178	CH7_MOD_179	CH7_MOD_180	CH7_MOD_181	CH7_MOD_182	CH7_MOD_183	CH7_MOD_184	0xFF	0xFF	0xFF
	0xC7	CH7_MOD_185	CH7_MOD_186	CH7_MOD_187	CH7_MOD_188	CH7_MOD_189	CH7_MOD_190	CH7_MOD_191	CH7_MOD_192	0xFF	0xFF	0xFF
	0xC8	CH8_MOD_01	CH8_MOD_02	CH8_MOD_03	CH8_MOD_04	CH8_MOD_05	CH8_MOD_06	CH8_MOD_07	CH8_MOD_08	0xFF	0xFF	0xFF
	0xC9	CH8_MOD_09	CH8_MOD_10	CH8_MOD_11	CH8_MOD_12	CH8_MOD_13	CH8_MOD_14	CH8_MOD_15	CH8_MOD_16	0xFF	0xFF	0xFF
	0xCA	CH8_MOD_17	CH8_MOD_18	CH8_MOD_19	CH8_MOD_20	CH8_MOD_21	CH8_MOD_22	CH8_MOD_23	CH8_MOD_24	0xFF	0xFF	0xFF
	0xCB	CH8_MOD_25	CH8_MOD_26	CH8_MOD_27	CH8_MOD_28	CH8_MOD_29	CH8_MOD_30	CH8_MOD_31	CH8_MOD_32	0xFF	0xFF	0xFF
	0xCC	CH8_MOD_33	CH8_MOD_34	CH8_MOD_35	CH8_MOD_36	CH8_MOD_37	CH8_MOD_38	CH8_MOD_39	CH8_MOD_40	0xFF	0xFF	0xFF
	0xCD	CH8_MOD_41	CH8_MOD_42	CH8_MOD_43	CH8_MOD_44	CH8_MOD_45	CH8_MOD_46	CH8_MOD_47	CH8_MOD_48	0xFF	0xFF	0xFF
	0xCE	CH8_MOD_49	CH8_MOD_50	CH8_MOD_51	CH8_MOD_52	CH8_MOD_53	CH8_MOD_54	CH8_MOD_55	CH8_MOD_56	0xFF	0xFF	0xFF
	0xCF	CH8_MOD_57	CH8_MOD_58	CH8_MOD_59	CH8_MOD_60	CH8_MOD_61	CH8_MOD_62	CH8_MOD_63	CH8_MOD_64	0xFF	0xFF	0xFF
	0xD0	CH8_MOD_65	CH8_MOD_66	CH8_MOD_67	CH8_MOD_68	CH8_MOD_69	CH8_MOD_70	CH8_MOD_71	CH8_MOD_72	0xFF	0xFF	0xFF
	0xD1	CH8_MOD_73	CH8_MOD_74	CH8_MOD_75	CH8_MOD_76	CH8_MOD_77	CH8_MOD_78	CH8_MOD_79	CH8_MOD_80	0xFF	0xFF	0xFF
	0xD2	CH8_MOD_81	CH8_MOD_82	CH8_MOD_83	CH8_MOD_84	CH8_MOD_85	CH8_MOD_86	CH8_MOD_87	CH8_MOD_88	0xFF	0xFF	0xFF
	0xD3	CH8_MOD_89	CH8_MOD_90	CH8_MOD_91	CH8_MOD_92	CH8_MOD_93	CH8_MOD_94	CH8_MOD_95	CH8_MOD_96	0xFF	0xFF	0xFF
	0xD4	CH8_MOD_97	CH8_MOD_98	CH8_MOD_99	CH8_MOD_100	CH8_MOD_101	CH8_MOD_102	CH8_MOD_103	CH8_MOD_104	0xFF	0xFF	0xFF
	0xD5	CH8_MOD_105	CH8_MOD_106	CH8_MOD_107	CH8_MOD_108	CH8_MOD_109	CH8_MOD_110	CH8_MOD_111	CH8_MOD_112	0xFF	0xFF	0xFF
	0xD6	CH8_MOD_113	CH8_MOD_114	CH8_MOD_115	CH8_MOD_116	CH8_MOD_117	CH8_MOD_118	CH8_MOD_119	CH8_MOD_120	0xFF	0xFF	0xFF
	0xD7	CH8_MOD_121	CH8_MOD_122	CH8_MOD_123	CH8_MOD_124	CH8_MOD_125	CH8_MOD_126	CH8_MOD_127	CH8_MOD_128	0xFF	0xFF	0xFF
	0xD8	CH8_MOD_129	CH8_MOD_130	CH8_MOD_131	CH8_MOD_132	CH8_MOD_133	CH8_MOD_134	CH8_MOD_135	CH8_MOD_136	0xFF	0xFF	0xFF
	0xD9	CH8_MOD_137	CH8_MOD_138	CH8_MOD_139	CH8_MOD_140	CH8_MOD_141	CH8_MOD_142	CH8_MOD_143	CH8_MOD_144	0xFF	0xFF	0xFF
	0xDA	CH8_MOD_145	CH8_MOD_146	CH8_MOD_147	CH8_MOD_148	CH8_MOD_149	CH8_MOD_150	CH8_MOD_151	CH8_MOD_152	0xFF	0xFF	0xFF
	0xDB	CH8_MOD_153	CH8_MOD_154	CH8_MOD_155	CH8_MOD_156	CH8_MOD_157	CH8_MOD_158	CH8_MOD_159	CH8_MOD_160	0xFF	0xFF	0xFF
	0xDC	CH8_MOD_161	CH8_MOD_162	CH8_MOD_163	CH8_MOD_164	CH8_MOD_165	CH8_MOD_166	CH8_MOD_167	CH8_MOD_168	0xFF	0xFF	0xFF
	0xDD	CH8_MOD_169	CH8_MOD_170	CH8_MOD_171	CH8_MOD_172	CH8_MOD_173	CH8_MOD_174	CH8_MOD_175	CH8_MOD_176	0xFF	0xFF	0xFF
	0xDE	CH8_MOD_177	CH8_MOD_178	CH8_MOD_179	CH8_MOD_180	CH8_MOD_181	CH8_MOD_182	CH8_MOD_183	CH8_MOD_184	0xFF	0xFF	0xFF
	0xDF	CH8_MOD_185	CH8_MOD_186	CH8_MOD_187	CH8_MOD_188	CH8_MOD_189	CH8_MOD_190	CH8_MOD_191	CH8_MOD_192	0xFF	0xFF	0xFF

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK2	0xE0	*RESERVED*								0x00	0x00	0x00
	0xE1	*RESERVED*								0x00	0x00	0x00
	0xE2	*RESERVED*								0x00	0x00	0x00
	0xE3	*RESERVED*								0x00	0x00	0x00
	0xE4	*RESERVED*								0x00	0x00	0x00
	0xE5	*RESERVED*								0x00	0x00	0x00
	0xE6	*RESERVED*								0x00	0x00	0x00
	0xE7	*RESERVED*								0x00	0x00	0x00
	0xE8	*RESERVED*								0x00	0x00	0x00
	0xE9	*RESERVED*								0x00	0x00	0x00
	0xEA	*RESERVED*								0x00	0x00	0x00
	0xEB	*RESERVED*								0x00	0x00	0x00
	0xEC	*RESERVED*								0x00	0x00	0x00
	0xED	*RESERVED*								0x00	0x00	0x00
	0xEE	*RESERVED*								0x00	0x00	0x00
	0xEF	*RESERVED*								0x00	0x00	0x00
	0xF0	*RESERVED*								0x00	0x00	0x00
	0xF1	*RESERVED*								0x00	0x00	0x00
	0xF2	*RESERVED*								0x00	0x00	0x00
	0xF3	*RESERVED*								0x00	0x00	0x00
	0xF4	*RESERVED*								0x00	0x00	0x00
	0xF5	*RESERVED*								0x00	0x00	0x00
	0xF6	*RESERVED*								0x00	0x00	0x00
	0xF7	*RESERVED*								0x00	0x00	0x00
	0xF8	*RESERVED*								R	R	R
	0xF9	*RESERVED*								R	R	R
	0xFA	*RESERVED*								R	R	R
	0xFB	*RESERVED*								R	R	R
	0xFC	-								0x00	0x00	0x00
	0xFD	-								0x00	0x00	0x00
	0xFE	-								0x00	0x00	0x00
	0xFF	-				BANK_SEL				0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK3	0x00	RESERVED								0xD0	0xE0	0xE0
	0x01	RESERVED								0x00	0x08	0x08
	0x02	RESERVED								0x87	0x0C	0x0C
	0x03	RESERVED								0x9F	0x9F	0x9F
	0x04	RESERVED								0x00	0x00	0x00
	0x05	RESERVED								0x20	0x20	0x20
	0x06	RESERVED								0x40	0x40	0x40
	0x07	RESERVED								0x80	0x80	0x80
	0x08	RESERVED								0x50	0x50	0x50
	0x09	RESERVED								0x38	0x38	0x38
	0x0A	RESERVED								0xFF	0x0F	0x0F
	0x0B	RESERVED								0x00	0x00	0x00
	0x0C	RESERVED								0x04	0x04	0x04
	0x0D	RESERVED								0x10	0x10	0x10
	0x0E	RESERVED								0x30	0x30	0x30
	0x0F	RESERVED								0x00	0x00	0x00
	0x10	RESERVED								0x06	0x06	0x06
	0x11	RESERVED								0x06	0x06	0x06
	0x12	RESERVED								0x00	0x00	0x00
	0x13	RESERVED								0x80	0x80	0x80
	0x14	RESERVED								0x37	0x37	0x37
	0x15	RESERVED								0x80	0x80	0x80
	0x16	RESERVED								0x49	0x49	0x49
	0x17	RESERVED								0x37	0x37	0x37
	0x18	RESERVED								0xEF	0xEF	0xEF
	0x19	RESERVED								0xDF	0xDF	0xDF
	0x1A	RESERVED								0xDF	0xDF	0xDF
	0x1B	RESERVED								0x15	0x15	0x15
	0x1C	RESERVED								0x0A	0x0A	0x0A
	0x1D	RESERVED								0xBC	0x0C	0x0C
	0x1E	RESERVED								0x01	0x00	0x00
	0x1F	RESERVED								0x88	0x88	0x88

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK3	0x20	*RESERVED*								0x80	0x80	0x80
	0x21	*RESERVED*								0x00	0x02	0x02
	0x22	*RESERVED*								0x23	0x23	0x23
	0x23	*RESERVED*								0x00	0x00	0x00
	0x24	*RESERVED*								0x2A	0x2A	0x2A
	0x25	*RESERVED*								0xC1	0xDC	0xCC
	0x26	*RESERVED*								0xF0	0xF0	0xF0
	0x27	*RESERVED*								0x57	0x57	0x57
	0x28	*RESERVED*								0xD0	0xD0	0xD0
	0x29	*RESERVED*								0x1F	0x1F	0x1F
	0x2A	*RESERVED*								0x50	0x50	0x50
	0x2B	*RESERVED*								0x80	0x9D	0x9D
	0x2C	*RESERVED*								0x00	0x00	0x00
	0x2D	*RESERVED*								0x68	0x68	0x68
	0x2E	*RESERVED*								0x00	0x00	0x00
	0x2F	*RESERVED*								0x07	0x07	0x07
	0x30	*RESERVED*								0xE0	0xE0	0xE0
	0x31	*RESERVED*								0x43	0x43	0x43
	0x32	*RESERVED*								0xA2	0xA2	0xA2
	0x33	*RESERVED*								0x00	0x00	0x00
	0x34	*RESERVED*								0x00	0x00	0x00
	0x35	*RESERVED*								0x17	0x15	0x17
	0x36	*RESERVED*								0x25	0x25	0x25
	0x37	*RESERVED*								0x00	0x00	0x00
	0x38	*RESERVED*								0x02	0x00	0x00
	0x39	*RESERVED*								0x02	0x02	0x02
	0x3A	*RESERVED*								0x00	0x02	0x02
	0x3B	*RESERVED*								0x11	0x00	0x00
	0x3C	**MPP_OUT_SEL1**								0x10	0x00	0x00
	0x3D	**MPP_OUT_SEL2**								0x32	0x00	0x00
	0x3E	**MPP_OUT_SEL3**								0x00	0x00	0x00
	0x3F	**MPP_OUT_SEL4**								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK 3	0x40	RESERVED								0xED	0x00	0x00
	0x41	RESERVED								0x3F	0x00	0x00
	0x42	RESERVED								0x00	0x00	0x00
	0x43	RESERVED								0x00	0x00	0x00
	0x44	RESERVED								0x00	0x00	0x00
	0x45	RESERVED								0x04	0x01	0x01
	0x46	RESERVED								0x00	0x00	0x00
	0x47	RESERVED								0x00	0x00	0x00
	0x48	RESERVED								0x00	0x00	0x00
	0x49	RESERVED								0x84	0x84	0x84
	0x4A	RESERVED								0x00	0x00	0x00
	0x4B	RESERVED								0x00	0x00	0x00
	0x4C	RESERVED								0x20	0x20	0x20
	0x4D	RESERVED								0x10	0x10	0x10
	0x4E	RESERVED								0x00	0x00	0x00
	0x4F	RESERVED								0x00	0x00	0x00
	0x50	RESERVED								0x00	0x00	0x00
	0x51	RESERVED								0xFF	0xFF	0xFF
	0x52	RESERVED								0xFF	0xFF	0xFF
	0x53	RESERVED								0x00	0x00	0x00
	0x54	-								0x00	0x00	0x00
	0x55	-								0x00	0x00	0x00
	0x56	-								0x00	0x00	0x00
	0x57	-								0x00	0x00	0x00
	0x58	-								0x00	0x00	0x00
	0x59	-								0x00	0x00	0x00
	0x5A	-								0x00	0x00	0x00
	0x5B	-								0x00	0x00	0x00
	0x5C	-								0x00	0x00	0x00
	0x5D	-								0x00	0x00	0x00
	0x5E	-								0x00	0x00	0x00
	0x5F	-								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK3	0x60	*RESERVED*								0x52	0x53	0x53
	0x61	*RESERVED*								0x00	0x00	0x00
	0x62	*RESERVED*								0x00	0x00	0x00
	0x63	SEL960H_08	SEL960H_07	SEL960H_06	SEL960H_05	SEL960H_04	SEL960H_03	SEL960H_02	SEL960H_01	0x00	0x00	0x00
	0x64	*RESERVED*								0x00	0x99	0x99
	0x65	*RESERVED*								0x00	0x99	0x99
	0x66	*RESERVED*								0x00	0x99	0x99
	0x67	*RESERVED*								0x00	0x99	0x99
	0x68	*RESERVED*								0xAA	0xFF	0xFF
	0x69	*RESERVED*								0xAA	0xFF	0xFF
	0x6A	*RESERVED*								0xAA	0x00	0x00
	0x6B	*RESERVED*								0xAA	0x00	0x00
	0x6C	*RESERVED*								0x00	0x00	0x00
	0x6D	*RESERVED*								0x00	0x00	0x00
	0x6E	*RESERVED*								0x00	0x00	0x00
	0x6F	*RESERVED*								0x00	0x00	0x00
	0x70	*RESERVED*								0xB8	0xB8	0xB8
	0x71	*RESERVED*								0x01	0x01	0x01
	0x72	*RESERVED*								0x06	0x06	0x06
	0x73	*RESERVED*								0x06	0x06	0x06
	0x74	*RESERVED*								0x11	0x11	0x11
	0x75	*RESERVED*								0x01	0x01	0x01
	0x76	*RESERVED*								0xB5	0xB5	0xB5
	0x77	*RESERVED*								0x13	0x13	0x13
	0x78	*RESERVED*								0x03	0x03	0x03
	0x79	*RESERVED*								0x22	0x22	0x22
	0x7A	-								0x00	0x00	0x00
	0x7B	-								0x00	0x00	0x00
	0x7C	-								0x00	0x00	0x00
	0x7D	-								0x00	0x00	0x00
	0x7E	-								0x00	0x00	0x00
	0x7F	-								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK3	0x80	*RESERVED*								0x00	0x00	0x00
	0x81	*RESERVED*								0x00	0x00	0x00
	0x82	*RESERVED*								0x00	0x00	0x00
	0x83	*RESERVED*								0x00	0x00	0x00
	0x84	*RESERVED*								0x00	0x00	0x00
	0x85	*RESERVED*								0x00	0x00	0x00
	0x86	*RESERVED*								0x00	0x00	0x00
	0x87	*RESERVED*								0x00	0x00	0x00
	0x88	*RESERVED*								0x00	0x00	0x00
	0x89	*RESERVED*								0x00	0x00	0x00
	0x8A	*RESERVED*								0x00	0x00	0x00
	0x8B	*RESERVED*								0x00	0x00	0x00
	0x8C	*RESERVED*								0x00	0x00	0x00
	0x8D	*RESERVED*								0x00	0x00	0x00
	0x8E	*RESERVED*								0x00	0x00	0x00
	0x8F	*RESERVED*								0x00	0x00	0x00
	0x90	*RESERVED*								0x01	0x01	0x01
	0x91	*RESERVED*								0x01	0x01	0x01
	0x92	*RESERVED*								0x01	0x01	0x01
	0x93	*RESERVED*								0x01	0x01	0x01
	0x94	*RESERVED*								0x01	0x01	0x01
	0x95	*RESERVED*								0x01	0x01	0x01
	0x96	*RESERVED*								0x01	0x01	0x01
	0x97	*RESERVED*								0x01	0x01	0x01
	0x98	-								0x00	0x00	0x00
	0x99	-								0x00	0x00	0x00
	0x9A	-								0x00	0x00	0x00
	0x9B	-								0x00	0x00	0x00
	0x9C	-								0x00	0x00	0x00
	0x9D	-								0x00	0x00	0x00
	0x9E	-								0x00	0x00	0x00
	0x9F	-								0x00	0x00	0x00

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
BANK3	0xA0	*RESERVED*								0x00	0x00	0x00
	0xA1	*RESERVED*								0x00	0x00	0x00
	0xA2	*RESERVED*								0x00	0x00	0x00
	0xA3	*RESERVED*								0x00	0x00	0x00
	0xA4	*RESERVED*								0x00	0x00	0x00
	0xA5	*RESERVED*								0x00	0x00	0x00
	0xA6	*RESERVED*								0x00	0x00	0x00
	0xA7	*RESERVED*								0x00	0x00	0x00
	0xA8	*RESERVED*								0x00	0x00	0x00
	0xA9	*RESERVED*								0x00	0x00	0x00
	0xAA	*RESERVED*								0x00	0x00	0x00
	0xAB	*RESERVED*								0x00	0x00	0x00
	0xAC	*RESERVED*								0x00	0x00	0x00
	0xAD	*RESERVED*								0x00	0x00	0x00
	0xAE	*RESERVED*								0x00	0x00	0x00
	0xAF	*RESERVED*								0x00	0x00	0x00
	0xB0	*RESERVED*								0x00	0x00	0x00
	0xB1	*RESERVED*								0x00	0x00	0x00
	0xB2	*RESERVED*								0x00	0x00	0x00
	0xB3	*RESERVED*								0x00	0x00	0x00
	0xB4	*RESERVED*								0x00	0x00	0x00
	0xB5	*RESERVED*								0x00	0x00	0x00
	0xB6	*RESERVED*								0x00	0x00	0x00
	0xB7	*RESERVED*								0x00	0x00	0x00
	0xB8	*RESERVED*								0x00	0x00	0x00
	0xB9	*RESERVED*								0x00	0x00	0x00
	0xBA	*RESERVED*								0x00	0x00	0x00
	0xBB	*RESERVED*								0x00	0x00	0x00
	0xBC	*RESERVED*								0x00	0x00	0x00
	0xBD	*RESERVED*								0x00	0x00	0x00
	0xBE	*RESERVED*								0x00	0x00	0x00
	0xBF	*RESERVED*								0x00	0x00	0x00
	0xFF	-				BANK_SEL				0x00	0x00	0x00

❖ Registers to Power down mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x02	PD_VDAC	[7]	0x10	0x10	**PD_VDAC :** Power down for ALL Video DAC **PD_VDAC_Y :** Power down for Y DAC **PD_VDAC_C :** Power down for C DAC **0 :** Normal Operation **1 :** Power Down
		PD_VDAC_Y	[6]			
		PD_VDAC_C	[5]			
		-	[4]			
		PD_VCH4	[3]			**PD_VCH4 :** Power down for CH4 Video AFE **PD_VCH3 :** Power down for CH3 Video AFE **PD_VCH2 :** Power down for CH2 Video AFE **PD_VCH1 :** Power down for CH1 Video AFE **0 :** Normal Operation **1 :** Power Down
		PD_VCH3	[2]			
		PD_VCH2	[1]			
		PD_VCH1	[0]			
	0x82	PD_VCH8	[3]	0x0	0x0	**PD_VCH8 :** Power down for CH8 Video AFE **PD_VCH7 :** Power down for CH7 Video AFE **PD_VCH6 :** Power down for CH6 Video AFE **PD_VCH5 :** Power down for CH5 Video AFE **0 :** Normal Operation **1 :** Power Down
		PD_VCH7	[2]			
		PD_VCH6	[1]			
		PD_VCH5	[0]			

❖ Registers to Video Standard

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x08	AUTO_1	[7]	0xA0	0xDD	**AUTO_x** **:** A register to set the Auto Detect Mode On/Off; When the AUTO mode has a high value, the Auto_NT_x bit value of the STATUS Register(BANK1, 0xEF / 0xF0]) is to be confirmed to distinguish NTSC-M/J and PAL-B/D/G/H standards. It does not support other standards, and when used in link with the DVR controller, it cannot be used in the NON_REAL_TIME mode. (x = channel 1~8) **0 :** Auto Detect OFF **1 :** Auto Detect ON
	0x09	AUTO_2				
	0x0A	AUTO_3				
	0x0B	AUTO_4				
	0x88	AUTO_5				
	0x89	AUTO_6				
	0x8A	AUTO_7				
	0x8B	AUTO_8				
	0x08	BSF_MODE_1	[6:5]			**BSF_MODE_x** **:** Selects the filter to make primary separation of the brightness and color signals. (x = channel 1~8) **00 :** Don't use **01 :** Mode 1 (NTSC) **10 :** Mode 2 (PAL) **11 :** Mode 3 (Large Noise)
	0x09	BSF_MODE_2				
	0x0A	BSF_MODE_3				
	0x0B	BSF_MODE_4				
	0x88	BSF_MODE_5				
	0x89	BSF_MODE_6				
	0x8A	BSF_MODE_7				
	0x8B	BSF_MODE_8				
	0x08	VIDEO_FORMAT_1	[4:0]			**VIDEO_FORMAT_x** **:** A register to determine the video standards of the input signal (x = channel 1~8) **00000 :** NTSC-M,J **10001 :** NTSC-4.43 **11101 :** PAL-B,D,G,H,I **10110 :** PAL-M **11111 :** PAL-Nc **10101 :** PAL-60 **Others :** None
	0x09	VIDEO_FORMAT_2				
	0x0A	VIDEO_FORMAT_3				
	0x0B	VIDEO_FORMAT_4				
	0x88	VIDEO_FORMAT_5				
	0x89	VIDEO_FORMAT_6				
	0x8A	VIDEO_FORMAT_7				
	0x8B	VIDEO_FORMAT_8				

❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x0C	BRIGHTNESS_1	[7:0]	0xF8	0xF8	**BRIGHTNESS_x** **:** Brightness control; DC level of the Luma signal is adjustable up to -128 ~ +127. BRIGHTNESS consists of 2's Complements. (x = channel 1~8) **00000001** : + 1 **01111111** : + 127 **10000000** : - 128 **11111111** : - 1
	0x0D	BRIGHTNESS_2				
	0x0E	BRIGHTNESS_3				
	0x0F	BRIGHTNESS_4				
	0x8C	BRIGHTNESS_5				
	0x8D	BRIGHTNESS_6				
	0x8E	BRIGHTNESS_7				
	0x8F	BRIGHTNESS_8				

❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x10	CONTRAST_1	[7:0]	0x80	0x80	**CONTRAST_x** **:** Contrast control, Gain level of the Luma signal is adjustable up to x2. (x = channel 1~8) **00000000** : ≒ x 0 **01000000** : ≒ x 0.5 **10000000** : ≒ x 1 **11111111** : ≒ x 2
	0x11	CONTRAST_2				
	0x12	CONTRAST_3				
	0x13	CONTRAST_4				
	0x90	CONTRAST_5				
	0x91	CONTRAST_6				
	0x92	CONTRAST_7				
	0x93	CONTRAST_8				

❖ Registers to Control Sharpness

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x14	H_SHARPNESS_1	[7:4]	0x80	0x80	**H_SHARPNESS_x** **:** Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~8) **0000** : x 0 **0100** : x 0.5 **1000** : x 1 **1111** : x 2
	0x15	H_SHARPNESS_2				
	0x16	H_SHARPNESS_3				
	0x17	H_SHARPNESS_4				
	0x94	H_SHARPNESS_5				
	0x95	H_SHARPNESS_6				
	0x96	H_SHARPNESS_7				
	0x97	H_SHARPNESS_8				
	0x14	V_SHARPNESS_1	[3:0]			**V_SHARPNESS_x** **:** Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~8) **0000** : x 1 **0100** : x 2 **1000** : x 3 **1111** : x 4
	0x15	V_SHARPNESS_2				
	0x16	V_SHARPNESS_3				
	0x17	V_SHARPNESS_4				
	0x94	V_SHARPNESS_5				
	0x95	V_SHARPNESS_6				
	0x96	V_SHARPNESS_7				
	0x97	V_SHARPNESS_8				

❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x18	Y_FIR_MODE_1	[3:0]	0x00	0x00	**Y_FIR_MODE_x** **:** Y Low Pass Filter control (x = channel 1~8) **0000** : 9MHz **0001** : 4.2MHz **0010** : 5.6MHz **0011** : 7.2MHz **0100 ~ 1111 :** Don't use
		Y_FIR_MODE_2	[7:4]			
	0x19	Y_FIR_MODE_3	[3:0]			
		Y_FIR_MODE_4	[7:4]			
	0x98	Y_FIR_MODE_5	[3:0]			
		Y_FIR_MODE_6	[7:4]			
	0x99	Y_FIR_MODE_7	[3:0]			
		Y_FIR_MODE_8	[7:4]			

❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x1A	Y_PEAK_MODE_1	[3:0]	0x11	0x11	**Y_PEAK_MODE_x** **:** Y Peaking Filter control (x = channel 1~8) **0000** : 0dB **0001** : 2dB **0010** : 3.5dB **0011** : 6dB **0100 ~ 1111 :** Don't use
		Y_PEAK_MODE_2	[7:4]			
	0x1B	Y_PEAK_MODE_3	[3:0]			
		Y_PEAK_MODE_4	[7:4]			
	0x9A	Y_PEAK_MODE_5	[3:0]			
		Y_PEAK_MODE_6	[7:4]			
	0x9B	Y_PEAK_MODE_7	[3:0]			
		Y_PEAK_MODE_8	[7:4]			

❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x1C	PED_ON_1	[6]	0x00	0x00	**PED_ON_x** **:** Select to Pedestal ON/OFF (x = channel 1~8) **0** : Pedestal OFF **1** : Pedestal ON
	0x1D	PED_ON_2				
	0x1E	PED_ON_3				
	0x1F	PED_ON_4				
	0x9C	PED_ON_5				
	0x9D	PED_ON_6				
	0x9E	PED_ON_7				
	0x9F	PED_ON_8				

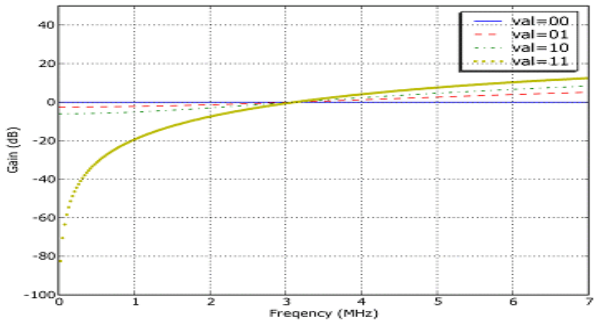
❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x30	Y_DELAY_1	[4:0]	0x08	0x08	**Y_DELAY_x** **:** Y DELAY Control, controllable between 0x00 ~ 0x1F. (x = channel 1~8)
	0x31	Y_DELAY_2				
	0x32	Y_DELAY_3				
	0x33	Y_DELAY_4				
	0xB0	Y_DELAY_5				
	0xB1	Y_DELAY_6				
	0xB2	Y_DELAY_7				
	0xB3	Y_DELAY_8				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x34	ACC_OFF_14	[7]	0x2F	0x2F	**ACC_OFF_14 (CH1~CH4) / ACC_OFF_58 (CH5~CH8)** **:** Continue to a constant gain value for chroma signal **0** : ON **1** : OFF
	0xB4	ACC_OFF_58				
	0x34	ACC_GAIN_SPD_14	[3:0]			**ACC_GAIN_SPD_14 (CH1~CH4) / ACC_GAIN_SPD_58 (CH5~CH8)** **:** 1 step value applied to the ACC Gain Accumulator (ACC Accumulator 1 Step value = 4 * ACC_GAIN_SPD + 2)
	0xB4	ACC_GAIN_SPD_58				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x35	PAL_CM_OFF_14	[7]	0x82	0x02	**PAL_CM_OFF_14 (CH1~CH4) / PAL_CM_OFF_58 (CH5~CH8)** **:** PAL Compensation On/Off. **0** : PAL Compensation applied **1** : PAL Compensation not applied.
	0xB5	PAL_CM_OFF_58				
	0x35	IF_FIR_SEL_14	[6:4]			**IF_FIR_SEL_14 (CH1~CH4) / IF_FIR_SEL_58 (CH5~CH8)** **:** IF Filter drive mode selected. **000** : bypass **001** : mode1 **010** : mode2 **Others** : mode3 
	0xB5	IF_FIR_SEL_58				
	0x35	CLPF_SEL_14	[3:0]			**CLPF_SEL_14 (CH1~CH4) / CLPF_SEL_58 (CH5~CH8)** **:** C low pass filter applied mode applied after color demodulation. **0000 :** Bypass **0001 :** 0.6MHz cut off **0010 :** 1.0MHz cut off **0011 :** 1.2MHz cut off **Others :** Bypass
	0xB5	CLPF_SEL_58				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0xB6	COLOROFF_8	[7]	0x0B	0x0B	**COLOROFF_x** **:** COLOR OFF (x = channel 1~8) **0 :** Color ON **1 :** Color OFF
		COLOROFF_7	[6]			
		COLOROFF_6	[5]			
		COLOROFF_5	[4]			
	0x36	COLOROFF_4	[7]			
		COLOROFF_3	[6]			
		COLOROFF_2	[5]			
		COLOROFF_1	[4]			
	0xB6	C_KILL_58	[3]			**C_KILL_14[3] (CH1~CH4) / C_KILL_14[3] (CH5 ~ CH8)** **:** Select to Color kill mode **0 :** Not Y/C separation **1 :** Color kill after Y/C separation
	0x36	C_KILL_14				
	0xB6	C_KILL_58	[2:0]			**C_KILL_14[2:0] (CH1~CH4) / C_KILL_14[2:0] (CH5 ~ CH8)** **:** color kill control. **000 :** Burst Amplitude 10% Under & FSC Unlock **001 :** Burst Amplitude 5% Under & FSC Unlock **010 :** Burst Amplitude 10 % Under **011 :** Burst Amplitude 5% Under **100 :** Always color on **101 :** Always color on. **110 :** Always color off **111 :** Always color off
	0x36	C_KILL_14				

❖ Registers to Control Sync Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x37	FLD_DET_SPD_14	[7:6]	0x43	0x43	**FLD_DET_SPD_14 (CH1~CH4) / FLD_DET_SPD_58 (CH5~CH8)** **:** Select the method to create the field information that will be externally output . **00 :** Middle **01 :** Slow **10 :** Fast **11 :** Fastest
	0xB7	FLD_DET_SPD_58				
	0x37	NOVID_MODE_14	[3:0]			**NOVID_MODE_14 (CH1~CH4) / NOVID_MODE_58 (CH5~CH8)** **:** Select Condition for No video detection, High Active. **[0] :** If the input video is not detected sync, decision to NO Video **[1] :** If width of detected sync is narrower than video standard, decision to NO Video **[2] :** If Vertical sync don't exist, decision to NO Video **[3] :** If the CLAMP is not stable, decision to NO Video
	0xB7	NOVID_MODE_58				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x38	CTI_GAIN_1	[7:0]	0x08	0x08	**CTI_GAIN_x[7:6]** **:** Adjust CTI Gain Delay **CTI_GAIN_x[4:0]** **:** Adjust gain level for CTI. (x = channel 1~8) **0x00** : No Gain **0x01 ~ 0x1F** : More larger gain
	0x39	CTI_GAIN_2				
	0x3A	CTI_GAIN_3				
	0x3B	CTI_GAIN_4				
	0xB8	CTI_GAIN_5				
	0xB9	CTI_GAIN_6				
	0xBA	CTI_GAIN_7				
	0xBB	CTI_GAIN_8				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x3C	SATURATION_1	[7:0]	0x80	0x80	**SATURATION_x** **:** Color Gain Value (Adjustable up to x2) (x = channel 1~8) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x3D	SATURATION_2				
	0x3E	SATURATION_3				
	0x3F	SATURATION_4				
	0xBC	SATURATION_5				
	0xBD	SATURATION_6				
	0xBE	SATURATION_7				
	0xBF	SATURATION_8				
	0x40	HUE_1	[7:0]	0x01	0x00	**HUE_x** **:** Color HUE Control Value (360°/256 per HUE Value 1 u nit) (x = channel 1~8) **00000000** : 0° **01000000** : 90° **10000000** : 180° **11111111** : 360°
	0x41	HUE_2				
	0x42	HUE_3				
	0x43	HUE_4				
	0xC0	HUE_5				
	0XC1	HUE_6				
	0xC2	HUE_7				
	0xC3	HUE_8				
	0x44	U_GAIN_1	[7:0]	0x00	0x00	**U_GAIN_x** **:** U Gain Value (Adjustable up to x2) (x = channel 1~8) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x45	U_GAIN_2				
	0x46	U_GAIN_3				
	0x47	U_GAIN_4				
	0xC4	U_GAIN_5				
	0xC5	U_GAIN_6				
	0xC6	U_GAIN_7				
	0xC7	U_GAIN_8				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x48	V_GAIN_1	[7:0]	0x00	0x00	**V_GAIN_x** **:** V Gain Value (Adjustable up to x2) (x = channel 1~8) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x49	V_GAIN_2				
	0x4A	V_GAIN_3				
	0x4B	V_GAIN_4				
	0xC8	V_GAIN_5				
	0xC9	V_GAIN_6				
	0xCA	V_GAIN_7				
	0xCB	V_GAIN_8				
	0x4C	U_OFFSET_1	[7:0]	0x00	0x04	**U_OFFSET_x** **:** U offset value is adjustable up to ± 7. U offset consists of 2's complements. (x = channel 1~8) **0111** : + 7 **0001** : + 1 **1111** : - 1 **1000** : - 8
	0x4D	U_OFFSET_2				
	0x4E	U_OFFSET_3				
	0x4F	U_OFFSET_4				
	0XCC	U_OFFSET_5				
	0xCD	U_OFFSET_6				
	0xCE	U_OFFSET_7				
	0xCF	U_OFFSET_8				
	0x50	V_OFFSET_1	[7:0]	0x00	0x04	**V_OFFSET_x** **:** V offset value is adjustable up to ± 7. V offset consists of 2's complements. (x = channel 1~8) **0111** : + 7 **0001** : + 1 **1111** : - 1 **1000** : - 8
	0x51	V_OFFSET_2				
	0x52	V_OFFSET_3				
	0x53	V_OFFSET_4				
	0xD0	V_OFFSET_5				
	0xD1	V_OFFSET_6				
	0xD2	V_OFFSET_7				
	0xD3	V_OFFSET_8				

❖ Registers to Control Field Polarity

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0xD4	FLD_INV_8	[7]	0xF	0x0	**FLD_INV_x** **:** Field Polarity Control (x = channel 1~8) **0** : not Inversion **1** : Inversion
		FLD_INV_7	[6]			
		FLD_INV_6	[5]			
		FLD_INV_5	[4]			
	0x54	FLD_INV_4	[7]			
		FLD_INV_3	[6]			
		FLD_INV_2	[5]			
		FLD_INV_1	[4]			

❖ Registers to Insert No Video Information

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x54	NOVID_INF_IN_14	[3]	0x0	0x0	**NOVID_INF_IN _14 (CH1~CH4) / NOVID_INF_IN_58 (CH5~CH8)** **:** It can include a NO-Video information at MSB of EAV and SAV. **0 :** No information **1 :** Put no-video information in EAV or SAV
	0xD4	NOVID_INF_IN_58				

❖ Registers to Control Channel ID

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x54	CHID_TYPE_14	[2:0]	0x1	0x1	**CHID_TYPE_x** **:** It determines type of channel ID.(x = channel 1~8)
	0xD4	CHID_TYPE_58				
	0x55	CHID_VIN_1	[3:0]	0x10	0x10	**CHID_VIN_x** **:** Register to put CHANNEL ID to distinguish channel. (0x0~0xF) (x = channel 1~8)
		CHID_VIN_2	[7:4]			
	0x56	CHID_VIN_3	[3:0]	0x32	0x32	
		CHID_VIN_4	[7:4]			
	0xD5	CHID_VIN_5	[3:0]	0x54	0x54	
		CHID_VIN_6	[7:4]			
	0xD6	CHID_VIN_7	[3:0]	0x76	0x76	
		CHID_VIN_8	[7:4]			

❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x58	H_DELAY_1	[7:0]	0xB2	0xB2	**H_DELAY_x** **:** Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal. (x = channel 1~8)
	0x59	H_DELAY_2				
	0x5A	H_DELAY_3				
	0x5B	H_DELAY_4				
	0xD8	H_DELAY_5				
	0xD9	H_DELAY_6				
	0xDA	H_DELAY_7				
	0xDB	H_DELAY_8				
	0x5C	V_DELAY_1	[7:0]	0x1E	0x1E	**V_DELAY_x[7:6]** **:** Select V Blank Start Line Variation every Field (x = channel 1~8) **00 :** Current Field **01 :** Inverted Current Field **10 :** 0 **11 :** 1 **V_DELAY_x[5]** **:** V_DELAY_x[4:0] Control Enable (x = channel 1~8) **V_DELAY_x[4:0] (When V_DELAY_x[5] = 1)** **:** Register to determine the Vertical start position of output image to Vsync extracted in analog input signal. (x = channel 1~8)
	0x5D	V_DELAY_2				
	0x5E	V_DELAY_3				
	0x5F	V_DELAY_4				
	0xDC	V_DELAY_5				
	0xDD	V_DELAY_6				
	0xDE	V_DELAY_7				
	0xDF	V_DELAY_8				

❖ Registers to Control Video Output Timing

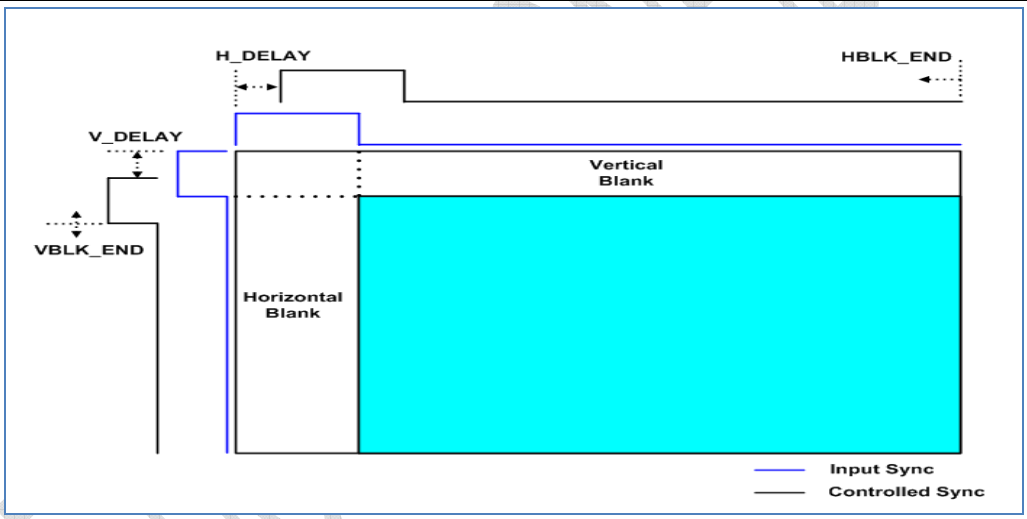
ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x60	HBLK_END_1	[7:0]	0x00	0x00	**HBLK_END_x** **:** Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed. (x = channel 1~8)
	0x61	HBLK_END_2				
	0x62	HBLK_END_3				
	0x63	HBLK_END_4				
	0xE0	HBLK_END_5				
	0xE1	HBLK_END_6				
	0xE2	HBLK_END_7				
	0xE3	HBLK_END_8				
	0x64	VBLK_END_1	[7:0]	0x08	0x0D	**VBLK_END_x[7:6]** **:** Select V Blank End Line Variation every Field (x = channel 1~8) **00 :** Current Field **01 :** Inverted Current Field **10 :** 0 **11 :** 1 **VBLK_END_x[5]** **:** VBLK_END_x[4:0] Control Enable (x = channel 1~8) **VBLK_END_x[4:0] (When VBLK_END_x[5] = 1)** **:** Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then V Active region is changed. (x = channel 1~8)
	0x65	VBLK_END_2				
	0x66	VBLK_END_3				
	0x67	VBLK_END_4				
	0xE4	VBLK_END_5				
	0xE5	VBLK_END_6				
	0xE6	VBLK_END_7				
	0xE7	VBLK_END_8				

❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x68	H_CROP_S_1	[7:0]	0x00	0x00	**H_CROP_S_x** **:** Adjust the horizontal crop start point. (x = channel 1~8)
	0x69	H_CROP_S_2				
	0x6A	H_CROP_S_3				
	0x6B	H_CROP_S_4				
	0xE8	H_CROP_S_5				
	0xE9	H_CROP_S_6				
	0xEA	H_CROP_S_7				
	0xEB	H_CROP_S_8				
	0x6C	H_CROP_E_1	[7:0]	0x00	0x00	**H_CROP_E_x** **:** Adjust the horizontal crop end point. (x = channel 1~8)
	0x6D	H_CROP_E_2				
	0x6E	H_CROP_E_3				
	0x6F	H_CROP_E_4				
	0xEC	H_CROP_E_5				
	0xED	H_CROP_E_6				
	0xEE	H_CROP_E_7				
	0xEF	H_CROP_E_8				

❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x70	V_CROP_S_1	[7:0]	0x00	0x00	V_CROP_S_x : Adjust the vertical crop start point. (x = channel 1~8)
	0x71	V_CROP_S_2				
	0x72	V_CROP_S_3				
	0x73	V_CROP_S_4				
	0xF0	V_CROP_S_5				
	0xF1	V_CROP_S_6				
	0xF2	V_CROP_S_7				
	0xF3	V_CROP_S_8				
	0x74	V_CROP_E_1	[7:0]	0x00	0x00	V_CROP_E_x : Adjust the vertical crop end point. (x = channel 1~8)
	0x75	V_CROP_E_2				
	0x76	V_CROP_E_3				
	0x77	V_CROP_E_4				
	0xF4	V_CROP_E_5				
	0xF5	V_CROP_E_6				
	0xF6	V_CROP_E_7				
	0xF7	V_CROP_E_8				



❖ Registers to Control Back Ground Color

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x78	BGDCOL_1	[3:0]	0x88	0x88	**BGDCOL_x** **:** When No-Video, BackGround Color is used. (x = channel 1~8) **0000** : Blue **0001** : White (75%) **0010** : Yellow **0011** : Cyan **0100** : Green **0101** : Magenta **0110** : Red **0111** : Blue **1000** : Black **1001** : Gray **1010** : Red (NEXTCHIP*) **1011** : Yellow (NEXTCHIP*) **1100** : Magenta (NEXTCHIP*) **1101** : Green (NEXTCHIP*) **1110** : Blue (NEXTCHIP*) **1111** : Cyan (NEXTCHIP*) *** These color information is exactly same as controllers provided by NEXTCHIP**
		BGDCOL_2	[7:4]			
	0x79	BGDCOL_3	[3:0]			
		BGDCOL_4	[7:4]			
	0xF8	BGDCOL_5	[3:0]			
		BGDCOL_6	[7:4]			
	0xF9	BGDCOL_7	[3:0]			
		BGDCOL_8	[7:4]			

❖ Registers to Control Data Out Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x7A	DATA_OUT_MODE_1	[3:0]	0x11	0x11	**DATA_OUT_MODE_x** **:** It limits a level of output data, can change signals of Cb and Cr each. (x = channel 1~8) **0000** : Y(016~235), Cb(016~240), Cr(016~240) **0010** : Y(000~255), Cb(000~255), Cr(000~255) **0100** : Cb / Cr Change, 001~254 **0110** : Cb / Cr Kill, 001~254 **0001** : Y(001~254), Cb(001~254), Cr(001~254) **0011** : Cb / Cr Change, 016~235 **0101** : Cb / Cr Kill, 016~235 **Others** : Background color output
		DATA_OUT_MODE_2	[7:4]			
	0x7B	DATA_OUT_MODE_3	[3:0]			
		DATA_OUT_MODE_4	[7:4]			
	0xFA	DATA_OUT_MODE_5	[3:0]			
		DATA_OUT_MODE_6	[7:4]			
	0xFB	DATA_OUT_MODE_7	[3:0]			
		DATA_OUT_MODE_8	[7:4]			

❖ Registers to Control Audio AFE and DFE

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x00	PD_AAL	[7]	0x02	0x02	**PD_AAL** **:** Audio AFE CH1~CH8 Power Down Mode selection 0 : Normal Operation 1 : Power Down
		PD_AAM	[6]			**PD_AAM** **:** Audio AFE MIC1~MIC2 Power Down Mode selection 0 : Normal Operation 1 : Power Down
		PD_AD	[4]			**PD_AD** **:** Audio DAC Power Down Mode selection 0 : Normal Operation 1 : Power Down
		RM_PB_PIN	[3]			**RM_PB_PIN** **:** Selection of clock and sync for ADATA_REC, ADATA_SP pin 0 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_REC, ADATA_SP pin 1 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_REC, ADATA_SP pin
		PB_RM_PIN	[2]			**PB_RM_PIN** **:** Selection of clock and sync for ADATA_PB pin 0 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_PB, 1 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_PB,
		FILTER_ON	[1]			**FILTER_ON** **:** Set ADC sampling rate 0 : Non-oversample (16KHz) 1 : Oversample (64KHz)
		EN_32K_MODE	[0]			**EN_32K_MODE** **:** Operate whole audio system as 32K mode 0 : 16K Mode 1 : 32K Mode

❖ Registers to Control Audio Input Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x01	AIGAIN_01	[3:0]	0x88	0x88	**AIGAIN_x / MIGAIN_x** **:** the gain of analog audio input AIN1-8,MICIN1 and MICIN2. **0000** : mute **0001** : 0.25 **0010** : 0.31 **0011** : 0.38 **0100** : 0.5 **0101** : 0.63 **0110** : 0.75 **0111** : 0.88 **1000** : 1.0 **1001** : 1.25 **1010** : 1.5 **1011** : 1.75 **1100** : 2.0 **1101** : 2.25 **1110** : 2.5 **1111** : 2.75
		AIGAIN_02	[7:4]			
	0x02	AIGAIN_03	[3:0]			
		AIGAIN_04	[7:4]			
	0x03	AIGAIN_05	[3:0]			
		AIGAIN_06	[7:4]			
	0x04	AIGAIN_07	[3:0]			
		AIGAIN_08	[7:4]			
	0x05	MIGAIN_01	[3:0]			
		MIGAIN_02	[7:4]			

❖ Registers to Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x06	CAS_PB	[7]	0x1B	0x1B	**CAS_PB** **:** The Usage of Playback Data when Cascade Mode **0** : use multiple playback data, received through all stage **1** : use single playback data, received through last stage
		TRANS_MODE	[6]			**TRANS_MODE** **:** Control the phase between transferred clock and cascade data **0** : Same phase **1** : Inverted phase
		CAS_PIN	[4]			**CAS_PIN** **:** Control the usage of ADATA_CASI and ADATA_CASO as cascade transmitting **0** : Don't Use **1** : Use
		CASCADE_MODE	[3]			**CASCADE_MODE** **:** Set the chip position when it is cascaded. **0** : ACLK/ASYNC/ADATA Use **1** : ALINKI/ALINKO Use
		PB_MODE	[2]			**PB_MODE** **:** Set Pin to receive playback audio data **0** : ADATA_PB **1** : ADATA_CASI
		CHIP_STAGE	[1:0]			**CHIP_STAGE** **:** Selection of chip state for cascade **0** : middle stage **1** : last stage **2** : first stage **3** : single chip operation
	0x07	RM_MASTER	[7]	0xCB	0xCB	**RM_MASTER** **:** Selection of master & slave mode of ACLK_REC and ASYNC_REC **0** : Slave mode operation **1** : Master mode operation
		RM_CLK	[6]			**RM_CLK** **:** Set the relationship between audio signal outputted to ADATA_REC and clock outputted to ACLK_REC **0** : inverted clock **1** : non-inverted clock
		RM_BITRATE	[5:4]			**RM_BITRATE** **:** Set the bit rate of audio signal outputted to ADATA_REC **0** : 256fs **1** : **384**fs **2** : 320fs **3** : Don't Use
		RM_SAMRATE	[3]			**RM_SAMRATE** **:** Set the sampling rate of data outputted to ADATA_REC **0** : 0KHz **1** : 16KHz
		RM_BITWID	[2]			**RM_BITWID** **:** Set the bit width of data outputted to ADATA_REC **0** : 16bits **1** : 8bits
		RM_SSP	[1]			**RM_SSP** **:** Selection of DSP mode and SSP mode for ADATA_REC pin, when ASYNC_REC is DSP mode. **0** : DAP mode **1** : SSP mode
		RM_SYNC	[0]			**RM_SYNC** **:** Set the sync's mode inputted/outputted to ASYNC_REC. **0** : I2S mode **1** : DSP mode

❖ Registers to Control Audio interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x08	RM_BIT_SWAP	[7]	0x03	0x03	**RM_BIT_SWAP** **:** Set the bit sequence of Audio Data for ADATA_REC **0** : MSB first **1** : LSB first
		R_ADATSP2	[3]			**R_ADATSP** **:** Selection of output data for ADATA_SP **0** : Speaker data **1** : Record data
		R_ADATSP	[2]			
		R_MULTCH	[1:0]			**R_MULTCH** **:** Selection of number of Channel for ADATA_REC **0** : 2ch **1** : 4ch **2** : 8ch **3** : 16ch

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x09	RM_FORMAT	[7:6]	0x00	0x00	**RM_FORMAT** **:** Define the data format outputted to ADATA_REC **0** : linear PCM **1** : Unsigned linear PCM **2** : G.711 format **3** : Don't Use
		RM_LAW_SEL	[3]			**RM_LAW_SEL** **:** Define the G.711 data format outputted to ADATA_REC **0** : u-law **1** : a-law

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x0A	R_SEQ_01	[3:0]	0x10	0x10	**R_SEQ** **:** Sequence of Audio Data for ADATA_REC **0000** : channel 1 data **0001** : channel 2 data **0010** : channel 3 data **0011** : channel 4 data **0100** : channel 5 data **0101** : channel 6 data **0110** : channel 7 data **0111** : channel 8 data **1000** : channel 9 data **1001** : channel 10 data **1010** : channel 11 data **1011** : channel 12 data **1100** : channel 13 data **1101** : channel 14 data **1110** : channel 15 data **1111** : channel 16 data
		R_SEQ_02	[7:4]			
	0x0B	R_SEQ_03	[3:0]	0x32	0x32	
		R_SEQ_04	[7:4]			
	0x0C	R_SEQ_05	[3:0]	0x54	0x54	
		R_SEQ_06	[7:4]			
	0x0D	R_SEQ_07	[3:0]	0x76	0x76	
		R_SEQ_08	[7:4]			
	0x0E	R_SEQ_09	[3:0]	0x98	0x98	
		R_SEQ_10	[7:4]			
	0x0F	R_SEQ_11	[3:0]	0xBA	0xBA	
		R_SEQ_12	[7:4]			
	0x10	R_SEQ_13	[3:0]	0xDC	0xDC	
		R_SEQ_14	[7:4]			
	0x11	R_SEQ_15	[3:0]	0xFE	0xFE	
		R_SEQ_16	[7:4]			

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x12	MIC_SEQ_01	[1:0]	0xE4	0xE4	**MIC_SEQ** **:** Sequence of Mic Data for ADATA_REC **0** : mic 1 data **1** : mic 2 data **2** : mic 3 data **3** : mic 4 data
		MIC_SEQ_02	[3:2]			
		MIC_SEQ_03	[5:4]			
		MIC_SEQ_04	[7:6]			

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x13	PB_MASTER	[7]	0x08	0x08	**PB_MASTER** **:** Selection of master & slave mode of ACLK_PB and ASYNC_PB **0** : Slave mode **1** : Master mode
		PB_CLK	[6]			**PB_CLK** **:** Set the relationship between audio signal outputted to ADATA_PB and clock outputted to ACLK_PB **0** : inverted clock **1** : non-inverted clock
		PB_BITRATE	[5:4]			**PB_BITRATE** **:** Set the bit rate of audio signal outputted to ADATA_PB **0** : 256fs **1** : **384**fs **2** : 320fs
		PB_SAMRATE	[3]			**PB_SAMRATE** **:** Set the sampling rate of data outputted to ADATA_PB **0** : **8**KHz **1** : 16KHz
		PB_BITWID	[2]			**PB_BITWID** **:** Set the bit width of data outputted to ADATA_PB **0** : 16bits **1** : 8bits
		PB_SSP	[1]			**PB_SSP** **:** Set the position of data and sync signals inputted to ADATA_PB, when ASYNC_PB is DSP mode. **0** : DSP mode **1** : SSP mode
		PB_SYNC	[0]			**PB_SYNC** **:** Set the sync's mode inputted/outputted to ASYNC_PB. **0** : I2S mode **1** : DSP mode

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x14	PB_BIT_SWAP	[7]	0x00	0x00	**PB_BIT_SWAP** **:** Set the bit sequence of Audio Data for ADATA_PB **0** : MSB first **1** : LSB first
		PB_SEL	[4:0]			**PB_SEL** **:** select the audio input channel for playback input **00** : channel 01 **01** : channel 02 **02** : channel 03 **03** : channel 04 **04** : channel 05 **05** : channel 06 **06** : channel 07 **07** : channel 08 **08** : channel 09 **09** : channel 10 **0A** : channel 11 **0B** : channel 12 **0C** : channel 13 **0D** : channel 14 **0E** : channel 15 **0F** : channel 16 **10** : Mic input 1 **11** : Mic input 2 **12** : Mic input 3 **13** : Mic input 4

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x15	PB_FORMAT	[7:6]	0x00	0x00	**PB_FORMAT** **:** Define the data format inputted to ADATA_PB **0** : linear PCM **1** : Unsigned linear PCM **2** : G.711 format **3** : Don't Use
		PB_LAW_SEL	[3]			**PB_LAW_SEL** **:** Define the G.711 data format inputted to ADATA_PB **0** : u-law **1** : a-law

❖ Registers to Control Audio Mixing Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x16	MIX_RATIO_01	[3:0]	0x88	0x88	**MIX_RATIO_x** **:** Set the mixing gain for AIN1-15. (x = channel 1~16) **0** : mute **1** : 0.25 **2** : 0.31 **3** : 0.38 **4** : 0.5 **5** : 0.63 **6** : 0.75 **7** : 0.88 **8** : 1.0 **9** : 1.25 **10** : 1.5 **11** : 1.75 **12** : 2.0 **13** : 2.25 **14** : 2.5 **15** : 2.75
		MIX_RATIO_02	[7:4]			
	0x17	MIX_RATIO_03	[3:0]			
		MIX_RATIO_04	[7:4]			
	0x18	MIX_RATIO_05	[3:0]			
		MIX_RATIO_06	[7:4]			
	0x19	MIX_RATIO_07	[3:0]			
		MIX_RATIO_08	[7:4]			
	0x1A	MIX_RATIO_09	[3:0]			
		MIX_RATIO_10	[7:4]			
	0x1B	MIX_RATIO_11	[3:0]			
		MIX_RATIO_12	[7:4]			
	0x1C	MIX_RATIO_13	[3:0]			
		MIX_RATIO_14	[7:4]			
	0x1D	MIX_RATIO_15	[3:0]			
		MIX_RATIO_16	[7:4]			

❖ Registers to Control Audio Mixing Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x1E	MIX_RATIO_M1	[3:0]	0x88	0x88	**MIX_RATIO_Mx/ MIX_RATIO_Px** **:** Set the mixing gain for MICIN1~4 / PBIN1~4. (x = channel 1~4) **0** : mute **1** : 0.25 **2** : 0.31 **3** : 0.38 **4** : 0.5 **5** : 0.63 **6** : 0.75 **7** : 0.88 **8** : 1.0 **9** : 1.25 **10** : 1.5 **11** : 1.75 **12** : 2.0 **13** : 2.25 **14** : 2.5 **15** : 2.75
		MIX_RATIO_M2	[7:4]			
	0x1F	MIX_RATIO_M3	[3:0]			
		MIX_RATIO_M4	[7:4]			
	0x20	MIX_RATIO_P1	[3:0]			
		MIX_RATIO_P2	[7:4]			
	0x21	MIX_RATIO_P3	[3:0]			
		MIX_RATIO_P4	[7:4]			
	0x22	AOGAIN	[7:4]	0x80	0x80	**AOGAIN** **:** Control the magnitude of output mixing signal **0** : mute **1** : 0.25 **2** : 0.31 **3** : 0.38 **4** : 0.5 **5** : 0.63 **6** : 0.75 **7** : 0.88 **8** : 1.0 **9** : 1.25 **10** : 1.5 **11** : 1.75 **12** : 2.0 **13** : 2.25 **14** : 2.5 **15** : 2.75

❖ Registers to Control Audio Mixing Output Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x23	MIX_DERATIO	[5]	0x19	0x19	**MIX_DERATIO** **:** Selection of the mixing gain mode **0** : Apply the mixing gain for MIX_RATIO_01-P4 (BANK1,0x16~0x21 Addr) separately **1** : Apply all mixing gain as the same gain (x1).
		MIX_OUTSEL	[4:0]			**MIX_OUTSEL** **:** Select the audio output for analog mixing out. **00** : Channel 1 **01** : Channel 2 **02** : Channel 3 **03** : Channel 4 **04** : Channel 5 **05** : Channel 6 **06** : Channel 7 **07** : Channel 8 **08** : Channel 9 **09** : Channel 10 **0A** : Channel 11 **0B** : Channel 12 **0C** : Channel 13 **0D** : Channel 14 **0E** : Channel 15 **0F** : Channel 16 **10** : playback audio (first stage playback audio) **11** : second playback audio (middle stage playback audio) **12** : third playback audio (middle stage playback audio) **13** : fourth playback audio (middle stage playback audio) **14** : Mic input 1 **15** : Mic input 2 **16** : Mic input 3 **17** : Mic input 4 **18** : Mixed audio **Others** : No audio output

❖ Registers to Control Analog and Digital Mixing output of BLADE

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x24	L_CH_OUTSEL	[4:0]	0x18	0x18	**L_CH_OUTSEL / R_CH_OUTSEL** **:** Select Left/Right channel of the audio output for ADATA_SP pin **00** : Channel 1 **01** : Channel 2 **02** : Channel 3 **03** : Channel 4 **04** : Channel 5 **05** : Channel 6 **06** : Channel 7 **07** : Channel 8 **08** : Channel 9 **09** : Channel 10 **0A** : Channel 11 **0B** : Channel 12 **0C** : Channel 13 **0D** : Channel 14 **0E** : Channel 15 **0F** : Channel 16 **10** : playback audio (first stage playback audio) **11** : second playback audio (middle stage playback audio) **12** : third playback audio (middle stage playback audio) **13** : fourth playback audio (middle stage playback audio) **14** : Mic input 1 **15** : Mic input 2 **16** : Mic input 3 **17** : Mic input 4 **18** : Mixed audio **Others** : No audio output
	0x25	R_CH_OUTSEL		0x16	0x16	

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x26	MIX_MUTE_01	[0]	0x00	0x00	**MIX_MUTE_x** **:** During mixing, selected channels are muted (x = channel value) **0** : mixing data output **1** : mute for selected channel
		MIX_MUTE_02	[1]			
		MIX_MUTE_03	[2]			
		MIX_MUTE_04	[3]			
		MIX_MUTE_05	[4]			
		MIX_MUTE_06	[5]			
		MIX_MUTE_07	[6]			
		MIX_MUTE_08	[7]			
	0x27	MIX_MUTE_09	[0]			
		MIX_MUTE_10	[1]			
		MIX_MUTE_11	[2]			
		MIX_MUTE_12	[3]			
		MIX_MUTE_13	[4]			
		MIX_MUTE_14	[5]			
		MIX_MUTE_15	[6]			
		MIX_MUTE_16	[7]			
	0x28	MIX_MUTE_P1	[0]			
		MIX_MUTE_P2	[1]			
		MIX_MUTE_P3	[2]			
		MIX_MUTE_P4	[3]			
		MIX_MUTE_M1	[4]			
		MIX_MUTE_M2	[5]			
		MIX_MUTE_M3	[6]			
		MIX_MUTE_M4	[7]			

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x29	ADET_MODE	[3]	0x88	0x88	**ADET_MODE** **:** Select the method to decide the existence of audio signals. **0** : Absolute amplitude detection mode **1** : Differential amplitude detection mode
		ADET_FILT	[2:0]			**ADET_FILT** **:** Set the time to decide the existence of audio signals. **0** : 16sec **1** : 15sec **2** : 9sec **3** : 5sec **4** : 3sec **5** : 1sec **6** : 0.6sec **7** : 0.5sec

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x2A	ADET_01	[0]	0xFF	0xFF	**ADET_0x / ADET_Mx** **:** Enable bit audio signal existence checking function for AIN1-8,MICIN1 and MICIN2. (x = channel 1~8) **0** : Don't use this function **1** : Use this function
		ADET_02	[1]			
		ADET_03	[2]			
		ADET_04	[3]			
		ADET_05	[4]			
		ADET_06	[5]			
		ADET_07	[6]			
		ADET_08	[7]			
	0x2B	ADET_M1	[6]	0xC0	0xC0	
		ADET_M2	[7]			

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x2C	ADET_TH_01	[3:0]	0xAA	0xAA	**ADET_TH_0x** **:** Set the threshold value for audio signal existence of AIN1-8, MICIN1 and MICIN2
		ADET_TH_02	[7:4]			
	0x2D	ADET_TH_03	[3:0]			
		ADET_TH_04	[7:4]			
	0x2E	ADET_TH_05	[3:0]			
		ADET_TH_06	[7:4]			
	0x2F	ADET_TH_07	[3:0]			
		ADET_TH_08	[7:4]			
	0x30	ADET_TH_M1	[3:0]			
		ADET_TH_M2	[7:4]			

❖ Registers to Control Audio Analog Input

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x31	DCA_0	[1:0]	0x02	0x02	**DC_A :** Set DC level of inputted audio signal through ADC for Live **DC_B :** Set DC level of inputted audio signal through ADC for Mic
	0x33	DCB_0				
	0x32	DCA_1	[7:0]	0x00	0x00	
	0x34	DCB_1				

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x37	REC_8K	[7:6]	0x00	0x00	**REC_8K** **:** Selection of 8K decimation filter **0** : 3 tap decimation filter **1** : 2 tap decimation filter **2** : Bypass 8k data **3** : 3 tap decimation filter
		PB_8K	[5:4]			**PB_8K** **:** Selection of 16K interpolation filter **0** : 3 tap interpolation filter **1** : 2 tap interpolation filter **2** : Bypass 8k data **3** : 3 tap interpolation filter

❖ Registers to Control Audio Input

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x38	AUD_SW_RST	[4]	0x00	0x00	**AUD_SW_RST** **:** Software Reset (High Active only) **0** : Normal Operation **0=>1** : Reset

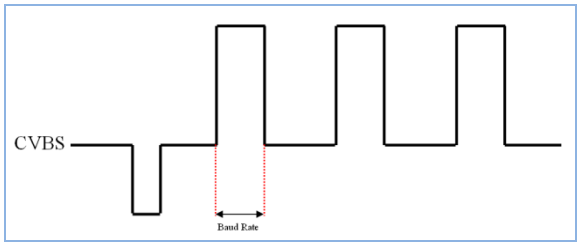
❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x39	RM_DELAY	[7]	0x05	0x05	**RM_DELAY** **:** ASYNCN_REC signal delay control (72MHz Clock Unit) **0** : No Delay **1** : 1clk delay
		PB_DELAY	[6]			**PB_DELAY** **:** ASYNCN_PB signal delay control (72MHz Clock Unit) **0** : No Delay **1** : 1clk delay

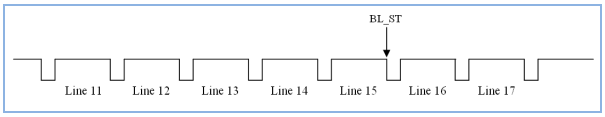
❖ Registers to Control Clock PLL

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x48	VPLL_C	[0]	0x60	0x60	**VPLL_C** **:** PLL Divide Value (OD, M, N) applied at PLL is permitted at a time (HIGH Active only) 0 : Not applied 1 : Applied
	0x49	PLL_OFF	[4]	0x00	0x00	**PLL_OFF** **:** Power down control; Active high 0 : Normal Operation 1 : PLL Power Down
		PLL_BP	[1]			**PLL_BP** **:** Bypass the PLL; Active high 0 : Normal Operation 1 : PLL Bypass
		PLL_RST	[0]			**PLL_RST** **:** PLL Debugging Mode 0 : Normal Operation 1 : Reset M/N dividers. PLL is open loop in VPLL_RST=1 mode, therefore the Output frequency becomes unknown. VPLL_RST=1 mode is for debugging only.
	0x4A	OD	[5:4]	0x22	0x22	**OD** **:** Output divider control pin
		N	[3:0]			**N** **:** Input 4-bit divider control pins, N[0] is LSB
	0x4B	M	[7:0]	0x20	0x20	**M** **:** Feedback 8-bit divider control pins, M[0] is LSB
Algorithmic for PLL Output Frequency						The PLL output frequency, PLL_OUT, is determined by the ratio set between the value set in the input divider and the feedback divider. PLL output frequency PLL_OUT is calculated from the following equations : **1) PLL OUT = XIN X** $\frac{M}{N}$ **X** $\frac{1}{NO}$ **2) M = M7X128 + M6X64 + M5X32 + M4X16 + M3X8 + M2X4 + M1X2 + M0X1** **3) N = N3X8 + N2X4 + N1X2 + N0X1** **4) NO =** $2^{OD\ 0+2\,xOD\ 1}$ **Where :** **PLL_OUT represents the output frequency** **XIN represents PLL input frequency** **N represents input divider value** **M represents feedback divider value** **NO represents output divider value** **[Attention]** **Please keep these condition through usage** **1.** **1MHz ≤** $\frac{XIN}{N}$ **≤ 25MHz** **2.** **200MHz ≤ PLL_OUT ≤ 1000MHz** **3.** **M ≥ 2 , N ≥ 2**

❖ Registers to Control Baud Rate

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x50	BAUD	[7:0]	0x37	0x37	**BAUD** : Samsung TX Baud Rate
	0x51	RBAUD	[7:0]	0x37	0x37	**RBAUD** : Samsung RX Baud Rate
	0x52	PELCO_BAUD	[7:0]	0x1B	0x1B	**PELCO_BAUD** : PELCO TX Baud Rate
Coaxial protocol 1H Line						

❖ Registers to Control Start Point of VBI(Vertical Blank Interval)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x53	BL_TXST_01	[7:0]	0x05	0x05	**BL_TXST_01** : Samsung Protocol TX start Line in VBI BL_TXST_01 is Lower 8bit
	0x54	BL_TXST_02	[3:0]	0x00	0x00	**BL_TXST_02** : Samsung Protocol TX start Line in VBI BL_TXST_02 is upper 4bit
	0x55	BL_RXST_01	[7:0]	0x07	0x07	**BL_RXST_01** : Samsung Protocol RX Start Line in VBI BL_RXST_01 is Lower 8bit
	0x56	BL_RXST_02	[3:0]	0x00	0x00	**BL_RXST_02** : Samsung Protocol RX Start Line in VBI BL_RXST_02 is upper 8bit
	0x57	PELCO_TXST_01	[7:0]	0x09	0x09	**PELCO_TXST_01** : PELCO Protocol TX Start Line in VBI PELCO_TXST_01 is lower 8bit
	0x58	PELCO_TXST_02	[3:0]	0x00	0x00	**PELCO_TXST_02** : PELCO Protocol TX Start Line in VBI PELCO_TXST_02 is upper 8bit
Coaxial protocol Active Start Point of VBI(Vertical Blank Interval)						

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x59	TX_START	[0]	0x00	0x00	**TX_START** : Samsung Protocol Enable Signal
	0x5A	TX_BYTE_LENGTH	[4:0]	0x08	0x08	**TX_BYTE_LENGTH** : Transmission amount In Samsung Protocol
	0x5B	PACKET_MODE	[2:0]	0x06	0x06	**PACKET_MODE** : Coaxial Protocol Type **0** : Samsung Protocol 2 Line Mode **2** : Pelco Protocol Origin Mode **1** : Samsung Protocol 4 Line Mode **6** : Pelco Protocol Exp mode
	0x5C	PELCO_CTEN	[0]	0x00	0x00	**PELCO_CTEN** : PELCO Protocol Enable Bit (Active High)
	0x5D	BL_HSP_01	[7:0]	0x46	0x46	**BL_HSP_01** : Start Point in Coaxial Protocol Active Line BL_HSP_01 is lower 8bit
	0x5E	BL_HSP_02	[7:0]	0x00	0x00	**BL_HSP_02** : Start Point in Coaxial Protocol Active Line BL_HSP_02 is upper 8bit
	0x5F	PELCO_SHOT	[0]	0x00	0x00	**PELCO_SHOT** : PELCO Protocol One Operation Enable signal

❖ Registers to Control Coaxial Data

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x60	TX_DATA_01	[7:0]	0xAA	0xAA	**TX_DATA_01 ~ TX_DATA_04** : 1st field Data in Samsung Protocol
	0x61	TX_DATA_02	[7:0]	0x1C	0x1C	
	0x62	TX_DATA_03	[7:0]	0x18	0x18	
	0x63	TX_DATA_04	[7:0]	0xFF	0xFF	
	0x64	TX_DATA_05	[7:0]	0xAA	0xAA	**TX_DATA_05 ~ TX_DATA_08** : 2nd field Data in Samsung Protocol
	0x65	TX_DATA_06	[7:0]	0x3C	0x3C	
	0x66	TX_DATA_07	[7:0]	0xFF	0xFF	
	0x67	TX_DATA_08	[7:0]	0xFF	0xFF	
	0x68	TX_DATA_09	[7:0]	0xAA	0xAA	**TX_DATA_09 ~ TX_DATA_12** : 3rd field Data in Samsung Protocol
	0x69	TX_DATA_10	[7:0]	0x1B	0x1B	
	0x6A	TX_DATA_11	[7:0]	0x00	0x00	
	0x6B	TX_DATA_12	[7:0]	0x00	0x00	
	0x6C	TX_DATA_13	[7:0]	0xAA	0xAA	**TX_DATA_13 ~ TX_DATA_16** : 4th field Data in Samsung Protocol
	0x6D	TX_DATA_14	[7:0]	0x3B	0x3B	
	0x6E	TX_DATA_15	[7:0]	0x00	0x00	
	0x6F	TX_DATA_16	[7:0]	0x00	0x00	
	0x70	PELCO_TXDAT_01	[7:0]	0x00	0x00	**PELCO_TXDAT_01 / PELCO_TXDAT_02** : 18th Line in PELCO Protocol
	0x71	PELCO_TXDAT_02	[7:0]	0x00	0x00	
	0x72	PELCO_TXDAT_03	[7:0]	0x00	0x00	**PELCO_TXDAT_03 ~ PELCO_TXDAT_04** : 19th Line in PELCO Protocol
	0x73	PELCO_TXDAT_04	[7:0]	0x00	0x00	

❖ Registers to Control Output Port of Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x74	RX_DATA_01	[7:0]	R	R	RX_DATA_01 ~ RX_DATA_04 : 1st line Rx data from Samsung Protocol
	0x75	RX_DATA_02	[7:0]	R	R	
	0x76	RX_DATA_03	[7:0]	R	R	
	0x77	RX_DATA_04	[7:0]	R	R	
	0x78	RX_DATA_05	[7:0]	R	R	RX_DATA_05 ~ RX_DATA_08 : 2nd line Rx data from Samsung Protocol
	0x79	RX_DATA_06	[7:0]	R	R	
	0x7A	RX_DATA_07	[7:0]	R	R	
	0x7B	RX_DATA_08	[7:0]	R	R	
	0x7C	VSO_INV	[7:0]	0x00	0x00	VSO_INV : Vertical Sync Inverter (Active High)
	0x7D	HSO_INV	[7:0]	0x00	0x00	HSO_INV : Horizontal Sync Inverter (Active High)
	0x7E	RX_THRESHOLD	[7:0]	0x80	0x80	RX_THRESHOLD : Controls Detecting Level of RX DATA
	0x7F	Hidden_Even_line_modification	[7:0]	0x01	0x01	Control Protocol Active line on each field
	0x8B	DEVICE_SEL	[2:0]	0x00	0x00	DEVICE_SEL : Control Video channel for Coaxial Protocol 0 : video ch 1 4 : video ch 5 1 : video ch 2 5 : video ch 6 2 : video ch 3 6 : video ch 7 3 : video ch 4 7 : video ch 8

❖ Registers to Control Output Port of Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x8C	COAX_OUT_SEL_1	[3:0]	0x10	0x10	COAX_OUT_SEL_x : Control output MPPx for coaxial command (x = channel number) 0 : MPP1 pin 5 : MPP5 pin 1 : MPP2 pin 6 : MPP6 pin 3 : MPP3 pin 7 : MPP7 pin 4 : MPP4 pin 8 : MPP8 pin
		COAX_OUT_SEL_2	[7:4]			
	0x8D	COAX_OUT_SEL_3	[3:0]	0x32	0x32	
		COAX_OUT_SEL_4	[7:4]			
	0x8E	COAX_OUT_SEL_5	[3:0]	0x54	0x54	
		COAX_OUT_SEL_6	[7:4]			
	0x8F	COAX_OUT_SEL_7	[3:0]	0x76	0x76	
		COAX_OUT_SEL_8	[7:4]			

❖ Registers to Control RX Clean of Samsung Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x90	CLEAN	[0]	0x00	0x00	**CLEAN** **:** RX Register is Read Only. So it need clean Condition First, this register set ON. Second, Read I2C Protocol 0x90. And then Clean the Samsung RX Registers.

❖ Registers to Control Video Encoder

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xA0	BW	[7]	0x00	0x0D	**BW** **:** Black & White On **0** : Off (Color) **1** : On (Black & White)
		CCIR656	[6]			**CCIR656** **:** Video Encoder Input Format Selection **0** : BT.1302 (960H) **1** : BT.656 (720H)
		PATTERN_ON	[5]			**PATTERN_ON** **:** Internal Patterns of Encoder **0** : Pattern Off **1** : Pattern On
		BLANK_ON	[4]			**BLANK_ON** **:** Pedestal Level On/Off **0** : Pedestal Level Off **1** : Pedestal Level On
		LNFMT	[3]			**LNFMT** **:** Field Frequency Selection **0** : 60Hz-NTSC **1** : 50Hz-PAL
		V_ALTER	[2]			**V_ALTER** **:** V alternation On/Off **0** : Off (NTSC) **1** : On (PAL)
		FSC_SEL	[1:0]			**FSC_SEL** **:** Subcarrier Frequency Selection **0** : NTSC-M **1** : PAL-B,D,G,H,I **2** : PAL-M **3** : PAL-N

❖ Registers to Control Video Encoder

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xA2	BURST_RST	[6]	0x47	0x47	**BURST_RST** **:** Color Burst generation Reset at field start point (Low Active only) **0** : Field Reset **1** : Normal Operation
		PAT_NO	[3:0]			**PAT_NO** **:** Internal Pattern Selection **0** : White **1** : Yellow **2** : Cyan **3** : Green **4** : Magenta **5** : Red **6** : Blue **7** : Black **8** : Color_bar **9** : Multi_Burst **Others** : Resolution

❖ Registers to Control Video Encoder

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xA3	CBYPASS	[7]	0x35	0x35	**CBYPASS** **:** Color low-pass filter bypass **0** : Filter Operation **1** : Filter Bypass
		CFIR_NO	[5:4]			**CFIR_NO** **:** Color Low-pass filter selection **0** : 0.6MHz (720H) **1** : 1.3MHz (720H) **2** : 0.6MHz (960H) **3** : 1.3MHz (960H)
		YFIR_NO	[2:0]			**YFIL_NO** **:** Y Low-pass filter selection **0** : 2.25MHz **1** : 3MHz **2** : 4MHz **3** : 5MHz **4** : 5.5MHz **5** : 6MHz **6** : 6.75MHz **7** : Bypass

❖ Registers to Control Video Encoder

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xA4	Y_GAIN	[7:0]	0x80	0x80	**Y_GAIN** **:** Luminance Gain **00000000** : x0 **10000000** : x1 **11111111** : x2
	0xA5	U_GAIN	[7:0]	0x85	0x95	**U_GAIN** **:** U Gain of Chrominance **00000000** : x0 **10000000** : x1 **11111111** : x2
	0xA6	V_GAIN	[7:0]	0x88	0x95	**V_GAIN** **:** V Gain of Chrominance **00000000** : x0 **10000000** : x1 **11111111** : x2
	0xA7	SYNC_GAIN	[7:0]	0x80	0x80	**SYNC_GAIN** **:** Sync Gain **00000000** : x0 **10000000** : x1 **11111111** : x2
	0xA8	BURST_GAIN	[7:0]	0x8C	0x93	**BURST_GAIN** **:** Color Burst Gain **00000000** : x0 **10000000** : x1 **11111111** : x2
	0xA9	PED_GAIN	[7:0]	0x80	0x80	**PED_GAIN** **:** Pedestal Level Gain **00000000** : x0 **10000000** : x1 **11111111** : x2
	0xAA	BLANK_LVL	[7:0]	0x80	0x80	**BLANK_LVL** **:** Blank Level Control **00000000** : -40 IRE DC DOWN **10000000** : 0 IRE DC (default) **11111111** : +40 IRE DC UP

❖ Registers to Control Video Encoder

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xAB	PHASE_TURN	[7:0]	0x80	0x80	**PHASE_TURN** **:** Control SCH (Sub Carrier to Horizontal) Phase **0x00~0xFF** : Phase Increase/Decrease
	0xAC	H_DELAY	[7:0]	0x00	0x00	**H_DELAY** **:** Horizontal Delay Control **0x00~0x7F** : Shift Left **0x80~0xFF** : Shift Right
	0xAD	V_DELAY	[7:0]	0x00	0x00	**V_DELAY** **:** Vertical Delay Control **0x00~0x7F** : Shift Up **0x80~0xFF** : Shift Down
	0xAE	YC_ON	[0]	0x01	0x01	**YC_ON** **:** Video Encoder Analog Output Selection (CVBS / S-VIDEO) **0** : CVBS output **1** : S-Video Output

❖ Registers to Control MPP

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
	0xBC	MPP_SEL1	[3:0]	0x00	0x00	**MPP_SELx** **:** Select MPPx pin output signals selection (x = MPP Pin number) When MPPx_MSB(BANK1,0x4D) = 0, **0 : 0 (Zero)** 1 : NOVIDEO status of ch.x 2 : Horizontal blank of ch.x 3 : Vertical blank of ch.x 4 : Field of ch.x 5 : Mute status of ch.x 6 : Motion status of ch.x 7 : interrupt request by the No video detection 8 : interrupt request by the Mute detection 9 : interrupt request by the Motion detection A : interrupt request by the Black detection B : interrupt request by the White detection C : MPP_GPIO[x-1] Value (BANK1, 0x4C) D : Coaxial Protocol Command of ch x E : Coaxial Protocol Command of ch total **F : Test Mode(Don't use)** When MPPx_MSB(BANK1,0x4D) = 1, **0 : 1 (One)** 1 : Novid | Motion interrupt request 2 : Novid | Black interrupt request 3 : Novid | White interrupt request 4 : Black | White interrupt request 5 : Black | Motion interrupt request 6 : White | Motion interrupt request 7 : Novid | Motion | Black interrupt request 8 : Novid | Motion | White interrupt request 9 : Novid | Motion | White interrupt request A : Novid | Motion | White | mute interrupt request B : Novid | Motion | Mute interrupt request C : Black | White | Motion interrupt request D : Black | White | Motion interrupt request E : Black | White | Motion interrupt request F : Black | White | Motion interrupt request
		MPP_SEL2	[7:4]			
	0xBD	MPP_SEL3	[3:0]			
		MPP_SEL4	[7:4]			
	0xBE	MPP_SEL5	[3:0]			
		MPP_SEL6	[7:4]			
	0xBF	MPP_SEL7	[3:0]			
		MPP_SEL8	[7:4]			

❖ Registers to Select Video Output

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xC0	VPORT1_SEQ1	[3:0]	0x10	0x10	**VPORTx_SEQy** **:** Select the type of output video signal through each video output port (x = VDO output port number, y= channel count for 1 port) **0** : Nomal Display of Channel 1 **1** : Nomal Display of Channel 2 **2** : Nomal Display of Channel 3 **3** : Nomal Display of Channel 4 **4** : Nomal Display of Channel 5 **5** : Nomal Display of Channel 6 **6** : Nomal Display of Channel 7 **7** : Nomal Display of Channel 8 **8** : Motion Display of Channel 1 **9** : Motion Display of Channel 2 **A** : Motion Display of Channel 3 **B** : Motion Display of Channel 4 **C** : Motion Display of Channel 5 **D** : Motion Display of Channel 6 **E** : Motion Display of Channel 7 **F** : Motion Display of Channel 8
		VPORT1_SEQ2	[7:4]			
	0xC1	VPORT1_SEQ3	[3:0]			
		VPORT1_SEQ4	[7:4]			
	0xC2	VPORT2_SEQ1	[3:0]	0x32	0x32	
		VPORT2_SEQ2	[7:4]			
	0xC3	VPORT2_SEQ3	[3:0]			
		VPORT2_SEQ4	[7:4]			
	0xC4	VPORT3_SEQ1	[3:0]	0x54	0x54	
		VPORT3_SEQ2	[7:4]			
	0xC5	VPORT3_SEQ3	[3:0]			
		VPORT3_SEQ4	[7:4]			
	0xC6	VPORT4_SEQ1	[3:0]	0x76	0x76	
		VPORT4_SEQ2	[7:4]			
	0xC7	VPORT4_SEQ3	[3:0]			
		VPORT4_SEQ4	[7:4]			
	0xC8	CH_OUT_SEL1	[3:0]	0x22	0x22	**CH_OUT_SEQx** **:** Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) **0** : 36MHz D1 data of 1ea channel **1** : 36MHz time-mixed CIF 2ea channel **2** : 72MHz time-mixed D1 data of 2ea channel **3** : 72MHz time-mixed CIF data of 4ea channel **4** : 72MHz time-mixed half c data of 8ea channel **5** : 144MHz time-mixed CIF data of 8ea channel **6** : 144MHz time-mixed y data of 8ea channel **7** : 144MHz time-mixed c data of 8ea channel **8** : 144MHz time-mixed D1 data of 4ea channel **9~F :** Don't use
		CH_OUT_SEL2	[7:4]			
	0xC9	CH_OUT_SEL3	[3:0]			
		CH_OUT_SEL4	[7:4]			

❖ Registers to Control Video Output Enable and MPP

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xCA	VDO_1_EN	[0]	0x0F	0x0F	**VDO_x_EN** **:** VDOx Port Enable (x = VDO output port number) **0** : Disable **1** : Enable
		VDO_2_EN	[1]			
		VDO_3_EN	[2]			
		VDO_4_EN	[3]			
	0xCB	MPP1_INV	[0]	0x00	0x00	**MPPx_INV** **:** MPPx pin output signal inversion (x = MPP pin number) **0** : Non- Inversion **1** : Inversion
		MPP2_INV	[1]			
		MPP3_INV	[2]			
		MPP4_INV	[3]			
		MPP5_INV	[4]			
		MPP6_INV	[5]			
		MPP7_INV	[6]			
		MPP8_INV	[7]			

❖ Registers to Select Video Output Clock

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xCC	VCLK1_SEL	[7:4]	0x30	0x30	**VCLKx_SEL** **:** Select clock frequency and phase of each port. (x = Port number) **0** : 36MHz clock with phase 1 **1** : 36MHz clock with phase 2 **2** : 36MHz clock with phase 3 **3** : 36MHz clock with phase 4 **4** : 72MHz clock with phase 1 **5** : 72MHz clock with phase 2 **6** : 144MHz clock with phase 1 **7** : 144MHz clock with phase 2
	0xCD	VCLK2_SEL				
	0xCE	VCLK3_SEL				
	0xCF	VCLK4_SEL				
	0xCC	VCLK_1_DLY_SEL	[3:0]			**VCLK_x_DLY_SEL** **:** Delay the output clock in the unit of ≒ 1ns. Can be delayed up to ≒ 15ns. (x = Port number) **0000** : ≒ 1ns. **0100** : ≒ 4ns. **1000** : ≒ 7ns. **1111** : ≒ 15ns.
	0xCD	VCLK_2_DLY_SEL				
	0xCE	VCLK_3_DLY_SEL				
	0xCF	VCLK_4_DLY_SEL				

❖ Registers to Control Data

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xD0	OUT_DATA_INV	[3:0]	0x00	0x00	**OUT_DATA_INV** **:** Each Channel VDO Output Data bit order control (**0 :** [7:0], **1 :** [0:7]) **OUT_DATA_INV[0]** : VDO1 Port output order control **OUT_DATA_INV[1]** : VDO2 Port output order control **OUT_DATA_INV[2]** : VDO3 Port output order control **OUT_DATA_INV[3]** : VDO4 Port output order control

❖ Registers to Control MPP

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xD5	S_CLK_ON	[0]	0x00	0x00	**S_CLK_ON** **:** ACLK_PB pin output selection for Clock Cascade **0** : 27MHz Clock Output **1** : ACLK_PB_out
	0xD6	MPP1_DIR	[0]	0x00	0x00	**MPPx_DIR** **:** MPPx pin direction control (x = MPP pin number) **0** : Output Direction **1** : Input Direction
		MPP2_DIR	[1]			
		MPP3_DIR	[2]			
		MPP4_DIR	[3]			
		MPP5_DIR	[4]			
		MPP6_DIR	[5]			
		MPP7_DIR	[6]			
		MPP8_DIR	[7]			

❖ Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xD8	NOVID_01	[0]	Read	Read	**NOVID_0x** **:** Each Channel Video Decoder No Video detection Status (x = Channel number) **0** : On Video **1** : No Video
		NOVID_02	[1]			
		NOVID_03	[2]			
		NOVID_04	[3]			
		NOVID_05	[4]			
		NOVID_06	[5]			
		NOVID_07	[6]			
		NOVID_08	[7]			
	0xD9	MOTION_01	[0]	Read	Read	**MOTION_0x** **:** Each Channel Motion detection Status (x = Channel number) **0** : No MOTION **1** : On MOTION
		MOTION_02	[1]			
		MOTION_03	[2]			
		MOTION_04	[3]			
		MOTION_05	[4]			
		MOTION_06	[5]			
		MOTION_07	[6]			
		MOTION_08	[7]			
	0xDA	BLACK_01	[0]	Read	Read	**BLACK_0x** **:** Each Channel BLACK detection Status (x = Channel number) **0** : No BLACK **1** : On BLACK
		BLACK_02	[1]			
		BLACK_03	[2]			
		BLACK_04	[3]			
		BLACK_05	[4]			
		BLACK_06	[5]			
		BLACK_07	[6]			
		BLACK_08	[7]			
	0xDB	WHITE_01	[0]	Read	Read	**WHITE_0x** **:** Each Channel WHITE detection Status (x = Channel number) . **0** : No WHITE **1** : On WHITE
		WHITE_02	[1]			
		WHITE_03	[2]			
		WHITE_04	[3]			
		WHITE_05	[4]			
		WHITE_06	[5]			
		WHITE_07	[6]			
		WHITE_08	[7]			

❖ Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xDC	MUTE_01	[0]	Read	Read	**MUTE_0x** **:** Each Internal 8 Channel MUTE detection Status (x = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTE _02	[1]			
		MUTE _03	[2]			
		MUTE _04	[3]			
		MUTE _05	[4]			
		MUTE _06	[5]			
		MUTE _07	[6]			
		MUTE _08	[7]			
	0xDD	MUTE _09	[0]	Read	Read	**MUTE_0x** **:** Each External 8 Channel MUTE detection Status (x-1 = EXT Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTE _10	[1]			
		MUTE _11	[2]			
		MUTE _12	[3]			
		MUTE _13	[4]			
		MUTE _14	[5]			
		MUTE _15	[6]			
		MUTE _16	[7]			
	0xDE	MUTEMIC_01	[0]	Read	Read	**MUTEMIC_0x** **:** Each Internal 2 Mic Channel MUTE detection Status (x = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTEMIC_02	[1]			
		MUTEMIC_03	[2]			**MUTEMIC_0x** **:** Each External 2 Mic Channel MUTE detection Status (x-1 = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTEMIC_04	[3]			
	0xE0	NOVID_01B	[0]	Read	Read	**NOVID_0xB** **:** Each Channel Video Decoder No Video detection Status with HOLD option (x = Channel number) **0** : On Video **1** : No Video
		NOVID_02B	[1]			
		NOVID_03B	[2]			
		NOVID_04B	[3]			
		NOVID_05B	[4]			
		NOVID_06B	[5]			
		NOVID_07B	[6]			
		NOVID_08B	[7]			
	0xE1	MOTION_01B	[0]	Read	Read	**MOTION_0xB** **:** Each Channel Motion detection Status with HOLD option (x = Channel number) **0** : No MOTION **1** : On MOTION
		MOTION_02B	[1]			
		MOTION_03B	[2]			
		MOTION_04B	[3]			
		MOTION_05B	[4]			
		MOTION_06B	[5]			
		MOTION_07B	[6]			
		MOTION_08B	[7]			

❖ Registers to Show Chip Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xE2	BLACK_01B	[0]	Read	Read	**BLACK_0xB** : Each Channel BLACK detection Status with HOLD option (x = Channel number) **0** : No BLACK **1** : On BLACK
		BLACK_02B	[1]			
		BLACK_03B	[2]			
		BLACK_04B	[3]			
		BLACK_05B	[4]			
		BLACK_06B	[5]			
		BLACK_07B	[6]			
		BLACK_08B	[7]			
	0xE3	WHITE_01B	[0]	Read	Read	**WHITE_0xB** : Each Channel WHITE detection Status with HOLD option (x = Channel number) **0** : No WHITE **1** : On WHITE
		WHITE_02B	[1]			
		WHITE_03B	[2]			
		WHITE_04B	[3]			
		WHITE_05B	[4]			
		WHITE_06B	[5]			
		WHITE_07B	[6]			
		WHITE_08B	[7]			
	0xE4	MUTE_01B	[0]	Read	Read	**MUTE_0xB** : Each Internal 8 Channel MUTE detection Status with HOLD option (x = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTE_02B	[1]			
		MUTE_03B	[2]			
		MUTE_04B	[3]			
		MUTE_05B	[4]			
		MUTE_06B	[5]			
		MUTE_07B	[6]			
		MUTE_08B	[7]			
	0xE5	MUTE_09B	[0]	Read	Read	**MUTE_0xB** : Each External 8 Channel MUTE detection Status with HOLD option (x-1 = EXT Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTE_10B	[1]			
		MUTE_11B	[2]			
		MUTE_12B	[3]			
		MUTE_13B	[4]			
		MUTE_14B	[5]			
		MUTE_15B	[6]			
		MUTE_16B	[7]			
	0xE6	MUTEMIC_01B	[0]	Read	Read	**MUTEMIC_0xB** : Each Internal 2 Mic Channel MUTE detection Status (x = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTEMIC_02B	[1]			
		MUTEMIC_03B	[2]			**MUTEMIC_0xB** : Each External 2 Mic Channel MUTE detection Status (x-1 = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTEMIC_04B	[3]			

❖ Registers to Show Chip Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xE8	RD_STATE_CLR	[7]	0x90	0x90	**RD_STATE_CLR** **:** Interrupt clear condition selection **0** : Interrupt clear when BANK1, 0xE0~0xE6 Addr Register Read **1** : Interrupt clear when BANK1, 0xD8~0xDE / 0xE0~0xE6 Addr Register Read
		STATE_HOLD	[4]	0x00	0x00	**STATE_HOLD** **:** Interrupt Hold condition selection **0** : No Hold Option, State is Real Time update. **1** : Hold Option operation. State is Hold until cleared
	0xE9	IRQ_INV	[3]	0x00	0x00	**IRQ_INV** **:** IRQ pin output signal inversion **0** : Not Inversion **1** : Inversion
		IRQ_SEL	[2:0]	0x00	0x00	**IRQ_SEL** **:** Select IRQ pin output signals selection When IRQ_MSB(BANK1,0x4E[0]) = 0, **0** : **0 (Zero)** **1** : interrupt request by the No video detection **2** : interrupt request by the Mute detection **3** : interrupt request by the Motion detection **4** : interrupt request by the Black detection **5** : interrupt request by the White detection **6** : ALINKO **7** : BNCO When IRQ_MSB(BANK1,0x4E[0]) = 1, **0** : Novid | Motion interrupt request **1** : Novid | Black interrupt request **2** : Novid | White interrupt request **3** : Black | White interrupt request **4** : Black | Motion interrupt request **5** : White | Motion interrupt request **6** : Novid | Motion | Black interrupt request **7** : Black | White | Motion interrupt request

❖ Registers to Show Chip Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xEC	AGC_LOCK_01	[0]	Read	Read	**AGC_LOCK_0x** **:** Video AGC Locking Status (x = channel number) **0** : No Locking **1** : Locking
		AGC_LOCK_02	[1]			
		AGC_LOCK_03	[2]			
		AGC_LOCK_04	[3]			
		AGC_LOCK_05	[4]			
		AGC_LOCK_06	[5]			
		AGC_LOCK_07	[6]			
		AGC_LOCK_08	[7]			

❖ Registers to Show Chip Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xED	CMP_LOCK_01	[0]	Read	Read	**CMP_LOCK_0x** **:** Video CLAMP Locking status (x = channel number) **0** : No Locking **1** : Locking
		CMP_LOCK_02	[1]			
		CMP_LOCK_03	[2]			
		CMP_LOCK_04	[3]			
		CMP_LOCK_05	[4]			
		CMP_LOCK_06	[5]			
		CMP_LOCK_07	[6]			
		CMP_LOCK_08	[7]			
	0xEE	H_LOCK_01	[0]	Read	Read	**H_LOCK_0x** **:** Video Horizontal Locking status (x = channel number) **0** : No Locking **1** : Locking
		H_LOCK_02	[1]			
		H_LOCK_03	[2]			
		H_LOCK_04	[3]			
		H_LOCK_05	[4]			
		H_LOCK_06	[5]			
		H_LOCK_07	[6]			
		H_LOCK_08	[7]			
	0xEF	Auto_NT_01	[1:0]	Read	Read	**Auto_NT_0x** **:** NT/PAL Detection status (x = channel number) **[0]=0** : PAL **[0]=1** : NTSC **[1]=0** : Not detect Standard **[1]=1** : Detect Standard
		Auto_NT_02	[3:2]			
		Auto_NT_03	[5:4]			
		Auto_NT_04	[7:6]			
	0xF0	Auto_NT_05	[1:0]	Read	Read	
		Auto_NT_06	[3:2]			
		Auto_NT_07	[5:4]			
		Auto_NT_08	[7:6]			
	0xF1	FLD_01	[1:0]	Read	Read	**FLD_0x** **:** Field Detection status (x = channel number) **[0]=0** : Odd Field **[0]=1** : Even Field **[1]=0** : Not detect Standard **[1]=1** : Detect Standard
		FLD_02	[3:2]			
		FLD_03	[5:4]			
		FLD_04	[7:6]			
	0xF2	FLD_05	[1:0]	Read	Read	
		FLD_06	[3:2]			
		FLD_07	[5:4]			
		FLD_08	[7:6]			
	0xF3	BW_01	[0]	Read	Read	**BW_0x** **:** Black / White Detection status (x = channel number) **0** : Color **1** : B/W
		BW_02	[1]			
		BW_03	[2]			
		BW_04	[3]			
		BW_05	[4]			
		BW_06	[5]			
		BW_07	[6]			
		BW_08	[7]			

❖ Registers to Show Chip Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xF4	DEV_ID	[7:0]	0x80	0x80	**DEV_ID** **:** It shows Device ID (NVP1918)
	0xF5	REV_ID	[3:0]	0x00	0x00	**REV_ID** **:** It shows Device ID (NVP1918)
	0xF6	CMP_VALUE	[7:0]	Read	Read	**CMP_VALUE** **:** Show the value for CLAMP about Channel selected by CMP_AGC_CH register
	0xF7	AGC_VALUE	[7:0]	Read	Read	**AGC_VALUE** **:** Show the value for AGC about Channel selected by CMP_AGC_CH register
	0xF8	CMP_AGC_CH	[3:0]	0x00	0x00	**CMP_AGC_CH** **:** Channel Number to check CLAMP/AGC Status **0** : Channel 1 **1** : Channel 2 **2** : Channel 3 **3** : Channel 4 **4** : Channel 5 **5** : Channel 6 **6** : Channel 7 **7** : Channel 8 **More than 8** : Not Use

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x00	MOTION_OFF_01	[4]	0x03	0x03	**MOTION_OFF_0x** **:** Motion Detection On/Off Selection (x = channel number) **0** : Motion detection on **1** : Motion detection off
	0x02	MOTION_OFF_02				
	0x04	MOTION_OFF_03				
	0x06	MOTION_OFF_04				
	0x08	MOTION_OFF_05				
	0x0A	MOTION_OFF_06				
	0x0C	MOTION_OFF_07				
	0x0E	MOTION_OFF_08				
	0x00	MOTION_PIC_01	[1:0]			**MOTION_PIC_0x** **:** Indicates the type of processing made on the area where motion is generated. (x = channel number) **0** : No processing made on the area where motion is generated. **1** : One Field (Luma – 32) **2** : One Field (Luma – 48) **3** : All Field (Luma – 48)
	0x02	MOTION_PIC_02				
	0x04	MOTION_PIC_03				
	0x06	MOTION_PIC_04				
	0x08	MOTION_PIC_05				
	0x0A	MOTION_PIC_06				
	0x0C	MOTION_PIC_07				
	0x0E	MOTION_PIC_08				
	0x01	MOD_TSEN_01	[7:0]	0x60	0x60	**MOD_TSEN_0x** **:** Motion Temporal Sensitivity. (x = channel number) The value (the sum of the motion block) bases on which it is determined whether motion is generated or not (0 -> 255 The greater the number, the less sensitive it gets)
	0x03	MOD_TSEN_02				
	0x05	MOD_TSEN_03				
	0x07	MOD_TSEN_04				
	0x09	MOD_TSEN_05				
	0x0B	MOD_TSEN_06				
	0x0D	MOD_TSEN_07				
	0x0F	MOD_TSEN_08				
	0x10	MOD_PSEN_01	[1:0]	0x00	0x00	**MOD_PSEN_0x** **:** Motion Pixed Sensitivity. Register that determines how much data input in the Motion block is used to search for motion (x = channel number) **0** : bypass **1** : 1/2 **2** : 1/4 **3** : 1/8
		MOD_PSEN_02	[3:2]			
		MOD_PSEN_03	[5:4]			
		MOD_PSEN_04	[7:6]			
	0x11	MOD_PSEN_05	[7:6]	0x00	0x00	
		MOD_PSEN_06	[5:4]			
		MOD_PSEN_07	[3:2]			
		MOD_PSEN_08	[1:0]			
	0x12	MD_960H_01	[0]	0xFF	0xFF	**MD_960H _0x** **:** Motion Detection 720H/960H Selection (x = channel number) **0** : Motion Detection 720H Operation **1** : Motion Detection 960H Operation
		MD_960H _02	[1]			
		MD_960H _03	[2]			
		MD_960H _04	[3]			
		MD_960H _05	[4]			
		MD_960H _06	[5]			
		MD_960H _07	[6]			
		MD_960H _08	[7]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x20 0x38 0x50 0x68 0x80 0x98 0xB0 0xC8	CHx_MOD_01	[7]	0xFF	0xFF	**CHx_MOD_01 ~ CHx_MOD_192 :** Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) **0 :** Motion/Black/White Block Disable **1 :** Motion/Black/White Block Enable
		CHx_MOD_02	[6]			
		CHx_MOD_03	[5]			
		CHx_MOD_04	[4]			
		CHx_MOD_05	[3]			
		CHx_MOD_06	[2]			
		CHx_MOD_07	[1]			
		CHx_MOD_08	[0]			
	0x21 0x39 0x51 0x69 0x81 0x99 0xB1 0xC9	CHx_MOD_09	[7]	0xFF	0xFF	
		CHx_MOD_10	[6]			
		CHx_MOD_11	[5]			
		CHx_MOD_12	[4]			
		CHx_MOD_13	[3]			
		CHx_MOD_14	[2]			
		CHx_MOD_15	[1]			
		CHx_MOD_16	[0]			
	0x22 0x3A 0x52 0x6A 0x82 0x9A 0xB2 0xCA	CHx_MOD_17	[7]	0xFF	0xFF	
		CHx_MOD_18	[6]			
		CHx_MOD_19	[5]			
		CHx_MOD_20	[4]			
		CHx_MOD_21	[3]			
		CHx_MOD_22	[2]			
		CHx_MOD_23	[1]			
		CHx_MOD_24	[0]			
	0x23 0x3B 0x53 0x6B 0x83 0x9B 0xB3 0xCB	CHx_MOD_25	[7]	0xFF	0xFF	
		CHx_MOD_26	[6]			
		CHx_MOD_27	[5]			
		CHx_MOD_28	[4]			
		CHx_MOD_29	[3]			
		CHx_MOD_30	[2]			
		CHx_MOD_31	[1]			
		CHx_MOD_32	[0]			
	0x24 0x3C 0x54 0x6C 0x84 0x9C 0xB4 0xCC	CHx_MOD_33	[7]	0xFF	0xFF	
		CHx_MOD_34	[6]			
		CHx_MOD_35	[5]			
		CHx_MOD_36	[4]			
		CHx_MOD_37	[3]			
		CHx_MOD_38	[2]			
		CHx_MOD_39	[1]			
		CHx_MOD_40	[0]			
	0x25 0x3D 0x55 0x6D 0x85 0x9D 0xB5 0xCD	CHx_MOD_41	[7]	0xFF	0xFF	
		CHx_MOD_42	[6]			
		CHx_MOD_43	[5]			
		CHx_MOD_44	[4]			
		CHx_MOD_45	[3]			
		CHx_MOD_46	[2]			
		CHx_MOD_47	[1]			
		CHx_MOD_48	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x26	CHx_MOD_49	[7]	0xFF	0xFF	**CHx_MOD_01 ~ CHx_MOD_192 :** Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) **0 :** Motion/Black/White Block Disable **1 :** Motion/Black/White Block Enable
	0x3E	CHx_MOD_50	[6]			
	0x56	CHx_MOD_51	[5]			
	0x6E	CHx_MOD_52	[4]			
	0x86	CHx_MOD_53	[3]			
	0x9E	CHx_MOD_54	[2]			
	0xB6	CHx_MOD_55	[1]			
	0xCE	CHx_MOD_56	[0]			
	0x27	CHx_MOD_57	[7]	0xFF	0xFF	
	0x3F	CHx_MOD_58	[6]			
	0x57	CHx_MOD_59	[5]			
	0x6F	CHx_MOD_60	[4]			
	0x87	CHx_MOD_61	[3]			
	0x9F	CHx_MOD_62	[2]			
	0xB7	CHx_MOD_63	[1]			
	0xCF	CHx_MOD_64	[0]			
	0x28	CHx_MOD_65	[7]	0xFF	0xFF	
	0x40	CHx_MOD_66	[6]			
	0x58	CHx_MOD_67	[5]			
	0x70	CHx_MOD_68	[4]			
	0x88	CHx_MOD_69	[3]			
	0xA0	CHx_MOD_70	[2]			
	0xB8	CHx_MOD_71	[1]			
	0xD0	CHx_MOD_72	[0]			
	0x29	CHx_MOD_73	[7]	0xFF	0xFF	
	0x41	CHx_MOD_74	[6]			
	0x59	CHx_MOD_75	[5]			
	0x71	CHx_MOD_76	[4]			
	0x89	CHx_MOD_77	[3]			
	0xA1	CHx_MOD_78	[2]			
	0xB9	CHx_MOD_79	[1]			
	0xD1	CHx_MOD_80	[0]			
	0x2A	CHx_MOD_81	[7]	0xFF	0xFF	
	0x42	CHx_MOD_82	[6]			
	0x5A	CHx_MOD_83	[5]			
	0x72	CHx_MOD_84	[4]			
	0x8A	CHx_MOD_85	[3]			
	0xA2	CHx_MOD_86	[2]			
	0xBA	CHx_MOD_87	[1]			
	0xD2	CHx_MOD_88	[0]			
	0x2B	CHx_MOD_89	[7]	0xFF	0xFF	
	0x43	CHx_MOD_90	[6]			
	0x5B	CHx_MOD_91	[5]			
	0x73	CHx_MOD_92	[4]			
	0x8B	CHx_MOD_93	[3]			
	0xA3	CHx_MOD_94	[2]			
	0xBB	CHx_MOD_95	[1]			
	0xD3	CHx_MOD_96	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x2C	CHx_MOD_97	[7]	0xFF	0xFF	**CHx_MOD_01 ~ CHx_MOD_192 :** Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) **0 :** Motion/Black/White Block Disable **1 :** Motion/Black/White Block Enable
	0x44	CHx_MOD_98	[6]			
	0x5C	CHx_MOD_99	[5]			
	0x74	CHx_MOD_100	[4]			
	0x8C	CHx_MOD_101	[3]			
	0xA4	CHx_MOD_102	[2]			
	0xBC	CHx_MOD_103	[1]			
	0xD4	CHx_MOD_104	[0]			
	0x2D	CHx_MOD_105	[7]	0xFF	0xFF	
	0x35	CHx_MOD_106	[6]			
	0x5D	CHx_MOD_107	[5]			
	0x75	CHx_MOD_108	[4]			
	0x8D	CHx_MOD_109	[3]			
	0xA5	CHx_MOD_110	[2]			
	0xBD	CHx_MOD_111	[1]			
	0xD5	CHx_MOD_112	[0]			
	0x2E	CHx_MOD_113	[7]	0xFF	0xFF	
	0x46	CHx_MOD_114	[6]			
	0x5E	CHx_MOD_115	[5]			
	0x76	CHx_MOD_116	[4]			
	0x8E	CHx_MOD_117	[3]			
	0xA6	CHx_MOD_118	[2]			
	0xBE	CHx_MOD_119	[1]			
	0xD6	CHx_MOD_120	[0]			
	0x2F	CHx_MOD_121	[7]	0xFF	0xFF	
	0x47	CHx_MOD_122	[6]			
	0x5F	CHx_MOD_123	[5]			
	0x77	CHx_MOD_124	[4]			
	0x8F	CHx_MOD_125	[3]			
	0xA7	CHx_MOD_126	[2]			
	0xBF	CHx_MOD_127	[1]			
	0xD7	CHx_MOD_128	[0]			
	0x30	CHx_MOD_129	[7]	0xFF	0xFF	
	0x48	CHx_MOD_130	[6]			
	0x60	CHx_MOD_131	[5]			
	0x78	CHx_MOD_132	[4]			
	0x90	CHx_MOD_133	[3]			
	0xA8	CHx_MOD_134	[2]			
	0xC0	CHx_MOD_135	[1]			
	0xD8	CHx_MOD_136	[0]			
	0x31	CHx_MOD_137	[7]	0xFF	0xFF	
	0x49	CHx_MOD_138	[6]			
	0x61	CHx_MOD_139	[5]			
	0x79	CHx_MOD_140	[4]			
	0x91	CHx_MOD_141	[3]			
	0xA9	CHx_MOD_142	[2]			
	0xC1	CHx_MOD_143	[1]			
	0xD9	CHx_MOD_144	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x32	CHx_MOD_145	[7]	0xFF	0xFF	**CHx_MOD_01 ~ CHx_MOD_192 :** Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) **0 :** Motion/Black/White Block Disable **1 :** Motion/Black/White Block Enable
	0x4A	CHx_MOD_146	[6]			
	0x62	CHx_MOD_147	[5]			
	0x7A	CHx_MOD_148	[4]			
	0x92	CHx_MOD_149	[3]			
	0xAA	CHx_MOD_150	[2]			
	0xC2	CHx_MOD_151	[1]			
	0xDA	CHx_MOD_152	[0]			
	0x33	CHx_MOD_153	[7]	0xFF	0xFF	
	0x4B	CHx_MOD_154	[6]			
	0x63	CHx_MOD_155	[5]			
	0x7B	CHx_MOD_156	[4]			
	0x93	CHx_MOD_157	[3]			
	0xAB	CHx_MOD_158	[2]			
	0xC3	CHx_MOD_159	[1]			
	0xDB	CHx_MOD_160	[0]			
	0x34	CHx_MOD_161	[7]	0xFF	0xFF	
	0x4C	CHx_MOD_162	[6]			
	0x64	CHx_MOD_163	[5]			
	0x7C	CHx_MOD_164	[4]			
	0x94	CHx_MOD_165	[3]			
	0xAC	CHx_MOD_166	[2]			
	0xC4	CHx_MOD_167	[1]			
	0xDC	CHx_MOD_168	[0]			
	0x35	CHx_MOD_169	[7]	0xFF	0xFF	
	0x4D	CHx_MOD_170	[6]			
	0x65	CHx_MOD_171	[5]			
	0x7D	CHx_MOD_172	[4]			
	0x95	CHx_MOD_173	[3]			
	0xAD	CHx_MOD_174	[2]			
	0xC5	CHx_MOD_175	[1]			
	0xDD	CHx_MOD_176	[0]			
	0x36	CHx_MOD_177	[7]	0xFF	0xFF	
	0x4E	CHx_MOD_178	[6]			
	0x66	CHx_MOD_179	[5]			
	0x7E	CHx_MOD_180	[4]			
	0x96	CHx_MOD_181	[3]			
	0xAE	CHx_MOD_182	[2]			
	0xC6	CHx_MOD_183	[1]			
	0xDE	CHx_MOD_184	[0]			
	0x37	CHx_MOD_185	[7]	0xFF	0xFF	
	0x4F	CHx_MOD_186	[6]			
	0x67	CHx_MOD_187	[5]			
	0x7F	CHx_MOD_188	[4]			
	0x97	CHx_MOD_189	[3]			
	0xAF	CHx_MOD_190	[2]			
	0xC7	CHx_MOD_191	[1]			
	0xDF	CHx_MOD_192	[0]			

❖ Registers to Detect BLACK and WHITE

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0xE0	CHx_MOD_145	[7]	0xFF	0xFF	**CHx_MOD_01 ~ CHx_MOD_192 :** Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) **0 :** Motion/Black/White Block Disable **1 :** Motion/Black/White Block Enable
		CHx_MOD_146	[6]			
		CHx_MOD_147	[5]			
		CHx_MOD_148	[4]			
		CHx_MOD_149	[3]			
		CHx_MOD_150	[2]			
		CHx_MOD_151	[1]			
		CHx_MOD_152	[0]			
	0x33 0x4B 0x63 0x7B 0x93 0xAB 0xC3 0xDB	CHx_MOD_153	[7]	0xFF	0xFF	
		CHx_MOD_154	[6]			
		CHx_MOD_155	[5]			
		CHx_MOD_156	[4]			
		CHx_MOD_157	[3]			
		CHx_MOD_158	[2]			
		CHx_MOD_159	[1]			
		CHx_MOD_160	[0]			
	0x34 0x4C 0x64 0x7C 0x94 0xAC 0xC4 0xDC	CHx_MOD_161	[7]	0xFF	0xFF	
		CHx_MOD_162	[6]			
		CHx_MOD_163	[5]			
		CHx_MOD_164	[4]			
		CHx_MOD_165	[3]			
		CHx_MOD_166	[2]			
		CHx_MOD_167	[1]			
		CHx_MOD_168	[0]			
	0x35 0x4D 0x65 0x7D 0x95 0xAD 0xC5 0xDD	CHx_MOD_169	[7]	0xFF	0xFF	
		CHx_MOD_170	[6]			
		CHx_MOD_171	[5]			
		CHx_MOD_172	[4]			
		CHx_MOD_173	[3]			
		CHx_MOD_174	[2]			
		CHx_MOD_175	[1]			
		CHx_MOD_176	[0]			
	0x36 0x4E 0x66 0x7E 0x96 0xAE 0xC6 0xDE	CHx_MOD_177	[7]	0xFF	0xFF	
		CHx_MOD_178	[6]			
		CHx_MOD_179	[5]			
		CHx_MOD_180	[4]			
		CHx_MOD_181	[3]			
		CHx_MOD_182	[2]			
		CHx_MOD_183	[1]			
		CHx_MOD_184	[0]			
	0x37 0x4F 0x67 0x7F 0x97 0xAF 0xC7 0xDF	CHx_MOD_185	[7]	0xFF	0xFF	
		CHx_MOD_186	[6]			
		CHx_MOD_187	[5]			
		CHx_MOD_188	[4]			
		CHx_MOD_189	[3]			
		CHx_MOD_190	[2]			
		CHx_MOD_191	[1]			
		CHx_MOD_192	[0]			

❖ Registers to Control Video Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
3	0x63	SEL960H_08	[7]	0x00	0x00	**SEL_960H_0x** **:** 720H/960H Selection (x = channel number) **0:** 36MHz 960H Mode **1:** 36MHz 720H Mode
		SEL960H_07	[6]			
		SEL960H_06	[5]			
		SEL960H_05	[4]			
		SEL960H_04	[3]			
		SEL960H_03	[2]			
		SEL960H_02	[1]			
		SEL960H_01	[0]			

8. Electrical characteristics

8.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V_{VDD1DM}	0.5	-	1.32	V
1.8V Analog Power Supply Voltage	V_{VDD1AM}	0.5	-	1.95	V
3.3V Digital Power Supply Voltage	V_{VDD3DM}	0.5	-	3.6	V
3.3V Analog Power Supply Voltage	V_{VDD3AM}	0.5	-	3.6	V
Voltage for Digital pins	V_{DIO}	0.5	-	4.6	V
Voltage for Analog Inputs	V_{AIO}	0.5	-	1.95	V
Storage Temperature	T_S	-40	-	125	℃
Junction Temperature	T_J	-40	-	125	℃
Vapor phase soldering (15 Sec)	T_{VSOL}	-	-	220	℃

Note : This Device should be operated under recommended operating condition. Since, absolute maximum rating condition can either cause device reliability problem or damage the device sufficiently to cause immediate failure.

8.2. Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V_{VDD1D}	1.08	1.2	1.32	V
1.8V Analog Power Supply Voltage	V_{VDD1A}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{VDD3D}	3.0	3.3	3.6	V
3.3V Analog Power Supply Voltage	V_{VDD3A}	3.0	3.3	3.6	V
Ambient operating temperature	V_A	0	-	70	℃

8.3. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Input High Voltage	V_{IH}	2	-	V_{DD3D}+0.3	V
Input Leakage Current	I_L	-	-	±1	uA
Input Capacitance (f = 1Mhz, V_{IN} = 2.4V)	C_{IN}	-	-	10	pF
Output Low Voltage (I_{OL} = 8.0mA)	V_{OL}	-	-	0.4	V
Output High Voltage (I_{OH} = 12mA)	V_{OH}	2.4	-	-	V
Tri-State Output Leakage Current	I_{OZ}	-	-	±1	uA
Output Capacitance	C_{OUT}	-	-	10	pF

8.4. AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
(Power Supply Current)					
1.2V Digital Power Supply Current	I_{VDD1D}	-	TBD	-	mA
1.8V Analog Power Supply Current	I_{VDD1A}	-	TBD	-	mA
3.3V Digital Power Supply Current	I_{VDD3D}	-	TBD	-	mA
3.3V Analog Power Supply Current	I_{VDD3A}	-	TBD	-	mA
(Clock Pin)					
XTALI frequency	f_{XTALI}	-	27.0	-	MHz
XTALI duty cycle	f_{DUTY}	45	-	55	%
XTALI pulse width low	t_{PWL_XTALI}	17.0	-	-	nsec
XTALI pulse width high	t_{PWH_XTAL}	17.0	-	-	nsec
(Reset Pin)					
RSTB setup time	t_{SU}	1			us
RSTB pulse width low	t_{PWL_rstb}	1			us
RSTB release time (low to high)	t_{REL_rstb}	10			us
(Host Interface Pins)					
SCL frequency	f_{SCL}	-	-	6	XTALI
SCL minimum pulse width low	t_{PWL_SCL}	6	-	-	XTALI
SCL minimum pulse width high	t_{PWH_SCL}	4	-	-	XTALI
SCL to SDA setup time	t_{IS_SDA}	2	-	-	XTALI
SCL to SDA hold time	t_{IH_SDA}	2	-	-	XTALI
SCL to SDA delay time	t_{OD_SDA}	-	-	6	XTALI
SCL to SDA hold time	t_{OH_SDA}	3	-	-	XTALI

9. Recommended Register Value

: For register values, always make sure to check and use updated values of recommendation.

9.1. NTSC Recommended Register Setting

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK0	0x00	0x11	0x11	0x10	-	0x00	0x00	0xAF	-	0xA0	0xA0	0xA0	0xA0	0xF8	0xF8	0xF8	0xF8
	0x10	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x00	0x00	0x11	0x11	0x8F	0x8F	0x8F	0x8F
	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x30	0x08	0x08	0x08	0x08	0x2F	0x82	0x0B	0x43	0x08	0x08	0x08	0x08	0x80	0x80	0x80	0x80
	0x40	0x01	0x01	0x01	0x01	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x50	0x00	0x00	0x00	0x00	0xF1	0x10	0x32	-	0xB2	0xB2	0xB2	0xB2	0x1E	0x1E	0x1E	0x1E
	0x60	0x00	0x00	0x00	0x00	0x08	0x08	0x08	0x08	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	-	-	-	-
	0x80	0x11	0x11	0x00	-	0x00	0x00	0xAF	-	0xA0	0xA0	0xA0	0xA0	0xF8	0xF8	0xF8	0xF8
	0x90	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x00	0x00	0x11	0x11	0x8F	0x8F	0x8F	0x8F
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x08	0x08	0x08	0x08	0x2F	0x82	0x0B	0x43	0x08	0x08	0x08	0x08	0x80	0x80	0x80	0x80
	0xC0	0x01	0x01	0x01	0x01	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xD0	0x00	0x00	0x00	0x00	0xF1	0x54	0x76	-	0xB2	0xB2	0xB2	0xB2	0x1E	0x1E	0x1E	0x1E
	0xE0	0x00	0x00	0x00	0x00	0x08	0x08	0x08	0x08	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	-	-	-	Bank

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK1	0x00	0x02	0x88	0x88	0x88	0x88	0x88	0x1B	0xC8	0x03	0x00	0x10	0x32	0x54	0x76	0x98	0xBA
	0x10	0xDC	0xFE	0xE4	0x08	0x00	0x00	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88
	0x20	0x88	0x88	0x80	0x19	0x18	0x16	0x00	0x00	0x00	0x88	0xFF	0xC0	0xAA	0xAA	0xAA	0xAA
	0x30	0xAA	0x02	0x00	0x02	0x00	0x00	0x00	0x00	0x00	0x05	0xA1	0x10	0x10	-	0x08	0x00
	0x40	-	-	-	-	0x14	0x01	0x00	0x00	0x60	0x00	0x22	0x20	0x00	0x00	0x00	-
	0x50	0x37	0x37	0x1B	0x05	0x00	0x07	0x00	0x09	0x00	0x00	0x08	0x06	0x00	0x46	0x00	0x00
	0x60	0xAA	0x1C	0x18	0xFF	0xAA	0x3C	0xFF	0xFF	0xAA	0x1B	0x00	0x00	0xAA	0x3B	0x00	0x00
	0x70	0x00	0x00	0x00	0x00	Read	Read	Read	Read	Read	Read	Read	Read	0x00	0x00	0x80	0x01
	0x80	0x00	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x54	0x76
	0x90	0x00	-	-	-	0x00	-	-	-	-	-	-	-	-	-	-	-
	0xA0	0x00	0x00	0x47	0x35	0x8D	0x85	0x88	0x80	0x8C	0x80	0x80	0x80	0x00	0x00	0x01	-
	0xB0	-	-	-	-	0x00	0x00	0x40	0x30	0x40	0x30	0x40	0x30	0x00	0x00	0x00	0x00
	0xC0	0x10	0x10	0x32	0x32	0x54	0x54	0x76	0x76	0x22	0x22	0x0F	0x00	0x30	0x30	0x30	0x30
	0xD0	0x00	0x00	0x00	-	0x00	0x00	0x00	-	Read	Read	Read	Read	Read	Read	Read	-
	0xE0	Read	Read	Read	Read	Read	Read	Read	-	0x90	0x00	-	-	Read	Read	Read	Read
	0xF0	Read	Read	Read	Read	0x80	0x00	Read	Read	0x00	-	-	-	-	-	-	Bank

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK2	0x00	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60
	0x10	0x00	0x00	0x00	0x00	0xC0	-	-	-	-	-	-	-	-	-	-	-
	0x20	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x30	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x40	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x50	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x60	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x70	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x80	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x90	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xA0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xB0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xC0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xD0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	Bank

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK3	0x00	0xE0	0x08	0x0C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x00
	0x10	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x15	0x0A	0x0C	0x01	0x88
	0x20	0x80	0x02	0x23	0x00	0x2A	0xDC	0xF0	0x57	0xD0	0x1F	0x50	0x9D	0x00	0x68	0x00	0x07
	0x30	0xE0	0x43	0xA2	0x00	0x00	0x15	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
	0x40	0x00	0x00	0x00	0x00	0x00	0x01	0x00	0x00	0x00	0x84	0x00	0x00	0x20	0x10	-	-
	0x50	0x00	0xFF	0xFF	0x00	-	-	-	-	-	-	-	-	-	-	-	-
	0x60	0x53	-	0x00	0x00	0x99	0x99	0x99	0x99	0xFF	0xFF	-	-	-	-	-	-
	0x70	0xB8	0x01	0x06	0x06	0x11	0x01	0xB5	0x13	0x03	0x22	-	-	-	-	-	-
	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x90	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	-	-	-	-	-	-	-	-
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

9.2. PAL Recommended Register Setting

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK0	0x00	0x11	0x11	0x10	-	0x00	0x00	0xAF	-	0xDD	0xDD	0xDD	0xDD	0xF8	0xF8	0xF8	0xF8
	0x10	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x00	0x00	0x11	0x11	0x8F	0x8F	0x8F	0x8F
	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x30	0x08	0x08	0x08	0x08	0x2F	0x02	0x0B	0x43	0x08	0x08	0x08	0x08	0x80	0x80	0x80	0x80
	0x40	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x04	0x04	0x04
	0x50	0x04	0x04	0x04	0x04	0x01	0x10	0x32	-	0xB2	0xB2	0xB2	0xB2	0x1E	0x1E	0x1E	0x1E
	0x60	0x00	0x00	0x00	0x00	0x0D	0x0D	0x0D	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	-	-	-	-
	0x80	0x11	0x11	0x00	-	0x00	0x00	0xAF	-	0xDD	0xDD	0xDD	0xDD	0xF8	0xF8	0xF8	0xF8
	0x90	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x00	0x00	0x11	0x11	0x8F	0x8F	0x8F	0x8F
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x08	0x08	0x08	0x08	0x2F	0x02	0x0B	0x43	0x08	0x08	0x08	0x08	0x80	0x80	0x80	0x80
	0xC0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x04	0x04	0x04
	0xD0	0x04	0x04	0x04	0x04	0x01	0x54	0x76	-	0xB2	0xB2	0xB2	0xB2	0x1E	0x1E	0x1E	0x1E
	0xE0	0x00	0x00	0x00	0x00	0x0D	0x0D	0x0D	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	-	-	-	Bank

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK1	0x00	0x02	0x88	0x88	0x88	0x88	0x88	0x1B	0xC8	0x03	0x00	0x10	0x32	0x54	0x76	0x98	0xBA
	0x10	0xDC	0xFE	0xE4	0x08	0x00	0x00	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88
	0x20	0x88	0x88	0x80	0x19	0x18	0x16	0x00	0x00	0x00	0x88	0xFF	0xC0	0xAA	0xAA	0xAA	0xAA
	0x30	0xAA	0x02	0x00	0x02	0x00	0x00	0x00	0x00	0x00	0x05	0xA1	0x10	0x10	-	0x08	0x00
	0x40	-	-	-	-	0x14	0x01	0x00	0x00	0x60	0x00	0x22	0x20	0x00	0x00	0x00	-
	0x50	0x37	0x37	0x1B	0x05	0x00	0x07	0x00	0x09	0x00	0x00	0x08	0x06	0x00	0x46	0x00	0x00
	0x60	0xAA	0x1C	0x18	0xFF	0xAA	0x3C	0xFF	0xFF	0xAA	0x1B	0x00	0x00	0xAA	0x3B	0x00	0x00
	0x70	0x00	0x00	0x00	0x00	Read	Read	Read	Read	Read	Read	Read	Read	0x00	0x00	0x80	0x01
	0x80	0x00	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x54	0x76
	0x90	0x00	-	-	-	0x00	-	-	-	-	-	-	-	-	-	-	-
	0xA0	0x0D	0x00	0x47	0x35	0x89	0x95	0x95	0x80	0x93	0x80	0x80	0x80	0x00	0x00	0x01	-
	0xB0	-	-	-	-	0x00	0x00	0x40	0x30	0x40	0x30	0x40	0x30	0x00	0x00	0x00	0x00
	0xC0	0x10	0x10	0x32	0x32	0x54	0x54	0x76	0x76	0x22	0x22	0x0F	0x00	0x30	0x30	0x30	0x30
	0xD0	0x00	0x00	0x00	-	0x00	0x00	0x00	-	Read	Read	Read	Read	Read	Read	Read	-
	0xE0	Read	Read	Read	Read	Read	Read	Read	-	0x90	0x00	-	-	Read	Read	Read	Read
	0xF0	Read	Read	Read	Read	0x80	0x00	Read	Read	0x00	-	-	-	-	-	-	Bank

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK2	0x00	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60
	0x10	0x00	0x00	0x00	0x00	0xC0	-	-	-	-	-	-	-	-	-	-	-
	0x20	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x30	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x40	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x50	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x60	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x70	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x80	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x90	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xA0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xB0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xC0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xD0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	Bank

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK3	0x00	0xE0	0x08	0x0C	0x9F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x00
	0x10	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x15	0x0A	0x0C	0x01	0x88
	0x20	0x80	0x02	0x23	0x00	0x2A	0xCC	0xF0	0x57	0xD0	0x1F	0x50	0x9D	0x00	0x68	0x00	0x07
	0x30	0xE0	0x43	0xA2	0x00	0x00	0x15	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
	0x40	0x00	0x00	0x00	0x00	0x00	0x01	0x00	0x00	0x00	0x84	0x00	0x00	0x20	0x10	-	-
	0x50	0x00	0xFF	0xFF	0x00	-	-	-	-	-	-	-	-	-	-	-	-
	0x60	0x53	-	0x00	0x00	0x99	0x99	0x99	0x99	0xFF	0xFF	-	-	-	-	-	-
	0x70	0xB8	0x01	0x06	0x06	0x11	0x01	0xB5	0x13	0x03	0x22	-	-	-	-	-	-
	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x90	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	-	-	-	-	-	-	-	-
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

9.3 Coaxial Protocol Recommended Register Setting

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK1	0x50	0x37	0x37	0x1B	0x05	0x00	0x07	0x00	0x09	0x00	0x00	0x08	0x06	0x00	0x46	0x00	0x00
BANK1	0x60	0xAA	0x1B	0x00	0x00	0xAA	0x3B	0x00	0xF1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
BANK1	0x70	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x80	0x00
BANK1	0x80	0xFF	0x00	0x00	0x00	0x00	0x00	0x06	0x01	0x00	0x00	0x00	0x00	0x10	0x32	0x54	0x76

9.4 H960 and SH720 NTSC Recommended difference Register Setting

ADDRESS			0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK0	0x10	H960									0x00	0x00						
		SH720									0x22	0x22						
	0x30	H960	0x08	0x08	0x08	0x08												
		SH720	0x06	0x06	0x06	0x06												
	0x50	H960									0xB2	0xB2	0xB2	0xB2				
		SH720									0xA2	0xA2	0xA2	0xA2				

ADDRESS			0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK3	0x50	H960				0xFF												
		SH720				0x00												
	0x60	H960				0x00												
		SH720				0xFF												
	0x80	H960		0x00		0x00		0x00		0x00								
		SH720		0x40		0x40		0x40		0x40								

9.5 H960 and SH720 PAL Recommended difference Register Setting

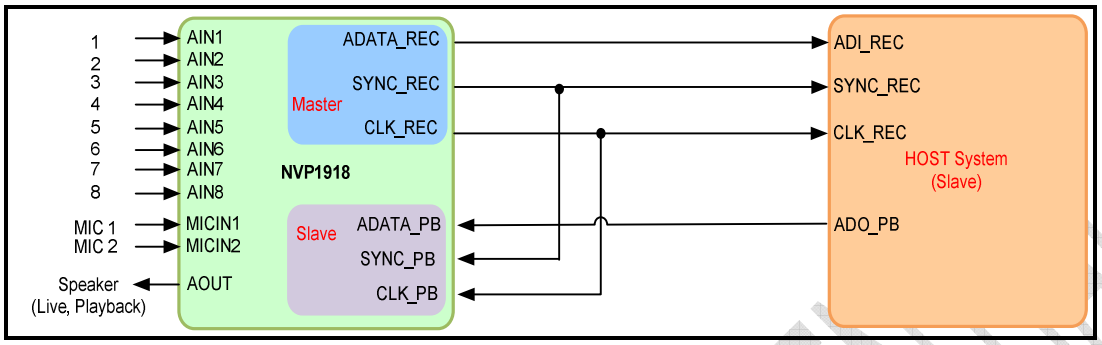
ADDRESS			0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK0	0x10	H960									0x00	0x00						
		SH720									0x33	0x33						
	0x30	H960	0x08	0x08	0x08	0x08												
		SH720	0x08	0x08	0x08	0x08												
	0x50	H960									0xB1	0xB1	0xB1	0xB1				
		SH720									0xB2	0xB2	0xB2	0xB2				

ADDRESS			0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK3	0x50	H960				0xFF												
		SH720				0x00												
	0x60	H960				0x00												
		SH720				0xFF												
	0x80	H960		0x00		0x00		0x00		0x00								
		SH720		0x40		0x40		0x40		0x40								

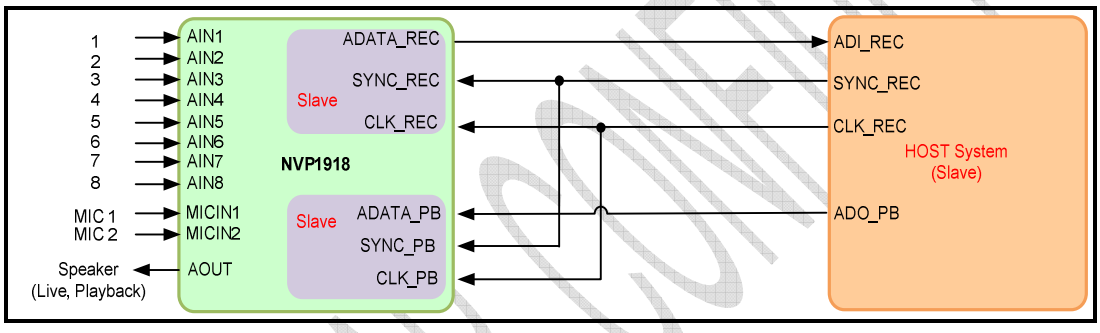
10. System Applications

10.1. 8-Channel, Master Mode

10.1.1. Block Diagram (8 Channel, Master Mode)

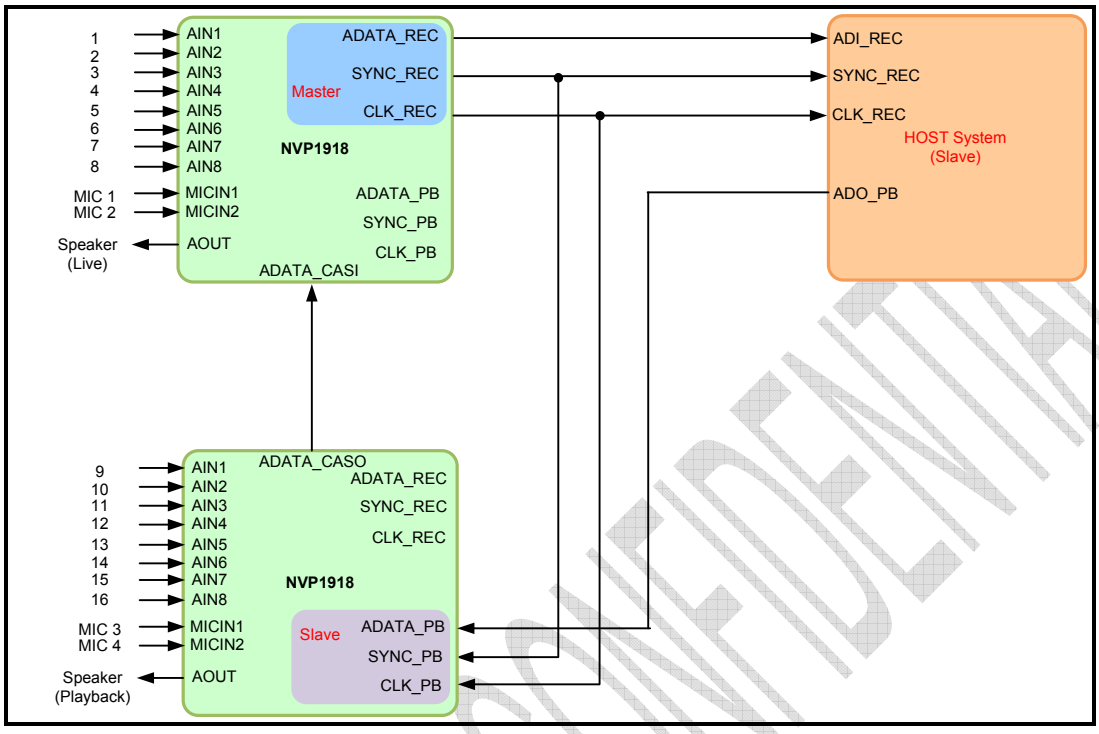


10.1.2. Block Diagram (8 Channel, Slave Mode)

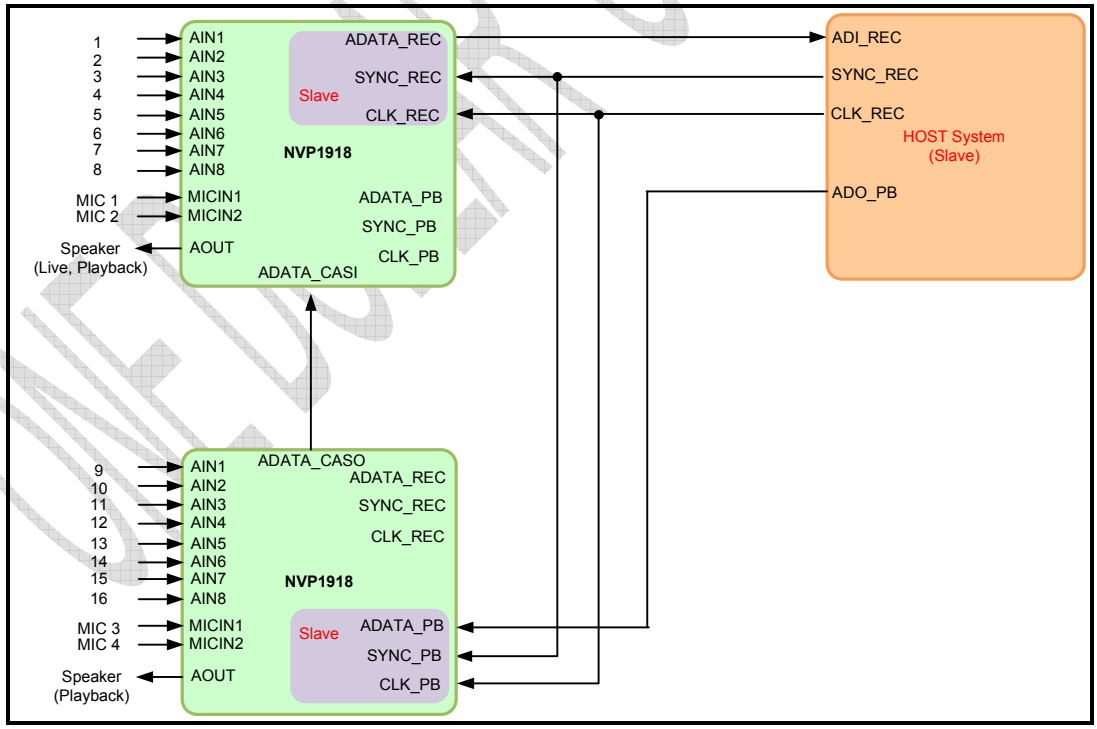


10.2. 16-Channel, Master Mode

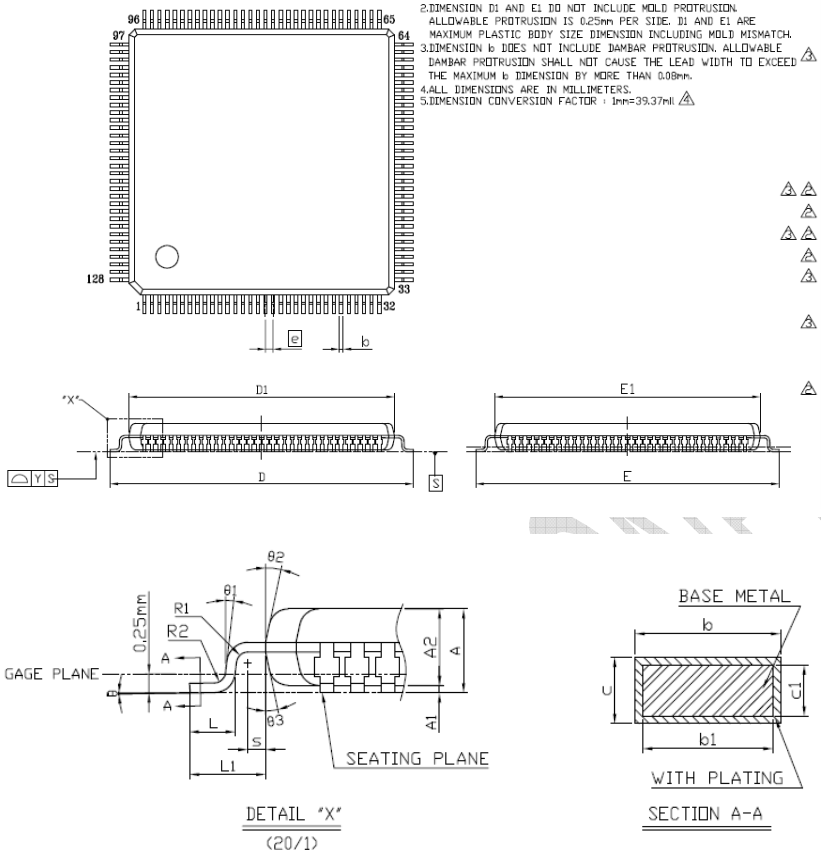
10.2.1. Block Diagram (16 Channel, Master Mode)



10.2.2. Block Diagram (16 Channel, Slave Mode)



11. Package Information



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63.0
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.35	1.40	1.45	53.1	55.1	57.1
b	0.13	0.18	0.23	5.1	7.1	9.1
b1	0.13	0.16	0.19	5.1	6.3	7.5
c	0.09		0.20	3.5		7.9
c1	0.09		0.16	3.5		6.3
D	15.85	16.00	16.15	624.0	629.9	635.8
D1	13.90	14.00	14.10	547.2	551.2	555.1
E	15.85	16.00	16.15	624.0	629.9	635.8
E1	13.90	14.00	14.10	547.2	551.2	555.1
e	0.35	0.40	0.45	13.8	15.7	17.7
L	0.45	0.60	0.75	17.7	23.6	29.5
L1	0.85	1.00	1.15	33.5	39.4	45.3
R1	0.08			3.1		
R2	0.08		0.20	3.1		7.9
Y			0.08			3.1
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		