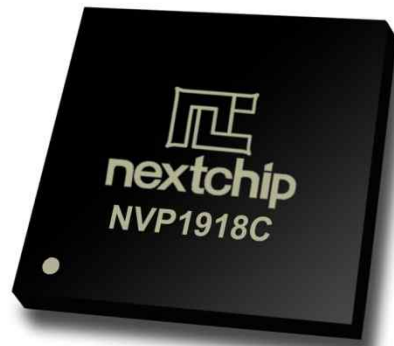


NVP1918C

8-CH 960H Video Decoders and 9-CH Audio Codecs



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2014.01.06

REV 0.0



Revision History

VERSION	DATE	DESCRIPTION	NOTE
REV 0.0	2014-01-06	- Initial Draft	

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8 CH 960H Video Decoders and 9 CH Audio Codecs

NVP1918C includes 8-Channel 720H/960H Video Decoders and 9-Channel Audio Codecs.

8-Channel 720H/960H Video Decoder delivers high quality images. It accepts separate 8 CVBS inputs from Camera, TV, DVD and the other video signal sources. It digitizes and decodes NTSC/PAL video signal into digital video components which represents 8-bit BT.1302 4:2:2 format with 36MHz or 72MHz/144MHz multiplexed. **NVP1918C** includes Clock PLL, so 72/144MHz time multiplexed function available.

9-Channel Audio Codec is 8-Channel Voice/1-Channel Mic PCM Codec which handles voice band signals(300Hz~3400Hz) with 8bit/16bit linear PCM, 8bit G.711(u-law, A-law) PCM. Built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

8-Channel Coaxial Communication Protocol communicates between controller(DVR) and camera on the video signal through coaxial cable.

Features

■ Video Decoder

- 8-Ch Video Decoder which accepts 8-CVBS
- Output in BT.656/BT1302 4:2:2 format with 27/36/54/72/108/144MHz
- Each Video Output Port 720H/960H Selectable
- On Chip Analog CLAMP/PGA and Anti-aliasing Filter
- Accepts NTSC-M/J/4.43, PAL-B/D/G/H/I/K/L/M/N/60
- Robust Sync detection for weak, non-standard signals
- High-performance 3H/5H 2D adaptive comb filter and Notch Filter
- Programmable H/V Peaking filter for Luminance
- CTI (Chrominance Transient Improvement)
- Color compensation for PAL
- IF compensation filter
- Robust No-video detection
- Programmable Brightness, Contrast, Saturation and Hue
- Programmable Picture Quality Control : GAMMA Curve extension, Universal Filter
- Internal Pattern Generator

■ Audio Codec

- 8-Ch Voice / 1-Ch Mic Record, 1-Ch Playback
- 10bit pipe-line ADC / 1* DAC
- Input / Output Analog Gain Control
- Linear PCM (8bit/16bit, 8K/16K/32K)
- G.711 a-law/u-law (8bits, 8K/16K/32K)
- Input Mixing, Digital Volume, Mute Detection & Auto Mute
- SSP/DSP/I2S Interface (Master/Slave mode)
- Cascade mode (up to 2 cascade support)
 - 16Channel recording (with 2channel mic recording), mixing output, playback

■ MISC

- Built in Clock PLL
- Single 27M Crystal for 720H/960H all video standards
- Built in 8-Ch Motion Detector
- Motion information at VBI region
- Horizontal ZOOM
- Support Coaxial Protocols up to 5C-2V(Coaxial Cable) 200M.
- Support 4-MPP Pin and IRQ Pin
- Support 2 Video Output Clocks
- Support I2C serial Interface
- 1.2V / 3.3V Supply Voltage
- 76eQFN, 9X9, 0.4p

■ Application

- Video Security System

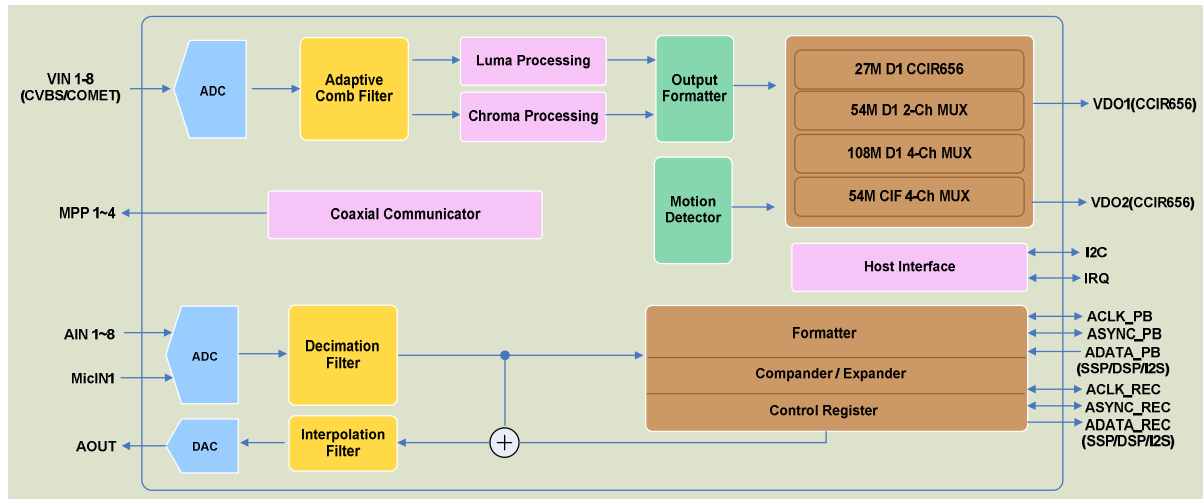
■ Ordering Information

Device	Package	Temperature Range
NVP1918C	76eQFN	0 ~ 70℃

■ Related Products

- NVC1700
- NVS3260
- HI3515/20/31

Functional Block Diagram



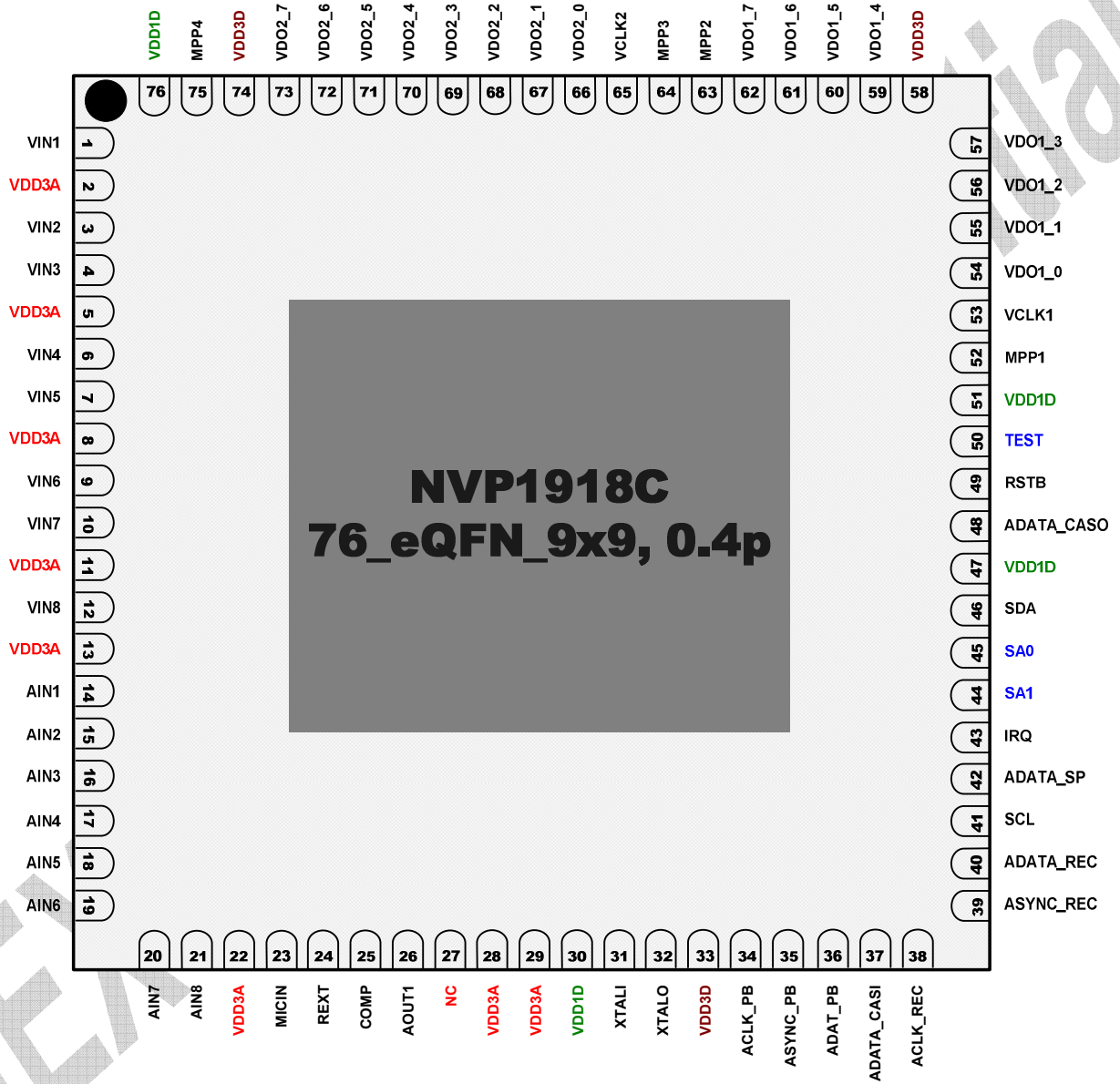
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1. Pin Information

1.1 Pin Assignments



1.2 Pin Description

Name	Pin number	Type	Descriptions
System Clock / Reset			
RSTB	49	DI	System Reset (Active low)
XTALO	32	DO	Crystal Out
XTAI	31	DI	Crystal Input (27MHz)
Analog Video Input/output Interface			
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7, VIN8	1, 3, 4, 6, 7, 9, 10, 12	AI	Analog Video Input (1 ~ 8 Respectively)
COMP	25	A	Audio DAC Compensation pin.
REXT	24	A	Audio DAC external resistor pin
Analog Audio Input/output Interface			
AIN1, AIN2, AIN3, AIN4 AIN5, AIN6, AIN7, AIN8	14, 15, 16, 17, 18, 19, 20, 21	AI	Analog Voice Input (1 ~ 8 Respectively)
MICIN	23	AI	Mic Input
AOUT	26	AO	Analog Audio Output
Digital Video Interface			
VDO1[7:0]	62, 61, 60, 59, 57, 56, 55, 54	O	Video Port 1 Output
VDO2[7:0]	73, 72, 71, 70, 69, 68, 67, 66	O	Video Port 2 Output
VCLK01, VCLK02	53, 65	O	Video Clock Output (1 ~ 2 Respectively)
ETC			
TEST	50	I	Test Pin (Connect to Ground)
IRQ	43	O	Interrupt Request Output
MPP1, MPP2, MPP3, MPP4	52, 63, 64, 75	O	Multi-Purpose Pin Output
Digital Audio Interface			
ACLK_REC	38	B	Clock for Record (M:output, S:Input)
ASYN_REC	39	B	Sync for Record(M:output, S:Input)
ADATA_REC	40	O	Audio Digital Data for Record
ADATA_SP	42	O	Audio Digital Data for Speaker
ADATA_CASO	48	O	Audio Digital Data for Cascade Output
ADATA_CASI	37	I	Audio Digital Data for Cascade Input
ACLK_PB	34	B	Clock for Playback (M:output, S:Input)
ASYN_PB	35	B	Sync for Playback (M:output, S:Input)
ADATA_PB	36	I	Audio Digital Data for Playback

Name	Pin number	Type	Descriptions
I2C Interface			
SDA	46	B	I2C Interface R/W Data
SCL	41	I	I2C Interface Clock
SA1, SA0	44, 45	I	Slave Address
No Connect			
NC	27	NC	NC
Power/Ground			
VDD1D	30, 47, 51, 76	P	Digital Power (Digital 1.2V)
VDD3D	33, 58, 74	P	Digital Power (Digital 3.3V)
VDD3A	2, 5, 8, 11, 13, 22, 28, 29	P	Analog Power (Analog 3.3V)

2. Video Decoder

NVP1918C is 8 Channel Video Decoder and delivers high quality images. It accepts separates 8 CVBS inputs from Camera, TV, or DVD and so on. It digitizes and decodes NTSC/PAL video formats into digital components video which represents 8-bit CCIR656 4:2:2 format with 36MHz, 72MHz and 144MHz multiplexed. 72/144MHz multiplexed function will be available, because It built in Clock PLL.

NVP1918C includes 8 Channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. It shows the best picture quality adopted by high performance 2D adaptive comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness and Contrast and several function such as CTI, Programmable peaking filter, PAL compensation and IF compensation filter.

2.1. Functional Overview

The role of video decoder is to separate luminance and chrominance signals from composite video signal. Figure 2.1 show the block diagram of the **NVP1918C**

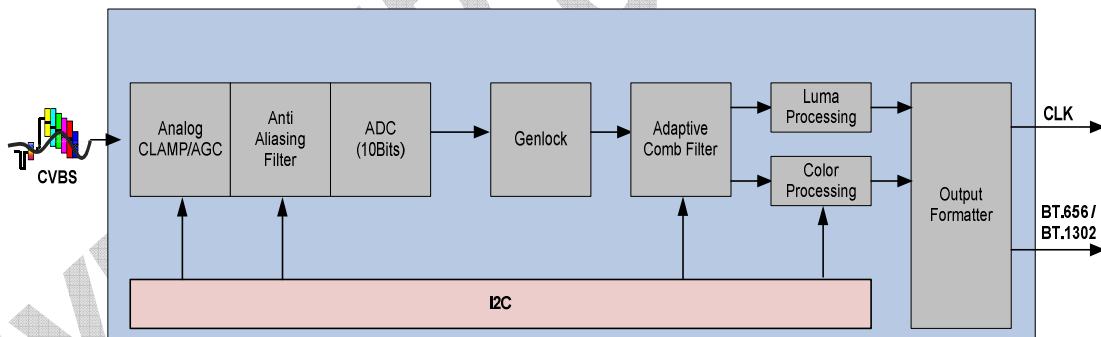


Figure 2.1. Video Decoder DATA FLOW of NVP1918C

The First step to decode composite video signals is to digitize the entire composite video signal using an A/D converter (ADC). **NVP1918C** uses the 10-bit ADC. Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic. The video signal also is low-pass filtered to about 9MHz in Anti aliasing Filter to remove any high-frequency components that may result in aliasing.

Vertical sync and horizontal sync information are recovered in Genlock block. When composite video signal is decoded, the luminance and chrominance are separated by Adaptive Comb Filter. The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, 2D Adaptive Comb Filter is used.

The chrominance demodulator in color processing block accepts modulated chrominance data from Adaptive Comb Filter which generate Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sin and cos subcarrier data.

2.2. Video Input Formats

NVP1918C supports all NTSC/PAL Video Standard. Table 2.1 show NTSC/PAL Video Standards and Register Setting Value (VIDEO_FORMAT, 0x08~0B[4:0]/0x88~8B[4:0], Bank0) to support them.

Table 2.1. NVP1918C Input Video Image Formats

VIDEO_FORMAT	FORMAT	LINE	HZ	Fsc(MHz)
0x00	NTSC-M,J	525	60	3.579545
0x11	NTSC-4.43	525	60	4.43361875
0x1D	PAL-B,D,G,H,I	625	50	4.43361875
0x16	PAL-M	525	60	3.57561149
0x1F	PAL-Nc	625	50	3.58205625
0x15	PAL-60	525	60	4.433619
<ul style="list-style-type: none"> ▪ Don't use auto-detect mode in case of NRT (Non Real Time) operation 				

2.3. Analog Front End (CLAMP, PGA, Anti-aliasing Filter)

NVP1918C includes 8 Channel Analog Processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. Because its design is dedicated for video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for **NVP1918C**. Figure 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by Register (BAND_SEL, 0x01[0], Bank3)

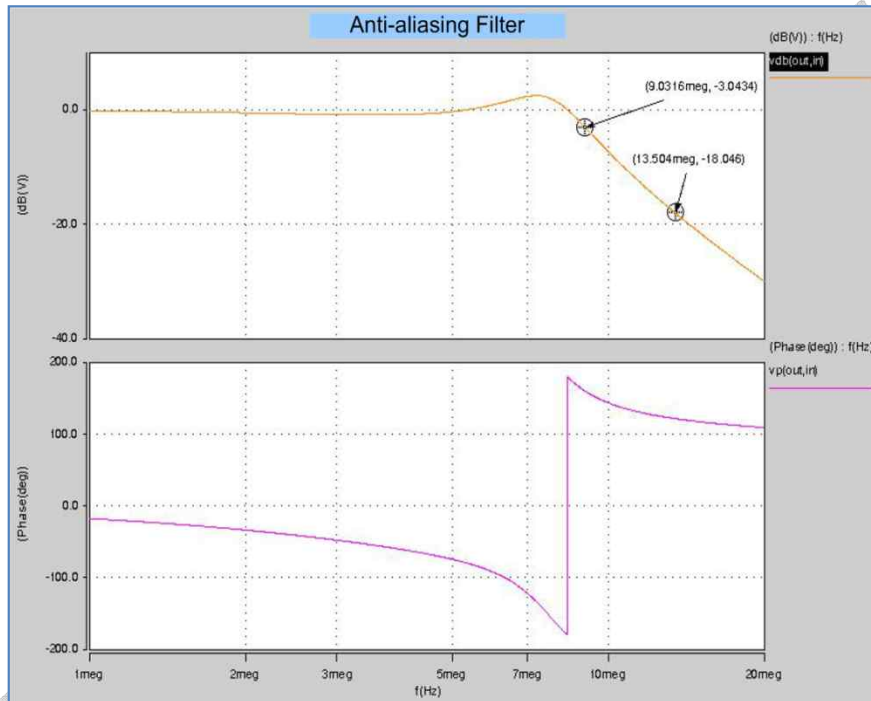


Figure 2.2. Anti-aliasing Filter characteristic

2.4. Genlock (Robust Sync Detection, Robust No-Video Detection)

NVP1918C provides a fully digital Genlocking circuitry. The digital Genlocking Circuitry use the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier.

NVP1918C uses the proprietary Genlock mechanism for video application system.

It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

2.5. Y/C separation (3H/5H Adaptive Comb Filter)

An adaptive comb filter is used to separate Y and C signal from NTSC/PAL standard video signal. Therefore, The output image is sharper and clearer compared to other video decoder. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows the Chroma BSF which is controlled by Register(BSF_MODE, 0x08~0B[6:5]/0x88~8B, Bank0).

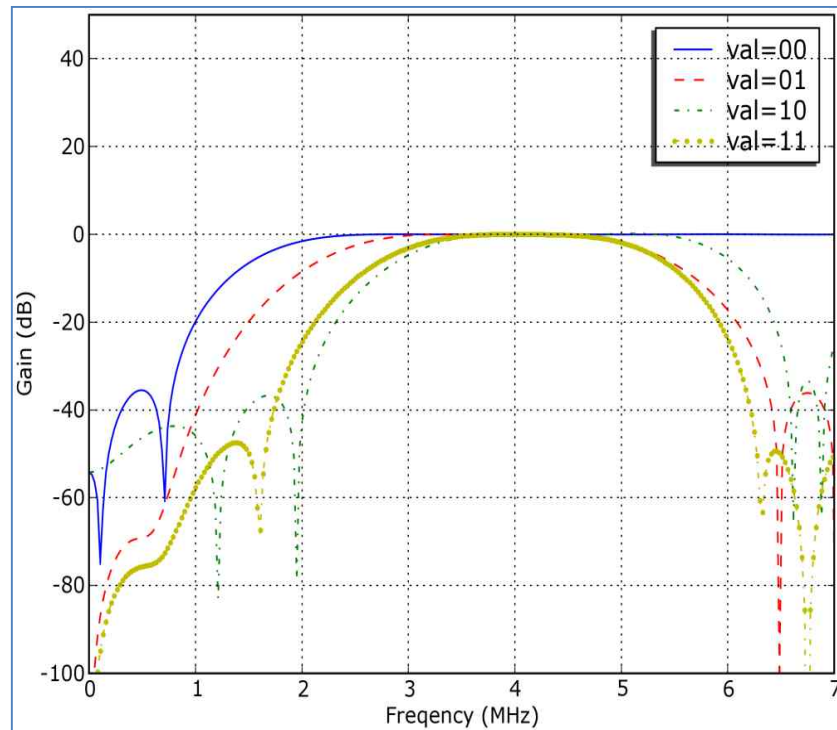


Figure 2.3. Band Split Filter Characteristic

NVP1918C can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the **NVP1918C**, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.6. Luma Processing

The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

Figure 2.4. shows Peaking Filter Characteristic. **NVP1918C** provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The Peaking filter is applied to this purpose and its characteristics can be controlled by register (Y_PEAK_MODE, 0x1A[1:0] / 0x1A[5:4] / 0x1B[1:0] / 0x1B[5:4] / 0x9A[1:0] / 0x9A[5:4] / 0x9B[1:0] / 0x9B[5:4], Bank0) via I2C interface.

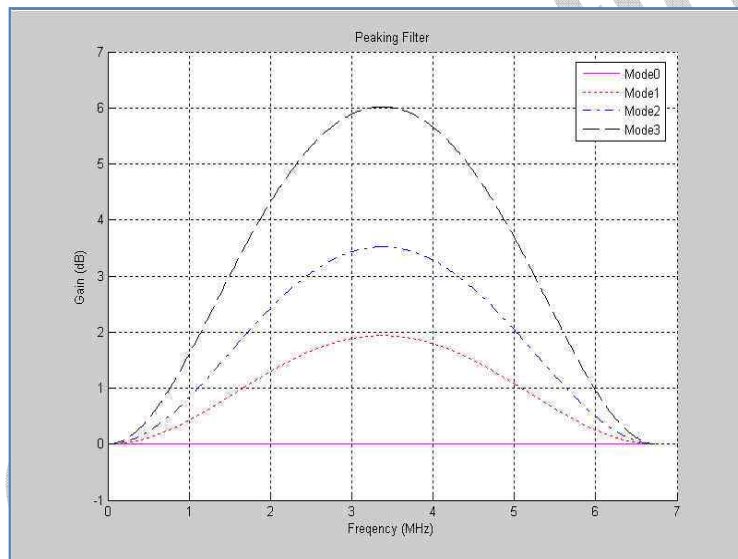


Figure 2.4. Peaking Filter Characteristic

2.7. Chroma Processing

Chroma Processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The Chroma Demodulator receives modulated chroma from YC separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6.

Users can select the chroma filter through I2C interface (CLPF_SEL, 0x35/B5[1:0], Bank0).

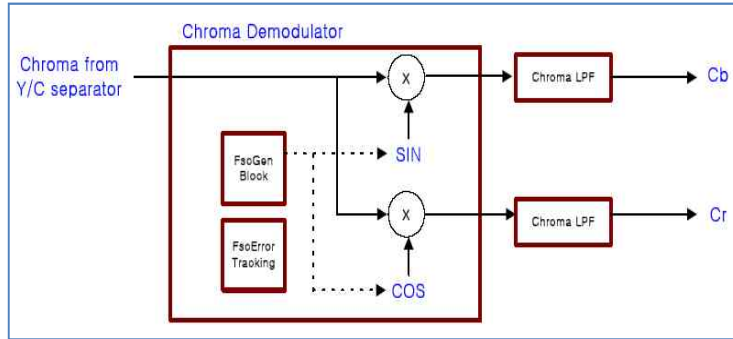


Figure 2.5. Chroma Process

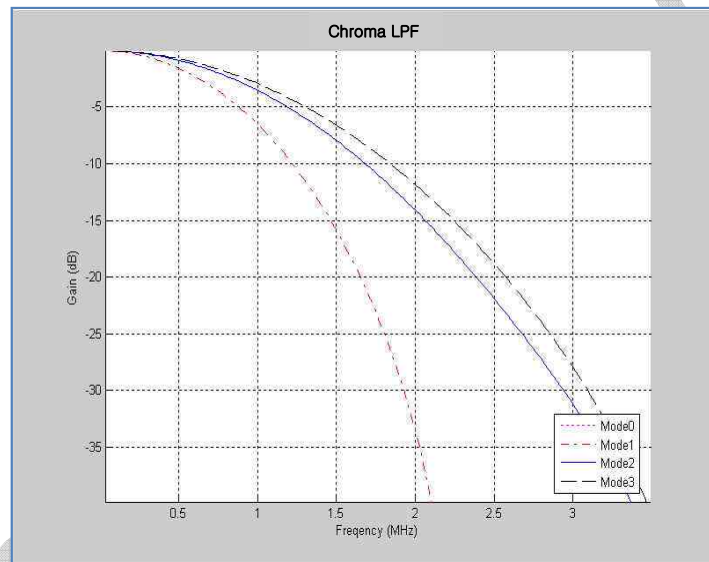


Figure 2.6. Chroma Low Pass filter Characteristic

2.8. Data Output Pin Order Control

NVP1918C can change the order of the output pin in the 36MHz/72MHz/144MHz Output Mode as shown in Table 2.2. (OUT_DATA_INV, 0xD0[1:0], Bank1)

Table 2.2. Data Output Pin Order Control

Address	state	Data Output of Port X
0xD0, OUT_DATA_INV [1]	0	VDO2 [7:0]
	1	VDO2 [0:7]
0xD0, OUT_DATA_INV [0]	0	VDO1 [7:0]
	1	VDO1 [0:7]

2.9. Output Format

NVP1918C supports a format of standard ITU-R BT.1302. Ports of 2 is synchronized by each output clock(VCLK_01~VCLK_02). Phase of clock is controlled by VCLK_SEL and VCLK_DLY_SEL of (BANK1, 0xCC~0xCD).

2.9.1. ITU-R BT.1302 Format

Codes of SAV and EAV are injected into data stream of ITU-R BT.1302 to indicate a start and a end of active. Note that a number of pixel for 1H Active line is always constant regardless of the actual incoming line length. Therefore, variance of analog input signal is applied to a blank section except codes of EAV and SAV. Figure 2.7 shows data stream of ITU-R BT.1302 format. If length of 1H of analog input signal increase or decrease, number of pixel of 'A' increase or decrease.

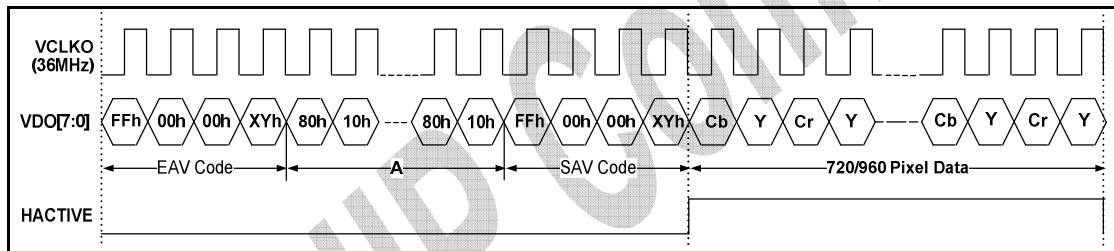


Figure 2.7. Region of active is constant

2.10. Output Mode

When it comes to the transfer of the output to the back-end device, **NVP1918C** supports all the output of 36MHz/72MHz/144MHz Data Rate.

2.10.1 36MHz 720H/960H 1-CH D1 Data Output Mode

Operated in the 36MHz D1 Data Out Mode, NVP1918C outputs VCLK01, VCLK02 and VDO1[7:0], VDO2[7:0] in the timing as shown in Figure 2.8. For VCLK01 and VCLK02 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC / CD[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC / CD[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4] / 0xC8[3:0], Bank1)

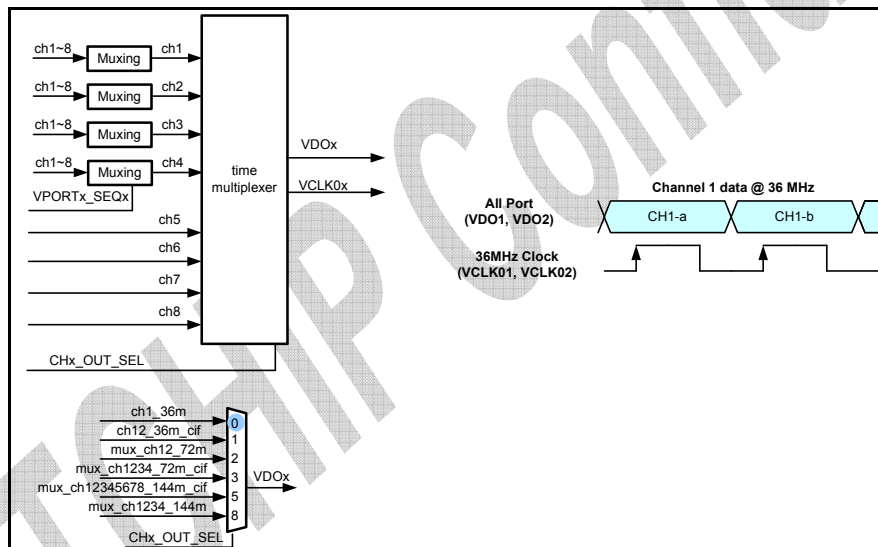


Figure 2.8. 36MHz D1 1Channel Data Output

2.10.2 72MHz 720H/960H 2-Ch D1 Data Output Mode

Operated in the 72MHz D1 Data Out Mode, **NVP1918C** outputs VCLK01, VCLK02 and VDO1[7:0], VDO2[7:0] in the timing as shown in Figure 2.9. Two channel video data stream represents 8bit BT.1302 4:2:2 format with 72MHz multiplexed. For VCLK01 and VCLK02 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC / CD[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC / CD[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4] / 0xC8[3:0], Bank1)

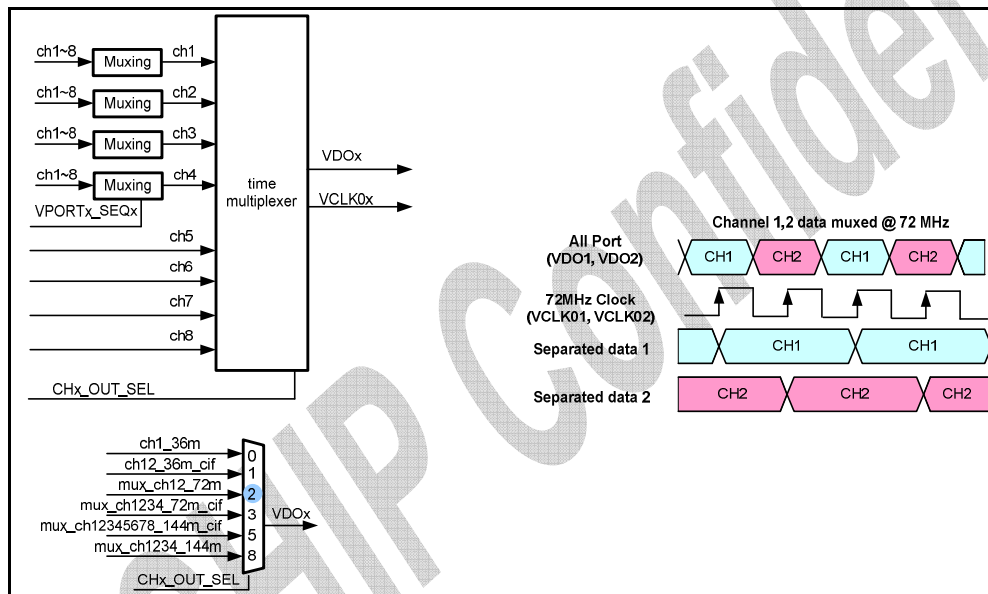


Figure 2.9. 72MHz D1 2Channel Data Output

2.10.3. 144MHz 720H/960H 4-Ch D1 Data Output Mode

Operated in the 144MHz D1 Data Out Mode, **NVP1918C** outputs VCLK01, VCLK02 and VDO1[7:0], VDO2[7:0] in the timing as shown in Figure 2.10. Four Channel Video data stream represents 8bit BT.1302 4:2:2 format with 144MHz multiplexed. For VCLK01 and VCLK02 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC / CD[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC / CD[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4] / 0xC8[3:0], Bank1)

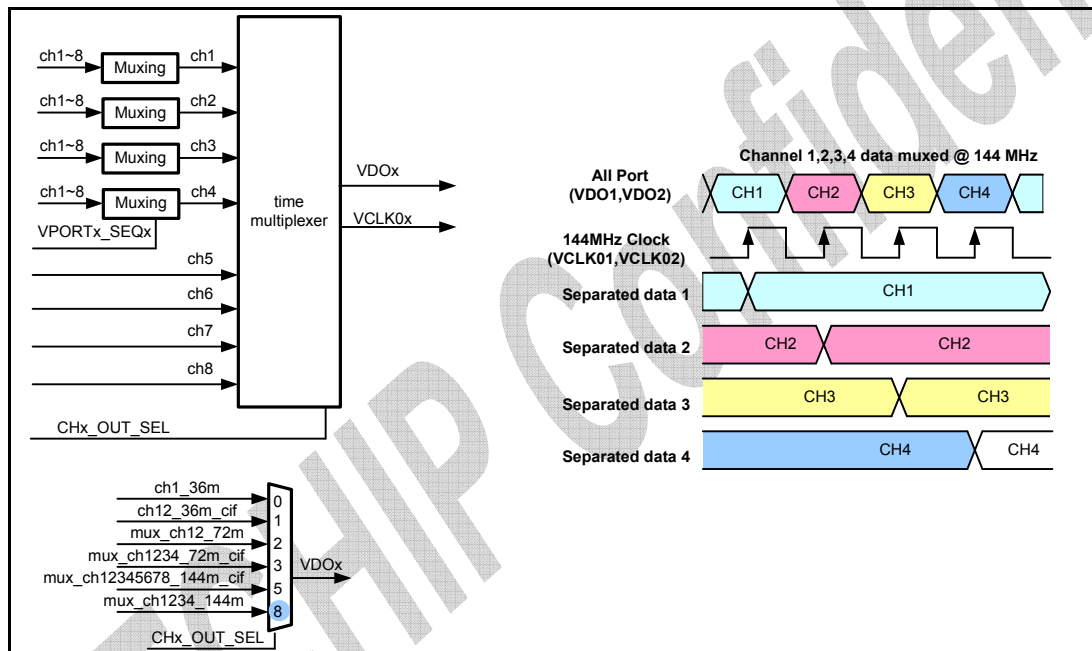
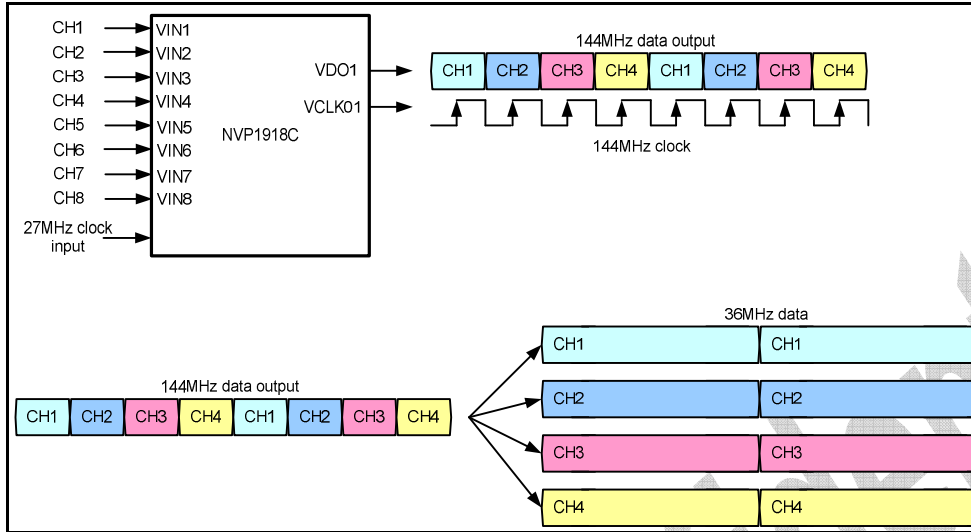


Figure 2.10. 144MHz D1 4Channel Data Output

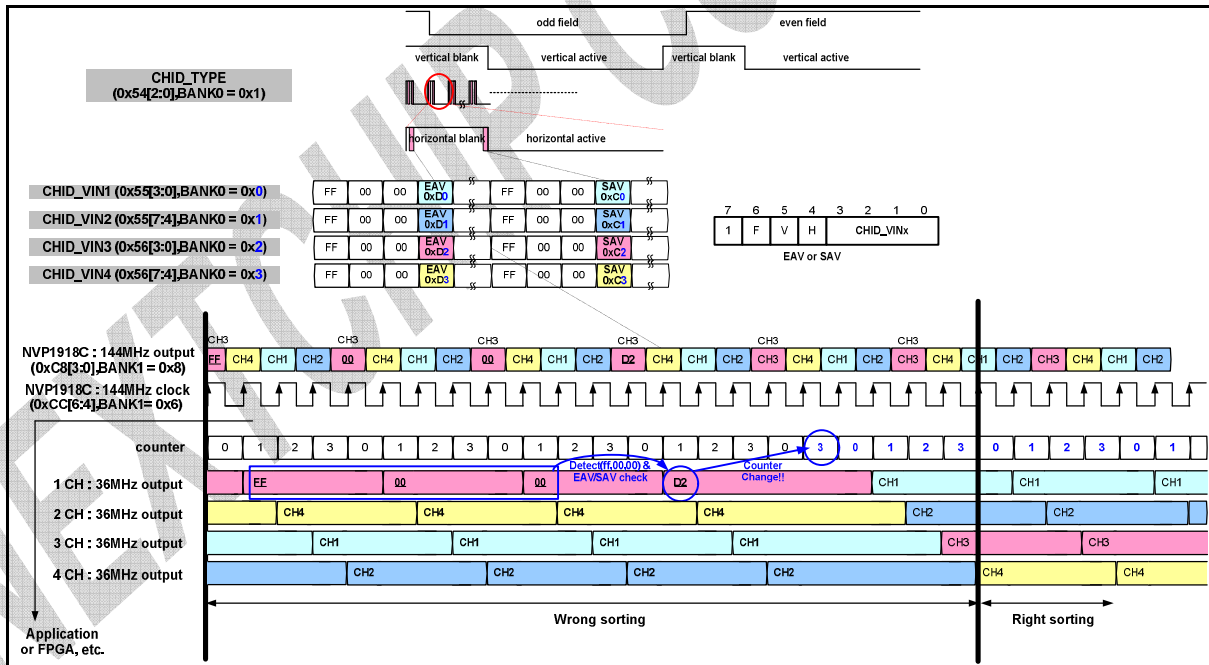
- Example of 144MHz D1 Data Output Mode with Channel ID
 1. In case of VDO1 output port and VCLK01 output clock use.
 2. Set VDO1 output(CH_OUT_SEL1, BANK1, 0xC8[3:0] = 0x8) and VCLK01 output (VCLK01_SEL, BANK1, 0xCC[6:4] = 0x6 or 0x7) .
 3. Set Channel ID Type (Refer to CHID_TYPE(0x54/D4[2:0], BANK0) Register Description)
 4. And then NVP1918C generate 144MHz clock and data output (Ex-Figure 1)

If you want to confirm the 144MHz Data using FPGA or Other device, Execute 5~11 item in next page.



Ex-figure 1

5. FPGA or equivalent devices which is input 144MHz time multiplexed data output, need to align with same channel data(36MHz 1,2,3,4 channel). EX-Figure 2 shows how to use Channel ID as a example.



Ex-Figure 2

6. CHID_TYPE(BANK0, 0x54[2:0]=001) mode described in top of Ex-Figure2

7. To generate 2bit digit, Design 2bit counter with VCLK01 (The 2bit digit means each channel).

8. Using 2bit digit, Convert from 144MHz Data to 36MHz Data (Wrong sorting part in Ex-Figure 2). and then Define the 2bit digit (**0** : 1ch data, **1** : 2ch data, **2** : 3ch data, **3** : 4ch data). namely, 144MHz data output separate only with 36MHz, 4channel data, is not align with channel data where becomes mapping in counter value.

9. For mapping between separated each channel data and specified counter value, Select channel among separated each channel(1CH selected in Ex-Figure 2).

If selected channel data become Right sorting condition, other 3 channel is sorted automatically.

10. Check the 1ch data output when 2bit counter value is only '0' and then Search the EAV/SAV[3:0] after FF 00 00 Code.

11. If the EAV/SAV[3:0] is '2', make a counter reset to '3' (Refer to Blue color in Ex-Figure 2)

12. Become Right sorting part.

2.10.4. 36MHz 2-Ch CIF Data Output Mode

Operated in the 36MHz CIF Data Out Mode, **NVP1918C** outputs VCLK01, VCLK02 and VDO1[7:0], VDO2[7:0] in the timing as shown in Figure 2.11. Two Channel CIF data stream represents 8bit BT.1302 4:2:2 format with 36MHz multiplexed.

For VCLK01 and VCLK02 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC/CD[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC/CD[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4]/0xC8[3:0], Bank1)

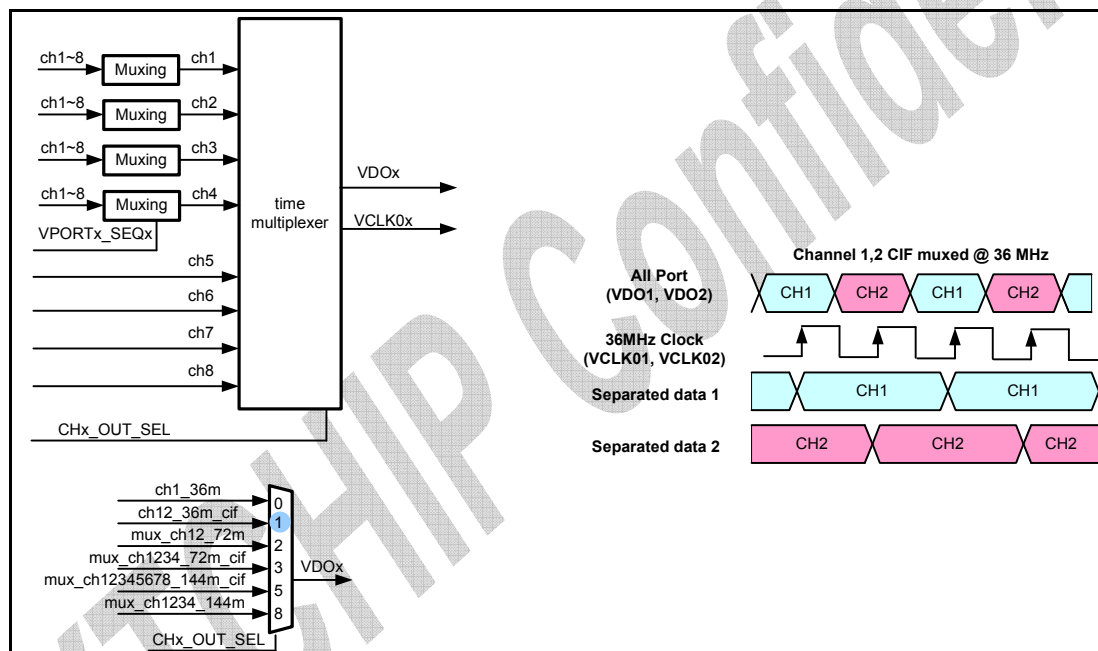


Figure 2.11. 36MHz CIF 2Channel Data Output

2.10.5. 72MHz 4-Ch CIF Data Output Mode

Operated in the 72MHz CIF Data Out Mode, **NVP1918C** outputs VCLK01, VCLK02 and VDO1[7:0], VDO2[7:0] in the timing as shown in Figure 2.12. Four Channel CIF data stream represents 8bit BT.1302 4:2:2 format with 72MHz multiplexed.

For VCLK01 and VCLK02 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC/CD[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC/CD[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4]/0xC8[3:0], Bank1)

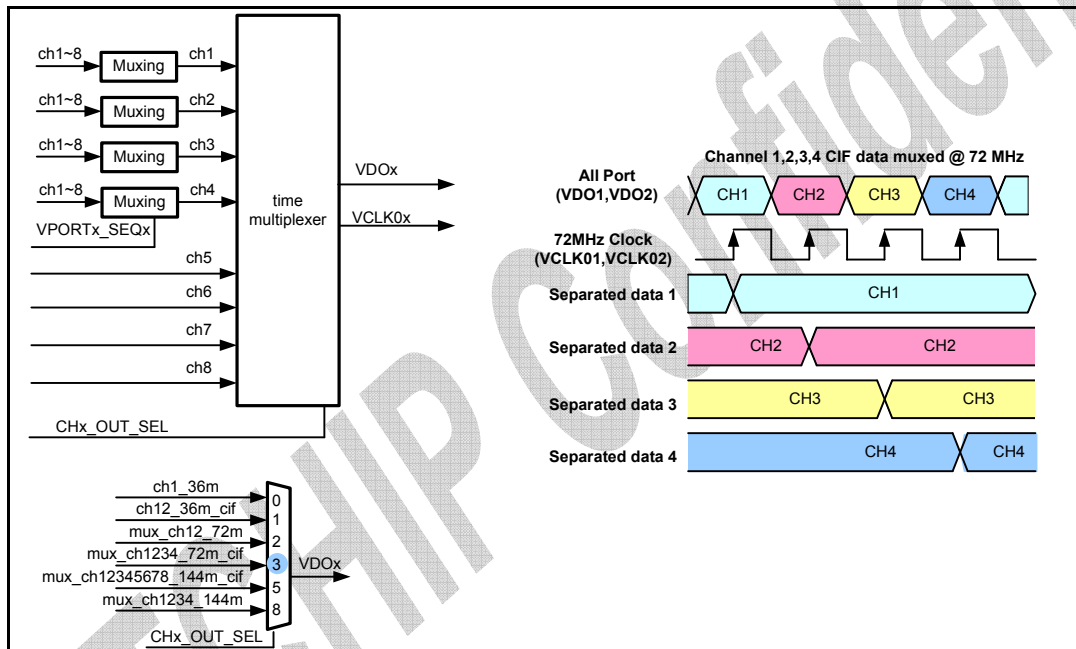


Figure 2.12 72MHz CIF 4Channel Data Output

2.10.6. 144MHz 8-Ch CIF Data Output Mode

Operated in the 144MHz CIF Data Out Mode, **NVP1918C** outputs VCLK01, VCLK02 and VDO1[7:0], VDO2[7:0] in the timing as shown in Figure 2.13. Eight Channel CIF data stream represents 8bit BT.1302 4:2:2 format with 144MHz multiplexed.

For VCLK01 and VCLK02 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC/CD[6:4], Bank1)
- (VCLK_x_DLY_SEL, 0xCC/CD[3:0], Bank1)
- (CH_OUT_SELx, 0xC8[7:4]/0xC8[3:0], Bank1)

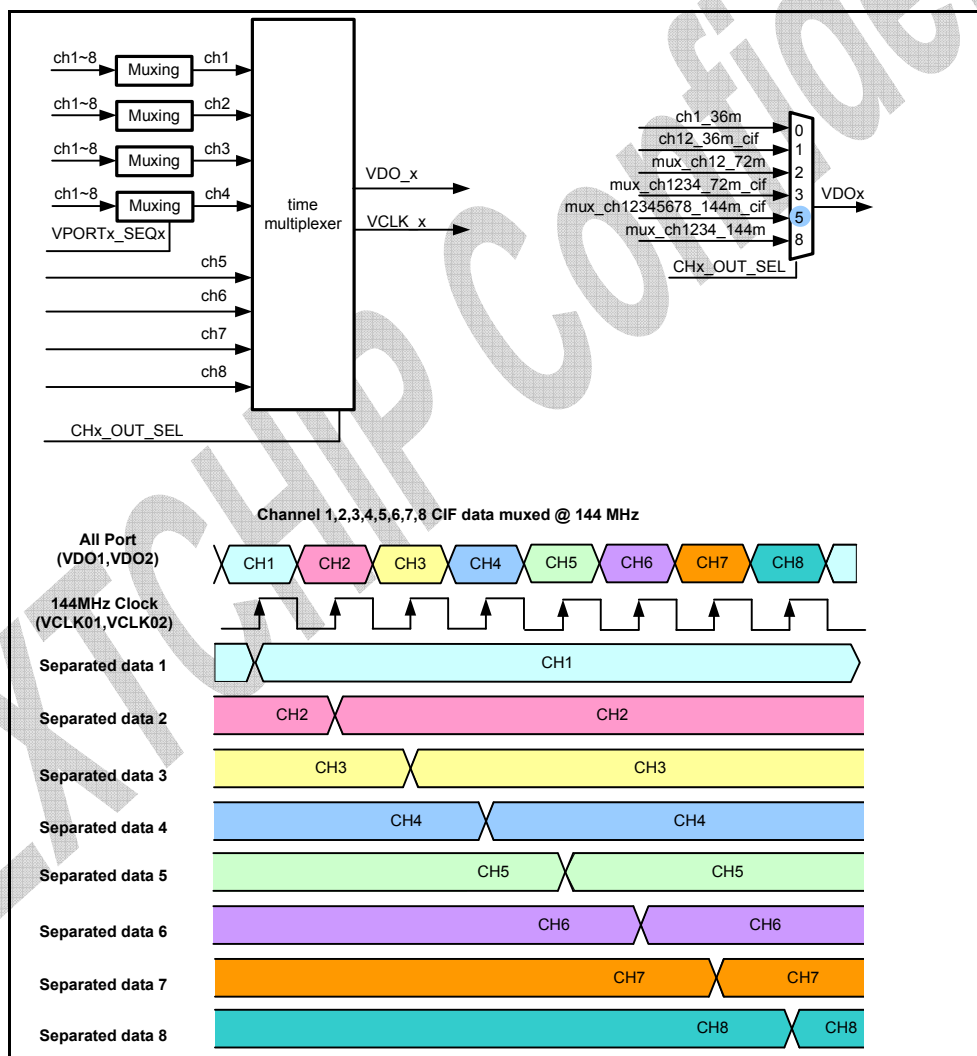


Figure 2.13. 144MHz CIF 8Channel Data Output

2.11. Motion Detector

NVP1918C supports 8 channel motion detection function. It supports the output of the detected motion information on the screen. The function allows a screen such as the one shown in Figure 2.14. to be divided in 192 sections each of which can generate information on the motion detection information.

For each section, motion detection can be controlled to be set at on/off. Once a motion is detected, the screen can be rendered dark or reversed in the unit of field to have the spot of the motion generated to be indicated in the screen.

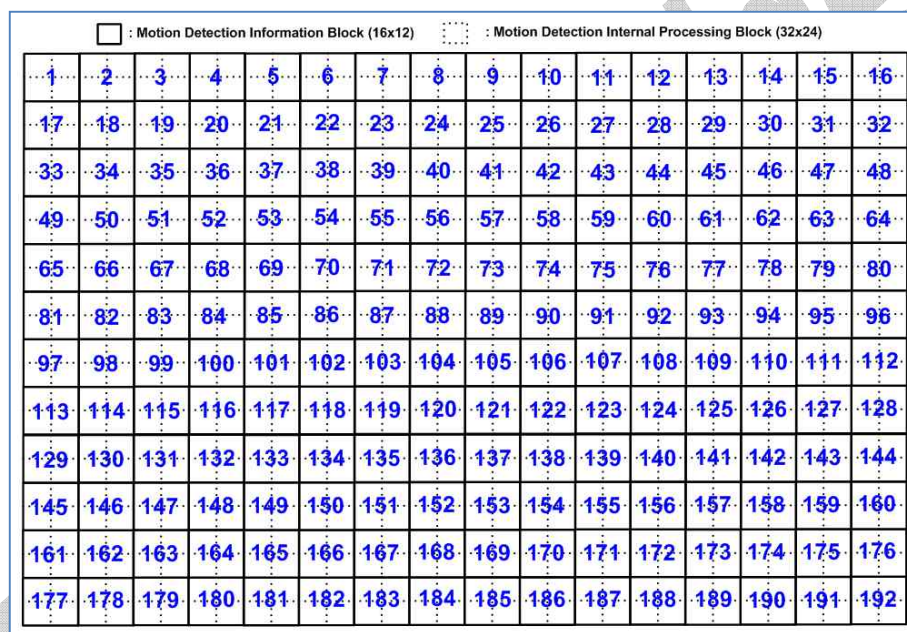


Figure 2.14. Motion Block Mapping

2.11.1. How to Operate the Motion Detection Function

- 1). Set the Motion detection On (Bank2, 0x00/02/04/06/08/0A/0C/0E[4]) - Set at low
- 2). Set the area for which to detect motion
 - : The screen is divided into 192 sections and each section is matched one to one.
 - (BANK2, 0x20~0x37 - Channel 1, Bank2, 0x38~4F - Channel 2)
 - (BANK2, 0x50~0x67 - Channel 3, Bank2, 0x68~7F - Channel 4)
 - (BANK2, 0x80~0x97 - Channel 5, Bank2, 0x98~AF - Channel 6)
 - (BANK2, 0xB0~0xC7 - Channel 7, Bank2, 0xC8~DF - Channel 8)
- 3). Set the motion sensitivity 1 (Pixel Sensitivity: Set at BANK2, 0x10/11)

4). Set the motion sensitivity 2 (Temporal Sensitivity : Set at BANK2 0x01/03/05/07/09/0B/0D/0F)
: When setting motion sensitivity, it is recommended to set the pixel sensitivity at "0x60" and use the temporal sensitivity to send the sensitivity to situation.

5). Output of Motion Detection

: Motion information generated from each section is not to be generated separately through data interface. In other words, the motion information needs to be confirmed in the register or It is not included in the BT.1302 data.

: Motion information generated from each area can be displayed on the screen.

Display can be done through three approaches. This can be controlled using MOTION_PIC (BANK2, 0x00/02/04/06/08/0A/0C/0E[1:0]).

3. Audio Codec

3.1. Description

NVP1918C outputs PCM digital audio signals converted from analog audio input signals and analog audio signals converted from PCM digital audio signals. **NVP1918C** has 9 channel ADCs and 1 channel DAC for audio signals.

Voice data convert to G.711 PCM and Linear PCM data, and these converted data is outputted via DSP/SSP/I2S interfaces. The output data will be saved at hard disk or any other storages. This process - to convert and save audio data into storage - is usually called as "Record Output".

The saved audio data is inputted to **NVP1918C** via DSP/SSP/I2S interfaces. The input audio data is outputted via audio DAC. This process is named as "Playback Output".

NVP1918C selects one audio input signal among 9 analog audio inputs(8-Ch voice/1-Ch mic) and this audio is outputted through audio ADC and audio DAC. And it also supports directly mixed audio output signal which 9 analog audio inputs are mixed. This function usually is called by "Live Output".

In addition, **NVP1918C** supports audio mute detection and cascade function up to 2 chips - 18 audio channels(16-Ch voice/2-Ch mic)

3.2. Record Output

Analog audio data is converted to PCM data and this data is outputted to the other **NVP1918C** or other IC via DSP/SSP/I2S interfaces. Record output is useful function to save compressed audio data into storage. Analog audio signal is finally outputted to ADATA_REC pin used for data of each channel and ADATA_SP pin used for one mixed signal of each channel's data. The output data from ADATA_SP pin is either same data of ADATA_REC pin or mixed signal of each channel's data.

PCM data is categorized based on sampling frequency, sampling data bit width and PCM method. G.711 (A-law/Mu-law), unsigned linear PCM and linear PCM are supported. 8KHz / 16KHz and 8bit/16bit are used for sampling frequency and sampling data bit width, respectively. Refer the following table when you set the register value.

Table 3.1. Sampling & PCM coding setting

	BANK1											
	8K/8bit		8K/16bit		16K/8bit		16K/16bit		32K/8bit		32K/16bit	
	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE
Linear PCM	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00
Unsigned Linear PCM	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01
G.711 U-law	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10
	0x08[6]	0	0x08[6]	0	0x08[6]	0	0x08[6]	0	0x08[6]	0	0x08[6]	0
G.711 A-law	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10
	0x08[6]	1	0x08[6]	1	0x08[6]	1	0x08[6]	1	0x08[6]	1	0x08[6]	1

DSP / SSP / I2S interfaces are supported as output data format. In addition, slave mode and master mode are also supported. At slave mode, input clock and synchronized signal come from external ICs, however Master mode generates clock and synchronized signal in itself.

3.2.1 Data Output Interface

NVP1918C outputs "Record Output" using ACLK_REC, ASYNC_REC, ADATA_REC and DATA_SP. ACLK_REC is a reference clock signal for Record Output Data and ASYNC_REC is a reference synchronization signal for Record Output Data. ADATA_REC and ADATA_SP are synchronized Record Output, data with reference clock and reference synchronized signal.

Table 3.2 Record Output Interface configuration

	BANK1					
	DSP		SSP		I2S	
	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE
Master	0x07[0]	1	0x07[0]	1	0x07[0]	0
	0x07[1]	0	0x07[1]	1	0x07[1]	0
	0x07[7]	1	0x07[7]	1	0x07[7]	1
Slave	0x07[0]	1	0x07[0]	1	0x07[0]	0
	0x07[1]	0	0x07[1]	1	0x07[1]	0
	0x07[7]	0	0x07[7]	0	0x07[7]	0

ACLK_REC is a reference clock of Record Output Data and ASYNC_REC is reference synchronized signal. ACLK_REC and ASYNC_REC signal support slave mode accepted external signals and master mode generating clock and synchronization signal in itself. And

DSP/SSP/I2S interfaces are supported by configuration of these pins defined by internal register setting value.

Figure 3.1, 3.2, 3.3 shows timing diagram of I2S, DSP, and SSP mode, respectively.

These figures show timing relation among ASYNC_REC, ACLK_REC and ADATA_REC, and ADATA_SP is outputted using same interface method of ADATA_REC. Polarity of ACLK_REC clock is changed by setting of internal register value (RM_CLK, 0x07[6], BANK1).

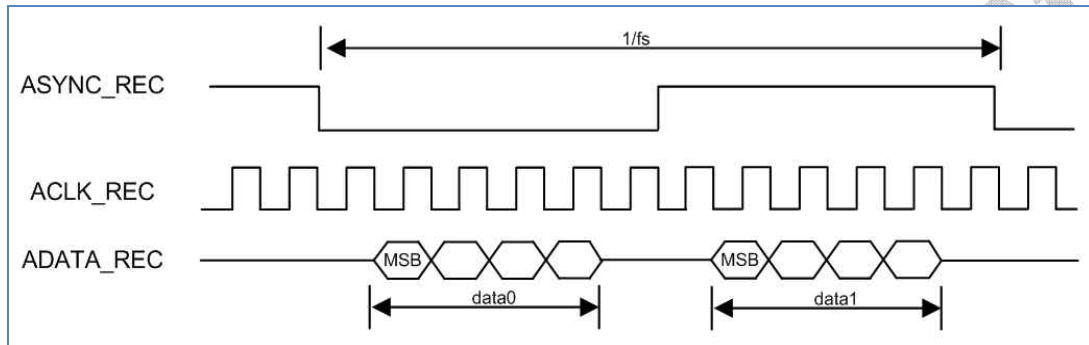


Figure 3.1 I2S mode

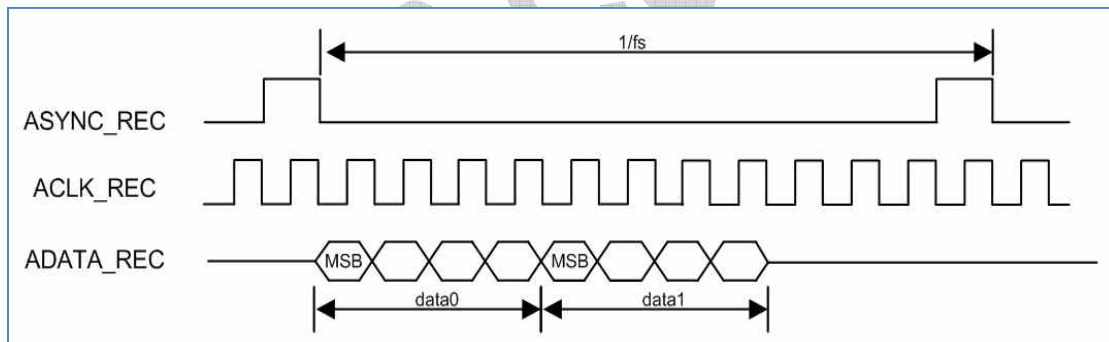


Figure 3.2 DSP mode

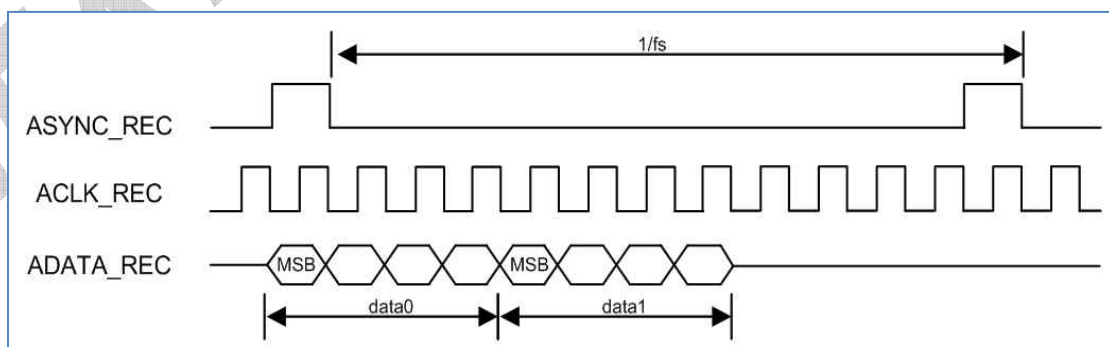


Figure 3.3 SSP mode

3.2.2. 2/4/8/16-Channel Data Output(256 fs)

ADATAR_REC supports up to 8 channel audio(8-Ch voice) using single chip and up to 16 channel(16-Ch voice) in cascade mode. In this case, the bitrate of the audio signal should be 256 fs(RM_BITRATE, 0x07[5:4], BANK1). The number of output channel is configured by internal register value (R_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R_SEQ, 0x09 ~ 0x12, / MIC_SEQ, 0x3C ~ 0x3D, BANK1). Therefore, the order of audio output can be changed.

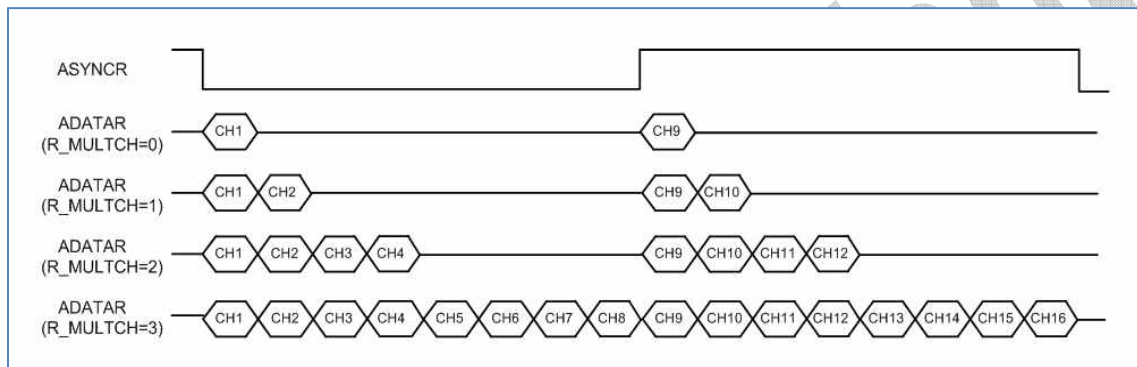


Figure 3.4. audio 2/4/8/16 channel data output <I2S mode, 256fs>

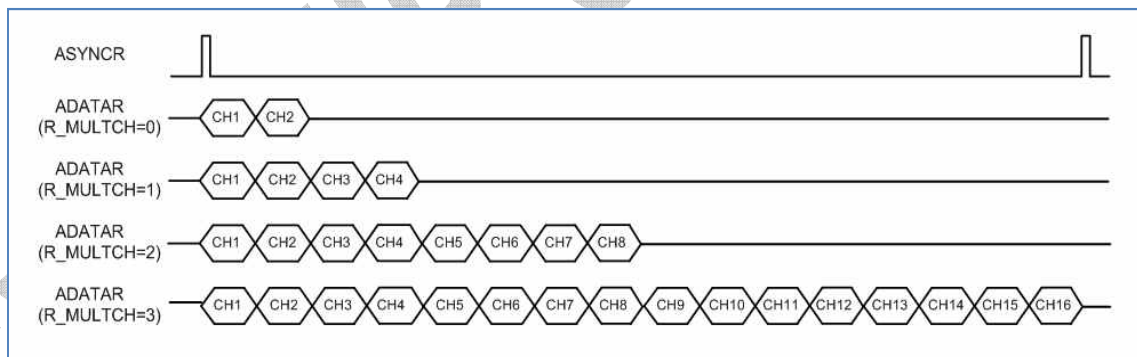


Figure 3.5. audio 2/4/8/16channel data output <DSP/SSP mode, 256fs>

3.2.3. 2/4/8/16-Channel Voice Data Output with 4-Channel Mic Data(320 fs)

ADATAR_REC supports up to 9 channel audio(8-Ch voice/1-Ch mic) using single chip and up to 18 channel(16-Ch voice/2-Ch mic) in cascade mode. In this case, the bitrate of the audio signal should be 320 fs(RM_BITRATE, 0x07[5:4], BANK1).

The number of output channel is configured by internal register value (R_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R_SEQ, 0x09 ~ 0x12, / MIC_SEQ, 0x3C ~ 0x3D, BANK1). Therefore, the order of audio output can be changed.

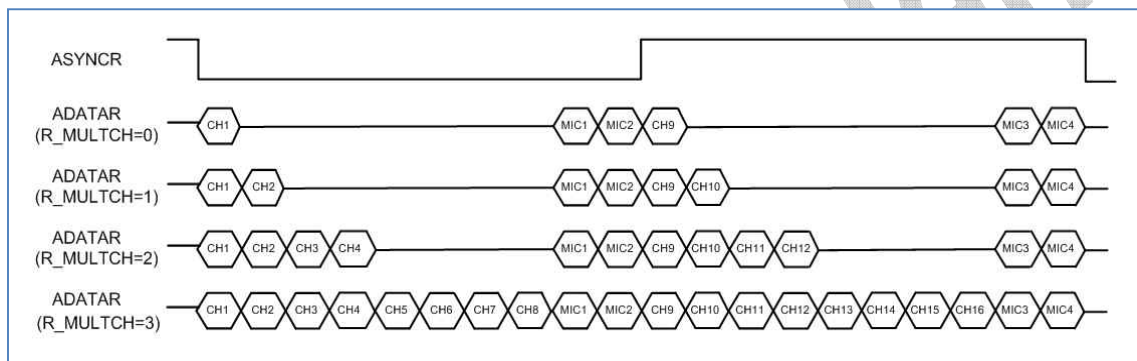


Figure 3.6 audio 2/4/6/8/16 channel data output(with 4 channel mic) <I2S mode, 320fs>

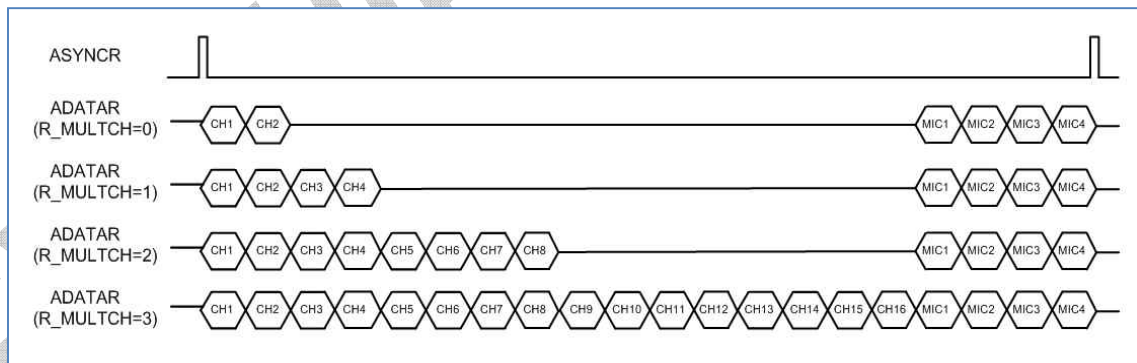


Figure 3.7. audio 2/4/8/16 channel data output(with 4 channel mic) <DSP/SSP mode, 320fs>

3.2.4. ADATA_SP Output

ADATA_SP supports 3 kinds of output method. Firstly, the output data of ADATA_SP pin is the exactly same as those of ADATA_REC except output data sequence. The order of output data is opposite. If the output data order of ADATA_REC is "CH1, CH2, CH9, CH10", the output data order of ADATA_SP is "CH16, CH15, CH8, CH7". That is to say, two output pin - ADATA_SP and ADATA_REC are complement relationship. Secondly, one of input signals is selected as output signal of ADATA_SP. The selectable input signal ranges from analog input signal to ADATA_PB signal. Lastly, mixed data of input signal is selected as the output signal of ADATA_SP. The mixing gain of each channel's input signal is determined by internal register setting value (MIX_RATIO, 0x16 ~ 0x21[7:0], BANK1).

The output configuration of ADATA_SP is determined by internal register setting. First and second configuration are determined by (R_ADATSP, 0x08[2], BANK1), and second and third configuration are determined by (L_CH_OUTSEL, 0x24[4:0], BANK1) and (R_CH_OUTSEL, 0x25[4:0], BANK1). In this case, L_CH_OUTSEL and R_CH_OUTSEL select one of input channels or mixed data.

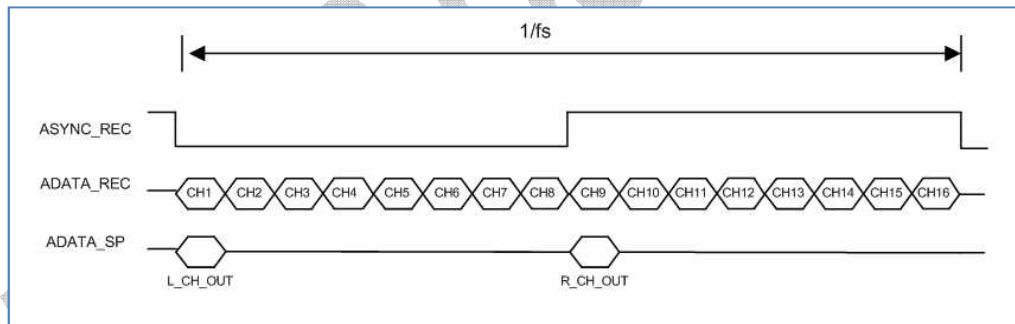


Figure 3.8 ADATA_SP Output <I2S mode>

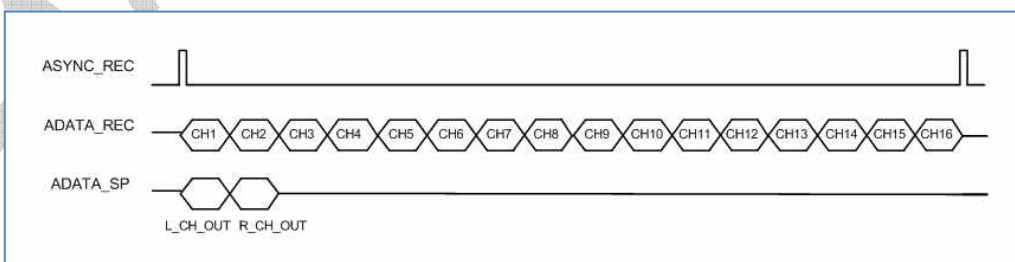


Figure 3.9 ADATA_SP Output <DSP/SSP mode>

3.3. Playback Output

Playback is to output stored audio data to external device through DAC after internal processing.

NVP1918C gives and takes a clock and synchronization signal through ACLK_PB and ASYNC_PB pin. In this case, interface is the exactly same as Record data's interface. When multi-channel audio is supported, selective playback for intended channel is enable using register setting (PB_SER, 0x14[4:0], BANK1). In case of single channel, PB_SEL should be set to "00000".

ACLK_PB and ASYNC_PB supports Master mode and Slave mode. In master mode, ACLK_PB and ASYNC_PB are outputted by **NVP1918C**, and clock and synchronization signal come from external devices at slave mode. Master/Slave mode is selected by setting internal register (PB_MASTER, 0x13[7], BANK1).

ADATA_PB accepts an audio data synchronized with ACLK_PB and ASYNC_PB. ACLK_PB and ASYNCP accept I2S/DSP/SSP mode input and output, and I2S and DSP mode is set by internal register value (PB_SYNC, 0x13[0], BANK1). When DSP mode is selected, DSP/SSP mode is set by (PB_SSP, 0x13[1], BANK1). The relation of clock, synchronized signal and data are the exactly same as that of record/mix output. PB_CLK can be inverted for all modes using setting of register(PB_CLK, 0x13[6], BANK1).

3.4. Audio Detection

NVP1918C has an audio mute detection block for individual 9 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the ADET_MODE(0x29[3], BANK1) and ADET_FILT (0x29[2:0], BANK1) register, and the detecting threshold values are defined by ADET_TH register(0x2C ~ 0x30, BANK1). According to this control bits and its result (audio detected), Interrupt is generated through the interrupt pins.

3.5. Cascade Operation

NVP1918C supports cascade mode. Maximum 2 NVP1918C chips can be connected together for cascade mode and can be processed 18 channel audio encoding data(16-Ch voice/2-Ch mic). Cascade is enabled by setting register(CHIP_STAGE, 0x06[1:0], BANK1). Figure 3.10 shows how to connect NVP1918C for the cascade mode. In this case, analog audio AOUT1 is assigned to AIN1-16 and MICIN1-2. 1 channel audio or all channel mixed audio signal is selected as output signal set by MIX_OUTSEL(0x23[4:0], BANK1).

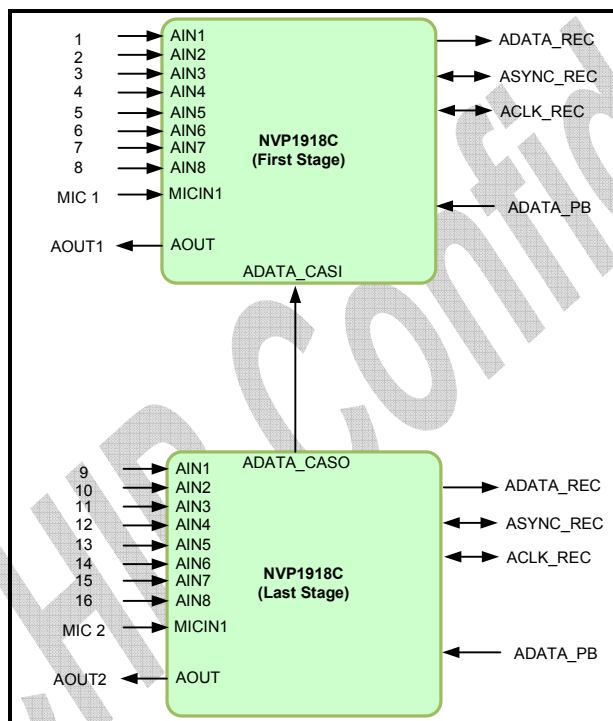


Figure 3. 10. NVP1918C & NVP1918C Cascade mode

4. Coaxial Protocol

NVP1918C includes Coaxial Protocol generator that sends control signal from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal. NVP1918C supports Pelco Protocol up to 5C-2V(coaxial cable) 200M. It depends on Coaxial Cable impedance characteristic. This document presents the concept of Coaxial Protocol. Coaxitron is Pelco's name for a method of sending control signaling from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal (Known as "Up The Coax" or "UTC").

There are two types of Coaxitron command structures. One type, Standard Coaxitron, is a series of 15 pulses, or data bits, that are sent within video line 18 of a video field. The other type, Extended Coaxitron, is a series of 32 pulses, where 16 pulses are sent in line 18 and 16 pulses in line 19 of a video field. Refer to Figure 4.1. No pulses are sent when the system is in an idle state

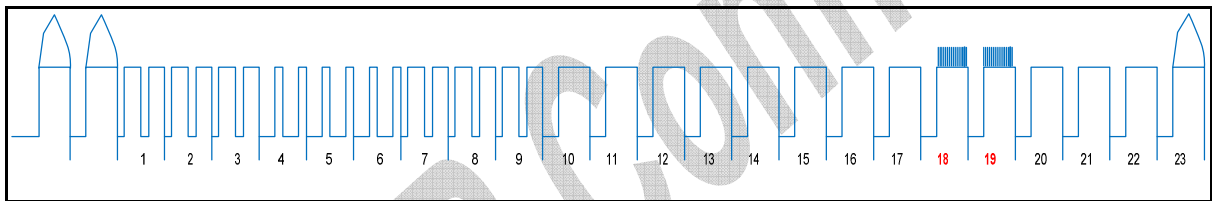


Figure 4.1. Coaxitron Active line

Coaxitron is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 2us pulse represents a one(1) and a 1us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 4.2. and Figure 4.3.

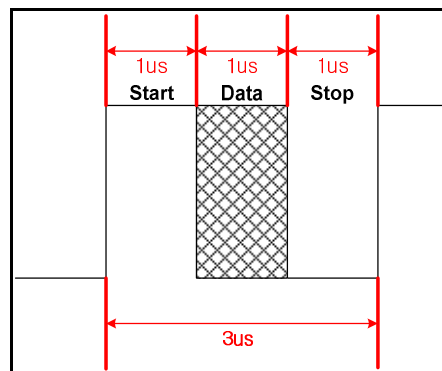


Figure 4.2. Description of One Coaxitron Bit

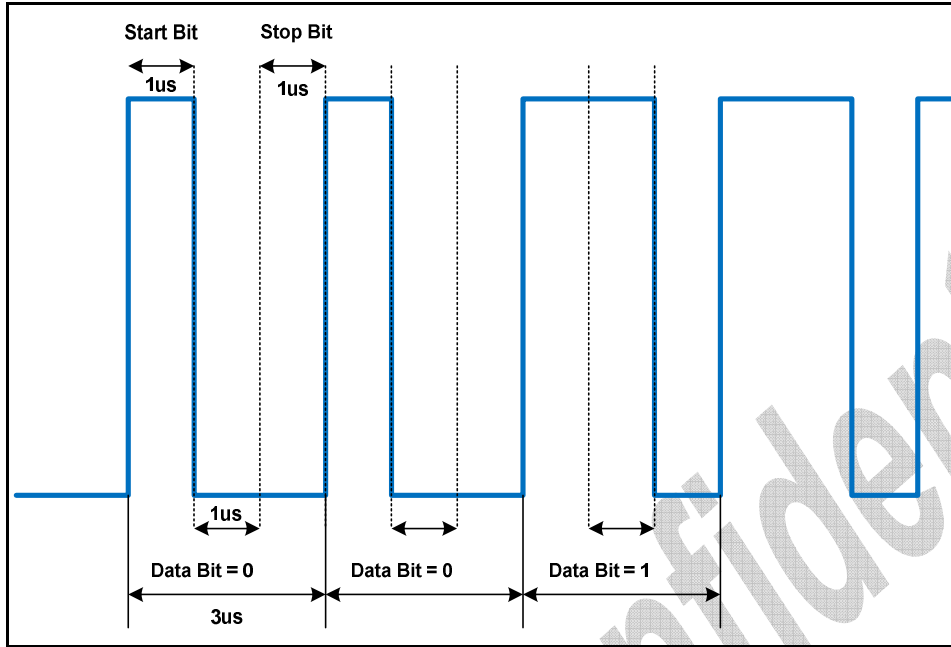


Figure 4.3. Coaxitron Bit Timing

NVP1918C is able to control coaxitron timing format on the video signal. Start Active line of Coaxitron (BL_TXST_01,0x53, BANK1) is 18th line on VBI. Pulse width of Coaxitron (BAUD, 0x52, BANK1) is fixed 1us. The size of Coaxial Data (PELCO_TXDAT_01~04, 0x70 ~ 0x73, BANK1) is 4 bytes. Refer to Figure 4.4.

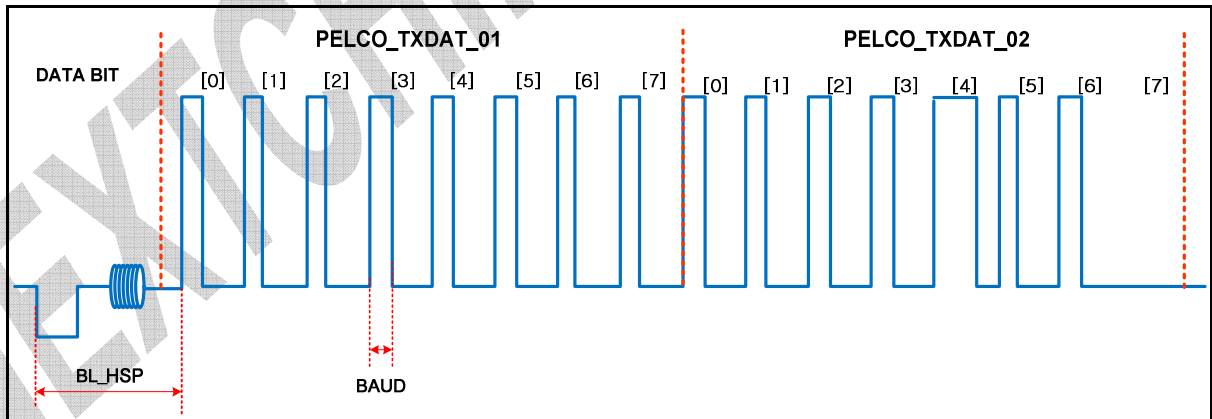


Figure 4.4. Data Structure of Coaxitron Origins (VBI 18th)

5. I2C Interface

I2C interface requires 2 wires, SCL (I2C clock) & SDA (I2C R/W data). **NVP1918C** provides special device ID as slave addresses (SA0, SA1). So any combination of 7 bit can be defined as slave address of **NVP1918C**. The Figure 5.1 shows read/write protocol of I2C interface. The 1st byte transfers slave address and read/write information. For write mode, the 2nd byte transfers base register index and the 3rd byte transfers data to be written.

For read mode, reading data is transferred during 2nd byte period. The brief I2C interface protocol is shown in Figure 5.2.

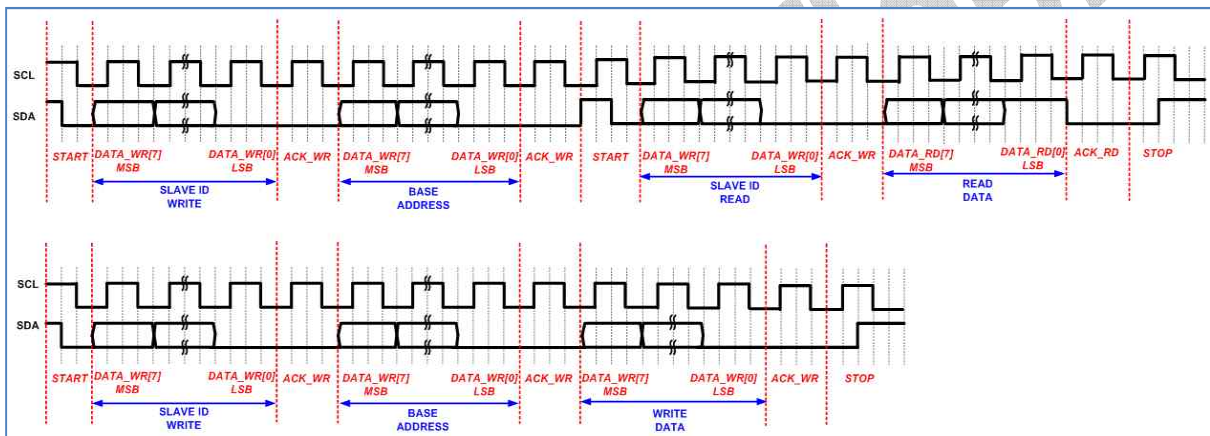


Figure 5.1. I2C Timing Diagram

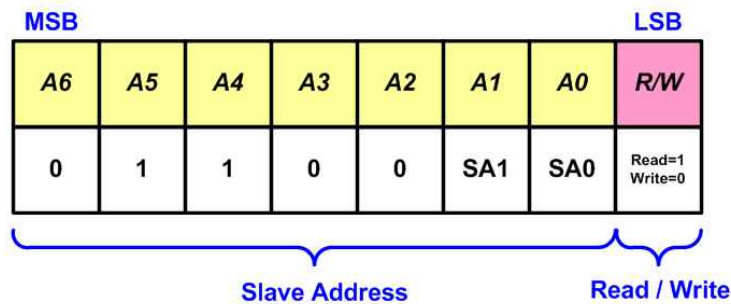


Figure 5.2. I2C Slave Address Configuration

6. Register Description

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
0x00	-RESERVED-								0x00	0x00	0x00	
0x01	-RESERVED-								0x00	0x00	0x00	
0x02	PD_ADAC	-RESERVED-			PD_VCH4	PD_VCH3	PD_VCH2	PD_VCH1	0x00	0x20	0x20	
0x03	-RESERVED-								0x00	0x00	0x00	
0x04	-RESERVED-								0x00	0x00	0x00	
0x05	-RESERVED-								0x00	0x00	0x00	
0x06	-RESERVED-								0xAF	0xAF	0xAF	
0x07	-								-	-	-	
0x08	AUTO_1	BSF_MODE_1		VIDEO_FORMAT_1				0xDD	0xA0	0xDD		
0x09	AUTO_2	BSF_MODE_2		VIDEO_FORMAT_2				0xDD	0xA0	0xDD		
0x0A	AUTO_3	BSF_MODE_3		VIDEO_FORMAT_3				0xDD	0xA0	0xDD		
0x0B	AUTO_4	BSF_MODE_4		VIDEO_FORMAT_4				0xDD	0xA0	0xDD		
B A N	0x0C	BRIGHTNESS_1								0xF8	0xFE	0xF8
	0x0D	BRIGHTNESS_2								0xF8	0xFE	0xF8
	0x0E	BRIGHTNESS_3								0xF8	0xFE	0xF8
	0x0F	BRIGHTNESS_4								0xF8	0xFE	0xF8
K O	0x10	CONTRAST_1								0x80	0x88	0x80
	0x11	CONTRAST_2								0x80	0x88	0x80
	0x12	CONTRAST_3								0x80	0x88	0x80
	0x13	CONTRAST_4								0x80	0x88	0x80
0x14	H_SHARPNESS_1				V_SHARPNESS_1				0x80	0x80	0x80	
0x15	H_SHARPNESS_2				V_SHARPNESS_2				0x80	0x80	0x80	
0x16	H_SHARPNESS_3				V_SHARPNESS_3				0x80	0x80	0x80	
0x17	H_SHARPNESS_4				V_SHARPNESS_4				0x80	0x80	0x80	
0x18	Y_FIR_MODE_2				Y_FIR_MODE_1				0x77	0x88	0x88	
0x19	Y_FIR_MODE_4				Y_FIR_MODE_3				0x77	0x88	0x88	
0x1A	Y_PEAK_MODE_2				Y_PEAK_MODE_1				0x11	0x11	0x11	
0x1B	Y_PEAK_MODE_4				Y_PEAK_MODE_3				0x11	0x11	0x11	
0x1C	-RESERVED-	PED_ON_1	-RESERVED-					0xA2	0xA4	0xA2		
0x1D	-RESERVED-	PED_ON_2	-RESERVED-					0xA2	0xA4	0xA2		
0x1E	-RESERVED-	PED_ON_3	-RESERVED-					0xA2	0xA4	0xA2		
0x1F	-RESERVED-	PED_ON_4	-RESERVED-					0xA2	0xA4	0xA2		

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
B	0x20				-						
	0x21				-						
	0x22				-						
	0x23				-						
	0x24				-						
	0x25				-						
	0x26				-						
	0x27				-						
	0x28				-						
	0x29				-						
	0x2A				-						
	0x2B				-						
	0x2C				-						
	0x2D				-						
A	0x2E				-						
	0x2F				-						
N	0x30		-RESERVED-				Y_DELAY_1		0x13	0x13	0x13
K	0x31		-RESERVED-				Y_DELAY_2		0x13	0x13	0x13
O	0x32		-RESERVED-				Y_DELAY_3		0x13	0x13	0x13
	0x33		-RESERVED-				Y_DELAY_4		0x13	0x13	0x13
	0x34	ACC_OFF_14		-RESERVED-			ACC_GAIN_SPD_14		0x2F	0x2F	0x2F
	0x35	PAL_CM_OFF_14		IF_FIR_SEL_14			CLPF_SEL_14		0x02	0x82	0x02
	0x36	COLOROFF_4	COLOROFF_3	COLOROFF_2	COLOROFF_1		C_KILL_14		0x0B	0x0B	0x0B
	0x37	FLD_DET_MODE_14		-RESERVED-			NOVID_DET_B_14		0x43	0x43	0x43
	0x38					CTI_GAIN_1			0x0A	0x0A	0x0A
	0x39					CTI_GAIN_2			0x0A	0x0A	0x0A
	0x3A					CTI_GAIN_3			0x0A	0x0A	0x0A
	0x3B					CTI_GAIN_4			0x0A	0x0A	0x0A
	0x3C					SATURATION_1			0x80	0x80	0x80
	0x3D					SATURATION_2			0x80	0x80	0x80
	0x3E					SATURATION_3			0x80	0x80	0x80
	0x3F					SATURATION_4			0x80	0x80	0x80

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
B A N K 0	0x40	HUE_1							0x00	0x01	0x00
	0x41	HUE_2							0x00	0x01	0x00
	0x42	HUE_3							0x00	0x01	0x00
	0x43	HUE_4							0x00	0x01	0x00
	0x44	U_GAIN_1							0x00	0x30	0x30
	0x45	U_GAIN_2							0x00	0x30	0x30
	0x46	U_GAIN_3							0x00	0x30	0x30
	0x47	U_GAIN_4							0x00	0x30	0x30
	0x48	V_GAIN_1							0x20	0x30	0x00
	0x49	V_GAIN_2							0x20	0x30	0x00
	0x4A	V_GAIN_3							0x20	0x30	0x00
	0x4B	V_GAIN_4							0x20	0x30	0x00
	0x4C	U_OFFSET_1							0x04	0x00	0x04
	0x4D	U_OFFSET_2							0x04	0x00	0x04
	0x4E	U_OFFSET_3							0x04	0x00	0x04
	0x4F	U_OFFSET_4							0x04	0x00	0x04
	0x50	V_OFFSET_1							0x04	0x00	0x04
	0x51	V_OFFSET_2							0x04	0x00	0x04
	0x52	V_OFFSET_3							0x04	0x00	0x04
	0x53	V_OFFSET_4							0x04	0x00	0x04
0x54	FLD_INV_4	FLD_INV_3	FLD_INV_2	FLD_INV_1	NOVID_INF_IN_14	CHID_TYPE_14		0x01	0xF1	0x01	
0x55	CHID_VIN2				CHID_VIN1				0x10	0x10	0x10
0x56	CHID_VIN4				CHID_VIN3				0x32	0x32	0x32
0x57	-							-	-	-	
0x58	H_DELAY_1							0xAC	0x44	0x45	
0x59	H_DELAY_2							0xAC	0x44	0x45	
0x5A	H_DELAY_3							0xAC	0x44	0x45	
0x5B	H_DELAY_4							0xAC	0x44	0x45	
0x5C	V_DELAY_1							0x1E	0x1E	0x1E	
0x5D	V_DELAY_2							0x1E	0x1E	0x1E	
0x5E	V_DELAY_3							0x1E	0x1E	0x1E	
0x5F	V_DELAY_4							0x1E	0x1E	0x1E	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 0	0x60				HBLK_END_1				0x00	0x00	0x00	
	0x61				HBLK_END_2				0x00	0x00	0x00	
	0x62				HBLK_END_3				0x00	0x00	0x00	
	0x63				HBLK_END_4				0x00	0x00	0x00	
	0x64				VBLK_END_1				0x0D	0x08	0x0D	
	0x65				VBLK_END_2				0x0D	0x08	0x0D	
	0x66				VBLK_END_3				0x0D	0x08	0x0D	
	0x67				VBLK_END_4				0x0D	0x08	0x0D	
	0x68				H_CROP_S_1				0x00	0x00	0x00	
	0x69				H_CROP_S_2				0x00	0x00	0x00	
	0x6A				H_CROP_S_3				0x00	0x00	0x00	
	0x6B				H_CROP_S_4				0x00	0x00	0x00	
	0x6C				H_CROP_E_1				0x00	0x00	0x00	
	0x6D				H_CROP_E_2				0x00	0x00	0x00	
	0x6E				H_CROP_E_3				0x00	0x00	0x00	
	0x6F				H_CROP_E_4				0x00	0x00	0x00	
	0x70				V_CROP_S_1				0x00	0x00	0x00	
	0x71				V_CROP_S_2				0x00	0x00	0x00	
	0x72				V_CROP_S_3				0x00	0x00	0x00	
	0x73				V_CROP_S_4				0x00	0x00	0x00	
	0x74				V_CROP_E_1				0x00	0x00	0x00	
	0x75				V_CROP_E_2				0x00	0x00	0x00	
	0x76				V_CROP_E_3				0x00	0x00	0x00	
	0x77				V_CROP_E_4				0x00	0x00	0x00	
	0x78		BGDCOL_2				BGDCOL_1			0x88	0x88	0x88
	0x79		BGDCOL_4				BGDCOL_3			0x88	0x88	0x88
	0x7A		DATA_OUT_MODE_2				DATA_OUT_MODE_1			0x11	0x11	0x11
	0x7B		DATA_OUT_MODE_4				DATA_OUT_MODE_3			0x11	0x11	0x11
	0x7C									-	-	-
	0x7D									-	-	-
	0x7E									-	-	-
	0x7F									-	-	-

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
0x80	-RESERVED-								0x00	0x00	0x00
0x81	-RESERVED-								0x00	0x00	0x00
0x82					PD_VCH8	PD_VCH7	PD_VCH6	PD_VCH5	0x00	0x00	0x00
0x83	-								0x00	0x00	0x00
0x84	-RESERVED-								0x00	0x00	0x00
0x85	-RESERVED-								0x00	0x00	0x00
0x86	-RESERVED-								0xAF	0xAF	0xAF
0x87	-RESERVED-								0x00	0x00	0x00
0x88	AUTO_5	BSF_MODE_5	VIDEO_FORMAT_5						0xDD	0xA0	0xDD
0x89	AUTO_6	BSF_MODE_6	VIDEO_FORMAT_6						0xDD	0xA0	0xDD
0x8A	AUTO_7	BSF_MODE_7	VIDEO_FORMAT_7						0xDD	0xA0	0xDD
0x8B	AUTO_8	BSF_MODE_8	VIDEO_FORMAT_8						0xDD	0xA0	0xDD
0x8C	BRIGHTNESS_5								0xF8	0xFE	0xF8
0x8D	BRIGHTNESS_6								0xF8	0xFE	0xF8
0x8E	BRIGHTNESS_7								0xF8	0xFE	0xF8
0x8F	BRIGHTNESS_8								0xF8	0xFE	0xF8
0x90	CONTRAST_5								0x80	0x88	0x80
0x91	CONTRAST_6								0x80	0x88	0x80
0x92	CONTRAST_7								0x80	0x88	0x80
0x93	CONTRAST_8								0x80	0x88	0x80
0x94	H_SHARPNESS_5		V_SHARPNESS_5						0x80	0x80	0x80
0x95	H_SHARPNESS_6		V_SHARPNESS_6						0x80	0x80	0x80
0x96	H_SHARPNESS_7		V_SHARPNESS_7						0x80	0x80	0x80
0x97	H_SHARPNESS_8		V_SHARPNESS_8						0x80	0x80	0x80
0x98	Y_FIR_MODE_6		Y_FIR_MODE_5						0x77	0x88	0x88
0x99	Y_FIR_MODE_8		Y_FIR_MODE_7						0x77	0x88	0x88
0x9A	Y_PEAK_MODE_6		Y_PEAK_MODE_5						0x11	0x11	0x11
0x9B	Y_PEAK_MODE_8		Y_PEAK_MODE_7						0x11	0x11	0x11
0x9C	-RESERVED-	PED_ON_5	-RESERVED-						0xA2	0xA4	0xA2
0x9D	-RESERVED-	PED_ON_6	-RESERVED-						0xA2	0xA4	0xA2
0x9E	-RESERVED-	PED_ON_7	-RESERVED-						0xA2	0xA4	0xA2
0x9F	-RESERVED-	PED_ON_8	-RESERVED-						0xA2	0xA4	0xA2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
0xA0					-						
0xA1					-						
0xA2					-						
0xA3					-						
0xA4					-						
0xA5					-						
0xA6					-						
0xA7					-						
0xA8					-						
0xA9					-						
0xAA					-						
0xAB					-						
0xAC					-						
0xAD					-						
0xAE					-						
0xAF					-						
0xB0		-RESERVED-				Y_DELAY_5			0x13	0x13	0x13
0xB1		-RESERVED-				Y_DELAY_6			0x13	0x13	0x13
0xB2		-RESERVED-				Y_DELAY_7			0x13	0x13	0x13
0xB3		-RESERVED-				Y_DELAY_8			0x13	0x13	0x13
0xB4	ACC_OFF_58		-RESERVED-			ACC_GAIN_SPD_58			0x2F	0x2F	0x2F
0xB5	PAL_CM_OFF_58		IF_FIR_SEL_58			CLPF_SEL_58			0x02	0x82	0x02
0xB6	COLOROFF_8	COLOROFF_7	COLOROFF_6	COLOROFF_5		C_KILL_58			0x0B	0x0B	0x0B
0xB7	FLD_DET_MODE_58		-RESERVED-			NOVID_DET_B_58			0x43	0x43	0x43
0xB8					CTI_GAIN_5				0x0A	0x0A	0x0A
0xB9					CTI_GAIN_6				0x0A	0x0A	0x0A
0xBA					CTI_GAIN_7				0x0A	0x0A	0x0A
0xBB					CTI_GAIN_8				0x0A	0x0A	0x0A
0xBC					SATURATION_5				0x80	0x80	0x80
0xBD					SATURATION_6				0x80	0x80	0x80
0xBE					SATURATION_7				0x80	0x80	0x80
0xBF					SATURATION_8				0x80	0x80	0x80

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
B A N K 0	0xC0	HUE_5							0x00	0x01	0x00
	0xC1	HUE_6							0x00	0x01	0x00
	0xC2	HUE_7							0x00	0x01	0x00
	0xC3	HUE_8							0x00	0x01	0x00
	0xC4	U_GAIN_5							0x00	0x30	0x30
	0xC5	U_GAIN_6							0x00	0x30	0x30
	0xC6	U_GAIN_7							0x00	0x30	0x30
	0xC7	U_GAIN_8							0x00	0x30	0x30
	0xC8	V_GAIN_5							0x20	0x30	0x00
	0xC9	V_GAIN_6							0x20	0x30	0x00
	0xCA	V_GAIN_7							0x20	0x30	0x00
	0xCB	V_GAIN_8							0x20	0x30	0x00
	0xCC	U_OFFSET_5							0x04	0x00	0x04
	0xCD	U_OFFSET_6							0x04	0x00	0x04
	0xCE	U_OFFSET_7							0x04	0x00	0x04
	0xCF	U_OFFSET_8							0x04	0x00	0x04
0xD0	V_OFFSET_5							0x04	0x00	0x04	
0xD1	V_OFFSET_6							0x04	0x00	0x04	
0xD2	V_OFFSET_7							0x04	0x00	0x04	
0xD3	V_OFFSET_8							0x04	0x00	0x04	
0xD4	FLD_INV_8	FLD_INV_7	FLD_INV_6	FLD_INV_5	NOVID_INF_IN_58	CHID_TYPE_14			0x01	0xF1	0x01
0xD5	CHID_VIN6				CHID_VIN5			0x54	0x54	0x54	
0xD6	CHID_VIN8				CHID_VIN7			0x76	0x76	0x76	
0xD7	-							-	-	-	
0xD8	H_DELAY_5							0xAC	0x44	0x45	
0xD9	H_DELAY_6							0xAC	0x44	0x45	
0xDA	H_DELAY_7							0xAC	0x44	0x45	
0xDB	H_DELAY_8							0xAC	0x44	0x45	
0xDC	V_DELAY_5							0x1E	0x1E	0x1E	
0xDD	V_DELAY_6							0x1E	0x1E	0x1E	
0xDE	V_DELAY_7							0x1E	0x1E	0x1E	
0xDF	V_DELAY_8							0x1E	0x1E	0x1E	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
0xE0				HBLK_END_5					0x00	0x00	0x00
0xE1				HBLK_END_6					0x00	0x00	0x00
0xE2				HBLK_END_7					0x00	0x00	0x00
0xE3				HBLK_END_8					0x00	0x00	0x00
0xE4				VBLK_END_5					0x0D	0x08	0x0D
0xE5				VBLK_END_6					0x0D	0x08	0x0D
0xE6				VBLK_END_7					0x0D	0x08	0x0D
0xE7				VBLK_END_8					0x0D	0x08	0x0D
0xE8				H_CROP_S_5					0x00	0x00	0x00
0xE9				H_CROP_S_6					0x00	0x00	0x00
0xEA				H_CROP_S_7					0x00	0x00	0x00
0xEB				H_CROP_S_8					0x00	0x00	0x00
0xEC				H_CROP_E_5					0x00	0x00	0x00
0xED				H_CROP_E_6					0x00	0x00	0x00
0xEE				H_CROP_E_7					0x00	0x00	0x00
0xEF				H_CROP_E_8					0x00	0x00	0x00
0xF0				V_CROP_S_5					0x00	0x00	0x00
0xF1				V_CROP_S_6					0x00	0x00	0x00
0xF2				V_CROP_S_7					0x00	0x00	0x00
0xF3				V_CROP_S_8					0x00	0x00	0x00
0xF4				V_CROP_E_5					0x00	0x00	0x00
0xF5				V_CROP_E_6					0x00	0x00	0x00
0xF6				V_CROP_E_7					0x00	0x00	0x00
0xF7				V_CROP_E_8					0x00	0x00	0x00
0xF8		BGDCOL_6						BGDCOL_5	0x88	0x88	0x88
0xF9		BGDCOL_8						BGDCOL_7	0x88	0x88	0x88
0xFA		DATA_OUT_MODE_6						DATA_OUT_MODE_5	0x11	0x11	0x11
0xFB		DATA_OUT_MODE_8						DATA_OUT_MODE_7	0x11	0x11	0x11
0xFC									-	-	-
0xFD									-	-	-
0xFE									-	-	-
0xFF								BANK_SEL	0x00	0x00	0x00

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
0x00	PD_AAFE	-	-RESERVED-	RM_PB_PIN	PB_RM_PIN	FILTER_ON	EN_32K_MODE	0x02	0x02	0x02	
0x01	AIGAIN_01								0x00	0x08	0x08
0x02	AIGAIN_02								0x00	0x08	0x08
0x03	AIGAIN_03								0x00	0x08	0x08
0x04	AIGAIN_04								0x00	0x08	0x08
0x05	MIGAIN_01								0x00	0x08	0x08
0x06	CAS_PB	TRANS_MODE	CAS_4CH	CAS_PIN	-RESERVED-	CHIP_STAGE		0x1B	0x1B	0x1B	
0x07	RM_MASTER	RM_CLK	RM_BITRATE		RM_SAMRATE	RM_BITWID	RM_SSP	RM_SYNC	0xC8	0xC8	0xC8
0x08	RM_BIT_SWAP	RM_LAW_SEL	RM_FORMAT		R_ADATSP2	R_ADATSP	R_MULTCH		0x03	0x03	0x03
0x09	R_SEQ_08[4]	R_SEQ_07[4]	R_SEQ_06[4]	R_SEQ_05[4]	R_SEQ_04[4]	R_SEQ_03[4]	R_SEQ_02[4]	R_SEQ_01[4]	0x00	0x00	0x00
0x0A	R_SEQ_02[3:0]				R_SEQ_01[3:0]				0x10	0x10	0x10
0x0B	R_SEQ_04[3:0]				R_SEQ_03[3:0]				0x32	0x32	0x32
0x0C	R_SEQ_06[3:0]				R_SEQ_05[3:0]				0x54	0x54	0x54
0x0D	R_SEQ_08[3:0]				R_SEQ_07[3:0]				0x76	0x76	0x76
0x0E	R_SEQ_16[4]	R_SEQ_15[4]	R_SEQ_14[4]	R_SEQ_13[4]	R_SEQ_12[4]	R_SEQ_11[4]	R_SEQ_10[4]	R_SEQ_09[4]	0x00	0x00	0x00
0x0F	R_SEQ_10[3:0]				R_SEQ_09[3:0]				0x98	0x98	0x98
0x10	R_SEQ_12[3:0]				R_SEQ_11[3:0]				0xBA	0xBA	0xBA
0x11	R_SEQ_14[3:0]				R_SEQ_13[3:0]				0xDC	0xDC	0xDC
0x12	R_SEQ_16[3:0]				R_SEQ_15[3:0]				0xFE	0xFE	0xFE
0x13	PB_MASTER	PB_CLK	PB_BITRATE		PB_SAMRATE	PB_BITWID	PB_SSP	PB_SYNC	0x08	0x08	0x08
0x14	PB_BIT_SWAP	-		PB_SEL				0x00	0x00	0x00	
0x15	PB_FORMAT		-		PB_LAW_SEL	--RESERVED--		0x00	0x00	0x00	
0x16	MIX_RATIO_02				MIX_RATIO_01				0x88	0x88	0x88
0x17	MIX_RATIO_04				MIX_RATIO_03				0x88	0x88	0x88
0x18	MIX_RATIO_06				MIX_RATIO_05				0x88	0x88	0x88
0x19	MIX_RATIO_08				MIX_RATIO_07				0x88	0x88	0x88
0x1A	MIX_RATIO_10				MIX_RATIO_09				0x88	0x88	0x88
0x1B	MIX_RATIO_12				MIX_RATIO_11				0x88	0x88	0x88
0x1C	MIX_RATIO_14				MIX_RATIO_13				0x88	0x88	0x88
0x1D	MIX_RATIO_16				MIX_RATIO_15				0x88	0x88	0x88
0x1E	MIX_RATIO_M2				MIX_RATIO_M1				0x88	0x88	0x88
0x1F	MIX_RATIO_M4				MIX_RATIO_M3				0x88	0x88	0x88

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
0x20	MIX_RATIO_P2				MIX_RATIO_P1				0x88	0x88	0x88
0x21	MIX_RATIO_P4				MIX_RATIO_P3				0x88	0x88	0x88
0x22	AOGAIN								0x00	0x08	0x08
0x23	-RESERVED-	MIX_DERATIO		MIX_OUTSEL				0x19	0x19	0x19	
0x24	-			L_CH_OUTSEL				0x18	0x18	0x18	
0x25	-			R_CH_OUTSEL				0x16	0x16	0x16	
0x26	MIX_MUTE_08	MIX_MUTE_07	MIX_MUTE_06	MIX_MUTE_05	MIX_MUTE_04	MIX_MUTE_03	MIX_MUTE_02	MIX_MUTE_01	0x00	0x00	0x00
0x27	MIX_MUTE_16	MIX_MUTE_15	MIX_MUTE_14	MIX_MUTE_13	MIX_MUTE_12	MIX_MUTE_11	MIX_MUTE_10	MIX_MUTE_09	0x00	0x00	0x00
0x28	MIX_MUTE_M 4	MIX_MUTE_M 3	MIX_MUTE_M 2	MIX_MUTE_M 1	MIX_MUTE_P4	MIX_MUTE_P3	MIX_MUTE_P2	MIX_MUTE_P1	0x00	0x00	0x00
0x29	-RESERVED-				ADET_MODE	ADET_FILT			0x88	0x88	0x88
0x2A	ADET_08	ADET_07	ADET_06	ADET_05	ADET_04	ADET_03	ADET_02	ADET_01	0xFF	0xFF	0xFF
0x2B	-	ADET_M1		-				0xC0	0x40	0x40	
0x2C	ADET_TH_02				ADET_TH_01				0xAA	0xAA	0xAA
0x2D	ADET_TH_04				ADET_TH_03				0xAA	0xAA	0xAA
0x2E	ADET_TH_06				ADET_TH_05				0xAA	0xAA	0xAA
0x2F	ADET_TH_08				ADET_TH_07				0xAA	0xAA	0xAA
0x30	-			ADET_TH_M1				0xAA	0x0A	0x0A	
0x31	-RESERVED-								0x02	0x82	0x82
0x32	-RESERVED-								0x00	0x00	0x00
0x33	-										
0x34	-RESERVED-								0x00	0x00	0x00
0x35	-RESERVED-								0x00	0x8C	0x8C
0x36	-RESERVED-								0x00	0xA0	0xA0
0x37	-RESERVED-								0x00	0x00	0x00
0x38	-RESERVED-			AUD_SW_RST	-RESERVED-				0x00	0x08	0x08
0x39	RM_DELAY	PB_DELAY	-RESERVED-				0x05	0x01	0x01		
0x3A	-RESERVED-								0xA2	0x81	0x81
0x3B	-RESERVED-								0x10	0x10	0x10
0x3C	-			MIC_SEQ_01 [4]	MIC_SEQ_01[3:0]				0x00	0x00	0x00
0x3D	-			MIC_SEQ_02 [4]	MIC_SEQ_02[3:0]				0x00	0x00	0x00
0x3E	-RESERVED-								0x10	0x00	0x00
0x3F	-								0x11	0x00	0x00

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 1	0x40	AIGAIN_05							0x00	0x08	0x08	
	0x41	AIGAIN_06							0x00	0x08	0x08	
	0x42	AIGAIN_07							0x00	0x08	0x08	
	0x43	AIGAIN_08							0x00	0x08	0x08	
	0x44	-RESERVED-							0x11	0x14	0x14	
	0x45	-RESERVED-							0x00	0x01	0x01	
	0x46	-RESERVED-							0x00	0x00	0x00	
	0x47	-RESERVED-							0x20	0x40	0x40	
	0x48	-RESERVED-							0x60	0x60	0x60	
	0x49	-RESERVED-							0x00	0x00	0x00	
	0x4A	-RESERVED-							0x22	0x03	0x03	
	0x4B	-RESERVED-							0x20	0x10	0x10	
	0x4C	-RESERVED-							0x00	0x00	0x00	
	0x4D	-RESERVED-							0x00	0x00	0x00	
	0x4E	-RESERVED-							0x00	0x00	0x00	
	0x4F	-							-	-	-	
	0x50	BAUD							0x37	0x37	0x37	
	0x51	RBAUD							0x37	0x37	0x37	
	0x52	PELCO_BAUD							0x1B	0x1B	0x1B	
	0x53	BL_TXST_01							0x05	0x05	0x05	
	0x54	-			BL_TXST_02				0x00	0x00	0x00	
	0x55	BL_RXST_01							0x07	0x07	0x07	
	0x56	-			BL_RXST_02				0x00	0x00	0x00	
	0x57	PELCO_TXST_01							0x09	0x09	0x09	
	0x58	-			PELCO_TXST_02				0x00	0x00	0x00	
	0x59	-							TX_START	0x00	0x00	0x00
	0x5A	-			TX_BYTE_LENGTH				0x08	0x08	0x08	
	0x5B	-			PACKET_MODE				0x06	0x06	0x06	
	0x5C	-							PELCO_CTEN	0x00	0x00	0x00
	0x5D	BL_HSP_01							0x46	0x46	0x46	
	0x5E	AUD_72M	-		BL_HSP_02				0x00	0x00	0x00	
0x5F	-							PELCO_SHOT	0x00	0x00	0x00	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 1	0x60								TX_DATA_01	0xAA	0xAA	0xAA
	0x61								TX_DATA_02	0x1B	0x1C	0x1C
	0x62								TX_DATA_03	0x00	0x18	0x18
	0x63								TX_DATA_04	0x00	0xFF	0xFF
	0x64								TX_DATA_05	0xAA	0xAA	0xAA
	0x65								TX_DATA_06	0x3B	0x3C	0x3C
	0x66								TX_DATA_07	0x00	0xFF	0xFF
	0x67								TX_DATA_08	0x1F	0xFF	0xFF
	0x68								TX_DATA_09	0xAA	0xAA	0xAA
	0x69								TX_DATA_10	0x1C	0x1B	0x1B
	0x6A								TX_DATA_11	0x18	0x00	0x00
	0x6B								TX_DATA_12	0xFF	0x00	0x00
	0x6C								TX_DATA_13	0xAA	0xAA	0xAA
	0x6D								TX_DATA_14	0x3C	0x3B	0x3B
	0x6E								TX_DATA_15	0xFF	0x00	0x00
	0x6F								TX_DATA_16	0xFF	0x00	0x00
	0x70								PELCO_TXDAT_01	0xFF	0x00	0x00
	0x71								PELCO_TXDAT_02	0x00	0x00	0x00
	0x72								PELCO_TXDAT_03	0xFF	0x00	0x00
	0x73								PELCO_TXDAT_04	0x00	0x00	0x00
	0x74								RX_DATA_01	R	R	R
	0x75								RX_DATA_02	R	R	R
	0x76								RX_DATA_03	R	R	R
	0x77								RX_DATA_04	R	R	R
	0x78								RX_DATA_05	R	R	R
	0x79								RX_DATA_06	R	R	R
	0x7A								RX_DATA_07	R	R	R
	0x7B								RX_DATA_08	R	R	R
	0x7C								VSO_INV	0x00	0x00	0x00
	0x7D								HSD_INV	0x00	0x00	0x00
	0x7E								RX_THRESHOLD	0x80	0x80	0x80
	0x7F								Hidden_Even_line_modification	0x01	0x01	0x01

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
B A N K 1	0x80	-RESERVED-							0x00	0x00	0x00
	0x81	-RESERVED-							0xFF	0xFF	0xFF
	0x82	-RESERVED-							0x00	0x00	0x00
	0x83	-RESERVED-							0x00	0x00	0x00
	0x84	-RESERVED-							0x00	0x00	0x00
	0x85	-RESERVED-							0x00	0x00	0x00
	0x86	-RESERVED-							0x06	0x00	0x00
	0x87	-RESERVED-							0x01	0x00	0x00
	0x88	-RESERVED-							0x00	0x00	0x00
	0x89	-RESERVED-							0x00	0x00	0x00
	0x8A	-RESERVED-							0x00	0x00	0x00
	0x8B	-				DEVICE_SEL			0x00	0x00	0x00
	0x8C	COAX_OUT_SEL_2			COAX_OUT_SEL_1				0x10	0x10	0x10
	0x8D	COAX_OUT_SEL_4			COAX_OUT_SEL_3				0x32	0x32	0x32
	0x8E	-RESERVED-							0x00	0x00	0x00
	0x8F	-RESERVED-							0x00	0x00	0x00
0x90								CLEAN	0x00	0x00	0x00
0x91	-							-	-	-	
0x92	-							-	-	-	
0x93	-							-	-	-	
0x94	-RESERVED-							0x00	0x00	0x00	
0x95	-							-	-	-	
0x96	-							-	-	-	
0x97	-							-	-	-	
0x98	-							-	-	-	
0x99	-							-	-	-	
0x9A	-							-	-	-	
0x9B	-							-	-	-	
0x9C	-							-	-	-	
0x9D	-							-	-	-	
0x9E	-							-	-	-	
0x9F	-							-	-	-	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL
0xA0					-						
0xA1					-						
0xA2					-						
0xA3					-						
0xA4					-						
0xA5					-						
0xA6					-						
0xA7					-						
0xA8					-						
0xA9					-						
0xAA					-						
0xAB					-						
0xAC					-						
0xAD					-						
0xAE					-						
0xAF					-						
0xB0					-						
0xB1					-						
0xB2					-						
0xB3					-						
0xB4					-RESERVED-				0x00	0x40	0x40
0xB5					-RESERVED-				0x00	0x30	0x30
0xB6					-RESERVED-				0x00	0x40	0x40
0xB7					-RESERVED-				0x00	0x30	0x30
0xB8					-				0x00	0x00	0x00
0xB9					-				0x00	0x00	0x00
0xBA					-				0x00	0x00	0x00
0xBB					-				0x00	0x00	0x00
0xBC			MPP_SEL2				MPP_SEL1		0x00	0x00	0x00
0xBD			MPP_SEL4				MPP_SEL3		0x00	0x00	0x00
0xBE					-				0x00	0x00	0x00
0xBF					-				0x00	0x00	0x00

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 1	0xC0	VPORTA_SEQ2			VPORTA_SEQ1				0x10	0x10	0x10	
	0xC1	VPORTA_SEQ4			VPORTA_SEQ3				0x10	0x32	0x32	
	0xC2	VPORTB_SEQ2			VPORTB_SEQ1				0x32	0x54	0x54	
	0xC3	VPORTB_SEQ4			VPORTB_SEQ3				0x32	0x76	0x76	
	0xC4								0x00	0x00	0x00	
	0xC5								0x00	0x00	0x00	
	0xC6								0x00	0x00	0x00	
	0xC7								0x00	0x00	0x00	
	0xC8	CH_OUT_SELB			CH_OUT_SELA				0x22	0x88	0x88	
	0xC9								0x00	0x00	0x00	
	0xCA							VDO_2_EN	VDO_1_EN	0x00	0x03	0x03
	0xCB							-RESERVED-		0x00	0x00	0x00
	0xCC	-	VCLK_1_SEL		VCLK_1_DLY_SEL					0x30	0x70	0x70
	0xCD	-	VCLK_2_SEL		VCLK_2_DLY_SEL					0x10	0x70	0x70
	0xCE									0x00	0x00	0x00
	0xCF									0x00	0x00	0x00
	0xD0							OUT_DATA_INV		0x00	0x00	0x00
	0xD1							-RESERVED-		0x00	0x00	0x00
	0xD2									0x00	0x00	0x00
	0xD3							-RESERVED-		0x00	0x00	0x00
	0xD4							-RESERVED-		0x00	0x00	0x00
	0xD5							-RESERVED-		0x00	0x01	0x01
	0xD6							-RESERVED-		0x00	0x00	0x00
	0xD7									-	-	-
	0xD8	NOVID_08	NOVID_07	NOVID_06	NOVID_05	NOVID_04	NOVID_03	NOVID_02	NOVID_01	R	R	R
	0xD9	MOTION_08	MOTION_07	MOTION_06	MOTION_05	MOTION_04	MOTION_03	MOTION_02	MOTION_01	R	R	R
	0xDA	BLACK_08	BLACK_07	BLACK_06	BLACK_05	BLACK_04	BLACK_03	BLACK_02	BLACK_01	R	R	R
	0xDB	WHITE_08	WHITE_07	WHITE_06	WHITE_05	WHITE_04	WHITE_03	WHITE_02	WHITE_01	R	R	R
0xDC	MUTE_08	MUTE_07	MUTE_06	MUTE_05	MUTE_04	MUTE_03	MUTE_02	MUTE_01	R	R	R	
0xDD	MUTE_16	MUTE_15	MUTE_14	MUTE_13	MUTE_12	MUTE_11	MUTE_10	MUTE_09	R	R	R	
0xDE							MUTEMIC_02		MUTEMIC_01	R	R	R
0xDF												

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
0xE0	NOVID_08B	NOVID_07B	NOVID_06B	NOVID_05B	NOVID_04B	NOVID_03B	NOVID_02B	NOVID_01B	R	R	R	
0xE1	MOTION_08B	MOTION_07B	MOTION_06B	MOTION_05B	MOTION_04B	MOTION_03B	MOTION_02B	MOTION_01B	R	R	R	
0xE2	BLACK_08B	BLACK_07B	BLACK_06B	BLACK_05B	BLACK_04B	BLACK_03B	BLACK_02B	BLACK_01B	R	R	R	
0xE3	WHITE_08B	WHITE_07B	WHITE_06B	WHITE_05B	WHITE_04B	WHITE_03B	WHITE_02B	WHITE_01B	R	R	R	
0xE4	MUTE_08B	MUTE_07B	MUTE_06B	MUTE_05B	MUTE_04B	MUTE_03B	MUTE_02B	MUTE_01B	R	R	R	
0xE5	MUTE_16B	MUTE_15B	MUTE_14B	MUTE_13B	MUTE_12B	MUTE_11B	MUTE_10B	MUTE_09B	R	R	R	
0xE6	-			-	MUTEMIC_02B	-	MUTEMIC_01B		R	R	R	
0xE7	-											
0xE8	RD_STATE_CLR	-		STATE_HOLD	-				0x90	0x90	0x90	
0xE9	-RESERVED-								0x00	0x00	0x00	
0xEA	-											
0xEB	-											
0xEC	AGC_LOCK_08	AGC_LOCK_07	AGC_LOCK_06	AGC_LOCK_05	AGC_LOCK_04	AGC_LOCK_03	AGC_LOCK_02	AGC_LOCK_01	R	R	R	
0xED	CMP_LOCK_08	CMP_LOCK_07	CMP_LOCK_06	CMP_LOCK_05	CMP_LOCK_04	CMP_LOCK_03	CMP_LOCK_02	CMP_LOCK_01	R	R	R	
0xEE	H_LOCK_08	H_LOCK_07	H_LOCK_06	H_LOCK_05	H_LOCK_04	H_LOCK_03	H_LOCK_02	H_LOCK_01	R	R	R	
0xEF	AUTO_NT_04		AUTO_NT_03		AUTO_NT_02		AUTO_NT_01		R	R	R	
0xF0	AUTO_NT_08		AUTO_NT_07		AUTO_NT_06		AUTO_NT_05		R	R	R	
0xF1	FLD_04		FLD_03		FLD_02		FLD_01		R	R	R	
0xF2	FLD_08		FLD_07		FLD_06		FLD_05		R	R	R	
0xF3	BW_08	BW_07	BW_06	BW_05	BW_04	BW_03	BW_02	BW_01	R	R	R	
0xF4	DEV_ID (NVP1918C = 0x82)								R	R	R	
0xF5	-				REV_ID					R	R	R
0xF6	CMP_VALUE								R	R	R	
0xF7	AGC_VALUE								R	R	R	
0xF8	-				CMP_AGC_CH				0x00	0x00	0x00	
0xF9	-											
0xFA	-											
0xFB	-											
0xFC	-											
0xFD	-											
0xFE	-											
0xFF	-				BANK_SEL				0x00	0x00	0x00	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 2	0x00	-RESERVED-		MOTION_OFF01	-RESERVED-		MOTION_PIC_01		0x03	0x03	0x03	
	0x01	MOD_TSEN_01								0x60	0x60	0x60
	0x02	-RESERVED-		MOTION_OFF02	-RESERVED-		MOTION_PIC_02		0x03	0x03	0x03	
	0x03	MOD_TSEN_02								0x60	0x60	0x60
	0x04	-RESERVED-		MOTION_OFF03	-RESERVED-		MOTION_PIC_03		0x03	0x03	0x03	
	0x05	MOD_TSEN_03								0x60	0x60	0x60
	0x06	-RESERVED-		MOTION_OFF04	-RESERVED-		MOTION_PIC_04		0x03	0x03	0x03	
	0x07	MOD_TSEN_04								0x60	0x60	0x60
	0x08	-RESERVED-		MOTION_OFF05	-RESERVED-		MOTION_PIC_05		0x03	0x03	0x03	
	0x09	MOD_TSEN_05								0x60	0x60	0x60
	0x0A	-RESERVED-		MOTION_OFF06	-RESERVED-		MOTION_PIC_06		0x03	0x03	0x03	
	0x0B	MOD_TSEN_06								0x60	0x60	0x60
	0x0C	-RESERVED-		MOTION_OFF07	-RESERVED-		MOTION_PIC_07		0x03	0x03	0x03	
	0x0D	MOD_TSEN_07								0x60	0x60	0x60
	0x0E	-RESERVED-		MOTION_OFF08	-RESERVED-		MOTION_PIC_08		0x03	0x03	0x03	
	0x0F	MOD_TSEN_08								0x60	0x60	0x60
0x10	MOD_PSEN_01		MOD_PSEN_02		MOD_PSEN_03		MOD_PSEN_04		0x00	0x00	0x00	
0x11	MOD_PSEN_05		MOD_PSEN_06		MOD_PSEN_07		MOD_PSEN_08		0x00	0x00	0x00	
0x12	MD_H960_CH8	MD_H960_CH7	MD_H960_CH6	MD_H960_CH5	MD_H960_CH4	MD_H960_CH3	MD_H960_CH2	MD_H960_CH1	0x00	0xFF	0xFF	
0x13	-RESERVED-								0x00	0x00	0x00	
0x14	-RESERVED-								0x00	0xC0	0xC0	
0x15	-RESERVED-								0x00	0x00	0x00	
0x16	-RESERVED-								0x00	0x00	0x00	
0x17	-RESERVED-								0x00	0x00	0x00	
0x18	-								-	-	-	
0x19	-								-	-	-	
0x1A	-								-	-	-	
0x1B	-								-	-	-	
0x1C	-								-	-	-	
0x1D	-								-	-	-	
0x1E	-								-	-	-	
0x1F	-								-	-	-	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 2	0x20	CH1_MOD_01	CH1_MOD_02	CH1_MOD_03	CH1_MOD_04	CH1_MOD_05	CH1_MOD_06	CH1_MOD_07	CH1_MOD_08	0xFF	0xFF	0xFF
	0x21	CH1_MOD_09	CH1_MOD_10	CH1_MOD_11	CH1_MOD_12	CH1_MOD_13	CH1_MOD_14	CH1_MOD_15	CH1_MOD_16	0xFF	0xFF	0xFF
	0x22	CH1_MOD_17	CH1_MOD_18	CH1_MOD_19	CH1_MOD_20	CH1_MOD_21	CH1_MOD_22	CH1_MOD_23	CH1_MOD_24	0xFF	0xFF	0xFF
	0x23	CH1_MOD_25	CH1_MOD_26	CH1_MOD_27	CH1_MOD_28	CH1_MOD_29	CH1_MOD_30	CH1_MOD_31	CH1_MOD_32	0xFF	0xFF	0xFF
	0x24	CH1_MOD_33	CH1_MOD_34	CH1_MOD_35	CH1_MOD_36	CH1_MOD_37	CH1_MOD_38	CH1_MOD_39	CH1_MOD_40	0xFF	0xFF	0xFF
	0x25	CH1_MOD_41	CH1_MOD_42	CH1_MOD_43	CH1_MOD_44	CH1_MOD_45	CH1_MOD_46	CH1_MOD_47	CH1_MOD_48	0xFF	0xFF	0xFF
	0x26	CH1_MOD_49	CH1_MOD_50	CH1_MOD_51	CH1_MOD_52	CH1_MOD_53	CH1_MOD_54	CH1_MOD_55	CH1_MOD_56	0xFF	0xFF	0xFF
	0x27	CH1_MOD_57	CH1_MOD_58	CH1_MOD_59	CH1_MOD_60	CH1_MOD_61	CH1_MOD_62	CH1_MOD_63	CH1_MOD_64	0xFF	0xFF	0xFF
	0x28	CH1_MOD_65	CH1_MOD_66	CH1_MOD_67	CH1_MOD_68	CH1_MOD_69	CH1_MOD_70	CH1_MOD_71	CH1_MOD_72	0xFF	0xFF	0xFF
	0x29	CH1_MOD_73	CH1_MOD_74	CH1_MOD_75	CH1_MOD_76	CH1_MOD_77	CH1_MOD_78	CH1_MOD_79	CH1_MOD_80	0xFF	0xFF	0xFF
	0x2A	CH1_MOD_81	CH1_MOD_82	CH1_MOD_83	CH1_MOD_84	CH1_MOD_85	CH1_MOD_86	CH1_MOD_87	CH1_MOD_88	0xFF	0xFF	0xFF
	0x2B	CH1_MOD_89	CH1_MOD_90	CH1_MOD_91	CH1_MOD_92	CH1_MOD_93	CH1_MOD_94	CH1_MOD_95	CH1_MOD_96	0xFF	0xFF	0xFF
	0x2C	CH1_MOD_97	CH1_MOD_98	CH1_MOD_99	CH1_MOD_100	CH1_MOD_101	CH1_MOD_102	CH1_MOD_103	CH1_MOD_104	0xFF	0xFF	0xFF
	0x2D	CH1_MOD_105	CH1_MOD_106	CH1_MOD_107	CH1_MOD_108	CH1_MOD_109	CH1_MOD_110	CH1_MOD_111	CH1_MOD_112	0xFF	0xFF	0xFF
	0x2E	CH1_MOD_113	CH1_MOD_114	CH1_MOD_115	CH1_MOD_116	CH1_MOD_117	CH1_MOD_118	CH1_MOD_119	CH1_MOD_120	0xFF	0xFF	0xFF
	0x2F	CH1_MOD_121	CH1_MOD_122	CH1_MOD_123	CH1_MOD_124	CH1_MOD_125	CH1_MOD_126	CH1_MOD_127	CH1_MOD_128	0xFF	0xFF	0xFF
	0x30	CH1_MOD_129	CH1_MOD_130	CH1_MOD_131	CH1_MOD_132	CH1_MOD_133	CH1_MOD_134	CH1_MOD_135	CH1_MOD_136	0xFF	0xFF	0xFF
	0x31	CH1_MOD_137	CH1_MOD_138	CH1_MOD_139	CH1_MOD_140	CH1_MOD_141	CH1_MOD_142	CH1_MOD_143	CH1_MOD_144	0xFF	0xFF	0xFF
	0x32	CH1_MOD_145	CH1_MOD_146	CH1_MOD_147	CH1_MOD_148	CH1_MOD_149	CH1_MOD_150	CH1_MOD_151	CH1_MOD_152	0xFF	0xFF	0xFF
	0x33	CH1_MOD_153	CH1_MOD_154	CH1_MOD_155	CH1_MOD_156	CH1_MOD_157	CH1_MOD_158	CH1_MOD_159	CH1_MOD_160	0xFF	0xFF	0xFF
	0x34	CH1_MOD_161	CH1_MOD_162	CH1_MOD_163	CH1_MOD_164	CH1_MOD_165	CH1_MOD_166	CH1_MOD_167	CH1_MOD_168	0xFF	0xFF	0xFF
	0x35	CH1_MOD_169	CH1_MOD_170	CH1_MOD_171	CH1_MOD_172	CH1_MOD_173	CH1_MOD_174	CH1_MOD_175	CH1_MOD_176	0xFF	0xFF	0xFF
	0x36	CH1_MOD_177	CH1_MOD_178	CH1_MOD_179	CH1_MOD_180	CH1_MOD_181	CH1_MOD_182	CH1_MOD_183	CH1_MOD_184	0xFF	0xFF	0xFF
	0x37	CH1_MOD_185	CH1_MOD_186	CH1_MOD_187	CH1_MOD_188	CH1_MOD_189	CH1_MOD_190	CH1_MOD_191	CH1_MOD_192	0xFF	0xFF	0xFF
	0x38	CH2_MOD_01	CH2_MOD_02	CH2_MOD_03	CH2_MOD_04	CH2_MOD_05	CH2_MOD_06	CH2_MOD_07	CH2_MOD_08	0xFF	0xFF	0xFF
	0x39	CH2_MOD_09	CH2_MOD_10	CH2_MOD_11	CH2_MOD_12	CH2_MOD_13	CH2_MOD_14	CH2_MOD_15	CH2_MOD_16	0xFF	0xFF	0xFF
	0x3A	CH2_MOD_17	CH2_MOD_18	CH2_MOD_19	CH2_MOD_20	CH2_MOD_21	CH2_MOD_22	CH2_MOD_23	CH2_MOD_24	0xFF	0xFF	0xFF
	0x3B	CH2_MOD_25	CH2_MOD_26	CH2_MOD_27	CH2_MOD_28	CH2_MOD_29	CH2_MOD_30	CH2_MOD_31	CH2_MOD_32	0xFF	0xFF	0xFF
	0x3C	CH2_MOD_33	CH2_MOD_34	CH2_MOD_35	CH2_MOD_36	CH2_MOD_37	CH2_MOD_38	CH2_MOD_39	CH2_MOD_40	0xFF	0xFF	0xFF
	0x3D	CH2_MOD_41	CH2_MOD_42	CH2_MOD_43	CH2_MOD_44	CH2_MOD_45	CH2_MOD_46	CH2_MOD_47	CH2_MOD_48	0xFF	0xFF	0xFF
	0x3E	CH2_MOD_49	CH2_MOD_50	CH2_MOD_51	CH2_MOD_52	CH2_MOD_53	CH2_MOD_54	CH2_MOD_55	CH2_MOD_56	0xFF	0xFF	0xFF
	0x3F	CH2_MOD_57	CH2_MOD_58	CH2_MOD_59	CH2_MOD_60	CH2_MOD_61	CH2_MOD_62	CH2_MOD_63	CH2_MOD_64	0xFF	0xFF	0xFF

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 2	0x40	CH2_MOD_65	CH2_MOD_66	CH2_MOD_67	CH2_MOD_68	CH2_MOD_69	CH2_MOD_70	CH2_MOD_71	CH2_MOD_72	0xFF	0xFF	0xFF
	0x41	CH2_MOD_73	CH2_MOD_74	CH2_MOD_75	CH2_MOD_76	CH2_MOD_77	CH2_MOD_78	CH2_MOD_79	CH2_MOD_80	0xFF	0xFF	0xFF
	0x42	CH2_MOD_81	CH2_MOD_82	CH2_MOD_83	CH2_MOD_84	CH2_MOD_85	CH2_MOD_86	CH2_MOD_87	CH2_MOD_88	0xFF	0xFF	0xFF
	0x43	CH2_MOD_89	CH2_MOD_90	CH2_MOD_91	CH2_MOD_92	CH2_MOD_93	CH2_MOD_94	CH2_MOD_95	CH2_MOD_96	0xFF	0xFF	0xFF
	0x44	CH2_MOD_97	CH2_MOD_98	CH2_MOD_99	CH2_MOD_100	CH2_MOD_101	CH2_MOD_102	CH2_MOD_103	CH2_MOD_104	0xFF	0xFF	0xFF
	0x45	CH2_MOD_105	CH2_MOD_106	CH2_MOD_107	CH2_MOD_108	CH2_MOD_109	CH2_MOD_110	CH2_MOD_111	CH2_MOD_112	0xFF	0xFF	0xFF
	0x46	CH2_MOD_113	CH2_MOD_114	CH2_MOD_115	CH2_MOD_116	CH2_MOD_117	CH2_MOD_118	CH2_MOD_119	CH2_MOD_120	0xFF	0xFF	0xFF
	0x47	CH2_MOD_121	CH2_MOD_122	CH2_MOD_123	CH2_MOD_124	CH2_MOD_125	CH2_MOD_126	CH2_MOD_127	CH2_MOD_128	0xFF	0xFF	0xFF
	0x48	CH2_MOD_129	CH2_MOD_130	CH2_MOD_131	CH2_MOD_132	CH2_MOD_133	CH2_MOD_134	CH2_MOD_135	CH2_MOD_136	0xFF	0xFF	0xFF
	0x49	CH2_MOD_137	CH2_MOD_138	CH2_MOD_139	CH2_MOD_140	CH2_MOD_141	CH2_MOD_142	CH2_MOD_143	CH2_MOD_144	0xFF	0xFF	0xFF
	0x4A	CH2_MOD_145	CH2_MOD_146	CH2_MOD_147	CH2_MOD_148	CH2_MOD_149	CH2_MOD_150	CH2_MOD_151	CH2_MOD_152	0xFF	0xFF	0xFF
	0x4B	CH2_MOD_153	CH2_MOD_154	CH2_MOD_155	CH2_MOD_156	CH2_MOD_157	CH2_MOD_158	CH2_MOD_159	CH2_MOD_160	0xFF	0xFF	0xFF
	0x4C	CH2_MOD_161	CH2_MOD_162	CH2_MOD_163	CH2_MOD_164	CH2_MOD_165	CH2_MOD_166	CH2_MOD_167	CH2_MOD_168	0xFF	0xFF	0xFF
	0x4D	CH2_MOD_169	CH2_MOD_170	CH2_MOD_171	CH2_MOD_172	CH2_MOD_173	CH2_MOD_174	CH2_MOD_175	CH2_MOD_176	0xFF	0xFF	0xFF
	0x4E	CH2_MOD_177	CH2_MOD_178	CH2_MOD_179	CH2_MOD_180	CH2_MOD_181	CH2_MOD_182	CH2_MOD_183	CH2_MOD_184	0xFF	0xFF	0xFF
	0x4F	CH2_MOD_185	CH2_MOD_186	CH2_MOD_187	CH2_MOD_188	CH2_MOD_189	CH2_MOD_190	CH2_MOD_191	CH2_MOD_192	0xFF	0xFF	0xFF
	0x50	CH3_MOD_01	CH3_MOD_02	CH3_MOD_03	CH3_MOD_04	CH3_MOD_05	CH3_MOD_06	CH3_MOD_07	CH3_MOD_08	0xFF	0xFF	0xFF
	0x51	CH3_MOD_09	CH3_MOD_10	CH3_MOD_11	CH3_MOD_12	CH3_MOD_13	CH3_MOD_14	CH3_MOD_15	CH3_MOD_16	0xFF	0xFF	0xFF
	0x52	CH3_MOD_17	CH3_MOD_18	CH3_MOD_19	CH3_MOD_20	CH3_MOD_21	CH3_MOD_22	CH3_MOD_23	CH3_MOD_24	0xFF	0xFF	0xFF
	0x53	CH3_MOD_25	CH3_MOD_26	CH3_MOD_27	CH3_MOD_28	CH3_MOD_29	CH3_MOD_30	CH3_MOD_31	CH3_MOD_32	0xFF	0xFF	0xFF
	0x54	CH3_MOD_33	CH3_MOD_34	CH3_MOD_35	CH3_MOD_36	CH3_MOD_37	CH3_MOD_38	CH3_MOD_39	CH3_MOD_40	0xFF	0xFF	0xFF
	0x55	CH3_MOD_41	CH3_MOD_42	CH3_MOD_43	CH3_MOD_44	CH3_MOD_45	CH3_MOD_46	CH3_MOD_47	CH3_MOD_48	0xFF	0xFF	0xFF
	0x56	CH3_MOD_49	CH3_MOD_50	CH3_MOD_51	CH3_MOD_52	CH3_MOD_53	CH3_MOD_54	CH3_MOD_55	CH3_MOD_56	0xFF	0xFF	0xFF
	0x57	CH3_MOD_57	CH3_MOD_58	CH3_MOD_59	CH3_MOD_60	CH3_MOD_61	CH3_MOD_62	CH3_MOD_63	CH3_MOD_64	0xFF	0xFF	0xFF
	0x58	CH3_MOD_65	CH3_MOD_66	CH3_MOD_67	CH3_MOD_68	CH3_MOD_69	CH3_MOD_70	CH3_MOD_71	CH3_MOD_72	0xFF	0xFF	0xFF
	0x59	CH3_MOD_73	CH3_MOD_74	CH3_MOD_75	CH3_MOD_76	CH3_MOD_77	CH3_MOD_78	CH3_MOD_79	CH3_MOD_80	0xFF	0xFF	0xFF
	0x5A	CH3_MOD_81	CH3_MOD_82	CH3_MOD_83	CH3_MOD_84	CH3_MOD_85	CH3_MOD_86	CH3_MOD_87	CH3_MOD_88	0xFF	0xFF	0xFF
	0x5B	CH3_MOD_89	CH3_MOD_90	CH3_MOD_91	CH3_MOD_92	CH3_MOD_93	CH3_MOD_94	CH3_MOD_95	CH3_MOD_96	0xFF	0xFF	0xFF
	0x5C	CH3_MOD_97	CH3_MOD_98	CH3_MOD_99	CH3_MOD_100	CH3_MOD_101	CH3_MOD_102	CH3_MOD_103	CH3_MOD_104	0xFF	0xFF	0xFF
	0x5D	CH3_MOD_105	CH3_MOD_106	CH3_MOD_107	CH3_MOD_108	CH3_MOD_109	CH3_MOD_110	CH3_MOD_111	CH3_MOD_112	0xFF	0xFF	0xFF
	0x5E	CH3_MOD_113	CH3_MOD_114	CH3_MOD_115	CH3_MOD_116	CH3_MOD_117	CH3_MOD_118	CH3_MOD_119	CH3_MOD_120	0xFF	0xFF	0xFF
	0x5F	CH3_MOD_121	CH3_MOD_122	CH3_MOD_123	CH3_MOD_124	CH3_MOD_125	CH3_MOD_126	CH3_MOD_127	CH3_MOD_128	0xFF	0xFF	0xFF

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 2	0x60	CH3_MOD_129	CH3_MOD_130	CH3_MOD_131	CH3_MOD_132	CH3_MOD_133	CH3_MOD_134	CH3_MOD_135	CH3_MOD_136	0xFF	0xFF	0xFF
	0x61	CH3_MOD_137	CH3_MOD_138	CH3_MOD_139	CH3_MOD_140	CH3_MOD_141	CH3_MOD_142	CH3_MOD_143	CH3_MOD_144	0xFF	0xFF	0xFF
	0x62	CH3_MOD_145	CH3_MOD_146	CH3_MOD_147	CH3_MOD_148	CH3_MOD_149	CH3_MOD_150	CH3_MOD_151	CH3_MOD_152	0xFF	0xFF	0xFF
	0x63	CH3_MOD_153	CH3_MOD_154	CH3_MOD_155	CH3_MOD_156	CH3_MOD_157	CH3_MOD_158	CH3_MOD_159	CH3_MOD_160	0xFF	0xFF	0xFF
	0x64	CH3_MOD_161	CH3_MOD_162	CH3_MOD_163	CH3_MOD_164	CH3_MOD_165	CH3_MOD_166	CH3_MOD_167	CH3_MOD_168	0xFF	0xFF	0xFF
	0x65	CH3_MOD_169	CH3_MOD_170	CH3_MOD_171	CH3_MOD_172	CH3_MOD_173	CH3_MOD_174	CH3_MOD_175	CH3_MOD_176	0xFF	0xFF	0xFF
	0x66	CH3_MOD_177	CH3_MOD_178	CH3_MOD_179	CH3_MOD_180	CH3_MOD_181	CH3_MOD_182	CH3_MOD_183	CH3_MOD_184	0xFF	0xFF	0xFF
	0x67	CH3_MOD_185	CH3_MOD_186	CH3_MOD_187	CH3_MOD_188	CH3_MOD_189	CH3_MOD_190	CH3_MOD_191	CH3_MOD_192	0xFF	0xFF	0xFF
	0x68	CH4_MOD_01	CH4_MOD_02	CH4_MOD_03	CH4_MOD_04	CH4_MOD_05	CH4_MOD_06	CH4_MOD_07	CH4_MOD_08	0xFF	0xFF	0xFF
	0x69	CH4_MOD_09	CH4_MOD_10	CH4_MOD_11	CH4_MOD_12	CH4_MOD_13	CH4_MOD_14	CH4_MOD_15	CH4_MOD_16	0xFF	0xFF	0xFF
	0x6A	CH4_MOD_17	CH4_MOD_18	CH4_MOD_19	CH4_MOD_20	CH4_MOD_21	CH4_MOD_22	CH4_MOD_23	CH4_MOD_24	0xFF	0xFF	0xFF
	0x6B	CH4_MOD_25	CH4_MOD_26	CH4_MOD_27	CH4_MOD_28	CH4_MOD_29	CH4_MOD_30	CH4_MOD_31	CH4_MOD_32	0xFF	0xFF	0xFF
	0x6C	CH4_MOD_33	CH4_MOD_34	CH4_MOD_35	CH4_MOD_36	CH4_MOD_37	CH4_MOD_38	CH4_MOD_39	CH4_MOD_40	0xFF	0xFF	0xFF
	0x6D	CH4_MOD_41	CH4_MOD_42	CH4_MOD_43	CH4_MOD_44	CH4_MOD_45	CH4_MOD_46	CH4_MOD_47	CH4_MOD_48	0xFF	0xFF	0xFF
	0x6E	CH4_MOD_49	CH4_MOD_50	CH4_MOD_51	CH4_MOD_52	CH4_MOD_53	CH4_MOD_54	CH4_MOD_55	CH4_MOD_56	0xFF	0xFF	0xFF
	0x6F	CH4_MOD_57	CH4_MOD_58	CH4_MOD_59	CH4_MOD_60	CH4_MOD_61	CH4_MOD_62	CH4_MOD_63	CH4_MOD_64	0xFF	0xFF	0xFF
	0x70	CH4_MOD_65	CH4_MOD_66	CH4_MOD_67	CH4_MOD_68	CH4_MOD_69	CH4_MOD_70	CH4_MOD_71	CH4_MOD_72	0xFF	0xFF	0xFF
	0x71	CH4_MOD_73	CH4_MOD_74	CH4_MOD_75	CH4_MOD_76	CH4_MOD_77	CH4_MOD_78	CH4_MOD_79	CH4_MOD_80	0xFF	0xFF	0xFF
	0x72	CH4_MOD_81	CH4_MOD_82	CH4_MOD_83	CH4_MOD_84	CH4_MOD_85	CH4_MOD_86	CH4_MOD_87	CH4_MOD_88	0xFF	0xFF	0xFF
	0x73	CH4_MOD_89	CH4_MOD_90	CH4_MOD_91	CH4_MOD_92	CH4_MOD_93	CH4_MOD_94	CH4_MOD_95	CH4_MOD_96	0xFF	0xFF	0xFF
	0x74	CH4_MOD_97	CH4_MOD_98	CH4_MOD_99	CH4_MOD_100	CH4_MOD_101	CH4_MOD_102	CH4_MOD_103	CH4_MOD_104	0xFF	0xFF	0xFF
	0x75	CH4_MOD_105	CH4_MOD_106	CH4_MOD_107	CH4_MOD_108	CH4_MOD_109	CH4_MOD_110	CH4_MOD_111	CH4_MOD_112	0xFF	0xFF	0xFF
	0x76	CH4_MOD_113	CH4_MOD_114	CH4_MOD_115	CH4_MOD_116	CH4_MOD_117	CH4_MOD_118	CH4_MOD_119	CH4_MOD_120	0xFF	0xFF	0xFF
	0x77	CH4_MOD_121	CH4_MOD_122	CH4_MOD_123	CH4_MOD_124	CH4_MOD_125	CH4_MOD_126	CH4_MOD_127	CH4_MOD_128	0xFF	0xFF	0xFF
	0x78	CH4_MOD_129	CH4_MOD_130	CH4_MOD_131	CH4_MOD_132	CH4_MOD_133	CH4_MOD_134	CH4_MOD_135	CH4_MOD_136	0xFF	0xFF	0xFF
	0x79	CH4_MOD_137	CH4_MOD_138	CH4_MOD_139	CH4_MOD_140	CH4_MOD_141	CH4_MOD_142	CH4_MOD_143	CH4_MOD_144	0xFF	0xFF	0xFF
	0x7A	CH4_MOD_145	CH4_MOD_146	CH4_MOD_147	CH4_MOD_148	CH4_MOD_149	CH4_MOD_150	CH4_MOD_151	CH4_MOD_152	0xFF	0xFF	0xFF
	0x7B	CH4_MOD_153	CH4_MOD_154	CH4_MOD_155	CH4_MOD_156	CH4_MOD_157	CH4_MOD_158	CH4_MOD_159	CH4_MOD_160	0xFF	0xFF	0xFF
	0x7C	CH4_MOD_161	CH4_MOD_162	CH4_MOD_163	CH4_MOD_164	CH4_MOD_165	CH4_MOD_166	CH4_MOD_167	CH4_MOD_168	0xFF	0xFF	0xFF
	0x7D	CH4_MOD_169	CH4_MOD_170	CH4_MOD_171	CH4_MOD_172	CH4_MOD_173	CH4_MOD_174	CH4_MOD_175	CH4_MOD_176	0xFF	0xFF	0xFF
0x7E	CH4_MOD_177	CH4_MOD_178	CH4_MOD_179	CH4_MOD_180	CH4_MOD_181	CH4_MOD_182	CH4_MOD_183	CH4_MOD_184	0xFF	0xFF	0xFF	
0x7F	CH4_MOD_185	CH4_MOD_186	CH4_MOD_187	CH4_MOD_188	CH4_MOD_189	CH4_MOD_190	CH4_MOD_191	CH4_MOD_192	0xFF	0xFF	0xFF	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 2	0x80	CH5_MOD_01	CH5_MOD_02	CH5_MOD_03	CH5_MOD_04	CH5_MOD_05	CH5_MOD_06	CH5_MOD_07	CH5_MOD_08	0xFF	0xFF	0xFF
	0x81	CH5_MOD_09	CH5_MOD_10	CH5_MOD_11	CH5_MOD_12	CH5_MOD_13	CH5_MOD_14	CH5_MOD_15	CH5_MOD_16	0xFF	0xFF	0xFF
	0x82	CH5_MOD_17	CH5_MOD_18	CH5_MOD_19	CH5_MOD_20	CH5_MOD_21	CH5_MOD_22	CH5_MOD_23	CH5_MOD_24	0xFF	0xFF	0xFF
	0x83	CH5_MOD_25	CH5_MOD_26	CH5_MOD_27	CH5_MOD_28	CH5_MOD_29	CH5_MOD_30	CH5_MOD_31	CH5_MOD_32	0xFF	0xFF	0xFF
	0x84	CH5_MOD_33	CH5_MOD_34	CH5_MOD_35	CH5_MOD_36	CH5_MOD_37	CH5_MOD_38	CH5_MOD_39	CH5_MOD_40	0xFF	0xFF	0xFF
	0x85	CH5_MOD_41	CH5_MOD_42	CH5_MOD_43	CH5_MOD_44	CH5_MOD_45	CH5_MOD_46	CH5_MOD_47	CH5_MOD_48	0xFF	0xFF	0xFF
	0x86	CH5_MOD_49	CH5_MOD_50	CH5_MOD_51	CH5_MOD_52	CH5_MOD_53	CH5_MOD_54	CH5_MOD_55	CH5_MOD_56	0xFF	0xFF	0xFF
	0x87	CH5_MOD_57	CH5_MOD_58	CH5_MOD_59	CH5_MOD_60	CH5_MOD_61	CH5_MOD_62	CH5_MOD_63	CH5_MOD_64	0xFF	0xFF	0xFF
	0x88	CH5_MOD_65	CH5_MOD_66	CH5_MOD_67	CH5_MOD_68	CH5_MOD_69	CH5_MOD_70	CH5_MOD_71	CH5_MOD_72	0xFF	0xFF	0xFF
	0x89	CH5_MOD_73	CH5_MOD_74	CH5_MOD_75	CH5_MOD_76	CH5_MOD_77	CH5_MOD_78	CH5_MOD_79	CH5_MOD_80	0xFF	0xFF	0xFF
	0x8A	CH5_MOD_81	CH5_MOD_82	CH5_MOD_83	CH5_MOD_84	CH5_MOD_85	CH5_MOD_86	CH5_MOD_87	CH5_MOD_88	0xFF	0xFF	0xFF
	0x8B	CH5_MOD_89	CH5_MOD_90	CH5_MOD_91	CH5_MOD_92	CH5_MOD_93	CH5_MOD_94	CH5_MOD_95	CH5_MOD_96	0xFF	0xFF	0xFF
	0x8C	CH5_MOD_97	CH5_MOD_98	CH5_MOD_99	CH5_MOD_100	CH5_MOD_101	CH5_MOD_102	CH5_MOD_103	CH5_MOD_104	0xFF	0xFF	0xFF
	0x8D	CH5_MOD_105	CH5_MOD_106	CH5_MOD_107	CH5_MOD_108	CH5_MOD_109	CH5_MOD_110	CH5_MOD_111	CH5_MOD_112	0xFF	0xFF	0xFF
	0x8E	CH5_MOD_113	CH5_MOD_114	CH5_MOD_115	CH5_MOD_116	CH5_MOD_117	CH5_MOD_118	CH5_MOD_119	CH5_MOD_120	0xFF	0xFF	0xFF
	0x8F	CH5_MOD_121	CH5_MOD_122	CH5_MOD_123	CH5_MOD_124	CH5_MOD_125	CH5_MOD_126	CH5_MOD_127	CH5_MOD_128	0xFF	0xFF	0xFF
	0x90	CH5_MOD_129	CH5_MOD_130	CH5_MOD_131	CH5_MOD_132	CH5_MOD_133	CH5_MOD_134	CH5_MOD_135	CH5_MOD_136	0xFF	0xFF	0xFF
	0x91	CH5_MOD_137	CH5_MOD_138	CH5_MOD_139	CH5_MOD_140	CH5_MOD_141	CH5_MOD_142	CH5_MOD_143	CH5_MOD_144	0xFF	0xFF	0xFF
	0x92	CH5_MOD_145	CH5_MOD_146	CH5_MOD_147	CH5_MOD_148	CH5_MOD_149	CH5_MOD_150	CH5_MOD_151	CH5_MOD_152	0xFF	0xFF	0xFF
	0x93	CH5_MOD_153	CH5_MOD_154	CH5_MOD_155	CH5_MOD_156	CH5_MOD_157	CH5_MOD_158	CH5_MOD_159	CH5_MOD_160	0xFF	0xFF	0xFF
	0x94	CH5_MOD_161	CH5_MOD_162	CH5_MOD_163	CH5_MOD_164	CH5_MOD_165	CH5_MOD_166	CH5_MOD_167	CH5_MOD_168	0xFF	0xFF	0xFF
	0x95	CH5_MOD_169	CH5_MOD_170	CH5_MOD_171	CH5_MOD_172	CH5_MOD_173	CH5_MOD_174	CH5_MOD_175	CH5_MOD_176	0xFF	0xFF	0xFF
	0x96	CH5_MOD_177	CH5_MOD_178	CH5_MOD_179	CH5_MOD_180	CH5_MOD_181	CH5_MOD_182	CH5_MOD_183	CH5_MOD_184	0xFF	0xFF	0xFF
	0x97	CH5_MOD_185	CH5_MOD_186	CH5_MOD_187	CH5_MOD_188	CH5_MOD_189	CH5_MOD_190	CH5_MOD_191	CH5_MOD_192	0xFF	0xFF	0xFF
	0x98	CH6_MOD_01	CH6_MOD_02	CH6_MOD_03	CH6_MOD_04	CH6_MOD_05	CH6_MOD_06	CH6_MOD_07	CH6_MOD_08	0xFF	0xFF	0xFF
	0x99	CH6_MOD_09	CH6_MOD_10	CH6_MOD_11	CH6_MOD_12	CH6_MOD_13	CH6_MOD_14	CH6_MOD_15	CH6_MOD_16	0xFF	0xFF	0xFF
	0x9A	CH6_MOD_17	CH6_MOD_18	CH6_MOD_19	CH6_MOD_20	CH6_MOD_21	CH6_MOD_22	CH6_MOD_23	CH6_MOD_24	0xFF	0xFF	0xFF
	0x9B	CH6_MOD_25	CH6_MOD_26	CH6_MOD_27	CH6_MOD_28	CH6_MOD_29	CH6_MOD_30	CH6_MOD_31	CH6_MOD_32	0xFF	0xFF	0xFF
	0x9C	CH6_MOD_33	CH6_MOD_34	CH6_MOD_35	CH6_MOD_36	CH6_MOD_37	CH6_MOD_38	CH6_MOD_39	CH6_MOD_40	0xFF	0xFF	0xFF
	0x9D	CH6_MOD_41	CH6_MOD_42	CH6_MOD_43	CH6_MOD_44	CH6_MOD_45	CH6_MOD_46	CH6_MOD_47	CH6_MOD_48	0xFF	0xFF	0xFF
0x9E	CH6_MOD_49	CH6_MOD_50	CH6_MOD_51	CH6_MOD_52	CH6_MOD_53	CH6_MOD_54	CH6_MOD_55	CH6_MOD_56	0xFF	0xFF	0xFF	
0x9F	CH6_MOD_57	CH6_MOD_58	CH6_MOD_59	CH6_MOD_60	CH6_MOD_61	CH6_MOD_62	CH6_MOD_63	CH6_MOD_64	0xFF	0xFF	0xFF	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 2	0xA0	CH6_MOD_65	CH6_MOD_66	CH6_MOD_67	CH6_MOD_68	CH6_MOD_69	CH6_MOD_70	CH6_MOD_71	CH6_MOD_72	0xFF	0xFF	0xFF
	0xA1	CH6_MOD_73	CH6_MOD_74	CH6_MOD_75	CH6_MOD_76	CH6_MOD_77	CH6_MOD_78	CH6_MOD_79	CH6_MOD_80	0xFF	0xFF	0xFF
	0xA2	CH6_MOD_81	CH6_MOD_82	CH6_MOD_83	CH6_MOD_84	CH6_MOD_85	CH6_MOD_86	CH6_MOD_87	CH6_MOD_88	0xFF	0xFF	0xFF
	0xA3	CH6_MOD_89	CH6_MOD_90	CH6_MOD_91	CH6_MOD_92	CH6_MOD_93	CH6_MOD_94	CH6_MOD_95	CH6_MOD_96	0xFF	0xFF	0xFF
	0xA4	CH6_MOD_97	CH6_MOD_98	CH6_MOD_99	CH6_MOD_100	CH6_MOD_101	CH6_MOD_102	CH6_MOD_103	CH6_MOD_104	0xFF	0xFF	0xFF
	0xA5	CH6_MOD_105	CH6_MOD_106	CH6_MOD_107	CH6_MOD_108	CH6_MOD_109	CH6_MOD_110	CH6_MOD_111	CH6_MOD_112	0xFF	0xFF	0xFF
	0xA6	CH6_MOD_113	CH6_MOD_114	CH6_MOD_115	CH6_MOD_116	CH6_MOD_117	CH6_MOD_118	CH6_MOD_119	CH6_MOD_120	0xFF	0xFF	0xFF
	0xA7	CH6_MOD_121	CH6_MOD_122	CH6_MOD_123	CH6_MOD_124	CH6_MOD_125	CH6_MOD_126	CH6_MOD_127	CH6_MOD_128	0xFF	0xFF	0xFF
	0xA8	CH6_MOD_129	CH6_MOD_130	CH6_MOD_131	CH6_MOD_132	CH6_MOD_133	CH6_MOD_134	CH6_MOD_135	CH6_MOD_136	0xFF	0xFF	0xFF
	0xA9	CH6_MOD_137	CH6_MOD_138	CH6_MOD_139	CH6_MOD_140	CH6_MOD_141	CH6_MOD_142	CH6_MOD_143	CH6_MOD_144	0xFF	0xFF	0xFF
	0xAA	CH6_MOD_145	CH6_MOD_146	CH6_MOD_147	CH6_MOD_148	CH6_MOD_149	CH6_MOD_150	CH6_MOD_151	CH6_MOD_152	0xFF	0xFF	0xFF
	0xAB	CH6_MOD_153	CH6_MOD_154	CH6_MOD_155	CH6_MOD_156	CH6_MOD_157	CH6_MOD_158	CH6_MOD_159	CH6_MOD_160	0xFF	0xFF	0xFF
	0xAC	CH6_MOD_161	CH6_MOD_162	CH6_MOD_163	CH6_MOD_164	CH6_MOD_165	CH6_MOD_166	CH6_MOD_167	CH6_MOD_168	0xFF	0xFF	0xFF
	0xAD	CH6_MOD_169	CH6_MOD_170	CH6_MOD_171	CH6_MOD_172	CH6_MOD_173	CH6_MOD_174	CH6_MOD_175	CH6_MOD_176	0xFF	0xFF	0xFF
	0xAE	CH6_MOD_177	CH6_MOD_178	CH6_MOD_179	CH6_MOD_180	CH6_MOD_181	CH6_MOD_182	CH6_MOD_183	CH6_MOD_184	0xFF	0xFF	0xFF
	0xAF	CH6_MOD_185	CH6_MOD_186	CH6_MOD_187	CH6_MOD_188	CH6_MOD_189	CH6_MOD_190	CH6_MOD_191	CH6_MOD_192	0xFF	0xFF	0xFF
	0xB0	CH7_MOD_01	CH7_MOD_02	CH7_MOD_03	CH7_MOD_04	CH7_MOD_05	CH7_MOD_06	CH7_MOD_07	CH7_MOD_08	0xFF	0xFF	0xFF
	0xB1	CH7_MOD_09	CH7_MOD_10	CH7_MOD_11	CH7_MOD_12	CH7_MOD_13	CH7_MOD_14	CH7_MOD_15	CH7_MOD_16	0xFF	0xFF	0xFF
	0xB2	CH7_MOD_17	CH7_MOD_18	CH7_MOD_19	CH7_MOD_20	CH7_MOD_21	CH7_MOD_22	CH7_MOD_23	CH7_MOD_24	0xFF	0xFF	0xFF
	0xB3	CH7_MOD_25	CH7_MOD_26	CH7_MOD_27	CH7_MOD_28	CH7_MOD_29	CH7_MOD_30	CH7_MOD_31	CH7_MOD_32	0xFF	0xFF	0xFF
	0xB4	CH7_MOD_33	CH7_MOD_34	CH7_MOD_35	CH7_MOD_36	CH7_MOD_37	CH7_MOD_38	CH7_MOD_39	CH7_MOD_40	0xFF	0xFF	0xFF
	0xB5	CH7_MOD_41	CH7_MOD_42	CH7_MOD_43	CH7_MOD_44	CH7_MOD_45	CH7_MOD_46	CH7_MOD_47	CH7_MOD_48	0xFF	0xFF	0xFF
	0xB6	CH7_MOD_49	CH7_MOD_50	CH7_MOD_51	CH7_MOD_52	CH7_MOD_53	CH7_MOD_54	CH7_MOD_55	CH7_MOD_56	0xFF	0xFF	0xFF
	0xB7	CH7_MOD_57	CH7_MOD_58	CH7_MOD_59	CH7_MOD_60	CH7_MOD_61	CH7_MOD_62	CH7_MOD_63	CH7_MOD_64	0xFF	0xFF	0xFF
	0xB8	CH7_MOD_65	CH7_MOD_66	CH7_MOD_67	CH7_MOD_68	CH7_MOD_69	CH7_MOD_70	CH7_MOD_71	CH7_MOD_72	0xFF	0xFF	0xFF
	0xB9	CH7_MOD_73	CH7_MOD_74	CH7_MOD_75	CH7_MOD_76	CH7_MOD_77	CH7_MOD_78	CH7_MOD_79	CH7_MOD_80	0xFF	0xFF	0xFF
	0xBA	CH7_MOD_81	CH7_MOD_82	CH7_MOD_83	CH7_MOD_84	CH7_MOD_85	CH7_MOD_86	CH7_MOD_87	CH7_MOD_88	0xFF	0xFF	0xFF
	0xBB	CH7_MOD_89	CH7_MOD_90	CH7_MOD_91	CH7_MOD_92	CH7_MOD_93	CH7_MOD_94	CH7_MOD_95	CH7_MOD_96	0xFF	0xFF	0xFF
0xBC	CH7_MOD_97	CH7_MOD_98	CH7_MOD_99	CH7_MOD_100	CH7_MOD_101	CH7_MOD_102	CH7_MOD_103	CH7_MOD_104	0xFF	0xFF	0xFF	
0xBD	CH7_MOD_105	CH7_MOD_106	CH7_MOD_107	CH7_MOD_108	CH7_MOD_109	CH7_MOD_110	CH7_MOD_111	CH7_MOD_112	0xFF	0xFF	0xFF	
0xBE	CH7_MOD_113	CH7_MOD_114	CH7_MOD_115	CH7_MOD_116	CH7_MOD_117	CH7_MOD_118	CH7_MOD_119	CH7_MOD_120	0xFF	0xFF	0xFF	
0xBF	CH7_MOD_121	CH7_MOD_122	CH7_MOD_123	CH7_MOD_124	CH7_MOD_125	CH7_MOD_126	CH7_MOD_127	CH7_MOD_128	0xFF	0xFF	0xFF	

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	NT	PAL	
B A N K 2	0xC0	CH7_MOD_129	CH7_MOD_130	CH7_MOD_131	CH7_MOD_132	CH7_MOD_133	CH7_MOD_134	CH7_MOD_135	CH7_MOD_136	0xFF	0xFF	0xFF
	0xC1	CH7_MOD_137	CH7_MOD_138	CH7_MOD_139	CH7_MOD_140	CH7_MOD_141	CH7_MOD_142	CH7_MOD_143	CH7_MOD_144	0xFF	0xFF	0xFF
	0xC2	CH7_MOD_145	CH7_MOD_146	CH7_MOD_147	CH7_MOD_148	CH7_MOD_149	CH7_MOD_150	CH7_MOD_151	CH7_MOD_152	0xFF	0xFF	0xFF
	0xC3	CH7_MOD_153	CH7_MOD_154	CH7_MOD_155	CH7_MOD_156	CH7_MOD_157	CH7_MOD_158	CH7_MOD_159	CH7_MOD_160	0xFF	0xFF	0xFF
	0xC4	CH7_MOD_161	CH7_MOD_162	CH7_MOD_163	CH7_MOD_164	CH7_MOD_165	CH7_MOD_166	CH7_MOD_167	CH7_MOD_168	0xFF	0xFF	0xFF
	0xC5	CH7_MOD_169	CH7_MOD_170	CH7_MOD_171	CH7_MOD_172	CH7_MOD_173	CH7_MOD_174	CH7_MOD_175	CH7_MOD_176	0xFF	0xFF	0xFF
	0xC6	CH7_MOD_177	CH7_MOD_178	CH7_MOD_179	CH7_MOD_180	CH7_MOD_181	CH7_MOD_182	CH7_MOD_183	CH7_MOD_184	0xFF	0xFF	0xFF
	0xC7	CH7_MOD_185	CH7_MOD_186	CH7_MOD_187	CH7_MOD_188	CH7_MOD_189	CH7_MOD_190	CH7_MOD_191	CH7_MOD_192	0xFF	0xFF	0xFF
	0xC8	CH8_MOD_01	CH8_MOD_02	CH8_MOD_03	CH8_MOD_04	CH8_MOD_05	CH8_MOD_06	CH8_MOD_07	CH8_MOD_08	0xFF	0xFF	0xFF
	0xC9	CH8_MOD_09	CH8_MOD_10	CH8_MOD_11	CH8_MOD_12	CH8_MOD_13	CH8_MOD_14	CH8_MOD_15	CH8_MOD_16	0xFF	0xFF	0xFF
	0xCA	CH8_MOD_17	CH8_MOD_18	CH8_MOD_19	CH8_MOD_20	CH8_MOD_21	CH8_MOD_22	CH8_MOD_23	CH8_MOD_24	0xFF	0xFF	0xFF
	0xCB	CH8_MOD_25	CH8_MOD_26	CH8_MOD_27	CH8_MOD_28	CH8_MOD_29	CH8_MOD_30	CH8_MOD_31	CH8_MOD_32	0xFF	0xFF	0xFF
	0xCC	CH8_MOD_33	CH8_MOD_34	CH8_MOD_35	CH8_MOD_36	CH8_MOD_37	CH8_MOD_38	CH8_MOD_39	CH8_MOD_40	0xFF	0xFF	0xFF
	0xCD	CH8_MOD_41	CH8_MOD_42	CH8_MOD_43	CH8_MOD_44	CH8_MOD_45	CH8_MOD_46	CH8_MOD_47	CH8_MOD_48	0xFF	0xFF	0xFF
	0xCE	CH8_MOD_49	CH8_MOD_50	CH8_MOD_51	CH8_MOD_52	CH8_MOD_53	CH8_MOD_54	CH8_MOD_55	CH8_MOD_56	0xFF	0xFF	0xFF
	0xCF	CH8_MOD_57	CH8_MOD_58	CH8_MOD_59	CH8_MOD_60	CH8_MOD_61	CH8_MOD_62	CH8_MOD_63	CH8_MOD_64	0xFF	0xFF	0xFF
	0xD0	CH8_MOD_65	CH8_MOD_66	CH8_MOD_67	CH8_MOD_68	CH8_MOD_69	CH8_MOD_70	CH8_MOD_71	CH8_MOD_72	0xFF	0xFF	0xFF
	0xD1	CH8_MOD_73	CH8_MOD_74	CH8_MOD_75	CH8_MOD_76	CH8_MOD_77	CH8_MOD_78	CH8_MOD_79	CH8_MOD_80	0xFF	0xFF	0xFF
	0xD2	CH8_MOD_81	CH8_MOD_82	CH8_MOD_83	CH8_MOD_84	CH8_MOD_85	CH8_MOD_86	CH8_MOD_87	CH8_MOD_88	0xFF	0xFF	0xFF
	0xD3	CH8_MOD_89	CH8_MOD_90	CH8_MOD_91	CH8_MOD_92	CH8_MOD_93	CH8_MOD_94	CH8_MOD_95	CH8_MOD_96	0xFF	0xFF	0xFF
	0xD4	CH8_MOD_97	CH8_MOD_98	CH8_MOD_99	CH8_MOD_100	CH8_MOD_101	CH8_MOD_102	CH8_MOD_103	CH8_MOD_104	0xFF	0xFF	0xFF
	0xD5	CH8_MOD_105	CH8_MOD_106	CH8_MOD_107	CH8_MOD_108	CH8_MOD_109	CH8_MOD_110	CH8_MOD_111	CH8_MOD_112	0xFF	0xFF	0xFF
	0xD6	CH8_MOD_113	CH8_MOD_114	CH8_MOD_115	CH8_MOD_116	CH8_MOD_117	CH8_MOD_118	CH8_MOD_119	CH8_MOD_120	0xFF	0xFF	0xFF
	0xD7	CH8_MOD_121	CH8_MOD_122	CH8_MOD_123	CH8_MOD_124	CH8_MOD_125	CH8_MOD_126	CH8_MOD_127	CH8_MOD_128	0xFF	0xFF	0xFF
	0xD8	CH8_MOD_129	CH8_MOD_130	CH8_MOD_131	CH8_MOD_132	CH8_MOD_133	CH8_MOD_134	CH8_MOD_135	CH8_MOD_136	0xFF	0xFF	0xFF
	0xD9	CH8_MOD_137	CH8_MOD_138	CH8_MOD_139	CH8_MOD_140	CH8_MOD_141	CH8_MOD_142	CH8_MOD_143	CH8_MOD_144	0xFF	0xFF	0xFF
	0xDA	CH8_MOD_145	CH8_MOD_146	CH8_MOD_147	CH8_MOD_148	CH8_MOD_149	CH8_MOD_150	CH8_MOD_151	CH8_MOD_152	0xFF	0xFF	0xFF
	0xDB	CH8_MOD_153	CH8_MOD_154	CH8_MOD_155	CH8_MOD_156	CH8_MOD_157	CH8_MOD_158	CH8_MOD_159	CH8_MOD_160	0xFF	0xFF	0xFF
	0xDC	CH8_MOD_161	CH8_MOD_162	CH8_MOD_163	CH8_MOD_164	CH8_MOD_165	CH8_MOD_166	CH8_MOD_167	CH8_MOD_168	0xFF	0xFF	0xFF
	0xDD	CH8_MOD_169	CH8_MOD_170	CH8_MOD_171	CH8_MOD_172	CH8_MOD_173	CH8_MOD_174	CH8_MOD_175	CH8_MOD_176	0xFF	0xFF	0xFF
	0xDE	CH8_MOD_177	CH8_MOD_178	CH8_MOD_179	CH8_MOD_180	CH8_MOD_181	CH8_MOD_182	CH8_MOD_183	CH8_MOD_184	0xFF	0xFF	0xFF
	0xDF	CH8_MOD_185	CH8_MOD_186	CH8_MOD_187	CH8_MOD_188	CH8_MOD_189	CH8_MOD_190	CH8_MOD_191	CH8_MOD_192	0xFF	0xFF	0xFF

Reserved BANK2 Register(0xE0~0xFF)

ADDRESS			0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
B A N K 2	0xE0	Def	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0xF0	Def	0x18	0x70	0x20	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	Bank
	NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	Bank
	PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	Bank

Reserved BANK3 Register(0x00~0x7F)

ADDRESS			0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
B A N K 3	0x00	Def	0xE0	0x09	0x0C	0x1F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x00
		NT	0xE0	0x09	0x0C	0x1F	0x00	0x20	0x60	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x03
		PAL	0xE0	0x09	0x0C	0x1F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x03
	0x10	Def	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x14	0x50	0x0C	0x00	0x88
		NT	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x20	0x50	0x0C	0xFF	0x88
		PAL	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x20	0x50	0x0C	0x00	0x88
	0x20	Def	0x80	0x24	0x23	0x00	0x2A	0xCC	0xF0	0x57	0x90	0x1F	0x52	0x78	0x00	0x68	0x00	0x07
		NT	0x84	0x24	0x23	0x00	0x2A	0xDC	0xF0	0x57	0x90	0x1F	0x52	0x78	0x00	0x68	0x00	0x07
		PAL	0x80	0x24	0x23	0x00	0x2A	0xCC	0xF0	0x57	0x90	0x1F	0x52	0x78	0x00	0x68	0x00	0x07
	0x30	Def	0xE0	0x43	0xA2	0x00	0x00	0x17	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
		NT	0xE0	0x43	0xA2	0x00	0x00	0x15	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
		PAL	0xE0	0x43	0xA2	0x00	0x00	0x17	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
	0x40	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x20	0x10	0x00	0x00
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x20	0x10	0x00	0x00
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x20	0x10	0x00	0x00
	0x50	Def	0x00	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x00	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x60	Def	0x53	0x53	0x21	0x00	0x22	0x22	0x22	0x22	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x53	0x53	0x21	0x00	0x22	0x22	0x22	0x22	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x53	0x53	0x21	0x00	0x22	0x22	0x22	0x22	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	Def	0xC0	0x01	0x06	0x06	0x11	0x00	0x0F	0x8F	0x0F	0x0F	0x0F	0x8F	0x0F	0x0F	0x00	0x00
		NT	0xC0	0x01	0x06	0x06	0x11	0x00	0xFF	0x80	0x00	0xFF	0xFF	0x80	0x00	0xFF	0x00	0x00
		PAL	0xC0	0x01	0x06	0x06	0x11	0x00	0xFF	0x80	0x00	0xFF	0xFF	0x80	0x00	0xFF	0x00	0x00

Reserved BANK3 Register(0x80~0xFF)

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
B A N K 3	0x80	Def	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08
		NT	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08
		PAL	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08
	0x90	Def	0x0D	0x0D	0x0D	0x0D	0x0D	0x0D	0x0D	0x0D	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
		NT	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
		PAL	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
	0xA0	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xC0	Def	0x10	0x10	0x0E	0x70	0x10	0x34	0x70	0x5C	0x40	0x20	0x30	0x40	0x50	0x08	0x28	0x20
		NT	0x10	0x70	0x0C	0x50	0x10	0x34	0x70	0x50	0x20	0x20	0x30	0x40	0x60	0x20	0x20	0x20
		PAL	0x10	0x10	0x0E	0x70	0x10	0x34	0x70	0x5C	0x40	0x20	0x30	0x40	0x50	0x08	0x28	0x20
	0xD0	Def	0x40	0x50	0x0E	0x00	0x00	0x00	0x00	0x00	0x39	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
		NT	0x40	0x50	0x0E	0x00	0x00	0x00	0x00	0x00	0xB9	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
		PAL	0x40	0x50	0x0E	0x00	0x00	0x00	0x00	0x00	0xB9	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
	0xE0	Def	0x21	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x21	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x21	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x86	0x04	0x05	0x93	0x22	0x5C	Bank
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x86	0x04	0x05	0x93	0x22	0x5C	Bank
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x86	0x04	0x05	0x93	0x22	0x5C	Bank

Reserved BANK4 Register(0x00~0x7F)

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
B A N K 4	0x00	Def	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
		NT	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
		PAL	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
	0x10	Def	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		NT	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		PAL	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x20	Def	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
		NT	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
		PAL	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
	0x30	Def	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		NT	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		PAL	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x40	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x64	0xFF	0x06	0x06	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x64	0xFF	0x06	0x06	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x50	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x60	Def	0x33	0x33	0x33	0x33	0xAA	0xAA	0xAA	0xAA	0x77	0x77	0x77	0x77	0x33	0x33	0x33	0x33
		NT	0x44	0x44	0x44	0x44	0x55	0x55	0x55	0x55	0x44	0x44	0x44	0x44	0x33	0x33	0x33	0x33
		PAL	0x33	0x33	0x33	0x33	0xAA	0xAA	0xAA	0xAA	0x77	0x77	0x77	0x77	0x33	0x33	0x33	0x33
	0x70	Def	0xFF	0x55	0x55	0x55	0x55	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0xFF	0x55	0x55	0x55	0x55	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0xFF	0x55	0x55	0x55	0x55	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

Reserved BANK4 Register(0x80~0xBF)

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F		
B A N K 4	0x80	Def	0x03	0x80	0x80	0x08	0x08	0x7E	0x00	0x80	0x80	0x80	0x14	0x13	0x00	0x03	0x80	0x00	
		NT	0x02	0x80	0x80	0x08	0x08	0x78	0x2A	0x80	0x80	0x80	0x14	0x01	0x00	0x01	0x80	0x00	
		PAL	0x03	0x80	0x80	0x08	0x08	0x7E	0x00	0x80	0x80	0x80	0x14	0x13	0x00	0x03	0x80	0x00	
	0x90	Def	0x00	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x00	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xA0	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		NT	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		PAL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

❖ Registers to Power down mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x02	PD_ADAC	[7]	0x00	0x00	PD_ADAC : Power down for AUDIO DAC 0 : ON 1 : OFF
		PD_VCH4	[3]			PD_VCH4 : Power down for CH4 Video AFE PD_VCH3 : Power down for CH3 Video AFE PD_VCH2 : Power down for CH2 Video AFE PD_VCH1 : Power down for CH1 Video AFE 0 : ON 1 : OFF
		PD_VCH3	[2]			
		PD_VCH2	[1]			
		PD_VCH1	[0]			
	0x82	PD_VCH8	[3]	0x0	0x0	PD_VCH8 : Power down for CH8 Video AFE PD_VCH7 : Power down for CH7 Video AFE PD_VCH6 : Power down for CH6 Video AFE PD_VCH5 : Power down for CH5 Video AFE 0 : ON 1 : OFF
		PD_VCH7	[2]			
		PD_VCH6	[1]			
		PD_VCH5	[0]			

❖ Registers to Control Comb Filter and Video Format

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION		
Bank	Addr			NTSC	PAL			
0	0x08	AUTO_1	[7]	0xA0	0xDD	AUTO_x : A register to set the Auto Detect Mode On/Off; When the AUTO mode has a high value, the Auto_NT_x bit value of the STATUS Register(BANK1, 0xEF / 0xF0) is to be confirmed to distinguish NTSC-M/J and PAL-B / D / G / H standards. It does not support other standards, and when used in link with the DVR controller, it cannot be used in the NON_REAL_TIME mode. (x = channel 1~8) 0 : Auto Detect OFF 1 : Auto Detect ON		
	0x09	AUTO_2						
	0x0A	AUTO_3						
	0x0B	AUTO_4						
	0x88	AUTO_5						
	0x89	AUTO_6						
	0x8A	AUTO_7						
	0x8B	AUTO_8						
	0x08	BSF_MODE_1	[6:5]			0xA0	0xDD	BSF_MODE_x : Selects the filter to make primary separation of the brightness and color signals. (x = channel 1~8) 00 : 9.6M LPF 01 : Mode 1 (2.7~5.4MHz Cut-off) 10 : Mode 2 (3.5~5.6MHz Cut-off) 11 : Manual(BANK3,0xE0 ~ 0xF2)
	0x09	BSF_MODE_2						
	0x0A	BSF_MODE_3						
	0x0B	BSF_MODE_4						
	0x88	BSF_MODE_5						
	0x89	BSF_MODE_6						
	0x8A	BSF_MODE_7						
	0x8B	BSF_MODE_8						
	0x08	VIDEO_FORMAT_1	[4:0]			0xA0	0xDD	VIDEO_FORMAT_x : A register to determine the video standards of the input signal (x = channel 1~8) 00000 : NTSC-M,J 10001 : NTSC-4.43 11101 : PAL-B,D,G,H,I 10110 : PAL-M 11111 : PAL-Nc 10101 : PAL-60 Others : None
	0x09	VIDEO_FORMAT_2						
	0x0A	VIDEO_FORMAT_3						
	0x0B	VIDEO_FORMAT_4						
	0x88	VIDEO_FORMAT_5						
	0x89	VIDEO_FORMAT_6						
	0x8A	VIDEO_FORMAT_7						
	0x8B	VIDEO_FORMAT_8						

❖ Registers to Control Low Pass Filter

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x18	Y_FIR_MODE_1	[3:0]	0x88 (960H) / 0x44 (720H)	0x88 (960H) / 0x44 (720H)	Y_FIR_MODE_x : Y Low Pass Filter control. (x = channel 1~8) 0000 : bypass 0001 : 6MHz 0010 : 6.5MHz 0011 : 7MHz 0100 : 7.5MHz 0101 : 8MHz 0110 : 8.5MHz 0111 : 9MHz 1000 : 9.5MHz
		Y_FIR_MODE_2	[7:4]			
	0x19	Y_FIR_MODE_3	[3:0]			
		Y_FIR_MODE_4	[7:4]			
	0x98	Y_FIR_MODE_5	[3:0]			
		Y_FIR_MODE_6	[7:4]			
	0x99	Y_FIR_MODE_7	[3:0]			
		Y_FIR_MODE_8	[7:4]			

❖ Registers to Control Peaking Filter

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x1A	Y_PEAK_MODE_1	[3:0]	0x11	0x11	Y_PEAK_MODE_x : Y Peaking Filter control. (x = channel 1~8) 0000 : 0dB 0001 : 2dB 0010 : 3.5dB 0011 : 6dB 0100 ~ 1111 : Don't use
		Y_PEAK_MODE_2	[7:4]			
	0x1B	Y_PEAK_MODE_3	[3:0]			
		Y_PEAK_MODE_4	[7:4]			
	0x9A	Y_PEAK_MODE_5	[3:0]			
		Y_PEAK_MODE_6	[7:4]			
	0x9B	Y_PEAK_MODE_7	[3:0]			
		Y_PEAK_MODE_8	[7:4]			

❖ Registers to Control Pedestal

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x1C	PED_ON_1	[6]	0xA4	0xA2	PED_ON_x : Select to Pedestal ON/OFF (x = channel 1~8) 0 : Pedestal OFF 1 : Pedestal ON
	0x1D	PED_ON_2				
	0x1E	PED_ON_3				
	0x1F	PED_ON_4				
	0x9C	PED_ON_5				
	0x9D	PED_ON_6				
	0x9E	PED_ON_7				
	0x9F	PED_ON_8				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x38	CTI_GAIN_1	[7:0]	0x0A	0x0A	CTI_GAIN_x[7:6] : Adjust CTI Gain Delay
	0x39	CTI_GAIN_2				
	0x3A	CTI_GAIN_3				
	0x3B	CTI_GAIN_4				
	0xB8	CTI_GAIN_5				
	0xB9	CTI_GAIN_6				
	0xBA	CTI_GAIN_7				
	0xBB	CTI_GAIN_8				
	0x3C	SATURATION_1	[7:0]	0x80	0x80	SATURATION_x : Color Gain Value (Adjustable up to x2) (x = channel 1~8) 00000000 : x 0 10000000 : x 1 11000000 : x 1.5 11111111 : x 2
	0x3D	SATURATION_2				
	0x3E	SATURATION_3				
	0x3F	SATURATION_4				
	0xBC	SATURATION_5				
	0xBD	SATURATION_6				
	0xBE	SATURATION_7				
	0xBF	SATURATION_8				
	0x40	HUE_1	[7:0]	0x01	0x00	HUE_x : Color HUE Control Value (360°/256 per HUE Value 1 unit) (x = channel 1~8) 00000000 : 0° 01000000 : 90° 10000000 : 180° 11111111 : 360°
	0x41	HUE_2				
	0x42	HUE_3				
	0x43	HUE_4				
	0xC0	HUE_5				
	0xC1	HUE_6				
	0xC2	HUE_7				
	0xC3	HUE_8				
	0x44	U_GAIN_1	[7:0]	0x30	0x30	U_GAIN_x : U Gain Value (Adjustable up to x2) (x = channel 1~8) 00000000 : x 0 10000000 : x 1 11000000 : x 1.5 11111111 : x 2
	0x45	U_GAIN_2				
	0x46	U_GAIN_3				
	0x47	U_GAIN_4				
	0xC4	U_GAIN_5				
	0xC5	U_GAIN_6				
	0xC6	U_GAIN_7				
	0xC7	U_GAIN_8				
0x48	V_GAIN_1	[7:0]	0x30	0x00	V_GAIN_x : V Gain Value (Adjustable up to x2) (x = channel 1~8) 00000000 : x 0 10000000 : x 1 11000000 : x 1.5 11111111 : x 2	
0x49	V_GAIN_2					
0x4A	V_GAIN_3					
0x4B	V_GAIN_4					
0xC8	V_GAIN_5					
0xC9	V_GAIN_6					
0xCA	V_GAIN_7					
0xCB	V_GAIN_8					

❖ Registers to Control Channel ID

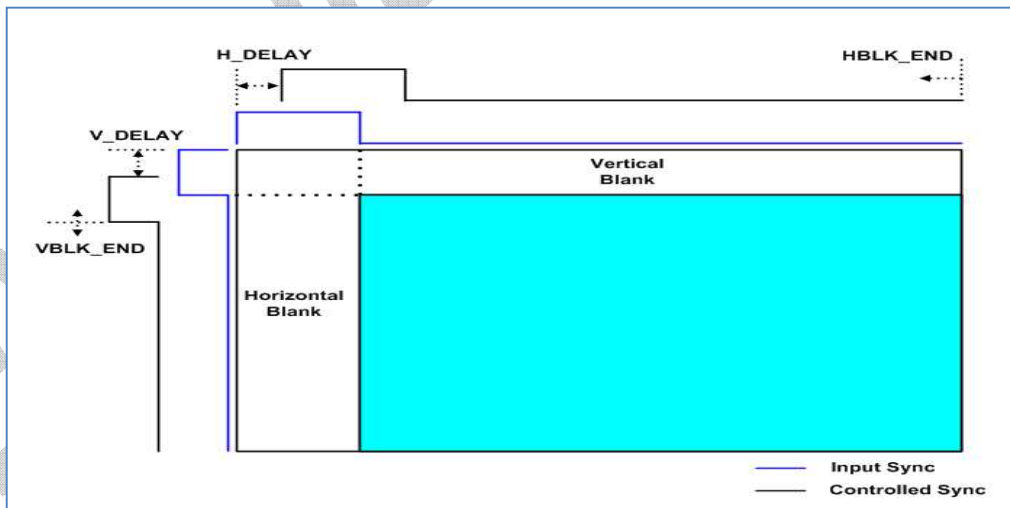
ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x54	CHID_TYPE_14	[2:0]	0x1	0x1	CHID_TYPE_x : It determines type of channel ID.(x = channel 1~8)
	0xD4	CHID_TYPE_58				
	0x55	CHID_VIN_1	[3:0]	0x10	0x10	CHID_VIN_x : Register to put CHANNEL ID to distinguish channel. (0x0~0xF) (x = channel 1~8)
		CHID_VIN_2	[7:4]			
	0x56	CHID_VIN_3	[3:0]	0x32	0x32	
		CHID_VIN_4	[7:4]			
	0xD5	CHID_VIN_5	[3:0]	0x54	0x54	
		CHID_VIN_6	[7:4]			
0xD6	CHID_VIN_7	[3:0]	0x76	0x76		
	CHID_VIN_8	[7:4]				

❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x58	H_DELAY_1	[7:0]	0x44	0x45	H_DELAY_x : Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal. (x = channel 1~8)
	0x59	H_DELAY_2				
	0x5A	H_DELAY_3				
	0x5B	H_DELAY_4				
	0xD8	H_DELAY_5				
	0xD9	H_DELAY_6				
	0xDA	H_DELAY_7				
	0xDB	H_DELAY_8				
	0x5C	V_DELAY_1	[7:0]	0x1E	0x1E	V_DELAY_x[7:6] : Select to vblk_str_fid (x = channel 1~8) 00 : evenfld 01 : !evenfld 10 : 0 11 : 1
	0x5D	V_DELAY_2				
	0x5E	V_DELAY_3				
	0x5F	V_DELAY_4				
	0xDC	V_DELAY_5				
	0xDD	V_DELAY_6				
	0xDE	V_DELAY_7				
0xDF	V_DELAY_8					

❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x60	HBLK_END_1	[7:0]	0x00	0x00	HBLK_END_x : Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed. (x = channel 1~8)
	0x61	HBLK_END_2				
	0x62	HBLK_END_3				
	0x63	HBLK_END_4				
	0xE0	HBLK_END_5				
	0xE1	HBLK_END_6				
	0xE2	HBLK_END_7				
	0xE3	HBLK_END_8				
	0x64	VBLK_END_1	[7:0]	0x08	0x0D	VBLK_END_x[7:6] : Select to vblk_end_fld (x = channel 1~8) 00 : evenfld 01 : levenfld 10 : 0 11 : 1 VBLK_END_x[5] : VBLK_END_x[4:0] Control Enable (x = channel 1~8) VBLK_END_x[4:0] (When VBLK_END_x[5] = 1) : Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then the Active region is changed. (x = channel 1~8)
	0x65	VBLK_END_2				
	0x66	VBLK_END_3				
	0x67	VBLK_END_4				
	0xE4	VBLK_END_5				
	0xE5	VBLK_END_6				
	0xE6	VBLK_END_7				
	0xE7	VBLK_END_8				



❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x68	H_CROP_S_1	[7:0]	0x00	0x00	H_CROP_S_x : Adjust the horizontal crop start point. (x = channel 1~8)
	0x69	H_CROP_S_2				
	0x6A	H_CROP_S_3				
	0x6B	H_CROP_S_4				
	0xE8	H_CROP_S_5				
	0xE9	H_CROP_S_6				
	0xEA	H_CROP_S_7				
	0xEB	H_CROP_S_8				
	0x6C	H_CROP_E_1	[7:0]	0x00	0x00	H_CROP_E_x : Adjust the horizontal crop end point. (x = channel 1~8)
	0x6D	H_CROP_E_2				
	0x6E	H_CROP_E_3				
	0x6F	H_CROP_E_4				
	0xEC	H_CROP_E_5				
	0xED	H_CROP_E_6				
	0xEE	H_CROP_E_7				
	0xEF	H_CROP_E_8				
	0x70	V_CROP_S_1	[7:0]	0x00	0x00	V_CROP_S_x : Adjust the vertical crop start point. (x = channel 1~8)
	0x71	V_CROP_S_2				
	0x72	V_CROP_S_3				
	0x73	V_CROP_S_4				
	0xF0	V_CROP_S_5				
	0xF1	V_CROP_S_6				
	0xF2	V_CROP_S_7				
	0xF3	V_CROP_S_8				
0x74	V_CROP_E_1	[7:0]	0x00	0x00	V_CROP_E_x : Adjust the vertical crop end point. (x = channel 1~8)	
0x75	V_CROP_E_2					
0x76	V_CROP_E_3					
0x77	V_CROP_E_4					
0xF4	V_CROP_E_5					
0xF5	V_CROP_E_6					
0xF6	V_CROP_E_7					
0xF7	V_CROP_E_8					

❖ Registers to Control Back Ground Color

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x78	BGDCOL_1	[3:0]	0x88	0x88	BGDCOL_x : When No-Video, BackGround Color is used. (x = channel 1~8) 0000 : Blue 0001 : White (75%) 0010 : Yellow 0011 : Cyan 0100 : Green 0101 : Magenta 0110 : Red 0111 : Blue 1000 : Black 1001 : Gray 1010 : Red (NEXTCHIP [®]) 1011 : Yellow (NEXTCHIP [®]) 1100 : Magenta (NEXTCHIP [®]) 1101 : Green (NEXTCHIP [®]) 1110 : Blue (NEXTCHIP [®]) 1111 : Cyan (NEXTCHIP [®]) * These color information is exactly same as controllers provided by NEXTCHIP
		BGDCOL_2	[7:4]			
	0x79	BGDCOL_3	[3:0]			
		BGDCOL_4	[7:4]			
	0xF8	BGDCOL_5	[3:0]			
		BGDCOL_6	[7:4]			
	0xF9	BGDCOL_7	[3:0]			
		BGDCOL_8	[7:4]			

❖ Registers to Control Data Out Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
0	0x7A	DATA_OUT_MODE_1	[3:0]	0x11	0x11	DATA_OUT_MODE_x : It limits a level of output data, can change signals of Cb and Cr each. (x = channel 1~8) 0000 : Y(016~235), Cb(016~240), Cr(016~240) 0001 : Y(001~254), Cb(001~254), Cr(001~254) 0010 : Y(000~255), Cb(000~255), Cr(000~255) 0011 : Cb / Cr Change, 016~235 0100 : Cb / Cr Change, 001~254 0101 : Cb / Cr Kill, 016~235 0110 : Cb / Cr Kill, 001~254 Others : Background color output
		DATA_OUT_MODE_2	[7:4]			
	0x7B	DATA_OUT_MODE_3	[3:0]			
		DATA_OUT_MODE_4	[7:4]			
	0xFA	DATA_OUT_MODE_5	[3:0]			
		DATA_OUT_MODE_6	[7:4]			
	0xFB	DATA_OUT_MODE_7	[3:0]			
		DATA_OUT_MODE_8	[7:4]			

❖ Registers to Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
	0x06	CAS_PB	[7]	0x1B	0x1B	CAS_PB : The Usage of Playback Data when Cascade Mode 0 : use multiple playback data, received through all stage 1 : use single playback data, received through last stage
		TRANS_MODE	[6]			TRANS_MODE : Control the phase between transferred clock and cascade data 0 : Same phase 1 : Inverted phase
		CAS_4CH	[5]			CAS_4CH : Audio Cascade Channels selection 0 : 8 Channels 1 : 4 Channels
		CAS_PIN	[4]			CAS_PIN : Control the usage of ADATA_CASI and ADATA_CASO as cascade transmitting 0 : Don't Use 1 : Use
		CHIP_STAGE	[1:0]			CHIP_STAGE : Selection of chip state for cascade 0 : middle stage 1 : last stage 2 : first stage 3 : single chip operation
1	0x07	RM_MASTER	[7]	0xC8	0xC8	RM_MASTER : Selection of master & slave mode of ACLK_REC and ASYNC_REC 0 : Slave mode operation 1 : Master mode operation
		RM_CLK	[6]			RM_CLK : Set the relationship between audio signal outputted to ADATA_REC and clock outputted to ACLK_REC 0 : inverted clock 1 : non-inverted clock
		RM_BITRATE	[5:4]			RM_BITRATE : Set the bit rate of audio signal outputted to ADATA_REC 0 : 256fs 1 : 384fs 2 : 320fs 3 : Don't Use
		RM_SAMRATE	[3]			RM_SAMRATE : Set the sampling rate of data outputted to ADATA_REC 0 : 8KHz 1 : 16KHz
		RM_BITWID	[2]			RM_BITWID : Set the bit width of data outputted to ADATA_REC 0 : 16bits 1 : 8bits
		RM_SSP	[1]			RM_SSP : Selection of DSP mode and SSP mode for ADATA_REC pin, when ASYNC_REC is DSP mode. 0 : DSP mode 1 : SSP mode
		RM_SYNC	[0]			RM_SYNC : Set the sync's mode inputted/outputted to ASYNC_REC. 0 : I2S mode 1 : DSP mode

❖ Registers to Control Audio interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x08	RM_BIT_SWAP	[7]	0x03	0x03	RM_BIT_SWAP : Set the bit sequence of Audio Data for ADATA_REC 0 : MSB first 1 : LSB first
		RM_LAW_SEL	[6]			RM_LAW_SEL : Define the G.711 data format outputted to ADATA_REC 0 : u-law 1 : a-law
		RM_FORMAT	[5:4]			RM_FORMAT : Define the data format outputted to ADATA_REC 0 : linear PCM 1 : Unsigned linear PCM 2 : G.711 format 3 : Don't Use
		R_ADATSP2	[3]			R_ADATSP : Selection of output data for ADATA_SP 0 : Speaker data 1 : Record data
		R_ADATSP	[2]			
		R_MULTCH	[1:0]			

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x09	R_SEQ_01[4]	[0]	0x0	0x0	R_SEQ : Sequence of Audio Data for ADATA_REC 00000 : channel 1 data 00001 : channel 2 data 00010 : channel 3 data 00011 : channel 4 data 00100 : channel 5 data 00101 : channel 6 data 00110 : channel 7 data 00111 : channel 8 data 01000 : channel 9 data 01001 : channel 10 data 01010 : channel 11 data 01011 : channel 12 data 01100 : channel 13 data 01101 : channel 14 data 01110 : channel 15 data 01111 : channel 16 data 10000 : Mic input 1 10001 : Mic input 2
		R_SEQ_02[4]	[1]	0x0	0x0	
		R_SEQ_03[4]	[2]	0x0	0x0	
		R_SEQ_04[4]	[3]	0x0	0x0	
		R_SEQ_05[4]	[4]	0x0	0x0	
		R_SEQ_06[4]	[5]	0x0	0x0	
		R_SEQ_07[4]	[6]	0x0	0x0	
		R_SEQ_08[4]	[7]	0x0	0x0	
	0x0A	R_SEQ_01	[3:0]	0x10	0x10	
		R_SEQ_02	[7:4]			
	0x0B	R_SEQ_03	[3:0]	0x32	0x32	
		R_SEQ_04	[7:4]			
	0x0C	R_SEQ_05	[3:0]	0x54	0x54	
		R_SEQ_06	[7:4]			
	0x0D	R_SEQ_07	[3:0]	0x76	0x76	
		R_SEQ_08	[7:4]			

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x0E	R_SEQ_09[4]	[0]	0x0	0x0	R_SEQ : Sequence of Audio Data for ADATA_REC 00000 : channel 1 data 00001 : channel 2 data 00010 : channel 3 data 00011 : channel 4 data 00100 : channel 5 data 00101 : channel 6 data 00110 : channel 7 data 00111 : channel 8 data 01000 : channel 9 data 01001 : channel 10 data 01010 : channel 11 data 01011 : channel 12 data 01100 : channel 13 data 01101 : channel 14 data 01110 : channel 15 data 01111 : channel 16 data 10000 : Mic input 1 10001 : Mic input 2
		R_SEQ_10[4]	[1]	0x0	0x0	
		R_SEQ_11[4]	[2]	0x0	0x0	
		R_SEQ_12[4]	[3]	0x0	0x0	
		R_SEQ_13[4]	[4]	0x0	0x0	
		R_SEQ_14[4]	[5]	0x0	0x0	
		R_SEQ_15[4]	[6]	0x0	0x0	
		R_SEQ_16[4]	[7]	0x0	0x0	
	0x0F	R_SEQ_09	[3:0]	0x98	0x98	
		R_SEQ_10	[7:4]			
	0x10	R_SEQ_11	[3:0]	0xBA	0xBA	
		R_SEQ_12	[7:4]			
	0x11	R_SEQ_13	[3:0]	0xDC	0xDC	
		R_SEQ_14	[7:4]			
	0x12	R_SEQ_15	[3:0]	0xFE	0xFE	
		R_SEQ_16	[7:4]			
	0x3C	MIC_SEQ_01	[4:0]	0x00	0x00	
	0x3D	MIC_SEQ_02	[4:0]	0x00	0x00	

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x13	PB_MASTER	[7]	0x08	0x08	PB_MASTER : Selection of master & slave mode of ACLK_PB and ASYNC_PB 0 : Slave mode 1 : Master mode
		PB_CLK	[6]			PB_CLK : Set the relationship between audio signal outputted to ADATA_PB and clock outputted to ACLK_PB 0 : inverted clock 1 : non-inverted clock
		PB_BITRATE	[5:4]			PB_BITRATE : Set the bit rate of audio signal outputted to ADATA_PB 0 : 256fs 1 : 384fs 2 : 320fs
		PB_SAMRATE	[3]			PB_SAMRATE : Set the sampling rate of data outputted to ADATA_PB 0 : 8KHz 1 : 16KHz
		PB_BITWID	[2]			PB_BITWID : Set the bit width of data outputted to ADATA_PB 0 : 16bits 1 : 8bits
		PB_SSP	[1]			PB_SSP : Set the position of data and sync signals inputted to ADATA_PB, when ASYNC_PB is DSP mode. 0 : DSP mode 1 : SSP mode
		PB_SYNC	[0]			PB_SYNC : Set the sync's mode inputted/outputted to ASYNC_PB. 0 : I2S mode 1 : DSP mode

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION	
Bank	Addr			NTSC	PAL		
1	0x14	PB_BIT_SWAP	[7]	0x00	0x00	PB_BIT_SWAP : Set the bit sequence of Audio Data for ADATA_PB 0 : MSB first 1 : LSB first	
		PB_SEL	[4:0]			PB_SEL : select the audio input channel for playback input 00 : channel 01 01 : channel 02 02 : channel 03 03 : channel 04 04 : channel 05 05 : channel 06 06 : channel 07 07 : channel 08 08 : channel 09 09 : channel 10 0A : channel 11 0B : channel 12 0C : channel 13 0D : channel 14 0E : channel 15 0F : channel 16 10 : Mic input 1 11 : Mic input 2	
	PB_FORMAT	[7:6]	0x00			0x00	PB_FORMAT : Define the data format inputted to ADATA_PB 0 : linear PCM 1 : Unsigned linear PCM 2 : G.711 format 3 : Don't Use
	PB_LAW_SEL	[3]					PB_LAW_SEL : Define the G.711 data format inputted to ADATA_PB 0 : u-law 1 : a-law

❖ Registers to Control Audio Mixing Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x16	MIX_RATIO_01	[3:0]	0x88	0x88	MIX_RATIO_x : Set the mixing gain for AIN1-15. (x = channel 1~16) 0 : mute 1 : 0.25 2 : 0.31 3 : 0.38 4 : 0.5 5 : 0.63 6 : 0.75 7 : 0.88 8 : 1.0 9 : 1.25 10 : 1.5 11 : 1.75 12 : 2.0 13 : 2.25 14 : 2.5 15 : 2.75
		MIX_RATIO_02	[7:4]			
	0x17	MIX_RATIO_03	[3:0]			
		MIX_RATIO_04	[7:4]			
	0x18	MIX_RATIO_05	[3:0]			
		MIX_RATIO_06	[7:4]			
	0x19	MIX_RATIO_07	[3:0]			
		MIX_RATIO_08	[7:4]			
	0x1A	MIX_RATIO_09	[3:0]			
		MIX_RATIO_10	[7:4]			
	0x1B	MIX_RATIO_11	[3:0]			
		MIX_RATIO_12	[7:4]			
	0x1C	MIX_RATIO_13	[3:0]			
		MIX_RATIO_14	[7:4]			
	0x1D	MIX_RATIO_15	[3:0]			
		MIX_RATIO_16	[7:4]			

❖ Registers to Control Analog and Digital Mixing output

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x24	L_CH_OUTSEL	[4:0]	0x18	0x18	L_CH_OUTSEL / R_CH_OUTSEL : Select Left/Right channel of the audio output for ADATA_SP pin 00 : Channel 1 0E : Channel 15 01 : Channel 2 0F : Channel 16 02 : Channel 3 10 : playback audio 03 : Channel 4 11 : second playback audio 04 : Channel 5 (first stage playback audio) 05 : Channel 6 (middle stage playback audio) 06 : Channel 7 12 : third playback audio 07 : Channel 8 13 : fourth playback audio 08 : Channel 9 (middle stage playback audio) 09 : Channel 10 (middle stage playback audio) 0A : Channel 11 14 : Mic input 1 0B : Channel 12 15 : Mic input 2 0C : Channel 13 18 : Mixed audio 0D : Channel 14 Others : No audio output
	0x25	R_CH_OUTSEL	[4:0]	0x16	0x16	

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x26	MIX_MUTE_01	[0]	0x00	0x00	MIX_MUTE_x : During mixing, selected channels are muted (x = channel value) 0 : mixing data output 1 : mute for selected channel
		MIX_MUTE_02	[1]			
		MIX_MUTE_03	[2]			
		MIX_MUTE_04	[3]			
		MIX_MUTE_05	[4]			
		MIX_MUTE_06	[5]			
		MIX_MUTE_07	[6]			
		MIX_MUTE_08	[7]			
	0x27	MIX_MUTE_09	[0]			
		MIX_MUTE_10	[1]			
		MIX_MUTE_11	[2]			
		MIX_MUTE_12	[3]			
		MIX_MUTE_13	[4]			
		MIX_MUTE_14	[5]			
		MIX_MUTE_15	[6]			
		MIX_MUTE_16	[7]			
	0x28	MIX_MUTE_P1	[0]			
		MIX_MUTE_P2	[1]			
		MIX_MUTE_P3	[2]			
		MIX_MUTE_P4	[3]			
		MIX_MUTE_M1	[4]			
		MIX_MUTE_M2	[5]			
		MIX_MUTE_M3	[6]			
		MIX_MUTE_M4	[7]			

❖ Registers to Control Audio CLK

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x38	AUD_SW_RST	[4]	0x08	0x08	AUD_SW_RST : Software Reset 0 : Normal Operation 1 : Reset

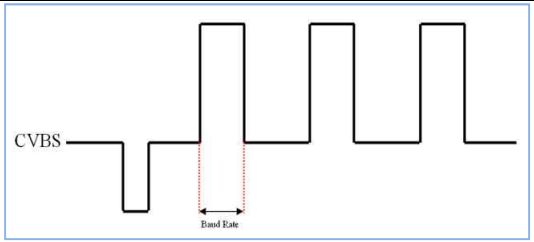
❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x39	RM_DELAY	[7]	0x01	0x01	RM_DELAY : ASYNCN_REC 를 원래보다 54MHz 기준으로 1 clk delay 0 : default 1 : 1clk delay
		PB_DELAY	[6]			PB_DELAY : ASYNCN_PB 를 원래보다 54MHz 기준으로 1 clk delay 0 : default 1 : 1clk delay

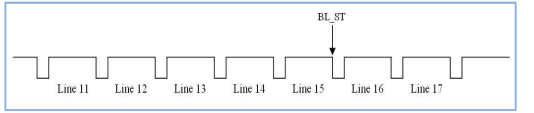
❖ Registers to Audio Enable

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x5E	AUD_72M	[7]	0x00 (960H) / 0x80 (720H)	0x00 (960H) / 0x80 (720H)	AUD_72M : Audio 72Mhz Enable Signal 0 : Audio 72Mhz Mode 1 : Audio 54Mhz Mode

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x50	BAUD	[7:0]	0x37	0x37	BAUD : Samsung TX Baud Rate
	0x51	RBAUD	[7:0]	0x37	0x37	RBAUD : Samsung RX Baud Rate
	0x52	PELCO_BAUD	[7:0]	0x1B	0x1B	PELCO_BAUD : PELCO TX Baud Rate
Coaxial protocol 1H Line						

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x53	BL_TXST_01	[7:0]	0x05	0x05	BL_TXST_01 : Samsung Protocol TX start Line in VBI BL_TXST_01 is Lower 8bit
	0x54	BL_TXST_02	[3:0]	0x00	0x00	BL_TXST_02 : Samsung Protocol TX start Line in VBI BL_TXST_02 is upper 4bit
	0x55	BL_RXST_01	[7:0]	0x07	0x07	BL_RXST_01 : Samsung Protocol RX Start Line in VBI BL_RXST_01 is Lower 8bit
	0x56	BL_RXST_02	[3:0]	0x00	0x00	BL_RXST_02 : Samsung Protocol RX Start Line in VBI BL_RXST_02 is upper 8bit
	0x57	PELCO_TXST_01	[7:0]	0x09	0x09	PELCO_TXST_01 : PELCO Protocol TX Start Line in VBI PELCO_TXST_01 is lower 8bit
	0x58	PELCO_TXST_02	[3:0]	0x00	0x00	PELCO_TXST_02 : PELCO Protocol TX Start Line in VBI PELCO_TXST_02 is upper 8bit
Coaxial protocol Active Start Point of VBI(Vertical Blank Interval)						

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x59	TX_START	[0]	0x00	0x00	TX_START : Samsung Protocol Enable Signal
	0x5A	TX_BYTE_LENGTH	[4:0]	0x08	0x08	TX_BYTE_LENGTH : Transmission amount In Samsung Protocol
	0x5B	PACKET_MODE	[2:0]	0x06	0x06	PACKET_MODE : Coaxial Protocol Type 0 : Samsung Protocol 2 Line Mode 1 : Samsung Protocol 4 Line Mode 2 : Pelco Protocol Origin Mode 4 : Pelco Protocol Exp mode
	0x5C	PELCO_CTEN	[0]	0x00	0x00	PELCO_CTEN : PELCO Protocol Enable Bit (Active High)
	0x5D	BL_HSP_01	[7:0]	0x46	0x46	BL_HSP_01 : Start Point in Coaxial Protocol Active Line BL_HSP_01 is lower 8bit
	0x5E	BL_HSP_02	[4:0]	0x00	0x00	BL_HSP_02 : Start Point in Coaxial Protocol Active Line BL_HSP_02 is upper 8bit
	0x5F	PELCO_SHOT	[0]	0x00	0x00	PELCO_SHOT : PELCO Protocol One Operation Enable signal

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x60	TX_DATA_01	[7:0]	0xAA	0xAA	TX_DATA_01 ~ TX_DATA_04 : 1 st field Data in Samsung Protocol
	0x61	TX_DATA_02	[7:0]	0x1C	0x1C	
	0x62	TX_DATA_03	[7:0]	0x18	0x18	
	0x63	TX_DATA_04	[7:0]	0xFF	0xFF	
	0x64	TX_DATA_05	[7:0]	0xAA	0xAA	TX_DATA_05 ~ TX_DATA_08 : 2 nd field Data in Samsung Protocol
	0x65	TX_DATA_06	[7:0]	0x3C	0x3C	
	0x66	TX_DATA_07	[7:0]	0xFF	0xFF	
	0x67	TX_DATA_08	[7:0]	0xFF	0xFF	
	0x68	TX_DATA_09	[7:0]	0xAA	0xAA	TX_DATA_09 ~ TX_DATA_12 : 3 rd field Data in Samsung Protocol
	0x69	TX_DATA_10	[7:0]	0x1B	0x1B	
	0x6A	TX_DATA_11	[7:0]	0x00	0x00	
	0x6B	TX_DATA_12	[7:0]	0x00	0x00	
	0x6C	TX_DATA_13	[7:0]	0xAA	0xAA	TX_DATA_13 ~ TX_DATA_16 : 4 th field Data in Samsung Protocol
	0x6D	TX_DATA_14	[7:0]	0x3B	0x3B	
	0x6E	TX_DATA_15	[7:0]	0x00	0x00	
	0x6F	TX_DATA_16	[7:0]	0x00	0x00	

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x90	CLEAN	[0]	0x00	0x00	CLEAN : RX Register is Read Only. So it need clean Condition First, this register set ON. Second, Read I2C Protocol 0x90. And then Clean the Samsung RX Registers.

❖ Registers to Control MPP

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xBC	MPP_SEL1	[3:0]	0x00	0x00	MPP_SELx : Select MPPx pin output signals selection (x = MPP Pin number) When MPPx_MSB(BANK1,0x4D) = 0, 0 : 0 (Zero) 1 : NOVIDEO status of ch.x 2 : Horizontal blank of ch.x 3 : Vertical blank of ch.x 4 : Field of ch.x 5 : Mute status of ch.x 6 : Motion status of ch.x 7 : interrupt request by the No video detection 8 : interrupt request by the Mute detection 9 : interrupt request by the Motion detection A : interrupt request by the Black detection B : interrupt request by the White detection D : Coaxial Protocol Command of ch x E : Coaxial Protocol Command of ch total
		MPP_SEL2	[7:4]			
	0xBD	MPP_SEL3	[3:0]			
		MPP_SEL4	[7:4]			

❖ Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xD9	MOTION_01	[0]	Read	Read	MOTION_0x : Each Channel Motion detection Status (x = Channel number) 0 : No MOTION 1 : On MOTION
		MOTION_02	[1]			
		MOTION_03	[2]			
		MOTION_04	[3]			
		MOTION_05	[4]			
		MOTION_06	[5]			
		MOTION_07	[6]			
		MOTION_08	[7]			
	0xDA	BLACK_01	[0]	Read	Read	BLACK_0x : Each Channel BLACK detection Status (x = Channel number) 0 : No BLACK 1 : On BLACK
		BLACK_02	[1]			
		BLACK_03	[2]			
		BLACK_04	[3]			
		BLACK_05	[4]			
		BLACK_06	[5]			
		BLACK_07	[6]			
		BLACK_08	[7]			
	0xDB	WHITE_01	[0]	Read	Read	WHITE_0x : Each Channel WHITE detection Status (x = Channel number) 0 : No WHITE 1 : On WHITE
		WHITE_02	[1]			
		WHITE_03	[2]			
		WHITE_04	[3]			
		WHITE_05	[4]			
		WHITE_06	[5]			
		WHITE_07	[6]			
		WHITE_08	[7]			
	0xDC	MUTE_01	[0]	Read	Read	MUTE_0x : Each Internal 8 Channel MUTE detection Status (x = Channel number) 0 : On Audio 1 : No Audio (MUTE)
		MUTE_02	[1]			
		MUTE_03	[2]			
		MUTE_04	[3]			
		MUTE_05	[4]			
		MUTE_06	[5]			
		MUTE_07	[6]			
		MUTE_08	[7]			
0xDD	MUTE_09	[0]	Read	Read	MUTE_0x : Each External 8 Channel MUTE detection Status (x-1 = EXT Channel number) 0 : On Audio 1 : No Audio (MUTE)	
	MUTE_10	[1]				
	MUTE_11	[2]				
	MUTE_12	[3]				
	MUTE_13	[4]				
	MUTE_14	[5]				
	MUTE_15	[6]				
	MUTE_16	[7]				
0xDE	MUTEMIC_01	[0]	Read	Read	MUTEMIC_0x : Each Internal and External Mic Channel MUTE detection Status (x = Channel number) 0 : On Audio 1 : No Audio (MUTE)	
	MUTEMIC_02	[2]				

❖ Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0xE0	NOVID_01B	[0]	Read	Read	NOVID_0xB : Each Channel Video Decoder No Video detection Status with HOLD option (x = Channel number) 0 : On Video 1 : No Video
		NOVID_02B	[1]			
		NOVID_03B	[2]			
		NOVID_04B	[3]			
		NOVID_05B	[4]			
		NOVID_06B	[5]			
		NOVID_07B	[6]			
		NOVID_08B	[7]			
	0xE1	MOTION_01B	[0]	Read	Read	MOTION_0xB : Each Channel Motion detection Status with HOLD option (x = Channel number) 0 : No MOTION 1 : On MOTION
		MOTION_02B	[1]			
		MOTION_03B	[2]			
		MOTION_04B	[3]			
		MOTION_05B	[4]			
		MOTION_06B	[5]			
		MOTION_07B	[6]			
		MOTION_08B	[7]			
	0xE2	BLACK_01B	[0]	Read	Read	BLACK_0xB : Each Channel BLACK detection Status with HOLD option (x = Channel number) 0 : No BLACK 1 : On BLACK
		BLACK_02B	[1]			
		BLACK_03B	[2]			
		BLACK_04B	[3]			
		BLACK_05B	[4]			
		BLACK_06B	[5]			
		BLACK_07B	[6]			
		BLACK_08B	[7]			
	0xE3	WHITE_01B	[0]	Read	Read	WHITE_0xB : Each Channel WHITE detection Status with HOLD option (x = Channel number) 0 : No WHITE 1 : On WHITE
		WHITE_02B	[1]			
		WHITE_03B	[2]			
		WHITE_04B	[3]			
		WHITE_05B	[4]			
		WHITE_06B	[5]			
		WHITE_07B	[6]			
		WHITE_08B	[7]			
0xE4	MUTE_01B	[0]	Read	Read	MUTE_0xB : Each Internal 8 Channel MUTE detection Status with HOLD option (x = Channel number) 0 : On Audio 1 : No Audio (MUTE)	
	MUTE_02B	[1]				
	MUTE_03B	[2]				
	MUTE_04B	[3]				
	MUTE_05B	[4]				
	MUTE_06B	[5]				
	MUTE_07B	[6]				
	MUTE_08B	[7]				

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
1	0x00	MOTION_OFF_1	[4]	0x03	0x03	MOTION_OFF_x : Motion Detection On/Off Selection (x = channel number) 0 : Motion detection on 1 : Motion detection off
	0x02	MOTION_OFF_2				
	0x04	MOTION_OFF_3				
	0x06	MOTION_OFF_4				
	0x08	MOTION_OFF_5				
	0x0A	MOTION_OFF_6				
	0x0C	MOTION_OFF_7				
	0x0E	MOTION_OFF_8				
	0x00	MOTION_PIC_1	[1:0]	0x03	0x03	MOTION_PIC_x : Indicates the type of processing made on the area where motion is generated. (x = channel number) 0 : No processing made on the area where motion is generated. 1 : EVEN_FLD (Luma – 32) 2 : EVEN_FLD (Luma – 48) 3 : ALL_FLD (Luma – 48)
	0x02	MOTION_PIC_2				
	0x04	MOTION_PIC_3				
	0x06	MOTION_PIC_4				
	0x08	MOTION_PIC_5				
	0x0A	MOTION_PIC_6				
	0x0C	MOTION_PIC_7				
	0x0E	MOTION_PIC_8				
	0x01	MOD_TSEN_1	[7:0]	0x60	0x60	MOD_TSEN_x : Motion Temporal Sensitivity. (x = channel number) The value (the sum of the motion block) bases on which it is determined whether motion is generated or not (0 -> 255 The greater the number, the less sensitive it gets)
	0x03	MOD_TSEN_2				
	0x05	MOD_TSEN_3				
	0x07	MOD_TSEN_4				
	0x09	MOD_TSEN_5				
	0x0B	MOD_TSEN_6				
	0x0D	MOD_TSEN_7				
	0x0F	MOD_TSEN_8				
	0x10	MOD_PSEN_1	[1:0]	0x00	0x00	MOD_PSEN_x : Motion Pixed Sensitivity. Register that determines how much data input in the Motion block is used to search for motion (x = channel number) 0 : bypass 1 : 1/2 2 : 1/4 3 : 1/8
		MOD_PSEN_2	[3:2]			
		MOD_PSEN_3	[5:4]			
		MOD_PSEN_4	[7:6]			
0x11	MOD_PSEN_5	[7:6]	0x00	0x00		
	MOD_PSEN_6	[5:4]				
	MOD_PSEN_7	[3:2]				
	MOD_PSEN_8	[1:0]				
0x12	MD_960H_01	[0]	0xFF	0xFF	MD_960H_0x : Motion Detection 720H/960H Selection (x = channel number) 0 : Motion Detection 720H Operation 1 : Motion Detection 960H Operation	
	MD_960H_02	[1]				
	MD_960H_03	[2]				
	MD_960H_04	[3]				
	MD_960H_05	[4]				
	MD_960H_06	[5]				
	MD_960H_07	[6]				
	MD_960H_08	[7]				

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x20	CHx_MOD_01	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number)</p> <p>0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
	0x38	CHx_MOD_02	[6]			
	0x50	CHx_MOD_03	[5]			
	0x68	CHx_MOD_04	[4]			
	0x80	CHx_MOD_05	[3]			
	0x98	CHx_MOD_06	[2]			
	0xB0	CHx_MOD_07	[1]			
	0xC8	CHx_MOD_08	[0]			
	0x21	CHx_MOD_09	[7]	0xFF	0xFF	
	0x39	CHx_MOD_10	[6]			
	0x51	CHx_MOD_11	[5]			
	0x69	CHx_MOD_12	[4]			
	0x81	CHx_MOD_13	[3]			
	0x99	CHx_MOD_14	[2]			
	0xB1	CHx_MOD_15	[1]			
	0xC9	CHx_MOD_16	[0]			
	0x22	CHx_MOD_17	[7]	0xFF	0xFF	
	0x3A	CHx_MOD_18	[6]			
	0x52	CHx_MOD_19	[5]			
	0x6A	CHx_MOD_20	[4]			
	0x82	CHx_MOD_21	[3]			
	0x9A	CHx_MOD_22	[2]			
	0xB2	CHx_MOD_23	[1]			
	0xCA	CHx_MOD_24	[0]			
	0x23	CHx_MOD_25	[7]	0xFF	0xFF	
	0x3B	CHx_MOD_26	[6]			
	0x53	CHx_MOD_27	[5]			
	0x6B	CHx_MOD_28	[4]			
	0x83	CHx_MOD_29	[3]			
	0x9B	CHx_MOD_30	[2]			
	0xB3	CHx_MOD_31	[1]			
	0xCB	CHx_MOD_32	[0]			
	0x24	CHx_MOD_33	[7]	0xFF	0xFF	
	0x3C	CHx_MOD_34	[6]			
	0x54	CHx_MOD_35	[5]			
	0x6C	CHx_MOD_36	[4]			
	0x84	CHx_MOD_37	[3]			
	0x9C	CHx_MOD_38	[2]			
	0xB4	CHx_MOD_39	[1]			
	0xCC	CHx_MOD_40	[0]			
	0x25	CHx_MOD_41	[7]	0xFF	0xFF	
	0x3D	CHx_MOD_42	[6]			
	0x55	CHx_MOD_43	[5]			
	0x6D	CHx_MOD_44	[4]			
	0x85	CHx_MOD_45	[3]			
	0x9D	CHx_MOD_46	[2]			
	0xB5	CHx_MOD_47	[1]			
	0xCD	CHx_MOD_48	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x26	CHx_MOD_49	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) 0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
	0x3E	CHx_MOD_50	[6]			
	0x56	CHx_MOD_51	[5]			
	0x6E	CHx_MOD_52	[4]			
	0x86	CHx_MOD_53	[3]			
	0x9E	CHx_MOD_54	[2]			
	0xB6	CHx_MOD_55	[1]			
	0xCE	CHx_MOD_56	[0]			
	0x27	CHx_MOD_57	[7]	0xFF	0xFF	
	0x3F	CHx_MOD_58	[6]			
	0x57	CHx_MOD_59	[5]			
	0x6F	CHx_MOD_60	[4]			
	0x87	CHx_MOD_61	[3]			
	0x9F	CHx_MOD_62	[2]			
	0xB7	CHx_MOD_63	[1]			
	0xCF	CHx_MOD_64	[0]			
	0x28	CHx_MOD_65	[7]	0xFF	0xFF	
	0x40	CHx_MOD_66	[6]			
	0x58	CHx_MOD_67	[5]			
	0x70	CHx_MOD_68	[4]			
	0x88	CHx_MOD_69	[3]			
	0xA0	CHx_MOD_70	[2]			
	0xB8	CHx_MOD_71	[1]			
	0xD0	CHx_MOD_72	[0]			
	0x29	CHx_MOD_73	[7]	0xFF	0xFF	
	0x41	CHx_MOD_74	[6]			
	0x59	CHx_MOD_75	[5]			
	0x71	CHx_MOD_76	[4]			
	0x89	CHx_MOD_77	[3]			
	0xA1	CHx_MOD_78	[2]			
	0xB9	CHx_MOD_79	[1]			
	0xD1	CHx_MOD_80	[0]			
	0x2A	CHx_MOD_81	[7]	0xFF	0xFF	
	0x42	CHx_MOD_82	[6]			
	0x5A	CHx_MOD_83	[5]			
	0x72	CHx_MOD_84	[4]			
	0x8A	CHx_MOD_85	[3]			
	0xA2	CHx_MOD_86	[2]			
	0xBA	CHx_MOD_87	[1]			
	0xD2	CHx_MOD_88	[0]			
	0x2B	CHx_MOD_89	[7]	0xFF	0xFF	
	0x43	CHx_MOD_90	[6]			
	0x5B	CHx_MOD_91	[5]			
	0x73	CHx_MOD_92	[4]			
	0x8B	CHx_MOD_93	[3]			
	0xA3	CHx_MOD_94	[2]			
	0xBB	CHx_MOD_95	[1]			
	0xD3	CHx_MOD_96	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x2C	CHx_MOD_97	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) 0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
	0x44	CHx_MOD_98	[6]			
	0x5C	CHx_MOD_99	[5]			
	0x74	CHx_MOD_100	[4]			
	0x8C	CHx_MOD_101	[3]			
	0xA4	CHx_MOD_102	[2]			
	0xBC	CHx_MOD_103	[1]			
	0xD4	CHx_MOD_104	[0]			
	0x2D	CHx_MOD_105	[7]	0xFF	0xFF	
	0x45	CHx_MOD_106	[6]			
	0x5D	CHx_MOD_107	[5]			
	0x75	CHx_MOD_108	[4]			
	0x8D	CHx_MOD_109	[3]			
	0xA5	CHx_MOD_110	[2]			
	0xBD	CHx_MOD_111	[1]			
	0xD5	CHx_MOD_112	[0]			
	0x2E	CHx_MOD_113	[7]	0xFF	0xFF	
	0x46	CHx_MOD_114	[6]			
	0x5E	CHx_MOD_115	[5]			
	0x76	CHx_MOD_116	[4]			
	0x8E	CHx_MOD_117	[3]			
	0xA6	CHx_MOD_118	[2]			
	0xBE	CHx_MOD_119	[1]			
	0xD6	CHx_MOD_120	[0]			
	0x2F	CHx_MOD_121	[7]	0xFF	0xFF	
	0x47	CHx_MOD_122	[6]			
	0x5F	CHx_MOD_123	[5]			
	0x77	CHx_MOD_124	[4]			
	0x8F	CHx_MOD_125	[3]			
	0xA7	CHx_MOD_126	[2]			
	0xBF	CHx_MOD_127	[1]			
	0xD7	CHx_MOD_128	[0]			
	0x30	CHx_MOD_129	[7]	0xFF	0xFF	
	0x48	CHx_MOD_130	[6]			
	0x60	CHx_MOD_131	[5]			
	0x78	CHx_MOD_132	[4]			
	0x90	CHx_MOD_133	[3]			
	0xA8	CHx_MOD_134	[2]			
	0xC0	CHx_MOD_135	[1]			
	0xD8	CHx_MOD_136	[0]			
	0x31	CHx_MOD_137	[7]	0xFF	0xFF	
	0x49	CHx_MOD_138	[6]			
	0x61	CHx_MOD_139	[5]			
	0x79	CHx_MOD_140	[4]			
	0x91	CHx_MOD_141	[3]			
	0xA9	CHx_MOD_142	[2]			
	0xC1	CHx_MOD_143	[1]			
	0xD9	CHx_MOD_144	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			NTSC	PAL	
2	0x32	CHx_MOD_145	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number) 0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
	0x4A	CHx_MOD_146	[6]			
	0x62	CHx_MOD_147	[5]			
	0x7A	CHx_MOD_148	[4]			
	0x92	CHx_MOD_149	[3]			
	0xAA	CHx_MOD_150	[2]			
	0xC2	CHx_MOD_151	[1]			
	0xDA	CHx_MOD_152	[0]			
	0x33	CHx_MOD_153	[7]			
	0x4B	CHx_MOD_154	[6]			
	0x63	CHx_MOD_155	[5]			
	0x7B	CHx_MOD_156	[4]			
	0x93	CHx_MOD_157	[3]			
	0xAB	CHx_MOD_158	[2]			
	0xC3	CHx_MOD_159	[1]			
	0xDB	CHx_MOD_160	[0]			
	0x34	CHx_MOD_161	[7]	0xFF	0xFF	
	0x4C	CHx_MOD_162	[6]			
	0x64	CHx_MOD_163	[5]			
0x7C	CHx_MOD_164	[4]				
0x94	CHx_MOD_165	[3]				
0xAC	CHx_MOD_166	[2]				
0xC4	CHx_MOD_167	[1]				
0xDC	CHx_MOD_168	[0]				
0x35	CHx_MOD_169	[7]	0xFF			0xFF
0x4D	CHx_MOD_170	[6]				
0x65	CHx_MOD_171	[5]				
0x7D	CHx_MOD_172	[4]				
0x95	CHx_MOD_173	[3]				
0xAD	CHx_MOD_174	[2]				
0xC5	CHx_MOD_175	[1]				
0xDD	CHx_MOD_176	[0]				
0x36	CHx_MOD_177	[7]		0xFF	0xFF	
0x4E	CHx_MOD_178	[6]				
0x66	CHx_MOD_179	[5]				
0x7E	CHx_MOD_180	[4]				
0x96	CHx_MOD_181	[3]				
0xAE	CHx_MOD_182	[2]				
0xC6	CHx_MOD_183	[1]				
0xDE	CHx_MOD_184	[0]				
0x37	CHx_MOD_185	[7]	0xFF			0xFF
0x4F	CHx_MOD_186	[6]				
0x67	CHx_MOD_187	[5]				
0x7F	CHx_MOD_188	[4]				
0x97	CHx_MOD_189	[3]				
0xAF	CHx_MOD_190	[2]				
0xC7	CHx_MOD_191	[1]				
0xDF	CHx_MOD_192	[0]				

7. Electrical characteristics

7.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V _{VDD1DM}	0.5	-	1.32	V
3.3V Digital Power Supply Voltage	V _{VDD3DM}	0.5	-	3.6	V
3.3V Analog Power Supply Voltage	V _{VDD3AM}	0.5	-	3.6	V
Voltage for Digital pins	V _{DIO}	0.5	-	4.6	V
Voltage for Analog Inputs	V _{AIO}	0.5	-	1.95	V
Storage Temperature	T _S	-40	-	125	°C
Junction Temperature	T _J	-40	-	125	°C
Vapor phase soldering (15 Sec)	T _{VSOL}	-	-	220	°C

Note : This Device should be operated under recommended operating condition. Since, absolute maximum rating condition can either cause device reliability problem or damage the device sufficiently to cause immediate failure.

7.2. Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V _{VDD1D}	1.08	1.2	1.32	V
3.3V Digital Power Supply Voltage	V _{VDD3D}	3.0	3.3	3.6	V
3.3V Analog Power Supply Voltage	V _{VDD3A}	3.0	3.3	3.6	V
Ambient operating temperature	V _A	0	-	70	°C

7.3. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V _{IL}	-0.3	-	0.8	V
Input High Voltage	V _{IH}	2	-	V _{DD3D} +0.3	V
Input Leakage Current	I _L	-	-	±1	µA
Input Capacitance (f = 1MHz, V _{IN} = 2.4V)	C _{IN}	-	-	10	pF
Output Low Voltage (I _{OL} = 8.0mA)	V _{OL}	-	-	0.4	V
Output High Voltage (I _{OH} = 12mA)	V _{OH}	2.4	-	-	V
Tri-State Output Leakage Current	I _{OZ}	-	-	±1	µA
Output Capacitance	C _{OUT}	-	-	10	pF

7.4. AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
(Power Supply Current)					
1.2V Digital Power Supply Current	I _{VDD1D}	-	TBD	-	mA
3.3V Digital Power Supply Current	I _{VDD3D}	-	TBD	-	mA
3.3V Analog Power Supply Current	I _{VDD3A}	-	TBD	-	mA
(Clock Pin)					
XTALI frequency	f _{XTALI}	-	27.0	-	MHz
XTALI duty cycle	f _{DUTY}	45	-	55	%
XTALI pulse width low	t _{PWL_XTALI}	17.0	-	-	nsec
XTALI pulse width high	t _{PWH_XTAL}	17.0	-	-	nsec
(Reset Pin)					
RSTB setup time	t _{SU}	1			us
RSTB pulse width low	t _{PWL_rstb}	1			us
RSTB release time (low to high)	t _{REL_rstb}	10			us
(Host Interface Pins)					
SCL frequency	f _{SCL}	-	-	6	XTALI
SCL minimum pulse width low	t _{PWL_SCL}	6	-	-	XTALI
SCL minimum pulse width high	t _{PWH_SCL}	4	-	-	XTALI
SCL to SDA setup time	t _{IS_SDA}	2	-	-	XTALI
SCL to SDA hold time	t _{IH_SDA}	2	-	-	XTALI
SCL to SDA delay time	t _{OD_SDA}	-	-	6	XTALI
SCL to SDA hold time	t _{OH_SDA}	3	-	-	XTALI

8. Recommended Register Value

: For register values, always make sure to check and use updated values of recommendation.

8.1. NTSC Recommended Register Setting

8.1.1 NTSC Register Bank0 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK0	0x00	0x00	0x00	0x20	0x00	0x00	0x00	0xAF	0x00	0xA0	0xA0	0xA0	0xA0	0xFE	0xFE	0xFE
	0x10	0x88	0x88	0x88	0x88	0x80	0x80	0x80	0x80	0x88	0x88	0x11	0x11	0xA4	0xA4	0xA4
	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x30	0x13	0x13	0x13	0x13	0x2F	0x82	0x0B	0x43	0x0A	0x0A	0x0A	0x0A	0x80	0x80	0x80
	0x40	0x01	0x01	0x01	0x01	0x30	0x30	0x30	0x30	0x30	0x30	0x30	0x30	0x00	0x00	0x00
	0x50	0x00	0x00	0x00	0x00	0xF1	0x10	0x32	0x00	0x44	0x44	0x44	0x44	0x1E	0x1E	0x1E
	0x60	0x00	0x00	0x00	0x00	0x08	0x08	0x08	0x08	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	0x00	0x00	0x00
	0x80	0x00	0x00	0x20	0x00	0x00	0x00	0xAF	0x00	0xA0	0xA0	0xA0	0xA0	0xFE	0xFE	0xFE
	0x90	0x88	0x88	0x88	0x88	0x80	0x80	0x80	0x80	0x88	0x88	0x11	0x11	0xA4	0xA4	0xA4
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x13	0x13	0x13	0x13	0x2F	0x82	0x0B	0x43	0x0A	0x0A	0x0A	0x0A	0x80	0x80	0x80
	0xC0	0x01	0x01	0x01	0x01	0x30	0x30	0x30	0x30	0x30	0x30	0x30	0x30	0x00	0x00	0x00
	0xD0	0x00	0x00	0x00	0x00	0xF1	0x54	0x76	0x00	0x44	0x44	0x44	0x44	0x1E	0x1E	0x1E
	0xE0	0x00	0x00	0x00	0x00	0x08	0x08	0x08	0x08	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	0x00	0x00	0x00

8.1.2 NTSC Register Bank1 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK1	0x00	0x02	0x08	0x08	0x08	0x08	0x08	0x1B	0xC8	0x03	0x00	0x10	0x32	0x54	0x76	
	0x10	0xBA	0xDC	0xFE	0x08	0x00	0x00	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88	
	0x20	0x88	0x88	0x08	0x19	0x18	0x16	0x00	0x00	0x00	0x88	0xFF	0x40	0xAA	0xAA	
	0x30	0x0A	0x82	0x00	0x00	0x00	0x00	0x00	0x00	0x08	0x01	0x81	0x10	0x00	0x00	
	0x40	0x08	0x08	0x08	0x08	0x14	0x01	0x00	0x40	0x60	0x00	0x03	0x10	0x00	0x00	
	0x50	0x37	0x37	0x1B	0x05	0x00	0x07	0x00	0x09	0x00	0x00	0x06	0x00	0x46	0x00	
	0x60	0xAA	0x1C	0x18	0xFF	0xAA	0x3C	0xFF	0xFF	0xAA	0x1B	0x00	0x00	0xAA	0x3B	
	0x70	0x00	0x00	0x00	0x00	Read	Read	Read	Read	Read	Read	Read	Read	0x00	0x00	
	0x80	0x00	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	
	0x90	0x00	-	-	-	0x00	-	-	-	-	-	-	-	-	-	
	0xA0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	0xB0	-	-	-	-	0x40	0x30	0x40	0x30	-	-	-	0x00	0x00	-	
	0xC0	0x10	0x32	0x54	0x76	-	-	-	-	0x88	-	0x03	0x00	0x70	0x70	
	0xD0	0x00	0x00	-	0x00	0x00	0x01	0x00	-	Read	Read	Read	Read	Read	Read	
	0xE0	Read	Read	Read	Read	Read	Read	Read	-	0x90	0x00	-	-	Read	Read	
	0xF0	Read	Read	Read	Read	0x82	Read	Read	Read	0x00	-	-	-	-	-	

8.1.3 NTSC Register Bank2 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK2	0x00	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	
	0x10	0x00	0x00	0xFF	0x00	0xC0	0x00	0x00	0x00	-	-	-	-	-	-	
	0x20	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x30	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x40	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x50	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x60	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x70	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x80	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x90	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xA0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xB0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xC0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xD0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	

8.1.4 NTSC Register Bank3 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
BANK3	0x00	0xE0	0x09	0x0C	0x1F	0x00	0x20	0x60	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x03
	0x10	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x20	0x50	0x0C	0xFF	0x88
	0x20	0x84	0x24	0x23	0x00	0x2A	0xDC	0xF0	0x57	0x90	0x1F	0x52	0x78	0x00	0x68	0x00	0x07
	0x30	0xE0	0x43	0xA2	0x00	0x00	0x15	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
	0x40	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x20	0x10	0x00	0x00
	0x50	0x00	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x60	0x53	0x53	0x21	0x00	0x22	0x22	0x22	0x22	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	0xC0	0x01	0x06	0x06	0x11	0x00	0xFF	0x80	0x00	0xFF	0xFF	0x80	0x00	0xFF	0x00	0x00
	0x80	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08
	0x90	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xC0	0x10	0x70	0x0C	0x50	0x10	0x34	0x70	0x50	0x20	0x20	0x30	0x40	0x60	0x20	0x20	0x20
	0xD0	0x40	0x50	0x0E	0x00	0x00	0x00	0x00	0x00	0xB9	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
	0xE0	0x21	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x86	0x04	0x05	0x93	0x22	0x5C	Bank

8.1.5 NTSC Register Bank4 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
BANK4	0x00	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
	0x10	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x20	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
	0x30	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x40	0x64	0xFF	0x06	0x06	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x50	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x60	0x44	0x44	0x44	0x44	0x55	0x55	0x55	0x55	0x44	0x44	0x44	0x44	0x33	0x33	0x33	0x33
	0x70	0xFF	0x55	0x55	0x55	0x55	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x80	0xFF	0x55	0x55	0x55	0x55	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x90	0x02	0x80	0x80	0x08	0x08	0x78	0x2A	0x80	0x80	0x80	0x14	0x01	0x00	0x01	0x80	0x00
	0xA0	0x00	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xC0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xD0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Bank

8.2. PAL Recommended Register Setting

8.2.1 PAL Register Bank0 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK0	0x00	0x00	0x00	0x20	0x00	0x00	0x00	0xAF	0x00	0xDD	0xDD	0xDD	0xDD	0xF8	0xF8	0xF8
	0x10	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x88	0x88	0x11	0x11	0xA2	0xA2	0xA2
	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x30	0x13	0x13	0x13	0x13	0x2F	0x02	0x0B	0x43	0x0A	0x0A	0x0A	0x0A	0x80	0x80	0x80
	0x40	0x00	0x00	0x00	0x00	0x30	0x30	0x30	0x30	0x00	0x00	0x00	0x00	0x04	0x04	0x04
	0x50	0x04	0x04	0x04	0x04	0x01	0x10	0x32	0x00	0x45	0x45	0x45	0x45	0x1E	0x1E	0x1E
	0x60	0x00	0x00	0x00	0x00	0x0D	0x0D	0x0D	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	0x00	0x00	0x00
	0x80	0x00	0x00	0x20	0x00	0x00	0x00	0xAF	0x00	0xDD	0xDD	0xDD	0xDD	0xF8	0xF8	0xF8
	0x90	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x88	0x88	0x11	0x11	0xA2	0xA2	0xA2
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x13	0x13	0x13	0x13	0x2F	0x02	0x0B	0x43	0x0A	0x0A	0x0A	0x0A	0x80	0x80	0x80
	0xC0	0x00	0x00	0x00	0x00	0x30	0x30	0x30	0x30	0x00	0x00	0x00	0x00	0x04	0x04	0x04
	0xD0	0x04	0x04	0x04	0x04	0x01	0x54	0x76	0x00	0x45	0x45	0x45	0x45	0x1E	0x1E	0x1E
	0xE0	0x00	0x00	0x00	0x00	0x0D	0x0D	0x0D	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x88	0x88	0x11	0x11	0x00	0x00	0x00

8.2.2 PAL Register Bank1 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK1	0x00	0x02	0x08	0x08	0x08	0x08	0x08	0x1B	0xC8	0x03	0x00	0x10	0x32	0x54	0x76	0x98
	0x10	0xBA	0xDC	0xFE	0x08	0x00	0x00	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88	0x88
	0x20	0x88	0x88	0x08	0x19	0x18	0x16	0x00	0x00	0x88	0xFF	0x40	0xAA	0xAA	0xAA	0xAA
	0x30	0x0A	0x82	0x00	0x00	0x00	0x8C	0xA0	0x00	0x08	0x01	0x81	0x10	0x00	0x00	0x00
	0x40	0x08	0x08	0x08	0x08	0x14	0x01	0x00	0x40	0x60	0x00	0x03	0x10	0x00	0x00	0x00
	0x50	0x37	0x37	0x1B	0x05	0x00	0x07	0x00	0x09	0x00	0x00	0x08	0x06	0x00	0x46	0x00
	0x60	0xAA	0x1C	0x18	0xFF	0xAA	0x3C	0xFF	0xFF	0xAA	0x1B	0x00	0x00	0xAA	0x3B	0x00
	0x70	0x00	0x00	0x00	0x00	Read	Read	Read	Read	Read	Read	Read	Read	0x00	0x00	0x80
	0x80	0x00	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x00	0x00
	0x90	0x00	-	-	-	0x00	-	-	-	-	-	-	-	-	-	-
	0xA0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	0xB0	-	-	-	-	0x40	0x30	0x40	0x30	-	-	-	-	0x00	0x00	-
	0xC0	0x10	0x32	0x54	0x76	-	-	-	-	0x88	-	0x03	0x00	0x70	0x70	-
	0xD0	0x00	0x00	-	0x00	0x00	0x01	0x00	-	Read	Read	Read	Read	Read	Read	Read
	0xE0	Read	Read	Read	Read	Read	Read	Read	-	0x90	0x00	-	-	Read	Read	Read
	0xF0	Read	Read	Read	Read	0x82	Read	Read	Read	0x00	-	-	-	-	-	-

8.2.3 PAL Register Bank2 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK2	0x00	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	0x03	0x60	
	0x10	0x00	0x00	0xFF	0x00	0xC0	0x00	0x00	-	-	-	-	-	-	-	
	0x20	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x30	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x40	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x50	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x60	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x70	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x80	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0x90	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xA0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xB0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xC0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xD0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
	0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	

8.2.4 PAL Register Bank3 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
BANK3	0x00	0xE0	0x09	0x0C	0x1F	0x00	0x20	0x40	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x03
	0x10	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x20	0x50	0x0C	0x00	0x88
	0x20	0x80	0x24	0x23	0x00	0x2A	0xCC	0xF0	0x57	0x90	0x1F	0x52	0x78	0x00	0x68	0x00	0x07
	0x30	0xE0	0x43	0xA2	0x00	0x00	0x17	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
	0x40	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x20	0x10	0x00	0x00
	0x50	0x00	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x60	0x53	0x53	0x21	0x00	0x22	0x22	0x22	0x22	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	0xC0	0x01	0x06	0x06	0x11	0x00	0xFF	0x80	0x00	0xFF	0xFF	0x80	0x00	0xFF	0x00	0x00
	0x80	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08	0x00	0x08
	0x90	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xC0	0x10	0x10	0x0E	0x70	0x10	0x34	0x70	0x5C	0x40	0x20	0x30	0x40	0x50	0x08	0x28	0x20
	0xD0	0x40	0x50	0x0E	0x00	0x00	0x00	0x00	0x00	0xB9	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
	0xE0	0x21	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x86	0x04	0x05	0x93	0x22	0x5C	Bank

8.2.5 PAL Register Bank4 of 960H

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
BANK4	0x00	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
	0x10	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x20	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
	0x30	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x40	0x64	0xFF	0x06	0x06	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x50	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x60	0x33	0x33	0x33	0x33	0xAA	0xAA	0xAA	0x77	0x77	0x77	0x77	0x77	0x33	0x33	0x33	0x33
	0x70	0xFF	0x55	0x55	0x55	0x55	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x80	0x03	0x80	0x80	0x08	0x08	0x7E	0x00	0x80	0x80	0x80	0x14	0x13	0x00	0x03	0x80	0x00
	0x90	0x00	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xA0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xB0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xC0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xD0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xE0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xF0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Bank

8.3 Coaxial Protocol Recommended Register Setting

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK1	0x50	0x37	0x37	0x1B	0x05	0x00	0x07	0x00	0x09	0x00	0x00	0x08	0x06	0x00	0x46	0x00
	0x60	0xAA	0x1C	0x18	0xFF	0xAA	0x3C	0xFF	0xFF	0xAA	0x1B	0x00	0x00	0xAA	0x3B	0x00
	0x70	0x00	0x00	0x00	0x00	Read	Read	Read	Read	Read	Read	Read	0x00	0x00	0x80	0x01
	0x80	0x00	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x10	0x32	0x54

8.4 H960 and SH720 Recommended difference Register Setting

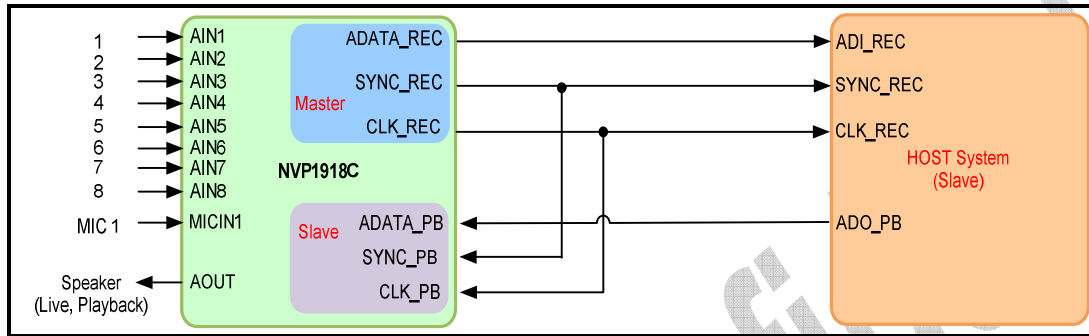
ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK0	0x10 / 0x90	H960							0x88	0x88						
		SH720							0x44	0x44						

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
BANK3	0x50	H960			0xFF											
		SH720			0x00											
	0x60	H960			0x00											
		SH720			0xFF											

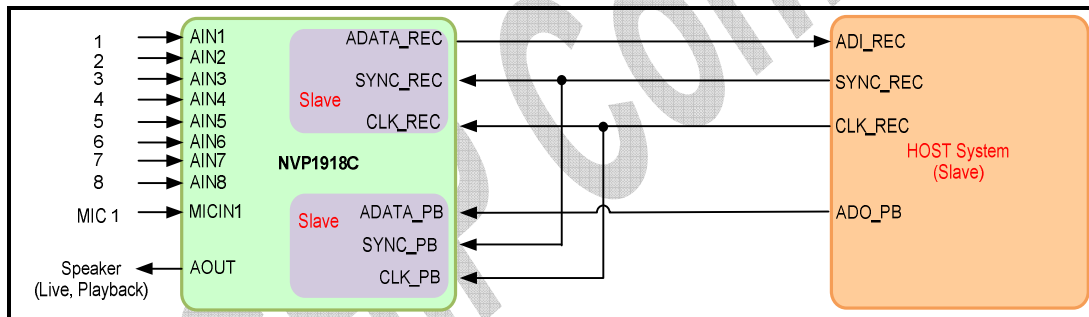
9. System Applications

9.1. 8-Channel, Master Mode

9.1.1. Block Diagram (8 Channel, Master Mode)

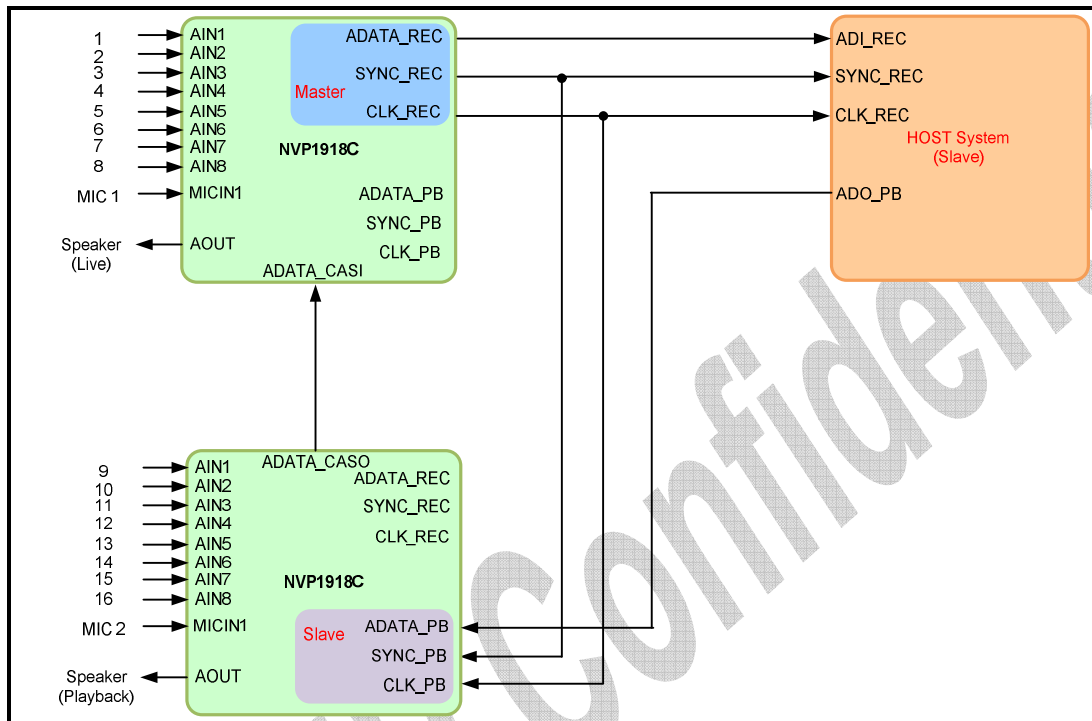


9.1.2. Block Diagram (8 Channel, Slave Mode)

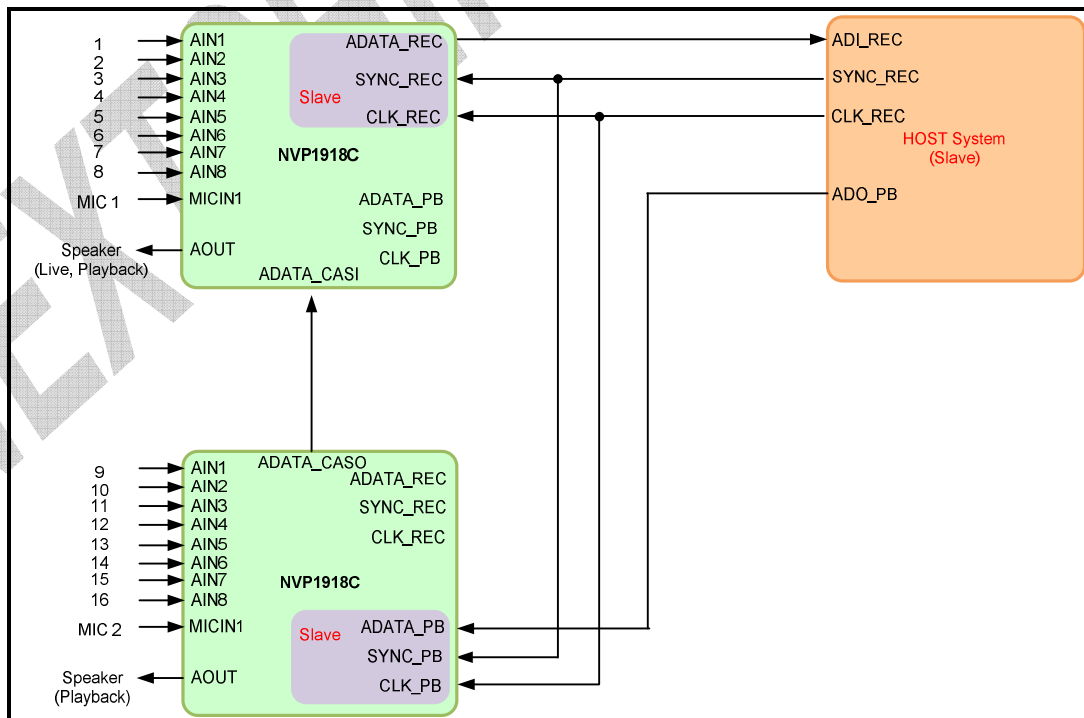


9.2. 16-Channel, Master Mode

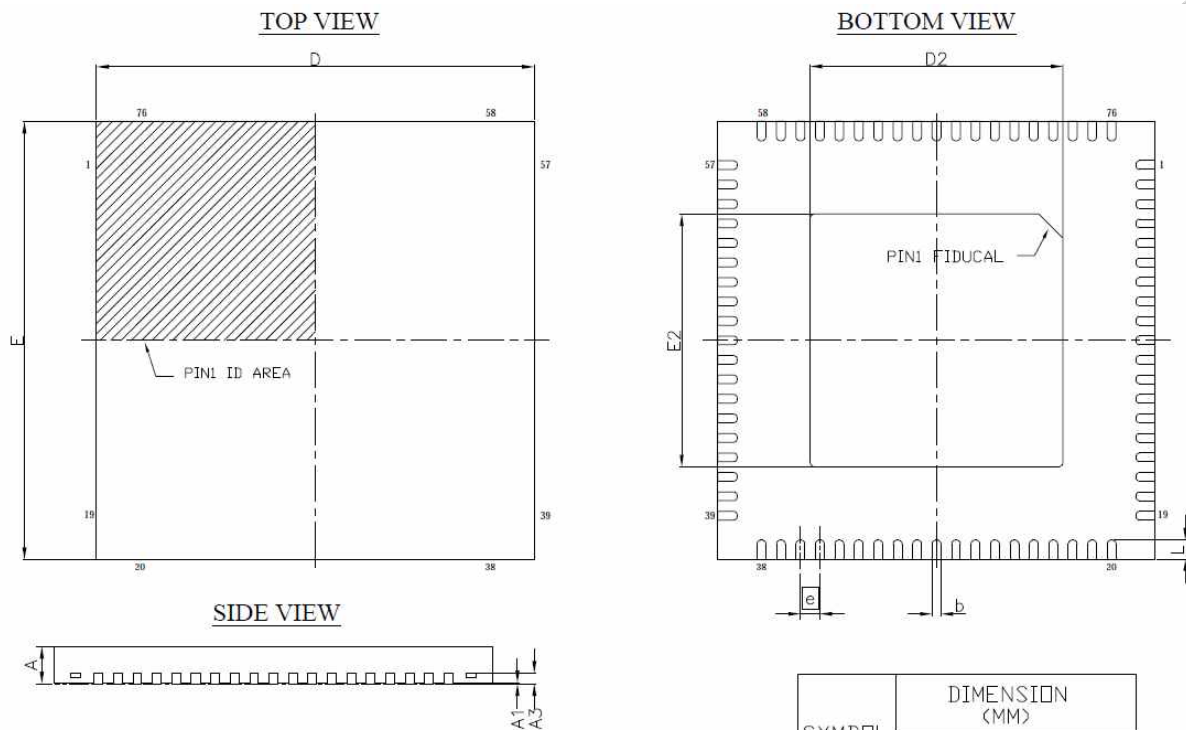
9.2.1. Block Diagram (16 Channel, Master Mode)



9.2.1. Block Diagram (16 Channel, Slave Mode)



10. Package Information



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	8.90	9.00	9.10
D2	5.10	5.20	5.30
E	8.90	9.00	9.10
E2	5.10	5.20	5.30
\triangle e	0.40 BSC		
L	0.30	0.40	0.50

11. Revision History

VERSION	DATE	DESCRIPTION	NOTE
Preliminary 0.0	2014-01-06	- Initial Draft	

12. Contact Information

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