PELICAN-S NVP2080 Datasheet

CCD Camera Image Signal Processor

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nextchip

Interlaced CCD Image Signal Processor

PELICAN-S is an image signal processor (ISP) device which outputs CVBS or S-Video data format after receiving color filter array (CFA) patterns from color-interlaced CCD sensor (760H), which is processed through an internal encoder and DAC. PELICAN-S internally includes AFE(It features a 25 MHz single-channel architecture designed to sample the outputs of CCD arrays. The signal chain consists of a digitally controlled variable gain amplifier(VGA), and a black level clamp. It offers 10-bit ADC resolution.) device that it is possible to design compact size of cameras. Even there are two main functions with AE and AWB functions. AE function indicates to stabilize output image brightness and AWB function which automatically adjust white balance even if the input images with different color temperature. It includes a menu function, OSD and ADC. Menu is controllable with ADC key which means camera is controllable without external MCU. PELICAN supports 485 and Coaxial cable communication which help cameras control remotely. Furthermore, PELICAN-S came out with 650TV line high resolution. Compare to past device, we provide better and high quality images. Besides many other functions, it also supports mirror function, lens shading correction, motion detection and DWDR which increases dynamic range with output image.

Features

ISP

-. Input: NTSC/PAL, 760H CCD format
-. Output: NTSC/PAL analog S-Video or CVBS
-. Programmable GAMMA processing(16 steps)
-. Supports horizontal resolution 650TV lines
-. De-moire
-. Video adjustment (brightness, contrast, saturation and hue)
-. Horizontal MIRROR
-. Blemish compensation → AUTO(73/247 points)
-. Color rolling / Breathing suppress.
-. DWDR(Digital Wide Dynamic Range)
-. Motion detection (motion block size : 48 x 15)
-. Lens shading
-. Parking Line
-. Enhanced IR SMART
-. High Light Compensation(HLC)
-. Back Light Compensation(BLC)
-. Privacy Mask
-. OSD : 9 language (ENG,CHN(Simplified, Traditional),SPN,RUS,JPN,POR,GER,FRA)
-. USER LOGO(120x58)
-. Communication : RS-485 (Pelco-D/P, NEXTCHIP)
-. Coaxial communication (Pelco-C, CCVC)
-. I2C Interface
-. On-chip Analog Front End (AFE)
-. On-chip optical detector (AE/AWB)

-. On-chip CCD timing generator
-. On-chip NTSC/PAL video encoder
-. On-chip 2CH DAC (S-video or CVBS and IRIS)
-. On-chip 1CH ADC (2CH MUX)
-. 5.0V / 3.3V operation (1.8V LDO include)

AFE

-. 25 MSPS correlated double sampler (CDS)
-. 6 dB to 40 dB 10-bit variable gain amplifier (VGA)
-. Low noise optical black clamp circuit
-. 10-bit 25 MSPS A/D converter

Ordering Information

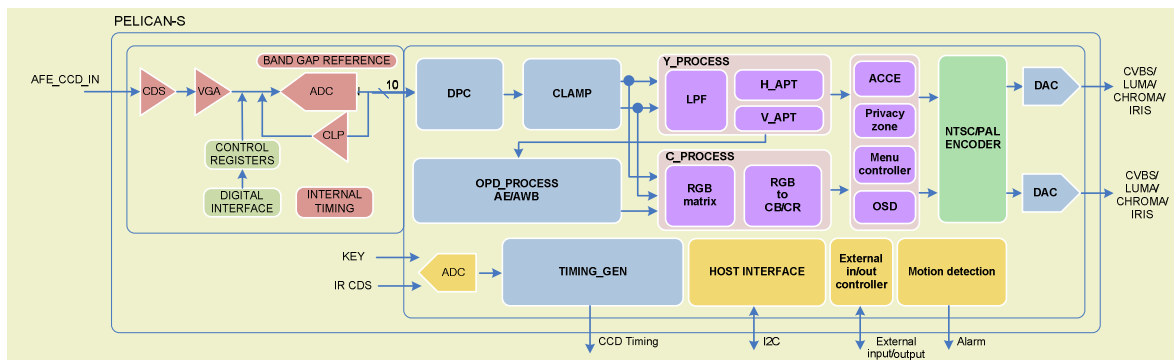| Device	Package	Temperature Range
PELICAN-S (NVP2080)	64-TQFP	-20℃ ~ 85℃

Applications

-. CCTV camera
-. Door phone camera
-. Video phone camera
-. Rear-view monitoring camera

Related Products

-. CCD   : NEPIS
-. V-Driver : NVD2014A (NEXTCHIP)

Block Diagram

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1. Pin information

1.1 Pin assignments
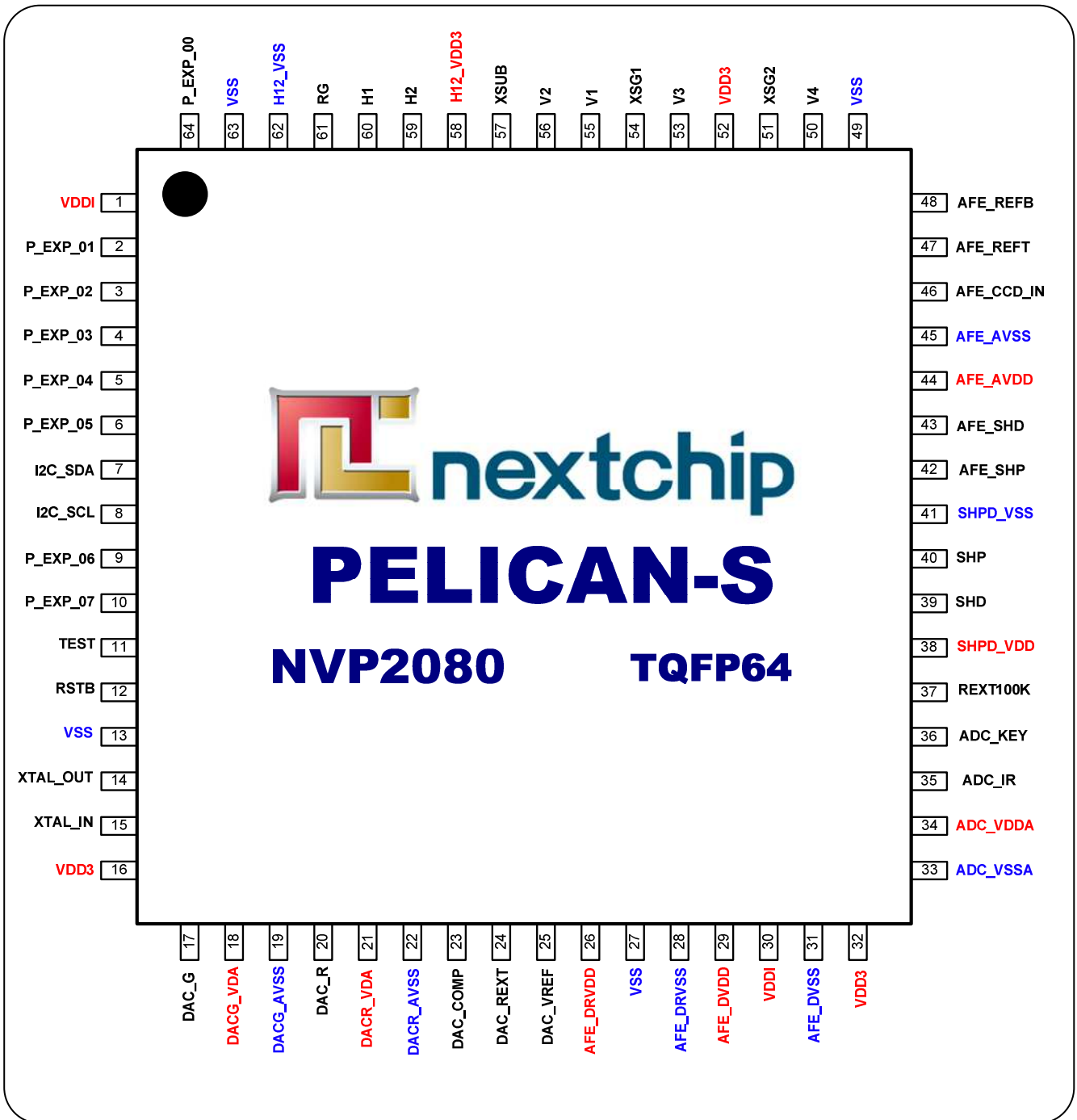
1.2 Pin description

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	VDDI	P	1.8V Digital power
2	P_EXP_01	B	GPIO In/Out
3	P_EXP_02	B	GPIO In/Out
4	P_EXP_03	B	GPIO In/Out
5	P_EXP_04	B	GPIO In/Out
6	P_EXP_05	B	GPIO In/Out
7	I2C_SDA	B	I2C data signal
8	I2C_SCL	B	I2C clock
9	P_EXP_06	B	GPIO in/out
10	P_EXP_07	B	GPIO in/out
11	TEST	I	Chip test pin
12	RESET	I	System reset pulse (active low)
13	VSS	G	Digital ground
14	XTAL_OUT	O	X-tal output
15	XTAL_IN	I	X-tal input (960 : 36MHz, NTSC : 28.6363MHz, PAL : 28.375MHz)
16	VDD3	P	3.3V Digital power
17	DAC_G	O	LUMA / CHROMA / CVBS / IRIS signal output
18	DACG_VDA	P	Analog power
19	DACG_AVSS	G	Analog ground
20	DAC_R	O	LUMA / CHROMA / CVBS / IRIS signal output
21	DACR_VDA	P	Analog power
22	DACR_AVSS	G	Analog ground
23	DAC_COMP	O	DAC12 comparator reference
24	DAC_REXT	B	DAC12 current reference
25	DAC_VREF	O	DAC12 voltage reference
26	AFE_DRVDD	P	3.3V AFE digital power
27	VSS	G	Digital ground
28	AFE_DRVSS	G	AFE digital ground
29	AFE_DVDD	P	3.3V AFE digital power
30	VDDI	P	1.8V digital power
31	AFE_DVSS	G	AFE digital ground
32	VDD3	P	3.3V digital power
33	ADC_VSSA	G	Analog ground
34	ADC_VDDA	P	Analog power
35	ADC_IR	I	IR CDS
36	ADC_KEY	I	ADC key
37	REXT100K	I	Analog input (100Kohm external resistor)
38	SHPD_VDD	P	3.3V Digital power
39	SHD	O	Charge CDS sample & hold pulse for data
40	SHP	O	CDS sample & hold pulse for pre-charge
41	SHPD_VSS	G	Digital ground
42	AFE_SHP	I	CDS sample & hold pulse for pre- charge(AFE)
43	AFE_SHD	I	charge CDS sample & hold pulse for data(AFE)
44	AFE_AVDD	P	AFE analog power
45	AFE_AVSS	G	AFE analog ground
46	AFE_CCD_IN	I	Analog input for CCD signal
47	AFE_REFT	O	A/D converter top reference voltage decoupling

PIN NO.	SYMBOL	I/O	DESCRIPTION
48	AFE_REFB	O	A/D converter bottom reference voltage decoupling
49	VSS	G	Digital ground
50	V4	O	CCD vertical driving pulse phase-4
51	XSG2	B	CCD read out pulse 2
52	VDD3	P	3.3V digital power
53	V3	O	CCD vertical driving pulse phase-3
54	XSG1	B	CCD read out pulse 1
55	V1	B	CCD vertical driving pulse phase-1
56	V2	B	CCD vertical driving pulse phase-2
57	XSUB	B	CCD shutter speed control pulse
58	H12_VDD3	P	5.0V digital power(H1/H2/RG)
59	H2	O	CCD horizontal driving pulse 2
60	H1	O	CCD horizontal driving pulse 1
61	RG	O	CCD reset gate pulse
62	H12_VSS	G	Digital ground
63	VSS	G	Digital ground
64	P_EXP_00	B	GPIO in/out

2. Information

2.1 Compare table

Function name	PELICAN-S (NVP2080)	PELICAN-N (NVP2081)	REFIA-S (NVP2090)
Support CCD	NEPIS	NEPIS	SONY/SHARP 510H/760H/960H
960 CCD support	X	X	O
On-chip AFE	O	O	O
Horizontal resolution	650	650	420/650/700
Dead pixel correction count	247	247	247
Motion detection	O	X	O
OSD	O	X	O
Coaxial communication	O	X	O

3. Electrical characteristics
3.1.   Absolute maximum ratings

Parameter	Min	Max	Unit
Power supply voltage	-0.5	6	V
Voltage on any 3.3V input pin	3.0	3.6	V
Voltage on any 5V input pin	4.5	5.5	V
Storage temperature	-40	125	℃

3.2.   Recommended operating condition

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Digital power supply voltage	VDD3 SHPD_VDD3 AFE_DRVDD AFE_DVDD	3.0	3.3	3.6	V
3.3V Analog power supply voltage	ADC_VDDA DACG_VDA DACR_VDA AFE_AVDD	3.0	3.3	3.6	V
5.0V Digital power supply voltage	H12_VDD3	4.5 3.0	5.0 3.3	5.5 3.6	V
Industrial temperature range	T_A	-20	-	85	℃

3.3   DC characteristics

Parameter	Symbol	Min	Typ	Max	Unit
3.3V IO *Note1					
Input low voltage	V_{IL3}	-0.3	-	0.8	V
Input high voltage	V_{IH3}	2.0	-	5.5	V
Input Leakage current	I_{IL3}	-	-	±10	uA
Threshold point	V_{T3}	1.35	1.47	1.60	V
Schmitt trig Low to High threshold point	V_{T3+}	1.40	1.50	1.59	V
Schmitt trig. High to Low threshold point	V_{T3-}	0.88	0.94	1.00	V
Output low voltage	V_{OL3}	-	-	0.4	V
Output high voltage	V_{OH3}	2.4	-	-	V
5.0V IO *Note2					
Input low voltage	V_{IL5}	-0.3	-	0.8	V
Input high voltage	V_{IH5}	2.0	-	5.5	V
Input Leakage current	I_{IL5}	-	-	±10	uA
Threshold point	V_{T5}	1.33	1.44	1.48	V
Schmitt trig Low to High threshold point	V_{T5+}	1.82	1.96	2.04	V
Schmitt trig. High to Low threshold point	V_{T5-}	1.12	1.22	1.28	V
Output low voltage	V_{OL5}	-	-	0.4	V
Output high voltage	V_{OH5}	2.4	-	-	V

*Note1 : 3.3V data pins(expect 5V data pins)
*Note2 : 5V data pins(XRG, H1, H2 pins)   /   3.3V data pins(XRG, H1, H2 pins)

4. Package information
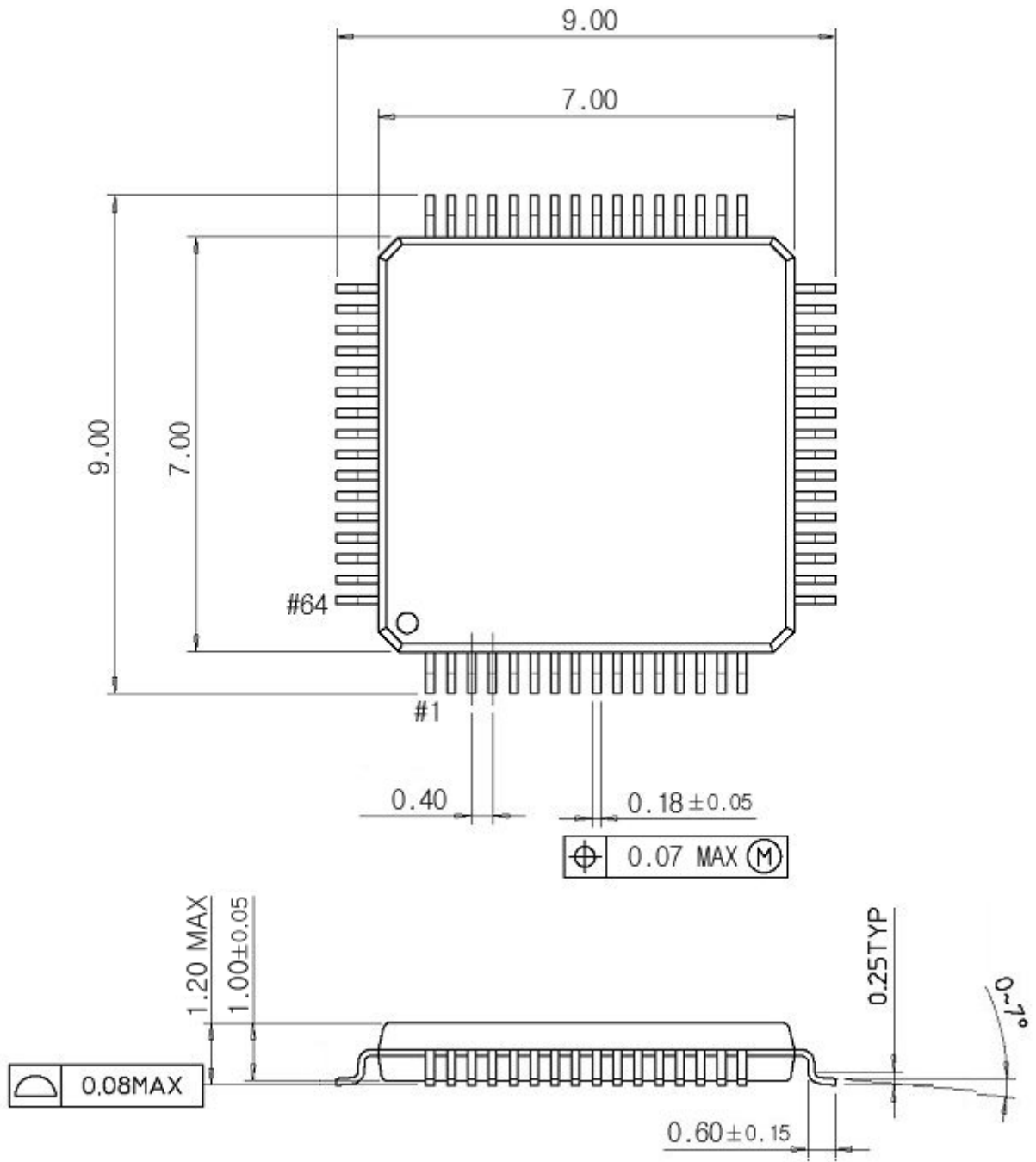
Package	Type	Pin pitch	Size(WxD)
	64 - TQFP	0.40mm	7x7mm

5. Revision history

REVISION	DATE	DESCRIPTION
rev 1.0	2012.03.20	ㆍGenerated

6. Contact information

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