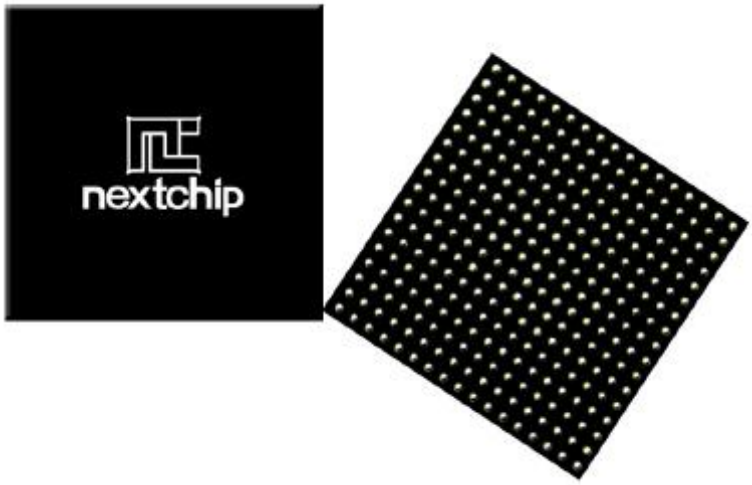
NVP2170E Data Sheet

High End CCD Image Signal Processor



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REV 1.0

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High end CCD Image Signal Processor

NVP2170E is image signal processor(ISP) which outputs image as CVBS or S-Video after receiving color filter array(CFA) patterns from the color-interlaced CCD interface, which are processed through an internal encoder and DAC.

Equipped with built-in MCU, NVP2170E can be provided OSD menu basically, which is enable to make up to 1024 letters as depending on user's choice without extra MCU.

To make CCD camera system be simplified NVP2170E is built-in timing generator(TG), and as further function there are 3D-NR to reduce the noise, Sense-Up function, Digital zoom for magnifying image without extra zoom lenses, privacy mask zone, motion detection, and etc.

Features

-. Input : NTSC/PAL, 760H CCD format
-. Output : NTSC/PAL analog S-Video or CVBS
ITU-R.656 digital out (27MHz/28.6366MHz/28.375MHz)
-. Programmable GAMMA processing
-. H/V aperture
-. Video adjustment (brightness, contrast, saturation and hue)
-. High quality color processing
-. H/V MIRROR
-. On Screen Display (OSD)
-. Blemish compensation(auto : 128 points / manual : 4 points)
-. Color rolling / Breathing suppress.
-. Supports horizontal resolution 560TV lines
-. Privacy mask 8 zone
-. Motion detection (detection area : 4 area)
-. Digital Wide Dynamic Range expansion
- Digital-Zoom
- 3D-Noise Reducer On/Off
- Support line lock external synchronization
-. Sense-up (~x256)
-. On-chip optical detector (AE/AWB/AF)
-. On-chip CCD timing generator
-. On-chip NTSC/PAL video encoder
-. On-chip 2CH DACx2 (S-video or CVBS or IRIS)
-. On-chip 1CH ADC(4CH MUX)
-. Include MCU(63KB SRAM)
-. Serial interface for AFE
-. Serial Peripheral Interface(3-wire)
-. 5.0V / 3.3V / 1.8 V operation

Ordering Information

Device	Package	Temperature Range
NVP2170E	144-FBGA	-25℃ ~ 85℃

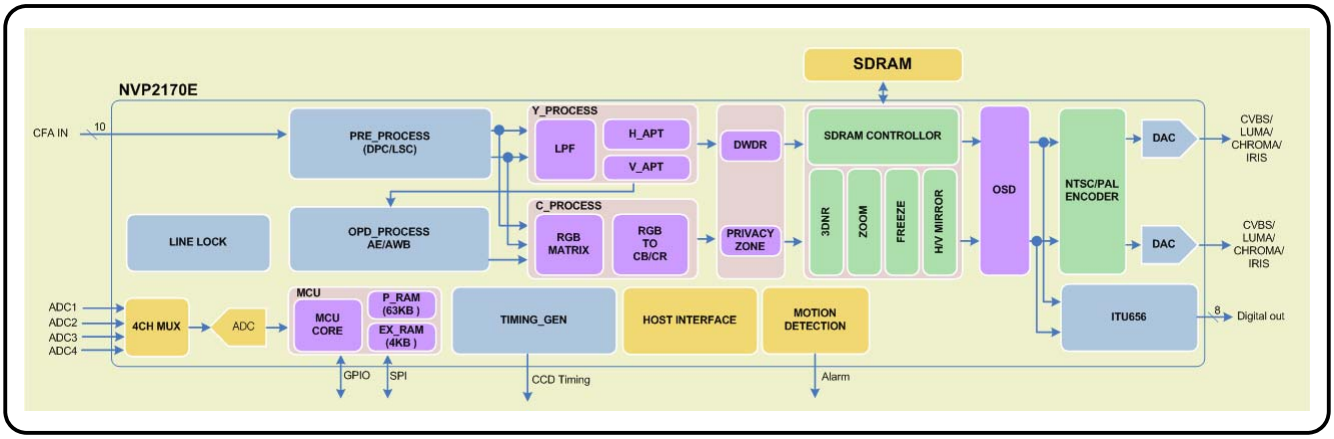
Applications

-. CCD camera
-. Zoom Lens Box camera
-. Video phone camera
-. Rear-view monitoring camera

Related Products

-. CCD : 760H color-interlaced CCD
(SONY, SHARP CCD)
-. AFE : AD9943 , HD49343HNP
-. V-Driver : NVD2014A (NEXTCHIP)

Functional Block Diagram



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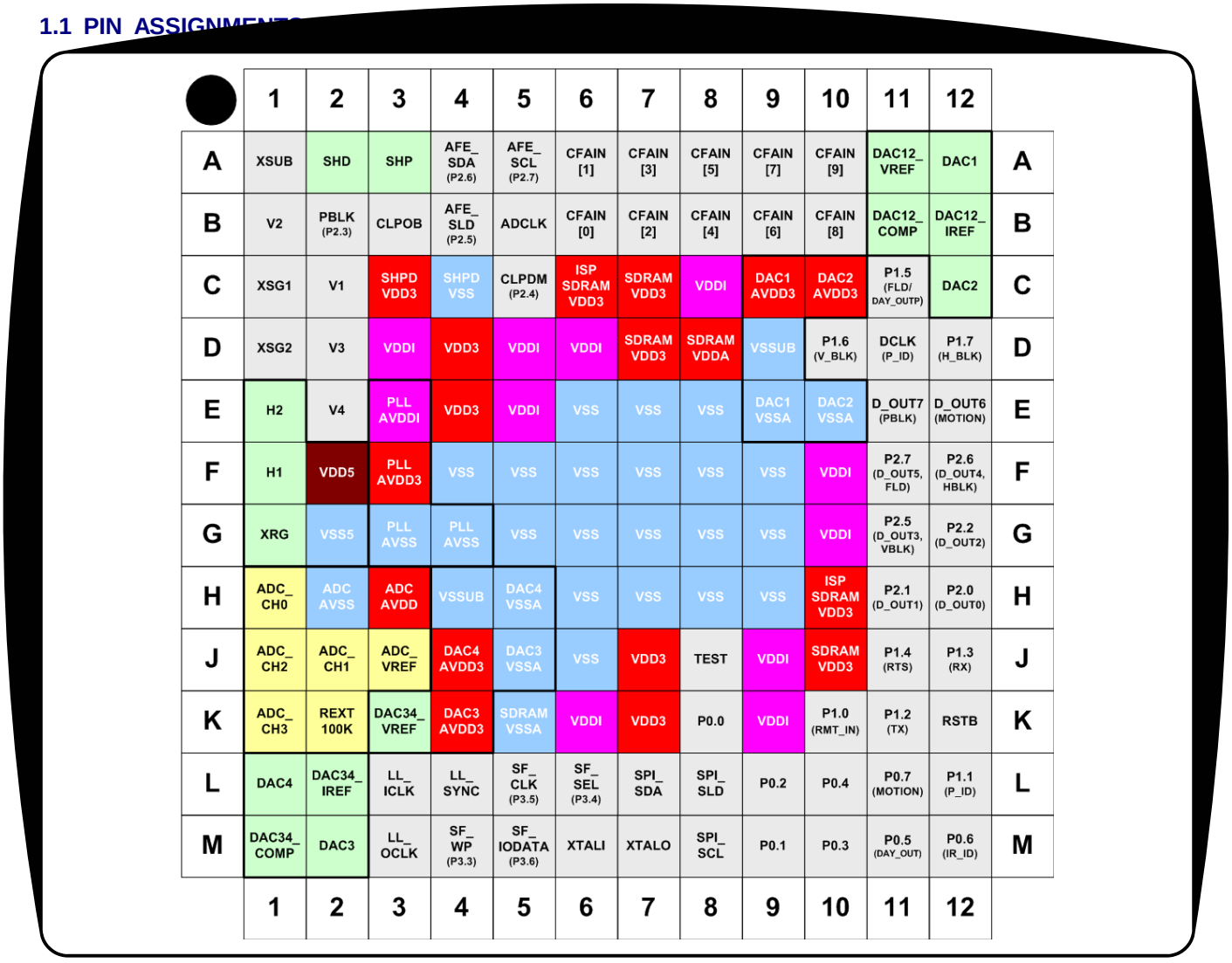
1. PIN INFORMATION

1.1 PIN ASSIGNMENT



	1	2	3	4	5	6	7	8	9	10	11	12	
A	XSUB	SHD	SHP	AFE_SDA (P2.6)	AFE_SCL (P2.7)	CFAIN [1]	CFAIN [3]	CFAIN [5]	CFAIN [7]	CFAIN [9]	DAC12_VREF	DAC1	A
B	V2	PBLK (P2.3)	CLPOB	AFE_SLD (P2.5)	ADCLK	CFAIN [0]	CFAIN [2]	CFAIN [4]	CFAIN [6]	CFAIN [8]	DAC12_COMP	DAC12_IREF	B
C	XSG1	V1	SHPD VDD3	SHPD VSS	CLPDM (P2.4)	ISP SDRAM VDD3	SDRAM VDD3	VDDI	DAC1 AVDD3	DAC2 AVDD3	P1.5 (FLD/ DAY_OUTP)	DAC2	C
D	XSG2	V3	VDDI	VDD3	VDDI	VDDI	SDRAM VDD3	SDRAM VDDA	VSSUB	P1.6 (V_BLK)	DCLK (P_ID)	P1.7 (H_BLK)	D
E	H2	V4	PLL AVDDI	VDD3	VDDI	VSS	VSS	VSS	DAC1 VSSA	DAC2 VSSA	D_OUT7 (PBLK)	D_OUT6 (MOTION)	E
F	H1	VDD5	PLL AVDD3	VSS	VSS	VSS	VSS	VSS	VSS	VDDI	P2.7 (D_OUT5, FLD)	P2.6 (D_OUT4, HBLK)	F
G	XRG	VSS5	PLL AVSS	PLL AVSS	VSS	VSS	VSS	VSS	VSS	VDDI	P2.5 (D_OUT3, VBLK)	P2.2 (D_OUT2)	G
H	ADC_CH0	ADC AVSS	ADC AVDD	VSSUB	DAC4 VSSA	VSS	VSS	VSS	VSS	ISP SDRAM VDD3	P2.1 (D_OUT1)	P2.0 (D_OUT0)	H
J	ADC_CH2	ADC_CH1	ADC_VREF	DAC4 AVDD3	DAC3 VSSA	VSS	VDD3	TEST	VDDI	SDRAM VDD3	P1.4 (RTS)	P1.3 (RX)	J
K	ADC_CH3	REXT 100K	DAC34_VREF	DAC3 AVDD3	SDRAM VSSA	VDDI	VDD3	P0.0	VDDI	P1.0 (RMT_IN)	P1.2 (TX)	RSTB	K
L	DAC4	DAC34_IREF	LL_ICLK	LL_SYNC	SF_CLK (P3.5)	SF_SEL (P3.4)	SPI_SDA	SPI_SLD	P0.2	P0.4	P0.7 (MOTION)	P1.1 (P_ID)	L
M	DAC34_COMP	DAC3	LL_OCLK	SF_WP (P3.3)	SF_IODATA (P3.6)	XTALI	XTALO	SPI_SCL	P0.1	P0.3	P0.5 (DAY_OUT)	P0.6 (IR_ID)	M
	1	2	3	4	5	6	7	8	9	10	11	12	

1.2 PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
A1	XSUB	O	CCD shutter speed control pulse
B1	V2	O	CCD vertical driving pulse phase-2
C2	V1	O	CCD vertical driving pulse phase-1
C1	XSG1	O	CCD Read out pulse 1
D2	V3	O	CCD vertical driving pulse phase-3
D1	XSG2	O	CCD Read out pulse 2
E2	V4	O	CCD vertical driving pulse phase-4
E1	H2	O	CCD Horizontal Driving pulse 2
F1	H1	O	CCD Horizontal Driving pulse 1
G1	XRG	O	CCD Reset gate pulse
A3	SHP	O	CDS sample & hold pulse for pre-charge
A2	SHD	O	CDS sample & hold pulse for data
B5	ADCLK	O	ADC sampling clock
B3	CLPOB	O	Optical Black signal
B2	PBLK(P2.3)	I/O	Pixel Blanking / GPIO 2.3
C5	CLPDM(P2.4)	I/O	Dummy cell clamping pulse / GPIO 2.4
B4	AFE_SLD(P2.5)	I/O	Serial Enable (AFE interface) / GPIO 2.5
A4	AFE_SDA(P2.6)	I/O	Serial data input/output (AFE interface) / GPIO 2.6
A5	AFE_SCL(P2.7)	I/O	Serial interface clock (AFE interface) / GPIO 2.7
B6	CFAIN[0]	I	CCD CFA pattern input 0
A6	CFAIN[1]	I	CCD CFA pattern input 1
B7	CFAIN[2]	I	CCD CFA pattern input 2
A7	CFAIN[3]	I	CCD CFA pattern input 3
B8	CFAIN[4]	I	CCD CFA pattern input 4
A8	CFAIN[5]	I	CCD CFA pattern input 5
B9	CFAIN[6]	I	CCD CFA pattern input 6
A9	CFAIN[7]	I	CCD CFA pattern input 7
B10	CFAIN[8]	I	CCD CFA pattern input 8
A10	CFAIN[9]	I	CCD CFA pattern input 9
M6	XTALI	I	X-tal input(NTSC:28.6363Mhz : PAL:28.375Mhz)
M7	XTALO	O	X-tal output
K12	RSTB	I	system reset pulse (active low)
L3	LL_ICLK	I	Line Lock input clock
M3	LL_OCLK	O	Line Lock output clock
L4	LL_SYNC	I	Line Lock External Sync
L8	SPI_SLD	I/O	SPI load signal
M8	SPI_SCL	I/O	SPI clock
L7	SPI_SDA	I/O	SPI data signal
M4	SF_WP(P3.3)	I/O	Serial Flash Write Protect / GPIO 3.3
L6	SF_SEL(P3.4)	I/O	Serial Flash select / GPIO 3.4
L5	SF_CLK(P3.5)	I/O	Serial Flash clk / GPIO 3.5
M5	SF_IODATA(P3.6)	I/O	Serial Flash IO data / GPIO 3.6
K8	P0.0	I/O	GPIO 0.0
M9	P0.1	I/O	GPIO 0.1
L9	P0.2	I/O	GPIO 0.2
M10	P0.3	I/O	GPIO 0.3

PIN NO.	SYMBOL	I/O	DESCRIPTION
L10	P0.4	I/O	GPIO 0.4
M11	P0.5(DAY_OUT)	I/O	Day & Night ON/OFF pulse / GPIO 0.5
M12	P0.6(IR_ID)	I/O	IR ON/OFF pulse / GPIO 0.6
L11	P0.7(MOTION)	I/O	Motion alarm pulse / GPIO 0.7
K10	P1.0(RMT_IN)	I/O	Remote control pulse input / GPIO 1.0
L12	P1.1(P_ID)	I/O	Power generation pulse / GPIO 1.1
K11	P1.2(TX)	I/O	485 TX / GPIO 1.2
J12	P1.3(RX)	I/O	485 RX / GPIO 1.3
J11	P1.4(RTS)	I/O	485 RTS / GPIO 1.4
C11	P1.5(FLD/DAY_OUTP)	I/O	FLD / Day & Night ON/OFF invert pulse / GPIO 1.5
D10	P1.6(V_BLK)	I/O	Vertical Blank pulse
D12	P1.7(H_BLK)	I/O	Horizantal Blank pulse
D11	DCLK(P_ID)	O	Digital Clock
H12	P2.0(D_OUT[0])	I/O	Digital data out 0 / GPIO 2.0
H11	P2.1(D_OUT[1])	I/O	Digital data out 1 / GPIO 2.1
G12	P2.2(D_OUT[2])	I/O	Digital data out 2 / GPIO 2.2
G11	P2.5(D_OUT[3]/VBLK)	O	Digital data out 3
F12	P2.6(D_OUT[4]/HBLK)	O	Digital data out 4
F11	P2.7(D_OUT[5]/FLD)	O	Digital data out 5
E12	MOTION(D_OUT[6])	O	Digital data out 6
E11	PBLK(D_OUT[7]	O	Digital data out 7
J8	TEST	I	Test pin
H1	ADC_CH0	I	ADC Channel 0 input
J2	ADC_CH1	I	ADC Channel 1 input
J1	ADC_CH2	I	ADC Channel 2 input
K1	ADC_CH3	I	ADC Channel 3 input
J3	ADC_VREF	-	ADC Voltage reference
K2	REXT100K	-	100K ohm external resistor
A12	DAC1	O	DAC 1 output
C12	DAC2	O	DAC 2 output
B12	DAC12_IREF	-	DAC current reference
A11	DAC12_VREF	-	DAC Voltage reference
B11	DAC12_COMP	-	DAC comparator reference
M2	DAC3	O	DAC 3 output
L1	DAC4	O	DAC 4 output
L2	DAC34_IREF	-	DAC current reference
K3	DAC34_VREF	-	DAC Voltage reference
M1	DAC34_COMP	-	DAC comparator reference

1.3 POWER PIN DESCRIPTION

PIN NO.	SYMBOL	V/G	DESCRIPTION
POWER			
C3	SHPD_VDD3	3.3V	SHP/SHD VDD
F2	VDD5	3.3V/5V	3.3V/5V power(for H1/H2/RG)
H3	ADC_AVDD	3.3V	ADC analog VDD
F3	PLL_AVDD3	3.3V	PLL analog VDD
E3	PLL_AVDDI	1.8V	PLL analog VDD
C9	DAC1_AVDD3	3.3V	DAC1 AVDD
C10	DAC2_AVDD3	3.3V	DAC2 AVDD
K4	DAC3_AVDD3	3.3V	DAC3 AVDD
J4	DAC4_AVDD3	3.3V	DAC4 AVDD
D8	SDRAM_VDDA	3.3V	SDRAM analog VDD
C7,D7,J10	SDRAM_VDD	3.3V	SDRAM digital VDD
C6,H10	ISP_SDRAM_VDD	3.3V	ISP SDRAM digital VDD
C8,D3,D5,D6,E5,F10, G10,J9,K6,K9	VDDI	1.8V	Internal digital VDD
D4,E4,J7,K7	VDD3	3.3V	Digital VDD
GROUND			
C4	SHPD_VSS	G	SHPD Digital ground
G2	VSS5	G	H1/H2/RG Digital ground
G3,G4	PLL_AVSS	G	PLL analog ground
H2	ADC_AVSS	G	ADC analog ground
E9	DAC1_VSSA	G	DAC1 analog ground
E10	DAC2_VSSA	G	DAC2 analog ground
J5	DAC3_VSSA	G	DAC3 analog ground
H5	DAC4_VSSA	G	DAC4 analog ground
D9,H4	VSSUB	G	DAC VSSUB
K5	SDRAM_VSSA	G	SDRAM analog ground
E6,E7,E8,F4,F5,F6,F7, F8,F9,G5,G6,G9,H6,H7, H8,H9,J6,G7,G8	VSS	G	Digital ground

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Power supply voltage	-0.5	6	V
Voltage on any 1..8V input pin	1.62	1.98	V
Voltage on any 3.3V input pin	3.0	3.6	V
Voltage on any 5V input pin	4.5	5.5	V
Storage temperature	-40	125	℃

2.2 RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit
1.8V Digital power supply voltage	VDDI PLL_AVDDI	1.62	1.8	1.98	V
3.3V IO power supply voltage	VDD3 SHPD_VDD3 SDRAM_VDD3 ISP_SDRAM_VDD3	3.0	3.3	3.6	V
3.3V Analog power supply voltage	ADC_AVDD PLL_AVDD3 DAC1_AVDD3 DAC2_AVDD3 DAC3_AVDD3 DAC4_AVDD3 SDRAM_VDDA	3.0	3.3	3.6	V
5.0V IO power supply voltage	VDD5	4.5	5.0	5.5	V
Industrial temperature range	T_A	-25	-	85	℃

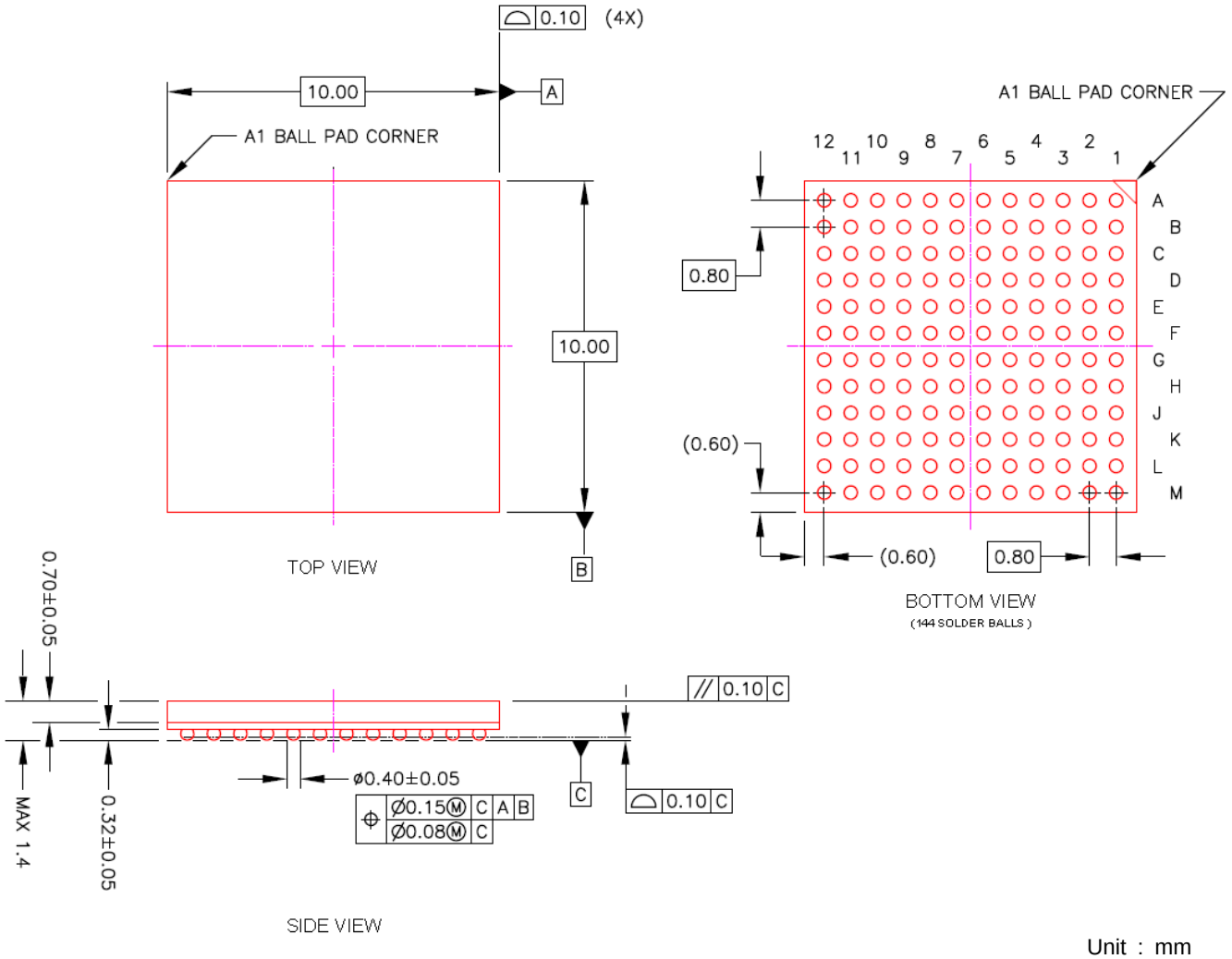
2.3 DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
3.3V IO *Note1					
Input low voltage	V_{IL3}	-0.3	-	0.8	V
Input high voltage	V_{IH3}	2.0	-	5.5	V
Input Leakage current	I_{IL3}	-	-	±10	uA
Threshold point	V_{T3}	1.35	1.47	1.60	V
Schmitt trig Low to High threshold point	V_{T3+}	1.40	1.50	1.59	V
Schmitt trig. High to Low threshold point	V_{T3-}	0.88	0.94	1.00	V
Output low voltage	V_{OL3}	-	-	0.4	V
Output high voltage	V_{OH3}	2.4	-	-	V
5.0V IO *Note2					
Input low voltage	V_{IL5}	-0.3	-	0.8	V
Input high voltage	V_{IH5}	2.0	-	5.5	V
Input Leakage current	I_{IL5}	-	-	±10	uA
Threshold point	V_{T5}	1.33	1.44	1.48	V
Schmitt trig Low to High threshold point	V_{T5+}	1.82	1.96	2.04	V
Schmitt trig. High to Low threshold point	V_{T5-}	1.12	1.22	1.28	V
Output low voltage	V_{OL5}	-	-	0.4	V
Output high voltage	V_{OH5}	2.4	-	-	V

*Note1 : 3.3V data pins(expect 5V data pins)

*Note2 : 5V data pins(XRG, H1, H2 pins)

3. PACKAGE INFORMATION



Unit : mm

NOTE

1. GENERAL TOLERANCE : ± 0.10

Package	Type	Ball pitch	Size(WxD)
	144 - FBGA	0.80mm	10x10mm

4. REVISION HISTORY

REVISION	DATE	DESCRIPTION
rev 1.0	2010.06.	· Generated

5. CONTACT INFORMATION

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