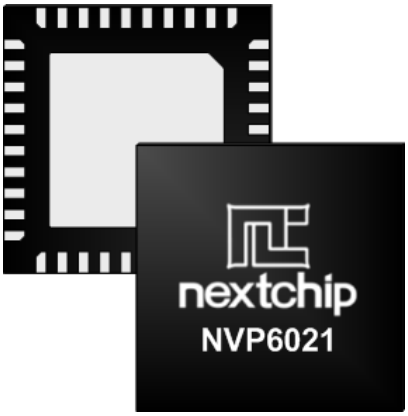
NVP6021



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Make sure to check and use an updated version of the Data sheet.

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2014. 11. 3

REV 0.0

[주]넥스트칩 nextchip

Revision History

VERSION	DATE	DESCRIPTION	NOTE
REV 0.0	2014-10-8	- Initial Draft	

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AHD Video Encoder

The **NVP6021** is high speed, digital-to-analog video encoder in a 40-eQFN package. 3.3 V, video DAC provides support for composite (HD-**AHD1.0/AHD2.0**) analog outputs in high definition (HD) video formats.

The **NVP6021** has a 16-bit video input port that can be configured in a variety of ways. Video input data can be supplied in the YCrCb 4:2:2 color space.

The **NVP6021** also supports embedded EAV/SAV timing codes, and I2C communication protocol.

Table 1 lists the video standards directly supported by the **NVP6021**.

Table 1. Standards Directly Supported by NVP6021

Active Resolution	I/P	Frame Rate (Hz)	Clock Input (MHz)	Standard
1280x720	P	30,60	74.25	BT.1543, SMPTE 296M
1280x720	P	25, 50	74.25	BT.1847, SMPTE 296M
1920x1080	P	30, 25	74.25	BT.1120(BT.709), SMPTE 274M

I = interlaced, P = progressive.

@ AHD Technology

AHD is a video transmission technology in high definition via coaxial cable.

AHD offer specifications - 720p(1280x720), 1080p(1920x1080); which are compatible with the industrial standard 720p and 1080p.

Features

- High quality, video DAC
  - 4x oversampling for HD
  - 2x oversampling for FHD
- Multi-format video input support
  - HD(720p): BT.1543, BT.1847, SMPTE 296M
  - FHD(1080p): BT.1120(BT.709), SMPTE 274M
- Multi-format video output support
  - Composite (AHD1.0/AHD2.0)
- On-chip test pattern generation
  - Color bar, Check, Multi-burst
- Programmable features
  - Color space conversion
  - Luminance and chrominance filter response
  - Subcarrier frequency (fsc) and phase
- 3.3V analog operation
- 1.2V digital operation
- 3.3V I/O operation
- Pin compatible with NVP6011

Application

- CCTV camera
- Automotive infotainment

Ordering Information

Device	Package	Temperature Range
NVP6021	40eQFN	0 ~ 70℃

Functional Block Diagram

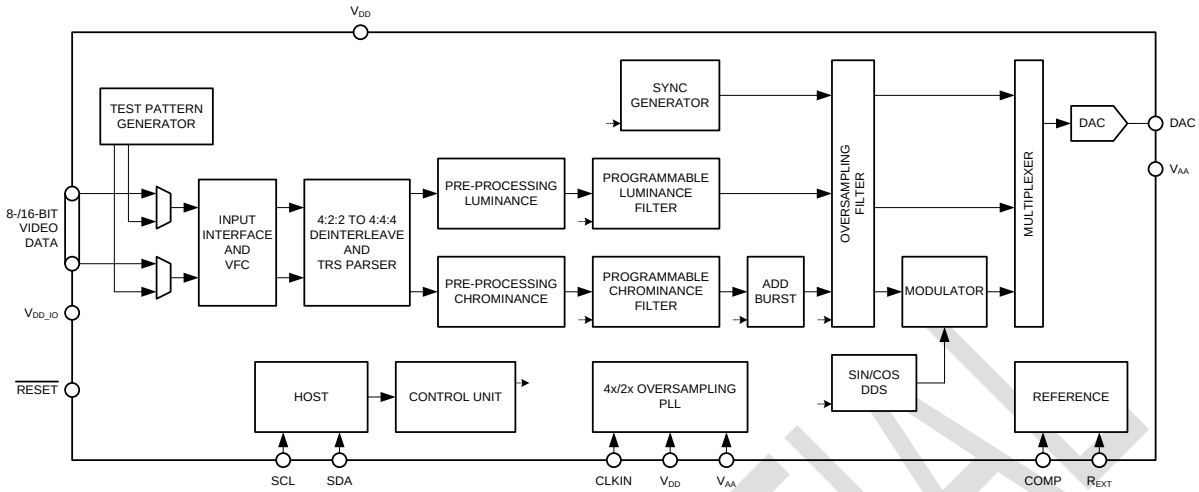


Figure 1.

Contents

1. Pin Information

1.1 Pin Configuration

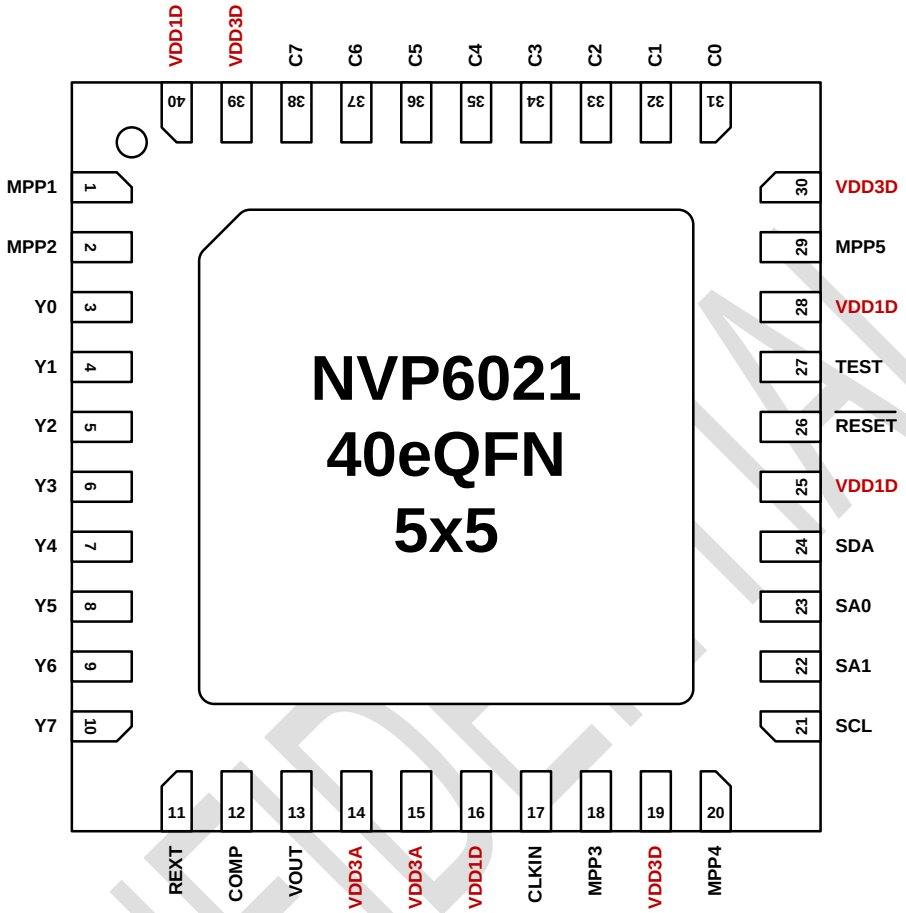


Figure 2.

1.2 Pin Function Descriptions

Table 2. Pin Descriptions

Name	Pin No.	Type	Descriptions
System Clock / Reset			
RESET	26	I	System Reset (Active low).
CLKIN	17	I	Input Clock.
Analog Video Interface			
VOUT	13	O	Analog Video Output.
COMP	12	O	Video DAC Compensation pin.
REXT	11		External Voltage Reference Input for DAC.
Digital Video Interface			
Y7 to Y0	3, 4, 5, 6, 7, 8, 9, 10	I	8-Bit Pixel Port (Y7 to Y0). Y0 is the LSB.
C7 to C0	31, 32, 33, 34, 35, 36, 37, 38	I	8-Bit Pixel Port (C9 to C0). C0 is the LSB.
etc.			
TEST	27	I	Chi Test Enable Pin (Connect to Ground).
MPP5	29	I	Chi Test Enable Pin (Connect to Ground).
MPP#	1, 2, 18, 20	B	MPP1~4, Multi-Purpose pins.
I^2C Interface			
SDA	24	I/O	I^2C Data Input/Output (3.3V tolerant).
SCL	21	I	I^2C Clock Input (3.3V tolerant).
SA1, SA0	22, 23	I	Slave Address.
Power			
VDD1D	16, 25, 28, 40		Digital Power Supply (Digital 1.2V).
VDD3D	19, 30, 39		Digital Power Supply (Digital 3.3V).
VDD3A	14, 15		Analog Power Supply (Analog 3.3V).
Expose Pad			Ground.

2. Detailed Description

2.1 Input Video Data Formats

The NVP6021 support a number of different input modes. The desired input mode is selected using register. Table 3 provides an overview of all possible input configurations. Each input mode is described in detail in this section.

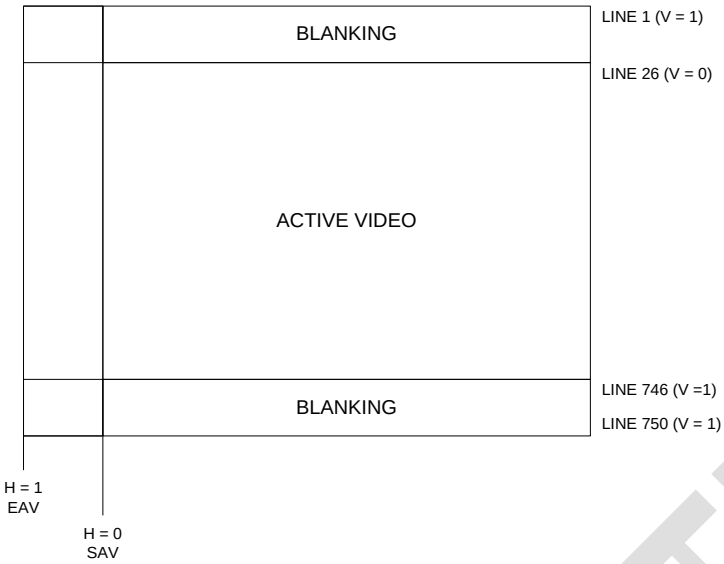
Table 3. NVP6021 Input Configuration

Input Mode			Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	C7	C6	C5	C4	C3	C2	C1	C0
HD	16-bit	1280x720x30p	Y								CbCr							
			FORMAT = 0xEA															
		1280x720x25p	Y								CbCr							
			FORMAT = 0xEB															
		1280x720x60p	Y								CbCr							
			FORMAT = 0xE2															
		1280x720x50p	Y								CbCr							
			FORMAT = 0xE3															
FHD	16-bit	1920x1080x30p	Y								CbCr							
			FORMAT = 0xF0															
		1920x1080x25p	Y								CbCr							
			FORMAT = 0xF1															

2.1.1 High Definition Video Input Formats - 720p

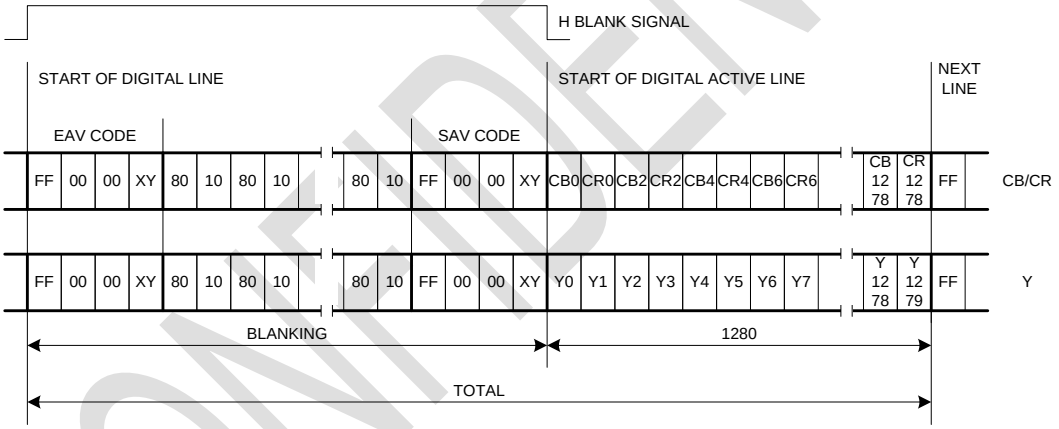
The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for progressive scan 720-line HD image formats. SMPTE 296M specifies the representation for 720p digital YCbCr 4:2:2 signals at pixel rates of 74.25MHz. To reduce the number of wires required for the interface, timing codes are embedded in the video stream to provide information traditionally transmitted by dedicated HSYNC, VSYNC, and BLANK signals. Figure 3 and Figure 4 show the multiplexed 16-bit 4:2:2 YCbCr data for 720 line video. The start of active video and the end of active video are marked by the SAV and EAV codes, respectively. The values of these codes are reserved for this purpose and should not occur elsewhere in the video raster. F, V, H timing information is stored in the 8-bit XY word as follows:

- Bit 6 - (F-bit) 0 for field one; and 1 for field two
- Bit 5 - (V-bit) 1 in vertical blanking interval; and 0 during active video lines
- Bit 4 - (H-bit) 1 indicates the EAV sequence; and 0 indicates the SAV sequence



LINE NUMBER	F	V
1-25	0	1
26-745	0	0
746-750	0	1

Figure 3. Digital Vertical Timing. 720p system.



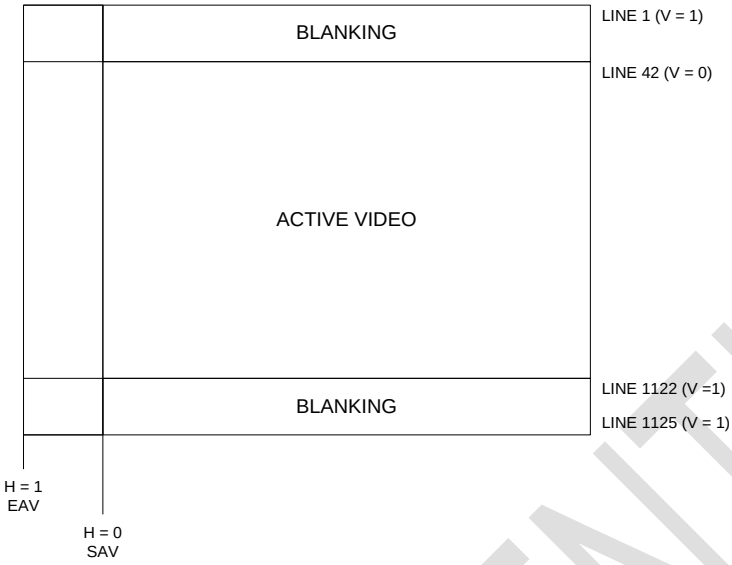
FRAME RATE	TOTAL	BLANKING
25	3960	2680
30	3300	2020
50	1980	700
60	1650	370

Figure 4. Parallel Interface Data for One Scan Line. 720p; 4:2:2 YCbCr; 1280 active samples per line; 74.25MHz clock; 16-bit system.

2.1.2 High Definition Video Input Formats - 1080p

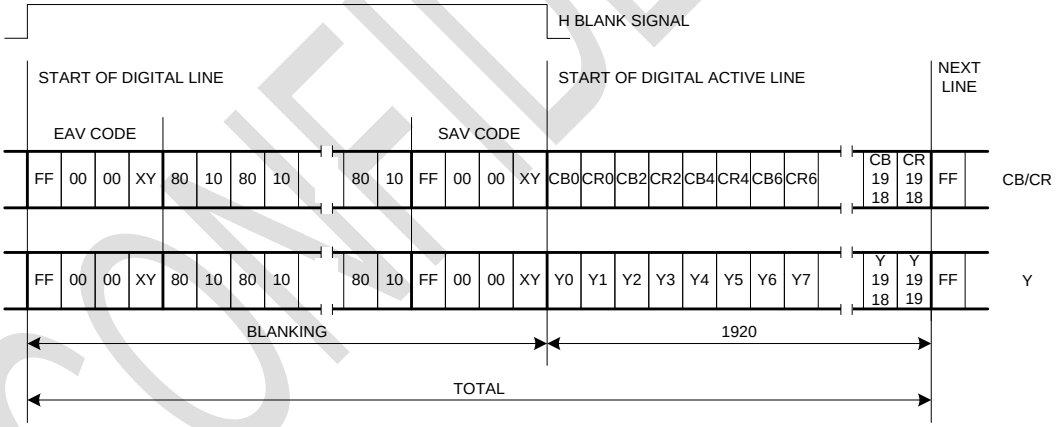
The Society of Motion Picture and Television Engineers (SMPTE) and ITU defines the standard for progressive scan 1080-line HD image formats. SMPTE 274M and ITU-R BT.709(BT.1120) specifies the representation for 1080p digital YCbCr 4:2:2 signals at pixel rates of 74.25MHz. As with HD video

input formats, the field/frame blanking period (V), the line blanking period (H), and the field identification (F), are embedded as digital timing codes (TRS) within the video.



LINE NUMBER	F	V
1-41	0	1
42-1121	0	0
1122-1125	0	1

Figure 5. Digital Vertical Timing. 1080p system.



FRAME RATE	TOTAL	BLANKING
25	2640	720
30	2200	280

Figure 6. Parallel Interface Data for One Scan Line. 1080p; 4:2:2 YCbCr; 1920 active samples per line; 74.25MHz clock; 16-bit system.

2.2 Pre-processing

2.2.1 Color Space Conversion Matrix

The internal color space conversion (CSC) matrix automatically performs color space conversions based on the color mode programmed in the mode select register (Bank2, 0x14). Table shows the coefficients in this matrix.

The CSC matrix scalar uses the following equations:

Y = a1 × (Y' - 64)

U = b1 × (Cb' - 64)

V = c1 × (Cr' - 64)

Table 4. Color Space Conversion Coefficients. (YCbCr to YUV)

Parameter	a1	b1	c1
Mode 0	0.591	0.504	0.711
Mode 1	0.625	0.533	0.752

2.2.2 Luminance, Chrominance and Color Burst Scale Control

The luminance, chrominance and color burst scale control feature can be used to scale the Y, Cb, Cr and color burst output levels. This feature can be controlled using Bank2, 0x1C, 0x1D, 0x1E, 0x37. This feature affects all output signals.

Four 8-bit registers (Y scale, Cb scale, Cr scale, and Color burst scale) control the scaling of the Y, Cb, Cr and color burst output levels. The Y scale register contains the scaling factor used to scale the Y level from 0.0 to 2.0 times its initial level. The Cb scale and Cr scale registers contain the scaling factors to scale the Cb and Cr levels from 0.0 to 2.0 times their initial levels, respectively. The color burst scale register contains the scaling factor used to scale the Y level from 0.0 to 2.0 times its initial level.

The values to be written to these 8-bit registers are calculated using the following equation:

Y, Cb, Cr or Color burst Scale Value = Scale Factor × 128

For example, if Scale Factor = 1.3

Y, Cb, Cr or Color burst Value = 1.3 × 128 = 166.4

Y, Cb, Cr or Color burst Value = 166 (rounded to the nearest integer)

Y, Cb, Cr or Color burst Value = 10100110b = 0xA6

It is recommended that the Luminance scale saturation feature be controlled when scaling the Y output level to avoid excessive Y output levels.

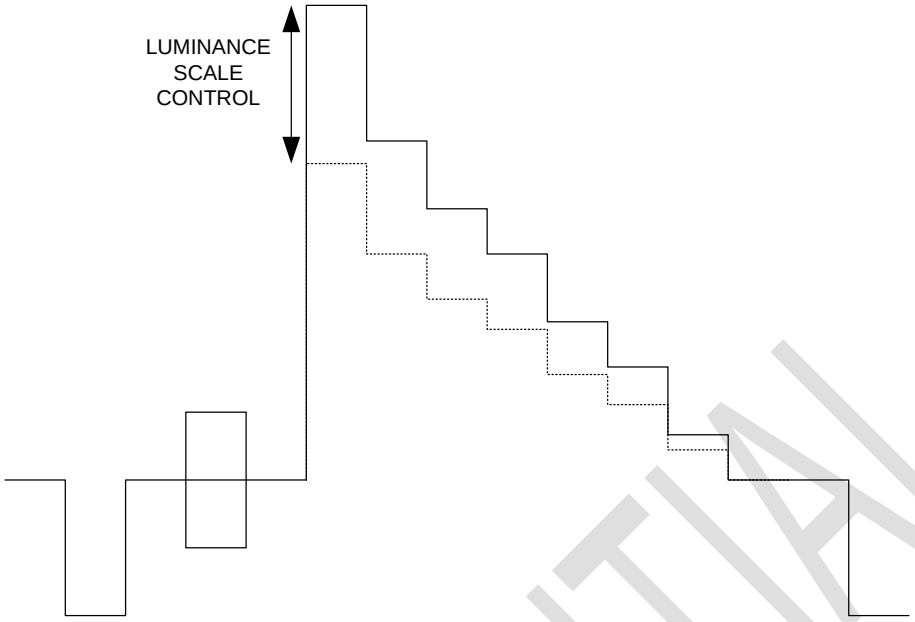


Figure 7. Luminance Scale Control.

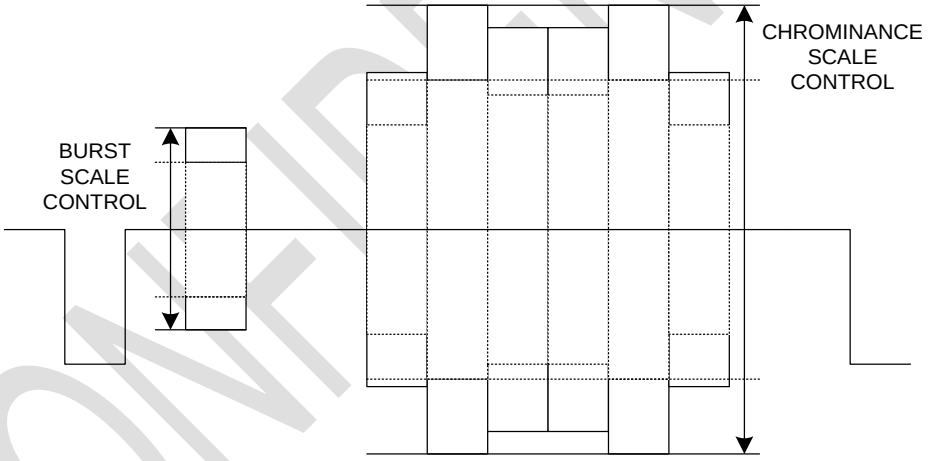


Figure 8. Chrominance and Color Burst Scale Control.

2.3 Filter-processing

The Y filter supports several different frequency responses, including twelve low-pass responses, as shown in Figure 9.

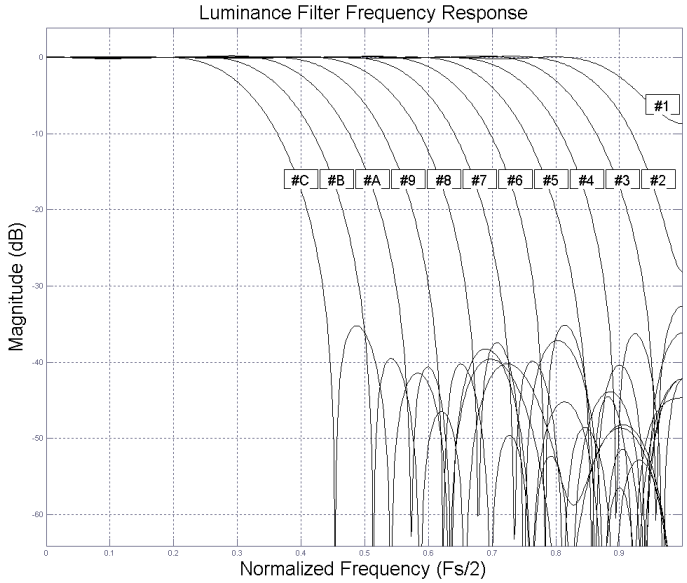


Figure 9. Luminance Filter Frequency Response.

The CbCr filter supports several different frequency responses, including eight low-pass responses, as shown in Figure 10.

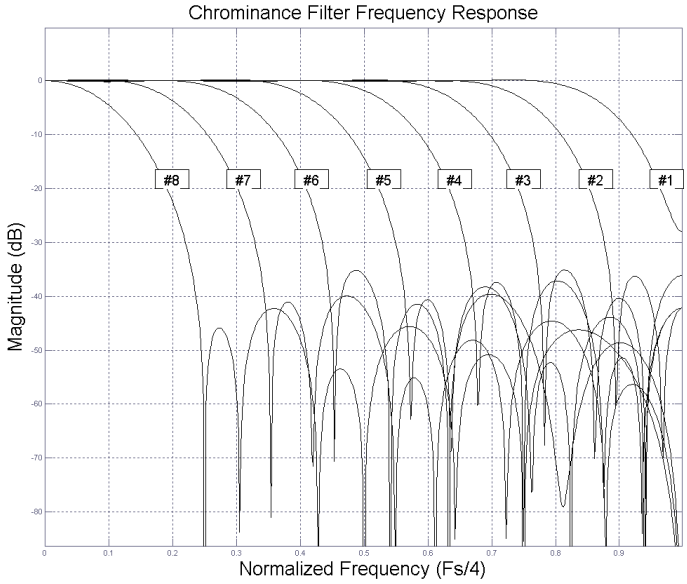


Figure 10. Chrominance Filter Frequency Response

3. HOST Description

3.1 I²C Operation

The NVP6021 supports a 2-wire serial bus driving multiple peripherals. This port operates in an open-drain configuration. Two wires, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus and the NVP6021. The slave address depends on the slave address pins, and the operations (read or write). See Figure 12 The LSB sets either a read or a write operation. Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation. Figure 18 Shows bus write and read sequences.

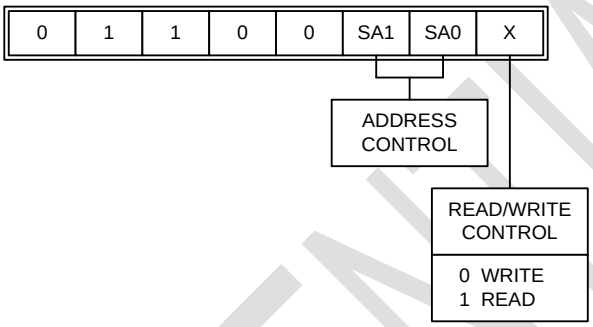


Figure 11. NVP6021 I²C Slave Address.

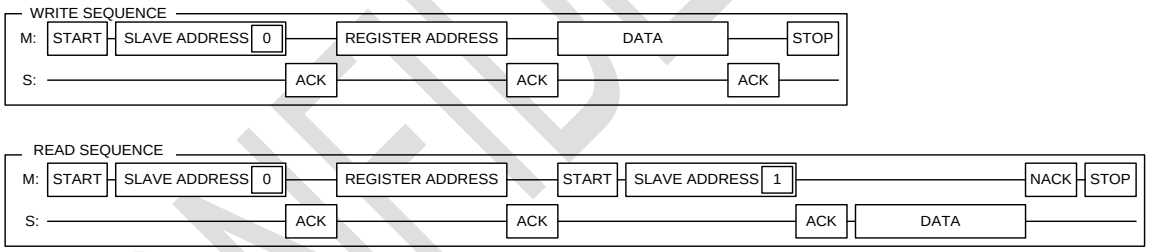


Figure 12. I²C Write and Read Sequence

4. Register Map Access

A microprocessor can read from or write to all registers of the NVP6021 via HOST, except for registers that are specified as read-only or write-only registers.

4.1 Register Programming

Table 5 to Table 7 describes the functionality of each register. All registers can be read from as well as written to, unless otherwise stated.

Table 5. Bank0 Register

Address		Register name	Bits	Description	1080p30	1080p25	720p60	720p50	720p30	720p25
Ba	Addr									
BANK0	0x00	SYSTEM_MODE	[1]	: PLL mode select 0: Auto mode, 1: Manual mode	0x00	0x00	0x00	0x00	0x00	0x00
			[2]	: Clock phase mode select 0: Auto mode, 1: Manual mode	0x00	0x00	0x00	0x00	0x00	0x00
	0x01	MAIN_FORMAT	[7:0]	: Video format select 0xF0: 1080p30, 0xF1: 1080p25 0xE2: 720p60, 0xE3: 720p50 0xEA: 720p30, 0xEB: 720p25	0xF0	0xF1	0xE2	0xE3	0xEA	0xEB
	0x04	PD_DAC	[0]	: DAC power 0: Power on, 1: Power off	0x00	0x00	0x00	0x00	0x00	0x00
	0x05	PD_PLL	[0]	: PLL power 0: Power on, 1: Power off	0x00	0x00	0x00	0x00	0x00	0x00
		PLL_BYPASS	[1]	: PLL bypass 0: Normal operation, 1: Bypass	0x00	0x00	0x00	0x00	0x00	0x00
		PLL_RST	[3]	: PLL reset 0: Normal operation, 1: Reset	0x00	0x00	0x00	0x00	0x00	0x00
		PLL_C	[4]	: PLL value applie 0: Stable, 1: Applied	0x00	0x00	0x00	0x00	0x00	0x00
	0x06	PLL_M	[7:0]	: Feedback 8-bit divider control	0x40	0x40	0x40	0x40	0x3A	0x3A
	0x07	PLL_N	[3:0]	: Input 4-bit divider control	0x08	0x08	0x08	0x08	0x0F	0x0F
		PLL_OD	[5:4]	: Output divider control	0x01	0x01	0x01	0x01	0x01	0x01
	0x10	DIV_SRC_SEL	[3:0]	: Video clock source select	0x00	0x00	0x00	0x00	0x00	0x00
	0x11	CLK_INPUT_SEL	[3:0]	: Input clock select	0x00	0x00	0x00	0x00	0x00	0x00
		CLK_INPUT_IF_SEL	[7:4]	: Input interface clock select 0: Input clock, 1: Input clock inversion, 2: Input clock/2 phase 0, 3: Input clock/2 phase 1	0x00	0x00	0x00	0x00	0x00	0x00
					0x00	0x00	0x00	0x00	0x00	0x00
	0x12	CLK_VFC_SEL	[3:0]	: VFC clock select 0: PLL_OUT/4 phase 0, 1: PLL_OUT/4 phase 1, 2: PLL_OUT/4 phase 2, 3: PLL_OUT/4 phase 3, 4: PLL_OUT/2 phase 0, 5: PLL_OUT/2 phase 1, 6: Input clock, 7: Input clock inversion, 8: Input clock/2 phase 0, 9: Input clock/2 phase 1	0x00	0x00	0x00	0x00	0x00	0x00
		CLK_SAMPLING_SEL	[7:4]	: Sampling clock select 0: PLL_OUT/4 phase 0, 1: PLL_OUT/4 phase 1, 2: PLL_OUT/4 phase 2, 3: PLL_OUT/4 phase 3, 4: PLL_OUT/2 phase 0, 5: PLL_OUT/2 phase 1, 6: PLL_OUT, 7: PLL_OUT inversion, 8: Input clock, 9: Input clock inversion	0x04	0x04	0x04	0x04	0x06	0x06
	0x13	CLK_DAC_INV	[0]	: DAV clock inversion 0: Bypass, 1: Inversion	0x00	0x00	0x00	0x00	0x00	0x00

Table 6. Bank1 Register

Address		Register name	Bits	Description	1080p30	1080p25	720p60	720p50	720p30	720p25
Ba	Addr									
BANK1	0x03	PATTERN_FORMAT	[7:0]	: Pattern format Pattern format setting	0x00	0x00	0x00	0x00	0x00	0x00
	0x04	PATTERN_EN	[0]	: Pattern enable 0: Disable, 1: Enable	0x00	0x00	0x00	0x00	0x00	0x00
		PATTERN_COLOR_FORMAT	[3]	: Pattern color format 0: NTSC type, 1: PAL type	0x00	0x00	0x00	0x00	0x00	0x00
		PATTERN_NO	[7:4]	: Pattern type select	0x00	0x00	0x00	0x00	0x00	0x00
	0x0E	REVERSE_BIT_Y	[0]	: Reverse bit Y	0x00	0x00	0x00	0x00	0x00	0x00
		REVERSE_BIT_C	[1]	: Reverse bit C	0x00	0x00	0x00	0x00	0x00	0x00
		SWAP_YC	[2]	: Swap Y/C	0x00	0x00	0x00	0x00	0x00	0x00

Table 7. Bank2 Register

Address		Register name	Bits	Description	1080p /30f	1080p /25f	720p /60f	720p 50/f	720p /30f	720p /25f
Ba	Addr									
BANK2	0x00	SUB_MODE	[1]	: Sub register block0 mode select 0: Auto, 1: Manual	0x00	0x00	0x00	0x00	0x00	0x00
			[2]	: Sub register block1 mode select 0: Auto, 1: Manual	0x00	0x00	0x00	0x00	0x00	0x00
			[6]	: Core register value applie 0: Stable, 1: Applied	0x00	0x00	0x00	0x00	0x00	0x00
			[7]	: Sampling register value applie 0: Stable, 1: Applied	0x00	0x00	0x00	0x00	0x00	0x00
	0x02	CORE_RST	[0]	: Core module reset 0: Normal operation, 1: Reset	0x00	0x00	0x00	0x00	0x00	0x00
	0x02	SAMPLING_RST	[1]	: Sampling module reset 0: Normal operation, 1: Reset	0x00	0x00	0x00	0x00	0x00	0x00
	0x04	PATTERN_EN	[0]	: Block0, Pattern enable 0: Disable, 1: Enable	0x00	0x00	0x00	0x00	0x00	0x00
	0x04	PATTERN_NO	[7:4]	: Block0, Pattern type select	0x05	0x05	0x05	0x05	0x05	0x05
	0x0C	SYNC_LEVEL	[7:0]	: Block0, Sync level value	0x04	0x04	0x04	0x04	0x04	0x04
	0x0D	BLANK_LEVEL	[7:0]	: Block0, Blank level value	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F
	0x0E	BLACK_LEVEL	[7:0]	: Block0, Black level value	0x00	0x00	0x00	0x00	0x00	0x00
	0x14	COLOR_MODE	[1:0]	: Block1, Color space conversion select 0: NTSC, 1: PAL/AHD, 3: Manual	0x01	0x01	0x01	0x01	0x01	0x01
	0x15	CSC_Y_VALUE[7:0]	[7:0]	: Block1, Color space conversion Y value at manual mode	0x00	0x00	0x00	0x00	0x00	0x00
	0x16	CSC_Y_VALUE[9:8]	[1:0]		0x00	0x00	0x00	0x00	0x00	0x00
	0x17	CSC_CB_VALUE[7:0]	[7:0]	: Block1, Color space conversion Cb value at manual mode	0x00	0x00	0x00	0x00	0x00	0x00
	0x18	CSC_CB_VALUE[9:8]	[1:0]		0x00	0x00	0x00	0x00	0x00	0x00
	0x19	CSC_CR_VALUE[7:0]	[7:0]	: Block1, Color space conversion Cr value at manual mode	0x00	0x00	0x00	0x00	0x00	0x00
	0x1A	CSC_CR_VALUE[9:8]	[1:0]		0x00	0x00	0x00	0x00	0x00	0x00
	0x1C	Y_SCALE	[7:0]	: Block0, Y scale value	0x80	0x80	0x80	0x80	0x80	0x80
	0x1D	CB_SCALE	[7:0]	: Block0, Cb scale value	0x80	0x80	0x80	0x80	0x80	0x80
	0x1E	CR_SCALE	[7:0]	: Block0, Cr scale value	0x80	0x80	0x80	0x80	0x80	0x80
	0x20	Y_FILTER_NO	[3:0]	: Block0, Y filter select	0x00	0x00	0x00	0x00	0x00	0x00
	0x20	C_FILTER_NO	[7:4]	: Block0, C filter select	0x08	0x08	0x08	0x08	0x08	0x08
	0x37	BURST_SCALE	[7:0]	: Block0, Burst scale value	0x80	0x80	0x80	0x80	0x80	0x80
	0x40	OUTPUT0_MODE	[3:0]	: Block1, Output select 0: No siganl, 1: Composite, 2: Component Y, 3: Modulated C, 4: Component Cb, 5: Component Cr,	0x01	0x01	0x01	0x01	0x01	0x01
	0x41	PEAK_LEVEL	[7:0]	: Block1, Peal level control	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	0x42	OUTPUT_SCALE	[7:0]	: Block0, Output scale value	0x80	0x80	0x80	0x80	0x80	0x80

5. Electrical characteristics

5.1 Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings.

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V_{VDD1DM}	0.5	-	1.32	V
1.8V Analog Power Supply Voltage	V_{VDD1AM}	0.5	-	1.95	V
3.3V Digital Power Supply Voltage	V_{VDD3DM}	0.5	-	3.6	V
3.3V Analog Power Supply Voltage	V_{VDD3AM}	0.5	-	3.6	V
Voltage for Digital pins	V_{DIO}	0.5	-	4.6	V
Voltage for Analog Inputs	V_{AIO}	0.5	-	1.95	V
Storage Temperature	T_S	-40	-	125	℃
Junction Temperature	T_J	-40	-	125	℃
Vapor phase soldering (15 Sec)	T_{VSOL}	-	-	220	℃

Note : This Device should be operated under recommended operating condition. Since, absolute maximum rating condition can either cause device reliability problem or damage the device sufficiently to cause immediate failure.

5.2 Recommended Operating Conditions

Table 9. Recommended Operating Conditions.

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V_{VDD1D}	1.08	1.2	1.32	V
1.8V Analog Power Supply Voltage	V_{VDD1A}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{VDD3D}	3.0	3.3	3.6	V
3.3V Analog Power Supply Voltage	V_{VDD3A}	3.0	3.3	3.6	V
Ambient operating temperature	V_A	0	-	70	℃

5.3 DC Electrical Characteristics

Table 10. DC Electrical Characteristics.

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Input High Voltage	V_{IH}	2	-	V_{DD3D}+0.3	V
Input Leakage Current	I_L	-	-	±1	uA
Input Capacitance (f = 1Mhz, V_{IN} = 2.4V)	C_{IN}	-	-	10	pF
Output Low Voltage (I_{OL} = 8.0mA)	V_{OL}	-	-	0.4	V
Output High Voltage (I_{OH} = 12mA)	V_{OH}	2.4	-	-	V
Tri-State Output Leakage Current	I_{OZ}	-	-	±1	uA
Output Capacitance	C_{OUT}	-	-	10	pF

5.4 AC Electrical Characteristics

Table 11. AC Electrical Characteristics.

Parameter	Symbol	Min	Typ	Max	Unit
(Power Supply Current)					
1.2V Digital Power Supply Current	I_{VDD1D}	-	TBD	-	mA
1.8V Analog Power Supply Current	I_{VDD1A}	-	TBD	-	mA
3.3V Digital Power Supply Current	I_{VDD3D}	-	TBD	-	mA
3.3V Analog Power Supply Current	I_{VDD3A}	-	TBD	-	mA
(Crystal Input)					
Nominal frequency		-	27.0	-	MHz
Duty cycle		45	-	55	%
(Oscillator Input, 27MHz)					
Nominal frequency			27.0		MHz
Duty cycle		45		55	%
(Oscillator Input, 74.25MHz)					
Nominal frequency			74.25		MHz
Duty cycle		45		55	%
(Reset Pin)					
RESET setup time	t_{SU}	1			us
RSTB pulse width low	t_{PWL_rstb}	1			us
RSTB release time (low to high)	t_{REL_rstb}	10			us
(Host Interface Pins)					
SCL frequency	f_{SCL}	-	-	6	XTALI
SCL minimum pulse width low	t_{PWL_SCL}	6	-	-	XTALI
SCL minimum pulse width high	t_{PWH_SCL}	4	-	-	XTALI
SCL to SDA setup time	t_{IS_SDA}	2	-	-	XTALI
SCL to SDA hold time	t_{IH_SDA}	2	-	-	XTALI
SCL to SDA delay time	t_{OD_SDA}	-	-	6	XTALI
SCL to SDA hold time	t_{OH_SDA}	3	-	-	XTALI

6. Simply Register Map

Address		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	R/W
BANK 0	0x00						SYSTEM_MODE			R/W
	0x01	MAIN_FORMAT								R/W
	0x02									
	0x03									
	0x04								PD_DAC	R/W
	0x05				PLL_C	PLL_RST		PLL_BYPASS	PD_PLL	R/W
	0x06	PLL_M								R/W
	0x07			PLL_OD		PLL_N				R/W
	0x08									
	0x09									
	0x0A									
	0x0B									
	0x0C									
	0x0D									
	0x0E									
	0x0F									
	0x10			ICLK_SEL	PLL_OUT_INV	DIV_SRC_SEL				R/W
	0x11	CLK_INPUT_IF_SEL				CLK_INPUT_SEL				R/W
	0x12	CLK_SAMPLING_SEL				CLK_VFC_SEL				R/W
	0x13								CLK_DAC_INV	R/W
	0x14									
	0x15									
	0x16									
	0x17									
	0x18									
	0x19									
	0x1A									
	0x1B									
	0x1C									
	0x1D									
	0x1E									
	0x1F									

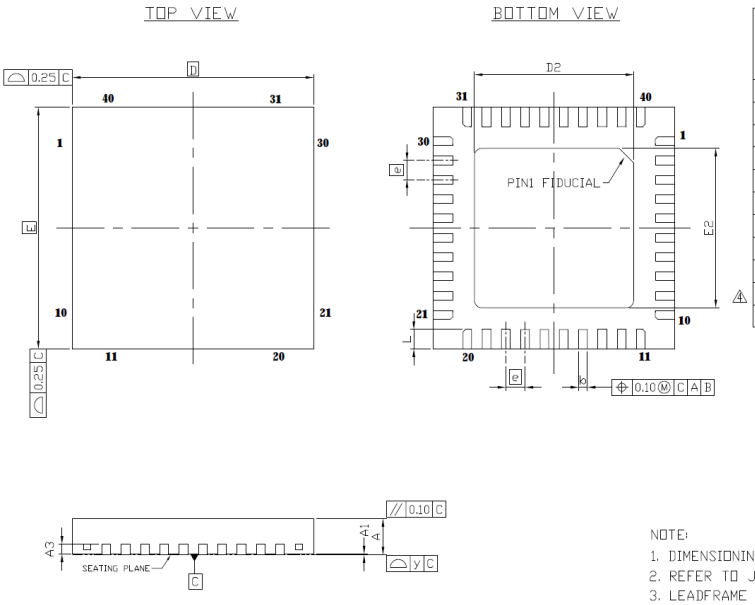
	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	R/W
BANK 1	0x00									
	0x01									
	0x02									
	0x03	PATTERN_FORMAT								R/W
	0x04	PATTERN_NO				C_FMT		PATTERN_EN		R/W
	0x05	Reserved								R/W
	0x06									
	0x07									
	0x08									
	0x09									
	0x0A									
	0x0B									
	0x0C									
	0x0D									
	0x0E						SWAP_YC	EVERSE_BIT_	EVERSE_BIT_	R/W
	0x0F	Reserved								
	0x10	Reserved								
	0x11									
	0x12	Reserved								R/W
	0x13									
	0x14									
	0x15									
	0x16									
	0x17									
	0x18									
	0x19									
	0x1A									
	0x1B									
	0x1C									
	0x1D									
	0x1E									
	0x1F									

	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	R/W
BANK 2	0x00	SUB_MODE								R/W
	0x01									R/W
	0x02							SAMPLING_RST	CORE_RST	R/W
	0x03									
	0x04	PATTERN_NO							PATTERN_EN	R/W
	0x05	Reserved								
	0x06	Reserved								
	0x07									
	0x08									
	0x09									
	0x0A									
	0x0B									
	0x0C	SYNC_LEVEL								R/W
	0x0D	BLANK_LEVEL								R/W
	0x0E	BLACK_LEVEL								R/W
	0x0F									
	0x10	Reserved								
	0x11	Reserved								
	0x12	Reserved								
	0x13	Reserved								
	0x14							COLOR_MODE		R/W
	0x15	CSC_Y_VALUE								R/W
	0x16							CSC_Y_VALUE		R/W
	0x17	CSC_CB_VALUE								R/W
	0x18							CSC_CB_VALUE		R/W
	0x19	CSC_CR_VALUE								R/W
	0x1A							CSC_CR_VALUE		R/W
	0x1B									
	0x1C	Y_SCALE								R/W
	0x1D	CB_SCALE								R/W
	0x1E	CR_SCALE								R/W
	0x1F									

	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	R/W
BANK 2	0x20	C_FILTER_NO					Y_FILTER_NO			R/W
	0x21	Reserved								
	0x22	Reserved								
	0x23	Reserved								
	0x24	Reserved								
	0x25	Reserved								
	0x26	Reserved								
	0x27	Reserved								
	0x28	Reserved								
	0x29	Reserved								
	0x2A	Reserved								
	0x2B	Reserved								
	0x2C	Reserved								
	0x2D	Reserved								
	0x2E	Reserved								
	0x2F	Reserved								
	0x30	Reserved								
	0x31	Reserved								
	0x32	Reserved								
	0x33	Reserved								
	0x34	Reserved								
	0x35									
	0x36	Reserved								
	0x37	BURST_SCALE								R/W
	0x38									
	0x39	Reserved								
	0x3A	Reserved								
	0x3B									
	0x3C	Reserved								
	0x3D	Reserved								
	0x3E	FSC_PHASE								R/W
	0x3F									

Address		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	R/W
BANK 2	0x40					OUTPUT0_MODE				R/W
	0x41	PEAK_LEVEL								R/W
	0x42	OUTPUT_SCALE								R/W
	0x43									
	0x44									
	0x45									
	0x46									
	0x47									
	0x48	Reserved								
	0x49	Reserved								
	0x4A	Reserved								
	0x4B	Reserved								
	0x4C	Reserved								
	0x4D	Reserved								
	0x4E	Reserved								
	0x4F	Reserved								
	0x50	Reserved								
	0x51	Reserved								
	0x52	Reserved								
	0x53	Reserved								
	0x54	Reserved								
	0x55	Reserved								
	0x56	Reserved								
	0x57	Reserved								
	0x58	Reserved								
	0x59	Reserved								
	0x5A	Reserved								
	0x5B									
	0x5C	Reserved								
	0x5D	Reserved								
	0x5E	Reserved								
	0x5F	Reserved								

7. Package Information



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	32
A1	0	0.02	0.05	0	0.8	2.0
A3		0.203 REF			8 REF	
b	0.15	0.20	0.25	6	8	10
D	4.90	5.00	5.10	193	197	201
D2	3.20	3.30	3.40	126	130	134
E	4.90	5.00	5.10	193	197	201
E2	3.20	3.30	3.40	126	130	134
e		0.40 BSC			16 BSC	
L	0.35	0.40	0.45	14	16	18
y			0.08			3

NOTE:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD. MO-220 WHHE-1
3. LEADFRAME MATERIAL IS OLIN194 AND THICKNESS IS 0.203mm (8 MIL)

Figure 13. NVP6021 Package Dimensions