

NVP6124

4-CH AHD2.0 RX and 9-CH Audio Codec

雅仪科技——【嵌入式智能互联设备】软硬件方案供应商。
专注【远程网络视频监控系统】研发设计。更多资讯浏览：
<http://www.travellinux.com> 获取。



Information contained here is subject to change without notice.
Make sure to check and use an updated version of the Data sheet.

www.nextchip.com

2015.02.11

REV 0.2



 **Revision History**

VERSION	DATE	DESCRIPTION	NOTE
Preliminary	2014-11-19	- Initial Draft	
V0.1	2014-11-27	- Pin MAP Information Modification (1~15 Pins)	6~8
V0.2	2015-02-11	- Pin MAP Information Modification (47, 48Pins) 47Pin (XTALI => SYS_CLK) 48Pin (XTALO => NC)	6~8

 **Contact Information**

Homepage : www.nextchip.com

E-mail : sales@nextchip.com

Phone : +82-2-3460-4700

NEXTCHIP Confidential

4-CH AHD2.0 RX and 9 CH-Audio Codec

NVP6124 include 4-Channels AHD2.0 RX and 9-Channels Audio Codec. It is sure that compatible with AHD1.0. The 4-Channels AHD2.0 RX delivers high quality images. It accepts separate 4 CVBS/COMET/AHD1.0/AHD2.0 inputs from Camera and the other video signal sources. It digitizes and decodes NTSC/PAL/COMET/AHD1.0/AHD2.0 video signal into digital video components which represents 8-bit BT.656/1120(like) 4:2:2 byte interleave format with 27/36/37.125/54/72/74.25 /108/144/148.5MHz multiplexed. The **NVP6124** includes Clock PLL, so 27/36/37.125/54/72/74.25 /108/144/148.5MHz byte-interleave function available. Especially, It is able to use same transmission cable with conventional one for COMET(SD level), AHD1.0 (HD level) and AHD 2.0 (Full HD level), and they provide the superior image quality by minimizing the interference when separating Y and C.

The 9-Channels Audio Codec is 8-Channels Voice/1-Channel Mic PCM Codec which handles voice band signals(300Hz~3400Hz) with 8bit/16bit linear PCM, 8bit G.711(u-law, a-law) PCM. Built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

The 4-Channels Coaxial Communication Protocol communicates between controller(DVR) and camera on the video signal through coaxial cable. It was includes Tx for transfer especially signals thought coaxial cable and Rx for receives especially signals to keep informed a user by control registers.

Features

■ AHD2.0 4CH RX

- **AHD2.0 RX which accepts 4-CVBS/COMET/720P@25p/30p(AHD1.0)/
720P@50p/60p(AHD2.0)/
1080P@25p/30p(AHD2.0)**
- Output in BT.656/1120(like) 4:2:2 byte interleave format with
27/36/37.125/54/72/74.25/108/144/148.5MHz
- Support 4*Video Output Port, Each Port Video Output Format Selectable
- Support Video Standard Auto-Detection for Each a Channel by Status
- On Chip Analog CLAMP, Anti-aliasing Filter and Equalizer Filter
- Accepts NTSC-M/J/4.43, PAL-B/D/G/H/I/K/L/M/N/60, COMET,
720P @25p/30p/50p/60p, 1080P@25p/30p
- Robust Sync detection for weak and unstable signals
- High-performance adaptive comb filter and Notch Filter
- Programmable H/V Peaking filter for Luminance
- CTI (Chrominance Transient Improvement)
- Color compensation for PAL
- IF compensation filter
- Robust No-video detection
- Programmable Brightness, Contrast, Saturation and Hue
- Programmable Picture Quality Control
- Programmable Gamma Correction

■ Audio Codec

- 8-Ch Audio / 1-Ch Mic Record, 1-Ch Playback
- 10bit pipe-line ADC / 1*DAC
- Input Analog PGA Control and control Gain digitally
- Linear PCM (8bit/16bit, 8K/16K/32K/44.1K)
- G.711 a-law/u-law (8bits, 8K/16K/32K/44.1K)
- Input Mixing, Digital Volume, Mute Detection
- SSP/DSP/I2S Interface (Master/Slave mode)
- Cascade mode (up to 2 cascade support)
 - 16-channels recording (with 2-channels MIC recording), mixing output, playback

■ MISC

- Built in Clock PLL
- Single 27M OSC for 720H/960H/COMET/AHD1.0/AHD2.0 all video standards
- Built in 4-Ch Motion/Black/White Detector(32x24)
- Support Coaxial Protocols for supported all video standard
- Support Each Channel MPP Pin and IRQ Pin
- Support 4 Video Output Clocks with controlled bi-directional
- Support I2C serial Interface
- 1.2V / 3.3V Supply Voltage
- 128 eTQFP, 14x14, 0.4p

■ Application

- Video Security System

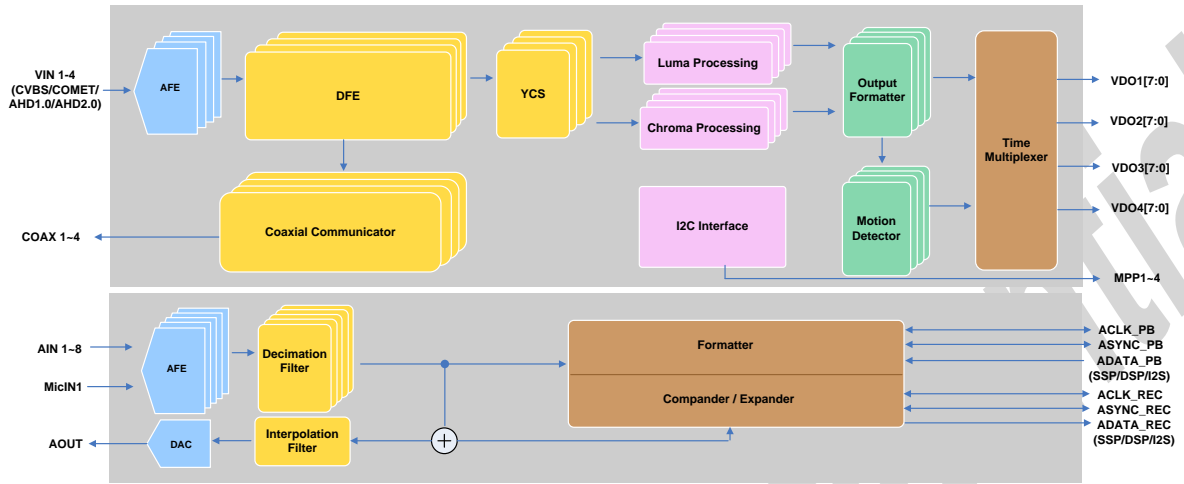
■ Ordering Information

Device	Package	Temperature Range
NVP6124	128eTQFP	0 ~ 70℃

■ Related Products

- HI3520D/HI3521/HI3531
- GM8283/GM8287/GM8210
- VC0736/VC0738

Functional Block Diagram



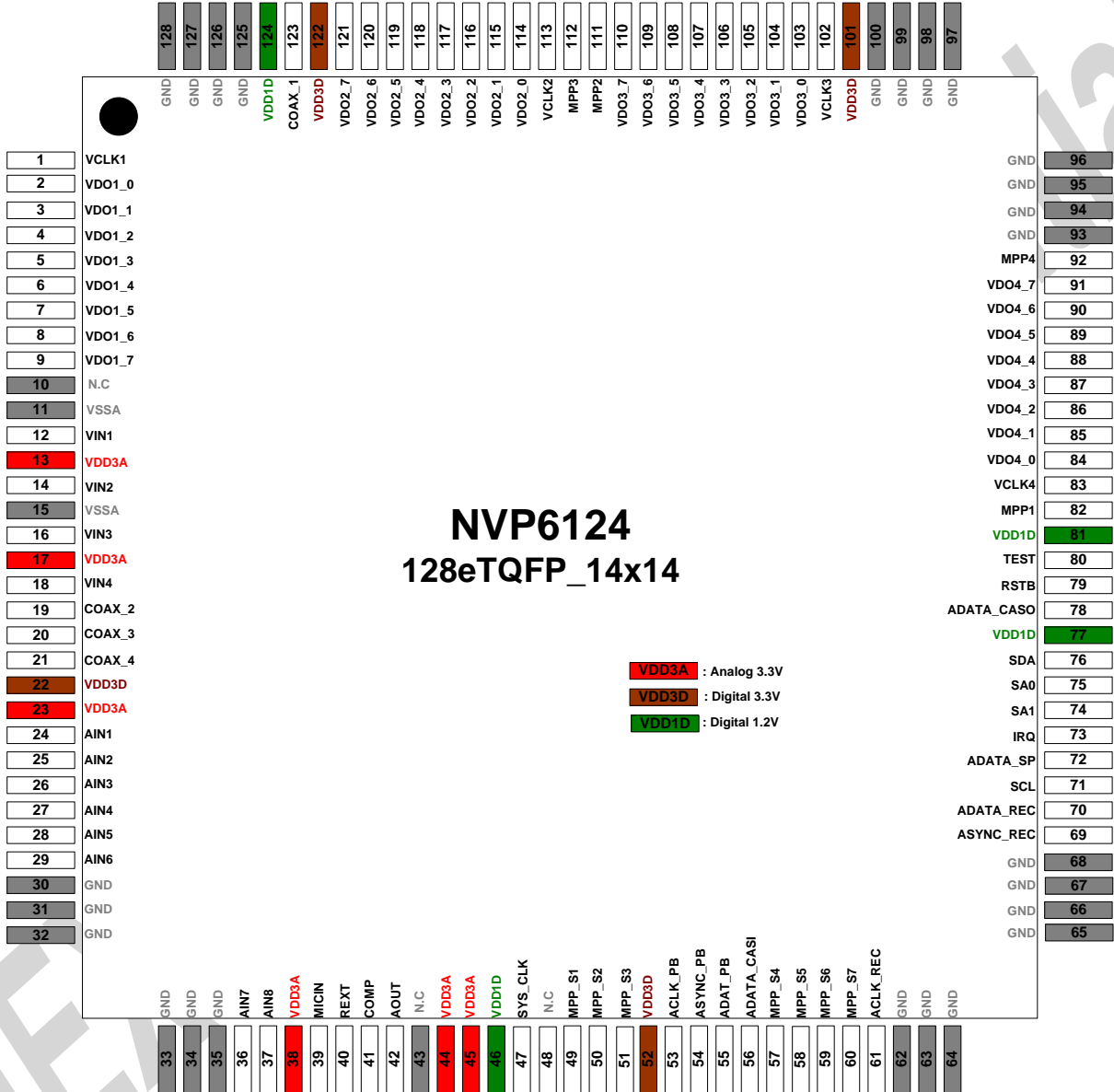
Contents

1. Pin Information	6
1.1 Pin Assignments	6
1.2 Pin Description.....	7
2. AHD1.0 RX	9
2.1. Functional Overview	9
2.2. Video Input Formats.....	10
2.3. Analog Front End (CLAMP, PGA, Anti-aliasing Filter).....	10
2.4. Genlock (Robust Sync Detection, Robust No-Video Detection)	11
2.5. YCS (Y/C separation)	12
2.6. Luma Processing	13
2.7. Chroma Processing	14
2.8. Data Output Order & Direction Control.....	15
2.9. Output Format.....	16
2.9.1. ITU-R BT.656/1120(like) Format	19
2.9.2. Video Output Timing Information	19
2.10. Output Mode	19
2.10.1. Single Output Mode.....	19
2.10.2. 2-Multiplex Output Mode	20
2.10.3. 4-Multiplex Output Mode	21
2.10.4. 148.5MHz 2-Ch CIF Data Output Mode.....	24
2.11. Video Frame Control	25
2.12. Motion Detector	25
3. Audio Codec	26
3.1. Description.....	27
3.2. Record Output	27
3.2.1 Data Output Interface	28
3.2.2. 2/4/8/16-Channel Data Output(256 fs).....	30
3.2.3. 2/4/8/16-Channel Audio Data Output with 4-Channel Mic Data(320 fs).....	31
3.2.4. ADATA_SP Output.....	32
3.3. Playback Output	33
3.4. Audio Detection.....	33
3.5. Cascade Operation.....	34
4. Coaxial Protocol	35
5. I2C Interface	37
6. Register Description	38

7. Electrical characteristics	120
7.1. Absolute Maximum Ratings.....	120
7.2. Recommended Operating Condition	120
7.3. DC Characteristics.....	120
7.4. AC Characteristics	121
8. System Applications	122
8.1. 4-Channel, Master Mode	122
8.1.1. Block Diagram (4 Channel, Master Mode).....	122
8.1.2. Block Diagram (4 Channel, Slave Mode).....	122
8.2. 8-Channel, Master Mode	123
8.2.1. Block Diagram (8 Channel, Master Mode).....	123
8.2.2. Block Diagram (8 Channel, Slave Mode).....	123
8.3. 16-Channel, Master Mode.....	124
8.3.1. Block Diagram (16 Channel, Master Mode).....	124
8.3.2. Block Diagram (16 Channel, Slave Mode).....	124
9. Package Information	125

1. Pin Information

1.1 Pin Assignments



1.2 Pin Description

Name	Pin number	Type	Descriptions
System Clock / Reset			
RSTB	79	DI	System Reset (Active low)
SYS_CLK	47	DI	OSC Input (27MHz)
Analog Video Input Interface			
VIN1, VIN2, VIN3, VIN4	12, 14, 16, 18	AI	Analog Video Input (1 ~ 4 Respectively)
Analog Audio Input/output Interface			
AIN1, AIN2, AIN3, AIN4 AIN5, AIN6, AIN7, AIN8	24, 25, 26, 27, 28, 29, 36, 37	AI	Analog Audio Input (1 ~ 8 Respectively)
MICIN	39	AI	Mic Input
AOUT	42	AO	Analog Audio Output
COMP	41	A	Audio DAC Compensation pin.
REXT	40	A	Audio DAC external resistor pin
Digital Video Interface			
VDO1[7:0]	9, 8, 7, 6, 5, 4, 3, 2	O	Video Port 1 Output
VDO2[7:0]	121, 120, 119, 118, 117, 116, 115, 114	O	Video Port 2 Output
VDO3[7:0]	110, 109, 108, 107, 106, 105, 104, 103	O	Video Port 3 Output
VDO4[7:0]	91, 90, 89, 88, 87, 86, 85, 84	O	Video Port 4 Output
VCLK1,VCLK2, VCLK3,VCLK4	1, 113, 102, 83	O	Video Clock Output (1 ~ 4 Respectively)
ETC			
TEST	80	I	Chip Test Pin (Connect to Ground)
IRQ	73	O	Interrupt Request Output
MPP1,MPP2,MPP3,MPP4	82, 111, 112, 92	O	Multi-Purpose Pin Output1
COAX_1, COAX_2, COAX_3, COAX_4	123, 19, 20, 21	O	Coaxial Communication Signal Output
MPP_S1, MPP_S2, MPP_S3, MPP_S4, MPP_S5, MPP_S6, MPP_S7	49, 50, 51, 57, 58, 59, 60	O	Multi-Purpose Pin Output2

Digital Audio Interface				
ACLK_REC	61	B	Clock for Record (M:output, S:Input)	
ASYNCR_REC	69	B	Sync for Record(M:output, S:Input)	
ADATA_REC	70	O	Audio Digital Data for Record	
ADATA_SP	72	O	Audio Digital Data for Speaker	
ADATA_CASO	78	O	Audio Digital Data for Cascade Output	
ADATA_CASI	56	I	Audio Digital Data for Cascade Input	
ACLK_PB	53	B	Clock for Playback (M:output, S:Input)	
ASYNCR_PB	54	B	Sync for Playback (M:output, S:Input)	
ADATA_PB	55	I	Audio Digital Data for Playback	
I2C Interface				
SDA	76	B	I2C Interface R/W Data (3.3V tolerant)	
SCL	71	I	I2C Interface Clock (3.3V tolerant)	
SA1, SA0	74, 75	I	Slave Address	
Power				
VDD1D	46, 77, 81, 124	P	Digital Power (Digital 1.2V)	
VDD3D	22, 52, 101, 122	P	Digital Power (Digital 3.3V)	
VDD3A	13, 17, 23, 38, 44, 45,	P	Analog Power (Analog 3.3V)	
Ground				
NC	10, 43, 48	G	No Connect Pin (Connect to GND)	
VSSA	11 15		Analog Ground	
GND	30 31 32 33, 34 35, 62 63, 64, 65, 66, 67, 68, 93, 94, 95, 96, 97, 98, 99, 100, 125, 126, 127, 128		Ground	

2. AHD2.0 RX

NVP6124 is 4 Channels AHD2.0 RX and delivers high quality images. It accepts separates 4 CVBS/COMET/AHD1.0/AHD2.0 inputs from Camera and the other video signal sources.

It digitizes and decodes NTSC/PAL/COMET/AHD1.0/AHD2.0 video formats into digital components video which represents 8-bit ITU-R BT.656/1120(like) 4:2:2 format with 27/36/37.125MHz, 54/72/74.25MHz and 108/144/148.5MHz multiplexed. 54/72/74.25/108/144/148.5MHz multiplexed function will be available, because It built in Clock PLL.

NVP6124 includes 4 Channels analog processing circuit that comprise anti-aliasing filter, ADC, CLAMP, Equalizer filter. It shows the best picture quality adopted by high performance adaptive comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness and Contrast and several function such as CTI, Programmable peaking filter, various compensation filters.

2.1. Functional Overview

The AHD2.0 RX separates luminance and chrominance signals from CVBS/COMET/AHD1.0 /AHD2.0. Figure 2.1 show the block diagram of the **NVP6124** Video processing.

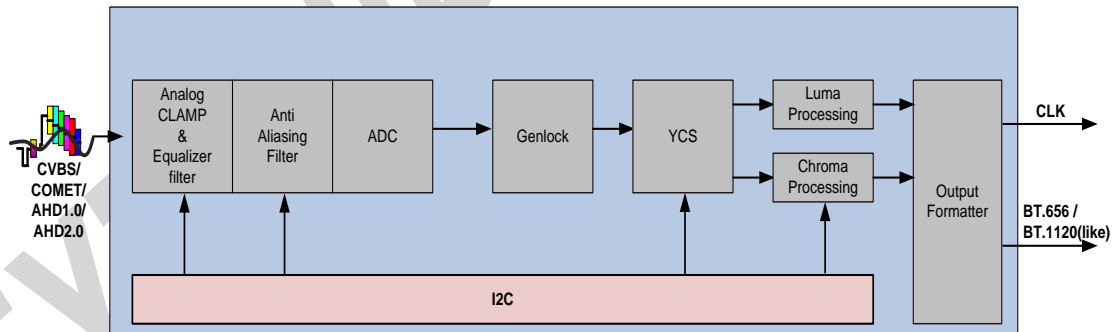


Figure 2.1. AHD2.0 RX Video Processing of NVP6124

The First step to decode CVBS/COMET/AHD1.0/AHD2.0 is to digitize the entire video signal using an A/D converter (ADC). Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic. The video signal also is low-pass filtered in Anti aliasing Filter to remove any high-frequency components that may result in aliasing.

Vertical sync and horizontal sync information are recovered in Genlock block. When composite video signal is decoded, the luminance and chrominance are separated by YCS(Y/C Separator). The quality of decoded image is strongly dependent on the signal quality of separated Y and C.

To achieve best quality of image, Adaptive Comb Filter is used.

The color demodulator in chroma processing block accepts modulated chrominance data from Adaptive Comb Filter which generate Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sin and cos subcarrier data.

2.2. Video Input Formats

NVP6124 supports NTSC/PAL/COMET/AHD1.0/AHD2.0 as all of the Video Formats. Table 2.1 show various Video Formats and Register Setting Value (VIDEO_FORMAT, 0x08~0B[4:0], Bank0 / AHD_MD, 0x81~84[3:0], Bank0) to support them.

Table 2.1. NVP6124 Input Video Image Formats

AHD_MD (Bank0, 0x81~84[3:0])	VIDEO_FORMAT (Bank0, 0x08~0B[4:0])	FORMAT	H x V	HZ	Fsc(MHz)
0x0 0x1	0x00	NTSC-M,J	720x240 960x240	59.94	3.579545
	0x11	NTSC-4.43	720x240 960x240	59.94	4.43361875
	0x1D	PAL-B,D,G,H,I	720x288 960x288	50	4.43361875
	0x16	PAL-M	720x240 960x240	59.94	3.57561149
	0x1F	PAL-Nc	720x288 960x288	50	3.58205625
	0x15	PAL-60	720x240 960x240	60	4.433619
0x2	Don't care	P1080	1920x1080	30	Flexible
0x3	Don't care	P1080	1920x1080	25	Flexible
0x4	Don't care	P720	1280x720	60	Flexible
0x5	Don't care	P720	1280x720	50	Flexible
0x6	Don't care	P720	1280x720	30	Flexible
0x7	Don't care	P720	1280x720	25	Flexible

2.3. Analog Front End (CLAMP, PGA, Anti-aliasing Filter)

NVP6124 includes 4 Channel Analog Processing circuit that comprise anti-aliasing filter, ADC, PGA and CLAMP. Because its design is dedicated for video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for **NVP6124**. Figure 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by Register and include bypass mode that don't have AFE filtering.

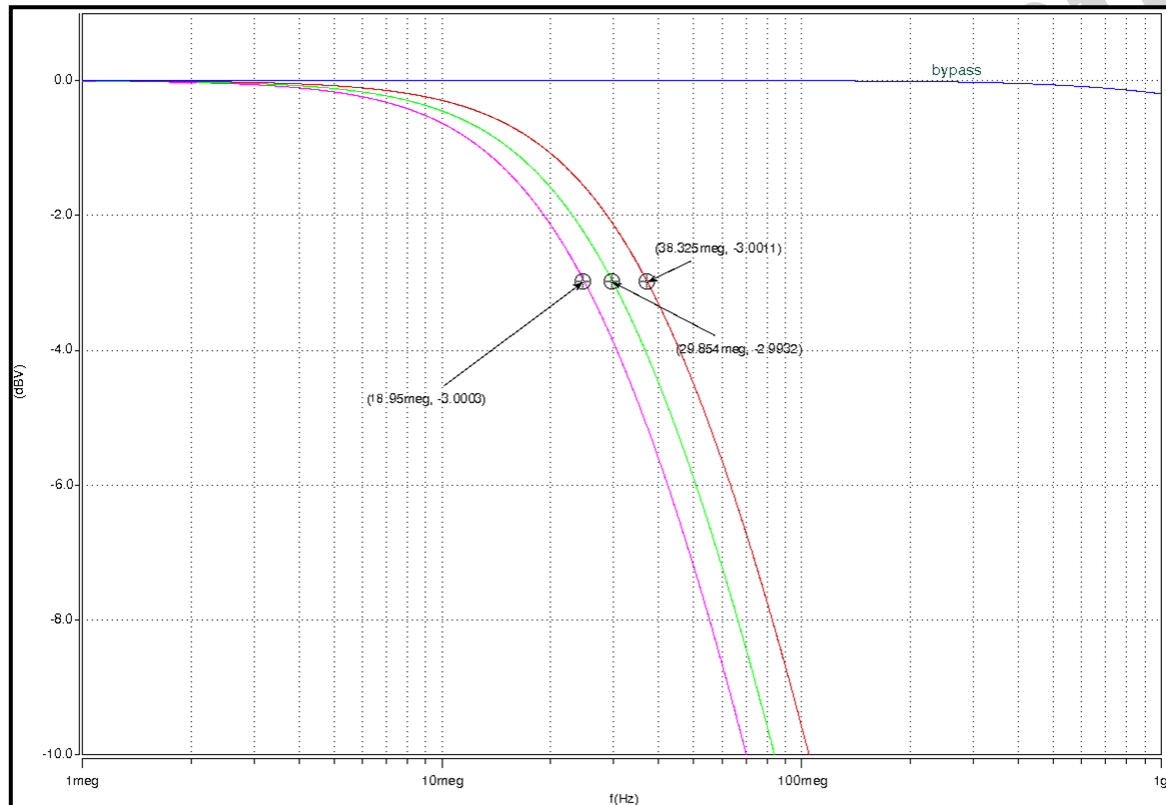


Figure 2.2. Anti-aliasing Filter characteristic

2.4. Genlock (Robust Sync Detection, Robust No-Video Detection)

NVP6124 provides a fully digital Genlocking circuitry. The digital Genlocking Circuitry use the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier.

NVP6124 uses the proprietary Genlock mechanism for video application system. It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

2.5. YCS (Y/C Separator)

The YCS is used to separate Y and C signal from CVBS/COMET/AHD1.0/AHD2.0 standard video signal. Therefore, The output image is sharper and clearer compared to other device. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows partial Characteristic of BSF. According to Input signal format, BSF characteristic can be selected.

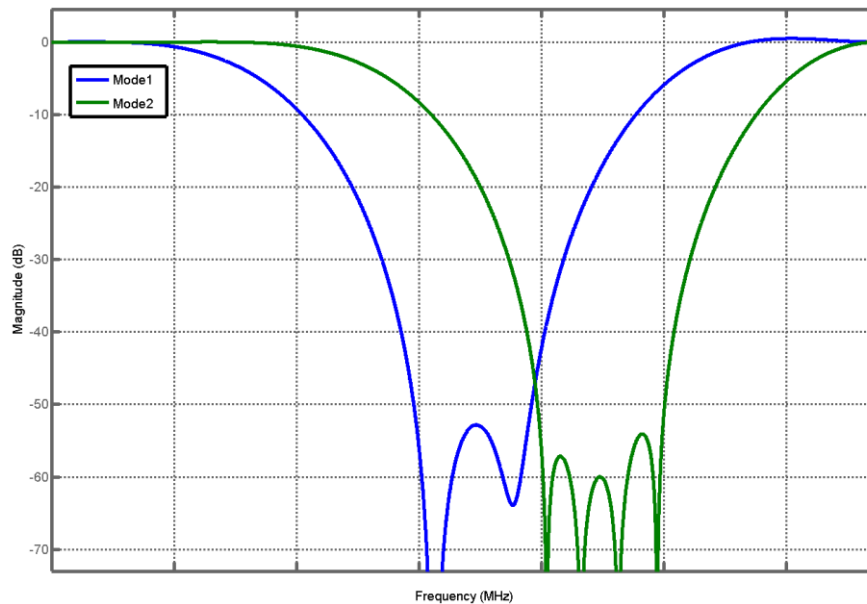


Figure 2.3. Band Split Filter Characteristic

NVP6124 can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the **NVP6124**, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.6. Luma Processing

The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

Figure 2.4. shows Peaking Filter Characteristic. **NVP6124** provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The Peaking filter is applied to this purpose and its characteristics can be controlled by register (Y_PEAK_MODE, 0x18[7:4] / 0x19[7:4] / 0x1A[7:4] / 0x1B[7:4], Bank0) via I2C interface.

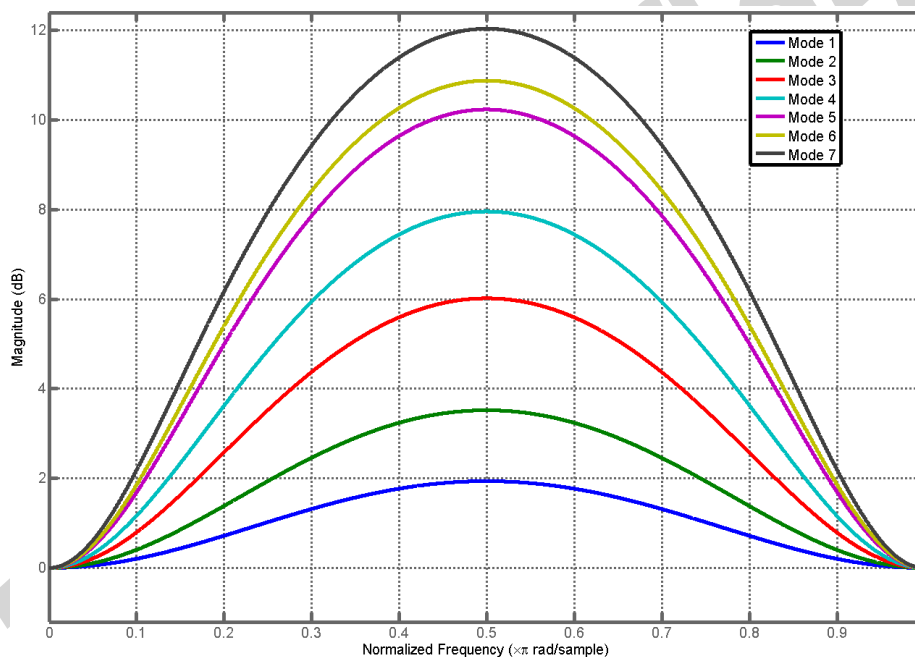


Figure 2.4. Peaking Filter Characteristic

2.7. Chroma Processing

The Chroma Processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The Chroma Demodulator receives modulated chroma from Y/C separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6.

Users can select the chroma filter through I2C interface (CLPF_SEL, 0x21/25/29/2D[3:0], Bank0).

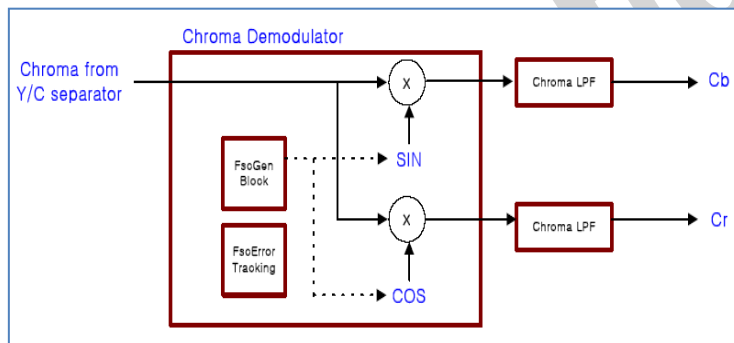


Figure 2.5. Chroma Process

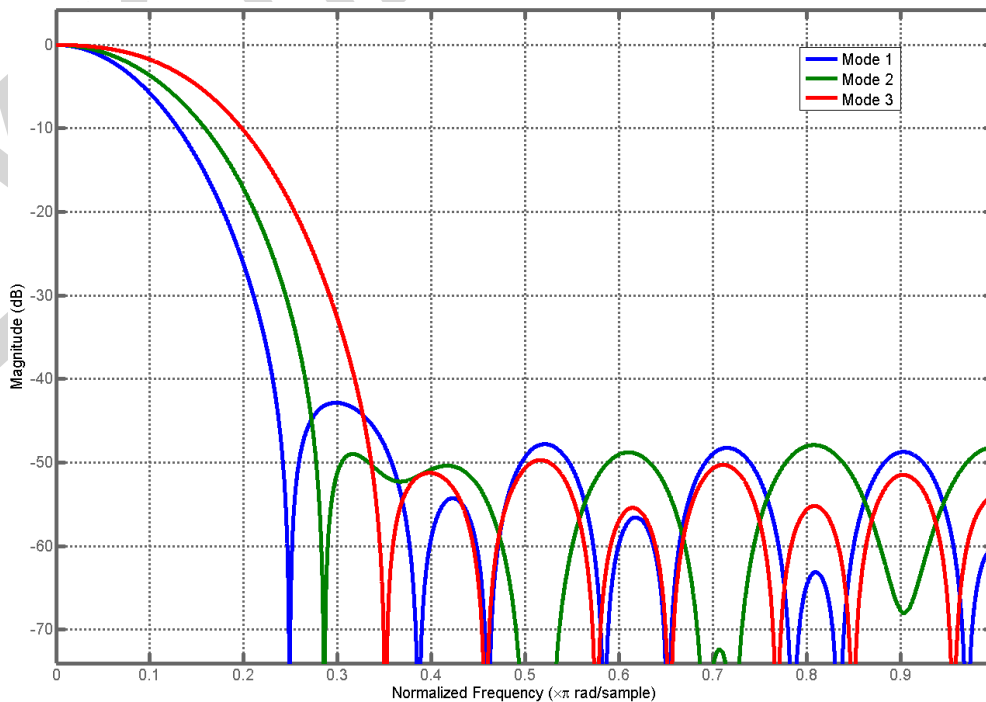


Figure 2.6. Chroma Low Pass filter Characteristic

2.8. Data Output Order & Direction Control

NVP6124 can change the order of the output pin in the All Output Mode as shown in Table 2.2. (OUT_DATA_INV, 0xD2[5:2] Bank1) Furthermore, as Clock and Data pins control direction so may it does nothing with interconnected back-end device and how control related control register as shown in Table 2.3. (VCLK_x_EN, 0xCA[7:5] Bank1 / VDO_x_EN, 0xCA[3:1] Bank1)

Table 2.2. Data Output Pin Order Control

Address (Bank1)	state	Data Output of Port X
0xD2, OUT_DATA_INV[5]	0	VDO4[7:0]
	1	VDO4[0:7]
0xD2, OUT_DATA_INV[4]	0	VDO3[7:0]
	1	VDO3[0:7]
0xD2, OUT_DATA_INV[3]	0	VDO2 [7:0]
	1	VDO2 [0:7]
0xD2, OUT_DATA_INV[2]	0	VDO1 [7:0]
	1	VDO1 [0:7]

Table 2.3. Output Clock and Data Direction Control

Address (Bank1)	state	Data Output of Port X
0xCA[4], VCLK_1_EN 0xCA[0], VDO_1_EN	0	High'z
	1	Output Enable
0xCA[5], VCLK_2_EN 0xCA[1], VDO_2_EN	0	High'z
	1	Output Enable
0xCA[6], VCLK_3_EN 0xCA[2], VDO_3_EN	0	High'z
	1	Output Enable
0xCA[7], VCLK_4_EN 0xCA[3], VDO_4_EN	0	High'z
	1	Output Enable

2.9. Output Format

NVP6124 supports a format of standard ITU-R BT.656/1120(like) Ports of 4 is synchronized by each output clock(VCLK1~VCLK4). Phase of clock is controlled by VCLK_SEL(BANK1, 0xCC~0xCF[6:4]) and VCLK_DLY_SEL(BANK1, 0xCC~0xCF[3:0]).

2.9.1. ITU-R BT.656/1120(like) Format

Codes of SAV and EAV are injected into data stream of ITU-R BT.656/1120(like) to indicate a start and a end of active. Note that a number of pixel for 1H active line is always constant regardless of the actual incoming line length. Therefore, variance of analog input signal is applied to a blank section except codes of EAV and SAV. Figure 2.7 shows data stream of ITU-R BT.656/1120(like) format. If length of 1H of analog input signal increase or decrease, number of pixel of 'A' increase or decrease.

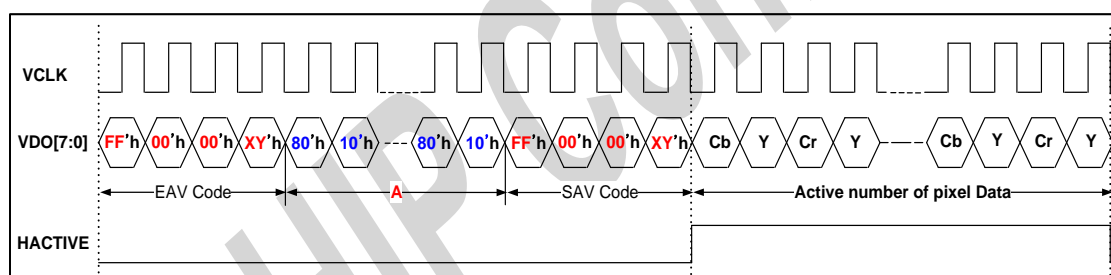


Figure 2.7. Region of active is constant

2.9.2. Video Output Timing Information

The AHD2.0 output timing like with SD resolution. But some synchronous signals difference with SD resolution as Field information that does not separated EVEN/ODD field. There is next sentence shown timing diagram point of video output.

2.9.2.1 720P@ 30P/25P, 60P/50P H/V Timing

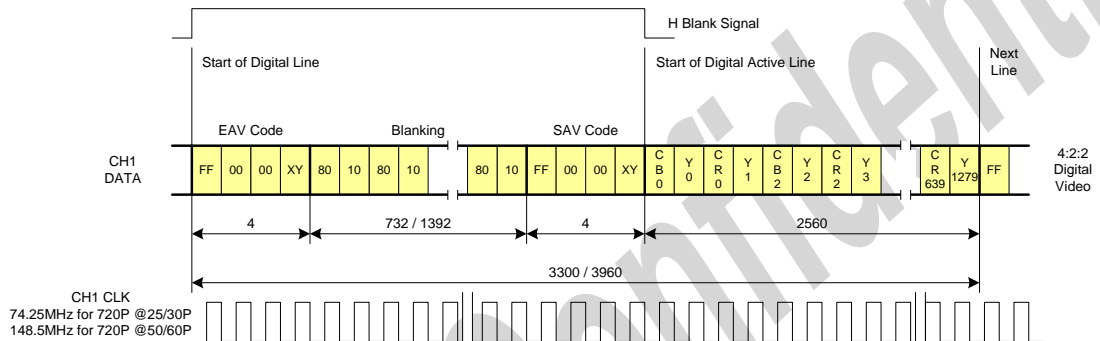


Figure 2.8. 720P@30P/25P, 60P/50P Horizontal Timing Diagram

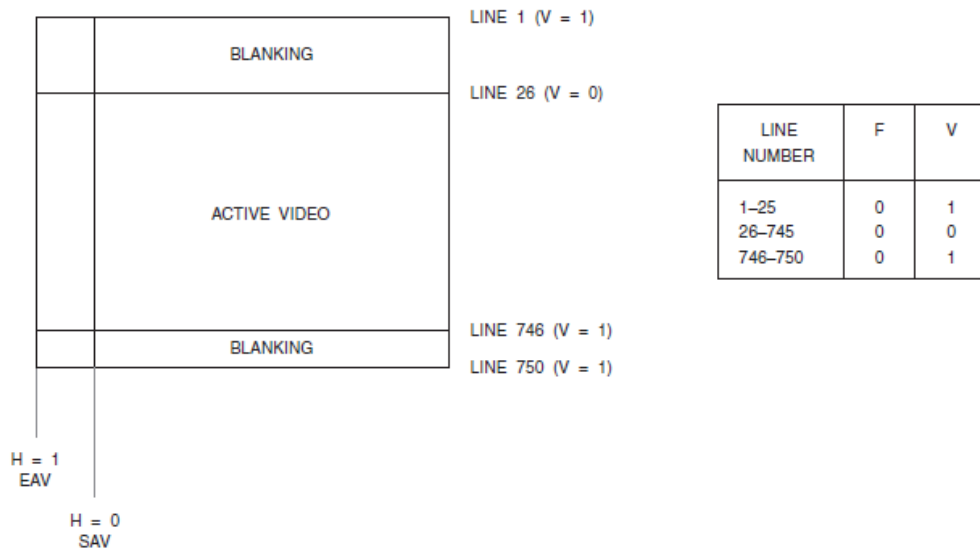


Figure 2.9. 720P@30P/25P, 60P/50P Vertical Timing Diagram

2.9.2.2 1080P@30P, 25P H/V Timing

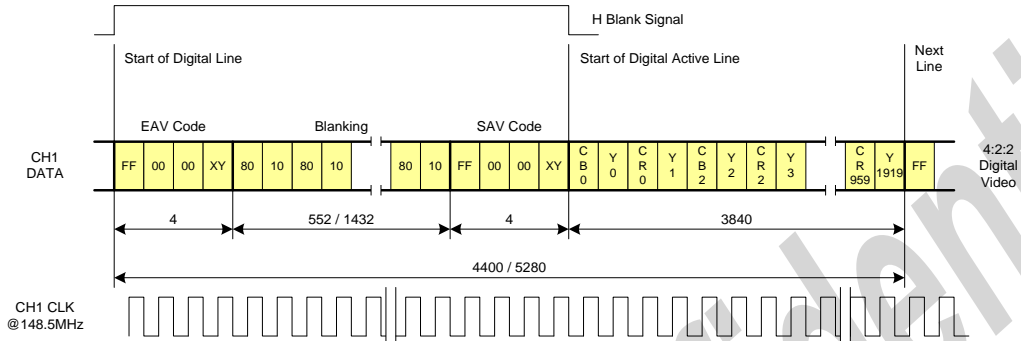


Figure 2.10. 1080P@30P,25P Horizontal Timing Diagram

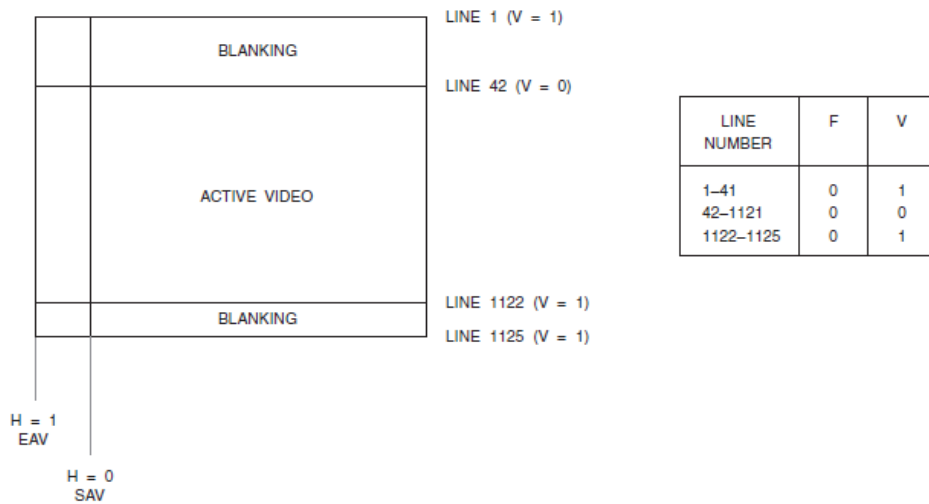


Figure 2.11. 1080P@30P,25P Vertical Timing Diagram

2.10. Output Mode

The NVP6124 output to the back-end devices whether transferring a channel by a port or 2/4-channels multiplexed output by a port. It is that as much as possible multiplexed channels by a port's output frequency same to sum of multiplexed video's frequency. The NVP6124 supports that output of 27/36/37.125/54/72/74.25/108/144/148.5MHz Data Rate.

2.10.1 Single Output Mode

Basically, a video channel output through a port. **NVP6124** output 4-clocks that VCLK1, VCLK2, VCLK3, VCLK4 and output 4-data that VDO1[7:0], VDO2[7:0], VDO3[7:0], VDO4[7]. There is timing as shown in Figure 2.12. For VCLK1, VCLK2, VCLK3 and VCLK4 phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC~CF[6:4], Control of Output Clock)
- (VCLK_x_DLY_SEL, 0xCC~CF[3:0], Control of Phase in Output Clock)
- (CH_OUT_SELx, 0xC8, 0xC9, Control how many multiplexed channel in a port)

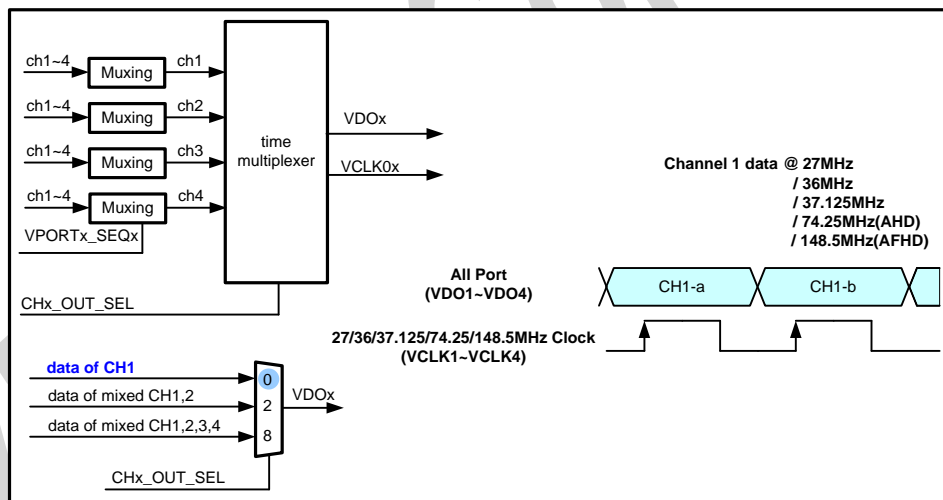


Figure 2.12. Block Diagram of Single-Channel Output

2.10.2 2-Multiplex Output Mode

In the 2-Multiplex Output Mode, **NVP6124** output multiplexed 2-channels video through in a port. Figure 2.13 shown as multiplexed with 2-channels video output to VDO1~VDO4. For VCLK1, VCLK2, VCLK3 and VCLK4 phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC~CF[6:4], Control of Output Clock)
- (VCLK_x_DLY_SEL, 0xCC~CF[3:0], Control of Phase in Output Clock)
- (CH_OUT_SELx, 0xC8, 0xC9, Control how many multiplexed channel in a port)

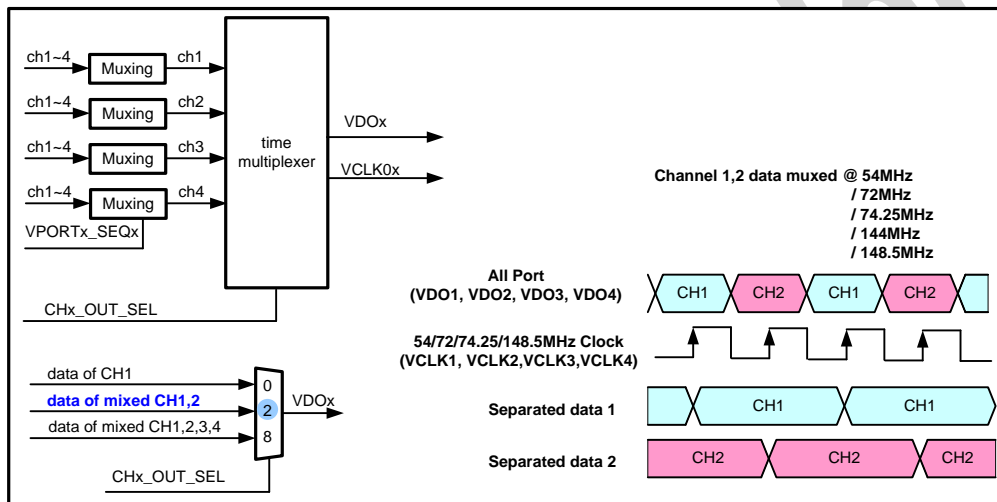


Figure 2.13. Block Diagram of Multiplexed 2-Channels Output

2.10.3 4-Multiplex Output Mode

In the 4-Multiplex Output Mode, NVP6124 output multiplexed 4-channels video through in a port. But is not multiplex AHD2.0 resolution due to same VCLK frequency with AHD2.0 sampling frequency. Figure2.14 shown as multiplexed with 4-channels video output to VDO1~VDO4. For VCLK1, VCLK2, VCLK3 and VCLK4 phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC~CF[6:4], Control of Output Clock)
- (VCLK_x_DLY_SEL, 0xCC~CF[3:0], Control of Phase in Output Clock)
- (CH_OUT_SELx, 0xC8, 0xC9, Control how many multiplexed channel in a port)

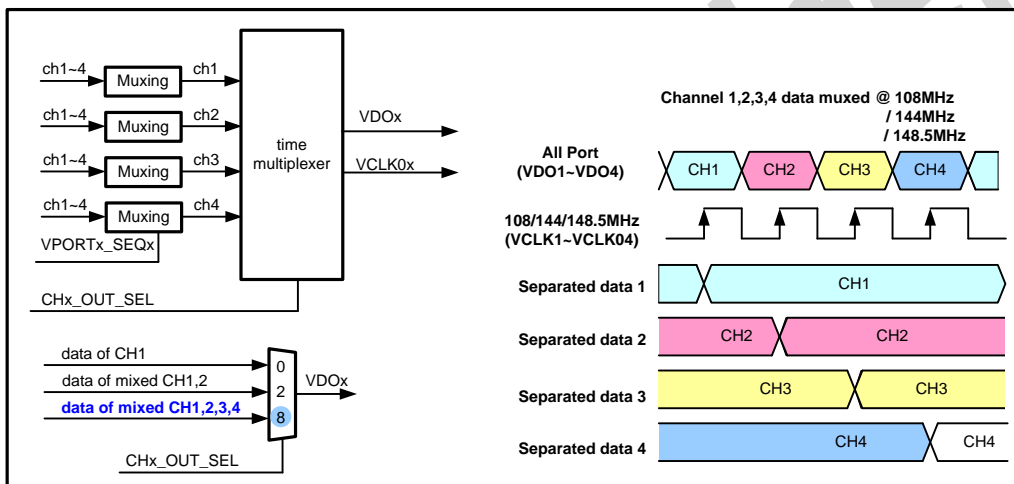


Figure 2.14. Block Diagram of Multiplexed 4-Channels Output

- Example of 148.5MHz(960H) D1 Data Output Mode with Channel ID
 1. In case of VDO1 output port and VCLK1 output clock use.
 2. Set VDO1 output(CH_OUT_SEL1,BANK1,0xC8[3:0] = 0x8) and VCLK1 output (VCLK1_SEL, BANK1,0xCC[6:4] = 0x6 or 0x7) .
 3. Set Channel ID Type (Refer to CHID_TYPE(Bank0, 0x54[2:0]) Register Description)
 4. And then NVP6124 generate 148.5MHz(960H) clock and data output (Figure 2.15)

If you want to confirm the 148.5MHz Data using FPGA or Other device, Execute 5~11 item in next page.

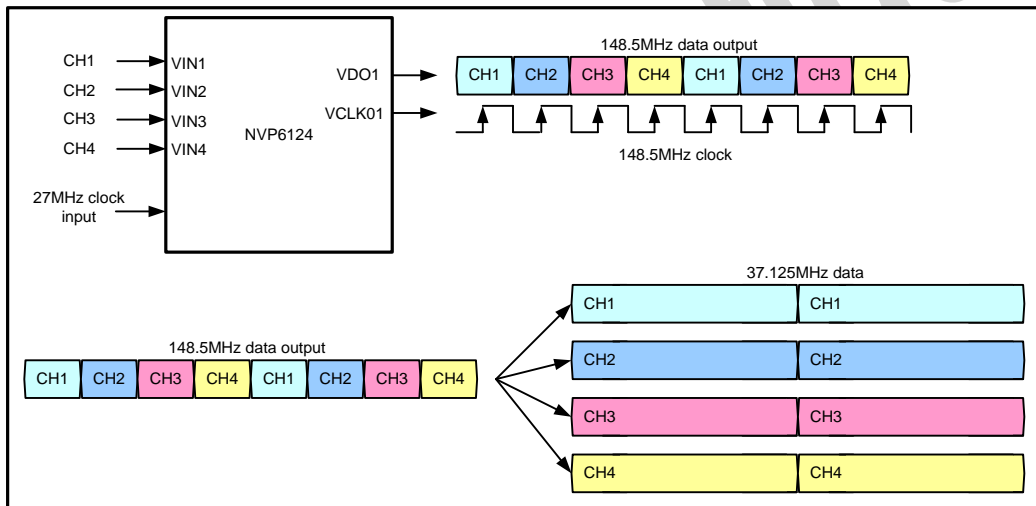


Figure 2.15. NVP6124 generate 148.5MHz(960H) clock and data output

5. FPGA or equivalent devices which is input 148.5MHz time multiplexed data output, need to align with same channel data(37.125MHz 1,2,3,4 channel). Figure2.16. shows how to use Channel ID as a example.

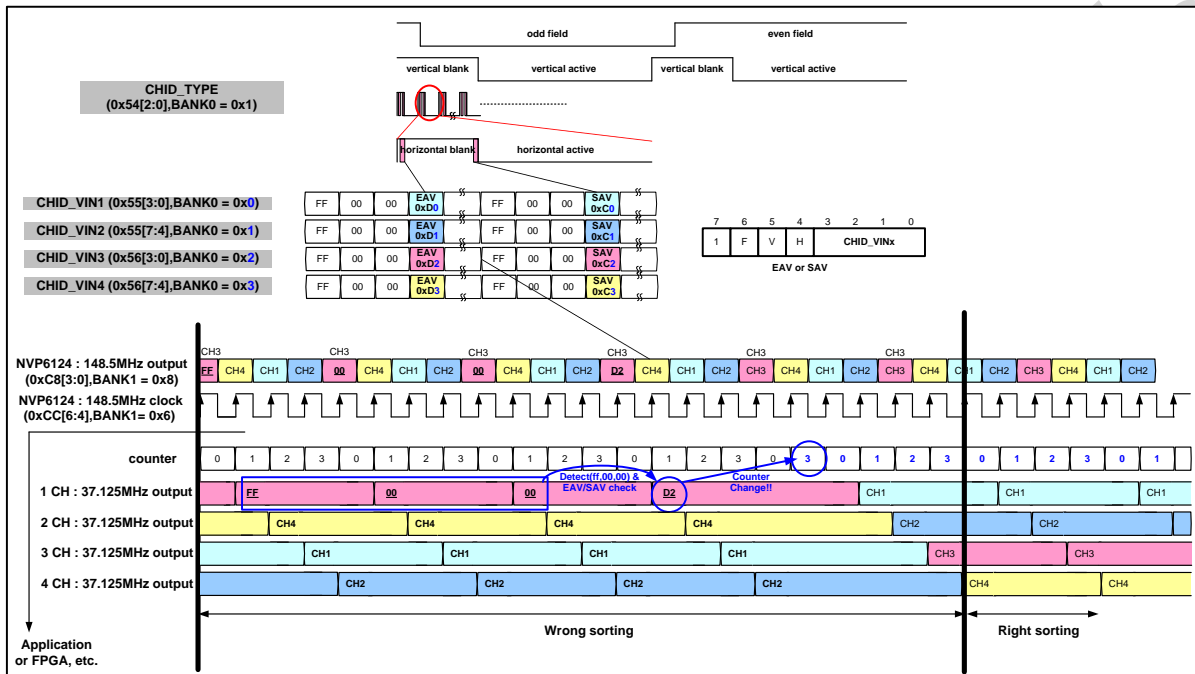


Figure 2.16. NVP6124 Select Channel ID

6. CHID_TYPE(BANK0, 0x54[2:0]=001) mode described in top of Figure2.16.
7. To generate 2bit digit, Design 2bit counter with VCLK1 (The 2bit digit means each channel).
8. Using 2bit digit, Convert from 148.5MHz Data to 37.125MHz Data (Wrong sorting part in Figure2.16.) and then Define the 2bit digit (0 : 1ch data, 1 : 2ch data, 2 : 3ch data, 3 : 4ch data). namely, 148.5MHz data output separate only with 37.125MHz, 4channel data, is not align with channel data where becomes mapping in counter value.
9. For mapping between separated each channel data and specified counter value, Select channel among separated each channel(1CH selected in Figure2.16.). If selected channel data become Right sorting condition, other 3 channel is sorted automatically.
10. Check the 1ch data output when 2bit counter value is only '0' and then Search the EAV/SAV[3:0] after FF 00 00 Code.
11. If the EAV/SAV[3:0] is '2', make a counter reset to '3' (Refer to Blue color in Figure2.16.)
12. Become Right sorting part.

2.10.4. 148.5MHz 2-Ch EX-FHD Data Output Mode

Operated in the 148.5MHz EX-FHD Data Out Mode, **NVP6124** outputs VCLK01, VCLK02, VCLK03, VCLK04 and VDO1[7:0], VDO2[7:0], VDO3[7:0], VDO4[7:0] in the timing as shown in Figure 2.17. Two Channel EX-FHD data stream represents 8bit BT.656/1120(like) 4:2:2 format with 148.5MHz multiplexed.

For VCLK01, VCLK02, VCLK03 and VCLK04, phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register.

- (VCLK_x_SEL, 0xCC~CF[6:4]=0x6 or 7, Control of Output Clock)
- (VCLK_x_DLY_SEL, 0xCC~CF[3:0]=0x0~F, Control of Phase in Output Clock)
- (CH_OUT_SELx, 0xC8[7:4], 0xC8[3:0], 0xC9[7:4], 0xC9[3:0]=0x11, Control how many multiplexed channel in a port)

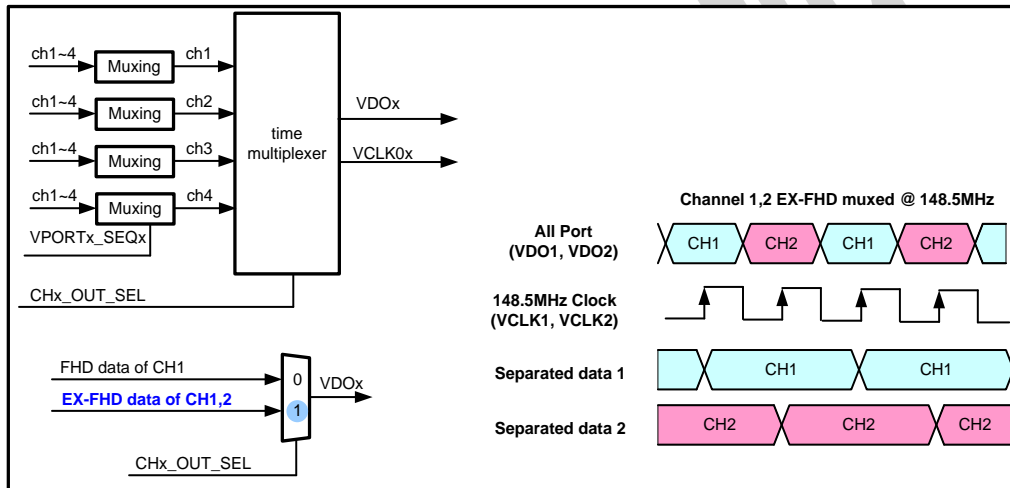


Figure 2.17. EX-FHD 2Channel muxed @148.5MHz Data Output

2.11. Video Frame Control

The **NVP6124** supports that a frame control of video output. So it is function that the decoder's output masking by the EAV/SAV make to blank region. If set to FRM_NRT_ON is High, so output finally which set by FRM_NRT_SEQ[29:0] that each a bit of FRM_NRT_SEQ[29:0] match to each a frame. And the FRM_NRT_SEQ rotates continuous then to end from FRM_NRT_SEQ[0] to FRM_NRT_SEQ[29]. If the FRAME_NRT_SEQ bit set to Low, a apply frame has blank region. So, It received back-end device nothing to do because is not active region.

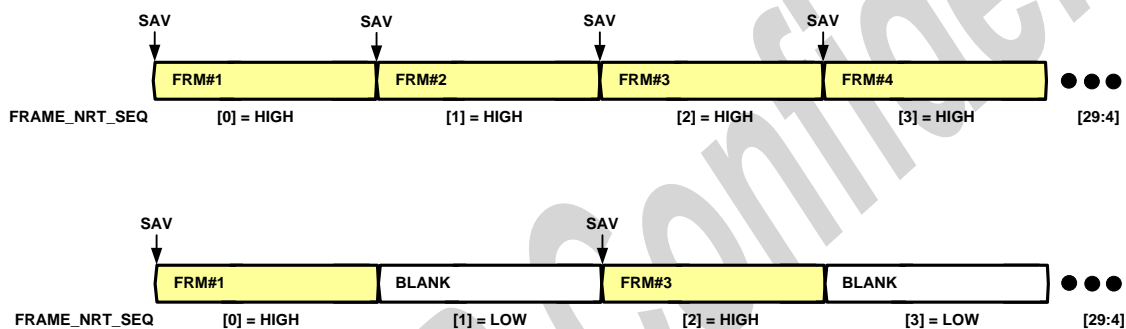


Figure 2.17. Method for Control Video Frame

2.12. Motion Detector

NVP6124 supports 4-Channels motion detection function. It supports the output of the detected motion information on the screen. The function allows a screen such as the one shown in Figure 2.18. to be divided in 192 sections each of which can generate information on the motion detection information.

For each section, motion detection can be controlled to be set at on/off. Once a motion is detected, the screen can be rendered dark or reversed in the unit of field to have the spot of the motion generated to be indicated in the screen.

□ : Motion Detection Information Block (16x12)								⋯ : Motion Detection Internal Processing Block (32x24)							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112
113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176
177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192

Figure 2.18. Motion Block Mapping

2.12.1. How to Operate the Motion Detection Function

- 1). Set the Motion detection On (Bank2, 0x00/02/04/06[4]) - Set at low

- 2). Set the area for which to detect motion
 - : The screen is divided into 192 sections and each section is matched one to one.
 - (BANK2, 0x20~0x37 - Channel 1, Bank2, 0x38~4F - Channel 2)
 - (BANK2, 0x50~0x67 - Channel 3, Bank2, 0x68~7F - Channel 4)

- 3). Set the motion sensitivity 1 (Pixel Sensitivity: Set at BANK2, 0x10)

- 4). Set the motion sensitivity 2 (Temporal Sensitivity : Set at BANK2 0x01/03/05/07)
 - : When setting motion sensitivity, it is recommended to set the pixel sensitivity at "0x60" and use the temporal sensitivity to send the sensitivity to situation.

- 5). Output of Motion Detection
 - : Motion information generated from each section is not to be generated separately through data interface. In other words, the motion information needs to be confirmed in the register or It is not included in the BT.656/1120(like) data.
 - : Motion information generated from each area can be displayed on the screen.
 - Display can be done through three approaches. This can be controlled using MOTION_PIC (BANK2, 0x00/02/04/06[1:0]).

3. Audio Codec

3.1. Description

NVP6124 outputs PCM digital audio signals converted from analog audio input signals and analog audio signals converted from PCM digital audio signals. **NVP6124** has 9 channels ADC and 1 channel DAC for audio signal.

Audio data convert to G.711 PCM and Linear PCM data, and these converted data is outputted via DSP/SSP/I2S interfaces. The output data will be saved at hard disk or any other storages. This process - to convert and save audio data into storage - is usually called as "Record Output".

The saved audio data is inputted to **NVP6124** via DSP/SSP/I2S interfaces. The input audio data is outputted via audio DAC. This process is named as "Playback Output".

NVP6124 selects one audio input signal among 9 analog audio input(8-Ch Audio/1-Ch mic) and this audio is outputted through audio ADC and audio DAC. And it also supports directly mixed audio output signal which 9 analog audio inputs are mixed. This function usually is called by "Live Output".

In addition, **NVP6124** supports audio mute detection and cascade function up to 2 chips - 18 audio channels(16-Ch Audio/2-Ch mic)

3.2. Record Output

Analog audio data is converted to PCM data and this data is outputted to the other **NVP6124** or other IC via DSP/SSP/I2S interfaces. Record output is useful function to save compressed audio data into storage. Analog audio signal is finally outputted to ADATA_REC pin used for data of each channel and ADATA_SP pin used for one mixed signal of each channel's data. The output data from ADATA_SP pin is either same data of ADATA_REC pin or mixed signal of each channel's data.

PCM data is categorized based on sampling frequency, sampling data bit width and PCM method. G.711 (A-law/Mu-law), unsigned linear PCM and linear PCM are supported. 8KHz / 16KHz and 8bit/16bit are used for sampling frequency and sampling data bit width, respectively. Refer the following table when you set the register value.

Table 3.1. Sampling & PCM coding setting

	BANK1											
	8K/8bit		8K/16bit		16K/8bit		16K/16bit		32K/8bit		32K/16bit	
	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE
Linear PCM	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00	0x08[5:4]	00
Unsigned Linear PCM	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01	0x08[5:4]	01
G.711 U-law	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10
	0x08[6]	0	0x08[6]	0	0x08[6]	0	0x08[6]	0	0x08[6]	0	0x08[6]	0
G.711 A-law	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	0	0x00[0]	1	0x00[0]	1
	0x07[3]	0	0x07[3]	0	0x07[3]	1	0x07[3]	1	0x07[3]	1	0x07[3]	1
	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0	0x07[2]	1	0x07[2]	0
	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10	0x08[5:4]	10
	0x08[6]	1	0x08[6]	1	0x08[6]	1	0x08[6]	1	0x08[6]	1	0x08[6]	1

DSP / SSP / I2S interfaces are supported as output data format. In addition, slave mode and master mode are also supported. At slave mode, input clock and synchronized signal come from external ICs, however Master mode generates clock and synchronized signal in itself.

3.2.1 Data Output Interface

NVP6124 outputs "Record Output" using ACLK_REC, ASYNC_REC, ADATA_REC and DATA_SP. ACLK_REC is a reference clock signal for Record Output Data and ASYNC_REC is a reference synchronization signal for Record Output Data. ADATA_REC and ADATA_SP are synchronized Record Output, data with reference clock and reference synchronized signal.

Table 3.2 Record Output Interface configuration

	BANK1					
	DSP		SSP		I2S	
	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE
Master	0x07[0]	1	0x07[0]	1	0x07[0]	0
	0x07[1]	0	0x07[1]	1	0x07[1]	0
	0x07[7]	1	0x07[7]	1	0x07[7]	1
Slave	0x07[0]	1	0x07[0]	1	0x07[0]	0
	0x07[1]	0	0x07[1]	1	0x07[1]	0
	0x07[7]	0	0x07[7]	0	0x07[7]	0

ACLK_REC is a reference clock of Record Output Data and ASYNC_REC is reference synchronized signal. ACLK_REC and ASYNC_REC signal support slave mode accepted external signals and master mode generating clock and synchronization signal in itself. And

DSP/SSP/I2S interfaces are supported by configuration of these pins defined by internal register setting value.

Figure 3.1, 3.2, 3.3 shows timing diagram of I2S, DSP, and SSP mode, respectively.

These figures show timing relation among ASYNC_REC, ACLK_REC and ADATA_REC, and ADATA_SP is outputted using same interface method of ADATA_REC. Polarity of ACLK_REC clock is changed by setting of internal register value (RM_CLK, 0x07[6], BANK1).

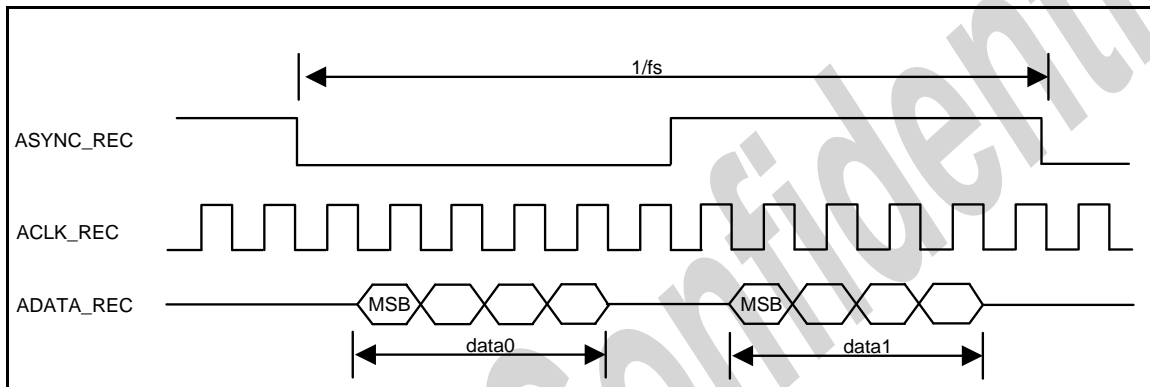


Figure 3.1 I2S mode

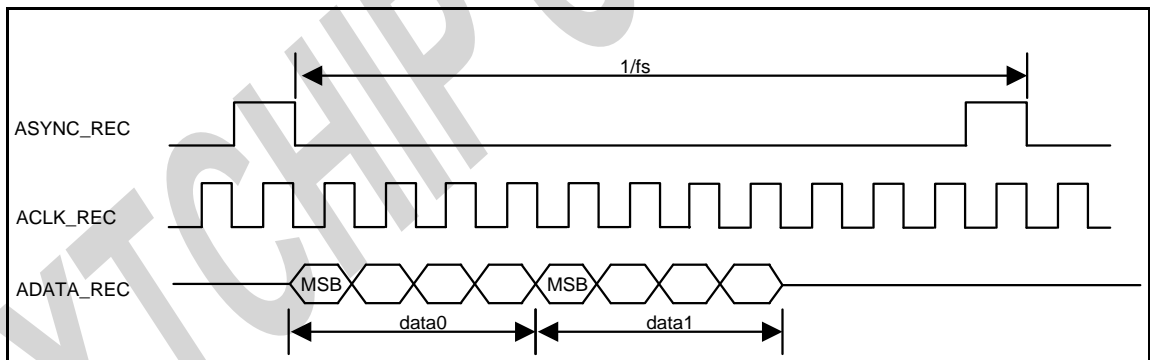


Figure 3.2 DSP mode

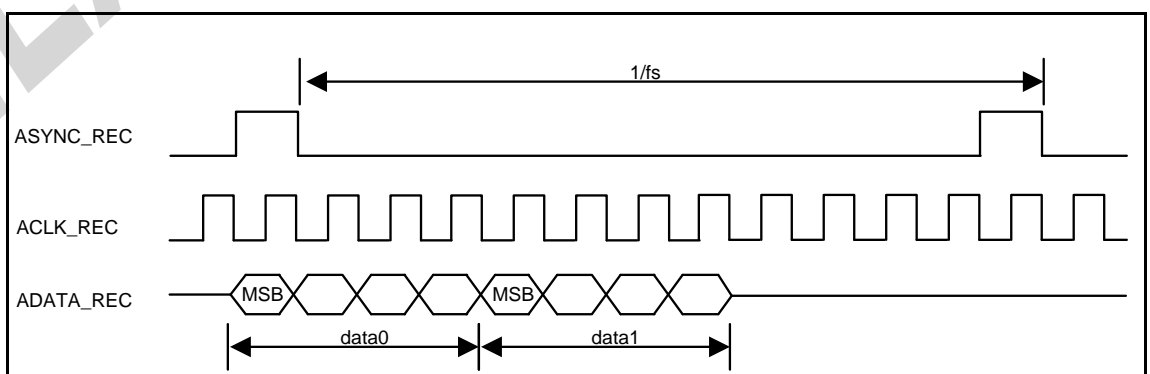


Figure 3.3 SSP mode

3.2.2. 2/4/8/16-Channel Data Output(256 fs)

ADATA_REC supports up to 8 channel audio using single chip and up to 16 channel audio in cascade mode. In this case, the bitrate of the audio signal should be 256 fs(RM_BITRATE, 0x07[5:4], BANK1). The number of output channel is configured by internal register value (R_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R_SEQ, 0x09 ~ 0x12, / MIC_SEQ, 0x3C ~ 0x3D, BANK1).

Therefore, the order of audio output can be changed.

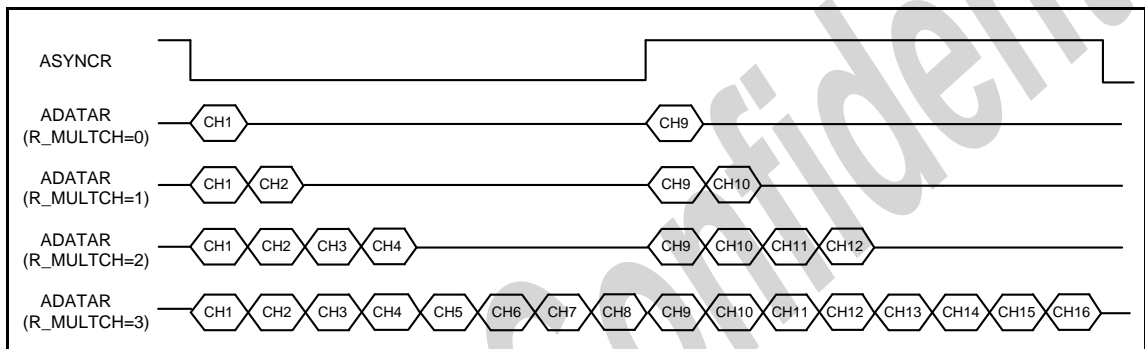


Figure 3.4. audio 2/4/8/16 channel data output <I2S mode, 256fs>

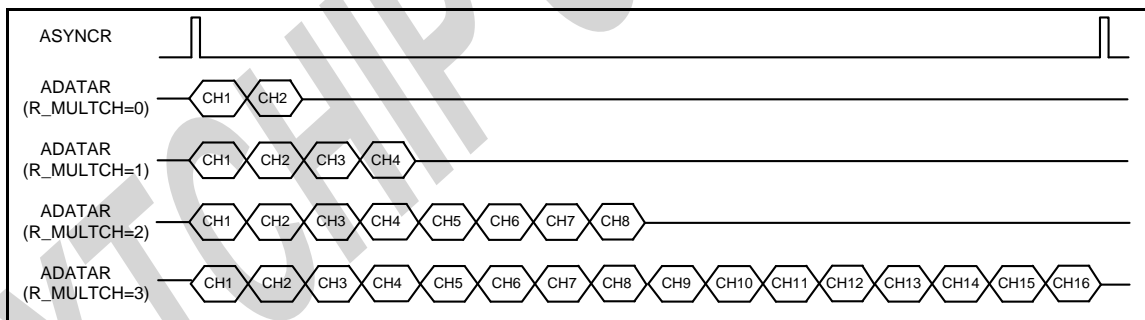


Figure 3.5. audio 2/4/8/16channel data output <DSP/SSP mode, 256fs>

3.2.3. 2/4/8/16-Channel Audio Data Output with 2-Channel Mic Data(320 fs)

ADATA_REC supports up to 9 channels(8-Ch audio/1-Ch mic) using single chip and up to 18 channel(16-Ch audio/2-Ch mic) in cascade mode. In this case, the bitrate of the audio signal should be 320 fs(RM_BITRATE, 0x07[5:4], BANK1).

The number of output channel is configured by internal register value (R_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R_SEQ, 0x09 ~ 0x12, / MIC_SEQ, 0x3C ~ 0x3D, BANK1). Therefore, the order of audio output can be changed.

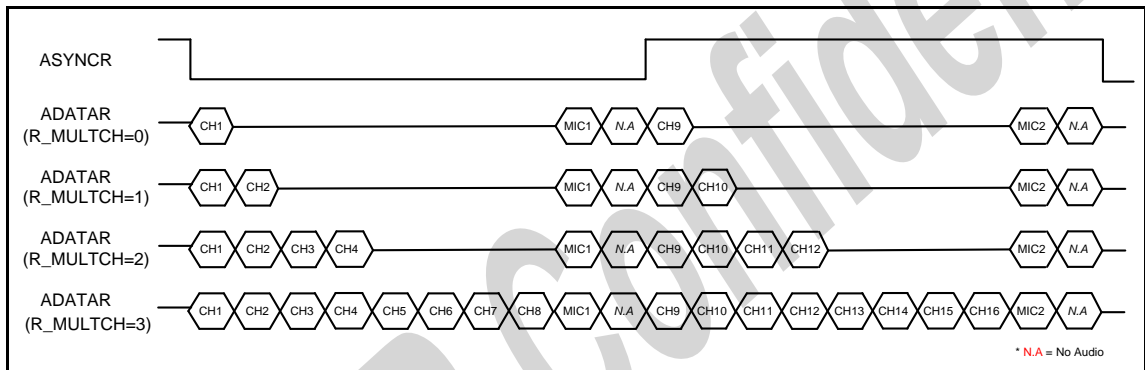


Figure 3.6 audio 2/4/6/8/16 channel data output(with 2 channel mic) <I2S mode, 320fs>

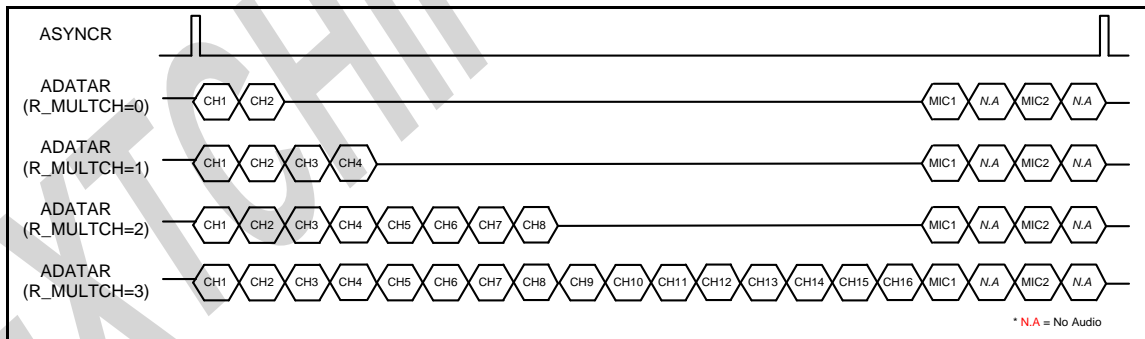


Figure 3.7. audio 2/4/8/16 channel data output(with 2 channel mic) <DSP/SSP mode, 320fs>

3.2.4. ADATA_SP Output

ADATA_SP supports 3 kinds of output method. Firstly, the output data of ADATA_SP pin is the exactly same as those of ADATA_REC except output data sequence. The order of output data is opposite. If the output data order of ADATA_REC is "CH1, CH2, CH9, CH10", the output data order of ADATA_SP is "CH16, CH15, CH8, CH7". That is to say, two output pin - ADATA_SP and ADATA_REC are complement relationship. Secondly, one of input signals is selected as output signal of ADATA_SP. The selectable input signal ranges from analog input signal to ADATA_PB signal. Lastly, mixed data of input signal is selected as the output signal of ADATA_SP. The mixing gain of each channel's input signal is determined by internal register setting value (MIX_RATIO, 0x16 ~ 0x21[7:0], BANK1).

The output configuration of ADATA_SP is determined by internal register setting. First and second configuration are determined by (R_ADATSP, 0x08[2], BANK1), and second and third configuration are determined by (L_CH_OUTSEL, 0x24[4:0], BANK1) and (R_CH_OUTSEL, 0x25[4:0], BANK1). In this case, L_CH_OUTSEL and R_CH_OUTSEL select one of input channels or mixed data.

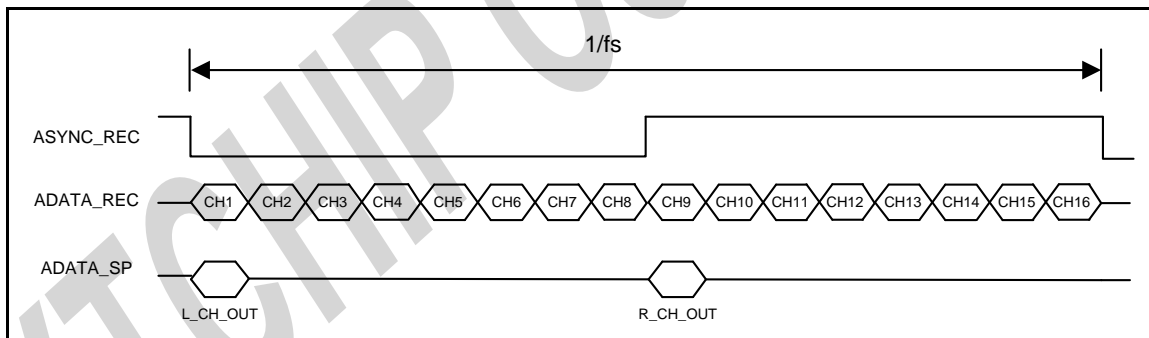


Figure 3.8 ADATA_SP Output <I2S mode>

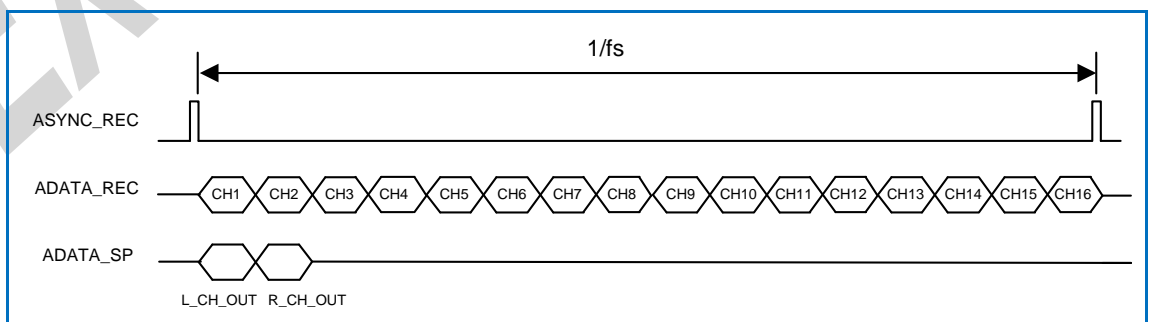


Figure 3.9 ADATA_SP Output <DSP/SSP mode>

3.3. Playback Output

Playback is to output stored audio data to external device through DAC after internal processing.

NVP6124 gives and takes a clock and synchronization signal through ACLK_PB and ASYNC_PB pin. In this case, interface is the exactly same as Record data's interface. When multi-channel audio is supported, selective playback for intended channel is enable using register setting (PB_SER, 0x14[4:0], BANK1). In case of single channel, PB_SEL should be set to "00000".

ACLK_PB and ASYNC_PB supports Master mode and Slave mode. In master mode, ACLK_PB and ASYNC_PB are outputted by **NVP6124**, and clock and synchronization signal come from external devices at slave mode. Master/Slave mode is selected by setting internal register (PB_MASTER, 0x13[7], BANK1).

ADATA_PB accepts an audio data synchronized with ACLK_PB and ASYNC_PB. ACLK_PB and ASYNCP accept I2S/DSP/SSP mode input and output, and I2S and DSP mode is set by internal register value (PB_SYNC, 0x13[0], BANK1). When DSP mode is selected, DSP/SSP mode is set by (PB_SSP, 0x13[1], BANK1). The relation of clock, synchronized signal and data are the exactly same as that of record/mix output. PB_CLK can be inverted for all modes using setting of register(PB_CLK, 0x13[6], BANK1).

3.4. Audio Detection

NVP6124 has an audio mute detection block for individual 9 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the ADET_MODE(0x29[3], BANK1) and ADET_FILT (0x29[2:0], BANK1) register, and the detecting threshold values are defined by ADET_TH register(0x2C ~ 0x30, BANK1). According to this control bits and its result (audio detected), Interrupt is generated through the interrupt pins.

3.5. Cascade Operation

NVP6124 supports cascade mode. Maximum 2 NVP6124 chips can be connected together for cascade mode and can be processed 18 channel audio encoding data(16-Ch Audio/2-Ch mic). Cascade is enabled by setting register(CHIP_STAGE, 0x06[1:0], BANK1). Figure 3.10 shows how to connect NVP6124 for the cascade mode. In this case, analog audio AOUT1 is assigned to AIN1-16 and MICIN1-2. 1 channel audio or all channel mixed audio signal is selected as output signal set by MIX_OUTSEL(0x23[4:0], BANK1).

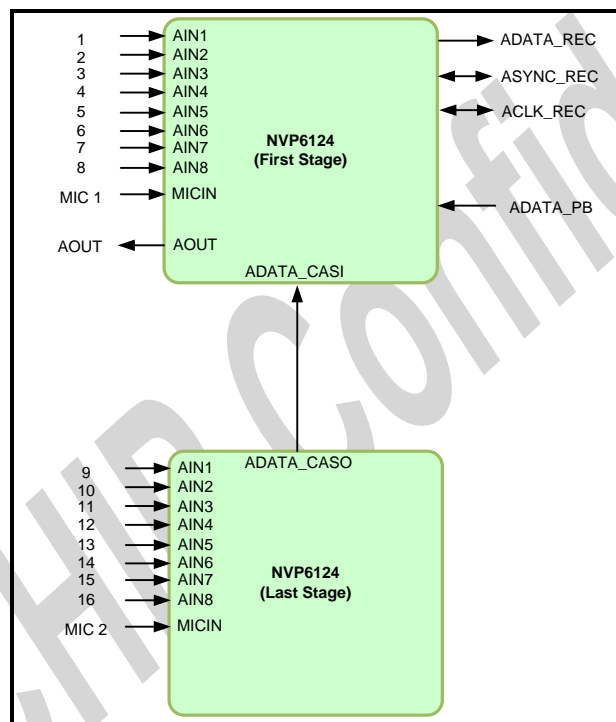


Figure 3. 10. Consist of Cascade System using 2-NVP6124

4. Coaxial Protocol

NVP6124 includes Coaxial Protocol generator that sends control signal from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal. **NVP6124** supports Protocol for CVBS/COMET(PELCO) & AHD(A-CP). It depends on Coaxial Cable impedance characteristic. This document presents the concept of Coaxial Protocol. Coaxitron is Pelco's name for a method of sending control signaling from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal (Known as "Up The Coax" or "UTC")

4.1. PELCO PROTOCOL

There are two types of Coaxitron command structures. One type, Standard Coaxitron, is a series of 15 pulses, or data bits, that are sent within video line 18 of a video field. The other type, Extended Coaxitron, is a series of 32 pulses, where 16 pulses are sent in line 18 and 16 pulses in line 19 of a video field. Refer to Figure 4.1. No pulses are sent when the system is in an idle state

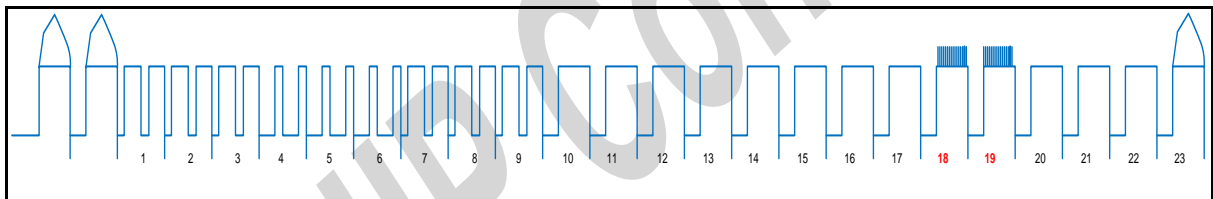


Figure 4.1. Coaxitron Active line

Coaxitron is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 2us pulse represents a one(1) and a 1us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 4.2. and Figure 4.3.

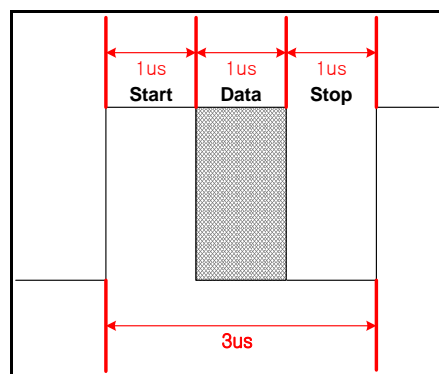


Figure 4.2. Description of One Coaxitron Bit

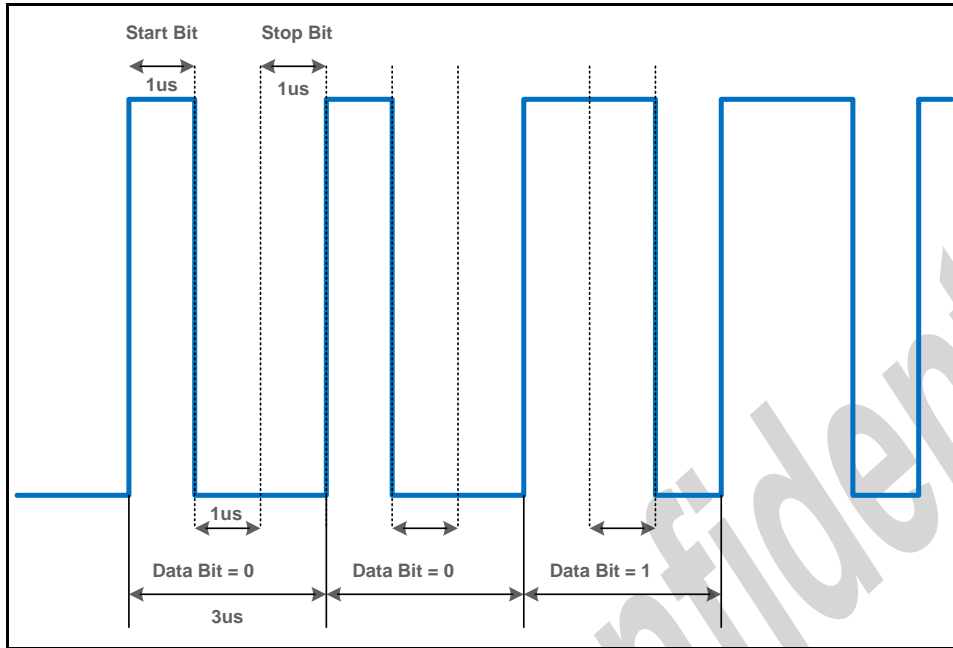


Figure 4.3. Coaxitron Bit Timing

NVP6124 is able to control coaxitron timing format on the video signal.

Start Active line of Coaxitron (BL_TXST, 0x03~04[3:0],0x83~84[3:0], BANK3~4) is 18th line on VBI. Pulse width of Coaxitron (BAUD, 0x00,80, BANK3~4) is fixed 1µs. The size of Coaxial Data (PELCO_TXDAT, 0x20~23,0xA0~A3, BANK3~4) is 4 bytes. Refer to Figure 4.4.

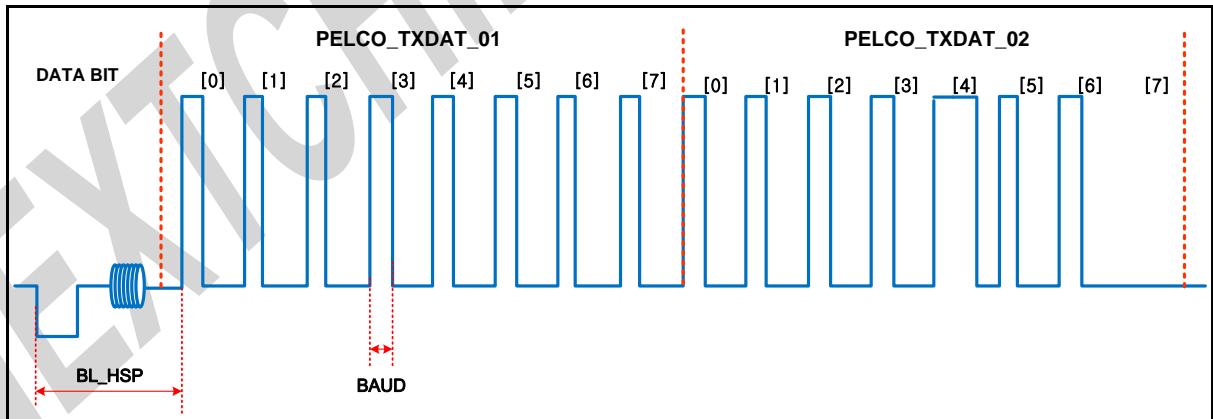


Figure 4.4. Data Structure of Coaxitron Origins (VBI 18th)

4.2. A-CP(AHD-Coaxial protocol)

A-CP is the specifications are made for use in the Coaxial protocol AHD.

As a major feature, A-CP Data located in the 17~20th line. Also Data is 8bit each line.

In this regard, please refer to the application note.

5. I2C Interface

I2C interface requires 2 wires, SCL (I2C clock) & SDA (I2C R/W data). **NVP6124** provides special device ID as slave addresses (SA0, SA1). So any combination of 7 bit can be defined as slave address of **NVP6124**. The Figure 5.1 shows read/write protocol of I2C interface. The 1st byte transfers slave address and read/write information. For write mode, the 2nd byte transfers base register index and the 3rd byte transfers date to be written.

For read mode, reading data is transferred during 2nd byte period. The brief I2C interface protocol is shown in Figure 5.2.

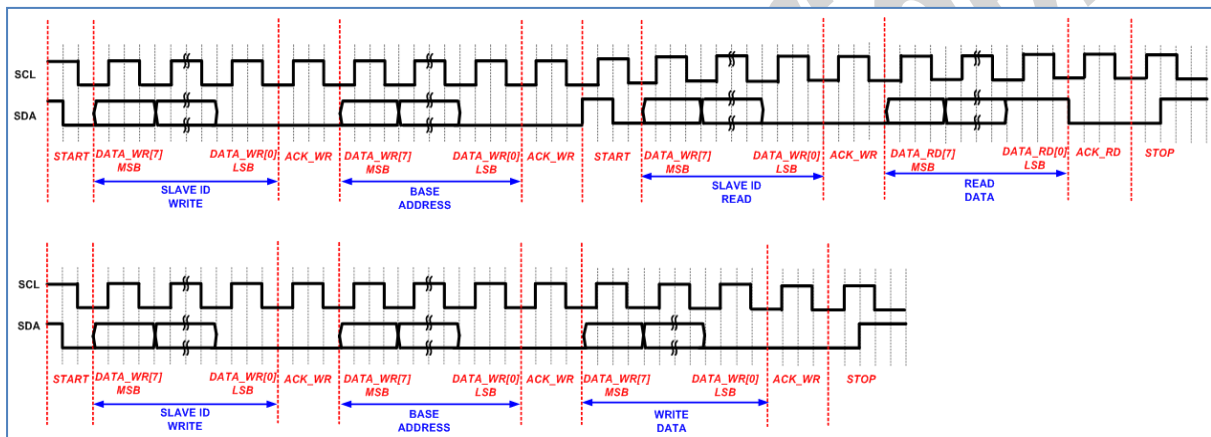


Figure 5.1. I2C Timing Diagram

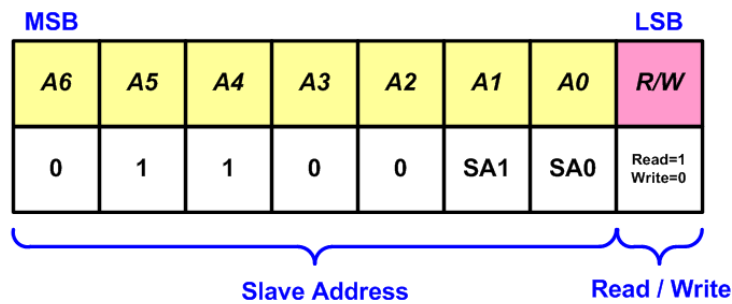



Figure 5.2. I2C Slave Address Configuration


6. Register Description

BANK0 Register(0x00~0x1F) : VIDEO


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x00	-RESERVED-								0x00	0x00	0x00
0x01	-RESERVED-								0x00	0x00	0x00
0x02	PD_ADAC	-RESERVED-			PD_VCH4	PD_VCH3	PD_VCH2	PD_VCH1	0xF0	0x20	0x20
0x03	-RESERVED-								0x00	0x00	0x00
0x04	-RESERVED-								0x00	0x00	0x00
0x05	-RESERVED-								0x00	0x00	0x00
0x06	-								-	-	-
0x07	-								-	-	-
0x08	AUTO_1	BSF_MODE_1		VIDEO_FORMAT_1					0x60	0x60	0x60
0x09	AUTO_2	BSF_MODE_2		VIDEO_FORMAT_2					0x60	0x60	0x60
0x0A	AUTO_3	BSF_MODE_3		VIDEO_FORMAT_3					0x60	0x60	0x60
0x0B	AUTO_4	BSF_MODE_4		VIDEO_FORMAT_4					0x60	0x60	0x60
0x0C	BRIGHTNESS_1								0x08	0x08	0x08
0x0D	BRIGHTNESS_2								0x08	0x08	0x08
0x0E	BRIGHTNESS_3								0x08	0x08	0x08
0x0F	BRIGHTNESS_4								0x08	0x08	0x08
0x10	CONTRAST_1								0x88	0x88	0x88
0x11	CONTRAST_2								0x88	0x88	0x88
0x12	CONTRAST_3								0x88	0x88	0x88
0x13	CONTRAST_4								0x88	0x88	0x88
0x14	H_SHARPNESS_1				V_SHARPNESS_1				0x90	0x90	0x90
0x15	H_SHARPNESS_2				V_SHARPNESS_2				0x90	0x90	0x90
0x16	H_SHARPNESS_3				V_SHARPNESS_3				0x90	0x90	0x90
0x17	H_SHARPNESS_4				V_SHARPNESS_4				0x90	0x90	0x90
0x18	Y_PEAK_MODE_1				Y_FIR_MODE_1				0x00	0x00	0x00
0x19	Y_PEAK_MODE_2				Y_FIR_MODE_2				0x00	0x00	0x00
0x1A	Y_PEAK_MODE_3				Y_FIR_MODE_3				0x00	0x00	0x00
0x1B	Y_PEAK_MODE_4				Y_FIR_MODE_4				0x00	0x00	0x00
0x1C	-RESERVED-								0xAF	0xAF	0xAF
0x1D	-RESERVED-								0xAF	0xAF	0xAF
0x1E	-RESERVED-								0xAF	0xAF	0xAF
0x1F	-RESERVED-								0xAF	0xAF	0xAF

 **BANK0 Register(0x20~0x3F) : VIDEO**


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK0	0x20	ACC_OFF_1	-RESERVED-		ACC_GAIN_SPD_1			0x2F	0x2F	0x2F	
	0x21	PAL_CM_OFF_1	IF_FIR_SEL_1		CLPF_SEL_1			0x82	0x82	0x82	
	0x22	-		COLOROFF_1	C_KILL_1			0x0B	0x0B	0x0B	
	0x23	FLD_DET_MODE_1		-RESERVED-		NOVID_DET_B_1			0x43	0x43	0x43
	0x24	ACC_OFF_2	-RESERVED-		ACC_GAIN_SPD_2			0x2F	0x2F	0x2F	
	0x25	PAL_CM_OFF_2	IF_FIR_SEL_2		CLPF_SEL_2			0x82	0x82	0x82	
	0x26	-		COLOROFF_2	C_KILL_2			0x0B	0x0B	0x0B	
	0x27	FLD_DET_MODE_2		-RESERVED-		NOVID_DET_B_2			0x43	0x43	0x43
	0x28	ACC_OFF_3	-RESERVED-		ACC_GAIN_SPD_3			0x2F	0x2F	0x2F	
	0x29	PAL_CM_OFF_3	IF_FIR_SEL_3		CLPF_SEL_3			0x82	0x82	0x82	
	0x2A	-		COLOROFF_3	C_KILL_3			0x0B	0x0B	0x0B	
	0x2B	FLD_DET_MODE_3		-RESERVED-		NOVID_DET_B_3			0x43	0x43	0x43
	0x2C	ACC_OFF_4	-RESERVED-		ACC_GAIN_SPD_4			0x2F	0x2F	0x2F	
	0x2D	PAL_CM_OFF_4	IF_FIR_SEL_4		CLPF_SEL_4			0x82	0x82	0x82	
	0x2E	-		COLOROFF_4	C_KILL_4			0x0B	0x0B	0x0B	
	0x2F	FLD_DET_MODE_4		-RESERVED-		NOVID_DET_B_4			0x43	0x43	0x43
	0x30	-RESERVED-		Y_DELAY_1			0x10	0x10	0x10		
	0x31	-RESERVED-		Y_DELAY_2			0x10	0x10	0x10		
	0x32	-RESERVED-		Y_DELAY_3			0x10	0x10	0x10		
	0x33	-RESERVED-		Y_DELAY_4			0x10	0x10	0x10		
0x34	-	PED_ON_1	-RESERVED-			0x02	0x04	0x02			
0x35	-	PED_ON_2	-RESERVED-			0x02	0x04	0x02			
0x36	-	PED_ON_3	-RESERVED-			0x02	0x04	0x02			
0x37	-	PED_ON_4	-RESERVED-			0x02	0x04	0x02			
0x38	CTI_GAIN_1				0x0A	0x0A	0x0A				
0x39	CTI_GAIN_2				0x0A	0x0A	0x0A				
0x3A	CTI_GAIN_3				0x0A	0x0A	0x0A				
0x3B	CTI_GAIN_4				0x0A	0x0A	0x0A				
0x3C	SATURATION_1				0x84	0x84	0x84				
0x3D	SATURATION_2				0x84	0x84	0x84				
0x3E	SATURATION_3				0x84	0x84	0x84				
0x3F	SATURATION_4				0x84	0x84	0x84				

 BANK0 Register(0x40~0x5F) : VIDEO


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
B A N K 0	0x40	HUE_1							0x00	0xFD	0x00
	0x41	HUE_2							0x00	0xFD	0x00
	0x42	HUE_3							0x00	0xFD	0x00
	0x43	HUE_4							0x00	0xFD	0x00
	0x44	U_GAIN_1							0x30	0x30	0x30
	0x45	U_GAIN_2							0x30	0x30	0x30
	0x46	U_GAIN_3							0x30	0x30	0x30
	0x47	U_GAIN_4							0x30	0x30	0x30
	0x48	V_GAIN_1							0x30	0x30	0x30
	0x49	V_GAIN_2							0x30	0x30	0x30
	0x4A	V_GAIN_3							0x30	0x30	0x30
	0x4B	V_GAIN_4							0x30	0x30	0x30
	0x4C	U_OFFSET_1							0x04	0x04	0x04
	0x4D	U_OFFSET_2							0x04	0x04	0x04
	0x4E	U_OFFSET_3							0x04	0x04	0x04
	0x4F	U_OFFSET_4							0x04	0x04	0x04
	0x50	V_OFFSET_1							0x04	0x04	0x04
	0x51	V_OFFSET_2							0x04	0x04	0x04
	0x52	V_OFFSET_3							0x04	0x04	0x04
	0x53	V_OFFSET_4							0x04	0x04	0x04
0x54	FLD_INV_4	FLD_INV_3	FLD_INV_2	FLD_INV_1	NOVID_INF_IN_14	CHID_TYPE_14			0x01	0xF1	0x01
0x55	CHID_VIN2				CHID_VIN1				0x10	0x10	0x10
0x56	CHID_VIN4				CHID_VIN3				0x32	0x10	0x10
0x57	-							-	-	-	
0x58	H_DELAY_1							0x90	0xA0	0x90	
0x59	H_DELAY_2							0x90	0xA0	0x90	
0x5A	H_DELAY_3							0x90	0xA0	0x90	
0x5B	H_DELAY_4							0x90	0xA0	0x90	
0x5C	V_DELAY_1							0x9E	0x9E	0x9E	
0x5D	V_DELAY_2							0x9E	0x9E	0x9E	
0x5E	V_DELAY_3							0x9E	0x9E	0x9E	
0x5F	V_DELAY_4							0x9E	0x9E	0x9E	

 **BANK0 Register(0x60~0x7F) : VIDEO**


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
B A N K 0	0x60	HBLK_END_1							0x00	0x00	0x00
	0x61	HBLK_END_2							0x00	0x00	0x00
	0x62	HBLK_END_3							0x00	0x00	0x00
	0x63	HBLK_END_4							0x00	0x00	0x00
	0x64	VBLK_END_1							0x8D	0xB2	0xB1
	0x65	VBLK_END_2							0x8D	0xB2	0xB1
	0x66	VBLK_END_3							0x8D	0xB2	0xB1
	0x67	VBLK_END_4							0x8D	0xB2	0xB1
	0x68	H_CROP_S_1							0x00	0x00	0x00
	0x69	H_CROP_S_2							0x00	0x00	0x00
	0x6A	H_CROP_S_3							0x00	0x00	0x00
	0x6B	H_CROP_S_4							0x00	0x00	0x00
	0x6C	H_CROP_E_1							0x00	0x00	0x00
	0x6D	H_CROP_E_2							0x00	0x00	0x00
	0x6E	H_CROP_E_3							0x00	0x00	0x00
	0x6F	H_CROP_E_4							0x00	0x00	0x00
	0x70	V_CROP_S_1							0x00	0x00	0x00
	0x71	V_CROP_S_2							0x00	0x00	0x00
	0x72	V_CROP_S_3							0x00	0x00	0x00
	0x73	V_CROP_S_4							0x00	0x00	0x00
	0x74	V_CROP_E_1							0x00	0x00	0x00
	0x75	V_CROP_E_2							0x00	0x00	0x00
	0x76	V_CROP_E_3							0x00	0x00	0x00
	0x77	V_CROP_E_4							0x00	0x00	0x00
	0x78	BGDCOL_2			BGDCOL_1				0x88	0x88	0x88
	0x79	BGDCOL_4			BGDCOL_3				0x88	0x88	0x88
	0x7A	DATA_OUT_MODE_2			DATA_OUT_MODE_1				0x11	0x11	0x11
	0x7B	DATA_OUT_MODE_4			DATA_OUT_MODE_3				0x11	0x11	0x11
	0x7C								-	-	-
	0x7D								-	-	-
	0x7E								-	-	-
	0x7F								-	-	-

 **BANK0 Register(0x80~0x9F) : VIDEO_ENABLE**


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
B A N K 0	0x80	-			EACH_REG_SET				0x00	0x00	0x00	
	0x81	-RESERVED-			AHD_MD_1				0x07	0x06	0x07	
	0x82	-RESERVED-			AHD_MD_2				0x07	0x06	0x07	
	0x83	-RESERVED-			AHD_MD_3				0x07	0x06	0x07	
	0x84	-RESERVED-			AHD_MD_4				0x07	0x06	0x07	
	0x85	-			STD_MD_1		-		AV_960H_1	0x00	0x00	0x00
	0x86	-			STD_MD_2		-		AV_960H_2	0x00	0x00	0x00
	0x87	-			STD_MD_3		-		AV_960H_3	0x00	0x00	0x00
	0x88	-			STD_MD_4		-		AV_960H_4	0x00	0x00	0x00
	0x89	-RESERVED-							SEL960H_01	0x10	0x10	0x10
	0x8A	-RESERVED-							SEL960H_02	0x10	0x10	0x10
	0x8B	-RESERVED-							SEL960H_03	0x10	0x10	0x10
	0x8C	-RESERVED-							SEL960H_04	0x10	0x10	0x10
	0x8D	-								-	-	-
	0x8E	-RESERVED-								0x0A	0x07	0x0B
	0x8F	-RESERVED-								0x0A	0x07	0x0B
	0x90	-RESERVED-								0x0A	0x07	0x0B
	0x91	-RESERVED-								0x0A	0x07	0x0B
	0x92	-								-	-	-
	0x93	-RESERVED-							HZOOM_ON_1	0x00	0x00	0x00
	0x94	-RESERVED-							HZOOM_ON_2	0x00	0x00	0x00
	0x95	-RESERVED-							HZOOM_ON_3	0x00	0x00	0x00
	0x96	-RESERVED-							HZOOM_ON_4	0x00	0x00	0x00
	0x97	-RESERVED-								0x00	0x00	0x00
	0x98	-RESERVED-								0x00	0x16	0x16
	0x99	-RESERVED-								0x00	0x16	0x16
	0x9A	-RESERVED-								0x00	0x16	0x16
	0x9B	-RESERVED-								0x00	0x16	0x16
0x9C	-RESERVED-								0x00	0x00	0x00	
0x9D	-RESERVED-								0x00	0x00	0x00	
0x9E	-RESERVED-								0x00	0x00	0x00	
0x9F	-RESERVED-								0x00	0x00	0x00	

 **BANK0 Register(0xA0~0xBF) : DELAY & STATUS**


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
B A N K 0	0xA0	DF_CDELAY_1			DF_YDELAY_1				0x00	0x00	0x00	
	0xA1	DF_CDELAY_2			DF_YDELAY_2				0x00	0x00	0x00	
	0xA2	DF_CDELAY_3			DF_YDELAY_3				0x00	0x00	0x00	
	0xA3	DF_CDELAY_4			DF_YDELAY_4				0x00	0x00	0x00	
	0xA4	DB_CDELAY_1			DB_YDELAY_1				0x10	0x10	0x10	
	0xA5	DB_CDELAY_2			DB_YDELAY_2				0x10	0x10	0x10	
	0xA6	DB_CDELAY_3			DB_YDELAY_3				0x10	0x10	0x10	
	0xA7	DB_CDELAY_4			DB_YDELAY_4				0x10	0x10	0x10	
	0xA8									-	-	-
	0xA9									-	-	-
	0xAA									-	-	-
	0xAB									-	-	-
	0xAC									-	-	-
	0xAD									-	-	-
	0xAE									-	-	-
	0xAF									-	-	-
	0xB0									-	-	-
	0xB1									-	-	-
	0xB2									-	-	-
	0xB3									-	-	-
	0xB4									-	-	-
	0xB5									-	-	-
	0xB6									-	-	-
	0xB7									-	-	-
	0xB8	-	-	-	-	NOVID_04	NOVID_03	NOVID_02	NOVID_01	R	R	R
	0xB9	-	-	-	-	MOTION_04	MOTION_03	MOTION_02	MOTION_01	R	R	R
	0xBA	-	-	-	-	BLACK_04	BLACK_03	BLACK_02	BLACK_01	R	R	R
	0xBB	-	-	-	-	WHITE_04	WHITE_03	WHITE_02	WHITE_01	R	R	R
0xBC	MUTE_08	MUTE_07	MUTE_06	MUTE_05	MUTE_04	MUTE_03	MUTE_02	MUTE_01	R	R	R	
0xBD	MUTE_16	MUTE_15	MUTE_14	MUTE_13	MUTE_12	MUTE_11	MUTE_10	MUTE_09	R	R	R	
0xBE	-	-	-	-	-	MUTEMIC_02	-	MUTEMIC_01	R	R	R	
0xBF	-	-	-	-	COAX_RX_DONE_4	COAX_RX_DONE_3	COAX_RX_DONE_2	COAX_RX_DONE_1	R	R	R	

 BANK0 Register(0xC0~0xDF) : STATUS

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0xC0	-	-	-	-	NOVID_04B	NOVID_03B	NOVID_02B	NOVID_01B	R	R	R
0xC1	-	-	-	-	MOTION_04B	MOTION_03B	MOTION_02B	MOTION_01B	R	R	R
0xC2	-	-	-	-	BLACK_04B	BLACK_03B	BLACK_02B	BLACK_01B	R	R	R
0xC3	-	-	-	-	WHITE_04B	WHITE_03B	WHITE_02B	WHITE_01B	R	R	R
0xC4	MUTE_08B	MUTE_07B	MUTE_06B	MUTE_05B	MUTE_04B	MUTE_03B	MUTE_02B	MUTE_01B	R	R	R
0xC5	MUTE_16B	MUTE_15B	MUTE_14B	MUTE_13B	MUTE_12B	MUTE_11B	MUTE_10B	MUTE_09B	R	R	R
0xC6	-	-	-	-	-	MUTEMIC_02B	-	MUTEMIC_01B	R	R	R
0xC7	-	-	-	-	COAX_RX_DONE_4B	COAX_RX_DONE_3B	COAX_RX_DONE_2B	COAX_RX_DONE_1B	R	R	R
0xC8	RD_STATE_CLR	-	-	STATE_HOLD	-	-	-	-	0x90	0x90	0x90
0xC9	-	-	-	-	IRQ_INV	IRQ_SEL		-	0x00	0x00	0x00
0xCA									-	-	-
0xCB									-	-	-
0xCC									-	-	-
0xCD									-	-	-
0xCE									-	-	-
0xCF									-	-	-
0xD0	1080P25_DET_1	1080P30_DET_1	720P50_DET_1	720P60_DET_1	720P25_DET_1	720P30_DET_1	SDPAL_DET_1	SDNT_DET_1	R	R	R
0xD1	1080P25_DET_2	1080P30_DET_2	720P50_DET_2	720P60_DET_2	720P25_DET_2	720P30_DET_2	SDPAL_DET_2	SDNT_DET_2	R	R	R
0xD2	1080P25_DET_3	1080P30_DET_3	720P50_DET_3	720P60_DET_3	720P25_DET_3	720P30_DET_3	SDPAL_DET_3	SDNT_DET_3	R	R	R
0xD3	1080P25_DET_4	1080P30_DET_4	720P50_DET_4	720P60_DET_4	720P25_DET_4	720P30_DET_4	SDPAL_DET_4	SDNT_DET_4	R	R	R
0xD4									-	-	-
0xD5									-	-	-
0xD6									-	-	-
0xD7									-	-	-
0xD8	STATUS_ACC_GAIN1								R	R	R
0xD9	STATUS_ACC_GAIN2								R	R	R
0xDA	STATUS_ACC_GAIN3								R	R	R
0xDB	STATUS_ACC_GAIN4								R	R	R
0xDC									-	-	-
0xDD									-	-	-
0xDE									-	-	-
0xDF									-	-	-

 **BANK0 Register(0xE0~0xFF) : STATUS**


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0xE0									-	-	-
0xE1									-	-	-
0xE2									-	-	-
0xE3									-	-	-
0xE4									-	-	-
0xE5									-	-	-
0xE6									-	-	-
0xE7									-	-	-
0xE8	PN_READ_MSB_VAL1[3:0]				FSC_CHG_DONE1	CKILL1	FSC_LOCK_DONE1	NOVIDEO1	R	R	R
0xE9	PN_READ_MSB_VAL2[3:0]				FSC_CHG_DONE2	CKILL2	FSC_LOCK_DONE2	NOVIDEO2	R	R	R
0xEA	PN_READ_MSB_VAL3[3:0]				FSC_CHG_DONE3	CKILL3	FSC_LOCK_DONE3	NOVIDEO3	R	R	R
0xEB	PN_READ_MSB_VAL4[3:0]				FSC_CHG_DONE4	CKILL4	FSC_LOCK_DONE4	NOVIDEO4	R	R	R
0xEC		-			AGC_LOCK_04	AGC_LOCK_03	AGC_LOCK_02	AGC_LOCK_01	R	R	R
0xED		-			CMP_LOCK_04	CMP_LOCK_03	CMP_LOCK_02	CMP_LOCK_01	R	R	R
0xEE		-			H_LOCK_04	H_LOCK_03	H_LOCK_02	H_LOCK_01	R	R	R
0xEF	AUTO_NT_04		AUTO_NT_03		AUTO_NT_02		AUTO_NT_01		R	R	R
0xF0									-	-	-
0xF1	FLD_04		FLD_03		FLD_02		FLD_01		R	R	R
0xF2									-	-	-
0xF3		-			BW_04	BW_03	BW_02	BW_01	R	R	R
0xF4	DEV_ID (NVP6124 = 0x84)								R	R	R
0xF5	-RESERVED-								R	R	R
0xF6	CMP_VALUE								R	R	R
0xF7	AGC_VALUE								R	R	R
0xF8	-RESERVED-								R	R	R
0xF9	-RESERVED-								R	R	R
0xFA	-RESERVED-								R	R	R
0xFB	-RESERVED-								R	R	R
0xFC	-								-	-	-
0xFD	-RESERVED-								R	R	R
0xFE	-RESERVED-								R	R	R
0xFF		-			BANK_SEL				0x00	0x00	0x00

 BANK1 Register(0x00~0x1F) : AUDIO


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x00	PD_AAFE		-		RM_PB_PIN	PB_RM_PIN	FILTER_ON	EN_32K_MODE	0x02	0x02	0x02
0x01	AIGAIN_01								0x00	0x0A	0x0A
0x02	AIGAIN_02								0x00	0x0A	0x0A
0x03	AIGAIN_03								0x00	0x0A	0x0A
0x04	AIGAIN_04								0x00	0x0A	0x0A
0x05	MIGAIN_01								0x00	0x0A	0x0A
0x06	CAS_PB	TRANS_MODE	-	CAS_PIN	-RESERVED-		CHIP_STAGE		0x1B	0x1B	0x1B
0x07	RM_MASTER	RM_CLK	RM_BITRATE		RM_SAMRATE	RM_BITWID	RM_SSP	RM_SYNC	0xC8	0xC8	0xC8
0x08	RM_BIT_SWAP	RM_LAW_SEL	RM_FORMAT		R_ADATSP2	R_ADATSP	R_MULTCH		0x03	0x03	0x03
0x09	R_SEQ_08[4]	R_SEQ_07[4]	R_SEQ_06[4]	R_SEQ_05[4]	R_SEQ_04[4]	R_SEQ_03[4]	R_SEQ_02[4]	R_SEQ_01[4]	0x00	0x00	0x00
0x0A	R_SEQ_02[3:0]				R_SEQ_01[3:0]				0x10	0x10	0x10
0x0B	R_SEQ_04[3:0]				R_SEQ_03[3:0]				0x32	0x32	0x32
0x0C	R_SEQ_06[3:0]				R_SEQ_05[3:0]				0x54	0x54	0x54
0x0D	R_SEQ_08[3:0]				R_SEQ_07[3:0]				0x76	0x76	0x76
0x0E	R_SEQ_16[4]	R_SEQ_15[4]	R_SEQ_14[4]	R_SEQ_13[4]	R_SEQ_12[4]	R_SEQ_11[4]	R_SEQ_10[4]	R_SEQ_09[4]	0x00	0x00	0x00
0x0F	R_SEQ_10[3:0]				R_SEQ_09[3:0]				0x98	0x98	0x98
0x10	R_SEQ_12[3:0]				R_SEQ_11[3:0]				0xBA	0xBA	0xBA
0x11	R_SEQ_14[3:0]				R_SEQ_13[3:0]				0xDC	0xDC	0xDC
0x12	R_SEQ_16[3:0]				R_SEQ_15[3:0]				0xFE	0xFE	0xFE
0x13	PB_MASTER	PB_CLK	PB_BITRATE		PB_SAMRATE	PB_BITWID	PB_SSP	PB_SYNC	0x08	0x08	0x08
0x14	PB_BIT_SWAP	-			PB_SEL				0x00	0x00	0x00
0x15	PB_FORMAT		-		PB_LAW_SEL	-RESERVED-			0x00	0x00	0x00
0x16	MIX_RATIO_02				MIX_RATIO_01				0x88	0x88	0x88
0x17	MIX_RATIO_04				MIX_RATIO_03				0x88	0x88	0x88
0x18	MIX_RATIO_06				MIX_RATIO_05				0x88	0x88	0x88
0x19	MIX_RATIO_08				MIX_RATIO_07				0x88	0x88	0x88
0x1A	MIX_RATIO_10				MIX_RATIO_09				0x88	0x88	0x88
0x1B	MIX_RATIO_12				MIX_RATIO_11				0x88	0x88	0x88
0x1C	MIX_RATIO_14				MIX_RATIO_13				0x88	0x88	0x88
0x1D	MIX_RATIO_16				MIX_RATIO_15				0x88	0x88	0x88
0x1E	MIX_RATIO_M2				MIX_RATIO_M1				0x88	0x88	0x88
0x1F	MIX_RATIO_M4				MIX_RATIO_M3				0x88	0x88	0x88

BANK1 Register(0x20~0x3F) : AUDIO

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x20	MIX_RATIO_P2				MIX_RATIO_P1				0x88	0x88	0x88
0x21	MIX_RATIO_P4				MIX_RATIO_P3				0x88	0x88	0x88
0x22	AOGAIN								0x00	0x0A	0x0A
0x23	-RESERVED-		MIX_DERATIO	MIX_OUTSEL				0x19	0x19	0x19	
0x24	-				L_CH_OUTSEL				0x18	0x18	0x18
0x25	-				R_CH_OUTSEL				0x16	0x16	0x16
0x26	MIX_MUTE_08	MIX_MUTE_07	MIX_MUTE_06	MIX_MUTE_05	MIX_MUTE_04	MIX_MUTE_03	MIX_MUTE_02	MIX_MUTE_01	0x00	0x00	0x00
0x27	MIX_MUTE_16	MIX_MUTE_15	MIX_MUTE_14	MIX_MUTE_13	MIX_MUTE_12	MIX_MUTE_11	MIX_MUTE_10	MIX_MUTE_09	0x00	0x00	0x00
0x28	MIX_MUTE_M4	MIX_MUTE_M3	MIX_MUTE_M2	MIX_MUTE_M1	MIX_MUTE_P4	MIX_MUTE_P3	MIX_MUTE_P2	MIX_MUTE_P1	0x00	0x00	0x00
0x29	-RESERVED-				ADET_MODE	ADET_FILT			0x88	0x88	0x88
0x2A	ADET_08	ADET_07	ADET_06	ADET_05	ADET_04	ADET_03	ADET_02	ADET_01	0xFF	0xFF	0xFF
0x2B	-	ADET_M1							0xC0	0x40	0x40
0x2C	ADET_TH_02				ADET_TH_01				0xAA	0xAA	0xAA
0x2D	ADET_TH_04				ADET_TH_03				0xAA	0xAA	0xAA
0x2E	ADET_TH_06				ADET_TH_05				0xAA	0xAA	0xAA
0x2F	ADET_TH_08				ADET_TH_07				0xAA	0xAA	0xAA
0x30	-				ADET_TH_M1				0xAA	0x0A	0x0A
0x31	-RESERVED-								0x02	0x82	0x82
0x32	-RESERVED-								0x00	0x00	0x00
0x33	-RESERVED-								0x00	0x01	0x01
0x34	-RESERVED-								0x00	0x00	0x00
0x35	-RESERVED-								0x00	0x8C	0x8C
0x36	-RESERVED-								0x00	0xA0	0xA0
0x37	-RESERVED-								0x00	0x00	0x00
0x38	-RESERVED-			AUD_SW_RST	-RESERVED-				0x00	0x08	0x08
0x39	RM_DELAY	PB_DELAY	-RESERVED-						0x05	0x01	0x01
0x3A	-RESERVED-								0x80	0x80	0x80
0x3B	-RESERVED-								0x10	0x30	0x30
0x3C	-				MIC_SEQ_01				0x00	0x00	0x00
0x3D	-				MIC_SEQ_02				0x00	0x00	0x00
0x3E	-RESERVED-								0x10	0x10	0x10
0x3F	-								0x11	0x00	0x00

 BANK1 Register(0x40~0x5F) : AUDIO


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
B A N K 1	0x40	AIGAIN_05							0x00	0x0A	0x0A
	0x41	AIGAIN_06							0x00	0x0A	0x0A
	0x42	AIGAIN_07							0x00	0x0A	0x0A
	0x43	AIGAIN_08							0x00	0x0A	0x0A
	0x44	-							-	-	-
	0x45	-							-	-	-
	0x46	-							-	-	-
	0x47	-							-	-	-
	0x48	-							-	-	-
	0x49	-RESERVED-							0x88	0x88	0x88
	0x4A	-RESERVED-							0xFF	0xFF	0xFF
	0x4B	-RESERVED-							0xAA	0xAA	0xAA
	0x4C	-RESERVED-							0xAA	0xAA	0xAA
	0x4D	-RESERVED-							0xAA	0xAA	0xAA
	0x4E	-RESERVED-							0xAA	0xAA	0xAA
	0x4F	-RESERVED-							0xA1	0xA1	0xA1
	0x50	-							-	-	-
	0x51	-							-	-	-
	0x52	-							-	-	-
	0x53	-							-	-	-
	0x54	-							-	-	-
	0x55	-							-	-	-
	0x56	-							-	-	-
	0x57	-							-	-	-
	0x58	-							-	-	-
	0x59	-							-	-	-
	0x5A	-							-	-	-
	0x5B	-							-	-	-
	0x5C	-							-	-	-
	0x5D	-							-	-	-
	0x5E	-							-	-	-
	0x5F	-							-	-	-

 BANK1 Register(0xA0~0xBF) : MPP


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK1	0xA0								-	-	-
	0xA1								-	-	-
	0xA2								-	-	-
	0xA3								-	-	-
	0xA4								-	-	-
	0xA5								-	-	-
	0xA6								-	-	-
	0xA7								-	-	-
	0xA8								-	-	-
	0xA9								-	-	-
	0xAA								-	-	-
	0xAB								-	-	-
	0xAC								-	-	-
	0xAD								-	-	-
	0xAE								-	-	-
	0xAF								-	-	-
0xB0	MPP_GPIO								0x00	0x00	0x00
0xB1	MPP4_MSB	-RESERVED-				MPP3_MSB	MPP2_MSB	MPP1_MSB	0x00	0x00	0x00
0xB2								IRQ_MSB	0x00	0x00	0x00
0xB3	-RESERVED-								0x00	0x00	0x00
0xB4	-RESERVED-								0x40	0x40	0x40
0xB5	-RESERVED-								0x40	0x40	0x40
0xB6	-RESERVED-								0x40	0x40	0x40
0xB7	-RESERVED-								0x40	0x40	0x40
0xB8	-RESERVED-								0x40	0x40	0x40
0xB9	-RESERVED-								0x40	0x40	0x40
0xBA	-RESERVED-								0x40	0x40	0x40
0xBB	-RESERVED-								0x40	0x40	0x40
0xBC	MPP_SEL2				MPP_SEL1				0x00	0x00	0x00
0xBD	COAX_SEL1				MPP_SEL3				0x00	0x00	0x00
0xBE	COAX_SEL3				COAX_SEL2				0x00	0x00	0x00
0xBF	MPP_SEL4				COAX_SEL4				0x00	0x00	0x00

 BANK1 Register(0xC0~0xDF) : OUTPUT PORT

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0xC0	VPORTA_SEQ2				VPORTA_SEQ1				0x10	0x00	0x00
0xC1	VPORTA_SEQ4				VPORTA_SEQ3				0x10	0x00	0x00
0xC2	VPORTB_SEQ2				VPORTB_SEQ1				0x32	0x11	0x11
0xC3	VPORTB_SEQ4				VPORTB_SEQ3				0x32	0x11	0x11
0xC4	VPORTC_SEQ2				VPORTC_SEQ1				0x10	0x22	0x22
0xC5	VPORTC_SEQ4				VPORTC_SEQ3				0x10	0x22	0x22
0xC6	VPORTD_SEQ2				VPORTD_SEQ1				0x32	0x33	0x33
0xC7	VPORTD_SEQ4				VPORTD_SEQ3				0x32	0x33	0x33
0xC8	CH_OUT_SELB				CH_OUT_SELA				0x22	0x00	0x00
0xC9	CH_OUT_SELD				CH_OUT_SELC				0x22	0x00	0x00
0xCA	VCLK_4_EN	VCLK_3_EN	VCLK_2_EN	VCLK_1_EN	VDO_4_EN	VDO_3_EN	VDO_2_EN	VDO_1_EN	0x00	0xFF	0xFF
0xCB	-RESERVED-								0x00	0x00	0x00
0xCC	-	VCLK_1_SEL			VCLK_1_DLY_SEL				0x60	0x40	0x40
0xCD	-	VCLK_2_SEL			VCLK_2_DLY_SEL				0x60	0x40	0x40
0xCE	-	VCLK_3_SEL			VCLK_3_DLY_SEL				0x60	0x40	0x40
0xCF	-	VCLK_4_SEL			VCLK_4_DLY_SEL				0x60	0x40	0x40
0xD0	DATA_CATCH_2				DATA_CATCH_1				0x00	0x00	0x00
0xD1	DATA_CATCH_4				DATA_CATCH_3				0x00	0x00	0x00
0xD2	-RESERVED-		OUT_DATA_INV			-RESERVED-			0x00	0x00	0x00
0xD3	-										
0xD4	-RESERVED-								0x00	0x00	0x00
0xD5	-							- 0 -	0x00	0x00	0x00
0xD6	-RESERVED-								0x00	0x00	0x00
0xD7	-RESERVED-								0x00	0x00	0x00
0xD8	-RESERVED-								0x00	0x00	0x00
0xD9	-RESERVED-								0x00	0x00	0x00
0xDA	-RESERVED-								0x00	0x00	0x00
0xDB	-RESERVED-								0x00	0x00	0x00
0xDC	-RESERVED-								0x00	0x00	0x00
0xDD	-RESERVED-								0x00	0x00	0x00
0xDE	-RESERVED-								0x00	0x00	0x00
0xDF	-RESERVED-								0x00	0x00	0x00

 BANK2 Register(0x00~0x1F) : MOTION


ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P		
B A N K 2	0x00	-RESERVED-			MOTION_OFF01	-RESERVED-		MOTION_PIC_01	0x03	0x03	0x03		
	0x01	MOD_TSEN_01									0x60	0x60	0x60
	0x02	-RESERVED-			MOTION_OFF02	-RESERVED-		MOTION_PIC_02	0x03	0x03	0x03		
	0x03	MOD_TSEN_02									0x60	0x60	0x60
	0x04	-RESERVED-			MOTION_OFF03	-RESERVED-		MOTION_PIC_03	0x03	0x03	0x03		
	0x05	MOD_TSEN_03									0x60	0x60	0x60
	0x06	-RESERVED-			MOTION_OFF04	-RESERVED-		MOTION_PIC_04	0x03	0x03	0x03		
	0x07	MOD_TSEN_04									0x60	0x60	0x60
	0x08										-	-	-
	0x09										-	-	-
	0x0A										-	-	-
	0x0B										-	-	-
	0x0C										-	-	-
	0x0D										-	-	-
	0x0E										-	-	-
	0x0F										-	-	-
	0x10	MOD_PSEN_01		MOD_PSEN_02		MOD_PSEN_03		MOD_PSEN_04		0x00	0x00	0x00	
	0x11	-RESERVED-									0x00	0x00	0x00
0x12	-RESERVED-			MD_H960_CH4	MD_H960_CH3	MD_H960_CH2	MD_H960_CH1	0x00	0x00	0x00			
0x13	-RESERVED-									0x00	0x00	0x00	
0x14	-RESERVED-									0x00	0xC0	0xC0	
0x15	-RESERVED-									0x00	0x00	0x00	
0x16	-RESERVED-									0x00	0x00	0x00	
0x17	-RESERVED-									0x00	0x00	0x00	
0x18										-	-	-	
0x19										-	-	-	
0x1A										-	-	-	
0x1B										-	-	-	
0x1C										-	-	-	
0x1D										-	-	-	
0x1E										-	-	-	
0x1F										-	-	-	

 **BANK2 Register(0x20~0x3F) : MOTION**

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
BANK2	0x20	CH1_MOD_01	CH1_MOD_02	CH1_MOD_03	CH1_MOD_04	CH1_MOD_05	CH1_MOD_06	CH1_MOD_07	CH1_MOD_08	0xFF	0xFF	0xFF
	0x21	CH1_MOD_09	CH1_MOD_10	CH1_MOD_11	CH1_MOD_12	CH1_MOD_13	CH1_MOD_14	CH1_MOD_15	CH1_MOD_16	0xFF	0xFF	0xFF
	0x22	CH1_MOD_17	CH1_MOD_18	CH1_MOD_19	CH1_MOD_20	CH1_MOD_21	CH1_MOD_22	CH1_MOD_23	CH1_MOD_24	0xFF	0xFF	0xFF
	0x23	CH1_MOD_25	CH1_MOD_26	CH1_MOD_27	CH1_MOD_28	CH1_MOD_29	CH1_MOD_30	CH1_MOD_31	CH1_MOD_32	0xFF	0xFF	0xFF
	0x24	CH1_MOD_33	CH1_MOD_34	CH1_MOD_35	CH1_MOD_36	CH1_MOD_37	CH1_MOD_38	CH1_MOD_39	CH1_MOD_40	0xFF	0xFF	0xFF
	0x25	CH1_MOD_41	CH1_MOD_42	CH1_MOD_43	CH1_MOD_44	CH1_MOD_45	CH1_MOD_46	CH1_MOD_47	CH1_MOD_48	0xFF	0xFF	0xFF
	0x26	CH1_MOD_49	CH1_MOD_50	CH1_MOD_51	CH1_MOD_52	CH1_MOD_53	CH1_MOD_54	CH1_MOD_55	CH1_MOD_56	0xFF	0xFF	0xFF
	0x27	CH1_MOD_57	CH1_MOD_58	CH1_MOD_59	CH1_MOD_60	CH1_MOD_61	CH1_MOD_62	CH1_MOD_63	CH1_MOD_64	0xFF	0xFF	0xFF
	0x28	CH1_MOD_65	CH1_MOD_66	CH1_MOD_67	CH1_MOD_68	CH1_MOD_69	CH1_MOD_70	CH1_MOD_71	CH1_MOD_72	0xFF	0xFF	0xFF
	0x29	CH1_MOD_73	CH1_MOD_74	CH1_MOD_75	CH1_MOD_76	CH1_MOD_77	CH1_MOD_78	CH1_MOD_79	CH1_MOD_80	0xFF	0xFF	0xFF
	0x2A	CH1_MOD_81	CH1_MOD_82	CH1_MOD_83	CH1_MOD_84	CH1_MOD_85	CH1_MOD_86	CH1_MOD_87	CH1_MOD_88	0xFF	0xFF	0xFF
	0x2B	CH1_MOD_89	CH1_MOD_90	CH1_MOD_91	CH1_MOD_92	CH1_MOD_93	CH1_MOD_94	CH1_MOD_95	CH1_MOD_96	0xFF	0xFF	0xFF
	0x2C	CH1_MOD_97	CH1_MOD_98	CH1_MOD_99	CH1_MOD_100	CH1_MOD_101	CH1_MOD_102	CH1_MOD_103	CH1_MOD_104	0xFF	0xFF	0xFF
	0x2D	CH1_MOD_105	CH1_MOD_106	CH1_MOD_107	CH1_MOD_108	CH1_MOD_109	CH1_MOD_110	CH1_MOD_111	CH1_MOD_112	0xFF	0xFF	0xFF
	0x2E	CH1_MOD_113	CH1_MOD_114	CH1_MOD_115	CH1_MOD_116	CH1_MOD_117	CH1_MOD_118	CH1_MOD_119	CH1_MOD_120	0xFF	0xFF	0xFF
	0x2F	CH1_MOD_121	CH1_MOD_122	CH1_MOD_123	CH1_MOD_124	CH1_MOD_125	CH1_MOD_126	CH1_MOD_127	CH1_MOD_128	0xFF	0xFF	0xFF
	0x30	CH1_MOD_129	CH1_MOD_130	CH1_MOD_131	CH1_MOD_132	CH1_MOD_133	CH1_MOD_134	CH1_MOD_135	CH1_MOD_136	0xFF	0xFF	0xFF
	0x31	CH1_MOD_137	CH1_MOD_138	CH1_MOD_139	CH1_MOD_140	CH1_MOD_141	CH1_MOD_142	CH1_MOD_143	CH1_MOD_144	0xFF	0xFF	0xFF
	0x32	CH1_MOD_145	CH1_MOD_146	CH1_MOD_147	CH1_MOD_148	CH1_MOD_149	CH1_MOD_150	CH1_MOD_151	CH1_MOD_152	0xFF	0xFF	0xFF
	0x33	CH1_MOD_153	CH1_MOD_154	CH1_MOD_155	CH1_MOD_156	CH1_MOD_157	CH1_MOD_158	CH1_MOD_159	CH1_MOD_160	0xFF	0xFF	0xFF
	0x34	CH1_MOD_161	CH1_MOD_162	CH1_MOD_163	CH1_MOD_164	CH1_MOD_165	CH1_MOD_166	CH1_MOD_167	CH1_MOD_168	0xFF	0xFF	0xFF
	0x35	CH1_MOD_169	CH1_MOD_170	CH1_MOD_171	CH1_MOD_172	CH1_MOD_173	CH1_MOD_174	CH1_MOD_175	CH1_MOD_176	0xFF	0xFF	0xFF
	0x36	CH1_MOD_177	CH1_MOD_178	CH1_MOD_179	CH1_MOD_180	CH1_MOD_181	CH1_MOD_182	CH1_MOD_183	CH1_MOD_184	0xFF	0xFF	0xFF
	0x37	CH1_MOD_185	CH1_MOD_186	CH1_MOD_187	CH1_MOD_188	CH1_MOD_189	CH1_MOD_190	CH1_MOD_191	CH1_MOD_192	0xFF	0xFF	0xFF
	0x38	CH2_MOD_01	CH2_MOD_02	CH2_MOD_03	CH2_MOD_04	CH2_MOD_05	CH2_MOD_06	CH2_MOD_07	CH2_MOD_08	0xFF	0xFF	0xFF
	0x39	CH2_MOD_09	CH2_MOD_10	CH2_MOD_11	CH2_MOD_12	CH2_MOD_13	CH2_MOD_14	CH2_MOD_15	CH2_MOD_16	0xFF	0xFF	0xFF
	0x3A	CH2_MOD_17	CH2_MOD_18	CH2_MOD_19	CH2_MOD_20	CH2_MOD_21	CH2_MOD_22	CH2_MOD_23	CH2_MOD_24	0xFF	0xFF	0xFF
	0x3B	CH2_MOD_25	CH2_MOD_26	CH2_MOD_27	CH2_MOD_28	CH2_MOD_29	CH2_MOD_30	CH2_MOD_31	CH2_MOD_32	0xFF	0xFF	0xFF
	0x3C	CH2_MOD_33	CH2_MOD_34	CH2_MOD_35	CH2_MOD_36	CH2_MOD_37	CH2_MOD_38	CH2_MOD_39	CH2_MOD_40	0xFF	0xFF	0xFF
	0x3D	CH2_MOD_41	CH2_MOD_42	CH2_MOD_43	CH2_MOD_44	CH2_MOD_45	CH2_MOD_46	CH2_MOD_47	CH2_MOD_48	0xFF	0xFF	0xFF
	0x3E	CH2_MOD_49	CH2_MOD_50	CH2_MOD_51	CH2_MOD_52	CH2_MOD_53	CH2_MOD_54	CH2_MOD_55	CH2_MOD_56	0xFF	0xFF	0xFF
	0x3F	CH2_MOD_57	CH2_MOD_58	CH2_MOD_59	CH2_MOD_60	CH2_MOD_61	CH2_MOD_62	CH2_MOD_63	CH2_MOD_64	0xFF	0xFF	0xFF

BANK2 Register(0x40~0x5F) : MOTION

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
BANK2	0x40	CH2_MOD_65	CH2_MOD_66	CH2_MOD_67	CH2_MOD_68	CH2_MOD_69	CH2_MOD_70	CH2_MOD_71	CH2_MOD_72	0xFF	0xFF	0xFF
	0x41	CH2_MOD_73	CH2_MOD_74	CH2_MOD_75	CH2_MOD_76	CH2_MOD_77	CH2_MOD_78	CH2_MOD_79	CH2_MOD_80	0xFF	0xFF	0xFF
	0x42	CH2_MOD_81	CH2_MOD_82	CH2_MOD_83	CH2_MOD_84	CH2_MOD_85	CH2_MOD_86	CH2_MOD_87	CH2_MOD_88	0xFF	0xFF	0xFF
	0x43	CH2_MOD_89	CH2_MOD_90	CH2_MOD_91	CH2_MOD_92	CH2_MOD_93	CH2_MOD_94	CH2_MOD_95	CH2_MOD_96	0xFF	0xFF	0xFF
	0x44	CH2_MOD_97	CH2_MOD_98	CH2_MOD_99	CH2_MOD_100	CH2_MOD_101	CH2_MOD_102	CH2_MOD_103	CH2_MOD_104	0xFF	0xFF	0xFF
	0x45	CH2_MOD_105	CH2_MOD_106	CH2_MOD_107	CH2_MOD_108	CH2_MOD_109	CH2_MOD_110	CH2_MOD_111	CH2_MOD_112	0xFF	0xFF	0xFF
	0x46	CH2_MOD_113	CH2_MOD_114	CH2_MOD_115	CH2_MOD_116	CH2_MOD_117	CH2_MOD_118	CH2_MOD_119	CH2_MOD_120	0xFF	0xFF	0xFF
	0x47	CH2_MOD_121	CH2_MOD_122	CH2_MOD_123	CH2_MOD_124	CH2_MOD_125	CH2_MOD_126	CH2_MOD_127	CH2_MOD_128	0xFF	0xFF	0xFF
	0x48	CH2_MOD_129	CH2_MOD_130	CH2_MOD_131	CH2_MOD_132	CH2_MOD_133	CH2_MOD_134	CH2_MOD_135	CH2_MOD_136	0xFF	0xFF	0xFF
	0x49	CH2_MOD_137	CH2_MOD_138	CH2_MOD_139	CH2_MOD_140	CH2_MOD_141	CH2_MOD_142	CH2_MOD_143	CH2_MOD_144	0xFF	0xFF	0xFF
	0x4A	CH2_MOD_145	CH2_MOD_146	CH2_MOD_147	CH2_MOD_148	CH2_MOD_149	CH2_MOD_150	CH2_MOD_151	CH2_MOD_152	0xFF	0xFF	0xFF
	0x4B	CH2_MOD_153	CH2_MOD_154	CH2_MOD_155	CH2_MOD_156	CH2_MOD_157	CH2_MOD_158	CH2_MOD_159	CH2_MOD_160	0xFF	0xFF	0xFF
	0x4C	CH2_MOD_161	CH2_MOD_162	CH2_MOD_163	CH2_MOD_164	CH2_MOD_165	CH2_MOD_166	CH2_MOD_167	CH2_MOD_168	0xFF	0xFF	0xFF
	0x4D	CH2_MOD_169	CH2_MOD_170	CH2_MOD_171	CH2_MOD_172	CH2_MOD_173	CH2_MOD_174	CH2_MOD_175	CH2_MOD_176	0xFF	0xFF	0xFF
	0x4E	CH2_MOD_177	CH2_MOD_178	CH2_MOD_179	CH2_MOD_180	CH2_MOD_181	CH2_MOD_182	CH2_MOD_183	CH2_MOD_184	0xFF	0xFF	0xFF
	0x4F	CH2_MOD_185	CH2_MOD_186	CH2_MOD_187	CH2_MOD_188	CH2_MOD_189	CH2_MOD_190	CH2_MOD_191	CH2_MOD_192	0xFF	0xFF	0xFF
	0x50	CH3_MOD_01	CH3_MOD_02	CH3_MOD_03	CH3_MOD_04	CH3_MOD_05	CH3_MOD_06	CH3_MOD_07	CH3_MOD_08	0xFF	0xFF	0xFF
	0x51	CH3_MOD_09	CH3_MOD_10	CH3_MOD_11	CH3_MOD_12	CH3_MOD_13	CH3_MOD_14	CH3_MOD_15	CH3_MOD_16	0xFF	0xFF	0xFF
	0x52	CH3_MOD_17	CH3_MOD_18	CH3_MOD_19	CH3_MOD_20	CH3_MOD_21	CH3_MOD_22	CH3_MOD_23	CH3_MOD_24	0xFF	0xFF	0xFF
	0x53	CH3_MOD_25	CH3_MOD_26	CH3_MOD_27	CH3_MOD_28	CH3_MOD_29	CH3_MOD_30	CH3_MOD_31	CH3_MOD_32	0xFF	0xFF	0xFF
0x54	CH3_MOD_33	CH3_MOD_34	CH3_MOD_35	CH3_MOD_36	CH3_MOD_37	CH3_MOD_38	CH3_MOD_39	CH3_MOD_40	0xFF	0xFF	0xFF	
0x55	CH3_MOD_41	CH3_MOD_42	CH3_MOD_43	CH3_MOD_44	CH3_MOD_45	CH3_MOD_46	CH3_MOD_47	CH3_MOD_48	0xFF	0xFF	0xFF	
0x56	CH3_MOD_49	CH3_MOD_50	CH3_MOD_51	CH3_MOD_52	CH3_MOD_53	CH3_MOD_54	CH3_MOD_55	CH3_MOD_56	0xFF	0xFF	0xFF	
0x57	CH3_MOD_57	CH3_MOD_58	CH3_MOD_59	CH3_MOD_60	CH3_MOD_61	CH3_MOD_62	CH3_MOD_63	CH3_MOD_64	0xFF	0xFF	0xFF	
0x58	CH3_MOD_65	CH3_MOD_66	CH3_MOD_67	CH3_MOD_68	CH3_MOD_69	CH3_MOD_70	CH3_MOD_71	CH3_MOD_72	0xFF	0xFF	0xFF	
0x59	CH3_MOD_73	CH3_MOD_74	CH3_MOD_75	CH3_MOD_76	CH3_MOD_77	CH3_MOD_78	CH3_MOD_79	CH3_MOD_80	0xFF	0xFF	0xFF	
0x5A	CH3_MOD_81	CH3_MOD_82	CH3_MOD_83	CH3_MOD_84	CH3_MOD_85	CH3_MOD_86	CH3_MOD_87	CH3_MOD_88	0xFF	0xFF	0xFF	
0x5B	CH3_MOD_89	CH3_MOD_90	CH3_MOD_91	CH3_MOD_92	CH3_MOD_93	CH3_MOD_94	CH3_MOD_95	CH3_MOD_96	0xFF	0xFF	0xFF	
0x5C	CH3_MOD_97	CH3_MOD_98	CH3_MOD_99	CH3_MOD_100	CH3_MOD_101	CH3_MOD_102	CH3_MOD_103	CH3_MOD_104	0xFF	0xFF	0xFF	
0x5D	CH3_MOD_105	CH3_MOD_106	CH3_MOD_107	CH3_MOD_108	CH3_MOD_109	CH3_MOD_110	CH3_MOD_111	CH3_MOD_112	0xFF	0xFF	0xFF	
0x5E	CH3_MOD_113	CH3_MOD_114	CH3_MOD_115	CH3_MOD_116	CH3_MOD_117	CH3_MOD_118	CH3_MOD_119	CH3_MOD_120	0xFF	0xFF	0xFF	
0x5F	CH3_MOD_121	CH3_MOD_122	CH3_MOD_123	CH3_MOD_124	CH3_MOD_125	CH3_MOD_126	CH3_MOD_127	CH3_MOD_128	0xFF	0xFF	0xFF	

 **BANK2 Register(0x60~0x7F) : MOTION**

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
BANK2	0x60	CH3_MOD_129	CH3_MOD_130	CH3_MOD_131	CH3_MOD_132	CH3_MOD_133	CH3_MOD_134	CH3_MOD_135	CH3_MOD_136	0xFF	0xFF	0xFF
	0x61	CH3_MOD_137	CH3_MOD_138	CH3_MOD_139	CH3_MOD_140	CH3_MOD_141	CH3_MOD_142	CH3_MOD_143	CH3_MOD_144	0xFF	0xFF	0xFF
	0x62	CH3_MOD_145	CH3_MOD_146	CH3_MOD_147	CH3_MOD_148	CH3_MOD_149	CH3_MOD_150	CH3_MOD_151	CH3_MOD_152	0xFF	0xFF	0xFF
	0x63	CH3_MOD_153	CH3_MOD_154	CH3_MOD_155	CH3_MOD_156	CH3_MOD_157	CH3_MOD_158	CH3_MOD_159	CH3_MOD_160	0xFF	0xFF	0xFF
	0x64	CH3_MOD_161	CH3_MOD_162	CH3_MOD_163	CH3_MOD_164	CH3_MOD_165	CH3_MOD_166	CH3_MOD_167	CH3_MOD_168	0xFF	0xFF	0xFF
	0x65	CH3_MOD_169	CH3_MOD_170	CH3_MOD_171	CH3_MOD_172	CH3_MOD_173	CH3_MOD_174	CH3_MOD_175	CH3_MOD_176	0xFF	0xFF	0xFF
	0x66	CH3_MOD_177	CH3_MOD_178	CH3_MOD_179	CH3_MOD_180	CH3_MOD_181	CH3_MOD_182	CH3_MOD_183	CH3_MOD_184	0xFF	0xFF	0xFF
	0x67	CH3_MOD_185	CH3_MOD_186	CH3_MOD_187	CH3_MOD_188	CH3_MOD_189	CH3_MOD_190	CH3_MOD_191	CH3_MOD_192	0xFF	0xFF	0xFF
	0x68	CH4_MOD_01	CH4_MOD_02	CH4_MOD_03	CH4_MOD_04	CH4_MOD_05	CH4_MOD_06	CH4_MOD_07	CH4_MOD_08	0xFF	0xFF	0xFF
	0x69	CH4_MOD_09	CH4_MOD_10	CH4_MOD_11	CH4_MOD_12	CH4_MOD_13	CH4_MOD_14	CH4_MOD_15	CH4_MOD_16	0xFF	0xFF	0xFF
	0x6A	CH4_MOD_17	CH4_MOD_18	CH4_MOD_19	CH4_MOD_20	CH4_MOD_21	CH4_MOD_22	CH4_MOD_23	CH4_MOD_24	0xFF	0xFF	0xFF
	0x6B	CH4_MOD_25	CH4_MOD_26	CH4_MOD_27	CH4_MOD_28	CH4_MOD_29	CH4_MOD_30	CH4_MOD_31	CH4_MOD_32	0xFF	0xFF	0xFF
	0x6C	CH4_MOD_33	CH4_MOD_34	CH4_MOD_35	CH4_MOD_36	CH4_MOD_37	CH4_MOD_38	CH4_MOD_39	CH4_MOD_40	0xFF	0xFF	0xFF
	0x6D	CH4_MOD_41	CH4_MOD_42	CH4_MOD_43	CH4_MOD_44	CH4_MOD_45	CH4_MOD_46	CH4_MOD_47	CH4_MOD_48	0xFF	0xFF	0xFF
	0x6E	CH4_MOD_49	CH4_MOD_50	CH4_MOD_51	CH4_MOD_52	CH4_MOD_53	CH4_MOD_54	CH4_MOD_55	CH4_MOD_56	0xFF	0xFF	0xFF
	0x6F	CH4_MOD_57	CH4_MOD_58	CH4_MOD_59	CH4_MOD_60	CH4_MOD_61	CH4_MOD_62	CH4_MOD_63	CH4_MOD_64	0xFF	0xFF	0xFF
	0x70	CH4_MOD_65	CH4_MOD_66	CH4_MOD_67	CH4_MOD_68	CH4_MOD_69	CH4_MOD_70	CH4_MOD_71	CH4_MOD_72	0xFF	0xFF	0xFF
	0x71	CH4_MOD_73	CH4_MOD_74	CH4_MOD_75	CH4_MOD_76	CH4_MOD_77	CH4_MOD_78	CH4_MOD_79	CH4_MOD_80	0xFF	0xFF	0xFF
	0x72	CH4_MOD_81	CH4_MOD_82	CH4_MOD_83	CH4_MOD_84	CH4_MOD_85	CH4_MOD_86	CH4_MOD_87	CH4_MOD_88	0xFF	0xFF	0xFF
	0x73	CH4_MOD_89	CH4_MOD_90	CH4_MOD_91	CH4_MOD_92	CH4_MOD_93	CH4_MOD_94	CH4_MOD_95	CH4_MOD_96	0xFF	0xFF	0xFF
	0x74	CH4_MOD_97	CH4_MOD_98	CH4_MOD_99	CH4_MOD_100	CH4_MOD_101	CH4_MOD_102	CH4_MOD_103	CH4_MOD_104	0xFF	0xFF	0xFF
	0x75	CH4_MOD_105	CH4_MOD_106	CH4_MOD_107	CH4_MOD_108	CH4_MOD_109	CH4_MOD_110	CH4_MOD_111	CH4_MOD_112	0xFF	0xFF	0xFF
	0x76	CH4_MOD_113	CH4_MOD_114	CH4_MOD_115	CH4_MOD_116	CH4_MOD_117	CH4_MOD_118	CH4_MOD_119	CH4_MOD_120	0xFF	0xFF	0xFF
	0x77	CH4_MOD_121	CH4_MOD_122	CH4_MOD_123	CH4_MOD_124	CH4_MOD_125	CH4_MOD_126	CH4_MOD_127	CH4_MOD_128	0xFF	0xFF	0xFF
	0x78	CH4_MOD_129	CH4_MOD_130	CH4_MOD_131	CH4_MOD_132	CH4_MOD_133	CH4_MOD_134	CH4_MOD_135	CH4_MOD_136	0xFF	0xFF	0xFF
	0x79	CH4_MOD_137	CH4_MOD_138	CH4_MOD_139	CH4_MOD_140	CH4_MOD_141	CH4_MOD_142	CH4_MOD_143	CH4_MOD_144	0xFF	0xFF	0xFF
	0x7A	CH4_MOD_145	CH4_MOD_146	CH4_MOD_147	CH4_MOD_148	CH4_MOD_149	CH4_MOD_150	CH4_MOD_151	CH4_MOD_152	0xFF	0xFF	0xFF
	0x7B	CH4_MOD_153	CH4_MOD_154	CH4_MOD_155	CH4_MOD_156	CH4_MOD_157	CH4_MOD_158	CH4_MOD_159	CH4_MOD_160	0xFF	0xFF	0xFF
	0x7C	CH4_MOD_161	CH4_MOD_162	CH4_MOD_163	CH4_MOD_164	CH4_MOD_165	CH4_MOD_166	CH4_MOD_167	CH4_MOD_168	0xFF	0xFF	0xFF
	0x7D	CH4_MOD_169	CH4_MOD_170	CH4_MOD_171	CH4_MOD_172	CH4_MOD_173	CH4_MOD_174	CH4_MOD_175	CH4_MOD_176	0xFF	0xFF	0xFF
0x7E	CH4_MOD_177	CH4_MOD_178	CH4_MOD_179	CH4_MOD_180	CH4_MOD_181	CH4_MOD_182	CH4_MOD_183	CH4_MOD_184	0xFF	0xFF	0xFF	
0x7F	CH4_MOD_185	CH4_MOD_186	CH4_MOD_187	CH4_MOD_188	CH4_MOD_189	CH4_MOD_190	CH4_MOD_191	CH4_MOD_192	0xFF	0xFF	0xFF	

Reserved BANK2 Register(0x80~0xBF)

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
B A N K 2	0x80	Def	0xA0	0xA0	0xA0	0xA0	-	-	-	-	0xA0	0xA0	0xA0	0xA0	-	-	-	-
		30P	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-
		25P	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-
	0x90	Def	0x18	0x70	0x20	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	-
		30P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	-
		25P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Read	Read	Read	Read	-	-	-	-
	0xA0	Def	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-
		30P	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-
		25P	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-
	0xB0	Def	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-
		30P	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-
		25P	0x00	0x00	0x00	0x00	-	-	-	-	0x00	0x00	0x00	0x00	-	-	-	-

 BANK3 Register(0x00~0x1F) : COAXIAL CH1

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x00	CH1_BAUD								0x0E	0x0E	0x0E
0x01	-								-	-	-
0x02	CH1_PELCO_BAUD								0x18	0x0D	0x0D
0x03	CH1_BL_TXST[7:0]								0x18	0x0E	0x0E
0x04	-			CH1_BL_TXST[11:8]					0x00	0x00	0x00
0x05	-			CH1_ACT_LEN					0x00	0x00	0x00
0x06	-			-					-	-	-
0x07	CH1_PELCO_TXST[7:0]								0x09	0x0E	0x0E
0x08	-			CH1_PELCO_TXST[11:8]					0x00	0x00	0x00
0x09	-		CH1_COAX_SW_RST	CH1_CNT_MODE	-			CH1_TX_START	0x00	0x08	0x08
0x0A	-		CH1_TX_BYTE_LENGTH					0x03	0x03	0x03	
0x0B	CH1_PELCO_8BIT	-		CH1_LINE_8BIT	-			CH1_PACKET_MODE	0x10	0x10	0x10
0x0C	-							CH1_PELCO_CTEN	0x00	0x00	0x00
0x0D	CH1_BL_HSP[7:0]								0x50	0x30	0x30
0x0E	-			CH1_BL_HSP[11:8]					0x00	0x04	0x04
0x0F	-							CH1_PELCO_SHOT	0x00	0x00	0x00
0x10	CH1_TX_DATA_01								0x02	0x00	0x00
0x11	CH1_TX_DATA_02								0x00	0x10	0x10
0x12	CH1_TX_DATA_03								0x00	0x18	0x18
0x13	CH1_TX_DATA_04								0x00	0xFF	0xFF
0x14	CH1_TX_DATA_05								0xAA	0xAA	0xAA
0x15	CH1_TX_DATA_06								0x3C	0x3C	0x3C
0x16	CH1_TX_DATA_07								0xFF	0xFF	0xFF
0x17	CH1_TX_DATA_08								0xFF	0xFF	0xFF
0x18	CH1_TX_DATA_09								0xAA	0xAA	0xAA
0x19	CH1_TX_DATA_10								0x1B	0x1B	0x1B
0x1A	CH1_TX_DATA_11								0x00	0x00	0x00
0x1B	CH1_TX_DATA_12								0x00	0x00	0x00
0x1C	CH1_TX_DATA_13								0xAA	0xAA	0xAA
0x1D	CH1_TX_DATA_14								0x3B	0x3B	0x3B
0x1E	CH1_TX_DATA_15								0x00	0x00	0x00
0x1F	CH1_TX_DATA_16								0x00	0x00	0x00

 BANK3 Register(0x20~0x3F) : COAXIAL CH1

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x20	CH1_PELCO_TXDAT_01								0x00	0x00	0x00
0x21	CH1_PELCO_TXDAT_02								0x00	0x00	0x00
0x22	CH1_PELCO_TXDAT_03								0x00	0x00	0x00
0x23	CH1_PELCO_TXDAT_04								0x00	0x00	0x00
0x24	-								-	-	-
0x25	-								-	-	-
0x26	-								-	-	-
0x27	-								-	-	-
0x28	-								-	-	-
0x29	-								-	-	-
0x2A	-								-	-	-
0x2B	-								-	-	-
0x2C	CH1_VSO_INV								0x00	0x00	0x00
0x2D	CH1_HSO_INV								0x00	0x00	0x00
0x2E	-								-	-	-
0x2F	CH1_Even_line_modification								0x00	0x00	0x00
0x30	-								-	-	-
0x31	-								-	-	-
0x32	-								-	-	-
0x33	-								-	-	-
0x34	-								-	-	-
0x35	-								-	-	-
0x36	-								-	-	-
0x37	-								-	-	-
0x38	-								-	-	-
0x39	-								-	-	-
0x3A	-							CH1_CLEAN	0x00	0x00	0x00
0x3B	CH1_AUTO	-	CH1_CMD_LIST						0x00	0x00	0x00
0x3C	-								-	-	-
0x3D	-								-	-	-
0x3E	-								-	-	-
0x3F	-								-	-	-

 BANK3 Register(0x40~0x5F) : COAXIAL CH1

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
BANK3	0x40	CH1_ORIGIN_A_00								R	R	R
	0x41	CH1_ORIGIN_A_01								R	R	R
	0x42	CH1_ORIGIN_A_02								R	R	R
	0x43	CH1_ORIGIN_A_03								R	R	R
	0x44	CH1_ORIGIN_A_04								R	R	R
	0x45	CH1_ORIGIN_A_05								R	R	R
	0x46	CH1_ORIGIN_B_00								R	R	R
	0x47	CH1_ORIGIN_B_01								R	R	R
	0x48	CH1_ORIGIN_B_02								R	R	R
	0x49	CH1_ORIGIN_B_03								R	R	R
	0x4A	CH1_ORIGIN_B_04								R	R	R
	0x4B	CH1_ORIGIN_B_05								R	R	R
	0x4C	-								-	-	-
	0x4D	-								-	-	-
	0x4E	-								-	-	-
	0x4F	-								-	-	-
	0x50	CH1_ORIGIN_C_00								R	R	R
	0x51	CH1_ORIGIN_C_01								R	R	R
	0x52	CH1_ORIGIN_C_02								R	R	R
	0x53	CH1_ORIGIN_C_03								R	R	R
	0x54	CH1_ORIGIN_C_04								R	R	R
	0x55	CH1_ORIGIN_C_05								R	R	R
	0x56	CH1_ORIGIN_D_00								R	R	R
	0x57	CH1_ORIGIN_D_01								R	R	R
	0x58	CH1_ORIGIN_D_02								R	R	R
	0x59	CH1_ORIGIN_D_03								R	R	R
	0x5A	CH1_ORIGIN_D_04								R	R	R
	0x5B	CH1_ORIGIN_D_05								R	R	R
	0x5C	-							CH1_RX_DONE	R	R	R
	0x5D	CH1_RX_COAX_DUTY								R	R	R
	0x5E	-								-	-	-
	0x5F	-								-	-	-

 BANK3 Register(0x60~0x7F) : COAXIAL CH1

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
0x60	CH1_DEVICE_ID								0x48	0x48	0x48	
0x61	-								-	-	-	
0x62	CH1_RX_AREA								0x06	0x06	0x06	
0x63	-		CH1_DELAY_ON		-			CH1_COMM_ON	0x01	0x01	0x01	
0x64	CH1_DELAY_CNT								0x00	0x00	0x00	
0x65	-							CH1_MSB	0x01	0x01	0x01	
0x66	CH1_A_DUTY_ON	-								0x80	0x80	0x80
0x67	-							CH1_INT_MODE	0x01	0x01	0x01	
0x68	CH1_RX_SZ				-				0x50	0x50	0x50	
0x69	CH1_M_DUTY								0x00	0x00	0x00	
0x6A	CH1_RX_START_POSITION								0x00	0x00	0x00	
0x6B	-								-	-	-	
0x6C	-								-	-	-	
0x6D	-								-	-	-	
0x6E	-								-	-	-	
0x6F	-								-	-	-	
0x70	CH1_PELCO16_00 [7:0]								R	R	R	
0x71	CH1_PELCO16_00 [15:8]								R	R	R	
0x72	CH1_PELCO16_01 [7:0]								R	R	R	
0x73	CH1_PELCO16_01 [15:8]								R	R	R	
0x74	-								-	-	-	
0x75	-								-	-	-	
0x76	-								-	-	-	
0x77	-								-	-	-	
0x78	CH1_PELCO8_0								R	R	R	
0x79	CH1_PELCO8_1								R	R	R	
0x7A	CH1_PELCO8_2								R	R	R	
0x7B	CH1_PELCO8_3								R	R	R	
0x7C	-								-	-	-	
0x7D	-								-	-	-	
0x7E	-								-	-	-	
0x7F	-								-	-	-	

 BANK3 Register(0x80~0x9F) : COAXIAL CH2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x80	CH2_BAUD								0x37	0x37	0x37
0x81	-								-	-	-
0x82	CH2_PELCO_BAUD								0x1B	0x1B	0x1B
0x83	CH2_BL_TXST[7:0]								0x05	0x05	0x05
0x84	-			CH2_BL_TXST[11:8]					0x00	0x00	0x00
0x85	-			CH2_ACT_LEN					0x00	0x00	0x00
0x86	-								-	-	-
0x87	CH2_PELCO_TXST[7:0]								0x09	0x09	0x09
0x88	-			CH2_PELCO_TXST[11:8]					0x00	0x00	0x00
0x89	-			CH2_COAX_SW_RST	CH2_CNT_MODE	-		CH2_TX_START	0x00	0x00	0x00
0x8A	-			CH2_TX_BYTE_LENGTH					0x08	0x08	0x08
0x8B	CH2_PELCO_8BIT	-		CH2_LINE_8BIT	-			CH2_PACKET_MODE	0x06	0x06	0x06
0x8C	-							CH2_PELCO_CTEN	0x00	0x00	0x00
0x8D	CH2_BL_HSP[7:0]								0x46	0x46	0x46
0x8E	-			CH2_BL_HSP[11:8]					0x00	0x00	0x00
0x8F	-							CH2_PELCO_SHOT	0x00	0x00	0x00
0x90	CH2_TX_DATA_01								0xA0	0xAA	0xAA
0x91	CH2_TX_DATA_02								0xA1	0x1C	0x1C
0x92	CH2_TX_DATA_03								0xA2	0x18	0x18
0x93	CH2_TX_DATA_04								0xA3	0xFF	0xFF
0x94	CH2_TX_DATA_05								0xA4	0xAA	0xAA
0x95	CH2_TX_DATA_06								0xA5	0x3C	0x3C
0x96	CH2_TX_DATA_07								0xA6	0xFF	0xFF
0x97	CH2_TX_DATA_08								0xA7	0xFF	0xFF
0x98	CH2_TX_DATA_09								0xA8	0xAA	0xAA
0x99	CH2_TX_DATA_10								0xA9	0x1B	0x1B
0x9A	CH2_TX_DATA_11								0xAA	0x00	0x00
0x9B	CH2_TX_DATA_12								0xAB	0x00	0x00
0x9C	CH2_TX_DATA_13								0xAC	0xAA	0xAA
0x9D	CH2_TX_DATA_14								0xAD	0x3B	0x3B
0x9E	CH2_TX_DATA_15								0xAE	0x00	0x00
0x9F	CH2_TX_DATA_16								0xAF	0x00	0x00

 BANK3 Register(0xA0~0xBF) : COAXIAL CH2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0xA0	CH2_PELCO_TXDAT_01								0xFF	0x00	0x00
0xA1	CH2_PELCO_TXDAT_02								0x00	0x00	0x00
0xA2	CH2_PELCO_TXDAT_03								0xFF	0x00	0x00
0xA3	CH2_PELCO_TXDAT_04								0x00	0x00	0x00
0xA4	-								-	-	-
0xA5	-								-	-	-
0xA6	-								-	-	-
0xA7	-								-	-	-
0xA8	-								-	-	-
0xA9	-								-	-	-
0xAA	-								-	-	-
0xAB	-								-	-	-
0xAC	CH2_VSO_INV								0x00	0x00	0x00
0xAD	CH2_HSO_INV								0x00	0x00	0x00
0xAE	-								-	-	-
0xAF	CH2_Even_line_modification								0x01	0x01	0x01
0xB0	-								-	-	-
0xB1	-								-	-	-
0xB2	-								-	-	-
0xB3	-								-	-	-
0xB4	-								-	-	-
0xB5	-								-	-	-
0xB6	-								-	-	-
0xB7	-								-	-	-
0xB8	-								-	-	-
0xB9	-								-	-	-
0xBA	-							CH2_CLEAN	0x00	0x00	0x00
0xBB	CH2_AUTO	-	CH2_CMD_LIST						0x00	0x00	0x00
0xBC	-								-	-	-
0xBD	-								-	-	-
0xBE	-								-	-	-
0xBF	-								-	-	-

 BANK3 Register(0xC0~0xDF) : COAXIAL CH2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
BANK3	0xC0	CH2_ORIGIN_A_00								R	R	R
	0xC1	CH2_ORIGIN_A_01								R	R	R
	0xC2	CH2_ORIGIN_A_02								R	R	R
	0xC3	CH2_ORIGIN_A_03								R	R	R
	0xC4	CH2_ORIGIN_A_04								R	R	R
	0xC5	CH2_ORIGIN_A_05								R	R	R
	0xC6	CH2_ORIGIN_B_00								R	R	R
	0xC7	CH2_ORIGIN_B_01								R	R	R
	0xC8	CH2_ORIGIN_B_02								R	R	R
	0xC9	CH2_ORIGIN_B_03								R	R	R
	0xCA	CH2_ORIGIN_B_04								R	R	R
	0xCB	CH2_ORIGIN_B_05								R	R	R
	0xCC	-								-	-	-
	0xCD	-								-	-	-
	0xCE	-								-	-	-
	0xCF	-								-	-	-
	0xD0	CH2_ORIGIN_C_00								R	R	R
	0xD1	CH2_ORIGIN_C_01								R	R	R
	0xD2	CH2_ORIGIN_C_02								R	R	R
	0xD3	CH2_ORIGIN_C_03								R	R	R
	0xD4	CH2_ORIGIN_C_04								R	R	R
	0xD5	CH2_ORIGIN_C_05								R	R	R
	0xD6	CH2_ORIGIN_D_00								R	R	R
	0xD7	CH2_ORIGIN_D_01								R	R	R
	0xD8	CH2_ORIGIN_D_02								R	R	R
	0xD9	CH2_ORIGIN_D_03								R	R	R
	0xDA	CH2_ORIGIN_D_04								R	R	R
	0xDB	CH2_ORIGIN_D_05								R	R	R
	0xDC	-							CH2_RX_DONE	R	R	R
	0xDD	CH2_RX_COAX_DUTY								R	R	R
	0xDE	-								-	-	-
	0xDF	-								-	-	-

 BANK3 Register(0xE0~0xFF) : COAXIAL CH2

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0xE0	CH2_DEVICE_ID								0x48	0x48	0x48
0xE1	-								-	-	-
0xE2	CH2_RX_AREA								0x06	0x06	0x06
0xE3	-		CH2_DELAY_ON		-		CH2_COMM_ON		0x01	0x01	0x01
0xE4	CH2_DELAY_CNT								0x00	0x00	0x00
0xE5	-							CH2_MSB	0x01	0x01	0x01
0xE6	CH2_A_DUTY_ON	-							0x80	0x80	0x80
0xE7	-							CH2_INT_MODE	0x01	0x01	0x01
0xE8	CH2_RX_SZ				-			0x50	0x50	0x50	
0xE9	CH2_M_DUTY								0x00	0x00	0x00
0xEA	CH2_RX_START_POSITION								0x00	0x00	0x00
0xEB	-								-	-	-
0xEC	-								-	-	-
0xED	-								-	-	-
0xEE	-								-	-	-
0xEF	-								-	-	-
0xF0	CH2_PELCO16_00_A								R	R	R
0xF1	CH2_PELCO16_00_B								R	R	R
0xF2	CH2_PELCO16_01_A								R	R	R
0xF3	CH2_PELCO16_02_B								R	R	R
0xF4	-								-	-	-
0xF5	-								-	-	-
0xF6	-								-	-	-
0xF7	-								-	-	-
0xF8	CH2_PELCO8_0								R	R	R
0xF9	CH2_PELCO8_1								R	R	R
0xFA	CH2_PELCO8_2								R	R	R
0xFB	CH2_PELCO8_3								R	R	R
0xFC	-								-	-	-
0xFD	-								-	-	-
0xFE	-								-	-	-
0xFF	-								-	-	-

 BANK4 Register(0x00~0x1F) : COAXIAL CH3

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x00	CH3_BAUD								0x0E	0x0E	0x0E
0x01	-								-	-	-
0x02	CH3_PELCO_BAUD								0x18	0x1B	0x1B
0x03	CH3_BL_TXST[7:0]								0x18	0x18	0x18
0x04	-			CH3_BL_TXST[11:8]					0x00	0x00	0x00
0x05	-			CH3_ACT_LEN					0x00	0x00	0x00
0x06	-								-	-	-
0x07	CH3_PELCO_TXST[7:0]								0x09	0x09	0x09
0x08	-			CH3_PELCO_TXST[11:8]					0x00	0x00	0x00
0x09	-			CH3_COAX_SW_RST	CH3_CNT_MODE	-		CH3_TX_START	0x00	0x00	0x00
0x0A	-			CH3_TX_BYTE_LENGTH					0x03	0x03	0x03
0x0B	CH3_PELCO_8BIT	-		CH3_LINE_8BIT	-			CH3_PACKET_MODE	0x10	0x10	0x10
0x0C	-							CH3_PELCO_CTEN	0x00	0x00	0x00
0x0D	CH3_BL_HSP[7:0]								0x50	0x50	0x50
0x0E	-			CH3_BL_HSP[11:8]					0x00	0x00	0x00
0x0F	-							CH3_PELCO_SHOT	0x00	0x00	0x00
0x10	CH3_TX_DATA_01								0x02	0xAA	0xAA
0x11	CH3_TX_DATA_02								0x00	0x1C	0x1C
0x12	CH3_TX_DATA_03								0x00	0x18	0x18
0x13	CH3_TX_DATA_04								0x00	0xFF	0xFF
0x14	CH3_TX_DATA_05								0xAA	0xAA	0xAA
0x15	CH3_TX_DATA_06								0x3C	0x3C	0x3C
0x16	CH3_TX_DATA_07								0xFF	0xFF	0xFF
0x17	CH3_TX_DATA_08								0xFF	0xFF	0xFF
0x18	CH3_TX_DATA_09								0xAA	0xAA	0xAA
0x19	CH3_TX_DATA_10								0x1B	0x1B	0x1B
0x1A	CH3_TX_DATA_11								0x00	0x00	0x00
0x1B	CH3_TX_DATA_12								0x00	0x00	0x00
0x1C	CH3_TX_DATA_13								0xAA	0xAA	0xAA
0x1D	CH3_TX_DATA_14								0x3B	0x3B	0x3B
0x1E	CH3_TX_DATA_15								0x00	0x00	0x00
0x1F	CH3_TX_DATA_16								0x00	0x00	0x00

 BANK4 Register(0x20~0x3F) : COAXIAL CH3

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x20	CH3_PELCO_TXDAT_01								0x00	0x00	0x00
0x21	CH3_PELCO_TXDAT_02								0x00	0x00	0x00
0x22	CH3_PELC O_TXDAT_03								0x00	0x00	0x00
0x23	CH3_PELCO_TXDAT_04								0x00	0x00	0x00
0x24	-								-	-	-
0x25	-								-	-	-
0x26	-								-	-	-
0x27	-								-	-	-
0x28	-								-	-	-
0x29	-								-	-	-
0x2A	-								-	-	-
0x2B	-								-	-	-
0x2C	CH3_VSO_INV								0x00	0x00	0x00
0x2D	CH3_HSO_INV								0x00	0x00	0x00
0x2E	-								-	-	-
0x2F	CH3_Hidden_Even_line_modification								0x00	0x00	0x00
0x30	-								-	-	-
0x31	-								-	-	-
0x32	-								-	-	-
0x33	-								-	-	-
0x34	-								-	-	-
0x35	-								-	-	-
0x36	-								-	-	-
0x37	-								-	-	-
0x38	-								-	-	-
0x39	-								-	-	-
0x3A	-							CH3_CLEAN	0x00	0x00	0x00
0x3B	CH3_AUTO	-		CH3_CMD_LIST					0x00	0x00	0x00
0x3C	-								-	-	-
0x3D	-								-	-	-
0x3E	-								-	-	-
0x3F	-								-	-	-

 BANK4 Register(0x40~0x5F) : COAXIAL CH3

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
B A N K 4	0x40	CH3_ORIGIN_A_00								R	R	R
	0x41	CH3_ORIGIN_A_01								R	R	R
	0x42	CH3_ORIGIN_A_02								R	R	R
	0x43	CH3_ORIGIN_A_03								R	R	R
	0x44	CH3_ORIGIN_A_04								R	R	R
	0x45	CH3_ORIGIN_A_05								R	R	R
	0x46	CH3_ORIGIN_B_00								R	R	R
	0x47	CH3_ORIGIN_B_01								R	R	R
	0x48	CH3_ORIGIN_B_02								R	R	R
	0x49	CH3_ORIGIN_B_03								R	R	R
	0x4A	CH3_ORIGIN_B_04								R	R	R
	0x4B	CH3_ORIGIN_B_05								R	R	R
	0x4C	-								-	-	-
	0x4D	-								-	-	-
	0x4E	-								-	-	-
	0x4F	-								-	-	-
	0x50	CH3_ORIGIN_C_00								R	R	R
	0x51	CH3_ORIGIN_C_01								R	R	R
	0x52	CH3_ORIGIN_C_02								R	R	R
	0x53	CH3_ORIGIN_C_03								R	R	R
	0x54	CH3_ORIGIN_C_04								R	R	R
	0x55	CH3_ORIGIN_C_05								R	R	R
	0x56	CH3_ORIGIN_D_00								R	R	R
	0x57	CH3_ORIGIN_D_01								R	R	R
	0x58	CH3_ORIGIN_D_02								R	R	R
	0x59	CH3_ORIGIN_D_03								R	R	R
	0x5A	CH3_ORIGIN_D_04								R	R	R
	0x5B	CH3_ORIGIN_D_05								R	R	R
	0x5C	-							CH3_RX_DONE	R	R	R
	0x5D	CH3_RX_COAX_DUTY								R	R	R
	0x5E	-								-	-	-
	0x5F	-								-	-	-

 BANK4 Register(0x60~0x7F) : COAXIAL CH3

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
0x60	CH3_DEVICE_ID								0x48	0x48	0x48	
0x61	-								-	-	-	
0x62	CH3_RX_AREA								0x06	0x06	0x06	
0x63	-		CH3_DELAY_ON		-		CH3_COMM_ON		0x01	0x01	0x01	
0x64	CH3_DELAY_CNT								0x00	0x00	0x00	
0x65	-								CH3_MSB	0x01	0x01	0x01
0x66	CH3_A_DUTY_ON	-								0x80	0x80	0x80
0x67	-								CH3_INT_MODE	0x01	0x01	0x01
0x68	CH3_RX_SZ				-				0x50	0x50	0x50	
0x69	CH3_M_DUTY								0x00	0x00	0x00	
0x6A	CH3_RX_START_POSITION								0x00	0x00	0x00	
0x6B	-								-	-	-	
0x6C	-								-	-	-	
0x6D	-								-	-	-	
0x6E	-								-	-	-	
0x6F	-								-	-	-	
0x70	CH3_PELCO16_00 [7:0]								R	R	R	
0x71	CH3_PELCO16_00 [15:8]								R	R	R	
0x72	CH3_PELCO16_01 [7:0]								R	R	R	
0x73	CH3_PELCO16_01 [15:8]								R	R	R	
0x74	-								-	-	-	
0x75	-								-	-	-	
0x76	-								-	-	-	
0x77	-								-	-	-	
0x78	CH3_PELCO8_0								R	R	R	
0x79	CH3_PELCO8_1								R	R	R	
0x7A	CH3_PELCO8_2								R	R	R	
0x7B	CH3_PELCO8_3								R	R	R	
0x7C	-								-	-	-	
0x7D	-								-	-	-	
0x7E	-								-	-	-	
0x7F	-								-	-	-	

 BANK4 Register(0x80~0x9F) : COAXIAL CH4

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0x80	CH4_BAUD								0x37	0x37	0x37
0x81	-								-	-	-
0x82	CH4_PELCO_BAUD								0x1B	0x1B	0x1B
0x83	CH4_BL_TXST[7:0]								0x05	0x05	0x05
0x84	-			CH4_BL_TXST[11:8]					0x00	0x00	0x00
0x85	-			CH4_ACT_LEN					0x00	0x00	0x00
0x86	-			-					-	-	-
0x87	CH4_PELCO_TXST[7:0]								0x09	0x09	0x09
0x88	-			CH4_PELCO_TXST[11:8]					0x00	0x00	0x00
0x89	-		CH4_COAX_SW_RST	CH4_CNT_MODE	-			CH4_TX_START	0x00	0x00	0x00
0x8A	-		CH4_TX_BYTE_LENGTH					0x08	0x08	0x08	
0x8B	CH4_PELCO_8BIT	-		CH4_LINE_8BIT	-			CH4_PACKET_MODE	0x06	0x06	0x06
0x8C	-							CH4_PELCO_CTEN	0x00	0x00	0x00
0x8D	CH4_BL_HSP[7:0]								0x46	0x46	0x46
0x8E	-			CH4_BL_HSP[11:8]					0x00	0x00	0x00
0x8F	-							CH4_PELCO_SHOT	0x00	0x00	0x00
0x90	CH4_TX_DATA_01								0xA0	0xAA	0xAA
0x91	CH4_TX_DATA_02								0xA1	0x1C	0x1C
0x92	CH4_TX_DATA_03								0xA2	0x18	0x18
0x93	CH4_TX_DATA_04								0xA3	0xFF	0xFF
0x94	CH4_TX_DATA_05								0xA4	0xAA	0xAA
0x95	CH4_TX_DATA_06								0xA5	0x3C	0x3C
0x96	CH4_TX_DATA_07								0xA6	0xFF	0xFF
0x97	CH4_TX_DATA_08								0xA7	0xFF	0xFF
0x98	CH4_TX_DATA_09								0xA8	0xAA	0xAA
0x99	CH4_TX_DATA_10								0xA9	0x1B	0x1B
0x9A	CH4_TX_DATA_11								0xAA	0x00	0x00
0x9B	CH4_TX_DATA_12								0xAB	0x00	0x00
0x9C	CH4_TX_DATA_13								0xAC	0xAA	0xAA
0x9D	CH4_TX_DATA_14								0xAD	0x3B	0x3B
0x9E	CH4_TX_DATA_15								0xAE	0x00	0x00
0x9F	CH4_TX_DATA_16								0xAF	0x00	0x00

 BANK4 Register(0xA0~0xBF) : COAXIAL CH4

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
0xA0	CH4_PELCO_TXDAT_01								0xFF	0x00	0x00
0xA1	CH4_PELCO_TXDAT_02								0x00	0x00	0x00
0xA2	CH4_PELCO_TXDAT_03								0xFF	0x00	0x00
0xA3	CH4_PELCO_TXDAT_04								0x00	0x00	0x00
0xA4	-								-	-	-
0xA5	-								-	-	-
0xA6	-								-	-	-
0xA7	-								-	-	-
0xA8	-								-	-	-
0xA9	-								-	-	-
0xAA	-								-	-	-
0xAB	-								-	-	-
0xAC	CH4_VSO_INV								0x00	0x00	0x00
0xAD	CH4_HSO_INV								0x00	0x00	0x00
0xAE	-								-	-	-
0xAF	CH4_Hidden_Even_line_modification								0x01	0x01	0x01
0xB0	-								-	-	-
0xB1	-								-	-	-
0xB2	-								-	-	-
0xB3	-								-	-	-
0xB4	-								-	-	-
0xB5	-								-	-	-
0xB6	-								-	-	-
0xB7	-								-	-	-
0xB8	-								-	-	-
0xB9	-								-	-	-
0xBA	-							CH4_CLEAN	0x00	0x00	0x00
0xBB	CH4_AUTO	-	CH4_CMD_LIST						0x00	0x00	0x00
0xBC	-								-	-	-
0xBD	-								-	-	-
0xBE	-								-	-	-
0xBF	-								-	-	-

 BANK4 Register(0xC0~0xDF) : COAXIAL CH4

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
B A N K 4	0xC0	CH4_ORIGIN_A_00								R	R	R
	0xC1	CH4_ORIGIN_A_01								R	R	R
	0xC2	CH4_ORIGIN_A_02								R	R	R
	0xC3	CH4_ORIGIN_A_03								R	R	R
	0xC4	CH4_ORIGIN_A_04								R	R	R
	0xC5	CH4_ORIGIN_A_05								R	R	R
	0xC6	CH4_ORIGIN_B_00								R	R	R
	0xC7	CH4_ORIGIN_B_01								R	R	R
	0xC8	CH4_ORIGIN_B_02								R	R	R
	0xC9	CH4_ORIGIN_B_03								R	R	R
	0xCA	CH4_ORIGIN_B_04								R	R	R
	0xCB	CH4_ORIGIN_B_05								R	R	R
	0xCC	-								-	-	-
	0xCD	-								-	-	-
	0xCE	-								-	-	-
	0xCF	-								-	-	-
	0xD0	CH4_ORIGIN_C_00								R	R	R
	0xD1	CH4_ORIGIN_C_01								R	R	R
	0xD2	CH4_ORIGIN_C_02								R	R	R
	0xD3	CH4_ORIGIN_C_03								R	R	R
	0xD4	CH4_ORIGIN_C_04								R	R	R
	0xD5	CH4_ORIGIN_C_05								R	R	R
	0xD6	CH4_ORIGIN_D_00								R	R	R
	0xD7	CH4_ORIGIN_D_01								R	R	R
	0xD8	CH4_ORIGIN_D_02								R	R	R
	0xD9	CH4_ORIGIN_D_03								R	R	R
	0xDA	CH4_ORIGIN_D_04								R	R	R
	0xDB	CH4_ORIGIN_D_05								R	R	R
	0xDC	-							CH4_RX_DONE	R	R	R
	0xDD	CH4_RX_COAX_DUTY								R	R	R
	0xDE	-								-	-	-
	0xDF	-								-	-	-

 BANK4 Register(0xE0~0xFF) : COAXIAL CH4

ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P	
0xE0	CH4_DEVICE_ID								0x48	0x48	0x48	
0xE1	-								-	-	-	
0xE2	CH4_RX_AREA								0x06	0x06	0x06	
0xE3	-		CH4_DELAY_ON		-		CH4_COMM_ON		0x01	0x01	0x01	
0xE4	CH4_DELAY_CNT								0x00	0x00	0x00	
0xE5	-							CH4_MSB	0x01	0x01	0x01	
0xE6	CH4_A_DUTY_ON	-								0x80	0x80	0x80
0xE7	-							CH4_INT_MODE	0x01	0x01	0x01	
0xE8	CH4_RX_SZ			-						0x50	0x50	0x50
0xE9	CH4_M_DUTY								0x00	0x00	0x00	
0xEA	CH4_RX_START_POSITION								0x00	0x00	0x00	
0xEB	-								-	-	-	
0xEC	-								-	-	-	
0xED	-								-	-	-	
0xEE	-								-	-	-	
0xEF	-								-	-	-	
0xF0	-			CH4_PELCO16_00_A						R	R	R
0xF1	-			CH4_PELCO16_00_B						R	R	R
0xF2	-			CH4_PELCO16_01_A						R	R	R
0xF3	-			CH4_PELCO16_02_B						R	R	R
0xF4	-								-	-	-	
0xF5	-								-	-	-	
0xF6	-								-	-	-	
0xF7	-								-	-	-	
0xF8	-			CH4_PELCO8_0						R	R	R
0xF9	-			CH4_PELCO8_1						R	R	R
0xFA	-			CH4_PELCO8_2						R	R	R
0xFB	-			CH4_PELCO8_3						R	R	R
0xFC	-								-	-	-	
0xFD	-								-	-	-	
0xFE	-								-	-	-	
0xFF	-								-	-	-	

Reserved BANK5/6/7/8 Registers(0x00~0x7F)

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
B A N K 5 / 6 / 7 / 8	0x00	Def	0xC0	0x09	0x0C	0x1F	0x00	0x24	0x60	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x00
		30P	0xC0	0x09	0x0C	0x1F	0x00	0x24	0x40	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x00
		25P	0xC0	0x09	0x0C	0x1F	0x00	0x24	0x40	0x80	0x50	0x38	0x0F	0x00	0x04	0x10	0x30	0x00
	0x10	Def	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x08	0x50	0x0C	0x00	0x88
		30P	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x08	0x50	0x0C	0x00	0x88
		25P	0x06	0x06	0x00	0x80	0x37	0x80	0x49	0x37	0xEF	0xDF	0xDF	0x08	0x50	0x0C	0x00	0x88
	0x20	Def	0x84	0x20	0x23	0x00	0x2A	0xD1	0xF0	0x57	0x90	0x70	0x52	0x78	0x00	0x68	0x00	0x07
		30P	0x84	0x20	0x23	0x00	0x2A	0xDC	0xF0	0x57	0x90	0x70	0x52	0x78	0x00	0x68	0x00	0x07
		25P	0x84	0x20	0x23	0x00	0x2A	0xDC	0xF0	0x57	0x90	0x70	0x52	0x78	0x00	0x68	0x00	0x07
	0x30	Def	0xE0	0x43	0xA2	0x00	0x00	0x17	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
		30P	0xE0	0x43	0xA2	0x00	0x00	0x15	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
		25P	0xE0	0x43	0xA2	0x00	0x00	0x17	0x25	0x00	0x00	0x02	0x02	0x00	0x00	0x00	0x00	0x00
	0x40	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x00	0x00	0x00	0x00
		30P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x00	0x00	0x00	0x00
		25P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x00	0x44	0xAA	0x00	0x00	0x00	0x00	0x00
	0x50	Def	0x84	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x30
		30P	0x04	0xFF	0xFF	0x00	0x00	0x00	0x00	0x03	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x30
		25P	0x04	0xFF	0xFF	0x00	0x00	0x00	0x00	0x03	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x30
	0x60	Def	0x53	0x53	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		30P	0x53	0x53	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		25P	0x53	0x53	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0x70	Def	0xC0	0x01	0x06	0x06	0x11	0x00	0x01	0x81	0x01	0x01	0x00	0x00	0x00	0x80	0x00	0x00
		30P	0xC0	0x01	0x06	0x06	0x11	0x00	0x01	0x81	0x01	0x01	0x00	0x00	0x00	0x80	0x00	0x00
		25P	0xC0	0x01	0x06	0x06	0x11	0x00	0x01	0x81	0x01	0x01	0x00	0x00	0x00	0x80	0x00	0x00

Reserved BANK5/6/7/8 Registers(0x80~0xFF)

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
B A N K 5 / 6 / 7 / 8	0x80	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x3F	0xFF	0xFF	0xFF	0x00	0x00	0x00
		30P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x3F	0xFF	0xFF	0xFF	0x00	0x00	0x00
		25P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x04	0x3F	0xFF	0xFF	0xF	0x00	0x00	0x00
	0x90	Def	0x01	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
		30P	0x01	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
		25P	0x01	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x48	0x84	0x00	0x80	0x00	0x00	0x00	0x00
	0xA0	Def	0x10	0x10	0x0E	0x70	0x10	0x34	0x70	0x5C	0x40	0x20	0x30	0x40	0x10	0x08	0x04	0x20
		30P	0x10	0x30	0x0C	0x50	0x10	0x34	0x70	0x5C	0x20	0x20	0x30	0x40	0x20	0x20	0x14	0x20
		25P	0x10	0x10	0x0E	0x70	0x10	0x34	0x70	0x5C	0x40	0x20	0x30	0x40	0x10	0x08	0x04	0x20
	0xB0	Def	0x40	0x50	0x0E	0x00	0x00	0x80	0x00	0x00	0x39	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
		30P	0x40	0x50	0x0E	0x00	0x00	0x80	0x00	0x00	0x39	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
		25P	0x40	0x50	0x0E	0x00	0x00	0x80	0x00	0x00	0x39	0xB2	0x05	0x00	0xC0	0x00	0x00	0x00
	0xC0	Def	0x0D	0x13	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x50
		30P	0x0D	0x13	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		25P	0x0D	0x13	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xD0	Def	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		30P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
		25P	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	0xE0	Def	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		30P	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		25P	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	0xF0	Def	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		30P	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		25P	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Reserved BANK9 Register(0x00~0x6F): FSC Value

ADDRESS		0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
BANK9	0x00	Def	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
		30P	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
		25P	0x02	0x04	0x06	0x08	0x0C	0x10	0x14	0x18	0x1C	0x20	0x28	0x30	0x38	0x40	0x48	0x50
	0x10	Def	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		30P	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		25P	0x58	0x60	0x68	0x70	0x78	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x20	Def	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
		30P	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
		25P	0x01	0x03	0x05	0x07	0x0B	0x0F	0x13	0x17	0x1B	0x1F	0x27	0x2F	0x37	0x3F	0x47	0x4F
	0x30	Def	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		30P	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
		25P	0x57	0x5F	0x67	0x6F	0x77	0x7F	0x87	0x8F	0x97	0x9F	0xAF	0xBF	0xCF	0xDF	0xEF	0xFF
	0x40	Def	0x00	0x00	0x00	0x00	0x0F	0x00	0x40	0x00	-	-	-	-	-	-	-	-
		30P	0x00	0x00	0x00	0x00	0x0F	0x00	0xC3	0x00	-	-	-	-	-	-	-	-
		25P	0x00	0x00	0x00	0x00	0x0F	0x00	0x00	0x00	-	-	-	-	-	-	-	-
	0x50	Def	0x46	0x08	0x10	0x4F	0x46	0x08	0x10	0x4F	0x46	0x08	0x10	0x4F	0x46	0x08	0x10	0x4F
		30P	0xEE	0x00	0xE5	0x4E	0xEE	0x00	0xE5	0x4E	0xEE	0x00	0xE5	0x4E	0xEE	0x00	0xE5	0x4E
		25P	0x46	0x08	0x10	0x4F	0x46	0x08	0x10	0x4F	0x46	0x08	0x10	0x4F	0x46	0x08	0x10	0x4F
	0x60	Def	0x00	0x00	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		30P	0x00	0x00	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		25P	0x00	0x00	-	-	-	-	-	-	-	-	-	-	-	-	-	-

VIDEO Registers

❖ Registers to Power Down Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x02	PD_ADAC	[7]	0x20	0x20	PD_ADAC : Power down for AUDIO DAC 0 : ON 1 : OFF
		PD_VCH4	[3]			PD_VCH4 : Power down for CH4 Video AFE
		PD_VCH3	[2]			PD_VCH3 : Power down for CH3 Video AFE
		PD_VCH2	[1]			PD_VCH2 : Power down for CH2 Video AFE
		PD_VCH1	[0]			PD_VCH1 : Power down for CH1 Video AFE 0 : ON 1 : OFF

❖ Registers to Control Comb Filter and Video Format

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x08	AUTO_1	[7]	0x60	0x60	AUTO_x : A register to set the Auto Detect Mode On/Off; When the AUTO mode has a high value, the Auto_NT_x bit value of the STATUS Register(BANK0, 0xEF) is to be confirmed to distinguish NTSC-M/J and PAL-B/D/G/H standards. It does not support other standards, and when used in link with the DVR controller, it cannot be used in the NON_REAL_TIME mode. (x = channel 1~4). 0 : Auto Detect OFF 1 : Auto Detect ON
	0x09	AUTO_2				
	0x0A	AUTO_3				
	0x0B	AUTO_4				
	0x08	BSF_MODE_1	[6:5]			BSF_MODE_x : Selects the filter to make primary separation of the brightness and color signals. (x = channel 1~4) 00 : Mode 0 01 : Mode 1 10 : Mode 2 11 : Others
	0x09	BSF_MODE_2				
	0x0A	BSF_MODE_3				
	0x0B	BSF_MODE_4				
	0x08	VIDEO_FORMAT_1	[4:0]			VIDEO_FORMAT_x : A register to determine the video standards of the input signal (x = channel 1~4) 0000 : NTSC-M,J 10001 : NTSC-4.43 11101 : PAL-B,D,G,H,I 10110 : PAL-M 11111 : PAL-Nc 10101 : PAL-60 Others : None
	0x09	VIDEO_FORMAT_2				
	0x0A	VIDEO_FORMAT_3				
	0x0B	VIDEO_FORMAT_4				

❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x0C	BRIGHTNESS_1	[7:0]	0x08	0x08	<p>BRIGHTNESS_x : Brightness control; DC level of the Luma signal is adjustable up to -128 ~ +127. BRIGHTNESS consists of 2's Complements. (x = channel 1~4)</p> <p>00000001 : +1 01111111 : +127 10000000 : -128 11111111 : -1</p>
	0x0D	BRIGHTNESS_2				
	0x0E	BRIGHTNESS_3				
	0x0F	BRIGHTNESS_4				

❖ Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x10	CONTRAST_1	[7:0]	0x88	0x88	<p>CONTRAST_x : Contrast control, Gain level of the Luma signal is adjustable up to x2. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4)</p> <p>00000000 : ≙ x 0 01000000 : ≙ x 0.5 10000000 : ≙ x 1 11111111 : ≙ x 2</p>
	0x11	CONTRAST_2				
	0x12	CONTRAST_3				
	0x13	CONTRAST_4				

❖ Registers to Control Sharpness

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x14	H_SHARPNESS_1	[7:4]	0x9	0x9	<p>H_SHARPNESS_x : Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4)</p> <p>0000 : x 0 0100 : x 0.5 1000 : x 1 1111 : x 2</p>
	0x15	H_SHARPNESS_2				
	0x16	H_SHARPNESS_3				
	0x17	H_SHARPNESS_4				
	0x14	V_SHARPNESS_1	[3:0]	0x0	0x0	<p>V_SHARPNESS_x : Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4)</p> <p>0000 : x 1 0100 : x 2 1000 : x 3 1111 : x 4</p>
	0x15	V_SHARPNESS_2				
	0x16	V_SHARPNESS_3				
	0x17	V_SHARPNESS_4				

❖ Registers to Control Low Pass Filter

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION	
Bank	Addr			30P	25P		
0	0x18	Y_FIR_MODE_1	[3:0]	0x0 (AHD) / 0x8 (960H)	0x0 (AHD) / 0x8 (960H)	Y_FIR_MODE_x : Y Low Pass Filter control (x = channel 1~4)	
	0x19	Y_FIR_MODE_2	[3:0]			0000 : bypass	0001 : 6MHz
	0x1A	Y_FIR_MODE_3	[3:0]			0010 : 6.5MHz	0011 : 7MHz
	0x1B	Y_FIR_MODE_4	[3:0]			0100 : 7.5MHz	0101 : 8MHz
						0110 : 8.5MHz	0111 : 9MHz
						1000 : 9.5MHz	etc : Don't use

❖ Registers to Control Peaking Filter

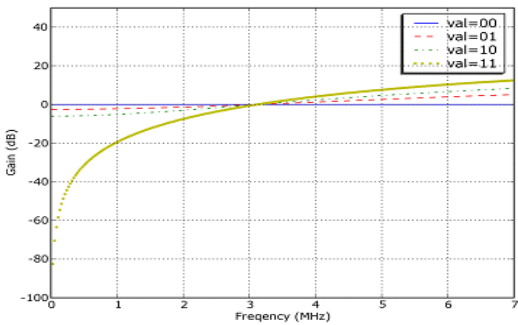
ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION	
Bank	Addr			30P	25P		
0	0x18	Y_PEAK_MODE_1	[7:4]	0x0	0x0	Y_PEAK_MODE_x : Y Peaking Filter control (x = channel 1~4)	
	0x19	Y_PEAK_MODE_2	[7:4]				
	0x1A	Y_PEAK_MODE_3	[7:4]			0000 : 0dB	0001 : 2dB
	0x1B	Y_PEAK_MODE_4	[7:4]			0010 : 3.5dB	0011 : 6dB
						0100 ~ 1111 : Don't use	

❖ Registers to Control ACC

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x20	ACC_OFF_1	[7]	0x2F	0x2F	ACC_OFF_x (x = channel 1~4) : Continue to a constant gain value for chroma signal 0 : ON 1 : OFF
	0x24	ACC_OFF_2				
	0x28	ACC_OFF_3				
	0x2C	ACC_OFF_4				
	0x24	ACC_GAIN_SPD_1	[3:0]			ACC_GAIN_SPD_x (x = channel 1~4) : 1 step value applied to the ACC Gain Accumulator (ACC Accumulator 1 Step value = 4 * ACC_GAIN_SPD + 2)
	0x34	ACC_GAIN_SPD_2				
	0x28	ACC_GAIN_SPD_3				
	0x2C	ACC_GAIN_SPD_4				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION		
Bank	Addr			30P	25P			
0	0x21	PAL_CM_OFF_1	[7]	0x92 (AHD) / 0x82 (960H)	0x92 (AHD) / 0x02 (960H)	PAL_CM_OFF_x (x = channel 1~4) : PAL Compensation On/Off. 0 : PAL Compensation applied 1 : PAL Compensation not applied.		
	0x25	PAL_CM_OFF_2						
	0x29	PAL_CM_OFF_3						
	0x2D	PAL_CM_OFF_4						
	0x21	IF_FIR_SEL_1	[6:4]			0x92 (AHD) / 0x82 (960H)	0x92 (AHD) / 0x02 (960H)	IF_FIR_SEL_x (x = channel 1~4) : IF Filter drive mode selected. 000 : bypass 001 : mode1 010 : mode2 Others : mode3
	0x25	IF_FIR_SEL_2						
	0x29	IF_FIR_SEL_3						
	0x2D	IF_FIR_SEL_4						
	0x21	CLPF_SEL_1	[3:0]			0x92 (AHD) / 0x82 (960H)	0x92 (AHD) / 0x02 (960H)	CLPF_SEL_x (x = channel 1~4) : C low pass filter applied mode applied after color demodulation. 0000 : Bypass 0001 : 0.6MHz cut off 0010 : 1.0MHz cut off 0011 : 1.2MHz cut off Others : Bypass
	0x25	CLPF_SEL_2						
	0x29	CLPF_SEL_3						
	0x2D	CLPF_SEL_4						



❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION		
Bank	Addr			30P	25P			
0	0x22	COLOROFF_1	[4]	0x0B	0x0B	COLOROFF_x (x = channel 1~4) : COLOR OFF 0 : Color ON 1 : Color OFF		
	0x26	COLOROFF_2						
	0x2A	COLOROFF_3						
	0x2E	COLOROFF_4						
	0x22	C_KILL_1	[3:0]			0x0B	0x0B	C_KILL_x[3] (x = channel 1~4) : Select to Color kill mode 0 : Not Y/C separation 1 : Color kill after Y/C separation C_KILL_x[2:0] (x = channel 1~4) : color kill control. 000 : Burst Amplitude 10% Under & FSC Unlock 001 : Burst Amplitude 5% Under & FSC Unlock 010 : Burst Amplitude 10 % Under 011 : Burst Amplitude 5% Under 100 : Always color on 101 : Always color on. 110 : Always color off 111 : Always color off
	0x26	C_KILL_2						
	0x2A	C_KILL_3						
	0x2E	C_KILL_4						

❖ Registers to Control Sync Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x23	FLD_DET_MODE_1	[7:6]	0x43	0x43	FLD_DET_MODE_x (x = channel 1~4) : Select the method to create the field information that will be externally output. 00 : Time-labs Mode : correction after Search for the two fields 01 : Normal toggle mode : correction after Search for the 16-fields 10 : normal mode : : Detection after Search for the 1-field 11 : Only toggle mode NOVID_DET_B_x (x = channel 1~4) : Select Condition for No video detection, High Active. [0] : If the input video is not detected sync, decision to NO Video [1] : If width of detected sync is narrower than video standard, decision to NO Video [2] : If Vertical sync don't exist, decision to NO Video [3] : If the CLAMP is not stable, decision to NO Video
	0x27	FLD_DET_MODE_2				
	0x2B	FLD_DET_MODE_3				
	0x2F	FLD_DET_MODE_4				
	0x23	NOVID_DET_B_1	[3:0]			
	0x27	NOVID_DET_B_2				
	0x2B	NOVID_DET_B_3				
	0x2F	NOVID_DET_B_4				

❖ Registers to Control Y_DELAY

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x30	Y_DELAY_1	[4:0]	0x10	0x10	Y_DELAY_ON_x (x = channel 1~4) : Y DELAY Control, controllable between 0x00 ~ 0x1F.
	0x31	Y_DELAY_2				
	0x32	Y_DELAY_3				
	0x33	Y_DELAY_4				

❖ Registers to Control Pedestal

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x34	PED_ON_1	[6]	0x04	0x02	PED_ON_x : Select to Pedestal ON/OFF (x = channel 1~4) 0 : Pedestal OFF 1 : Pedestal ON
	0x35	PED_ON_2				
	0x36	PED_ON_3				
	0x37	PED_ON_4				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x38	CTI_GAIN_1	[7:0]	0x0A	0x0A	CTI_GAIN_x[7:6] (x = channel 1~4) : Adjust CTI Gain Delay
	0x39	CTI_GAIN_2				
	0x3A	CTI_GAIN_3				
	0x3B	CTI_GAIN_4				
	0x3C	SATURATION_1	[7:0]	0x84	0x84	SATURATION_x (x = channel 1~4) : Color Gain Value (Adjustable up to x2) 00000000 : x 0 10000000 : x 1 11000000 : x 1.5 11111111 : x 2
	0x3D	SATURATION_2				
	0x3E	SATURATION_3				
	0x3F	SATURATION_4				
	0x40	HUE_1	[7:0]	0xFD	0x00	HUE_x (x = channel 1~4) : Color HUE Control Value (360°/256 per HUE Value 1 unit) 00000000 : 0° 01000000 : 90° 10000000 : 180° 11111111 : 360°
	0x41	HUE_2				
	0x42	HUE_3				
	0x43	HUE_4				

❖ Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x44	U_GAIN_1	[7:0]	0x30	0x30	U_GAIN_x (x = channel 1~4) : U Gain Value (Adjustable up to x2) 00000000 : x 0 10000000 : x 1 11000000 : x 1.5 11111111 : x 2
	0x45	U_GAIN_2				
	0x46	U_GAIN_3				
	0x47	U_GAIN_4				
	0x48	V_GAIN_1	[7:0]	0x30	0x30	V_GAIN_x (x = channel 1~4) : V Gain Value (Adjustable up to x2) 00000000 : x 0 10000000 : x 1 11000000 : x 1.5 11111111 : x 2
	0x49	V_GAIN_2				
	0x4A	V_GAIN_3				
	0x4B	V_GAIN_4				
	0x4C	U_OFFSET_1	[7:0]	0x04	0x04	U_OFFSET_x (x = channel 1~4) : U offset value is adjustable up to ± 7. U offset consists of 2's complements. 0001 : +1 0111 : +7 1000 : -8 1111 : -1
	0x4D	U_OFFSET_2				
	0x4E	U_OFFSET_3				
	0x4F	U_OFFSET_4				
	0x50	V_OFFSET_1	[7:0]	0x04	0x04	V_OFFSET_x (x = channel 1~4) : V offset value is adjustable up to ± 7. V offset consists of 2's complements. 0001 : +1 0111 : +7 1000 : -8 1111 : -1
	0x51	V_OFFSET_2				
	0x52	V_OFFSET_3				
	0x53	V_OFFSET_4				

❖ Registers to Control Field Polarity

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x54	FLD_INV_4	[7]	0xF	0x0	FLD_INV_x (x = channel 1~4) : Field Polarity Control 0 : not Inversion 1 : Inversion
		FLD_INV_3	[6]			
		FLD_INV_2	[5]			
		FLD_INV_1	[4]			

❖ Registers to Insert No Video Information

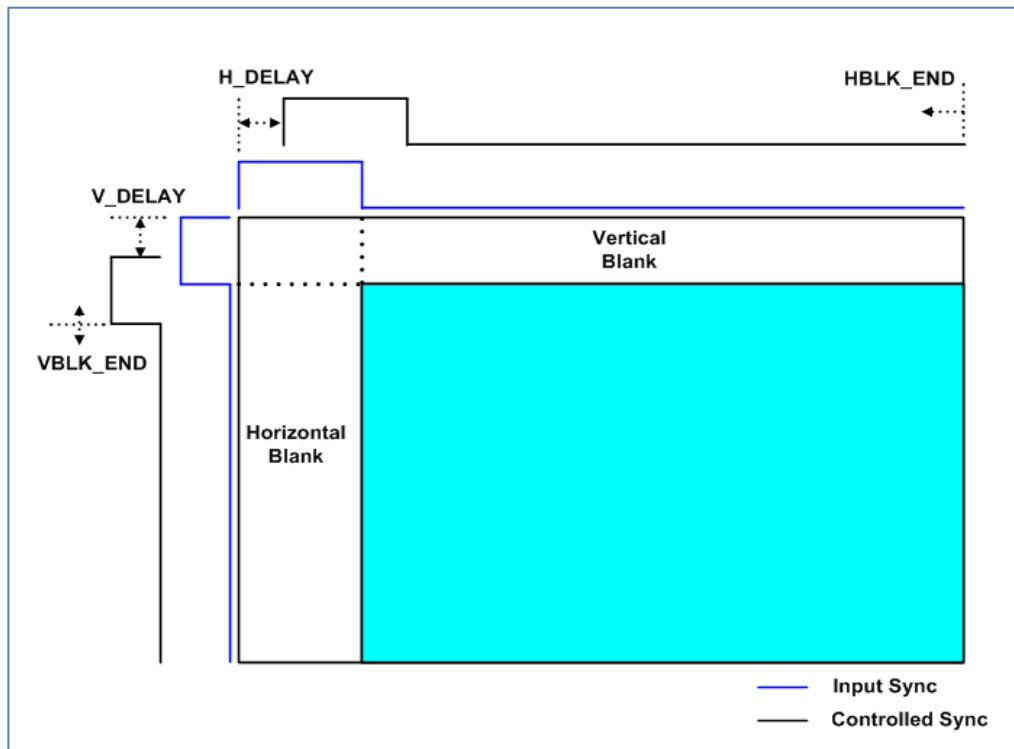
ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x54	NOVID_INF_IN_14	[3]	0x0	0x0	NOVID_INF_IN_14 (CH1~CH4) : It can include a NO-Video information at MSB of EAV and SAV. 0 : No information 1 : Put no-video information in EAV or SAV

❖ Registers to Control Channel ID

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x54	CHID_TYPE_14	[2:0]	0x1	0x1	CHID_TYPE_x (x = channel 1~4) : It determines type of channel ID.
	0x55	CHID_VIN_1	[3:0]	0x10	0x10	CHID_VIN_x (x = channel 1~4) : Register to put CHANNEL ID to distinguish channel. (0x0~0xF)
		CHID_VIN_2	[7:4]			
	0x56	CHID_VIN_3	[3:0]	0x10	0x10	
CHID_VIN_4		[7:4]				

❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x58	H_DELAY_1	[7:0]	0xA0	0x90	H_DELAY_x : Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal. (x = channel 1~4)
	0x59	H_DELAY_2				
	0x5A	H_DELAY_3				
	0x5B	H_DELAY_4				
	0x5C	V_DELAY_1	[5:0]	0x9E (AHD) 0x1E (960H)	0x9E (AHD) 0x1E (960H)	V_DELAY_x[5] : V_DELAY_x[4:0] Control Enable (x = channel 1~4)
	0x5D	V_DELAY_2				
	0x5E	V_DELAY_3				
	0x5F	V_DELAY_4				V_DELAY_x[4:0] (When V_DELAY_x[5] = 1) : Register to determine the Vertical start position of output image to Vsync extracted in analog input signal. (x = channel 1~4)



❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x60	HBLK_END_1	[7:0]	0x00	0x00	HBLK_END_x (x = channel 1~4) : Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed.
	0x61	HBLK_END_2				
	0x62	HBLK_END_3				
	0x63	HBLK_END_4				
	0x64	VBLK_END_1	[7:0]	0xB2 (AHD)	0xB1 (AHD)	VBLK_END_x[5] (x = channel 1~4) : VBLK_END_x[4:0] Control Enable VBLK_END_x[4:0] (When VBLK_END_x[5] = 1) : Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then the Active region is changed. (x = channel 1~4)
	0x65	VBLK_END_2				
	0x66	VBLK_END_3				
	0x67	VBLK_END_4				

❖ Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x68	H_CROP_S_1	[7:0]	0x00	0x00	H_CROP_S_x : Adjust the horizontal crop start point. (x = channel 1~4)
	0x69	H_CROP_S_2				
	0x6A	H_CROP_S_3				
	0x6B	H_CROP_S_4				
	0x6C	H_CROP_E_1	[7:0]	0x00	0x00	H_CROP_E_x : Adjust the horizontal crop end point. (x = channel 1~4)
	0x6D	H_CROP_E_2				
	0x6E	H_CROP_E_3				
	0x6F	H_CROP_E_4				
	0x70	V_CROP_S_1	[7:0]	0x00	0x00	V_CROP_S_x : Adjust the vertical crop start point. (x = channel 1~4)
	0x71	V_CROP_S_2				
	0x72	V_CROP_S_3				
	0x73	V_CROP_S_4				
	0x74	V_CROP_E_1	[7:0]	0x00	0x00	V_CROP_E_x : Adjust the vertical crop end point. (x = channel 1~4)
	0x75	V_CROP_E_2				
	0x76	V_CROP_E_3				
	0x77	V_CROP_E_4				

❖ Registers to Control Back Ground Color

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x78	BGDCOL_1	[3:0]	0x88	0x88	BGDCOL_x : When No-Video, BackGround Color is used. (x = channel 1~4) 0000 : Blue 0001 : White (75%) 0010 : Yellow 0011 : Cyan 0100 : Green 0101 : Magenta 0110 : Red 0111 : Blue 1000 : Black 1001 : Gray 1010 : Red (NEXTCHIP) ¹ 1011 : Yellow (NEXTCHIP) ¹ 1100 : Magenta (NEXTCHIP) ¹ 1101 : Green (NEXTCHIP) ¹ 1110 : Blue (NEXTCHIP) ¹ 1111 : Cyan (NEXTCHIP) ¹ * These color information is exactly same as controllers provided by NEXTCHIP
		BGDCOL_2	[7:4]			
	0x79	BGDCOL_3	[3:0]			
		BGDCOL_4	[7:4]			

❖ Registers to Control Data Out Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x7A	DATA_OUT_MODE_1	[3:0]	0x11	0x11	DATA_OUT_MODE_x : It limits a level of output data, can change signals of Cb and Cr each. (x = channel 1~4) 0000 : Y(016~235), Cb(016~240), Cr(016~240) 0001 : Y(001~254), Cb(001~254), Cr(001~254) 0010 : Y(000~255), Cb(000~255), Cr(000~255) 0011 : Cb / Cr Change, 016~235 0100 : Cb / Cr Change, 001~254 0101 : Cb / Cr Kill, 016~235 0110 : Cb / Cr Kill, 001~254 Others : Background color output
		DATA_OUT_MODE_2	[7:4]			
	0x7B	DATA_OUT_MODE_3	[3:0]			
		DATA_OUT_MODE_4	[7:4]			

Enable Registers

❖ Registers For Each Channel Control

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x80	EACH_REG_SET	[3:0]	0x0	0x0	DEC_REG_EACH : For each control CH1~CH4 register. 0x0 : same control 0xF : each control

❖ Registers to Select AHD Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x81	AHD_MD_1	[3:0]	0x6	0x7	AHD_MD : AHD Mode Selection. 0: SD Mode 2: AFHD 30P MODE 3: AFHD 25P MODE 4: AHD 60P MODE 5: AHD 50P MODE 6: AHD 30P MODE 7: AHD 25P MODE Etc.: Don't use
	0x82	AHD_MD_2				
	0x83	AHD_MD_3				
	0x84	AHD_MD_4				

❖ Registers to Control Active Region

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x85	AV_960H_1	[0]	0x0 (AHD)	0x0 (AHD)	AV_960H_x : Control To 1H_ACTIVE_REGION (x = channel 1~4) 0: Active_region of other modes 1: Active_region of 960H mode
	0x86	AV_960H_2				
	0x87	AV_960H_3				
	0x88	AV_960H_4				

❖ Registers to Select 960H

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x85	STD_MD_1	[4]	0	0	STD_MODE_x (x = channel 1~4) : 960H Mode Selection 0: H720 or AHD MODE 1: H960 MODE
	0x86	STD_MD_2				
	0x87	STD_MD_3				
	0x88	STD_MD_4				

❖ Registers to Select SH960

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x89	SEL960H_01	[0]	0	0	* This register is not apply to the AHD mode. (apply to only SD MODE) SEL_960H_0x : 37.125MHz 720H mode or 37.125MHz 960H mode selection. When STD_MODE_x (BANK0, 0x85-0x88[0]) = 0x0 0: 37.125MHz 960H Mode 1: 37.125MHz 720H Mode
	0x8A	SEL960H_02				
	0x8B	SEL960H_03				
	0x8C	SEL960H_04				

❖ Registers to Control Horizontal ZOOM

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x93	HZOOM_ON_1	[0]	0	0	HZOOM_ON_x (x = channel 1~4) : This Register can be turned on or off Horizontal ZOOM. 0: ZOOM OFF 1: ZOOM ON
	0x94	HZOOM_ON_2				
	0x95	HZOOM_ON_3				
	0x96	HZOOM_ON_4				

❖ Registers to Control Y/C DELAY

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xA0	DF_YDELAY_4	[3:0]	0x0	0x0	DF_YDELAY_x (x = channel 1~4) : Y(Luminance) delay control in the domain of 27MHz can be controlled between 0x0 ~ 0xF.
	0xA1	DF_YDELAY_3				
	0xA2	DF_YDELAY_2				
	0xA3	DF_YDELAY_1				
	0xA0	DF_CDELAY_4	[7:4]	0x0	0x0	DF_CDELAY_x (x = channel 1~4) : C(Chrominance) delay control in the domain of 27MHz can be controlled between 0x0 ~ 0xF.
	0xA1	DF_CDELAY_3				
	0xA2	DF_CDELAY_2				
	0xA3	DF_CDELAY_1				
	0xA4	DB_YDELAY_4	[3:0]	0x1	0x1	DB_YDELAY_x (x = channel 1~4) : Y(Luminance) delay control in the domain of 36MHz can be controlled between 0x0 ~ 0xF.
	0xA5	DB_YDELAY_3				
	0xA6	DB_YDELAY_2				
	0xA7	DB_YDELAY_1				
	0xA4	DB_CDELAY_4	[7:4]	0x0	0x0	DB_CDELAY_x (x = channel 1~4) : C(Chrominance) delay control in the domain of 36MHz can be controlled between 0x0 ~ 0xF.
	0xA5	DB_CDELAY_3				
	0xA6	DB_CDELAY_2				
	0xA7	DB_CDELAY_1				

❖ Registers for MUTE Detection Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xBC	MUTE_01	[0]	Read	Read	MUTE_0x : Each Internal 8 Channel MUTE detection Status (x = Channel number) 0 : On Audio 1 : No Audio (MUTE)
		MUTE_02	[1]			
		MUTE_03	[2]			
		MUTE_04	[3]			
		MUTE_05	[4]			
		MUTE_06	[5]			
		MUTE_07	[6]			
		MUTE_08	[7]			
	0xBD	MUTE_09	[0]	Read	Read	MUTE_0x : Each External 8 Channel MUTE detection Status (x-1 = EXT Channel number) 0 : On Audio 1 : No Audio (MUTE)
		MUTE_10	[1]			
		MUTE_11	[2]			
		MUTE_12	[3]			
		MUTE_13	[4]			
		MUTE_14	[5]			
		MUTE_15	[6]			
		MUTE_16	[7]			
	0xBE	MUTEMIC_01	[0]	Read	Read	MUTEMIC_0x : Each Internal and External Mic Channel MUTE detection Status (x = Channel number) 0 : On Audio 1 : No Audio (MUTE)
		MUTEMIC_02	[2]			

❖ Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xBF	COAX_RX_DONE_1	[0]	Read	Read	COAX_RX_DONE_x : COAXIAL_RX_Detecting Status (x = channel number) 0 : No Detecting 1 : COAXIAL_RX_Detecting
		COAX_RX_DONE_2	[1]			
		COAX_RX_DONE_3	[2]			
		COAX_RX_DONE_4	[3]			

❖ Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xC0	NOVID_01B	[0]	Read	Read	NOVID_0xB : Each Channel Video Decoder No Video detection Status with HOLD option (x = Channel number) 0 : On Video 1 : No Video
		NOVID_02B	[1]			
		NOVID_03B	[2]			
		NOVID_04B	[3]			

❖ Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xC1	MOTION_01B	[0]	Read	Read	MOTION_0xB : Each Channel Motion detection Status with HOLD option (x = Channel number) 0 : No MOTION 1 : On MOTION
		MOTION_02B	[1]			
		MOTION_03B	[2]			
		MOTION_04B	[3]			
	0xC2	BLACK_01B	[0]	Read	Read	BLACK_0xB : Each Channel BLACK detection Status with HOLD option (x = Channel number) 0 : No BLACK 1 : On BLACK
		BLACK_02B	[1]			
		BLACK_03B	[2]			
		BLACK_04B	[3]			
	0xC3	WHITE_01B	[0]	Read	Read	WHITE_0xB : Each Channel WHITE detection Status with HOLD option (x = Channel number) 0 : No WHITE 1 : On WHITE
		WHITE_02B	[1]			
		WHITE_03B	[2]			
		WHITE_04B	[3]			

❖ Registers to show Mute Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xC4	MUTE_01B	[0]	Read	Read	MUTE_0xB : Each Internal 8 Channel MUTE detection Status with HOLD option (x = Channel number) 0 : On Audio 1 : No Audio (MUTE)
		MUTE_02B	[1]			
		MUTE_03B	[2]			
		MUTE_04B	[3]			
		MUTE_05B	[4]			
		MUTE_06B	[5]			
		MUTE_07B	[6]			
		MUTE_08B	[7]			
	0xC5	MUTE_09B	[0]	Read	Read	MUTE_0xB : Each External 8 Channel MUTE detection Status with HOLD option (x-1 = EXT Channel number) 0 : On Audio 1 : No Audio (MUTE)
		MUTE_10B	[1]			
		MUTE_11B	[2]			
		MUTE_12B	[3]			
		MUTE_13B	[4]			
		MUTE_14B	[5]			
		MUTE_15B	[6]			
		MUTE_16B	[7]			
	0xC6	MUTEMIC_01B	[0]	Read	Read	MUTEMIC_0xB : Each Internal and External Mic Channel MUTE detection Status (x = Channel number) 0 : On Audio 1 : No Audio (MUTE)
		MUTEMIC_02B	[2]			

❖ Registers to Interrupt clear for Status Registers

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xC8	RD_STATE_CLR	[7]	0x90	0x90	RD_STATE_CLR : Interrupt clear condition selection 0 : Interrupt clear when BANK0, 0xC0-0xC6 Addr Register Read 1 : Interrupt clear when BANK0, 0xB8-0xBE / 0xC0-0xC6 Addr Register Read
		STATE_HOLD	[4]			STATE_HOLD : Interrupt Hold condition selection 0 : No Hold Option, State is Real Time update. 1 : Hold Option operation. State is Hold until cleared

❖ Registers to control IRQ

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xC9	IRQ_INV	[3]	0x00	0x00	IRQ_INV : IRQ pin output signal inversion 0 : Not Inversion 1 : Inversion
		IRQ_SEL	[2:0]			IRQ_SEL : Select IRQ pin output signals selection When IRQ_MSB(BANK1,0xB2[0]) = 0, 0 : 0 (Zero) 1 : interrupt request by the No video detection 2 : interrupt request by the Mute detection 3 : interrupt request by the Motion detection 4 : interrupt request by the Black detection 5 : interrupt request by the White detection 6 : ALINKO 7 : BNCO When IRQ_MSB(BANK1,0xB2[0]) = 1, 0 : No vid Motion interrupt request 1 : No vid Black interrupt request 2 : No vid White interrupt request 3 : Black White interrupt request 4 : Black Motion interrupt request 5 : White Motion interrupt request 6 : No vid Motion Black interrupt request 7 : Black White Motion interrupt request

❖ Registers to Show the Detect MODE (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xD0	MODE_DET_CH1	[7:0]	Read	Read	MODE_DET_CHx : MODE Detecting Status (x = channel number) 00 : No Detecting 01 : SD NTSC MODE 02 : SD PAL MODE 04 : AHD 30P MODE 08 : AHD 25P MODE 10 : AHD 60P MODE 20 : AHD 50P MODE 40 : AFHD 30P MODE 80 : AFHD 25P MODE
	0xD1	MODE_DET_CH2				
	0xD2	MODE_DET_CH3				
	0xD3	MODE_DET_CH4				

❖ Registers to Show the ACC GAIN (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xD8	STATUS_ACC_GAIN1	[7:0]	Read	Read	STATUS_ACC_GAIN_x : ACC GAIN Value Status (x = channel number)
	0xD9	STATUS_ACC_GAIN2				
	0xDA	STATUS_ACC_GAIN3				
	0xDB	STATUS_ACC_GAIN4				

❖ Registers to read the PN MSB value (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xE8	PN_READ_MSB_VAL1	[7:4]	Read	Read	PN_READ_MSB_VAL_x : PN_MSB Value Status (x = channel number)
	0xE9	PN_READ_MSB_VAL2				
	0xEA	PN_READ_MSB_VAL3				
	0xEB	PN_READ_MSB_VAL4				

❖ Registers to read the FSC Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xE8	FSC_CHG_DONE1	[3]	Read	Read	FSC_CHG_DONE_x : A status which FSC changed done or not (x = channel number) 0 : not changed 1 : changed
	0xE9	FSC_CHG_DONE2				
	0xEA	FSC_CHG_DONE3				
	0xEB	FSC_CHG_DONE4				
	0xE8	CKILL1	[2]	Read	Read	CKILL_x : color kill status (x = channel number) 0 : Color On 1 : Color Off
	0xE9	CKILL2				
	0xEA	CKILL3				
	0xEB	CKILL4				
	0xE8	FSC_LOCK_DONE1	[1]	Read	Read	FSC_LOCK_DONE_x : FSC LOCK Detection Status (x = channel number)
	0xE9	FSC_LOCK_DONE2				
	0xEA	FSC_LOCK_DONE3				
	0xEB	FSC_LOCK_DONE4				
	0xE8	NOVIDEO1	[0]	Read	Read	NOVIDEO_x : NOVIDEO Status (x = channel number)
	0xE9	NOVIDEO2				
	0xEA	NOVIDEO3				
	0xEB	NOVIDEO4				

❖ Registers to Show FLD & BW Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xF1	FLD_04	[7:6]	Read	Read	* This read register is not apply to the AHD mode. (apply to only SD MODE) FLD_0x : Field Detection status (x = channel number) FLD [0] = 0 : Odd Field 1 : Even Field FLD [1] = 0 : Not detect Standard 1 : Detect Standard
		FLD_03	[5:4]			
		FLD_02	[3:2]			
		FLD_01	[1:0]			
	0xF3	BW_04	[3]	Read	Read	
		BW_03	[2]			
		BW_02	[1]			
		BW_01	[0]			

❖ Registers to Show Chip Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xF4	DEV_ID	[7:0]	Read	Read	DEV_ID : It shows Device ID (NVP6124 = 0x84)
	0xF6	CMP_VALUE	[7:0]	Read	Read	CMP_VALUE : Show the value for CLAMP about Channel selected by CMP_AGC_CH register
	0xF7	AGC_VALUE	[7:0]	Read	Read	AGC_VALUE : Show the value for AGC about Channel selected by CMP_AGC_CH register

AUDIO Registers

❖ Registers to Control Audio AFE and DFE

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x00	PD_AAFE	[7]	0x02	0x02	PD_AAFE : Audio AFE LIVE CH1~CH8 and MIC1 Power Down Mode selection 0 : Operation 1 : Power Down
		RM_PB_PIN	[3]			RM_PB_PIN : Selection of clock and sync for ADATA_REC, ADATA_SP pin 0 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_REC, ADATA_SP pin 1 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_REC, ADATA_SP pin
		PB_RM_PIN	[2]			PB_RM_PIN : Selection of clock and sync for ADATA_PB pin 0 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_PB, 1 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_PB,
		FILTER_ON	[1]			FILTER_ON : Set ADC sampling rate 0 : Non-oversample (16KHz) 1 : Oversample (64KHz)
		EN_32K_MODE	[0]			EN_32K_MODE : Operate whole audio system as 32k mode 0 : 16K Mode 1 : 32K Mode

❖ Registers to Control Audio Input Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x01	AIGAIN_01	[7:0]	0x0A	0x0A	AIGAIN_x / MIGAIN_x : The gain of analog audio input AIN1-8 and MICIN1 0000 : mute 0001 : 0.125 0010 : 0.25 0011 : 0.375 0100 : 0.5 0101 : 0.625 0110 : 0.75 0111 : 0.875 1000 : 1.0 1001 : 1.125 1010 : 1.25 1011 : 1.375 1100 : 1.5 1101 : 1.625 1110 : 1.75 1111 : 1.875 10000 : 2.0 10001 : 2.125 10000 ~ 11111111 : step by about 0.125
	0x02	AIGAIN_02	[7:0]			
	0x03	AIGAIN_03	[7:0]			
	0x04	AIGAIN_04	[7:0]			
	0x40	AIGAIN_05	[7:0]			
	0x41	AIGAIN_06	[7:0]			
	0x42	AIGAIN_07	[7:0]			
	0x43	AIGAIN_08	[7:0]			
	0x05	MIGAIN_01	[3:0]			

❖ Registers to Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x06	CAS_PB	[7]	0x1B	0x1B	CAS_PB : The Usage of Playback Data when Cascade Mode 0 : use multiple playback data, received through all stage 1 : use single playback data, received through last stage
		TRANS_MODE	[6]			TRANS_MODE : Control the phase between transferred clock and cascade data 0 : Same phase 1 : Inverted phase
		CAS_PIN	[4]			CAS_PIN : Control the usage of ADATA_CASI and ADATA_CASO as cascade transmitting 0 : Don't Use 1 : Use
		CHIP_STAGE	[1:0]			CHIP_STAGE : Selection of chip state for cascade 0 : middle stage 1 : last stage 2 : first stage 3 : single chip operation
	0x07	RM_MASTER	[7]			RM_MASTER : Selection of master & slave mode of ACLK_REC and ASYNC_REC 0 : Slave mode operation 1 : Master mode operation
		RM_CLK	[6]			RM_CLK : Set the relationship between audio signal outputted to ADATA_REC and clock outputted to ACLK_REC 0 : inverted clock 1 : non-inverted clock
		RM_BITRATE	[5:4]			RM_BITRATE : Set the bit rate of audio signal outputted to ADATA_REC 0 : 256fs 1 : 384fs 2 : 320fs 3 : Don't Use
		RM_SAMRATE	[3]			RM_SAMRATE : Set the sampling rate of data outputted to ADATA_REC 0 : 8KHz 1 : 16KHz
		RM_BITWID	[2]	RM_BITWID : Set the bit width of data outputted to ADATA_REC 0 : 16bits 1 : 8bits		
		RM_SSP	[1]	RM_SSP : Selection of DSP mode and SSP mode for ADATA_REC pin, when ASYNC_REC is DSP mode. 0 : DSP mode 1 : SSP mode		
		RM_SYNC	[0]	RM_SYNC : Set the sync's mode inputted/outputted to ASYNC_REC. 0 : I2S mode 1 : DSP mode		

❖ Registers to Control Audio interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x08	RM_BIT_SWAP	[7]	0x03	0x03	RM_BIT_SWAP : Set the bit sequence of Audio Data for ADATA_REC 0 : MSB first 1 : LSB first
		RM_LAW_SEL	[6]			RM_LAW_SEL : Define the G.711 data format outputted to ADATA_REC 0 : u-law 1 : a-law
		RM_FORMAT	[5:4]			RM_FORMAT : Define the data format outputted to ADATA_REC 0 : linear PCM 1 : Unsigned linear PCM 2 : G.711 format 3 : Don't Use
		R_ADATSP2	[3]			R_ADATSP : Selection of output data for ADATA_SP 0 : Speaker data 1 : Record data
		R_ADATSP	[2]			
		R_MULTCH	[1:0]			R_MULTCH : Selection of number of Channel for ADATA_REC 0 : 2ch 1 : 4ch 2 : 8ch 3 : 16ch

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x09	R_SEQ_01[4]	[0]	0x0	0x0	R_SEQ : Sequence of Audio Data for ADATA_REC 00000 : channel 1 data 00001 : channel 2 data 00010 : channel 3 data 00011 : channel 4 data 00100 : channel 5 data 00101 : channel 6 data 00110 : channel 7 data 00111 : channel 8 data 01000 : channel 9 data 01001 : channel 10 data 01010 : channel 11 data 01011 : channel 12 data 01100 : channel 13 data 01101 : channel 14 data 01110 : channel 15 data 01111 : channel 16 data 10000 : Mic input 1 10001 : Mic input 2
		R_SEQ_02[4]	[1]	0x0	0x0	
		R_SEQ_03[4]	[2]	0x0	0x0	
		R_SEQ_04[4]	[3]	0x0	0x0	
		R_SEQ_05[4]	[4]	0x0	0x0	
		R_SEQ_06[4]	[5]	0x0	0x0	
		R_SEQ_07[4]	[6]	0x0	0x0	
		R_SEQ_08[4]	[7]	0x0	0x0	
	0x0A	R_SEQ_01	[3:0]	0x10	0x10	
		R_SEQ_02	[7:4]			
	0x0B	R_SEQ_03	[3:0]	0x32	0x32	
		R_SEQ_04	[7:4]			
	0x0C	R_SEQ_05	[3:0]	0x54	0x54	
		R_SEQ_06	[7:4]			
	0x0D	R_SEQ_07	[3:0]	0x76	0x76	
		R_SEQ_08	[7:4]			

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x0E	R_SEQ_09[4]	[0]	0x0	0x0	R_SEQ : Sequence of Audio Data for ADATA_REC 00000 : channel 1 data 00001 : channel 2 data 00010 : channel 3 data 00011 : channel 4 data 00100 : channel 5 data 00101 : channel 6 data 00110 : channel 7 data 00111 : channel 8 data 01000 : channel 9 data 01001 : channel 10 data 01010 : channel 11 data 01011 : channel 12 data 01100 : channel 13 data 01101 : channel 14 data 01110 : channel 15 data 01111 : channel 16 data 10000 : Mic input 1 10001 : Mic input 2
		R_SEQ_10[4]	[1]	0x0	0x0	
		R_SEQ_11[4]	[2]	0x0	0x0	
		R_SEQ_12[4]	[3]	0x0	0x0	
		R_SEQ_13[4]	[4]	0x0	0x0	
		R_SEQ_14[4]	[5]	0x0	0x0	
		R_SEQ_15[4]	[6]	0x0	0x0	
		R_SEQ_16[4]	[7]	0x0	0x0	
	0x0F	R_SEQ_09	[3:0]	0x98	0x98	
		R_SEQ_10	[7:4]			
	0x10	R_SEQ_11	[3:0]	0xBA	0xBA	
		R_SEQ_12	[7:4]			
	0x11	R_SEQ_13	[3:0]	0xDC	0xDC	
		R_SEQ_14	[7:4]			
	0x12	R_SEQ_15	[3:0]	0xFE	0xFE	
		R_SEQ_16	[7:4]			
	0x3C	MIC_SEQ_01	[4:0]	0x00	0x00	
0x3D	MIC_SEQ_02	[4:0]	0x00	0x00		

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x13	PB_MASTER	[7]			PB_MASTER : Selection of master & slave mode of ACLK_PB and ASYNC_PB 0 : Slave mode 1 : Master mode
		PB_CLK	[6]			PB_CLK : Set the relationship between audio signal outputted to ADATA_PB and clock outputted to ACLK_PB 0 : inverted clock 1 : non-inverted clock
		PB_BITRATE	[5:4]			PB_BITRATE : Set the bit rate of audio signal outputted to ADATA_PB 0 : 256fs 1 : 384fs 2 : 320fs
		PB_SAMRATE	[3]	0x08	0x08	PB_SAMRATE : Set the sampling rate of data outputted to ADATA_PB 0 : 8KHz 1 : 16KHz
		PB_BITWID	[2]			PB_BITWID : Set the bit width of data outputted to ADATA_PB 0 : 16bits 1 : 8bits
		PB_SSP	[1]			PB_SSP : Set the position of data and sync signals inputted to ADATA_PB, when ASYNC_PB is DSP mode. 0 : DSP mode 1 : SSP mode
		PB_SYNC	[0]			PB_SYNC : Set the sync's mode inputted/outputted to ASYNC_PB. 0 : I2S mode 1 : DSP mode

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x14	PB_BIT_SWAP	[7]	0x00	0x00	PB_BIT_SWAP : Set the bit sequence of Audio Data for ADATA_PB 0 : MSB first 1 : LSB first
		PB_SEL	[4:0]			PB_SEL : select the audio input channel for playback input 00 : channel 01 01 : channel 02 02 : channel 03 03 : channel 04 04 : channel 05 05 : channel 06 06 : channel 07 07 : channel 08 08 : channel 09 09 : channel 10 0A : channel 11 0B : channel 12 0C : channel 13 0D : channel 14 0E : channel 15 0F : channel 16 10 : Mic input 1 11 : Mic input 2
	PB_FORMAT	[7:6]	PB_FORMAT : Define the data format inputted to ADATA_PB 0 : linear PCM 1 : Unsigned linear PCM 2 : G.711 format 3 : Don't Use			
	PB_LAW_SEL	[3]	PB_LAW_SEL : Define the G.711 data format inputted to ADATA_PB 0 : u-law 1 : a-law			

❖ Registers to Control Audio Mixing Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x16	MIX_RATIO_01	[3:0]	0x88	0x88	MIX_RATIO_x : Set the mixing gain for AIN1-15. (x = channel 1~16) 0 : mute 1 : 0.25 2 : 0.31 3 : 0.38 4 : 0.5 5 : 0.63 6 : 0.75 7 : 0.88 8 : 1.0 9 : 1.25 10 : 1.5 11 : 1.75 12 : 2.0 13 : 2.25 14 : 2.5 15 : 2.75
		MIX_RATIO_02	[7:4]			
	0x17	MIX_RATIO_03	[3:0]			
		MIX_RATIO_04	[7:4]			
	0x18	MIX_RATIO_05	[3:0]			
		MIX_RATIO_06	[7:4]			
	0x19	MIX_RATIO_07	[3:0]			
		MIX_RATIO_08	[7:4]			
	0x1A	MIX_RATIO_09	[3:0]			
		MIX_RATIO_10	[7:4]			
	0x1B	MIX_RATIO_11	[3:0]			
		MIX_RATIO_12	[7:4]			
	0x1C	MIX_RATIO_13	[3:0]			
		MIX_RATIO_14	[7:4]			
	0x1D	MIX_RATIO_15	[3:0]			
		MIX_RATIO_16	[7:4]			

❖ Registers to Control Audio Mixing Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x1E	MIX_RATIO_M1	[3:0]	0x88	0x88	MIX_RATIO_Mx/ MIX_RATIO_Px : Set the mixing gain for MICIN1~4 / PBIN1~4. (x = channel 1~4) 0 : mute 1 : 0.25 2 : 0.31 3 : 0.38 4 : 0.5 5 : 0.63 6 : 0.75 7 : 0.88 8 : 1.0 9 : 1.25 10 : 1.5 11 : 1.75 12 : 2.0 13 : 2.25 14 : 2.5 15 : 2.75
		MIX_RATIO_M2	[7:4]			
	0x1F	MIX_RATIO_M3	[3:0]			
		MIX_RATIO_M4	[7:4]			
	0x20	MIX_RATIO_P1	[3:0]			
		MIX_RATIO_P2	[7:4]			
	0x21	MIX_RATIO_P3	[3:0]			
		MIX_RATIO_P4	[7:4]			

❖ Registers to Control Audio Output Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x22	AOGAIN	[7:0]	0x0A	0x0A	AOGAIN : The gain of analog audio output 0000 : mute 0001 : 0.125 0010 : 0.25 0011 : 0.375 0100 : 0.5 0101 : 0.625 0110 : 0.75 0111 : 0.875 1000 : 1.0 1001 : 1.125 1010 : 1.25 1011 : 1.375 1100 : 1.5 1101 : 1.625 1110 : 1.75 1111 : 1.875 10000 ~ 11111111 : step by about 0.125

❖ Registers to Control Audio Mixing Output Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x23	MIX_DERATIO	[5]			MIX_DERATIO : Selection of the mixing gain mode 0 : Apply the mixing gain for MIX_RATIO_01-P4 (BANK1,0x16~0x21) separately 1 : Apply all mixing gain as the same gain (x1).
		MIX_OUTSEL	[4:0]	0x19	0x19	MIX_OUTSEL : Select the audio output for analog mixing out. 00 : Channel 1 0E : Channel 15 01 : Channel 2 0F : Channel 16 02 : Channel 3 10 : playback audio 03 : Channel 4 11 : second playback audio 04 : Channel 5 (first stage playback audio) 05 : Channel 6 (middle stage playback audio) 06 : Channel 7 12 : third playback audio 07 : Channel 8 13 : fourth playback audio 08 : Channel 9 (middle stage playback audio) 09 : Channel 10 (middle stage playback audio) 0A : Channel 11 14 : Mic input 1 0B : Channel 12 15 : Mic input 2 0C : Channel 13 18 : Mixed audio 0D : Channel 14 Others : No audio output

❖ Registers to Control Analog and Digital Mixing output

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x24	L_CH_OUTSEL	[4:0]	0x18	0x18	L_CH_OUTSEL / R_CH_OUTSEL : Select Left/Right channel of the audio output for ADATA_SP pin 00 : Channel 1 0E : Channel 15 01 : Channel 2 0F : Channel 16 02 : Channel 3 10 : playback audio 03 : Channel 4 11 : second playback audio 04 : Channel 5 (first stage playback audio) 05 : Channel 6 (middle stage playback audio) 06 : Channel 7 12 : third playback audio 07 : Channel 8 13 : fourth playback audio 08 : Channel 9 (middle stage playback audio) 09 : Channel 10 (middle stage playback audio) 0A : Channel 11 14 : Mic input 1 0B : Channel 12 15 : Mic input 2 0C : Channel 13 18 : Mixed audio 0D : Channel 14 Others : No audio output
	0x25	R_CH_OUTSEL		0x16	0x16	

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x26	MIX_MUTE_01	[0]	0x00	0x00	<p>MIX_MUTE_x : During mixing, selected channels are muted (x = channel value)</p> <p>0 : mixing data output 1 : mute for selected channel</p>
		MIX_MUTE_02	[1]			
		MIX_MUTE_03	[2]			
		MIX_MUTE_04	[3]			
		MIX_MUTE_05	[4]			
		MIX_MUTE_06	[5]			
		MIX_MUTE_07	[6]			
		MIX_MUTE_08	[7]			
	0x27	MIX_MUTE_09	[0]			
		MIX_MUTE_10	[1]			
		MIX_MUTE_11	[2]			
		MIX_MUTE_12	[3]			
		MIX_MUTE_13	[4]			
		MIX_MUTE_14	[5]			
		MIX_MUTE_15	[6]			
		MIX_MUTE_16	[7]			
	0x28	MIX_MUTE_P1	[0]			
		MIX_MUTE_P2	[1]			
		MIX_MUTE_P3	[2]			
		MIX_MUTE_P4	[3]			
		MIX_MUTE_M1	[4]			
MIX_MUTE_M2		[5]				
MIX_MUTE_M3		[6]				
MIX_MUTE_M4		[7]				

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x29	ADET_MODE	[3]	0x88	0x88	<p>ADET_MODE : Select the method to decide the existence of audio signals.</p> <p>0 : Absolute amplitude detection mode 1 : Differential amplitude detection mode</p>
		ADET_FILTER	[2:0]			<p>ADET_FILTER : Set the time to decide the existence of audio signals.</p> <p>0 : 16sec 1 : 15sec 2 : 9sec 3 : 5sec 4 : 3sec 5 : 1sec 6 : 0.6sec 7 : 0.5sec</p>

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x2A	ADET_01	[0]	0xFF	0xFF	ADET_0x / ADET_Mx : Enable bit audio signal existence checking function for AIN1-8 and MICIN1. (x = channel 1~8) 0 : Don't use this function 1 : Use this function
		ADET_02	[1]			
		ADET_03	[2]			
		ADET_04	[3]			
		ADET_05	[4]			
		ADET_06	[5]			
		ADET_07	[6]			
	ADET_08	[7]				
	0x2B	ADET_M1	[6]	0x40	0x40	

❖ Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x2C	ADET_TH_01	[3:0]	0xAA	0xAA	ADET_TH_0x : Set the thesshold value for audio signal existence of AIN1-8 and MICIN1
		ADET_TH_02	[7:4]			
	0x2D	ADET_TH_03	[3:0]			
		ADET_TH_04	[7:4]			
	0x2E	ADET_TH_05	[3:0]			
		ADET_TH_06	[7:4]			
	0x2F	ADET_TH_07	[3:0]			
		ADET_TH_08	[7:4]			
		0x30	ADET_TH_M1			

❖ Registers to Control Audio Software Reset

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x38	AUD_SW_RST	[4]	0x08	0x08	AUD_SW_RST : Software Reset 0 : Normal Operation 1 : Reset

❖ Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x39	RM_DELAY	[7]	0x01	0x01	RM_DELAY : Internal Record-Sync signal to 1-clock delay 0 : default 1 : 1 clk delay
		PB_DELAY	[6]			PB_DELAY : Internal Play-Back-Sync signal to 1-clock delay 0 : default 1 : 1 clk delay

VIDEO Control Registers

❖ Registers for Control MPP

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xB0	MPP_GPIO	[7:0]	0x00	0x00	MPP_GPIO : Global Purpose Output Setting Register (output only) Ex) control Coaxial mux control pins
	0xB1	MPP4_MSB	[7]	0x00	0x00	MPPx_MSB : Control output data of MPPx pin (x = MPP pin number) 0 : 1 item output for MPP signal 1 : 2-5 item OR output for MPP signal
		MPP3_MSB	[2]			
		MPP2_MSB	[1]			
		MPP1_MSB	[0]			
0xB2	IRQ_MSB	[0]	0	0	IRQ_MSB : Control output data of IRQ pin 0 : 1 item output for MPP signal 1 : 2-5 item OR output for MPP signal	

❖ Registers to Control COAX

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xBD	COAX_SEL1	[7:4]	0x0	0x0	COAX_SELx : Select COAX_x pin output signals selection (x = COAX Pin number) 0 : 0 (Zero) 1-C : Reserved D : Coaxial Protocol Command of ch x E : Coaxial Protocol Command of ch total F : Reserved
	0xBE	COAX_SEL2	[3:0]			
		COAX_SEL3	[7:4]			
		0xBF	COAX_SEL4			

❖ Registers to Control MPP

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xBC	MPP_SEL1	[3:0]	0x0	0x0	<p>MPP_SELx : Select MPPx pin output signals selection (x = MPP Pin number)</p> <p>When MPPx_MSB(BANK1,0xB1) = 0, 0 : 0 (Zero) 1 : NOVIDEO status of ch.x 2 : Horizontal blank of ch.x 3 : Vertical blank of ch.x 4 : Field of ch.x 5 : Mute status of ch.x 6 : Motion status of ch.x 7 : interrupt request by the No video detection 8 : interrupt request by the Mute detection 9 : interrupt request by the Motion detection A : interrupt request by the Black detection B : interrupt request by the White detection C : MPP_GPIO[x-1] Value (BANK1, 0xB0) Others : Don't Use</p>
		MPP_SEL2	[7:4]			
	0xBD	MPP_SEL3	[3:0]			
	0xBF	MPP_SEL4	[7:4]			

❖ Registers to Control Coaxial PIN

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xBD	COAX_SEL1	[7:4]	0xD	0xD	<p>COAX_SELx : Select COAX_x pin output signals selection (x = COAX Pin number)</p> <p>When MPPx_MSB(BANK1,0xB1) = 0, 0 : 0 (Zero) D : Coaxial Protocol Command of ch x Others : Don't Use</p>
	0xBE	COAX_SEL2	[7:4]			
	0xBE	COAX_SEL3	[3:0]			
	0xBF	COAX_SEL4	[7:4]			

❖ Registers to Select Video Output

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xC0	VPORT1_SEQ1	[3:0]	0x00	0x00	VPORTx_SEQy : Select the type of output video signal through each video output port (x = VDO output port number, y= channel count for 1-port) 0 : Nomal Display of Channel 1 1 : Nomal Display of Channel 2 2 : Nomal Display of Channel 3 3 : Nomal Display of Channel 4 8 : Motion Display of Channel 1 9 : Motion Display of Channel 2 A : Motion Display of Channel 3 B : Motion Display of Channel 4 Etc.: Don't use
		VPORT1_SEQ2	[7:4]			
	0xC1	VPORT1_SEQ3	[3:0]	0x00	0x00	
		VPORT1_SEQ4	[7:4]			
	0xC2	VPORT2_SEQ1	[3:0]	0x11	0x11	
		VPORT2_SEQ2	[7:4]			
	0xC3	VPORT2_SEQ3	[3:0]	0x11	0x11	
		VPORT2_SEQ4	[7:4]			
	0xC4	VPORT3_SEQ1	[3:0]	0x22	0x22	
		VPORT3_SEQ2	[7:4]			
	0xC5	VPORT3_SEQ3	[3:0]	0x22	0x22	
		VPORT3_SEQ4	[7:4]			
	0xC6	VPORT4_SEQ1	[3:0]	0x33	0x33	
		VPORT4_SEQ2	[7:4]			
	0xC7	VPORT4_SEQ3	[3:0]	0x33	0x33	
		VPORT4_SEQ4	[7:4]			

❖ Registers to Select Video Output

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xC8	CH_OUT_SELA	[3:0]	0x00	0x00	CH_OUT_SEQx : Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) When MODE_ENABLE (BANK0,0x81~0x83) = 0x02~0x05 2 : 148.5MHz AFHD and AHD 60/50P data of ch 1 3 : 148.5MHz time-mixed CIF AFHD and AHD 60/50P data of ch 1,2 Etc.: Don't use When MODE_ENABLE (BANK0,0x81~0x83) ≠ 0x00, 0x02~0x05 0 : 74.25MHz AHD data of ch 1 1 : 74.25MHz time-mixed CIF AHD data of ch 1,2 2 : 148.5MHz time-mixed AHD data of ch 1,2 3 : 148.5MHz time-mixed CIF AHD data of ch 1,2,3,4 Etc.: Don't use When MODE_ENABLE (BANK0,0x81~0x83) = 0x00, 0 : 27/37.125MHz D1 data of ch 1 (SD 720H/960H_MODE) 1 : 27/37.125MHz time-mixed CIF D1 data of ch 1,2 (SD 720H/960H_MODE) 2 : 54/74.25MHz time-mixed D1 data of ch 1,2 (SD 720H/960H_MODE) 3 : 54/74.25MHz time-mixed CIF D1 data of ch 1,2,3,4 (SD 720H/960H_MODE) 8 : 108/148.5MHz time-mixed D1 data of ch 1,2,3,4 (Only SD 720H/960H_MODE) Etc.: Don't use
		CH_OUT_SELB	[7:4]			
	0xC9	CH_OUT_SELC	[3:0]			
		CH_OUT SELD	[7:4]			

❖ Registers to Control Video Output Port Enable

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION	
Bank	Addr			30P	25P		
1	0xCA	VCLK_4_EN	[7]	0xFF	0xFF	VCLK_x_EN : Video Output Port_x CLK Enable (x = VDO output port number) 0 : Disable 1 : Enable	
		VCLK_3_EN	[6]				
		VCLK_2_EN	[5]				
		VCLK_1_EN	[4]				
		VDO_4_EN	[3]				VDO_x_EN : VDOx DATA Enable (x = VDO output port number) 0 : Disable 1 : Enable
		VDO_3_EN	[2]				
		VDO_2_EN	[1]				
		VDO_1_EN	[0]				

❖ Registers to Select Video Output Clock

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION	
Bank	Addr			30P	25P		
1	0xCC	VCLK1_SEL	[6:4]	0x60	0x60	VCLKx_SEL : Select clock frequency and phase of each port. (x = Port number) 0 : 37.125MHz clock with phase 1 (delay=0ns) 1 : 37.125MHz clock with phase 2 (delay=6.76ns) 2 : 37.125MHz clock with phase 3 (delay=13.47ns) 3 : 37.125MHz clock with phase 4 (delay=26.9ns) * 0-3 : Don't use When AHD or AFHD MODE 4 : 74.125MHz clock with phase 1 (delay=0ns) 5 : 74.125MHz clock with phase 2 (delay=13.47ns) 6 : 148.5MHz clock with phase 1 (delay=0ns) 7 : 148.5MHz clock with phase 2 (delay=6.73ns)	
	0xCD	VCLK2_SEL					
	0xCE	VCLK3_SEL					
	0xCF	VCLK4_SEL					
	0xCC	VCLK_1_DLY_SEL	[3:0]				VCLK_x_DLY_SEL : Delay the output clock in the unit of \approx 1ns. Can be delayed up to \approx 15ns. (x = Port number) 0000 : \approx 0ns. 0100 : \approx 4ns. 1000 : \approx 7ns. 1111 : \approx 15ns.
	0xCD	VCLK_2_DLY_SEL					
	0xCE	VCLK_3_DLY_SEL					
	0xCF	VCLK_4_DLY_SEL					

❖ Registers to Control Data Catch

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xD0	DATA_CATCH_2	[7:4]	0x00	0x00	DATA_CATCH_x (x = Channel number) : It can move a catch point to catch a stable data in each other frequency. (Change 37.125MHz Clock Domain to 148.5MHz Clock Domain)
		DATA_CATCH_1	[3:0]			
	0xD1	DATA_CATCH_4	[7:4]			
		DATA_CATCH_3	[3:0]			

❖ Registers to Control Data

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xD2	OUT_DATA_INV	[5:2]	0x00	0x00	OUT_DATA_INV : It sorts output video data inversely. (0 : [7:0], 1 : [0:7]) OUT_DATA_INV[0] : VDO1 Port output order control OUT_DATA_INV[1] : VDO2 Port output order control OUT_DATA_INV[2] : VDO3 Port output order control OUT_DATA_INV[3] : VDO4 Port output order control

MOTION Registers

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
2	0x00	MOTION_OFF_1	[4]	0x03	0x03	MOTION_OFF_x : Motion Detection On/Off Selection (x = channel number) 0 : Motion detection on 1 : Motion detection off
	0x02	MOTION_OFF_2				
	0x04	MOTION_OFF_3				
	0x06	MOTION_OFF_4				
	0x00	MOTION_PIC_1	[1:0]	0x03	0x03	MOTION_PIC_x : Indicates the type of processing made on the area where motion is generated. (x = channel number) 0 : No processing made on the area where motion is generated. 1 : EVEN_FLD (Luma – 32) 2 : EVEN_FLD (Luma – 48) 3 : ALL_FLD (Luma – 48)
	0x02	MOTION_PIC_2				
	0x04	MOTION_PIC_3				
	0x06	MOTION_PIC_4				
	0x01	MOD_TSEN_1	[7:0]	0x60	0x60	MOD_TSEN_x : Motion Temporal Sensitivity. (x = channel number) The value (the sum of the motion block) bases on which it is determined whether motion is generated or not (0 -> 255 The greater the number, the less sensitive it gets)
	0x03	MOD_TSEN_2				
	0x05	MOD_TSEN_3				
	0x07	MOD_TSEN_4				
	0x10	MOD_PSEN_1	[7:6]	0x00	0x00	MOD_PSEN_x : Motion Pixed Sensitivity. Register that determines how much data input in the Motion block is used to search for motion (x = channel number) 0 : bypass 1 : 1/2 2 : 1/4 3 : 1/8
		MOD_PSEN_2	[5:4]			
		MOD_PSEN_3	[3:2]			
		MOD_PSEN_4	[1:0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
2	0x20 0x38 0x50 0x68	CHx_MOD_01	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number)</p> <p>0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
		CHx_MOD_02	[6]			
		CHx_MOD_03	[5]			
		CHx_MOD_04	[4]			
		CHx_MOD_05	[3]			
		CHx_MOD_06	[2]			
		CHx_MOD_07	[1]			
		CHx_MOD_08	[0]			
	0x21 0x39 0x51 0x69	CHx_MOD_09	[7]	0xFF	0xFF	
		CHx_MOD_10	[6]			
		CHx_MOD_11	[5]			
		CHx_MOD_12	[4]			
		CHx_MOD_13	[3]			
		CHx_MOD_14	[2]			
		CHx_MOD_15	[1]			
		CHx_MOD_16	[0]			
	0x22 0x3A 0x52 0x6A	CHx_MOD_17	[7]	0xFF	0xFF	
		CHx_MOD_18	[6]			
		CHx_MOD_19	[5]			
		CHx_MOD_20	[4]			
		CHx_MOD_21	[3]			
		CHx_MOD_22	[2]			
		CHx_MOD_23	[1]			
		CHx_MOD_24	[0]			
	0x23 0x3B 0x53 0x6B	CHx_MOD_25	[7]	0xFF	0xFF	
		CHx_MOD_26	[6]			
		CHx_MOD_27	[5]			
		CHx_MOD_28	[4]			
		CHx_MOD_29	[3]			
		CHx_MOD_30	[2]			
		CHx_MOD_31	[1]			
		CHx_MOD_32	[0]			
	0x24 0x3C 0x54 0x6C	CHx_MOD_33	[7]	0xFF	0xFF	
		CHx_MOD_34	[6]			
		CHx_MOD_35	[5]			
		CHx_MOD_36	[4]			
		CHx_MOD_37	[3]			
		CHx_MOD_38	[2]			
		CHx_MOD_39	[1]			
		CHx_MOD_40	[0]			
	0x25 0x3D 0x55 0x6D	CHx_MOD_41	[7]	0xFF	0xFF	
		CHx_MOD_42	[6]			
		CHx_MOD_43	[5]			
		CHx_MOD_44	[4]			
		CHx_MOD_45	[3]			
		CHx_MOD_46	[2]			
		CHx_MOD_47	[1]			
		CHx_MOD_48	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
2	0x26 0x3E 0x56 0x6E	CHx_MOD_49	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number)</p> <p>0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
		CHx_MOD_50	[6]			
		CHx_MOD_51	[5]			
		CHx_MOD_52	[4]			
		CHx_MOD_53	[3]			
		CHx_MOD_54	[2]			
		CHx_MOD_55	[1]			
	CHx_MOD_56	[0]				
	0x27 0x3F 0x57 0x6F	CHx_MOD_57	[7]	0xFF	0xFF	
		CHx_MOD_58	[6]			
		CHx_MOD_59	[5]			
		CHx_MOD_60	[4]			
		CHx_MOD_61	[3]			
		CHx_MOD_62	[2]			
		CHx_MOD_63	[1]			
	CHx_MOD_64	[0]				
	0x28 0x40 0x58 0x70	CHx_MOD_65	[7]	0xFF	0xFF	
		CHx_MOD_66	[6]			
		CHx_MOD_67	[5]			
		CHx_MOD_68	[4]			
		CHx_MOD_69	[3]			
		CHx_MOD_70	[2]			
	0x29 0x41 0x59 0x71	CHx_MOD_71	[1]	0xFF	0xFF	
		CHx_MOD_72	[0]			
		CHx_MOD_73	[7]			
		CHx_MOD_74	[6]			
		CHx_MOD_75	[5]			
		CHx_MOD_76	[4]			
	0x2A 0x42 0x5A 0x72	CHx_MOD_77	[3]	0xFF	0xFF	
		CHx_MOD_78	[2]			
		CHx_MOD_79	[1]			
		CHx_MOD_80	[0]			
		CHx_MOD_81	[7]			
		CHx_MOD_82	[6]			
		CHx_MOD_83	[5]			
	0x2B 0x43 0x5B 0x73	CHx_MOD_84	[4]	0xFF	0xFF	
		CHx_MOD_85	[3]			
		CHx_MOD_86	[2]			
		CHx_MOD_87	[1]			
		CHx_MOD_88	[0]			
		CHx_MOD_89	[7]			
	CHx_MOD_90	[6]				
	CHx_MOD_91	[5]				
	CHx_MOD_92	[4]				
	CHx_MOD_93	[3]				
	CHx_MOD_94	[2]				
	CHx_MOD_95	[1]				
	CHx_MOD_96	[0]				

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
2	0x2C 0x44 0x5C 0x74	CHx_MOD_97	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number)</p> <p>0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
		CHx_MOD_98	[6]			
		CHx_MOD_99	[5]			
		CHx_MOD_100	[4]			
		CHx_MOD_101	[3]			
		CHx_MOD_102	[2]			
		CHx_MOD_103	[1]			
		CHx_MOD_104	[0]			
	0x2D 0x45 0x5D 0x75	CHx_MOD_105	[7]	0xFF	0xFF	
		CHx_MOD_106	[6]			
		CHx_MOD_107	[5]			
		CHx_MOD_108	[4]			
		CHx_MOD_109	[3]			
		CHx_MOD_110	[2]			
		CHx_MOD_111	[1]			
		CHx_MOD_112	[0]			
	0x2E 0x46 0x5E 0x76	CHx_MOD_113	[7]	0xFF	0xFF	
		CHx_MOD_114	[6]			
		CHx_MOD_115	[5]			
		CHx_MOD_116	[4]			
		CHx_MOD_117	[3]			
		CHx_MOD_118	[2]			
		CHx_MOD_119	[1]			
		CHx_MOD_120	[0]			
	0x2F 0x47 0x5F 0x77	CHx_MOD_121	[7]	0xFF	0xFF	
		CHx_MOD_122	[6]			
		CHx_MOD_123	[5]			
		CHx_MOD_124	[4]			
		CHx_MOD_125	[3]			
		CHx_MOD_126	[2]			
		CHx_MOD_127	[1]			
		CHx_MOD_128	[0]			
	0x30 0x48 0x60 0x78	CHx_MOD_129	[7]	0xFF	0xFF	
		CHx_MOD_130	[6]			
		CHx_MOD_131	[5]			
		CHx_MOD_132	[4]			
		CHx_MOD_133	[3]			
		CHx_MOD_134	[2]			
		CHx_MOD_135	[1]			
		CHx_MOD_136	[0]			
	0x31 0x49 0x61 0x79	CHx_MOD_137	[7]	0xFF	0xFF	
		CHx_MOD_138	[6]			
		CHx_MOD_139	[5]			
		CHx_MOD_140	[4]			
		CHx_MOD_141	[3]			
		CHx_MOD_142	[2]			
		CHx_MOD_143	[1]			
		CHx_MOD_144	[0]			

❖ Registers to Detect Motion

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
2	0x32 0x4A 0x62 0x7A	CHx_MOD_145	[7]	0xFF	0xFF	<p>CHx_MOD_01 ~ CHx_MOD_192 : Block enable to detect motion/black/white The entire screen is divided into 192 sections to each of while enable is allocated. (x = channel number)</p> <p>0 : Motion/Black/White Block Disable 1 : Motion/Black/White Block Enable</p>
		CHx_MOD_146	[6]			
		CHx_MOD_147	[5]			
		CHx_MOD_148	[4]			
		CHx_MOD_149	[3]			
		CHx_MOD_150	[2]			
		CHx_MOD_151	[1]			
	CHx_MOD_152	[0]				
	0x33 0x4B 0x63 0x7B	CHx_MOD_153	[7]	0xFF	0xFF	
		CHx_MOD_154	[6]			
		CHx_MOD_155	[5]			
		CHx_MOD_156	[4]			
		CHx_MOD_157	[3]			
		CHx_MOD_158	[2]			
		CHx_MOD_159	[1]			
	CHx_MOD_160	[0]				
	0x34 0x4C 0x64 0x7C	CHx_MOD_161	[7]	0xFF	0xFF	
		CHx_MOD_162	[6]			
		CHx_MOD_163	[5]			
CHx_MOD_164		[4]				
CHx_MOD_165		[3]				
CHx_MOD_166		[2]				
CHx_MOD_167		[1]				
CHx_MOD_168	[0]					
0x35 0x4D 0x65 0x7D	CHx_MOD_169	[7]	0xFF	0xFF		
	CHx_MOD_170	[6]				
	CHx_MOD_171	[5]				
	CHx_MOD_172	[4]				
	CHx_MOD_173	[3]				
	CHx_MOD_174	[2]				
	CHx_MOD_175	[1]				
CHx_MOD_176	[0]					
0x36 0x4E 0x66 0x7E	CHx_MOD_177	[7]	0xFF	0xFF		
	CHx_MOD_178	[6]				
	CHx_MOD_179	[5]				
	CHx_MOD_180	[4]				
	CHx_MOD_181	[3]				
	CHx_MOD_182	[2]				
	CHx_MOD_183	[1]				
CHx_MOD_184	[0]					
0x37 0x4F 0x67 0x7F	CHx_MOD_185	[7]	0xFF	0xFF		
	CHx_MOD_186	[6]				
	CHx_MOD_187	[5]				
	CHx_MOD_188	[4]				
	CHx_MOD_189	[3]				
	CHx_MOD_190	[2]				
	CHx_MOD_191	[1]				
CHx_MOD_192	[0]					

COAXIAL Registers

CH1 Coaxial Register : Bank3 0x00~0x7F

CH2 Coaxial Register : Bank3 0x80~0xFF

CH3 Coaxial Register : Bank4 0x00~0x7F

CH4 Coaxial Register : Bank4 0x80~0xFF

❖ Registers to Control Baud Rate

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x00 / 0x80	CHx_BAUD	[7:0]	0x0E	0x0E	CHx_BAUD (x = Channel Number) : Samsung and A-CP TX Baud Rate
	0x02 / 0x82	CHx_PELCO_BAUD	[7:0]	0x0D	0x0D	CHx_PELCO_BAUD (x = Channel Number) : PELCO TX Baud Rate
Coaxial protocol 1H Line						

❖ Registers to Control Start Point of VBI(Vertical Blank Interval)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x03 / 0x83	CHx_BL_TXST_01	[7:0]	0x0E	0x0E	CHx_BL_TXST_01 (x = Channel Number) : Samsung and A-CP Protocol TX start Line in VBI BL_TXST_01 is Lower 8bit
	0x04 / 0x84	CHx_BL_TXST_02	[3:0]	0x00	0x00	CHx_BL_TXST_02 (x = Channel Number) : Samsung and A-CP Protocol TX start Line in VBI BL_TXST_02 is upper 4bit
	0x05 / 0x85	CHx_ACT_LEN	[3:0]	0x00	0x00	CHx_ACT_LEN (x = Channel Number) : A-CP Line number
	0x07 / 0x87	CHx_PELCO_TXST [7:0]	[7:0]	0x0E	0x0E	CHx_PELCO_TXST_01 (x = Channel Number) : PELCO Protocol TX Start Line in VBI PELCO_TXST_01 is lower 8bit
	0x08 / 0x88	CHx_PELCO_TXST [11:8]	[3:0]	0x00	0x00	CHx_PELCO_TXST_02 (x = Channel Number) : PELCO Protocol TX Start Line in VBI PELCO_TXST_02 is upper 4bit
Coaxial protocol Active Start Point of VBI(Vertical Blank Interval)						

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x09 / 0x89	CHx_COAX_SW_RST	[5]	0x08	0x08	CHx_COAX_SW_RST (x = Channel Number) : Coaxial Software Reset
		CHx_CNT_MODE	[3]			CHx_CNT_MODE (x = Channel Number) : A-CP Protocol Enable Signal
		CHx_TX_START	[0]			CHx_TX_START (x = Channel Number) : A-CP Protocol Enable Signal
	0x0A / 0x8A	CHx_TX_BYTE_LENGTH	[4:0]	0x03	0x03	CHx_TX_BYTE_LENGTH (x = Channel Number) : Transmission amount In Samsung and A-CP Protocol
	0x0B / 0x8B	CHx_PELCO_8BIT	[7]	0x10	0x10	CHx_PELCO_8BIT (x = Channel Number) : Pelco Protocol 8Bit mode Selection 0 : Pelco Protocol Exp mode 1 : Pelco Protocol 8bit mode
		CHx_LINE_8BIT	[5]			CHx_LINE_8BIT (x = Channel Number) : A-CP Protocol Origin Mode Selection 0 : Samsung & Pelco Protocol Mode 1 : A-CP Protocol Origin Mode
		CHx_PACKET_MODE	[2:0]			CHx_PACKET_MODE (x = Channel Number) : Coaxial Protocol Type 0 : Reserved 1 : Samsung Protocol 4 Line Mode 2 : Pelco Protocol Origin Mode 4 : Pelco Protocol Exp mode(Pelco_32bit Mode)
	0x0C / 0x8C	CHx_PELCO_CTEN	[0]	0x00	0x00	CHx_PELCO_CTEN (x = Channel Number) : PELCO Protocol Enable Bit (Active High)
	0x0D / 0x8D	BL_HSP [7:0]	[7:0]	0x30	0x30	CHx_BL_HSP (x = Channel Number) : Start Point in Coaxial Protocol Active Line
	0x0E / 0x8E	BL_HSP [11:8]	[4:0]	0x04	0x04	
0x0F / 0x8F	CHx_PELCO_SHOT	[0]	0x00	0x00	CHx_PELCO_SHOT (x = Channel Number) : PELCO Protocol One Operation Enable signal	

❖ Registers to Control Coaxial Data

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3-4	0x10 / 0x90	CHx_TX_DATA_01	[7:0]	0x00	0x00	CHx_TX_DATA_01 ~ CHx_TX_DATA_04 (x = Channel Number) : 1 st field Data in Samsung and A-CP Protocol
	0x11 / 0x91	CHX_TX_DATA_02	[7:0]	0x10	0x10	
	0x12 / 0x92	CHX_TX_DATA_03	[7:0]	0x18	0x18	
	0x13 / 0x93	CHX_TX_DATA_04	[7:0]	0xFF	0xFF	
	0x14 / 0x94	CHX_TX_DATA_05	[7:0]	0xAA	0xAA	CHx_TX_DATA_05 ~ CHx_TX_DATA_08 (x = Channel Number) : 2 nd field Data in Samsung and A-CP Protocol
	0x15 / 0x95	CHX_TX_DATA_06	[7:0]	0x3C	0x3C	
	0x16 / 0x96	CHX_TX_DATA_07	[7:0]	0xFF	0xFF	
	0x17 / 0x97	CHX_TX_DATA_08	[7:0]	0xFF	0xFF	
	0x18 / 0x98	CHX_TX_DATA_09	[7:0]	0xAA	0xAA	CHx_TX_DATA_09 ~ CHx_TX_DATA_12 (x = Channel Number) : 3 rd field Data in Samsung and A-CP Protocol
	0x19 / 0x99	CHX_TX_DATA_10	[7:0]	0x1B	0x1B	
	0x1A / 0x9A	CHX_TX_DATA_11	[7:0]	0x00	0x00	
	0x1B / 0x9B	CHX_TX_DATA_12	[7:0]	0x00	0x00	
	0x1C / 0x9C	CHX_TX_DATA_13	[7:0]	0xAA	0xAA	CHx_TX_DATA_13 ~ CHx_TX_DATA_16 (x = Channel Number) : 4 th field Data in Samsung and A-CP Protocol
	0x1D / 0x9D	CHX_TX_DATA_14	[7:0]	0x3B	0x3B	
	0x1E / 0x9E	CHX_TX_DATA_15	[7:0]	0x00	0x00	
	0x1F / 0x9F	CHX_TX_DATA_16	[7:0]	0x00	0x00	

❖ Registers to Control Coaxial Data

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3-4	0x20 / 0xA0	CHx_PELCO_TXDAT_01	[7:0]	0x00	0x00	CHx_PELCO_TXDAT_01 ~ CHx_PELCO_TXDAT_02 : 18 th Line in PELCO Protocol (x = Channel Number)
	0x21 / 0xA1	CHx_PELCO_TXDAT_02	[7:0]	0x00	0x00	
	0x22 / 0xA2	CHx_PELCO_TXDAT_03	[7:0]	0x00	0x00	CHx_PELCO_TXDAT_03 ~ CHx_PELCO_TXDAT_04 : 19 th Line in PELCO Protocol (x = Channel Number)
	0x23 / 0xA3	CHx_PELCO_TXDAT_04	[7:0]	0x00	0x00	

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3-4	0x2C / 0xAC	CHx_VSO_INV	[7:0]	0x00	0x00	CHx_VSO_INV (x = Channel Number) : Vertical Sync Inverter (Active High)
	0x2D / 0xAD	CHx_HSO_INV	[7:0]	0x00	0x00	CHx_HSO_INV (x = Channel Number) : Horizontal Sync Inverter (Active High)
	0x2F / 0xAF	CHx_Even_line_modification	[7:0]	0x00	0x00	Control Protocol Active line on each field

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION																				
Bank	Addr			30P	25P																					
3-4	0x3A / 0xBA	CHx_CLEAN	[0]	0x00	0x00	CHx_CLEAN (x = Channel Number) : RX Register is Read Only. So it need clean Condition First, this register set ON. Second, Read I2C Protocol 0x90. And then Clean the Samsung RX Registers.																				
	0x3B / 0xBB	CHx_AUTO	[7]	0x00	0x00	CHx_AUTO (x = Channel Number) : Control PELCO Protocol Sequence simply Enable AUTO, and then Whenever writes I2C Protocol 0x94, Pelco Protocol is generated Automatically																				
		CHx_CMD_LIST	[4:0]			CHx_CMD_LIST (x = Channel Number) : PELCO Command List <table style="width: 100%; border: none;"> <tr> <td>00 : SET</td> <td>01 : UP</td> </tr> <tr> <td>02 : DOWN</td> <td>03 : LEFT</td> </tr> <tr> <td>04 : RIGHT</td> <td>05 : OSD ON</td> </tr> <tr> <td>06 : IRS_OPEN</td> <td>07 : IRS_CLOSE</td> </tr> <tr> <td>08 : FOCUS NEAR</td> <td>09 : FOCUS FAR</td> </tr> <tr> <td>0A : ZOOM WIDE</td> <td>0B : ZOOM TILT</td> </tr> <tr> <td>0C : SC1 SR</td> <td>0D : SC1 ST</td> </tr> <tr> <td>0E : PRE SET 1</td> <td>0F : PRE SET 2</td> </tr> <tr> <td>10 : PRE SET 3</td> <td>11 : PT 1 SR</td> </tr> <tr> <td>12 : PT 1 ST</td> <td>13 : PT 2 SR</td> </tr> <tr> <td>14 : PT 2 ST</td> <td>15 : PT 3 SR</td> </tr> <tr> <td>16 : PT 3 ST</td> <td>17 : PT RUN</td> </tr> </table> Default : CLEAN (all '0')	00 : SET	01 : UP	02 : DOWN	03 : LEFT	04 : RIGHT	05 : OSD ON	06 : IRS_OPEN	07 : IRS_CLOSE	08 : FOCUS NEAR	09 : FOCUS FAR	0A : ZOOM WIDE	0B : ZOOM TILT	0C : SC1 SR	0D : SC1 ST	0E : PRE SET 1	0F : PRE SET 2	10 : PRE SET 3	11 : PT 1 SR	12 : PT 1 ST	13 : PT 2 SR
00 : SET	01 : UP																									
02 : DOWN	03 : LEFT																									
04 : RIGHT	05 : OSD ON																									
06 : IRS_OPEN	07 : IRS_CLOSE																									
08 : FOCUS NEAR	09 : FOCUS FAR																									
0A : ZOOM WIDE	0B : ZOOM TILT																									
0C : SC1 SR	0D : SC1 ST																									
0E : PRE SET 1	0F : PRE SET 2																									
10 : PRE SET 3	11 : PT 1 SR																									
12 : PT 1 ST	13 : PT 2 SR																									
14 : PT 2 ST	15 : PT 3 SR																									
16 : PT 3 ST	17 : PT RUN																									

❖ Registers to Read Coaxial Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x40 / 0xC0	CHx_ORIGIN_A_00	[7:0]	Read	Read	CHx_ORIGIN_A_00 ~ CHx_ORIGIN_A_05 (x = Channel Number) : In the RX mode, data of parsing coaxial signal in first line.
	0x41 / 0xC1	CHx_ORIGIN_A_01	[7:0]	Read	Read	
	0x42 / 0xC2	CHx_ORIGIN_A_02	[7:0]	Read	Read	
	0x43 / 0xC3	CHx_ORIGIN_A_03	[7:0]	Read	Read	
	0x44 / 0xC4	CHx_ORIGIN_A_04	[7:0]	Read	Read	
	0x45 / 0xC5	CHx_ORIGIN_A_05	[7:0]	Read	Read	
	0x46 / 0xC6	CHx_ORIGIN_B_00	[7:0]	Read	Read	CHx_ORIGIN_B_00 ~ CHx_ORIGIN_B_05 (x = Channel Number) : In the RX mode, data of parsing coaxial signal in second line.
	0x47 / 0xC7	CHx_ORIGIN_B_01	[7:0]	Read	Read	
	0x48 / 0xC8	CHx_ORIGIN_B_02	[7:0]	Read	Read	
	0x49 / 0xC9	CHx_ORIGIN_B_03	[7:0]	Read	Read	
	0x4A / 0xCA	CHx_ORIGIN_B_04	[7:0]	Read	Read	
	0x4B / 0xCB	CHx_ORIGIN_B_05	[7:0]	Read	Read	
	0x50 / 0xD0	CHx_ORIGIN_C_00	[7:0]	Read	Read	CHx_ORIGIN_C_00 ~ CHx_ORIGIN_C_05 (x = Channel Number) : In the RX mode, data of parsing coaxial signal in third line.
	0x51 / 0xD1	CHx_ORIGIN_C_01	[7:0]	Read	Read	
	0x52 / 0xD2	CHx_ORIGIN_C_02	[7:0]	Read	Read	
	0x53 / 0xD3	CHx_ORIGIN_C_03	[7:0]	Read	Read	
	0x54 / 0xD4	CHx_ORIGIN_C_04	[7:0]	Read	Read	
	0x55 / 0xD5	CHx_ORIGIN_C_05	[7:0]	Read	Read	
	0x56 / 0xD6	CHx_ORIGIN_D_00	[7:0]	Read	Read	CHx_ORIGIN_D_00 ~ CHx_ORIGIN_D_05 (x = Channel Number) : In the RX mode, data of parsing coaxial signal in fourth line.
	0x57 / 0xD7	CHx_ORIGIN_D_01	[7:0]	Read	Read	
0x58 / 0xD8	CHx_ORIGIN_D_02	[7:0]	Read	Read		
0x59 / 0xD9	CHx_ORIGIN_D_03	[7:0]	Read	Read		
0x5A / 0xDA	CHx_ORIGIN_D_04	[7:0]	Read	Read		
0x5B / 0xDB	CHx_ORIGIN_D_05	[7:0]	Read	Read		

❖ Registers to Read Coaxial Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3-4	0x5C / 0xDC	CHx_RX_DONE	[0]	Read	Read	CHx_RX_DONE (x = Channel Number) : Coaxial RX Request Done

❖ Registers to Read Coaxial Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3-4	0x5D / 0xDD	CHx_RX_COAX_DUTY	[7:0]	Read	Read	CHx_RX_COAX_DUTY (x = Channel Number) : Coaxial RX 8bit DUTY Read

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3-4	0x60 / 0xE0	CHx_DEVICE_ID	[7:0]	0x84	0x84	CHx_DEVICE_ID (x = Channel Number) : Define Device_ID in Protocol's Header
	0x62 / 0xE2	CHx_RX_AREA	[7:0]	0x00	0x00	CHx_RX_AREA (x = Channel Number) : Coaxial RX Area 8-bit
	0x63 / 0xE3	CHx_DELAY_ON	[4]	0x01	0x01	CHx_DELAY_ON (x = Channel Number) : Delay Input CVBS signal which enable or disable
		CHx_COMM_ON	[0]			CHx_COMM_ON (x = Channel Number) : Coaxial RX Software Reset
	0x64 / 0xE4	CHx_DELAY_CNT	[7:0]	0x00	0x00	CHx_DELAY_CNT (x = Channel Number) : How many delay input signal based clock

❖ Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3-4	0x65 / 0xE5	CHx_MSB	[0]	0x01	0x01	CHx_MSB (x = Channel Number) : Coaxial RX MSB Change Mode
	0x66 / 0xE6	CHx_A_DUTY_ON	[7]	0x80	0x80	CHx_A_DUTY_ON (x = Channel Number) : Coaxial RX DUTY Mode
	0x67 / 0xE7	CHx_INT_MODE	[0]	0x01	0x01	CHx_INT_MODE (x = Channel Number) : Coaxial RX Interrupt Mode
	0x68 / 0xE8	CHx_RX_SZ	[7:4]	0x50	0x50	CHx_RX_SZ (x = Channel Number) : Coaxial RX Line MAX Set
	0x69 / 0xE9	CH1_M_DUTY	[7:0]	0x00	0x00	CH1_M_DUTY (x = Channel Number) : Coaxial RX DUTY Set
	0x6A / 0xEA	CH1_RX_START_POSITION	[7:0]	0x00	0x00	CH1_RX_START_POSITION (x = Channel Number) : Coaxial RX Start Point in Line

❖ Registers to Read Coaxial Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x70 / 0xF0	CHx_PELCO16_00 [7:0]	[7:0]	Read	Read	CHx_PELCO16_00 (x = Channel Number) : Coaxial Output 16bit Data1 Read Register
	0x71 / 0xF1	CHx_PELCO16_00 [15:8]	[7:0]	Read	Read	
	0x72 / 0xF2	CHx_PELCO16_01 [7:0]	[7:0]	Read	Read	CHx_PELCO16_01 (x = Channel Number) : Coaxial Output 16bit Data2 Read Register
	0x73 / 0xF3	CHx_PELCO16_01 [15:8]	[7:0]	Read	Read	
	0x78 / 0xF8	CHx_PELCO8_0	[7:0]	Read	Read	CHx_PELCO8_0 (x = Channel Number) : Coaxial Output 8bit Data1 Read Register
	0x79 / 0xF9	CHx_PELCO8_1	[7:0]	Read	Read	CHx_PELCO8_1 (x = Channel Number) : Coaxial Output 8bit Data2 Read Register
	0x7A / 0xFA	CHx_PELCO8_2	[7:0]	Read	Read	CHx_PELCO8_2 (x = Channel Number) : Coaxial Output 8bit Data3 Read Register
	0x7B / 0xFB	CHx_PELCO8_3	[7:0]	Read	Read	CHx_PELCO8_3 (x = Channel Number) : Coaxial Output 8bit Data4 Read Register

* Registers of Bank5~BankB are not for users.

7. Electrical characteristics

7.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V _{VDD1DM}	0.5	-	1.32	V
3.3V Digital Power Supply Voltage	V _{VDD3DM}	0.5	-	3.6	V
3.3V Analog Power Supply Voltage	V _{VDD3AM}	0.5	-	3.6	V
Voltage for Digital pins	V _{DIO}	0.5	-	4.6	V
Voltage for Analog Inputs	V _{AIO}	0.5	-	1.95	V
Storage Temperature	T _S	-40	-	125	°C
Junction Temperature	T _J	-40	-	125	°C
Vapor phase soldering (15 Sec)	T _{VSO}	-	-	220	°C

Note : This Device should be operated under recommended operating condition. Since, absolute maximum rating condition can either cause device reliability problem or damage the device sufficiently to cause immediate failure.

7.2. Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
1.2V Digital Power Supply Voltage	V _{VDD1D}	1.08	1.2	1.32	V
3.3V Digital Power Supply Voltage	V _{VDD3D}	3.0	3.3	3.6	V
3.3V Analog Power Supply Voltage	V _{VDD3A}	3.0	3.3	3.6	V
Ambient operating temperature	V _A	0	-	70	°C

7.3. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V _{IL}	-0.3	-	0.8	V
Input High Voltage	V _{IH}	2	-	V _{DD3D} +0.3	V
Input Leakage Current	I _L	-	-	±1	µA
Input Capacitance (f = 1Mhz, V _{IN} = 2.4V)	C _{IN}	-	-	10	pF
Output Low Voltage (I _{OL} = 8.0mA)	V _{OL}	-	-	0.4	V
Output High Voltage (I _{OH} = 12mA)	V _{OH}	2.4	-	-	V
Tri-State Output Leakage Current	I _{OZ}	-	-	±1	µA
Output Capacitance	C _{OUT}	-	-	10	pF

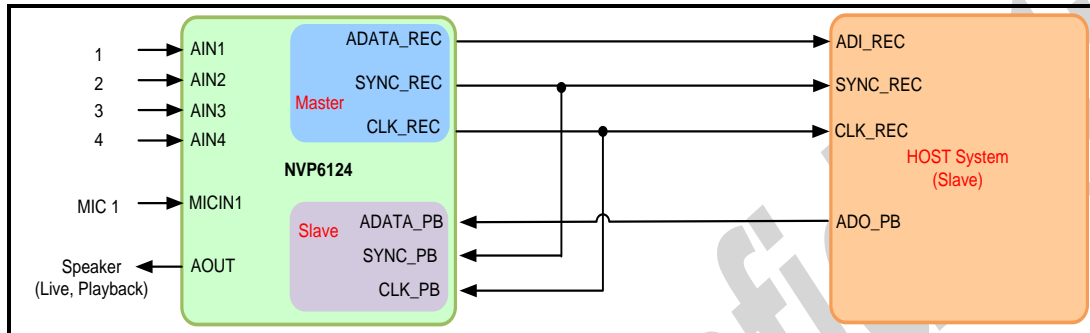
7.4. AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
(Power Supply Current)					
1.2V Digital Power Supply Current	I _{VDD1D}	-	230	-	mA
3.3V Digital Power Supply Current	I _{VDD3D}	-	110	-	mA
3.3V Analog Power Supply Current	I _{VDD3A}	-	100	-	mA
(Clock Pin)					
XTALI frequency	f _{XTALI}	-	27.0	-	MHz
XTALI duty cycle	f _{DUTY}	45	-	55	%
XTALI pulse width low	t _{PWL_XTALI}	17.0	-	-	nSec
XTALI pulse width high	t _{PWH_XTAL}	17.0	-	-	nSec
(Reset Pin)					
RSTB setup time	t _{SU}	1			uSec
RSTB pulse width low	t _{PWL_rstb}	1			uSec
RSTB release time (low to high)	t _{REL_rstb}	10			uSec
(Host Interface Pins)					
SCL frequency	f _{SCL}	-	-	6	XTALI
SCL minimum pulse width low	t _{PWL_SCL}	6	-	-	XTALI
SCL minimum pulse width high	t _{PWH_SCL}	4	-	-	XTALI
SCL to SDA setup time	t _{IS_SDA}	2	-	-	XTALI
SCL to SDA hold time	t _{IH_SDA}	2	-	-	XTALI
SCL to SDA delay time	t _{OD_SDA}	-	-	6	XTALI
SCL to SDA hold time	t _{OH_SDA}	3	-	-	XTALI

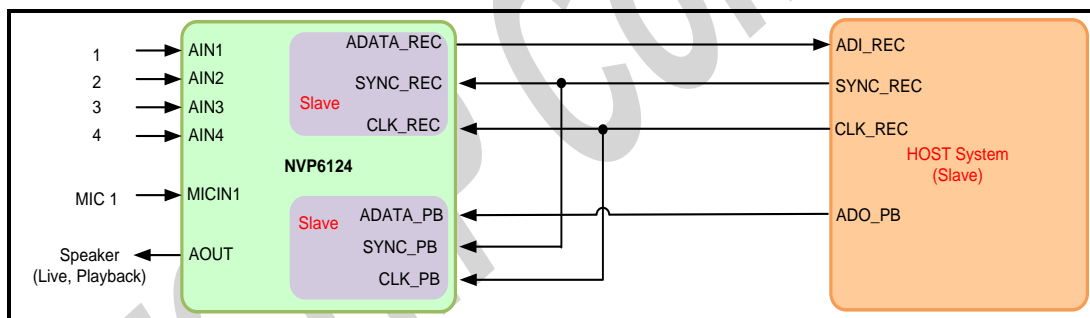
8. System Applications

8.1. 4-Channel, Master Mode

8.1.1. Block Diagram (4 channel, Master Mode)

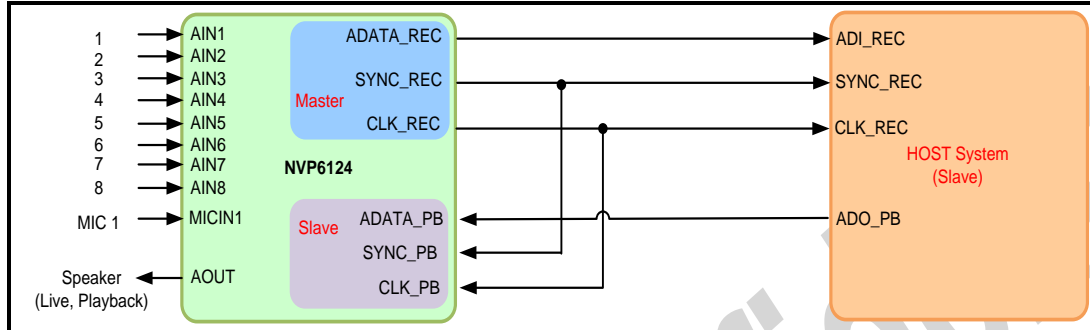


8.1.2. Block Diagram (4 channel, Slave Mode)

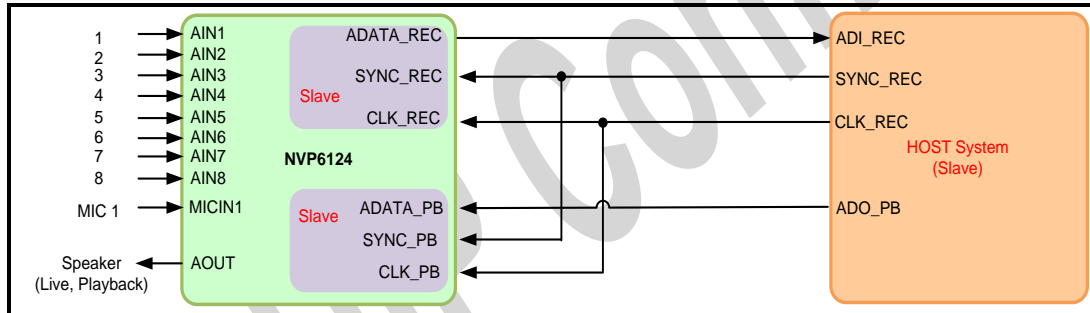


8.2. 8-Channel, Master Mode

8.2.1. Block Diagram (8 Channel, Master Mode)

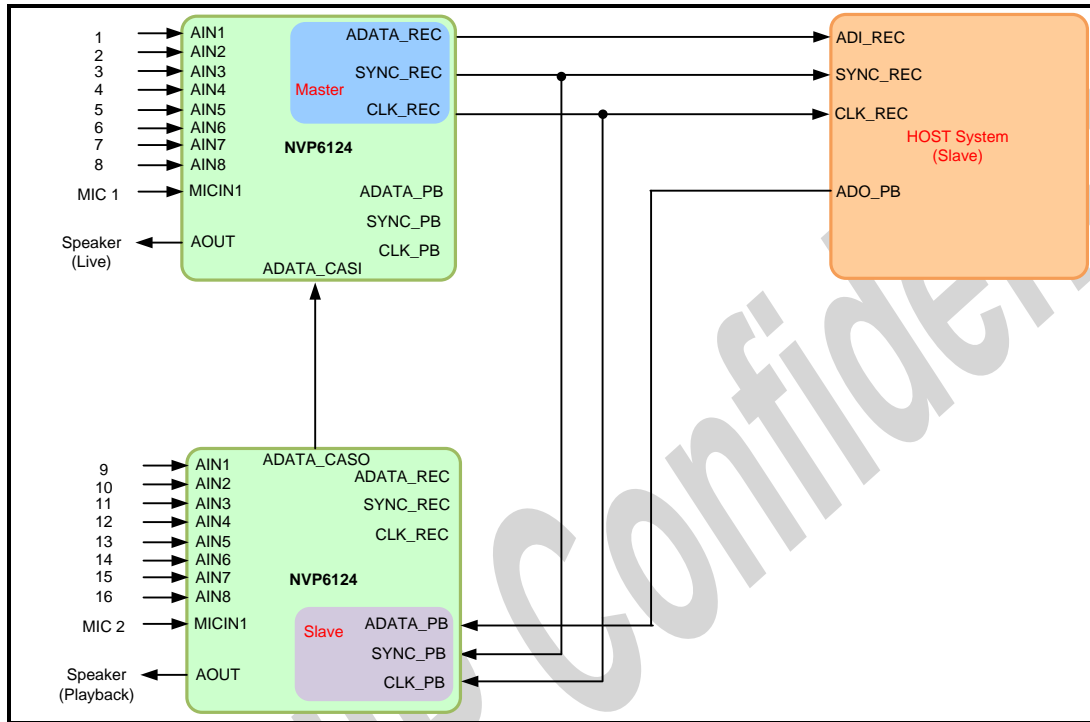


8.2.2. Block Diagram (8 Channel, Slave Mode)

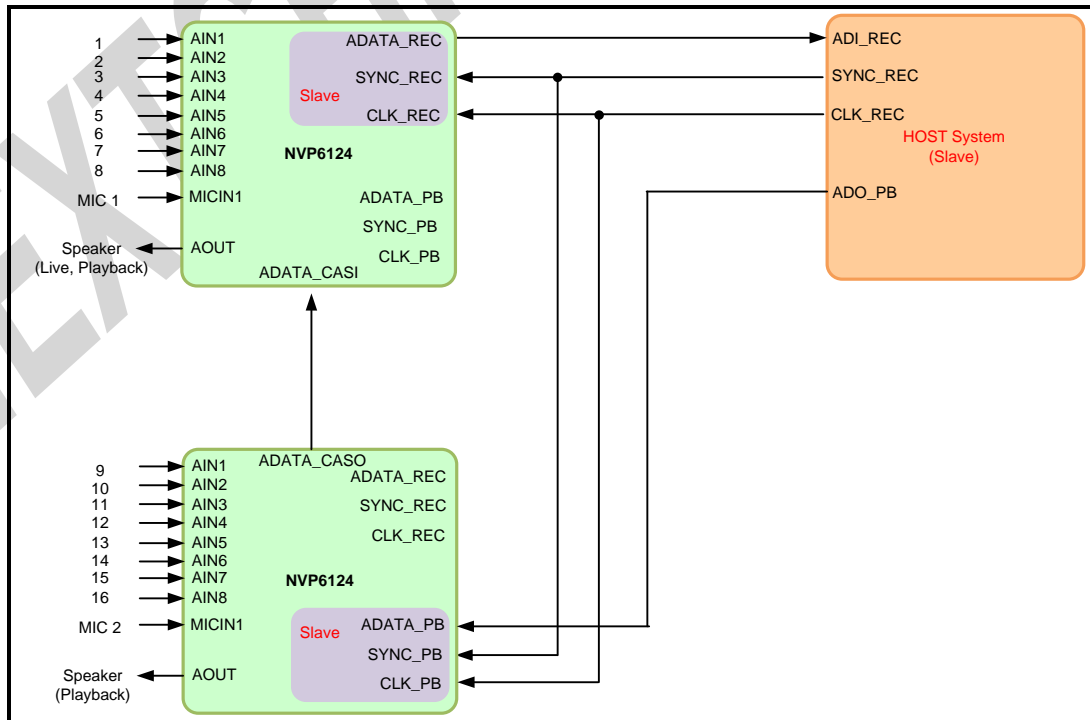


8.3. 16-Channel, Master Mode

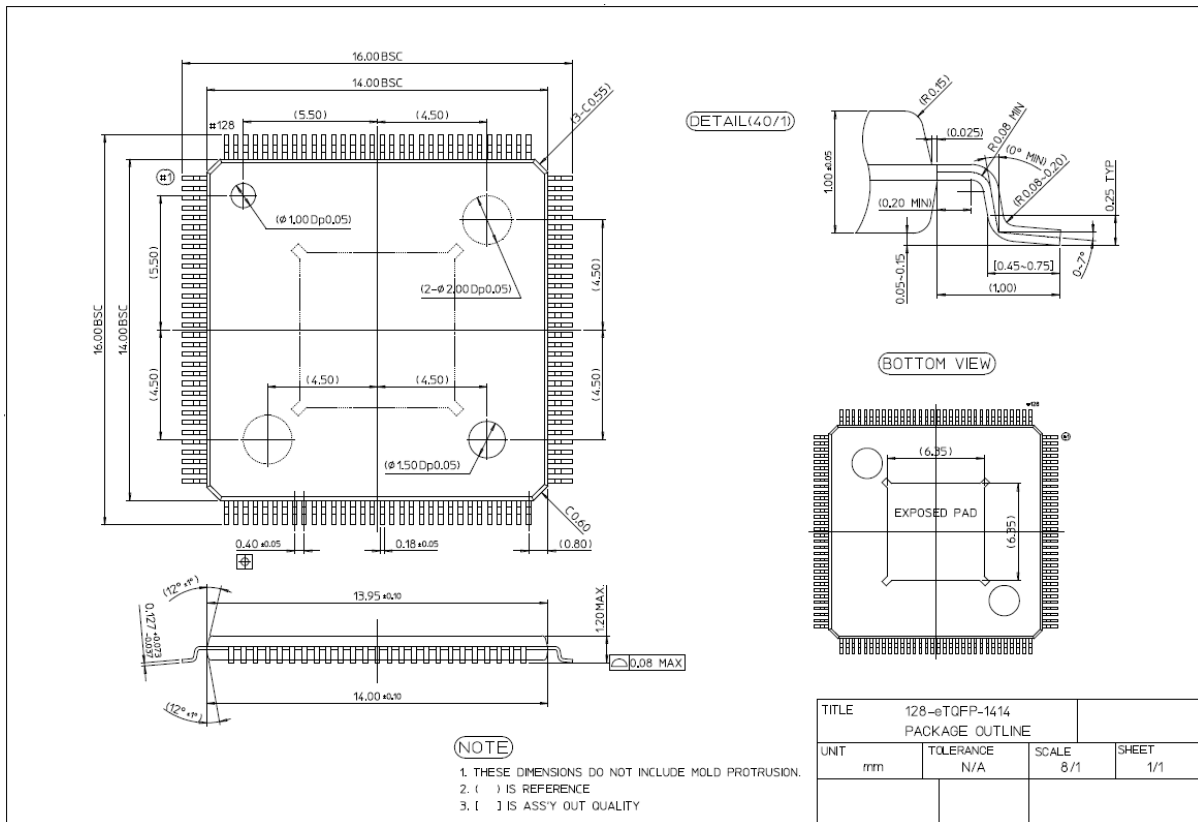
8.3.1. Block Diagram (16 Channel, Master Mode)



8.3.2. Block Diagram (16 Channel, Slave Mode)



9. Package Information



* Please refer to application note for further details.