300kHz & 600kHz SYNCHRONOUS PWM CONTROLLER WITH PROGRAMMABLE BUS UVLO

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2113 controller IC is a synchronous Buck controller IC designed for step down DC to DC converter applications. Synchronous control operation replaces the traditional catch diode with an Nch MOSFET resulting in improved converter efficiency. The NX2113 controller is optimized to convert bus voltages from 2V to 25V to outputs as low as 0.8V voltage using Enable pin to program the BUS voltage start up threshold. The NX2113 operates at 300kHz while 2113A is set at 600kHz operation which together with less than 50 nS of dead band provides an efficient and cost effective solution. Other features of the device are:

Internal digital soft start; Vcc undervoltage lock out; Output undervoltage protection with digital filter and shut-down capability via the enable pin.

FEATURES

- Synchronous Controller in 10 Pin Package
- Bus voltage operation from 2V to 25V
- Enable pin allows programmable BUS UVLO
- Less than 50 nS adaptive deadband
- Internal 300kHz for 2113 and 600kHz for 2113A
- Internal Digital Soft Start Function
- Separated power ground and analog ground for extra noise filtering
- Pb-free and RoHS compliant

APPLICATIONS

- Graphic Card on board converters
- Memory Vcore or Vddq supply
- On board DC to DC such as 12V, 5V to 3.3V, 2.5V or 1.8V
- Hard Disk Drive

TYPICAL APPLICATION

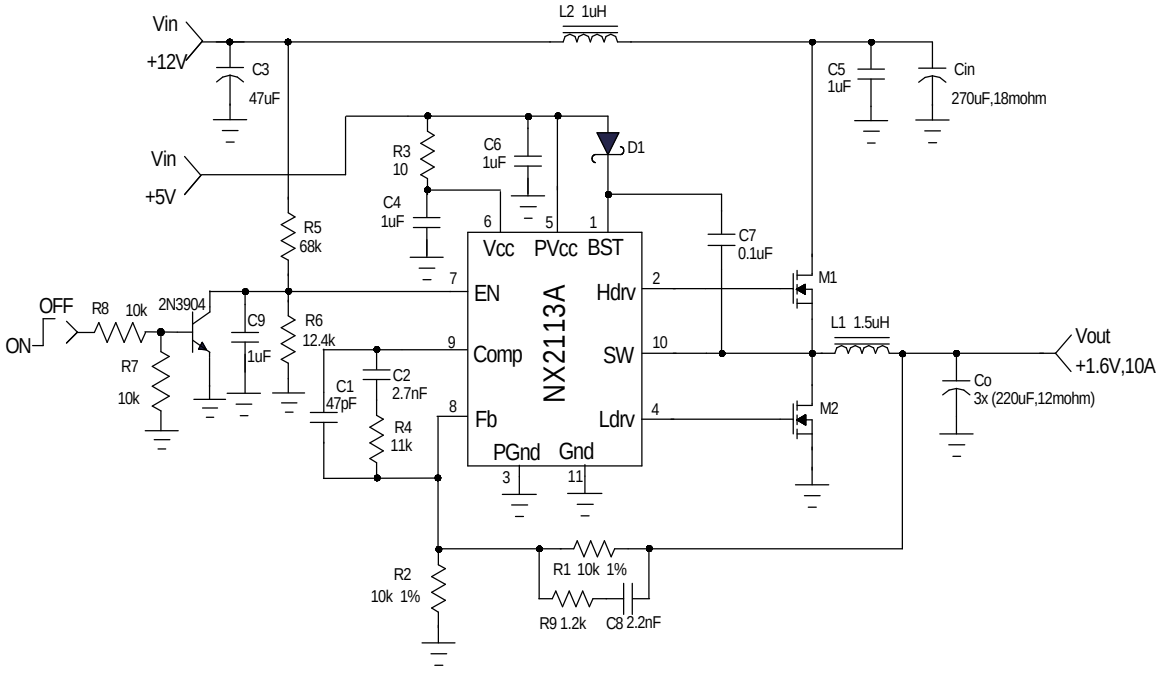

Figure1 - Typical application of 2113A

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2113CMTR	0 to 70°C	MLPD-10L	300kHz	Yes
NX2113CUTR	0 to 70° C	MSOP-10L	300kHz	Yes
NX2113ACMTR	0 to 70°C	MLPD-10L	600kHz	Yes
NX2113ACUTR	0 to 70° C	MSOP-10L	600kHz	Yes

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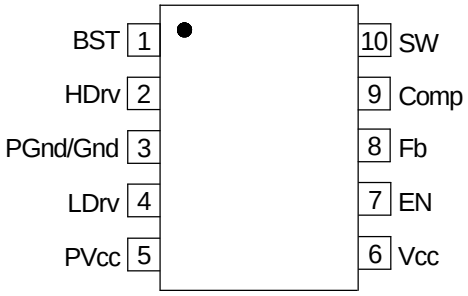
ABSOLUTE MAXIMUM RATINGS

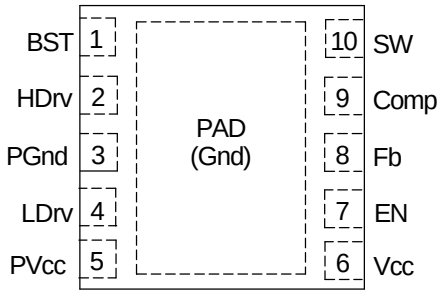
Vcc to GND & BST to SW voltage 6.5V
BST to GND Voltage 35V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

10-LEAD PLASTIC MSOP	10-LEAD PLASTIC MLPD
$\theta_{JA} \approx 200^{o}C/W$	$\theta_{JA} \approx 52^{o}C/W$





ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}	4.5V<Vcc<5.5V		0.8		V
Ref Voltage line regulation				0.4		%
Supply Voltage(Vcc)						
V_{CC} Voltage Range	V_{CC}		4.5	5	5.5	V
V_{CC} Supply Current (Static)	I_{CC} (Static)	Outputs not switching		2.1		mA
V_{CC} Supply Current (Dynamic)	I_{CC} (Dynamic)	C_{LOAD}=3300pF F_S=300kHz		5		mA
Supply Voltage(V_{BST})						
V_{BST} Supply Current (Static)	I_{BST} (Static)	Outputs not switching		0.15		mA
V_{BST} Supply Current (Dynamic)	I_{BST} (Dynamic)	C_{LOAD}=3300pF F_S=300kHz		5		mA
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		4.1		V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.22		V
SS						
Soft Start time	Tss	Fsw=300Khz, 2113 Fsw=600Khz, 2113A		3.4 1.7		mS

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Oscillator (Rt)						
Frequency	F_S	2113		300		kHz
		2113A		600		kHz
Ramp-Amplitude Voltage	V_{RAMP}			2.1		V
Max Duty Cycle				93		%
Min Duty Cycle					0	%
Error Amplifiers						
Transconductance				2100		umho
Input Bias Current	Ib			10		nA
FB Under Voltage Protection						
FB Under voltage threshold				0.4		V
EN						
Enable Threshold Voltage		Enable ramp up		1.25		V
Enable Hysterises				0.2		V
High Side Driver(CL=3300pF)						
Output Impedance , Sourcing Current	R_{source}(Hdrv)	I=200mA		1.1		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	I=200mA		0.8		ohm
Rise Time	THdrv(Rise)	V_{BST}-V_{SW}=4.5V		50		ns
Fall Time	THdrv(Fall)	V_{BST}-V_{SW}=4.5V		50		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10%-10%		30		ns
Low Side Driver (CL=3300pF)						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1.1		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		0.5		ohm
Rise Time	TLdrv(Rise)	10% to 90%		50		ns
Fall Time	TLdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		30		ns

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PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1 uF must be connected from this pin to SW pin.
2	HDRV	High side MOSFET gate driver.
3	PGND/Gnd	Power and analog ground pin. For MLPD package, analog ground and power ground are separated, additional pad pin(11) is available for analog ground.
4	LDRV	Low side MOSFET gate driver.
5	PVcc	Ldrv supply voltage. A 1uF high frequency cap must be connected from this pin to GND directly.
6	Vcc	Voltage supply for the internal circuit as well as the low side MOSFET gate driver. A 1uF high frequency ceramic capacitor must be connected from this pin to GND pin.
7	EN	Pull up this pin to Vcc for normal operation. Pulling this pin down below 1.25V shuts down the controller and resets the soft start. This pin can also be used as a UVLO detector for the bus voltage via a resistor divider.
8	FB	This pin is the error amplifier inverting input. This pin is also connected to the output UVLO comparator. When this pin falls below 0.4V, both HDRV and LDRV outputs are latched off.
9	COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop.
10	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.

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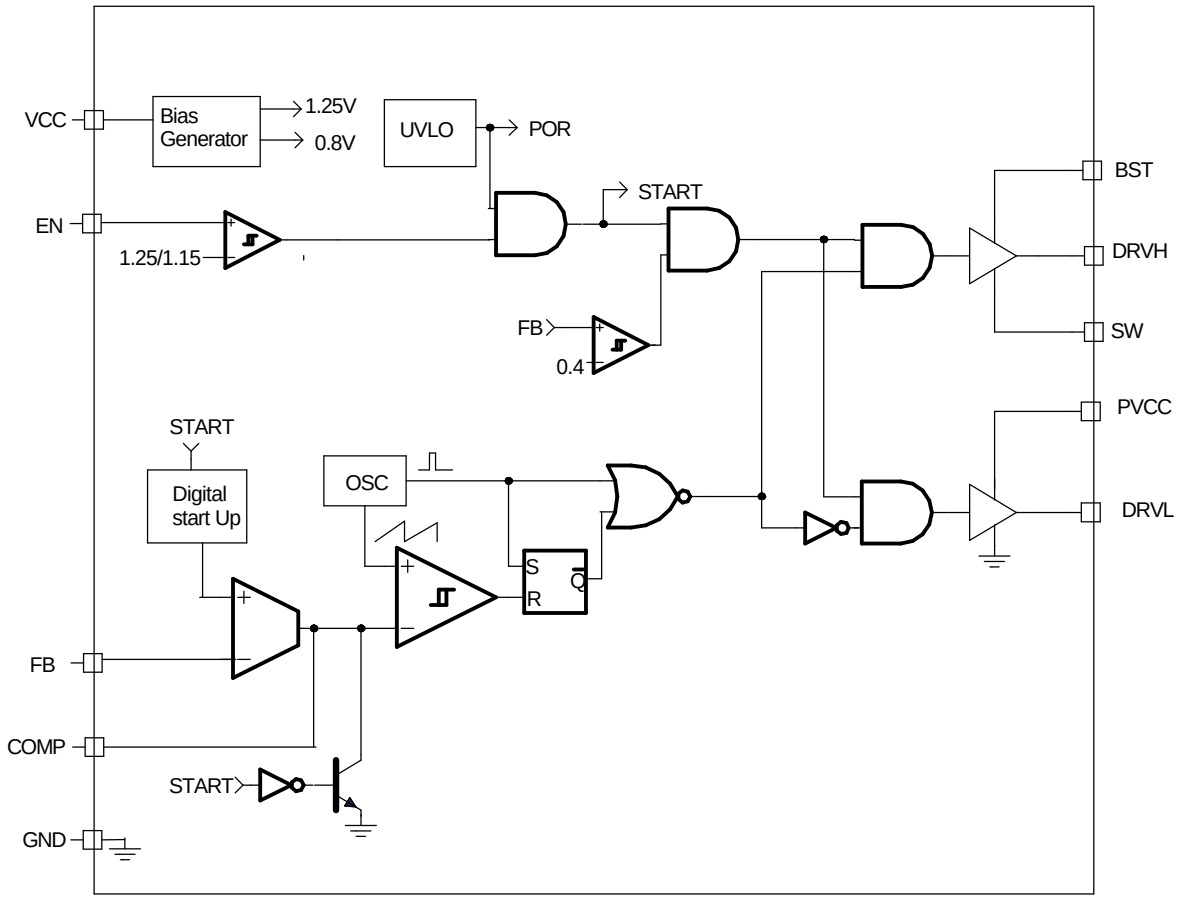
BLOCK DIAGRAM



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Demo Board Schematic

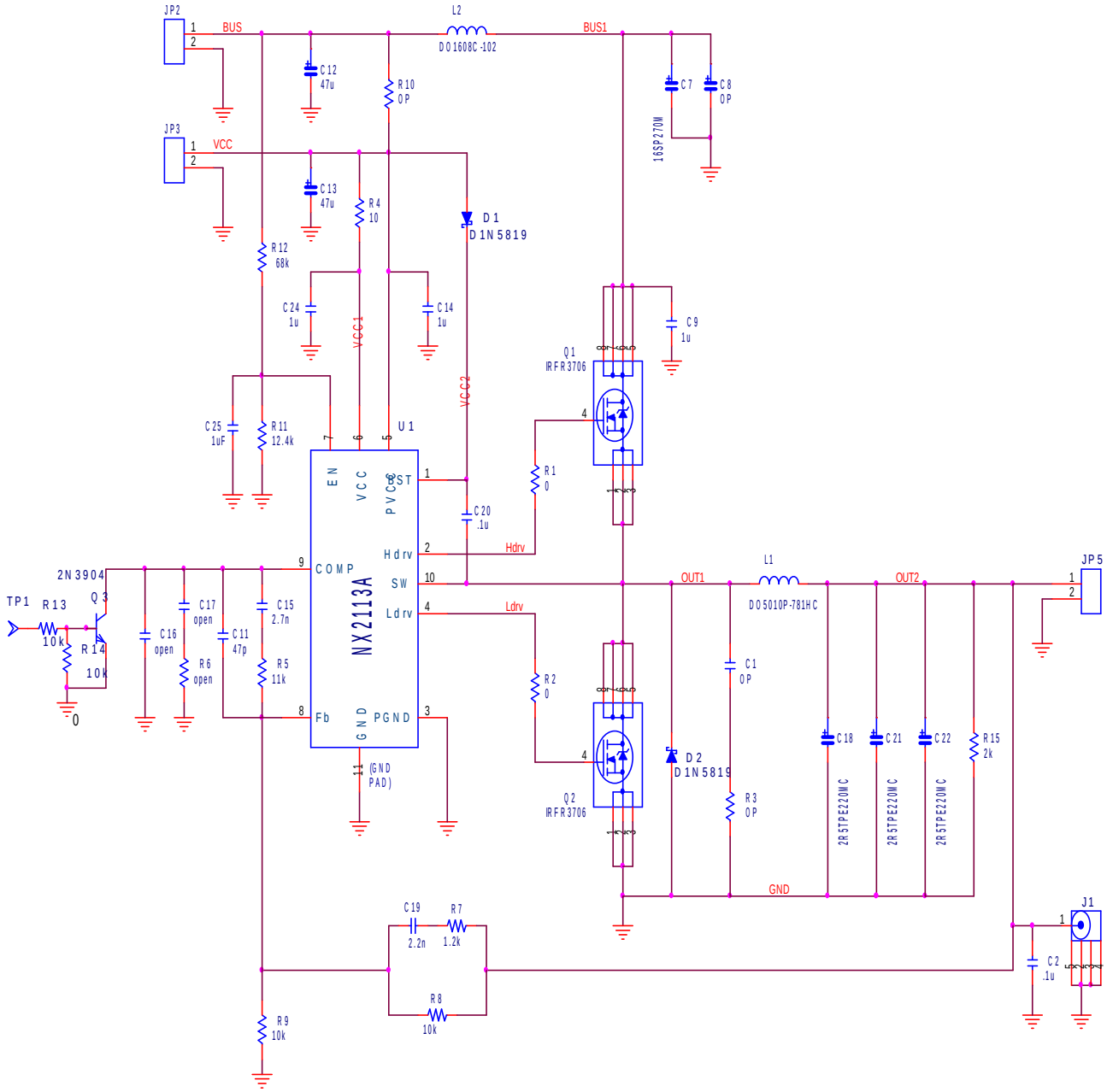

Figure 2 - Demoboard design on NX2113A

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Bill of Materials

Item	Quantity	Reference	Part	Manufacture
1	6	C1,R3,C8,R10,C23,D2	OPEN	
2	2	C2,C20	.1uF	
3	1	C7	16SP270M	SANYO
4	3	C9,C14,C24	1uF	
5	1	C11	47pF	
6	2	C12,C13	47uF	
7	1	C15	2.7nF	
8	3	R6,C16,C17	OPEN	
9	3	C18,C21,C22	220uF 2R5TPE220MC	SANYO
10	1	C19	2.2nF	
11	1	C25	1uF	
12	2	D1	D1N5819	
13	3	JP2,JP3,JP5	CON2	
14	2	J1	SCOPE TP	Tektronics
15	1	L1	DO5010P-781HC	Coilcraft
16	1	L2	DO1608C-102	Coilcraft
17	2	Q1,Q2	IRFR3706	International Rectifier
18	1	Q3	2N3904	
19	2	R1,R2	0	
20	1	R4	10	
21	1	R5	11k	
22	2	R8,R9,R13,R14	10k	
23	1	R7	1.2k	
24	1	R11	12.4k	
25	1	R12	68k	
26	1	R15	2k	
27	1	U1	NX2113	NEXSEM INC.

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DEMO BOARD WAVEFORM

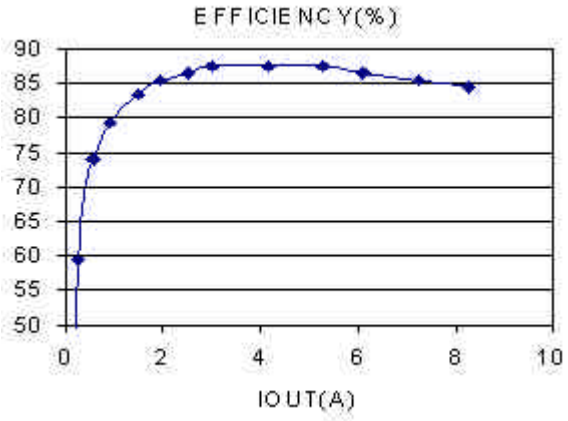

Figure 3: Output efficiency

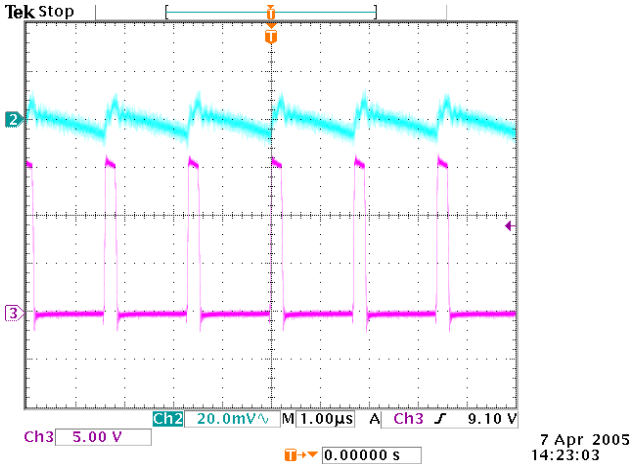

Figure 4: Voltage ripple @1.6 V output voltage. (Ch2-ripple, Ch3-Hdrv)

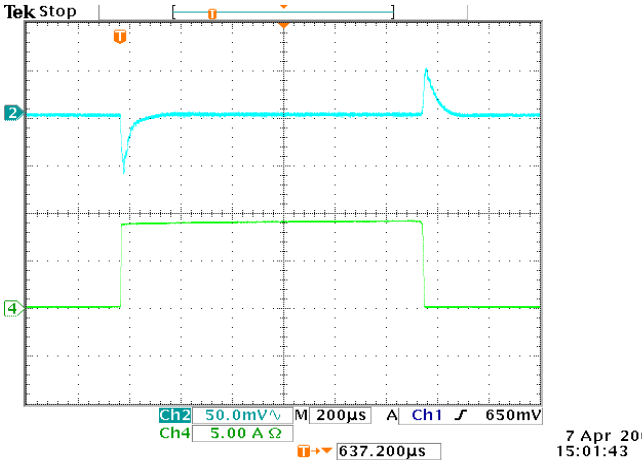

Figure 5: Output voltage transient response for load curent 0A-9A

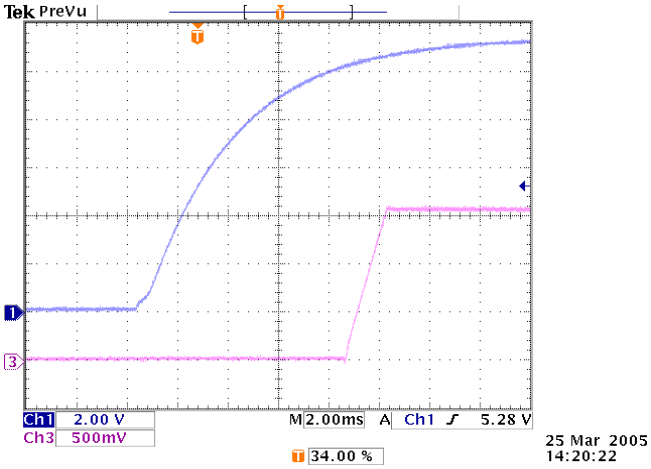

Figure 6: Start up time(Ch1-input volatge, Ch2-output voltage)

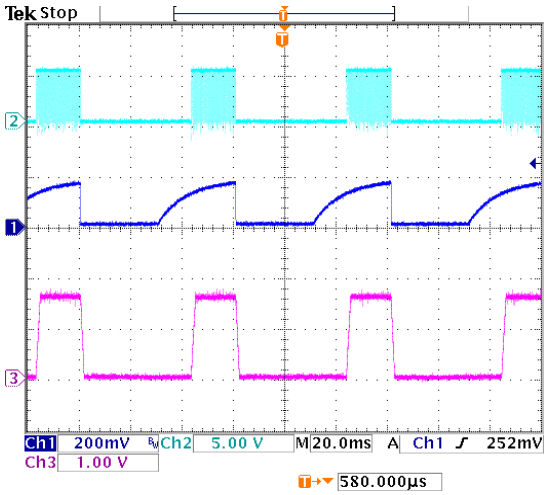

Figure 7: ENABLE function.(Ch1-enable, Ch2-Ldrv, Ch3-output voltage)

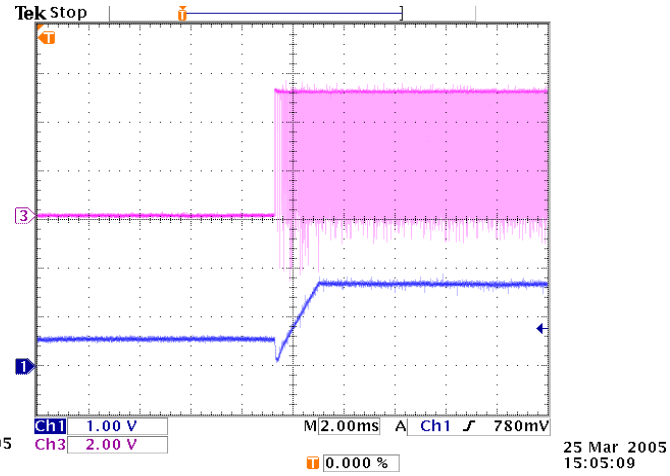

Figure 8: Startup operation waveform

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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage

V_{OUT} - Output voltage

I_{OUT} - Output current

ΔV_{RIPPLE} - Output voltage ripple

F_S - Working frequency

ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX2113A, the schematic is figure 2.

V_{IN} = 12V

V_{OUT}=1.6V

I_{OUT}=10A

ΔV_{RIPPLE}<=20mV

ΔV_{DROOP}<=80mV @ 10A step

F_S=600kHz

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, switching frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{\Delta I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.

Select k=0.3, then

$$L_{OUT}=\frac{12V-1.6V}{0.3\times 10A}\times\frac{1.6V}{12V}\times\frac{1}{600kHz}$$

$$L_{OUT}=0.8uH$$

Choose inductor from COILCRAFT DO5010P-781HC with L=0.78uH is a good choice.

Current Ripple is recalculated as

$$\Delta I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$

$$=\frac{12V-1.6V}{0.78uH}\times\frac{1.6v}{12v}\times\frac{1}{600kHz}=3A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, POSCAP are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{20mV}{3A}=6.7m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 20mV output ripple, POSCAP 2R5TPE220MC with 12mΩ are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N=\frac{12m\Omega\times 3A}{20mV}$$

N =1.8

The number of capacitor has to be round up to a integer. Choose N =2.

If ceramic capacitors are chosen as output ca-

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pacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors .

For example, one 100uF, X5R ceramic capacitor with 2mΩ ESR is used. The amount of output ripple is

$$\Delta V_{RIPPLE} = 2m\Omega \times 3A + \frac{3A}{8 \times 600kHz \times 100uF}$$
$$= 6mV + 6.2mV = 12.2mV$$

Although this meets DC ripple spec, however it needs to be studied for transient requirement.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as:

$\Delta V_{DROOP} < \Delta V_{TRAN}$ @ step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One Section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot, when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is dependent on the ESR of capacitor.

In most cases, the output capacitors are multiple capacitors in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 100mV for 10A load step.

If the POSCAP 2R5TPE220MC(220uF, 12mΩ) is used, the critical inductance is given as:

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} =$$
$$\frac{12m\Omega \times 220\mu F \times 1.6V}{10A} = 0.42\mu H$$

The selected inductor is 0.78uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitors is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E$$
$$= \frac{0.78\mu H \times 10A}{1.6V} - 12m\Omega \times 220\mu F = 2.24us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2$$
$$= \frac{12m\Omega \times 10A}{80mV} +$$
$$\frac{1.6V}{2 \times 1.5\mu H \times 220\mu F \times 80mV} \times (2.24us)^2$$
$$\approx 1.7$$

The number of capacitors has to satisfy both ripple and transient requirement. Overall, we can choose N=3.

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It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 10.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1-g_m\times Z_f}{1+g_m\times Z_{in}+Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R4>>2/gm. R1||R2||R3>>1/gm is desirable.

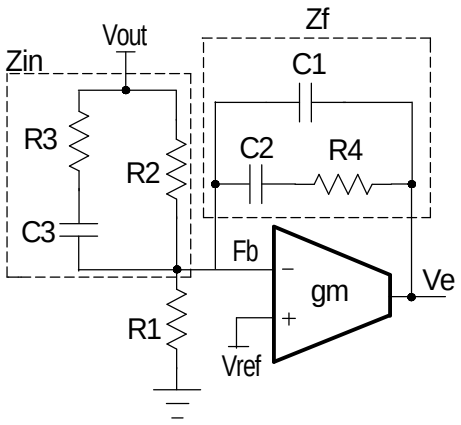

Figure 9 - Type III compensator using transconductance amplifier

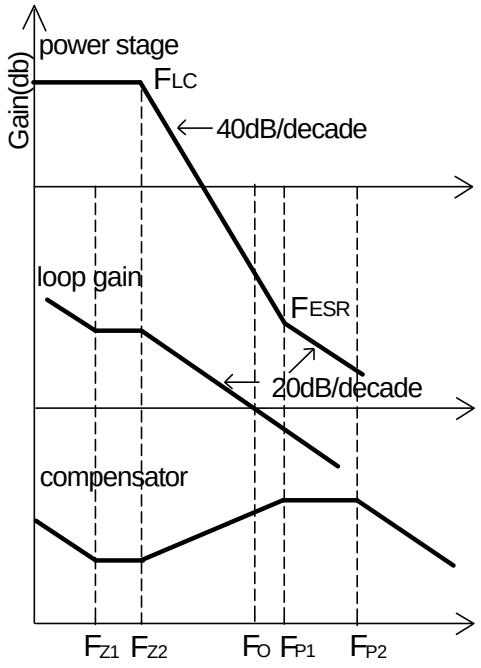

Figure 10 - Bode plot of Type III compensator

Design example for type III compensator are in order. Use the same power stage requirement as demo board. The crossover frequency has to be selected as $F_{LC}<F_O<F_{ESR,}$ and $F_O<=1/10~1/5F_s$.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{0.78uH\times 660uF}}$$
$$=7kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times 4m\Omega\times 660uF}$$
$$=60kHz$$

2.Set R_2 equal to10kΩ, then R_1= 10kΩ.

3. Set zero F_{Z2} = F_{LC} and F_{p1} =F_{ESR} .

4. Calculate R_4 and C_3 with the crossover frequency smaller than 1/10~ 1/5 of the switching frequency. Set F_O=45kHz.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)$$
$$=\frac{1}{2\times\pi\times 10k\Omega}\times\left(\frac{1}{7kHz}-\frac{1}{60kHz}\right)$$
$$=2nF$$

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out}$$
$$=\frac{2V}{12V}\times\frac{2\times\pi\times 45kHz\times 0.78uH}{2.2nF}\times 660uF$$
$$=11k\Omega$$

Choose C_3=2.2nF, R_4=11kΩ.

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{z1}\times R_4}$$
$$=\frac{1}{2\times\pi\times 0.75\times 7kHz\times 11k\Omega}$$
$$=2.75nF$$

Choose C_2=2.7nF.

6. Calculate C_1 by equation (14) with pole F_{p2} at half the swithing frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}$$
$$=\frac{1}{2\times\pi\times 11k\Omega\times 300kHz}$$
$$=48pF$$

Choose C_1=47pF.

7. Calculate R_3 by equation (13).

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}$$
$$=\frac{1}{2\times\pi\times 60kHz\times 2.2nF}$$
$$=1.2k\Omega$$

Choose R_3=1.2kΩ.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

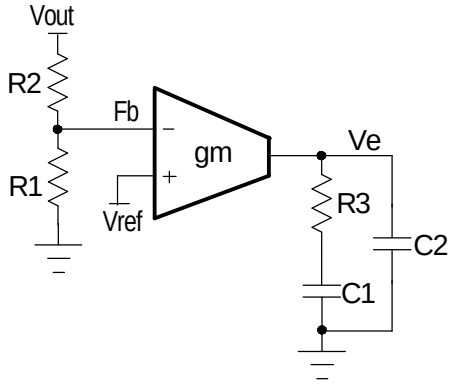

Figure 11 - Type II compensator with transconductance amplifier

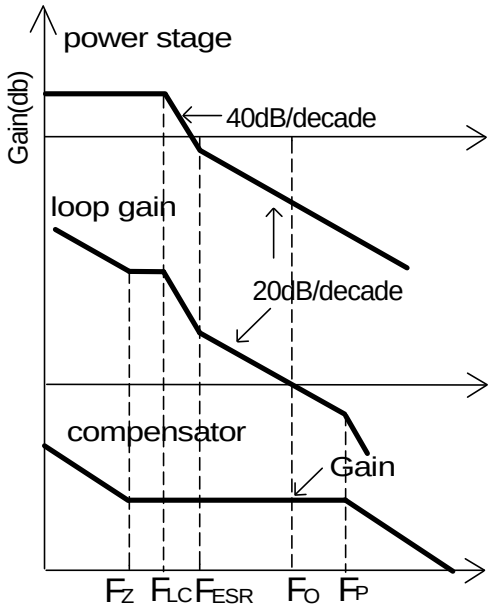

Figure 12 - Bode plot of Type II compensator

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 11. R3 and C1 introduce a zero to cancel the double pole effect. C2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain=g_m \times \frac{R_1}{R_1+R_2} \times R_3 \quad \text{... (15)}$$

$$F_z=\frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (17)}$$

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10\sim1/5F_s$.

The following uses typical design in figure 18 as an example for type II compensator design, two 680uF with 36mΩ electrolytic capacitors are used.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{4.7uH\times1360uF}}$$
$$=2.0kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times18m\Omega\times1360uF}$$
$$=6.5kHz$$

2.Set R_2 equal to10kΩ. Using equation 18.

$$R_1=\frac{10k\Omega\times0.8V}{2.5V\text{-}0.8V}=4.7k\Omega$$

3. Set crossover frequency at 1/10~ 1/5 of the swithing frequency, here F_O=30kHz.

4.Calculate R_3 value by the following equation.

$$R_3=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{R_{ESR}}\times\frac{1}{g_m}\times\frac{R_1+R_2}{R_1}$$
$$=\frac{2V}{12V}\times\frac{2\times\pi\times30kHz\times4.7uH}{18m\Omega}\times\frac{1}{2.5mA/V}$$
$$\times\frac{10k\Omega+4.7k\Omega}{4.7k\Omega}$$
$$=10.3k\Omega$$

Choose R_3 =10kΩ.

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5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1 = \frac{1}{2 \times \pi \times R_3 \times F_z}$$
$$= \frac{1}{2 \times \pi \times 10k\Omega \times 0.75 \times 6.5kHz}$$
$$= 10.7nF$$

Choose C_1=10nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{\pi \times R_3 \times F_s}$$
$$= \frac{1}{\pi \times 10k\Omega \times 300kHz}$$
$$= 106pF$$

Choose C_2=100pF.

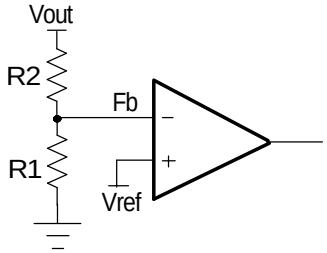
Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \qquad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Choose R_2=10kΩ, to set the output voltage at 1.6V, the result of R_1 is 10kΩ.



Voltage divider

Figure 13 - Voltage divider load

In general, the minimum output load impedance including the resistor divider should be less than 5kΩ to prevent overcharge the output voltage by leakage current (e.g. Error Amplifier feedback pin bias current). A minimum load for 5kΩ less (<1/16w for most of application) is recommended to put at the output. For example, in this application,

Vout=1.6V

The power loss is 1/16W less

$R_{LOAD} = 1.6V \times 1.6V / (1/16W) = 40\Omega$

Select minimum load is 1kΩ should be good enough.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise. The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \qquad ...(19)$$

V_{IN} = 12V, V_{OUT}=1.6V, I_{OUT}=10A, using equation (19), the result of input RMS current is 3.4A.

For higher efficiency, low ESR capacitors are recommended. One Sanyo OSCON SP series 16SP270M 16V 270uF with 4.4A is chosen as input bulk capacitor.

Power MOSFETs Selection

The NX2113 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example, two IRFR3706 are used. They have the following parameters: V_{DS}=30V, I_D =75A,R_{DSON} =9mΩ,Q_{GATE} =23nC.

There are three factors causing the MOSFET power loss: conduction loss, switching loss and gate driver loss.

Gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits. It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_S \quad ...(20)$$

where Q_{HGATE} is the high side MOSFETs gate charge, Q_{LGATE} is the low side MOSFETs gate charge, V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

According to equation (20), P_{GATE} =0.14W. This power dissipation should not exceed maximum power dissipation of the driver device.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2 \times D \times R_{DS(ON)} \times K$$
$$P_{LCON} = I_{OUT}^2 \times (1-D) \times R_{DS(ON)} \times K \quad ...(21)$$
$$P_{TOTAL} = P_{HCON} + P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K equals to 1.4 at 125°C according to IRFR3706 datasheet. Using equation (21), the result of P_{TOTAL} is 0.54W. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_S \quad ...(22)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. The result of P_{SW} is 3W. Swithing loss P_{SW} is frequency dependent.

Soft Start, Enable and shut Down

The NX2113 has a digital start up. It is based on digital counter with 1024 cycles. For NX2113 with 300kHz operation, the start up time is about 3.5ms. For NX2113A with 600kHz operation, the start up time is about half of NX2113, 1.75mS.

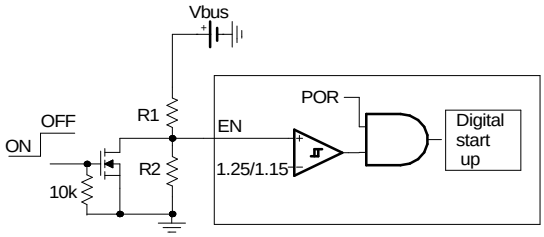


Figure 14 - Enable and Shut down NX2113 by pulling down EN pin.

The start up of NX2113/2113A can be programmed through resistor divider at Enable pin. For example, if the input bus voltage is 12V and we want NX2113 starts when Vbus is above 8V. We can select

R2=1.24k

$$R_1 = \frac{(8V - 1.25V) \times R_2}{1.25V} = 6.8k\Omega$$

The NX2113 can be turned off by pulling down the ENable pin by extra signal MOSFET or NPN transistor such as 2N3904 as shown in the above Figure. When Enable pin is below 1.15V, the digital soft start is reset to zero. In addition, all the high side is off and output voltage is turned off.

A resistor should be added as preload to prevent leakage current from FB pin charging the output capacitors.

Feedback Under Voltage Shut Down

NX2113 relies on the Feedback Under Voltage Lock Out (FB UVLO) to provide short circuit protection. Basically, NX2113 has a comparator compares the feedback voltage with the FB UVLO threshold 0.4V.

During the normal operation, if the output is short, the feedback voltage will be lower than 0.4V and comparator will change the state. After certain internal delay, both high side and low side driver will be turned off. The output will be latched. The normal operation should be achieved by removing the short and recycle the VCC.

During the start up, the output voltage is discharged to zero by the synchronous FET. FB voltage starts increase from zero when digital start block

operates. Before half of the start up time, the Feedback Under Voltage Lock Out comparator is disabled. After half of start up time, the Feedback UVLO comparator is enabled. The FB UVLO threshold is set to be half of voltage at the positive input of error amplifier. With this set up, if the output is short before soft start, the Feedback UVLO comparator can catch it and turn off the driver. The short circuit operation waveform during normal operation and during the soft start are shown as follows.

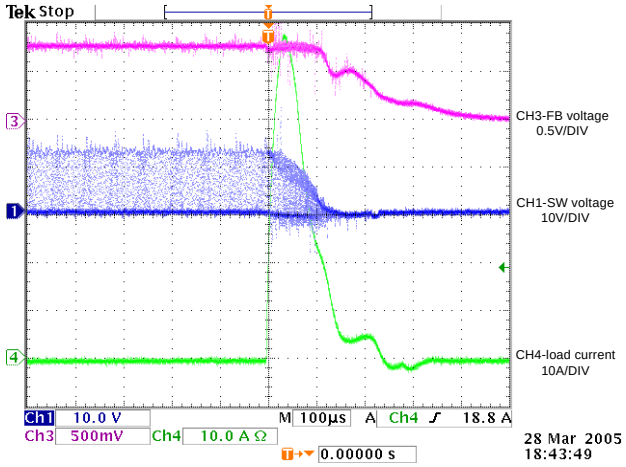


Figure 15 - Operation waveforms during short condition.

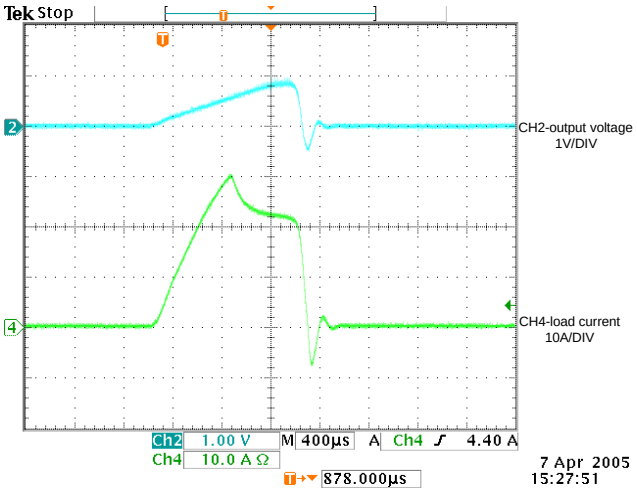


Figure 16 - Feedback UVLO with start up at short.

The Feedback UVLO can provide certain short circuit protection. However, since feedback does not have accurate information of current, this protection only provides certain level of over current protection. MOSFET should design such that it can survive with high pulse current for a short period of time.

The value of the capacitor on enable pin to ground and the resistor value of voltage divider on enable pin should be big enough to keep enable pin high during short. Otherwise, once output shorts, the input bus voltage drops, the chip is disabled before Feedback UVLO takes effect, and the system goes into hiccup status. This phenomena is easy to be found during system startup, if related resistor and capacitor value is not big enough.

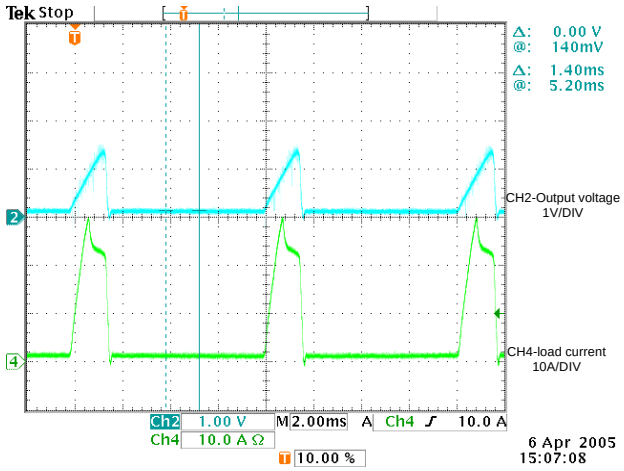


Figure 17 -Hiccup with start up at short.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to

reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced.

The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

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TYPICAL APPLICATION

Dual power supply (+5V BIAS,+12V BUS)

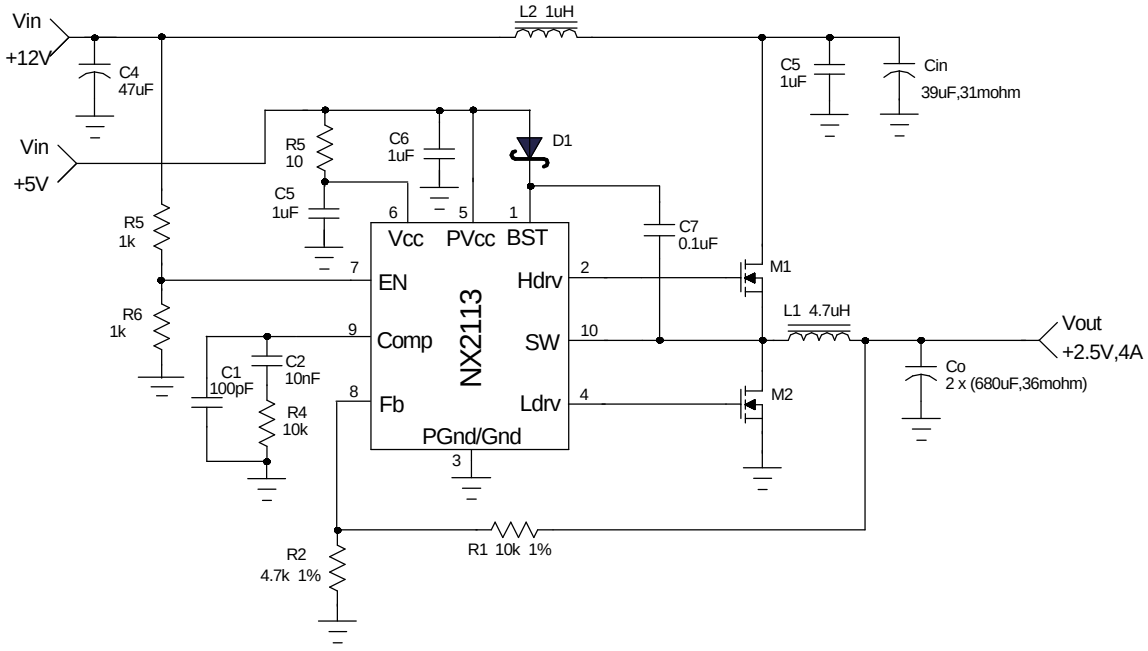

Figure 18 -Application of NX2113 for 5V bias and 12V input bus

Single power supply (+11V to +24V BUS)

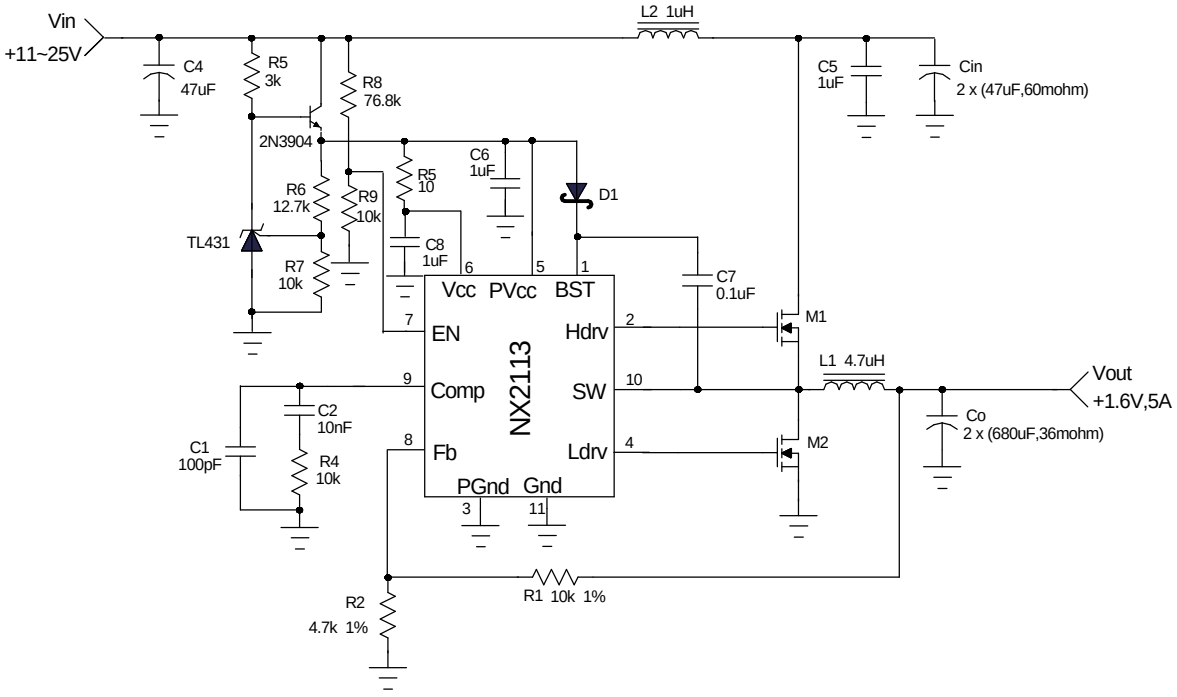

Figure 19 -Application of NX2113 for high input bus application

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TYPICAL APPLICATION

Single Supply 5V Input

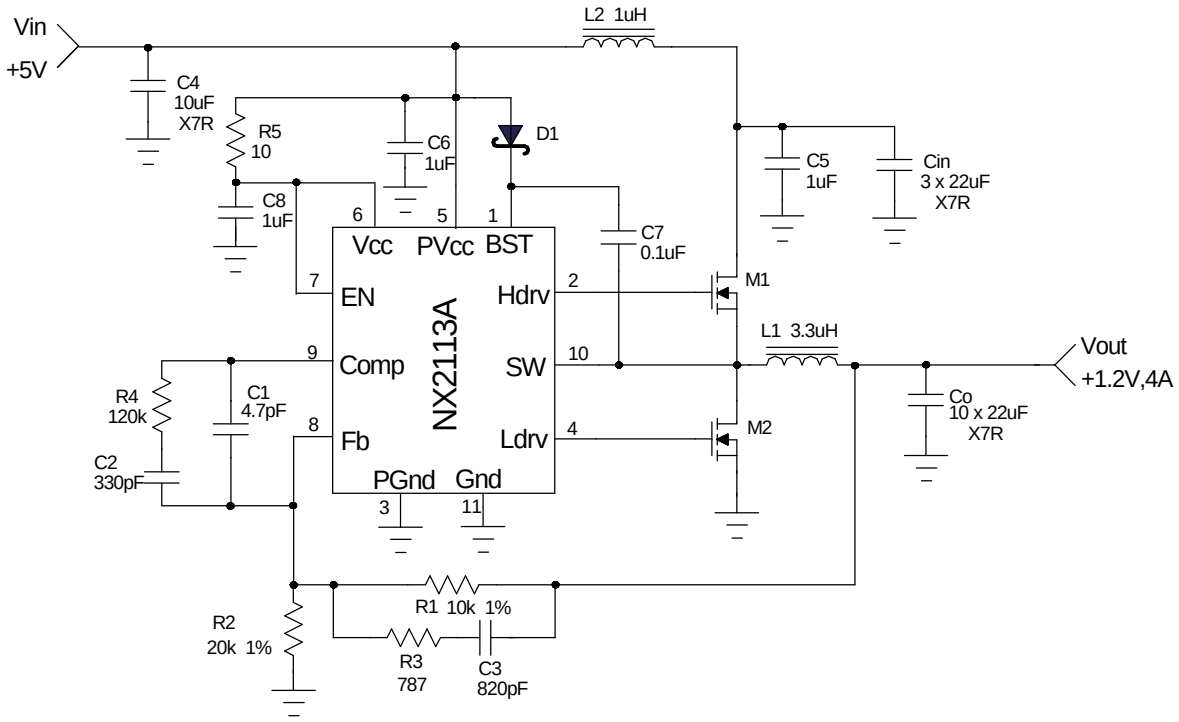

Figure 20 - Application of NX2113 A for 5V input and 1.6V output with ceramic output capacitors

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