NX26F011A
NX26F041A

NEXFLASH® Technologies, Inc.

1M-BIT AND 4M-BIT SERIAL FLASH MEMORY WITH 2-PIN NXS INTERFACE

PRE-RELEASE
MAY 1999

FEATURES

- **Tailored for Portable and Mobile Media-Storage**
  - Ideal for portable/mobile applications that transfer and store data, audio, or images
  - Removable Serial Flash Module package option
- ***NexFlash*™ Non-volatile Memory Technology**
  - Patented Single-Transistor EEPROM Cell
  - High-density, cost-effective, low-voltage/power
  - 10K/100K endurance, ten years data retention
- **Flash Memory for Battery-Operation**
  - Single 5V or 3V supply for Read, Erase/Write
  - Icc 5 mA active with 1 µA standby power
  - 5 ms Erase/Write times for efficient battery use
- **1M-bits or 4M-bits of *NexFlash* Serial Memory**
  - 512 or 2,048 sectors of 264 bytes each
  - Simple commands: Reset, Read, Write, Ready/Busy
  - No pre-erase required, auto-erases before write
- **Two-pin NXS Serial Interface**
  - Saves Microcontroller-pins, simplifies PCB layout, low switching noise compared to parallel Flash
  - Supports clock operation as fast as 16 MHz
  - Multi-device cascading, up to 16 devices
- **Development Tools and Accessories**
  - SFK-NXS Serial Flash Development Kit

Description

The *NexFlash*™ NX26F011A and NX26F041A Serial Flash Memories are tailored for portable/mobile media-storage applications that transfer and store data, audio and images. Manufactured using *NexFlash's* patented single transistor EEPROM memory cell, the NX26F011A and NX26F041A provide a high-density, low-voltage, low-power, and cost effective solution for battery-operated nonvolatile data storage requirements. The NX26F011A and NX26F041A can operate with a single 5V or 3V supply for Read, Write, and Erase. Power consumption is very low due to µA standby current and fast Erase/Write performance (as fast as 5 ms per sector) that minimizes power-on time, resulting in a highly efficient energy-per-transfer ratio. The NX26F011A and NX26F041A offer 1M-bits and 4M-bits of Flash memory organized in sectors of 264 bytes each. Each sector is individually addressable through basic commands or control functions such as Reset, Read, Erase/Write, and Ready/Busy. The NXS (*NexFlash* Serial) 2-wire serial interface is ideal for use with microcontrollers since it only requires two pins. This leaves pins normally used for parallel Flash free for other uses. The NXS interface supports clock rates as fast as 16 MHz and allows for multi-device cascading of up to 16 devices. It also simplifies PC-board layout and generates less transient noise than parallel devices. Development is supported with the NexFlash Serial Flash Development Kit.

Pin Descriptions

Package Types

The NX26F011A and NX26F041A is available in a 24/28-pin TSOP (Type II) package (Figure 1 and Table 1) or a removable Serial Flash Module (see NX25Mxxx/NX26Mxxx Serial Flash Module data sheet for further information).

Power Supply Pins (Vcc and GND)

The NX26F011A and NX26F041A support single power supply Read, Erase, and Write operations available in 5V and 3V Vcc versions. Active power requirements are as low as 15 mA for 3V versions with standby current in the 1 μA range.

NXS Serial Interface Pins (SCK and SIO)

The 2-wire NXS (NexFlash Serial) interface includes a Clock Input pin (SCK) and a single bidirectional I/O pin for data (SIO). All data to or from the SIO pin is clocked relative to the rising edge of SCK. The 2-wire NXS serial interface makes the NX26F011A and NX26F041A an ideal solution for removable non-volatile storage. A simple edge connector or cable/connector with four contacts (SCK, SIO, Vcc, and GND) can support communications with space efficiency and reliability. The NXS interface can operate at clock rates up to 16 MHz for 5V versions.

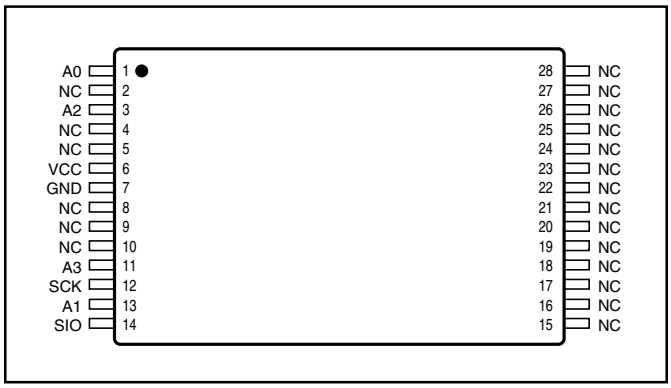


Figure 1. NX26F011A and NX26F041A Pin Assignments

Device Address Pins (A0, A1, A2, A3)

There is no active chip select on the NX26F011A and NX26F041A. Instead, four static device address pins (A0, A1, A2, and A3) are provided for decoding from one to 16 possible devices (Figure 2). This allows up to 4MB (using an NX26F011A device) or 32MB (using an NX26F041A device) to be addressed via a single 2-wire NXS interface. The static address pins (A0-A3) must be tied high or low to match the device address field (DA3-DA0) in the sector Read and Erase/Write instruction sequences.

No Connect Pins (N/C)

The NX26F011A and NX26F041A uses only a few signal pins. As a result, the TSOP package has numerous no connects (NC) that have no electrical contact to the die.

Table 1. Pin Descriptions

A0, A1, A2, A3	Device Address
SCK	Serial Clock
SIO	Serial Data I/O
Vcc	Power Supply
GND	Ground
NC	No Connect

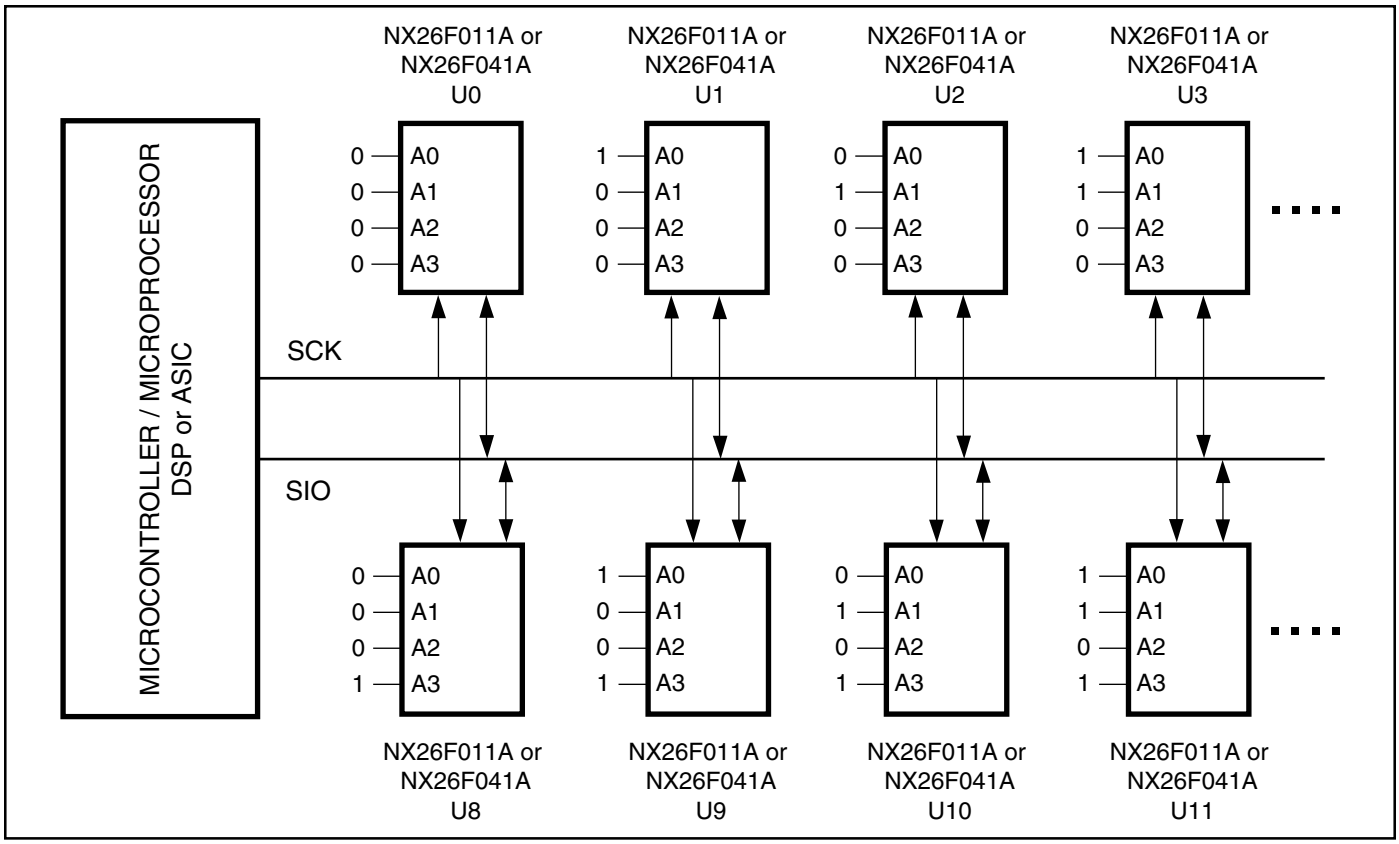


Figure 2. NX26F011A or NX26F041A Used in a Multi-device Configuration with up to 16-Devices on the 2-wire NSX

FUNCTIONAL OVERVIEW

The *NexFlash* NX26F011A and NX26F041A provide up to 1M-bits or 4M-bits of non-volatile memory organized as 512 or 2,048 small sectors of 264 bytes (4,288 bits) each (Figure 3). Each sector is individually addressable using basic instruction sequences and control functions communicated through the devices 2-wire NXS interface.

Read and Erase/Write Instruction Sequences

The NX26F011A and NX26F041A have two basic instruction sequences: Read and Erase/Write. Unlike some other Flash technologies, the erase and write operations of the NX26F011A and NX26F041A are performed together in one single operation (as fast as 5 ms per sector). Thus, pre-erase of the memory is not necessary.

Both Read and Erase/Write instructions are made up of a series of serial bit fields that include command, sector address, device address, and sector data. The Read instruction sequence also allows the device to be polled for Ready/Busy status.

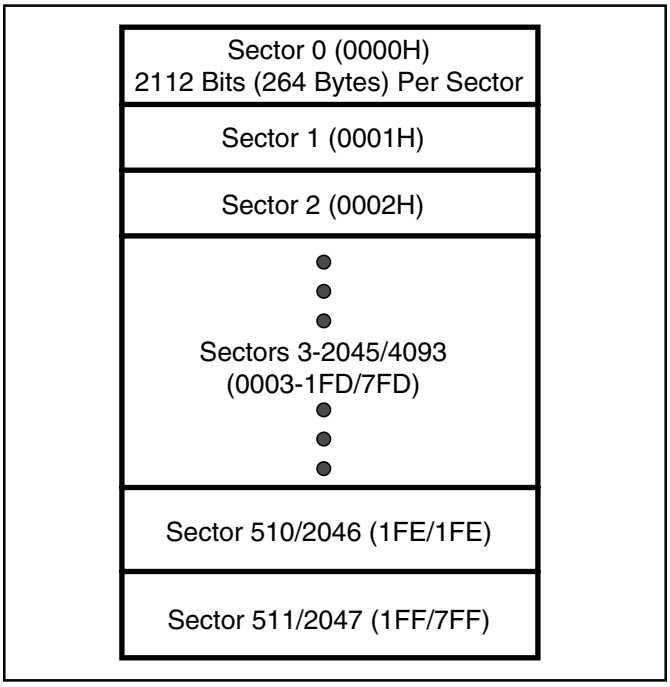


Figure 3. NX26F011A and NX26F041A Array

The instruction sequence format, flow charts, and clocking diagrams for Read and Erase/Write operations are shown in Figures 5 and 6, Figures 7 and 8, and Figures 9 and 10, respectively. All data within an instruction sequence is clocked on the rising edge. All instruction sequence fields are ordered by most significant bit first (MSB). Data is erased and written to the NX26F041A and NX26F011A memory array a full sector (264 bytes) at a time. If all 264 bytes of a given sector are not fully clocked into the device, the remaining byte locations will be overwritten with indeterminate values. To ensure the highest level of data integrity write operations should be verified and rewritten, if needed, (see High Data Integrity Applications).

Reset and Idle
Upon power-up and between Read and Erase/Write instruction sequences, the device's internal control logic will be reset. This is accomplished by asserting the SCK pin low (to V_{IL}) for greater than t_{RESET} (~5 ms to 10 ms depending on the voltage version being used). Once reset, the device enters standby operation and will not wake-up until the next rising edge of SCK. After an initial rising SCK occurs, the device becomes ready for a new instruction sequence. Full active power consumption starts after the correct device address is decoded during a Read or Write instruction sequence. To idle an instruction sequence between clocks, SCK must be kept high (at V_{IH}) for as long as needed. Note that power will be in the active state when SCK is held high.

Device Initialization
After power-up it is recommended that the device information sector be read to electronically identify the device. The device information format contains a device ID that identifies the manufacturer, part number (memory size), and operating range. It also contains a list of any restricted sectors (see Sector Tag/Sync bytes). For a further description of the NX26F011A and NX26F041A device information format, see the Serial Flash Device Information Sector Application Note SFAN-02.

As shown in Figure 6, the address for the device information sector address is at 5000H for both the NX26F011A and NX26F041A. The device information sector is a "read-only" sector. This assures that all device specific information, such as the restricted sector list, is maintained and never written over inadvertently.

Ready/Busy Status
After an Erase/Write instruction sequence has been executed, the device will become Busy while it erases and writes the addressed sector's memory. This period of time will not exceed t_{WP} (~5 to 30 ms based on the specified power supply operating voltage). During this time the device can be tested for a Ready/Busy condition via a 16-bit status value obtained in the Read instruction sequence. The Busy status condition (6666H) indicates that the device has not yet completed its write operation and will not accept read or write instructions. The Ready status condition (9999H) indicates that the device is available for further read or write operations. Note that a delay time of t_{RP} (~30 µs to 100 µs depending on the voltage version being used) is required after the first low to high clock transition of the Ready/Busy status read.

Sector Tag/Sync Bytes
The first byte of each sector is pre-programmed during manufacturing with a Tag/Sync value of "C9H". Although the first byte of each sector can be changed, it is recommended that Tag/Sync value be maintained and incorporated as part of the application's sector formatting. The Tag/Sync values serve two purposes. First, they provide a sync-detect that can help verify if the instruction sequence was clocked into the device properly. Secondly, they serve as a tag to identify a fully functional (valid) sector. This is especially important if "restricted sector" devices are used.

Restricted sector devices provide a more cost effective alternative to NX26F011A or NX26F041A devices with 100% valid sectors. Restricted sector devices have a limited number of sectors (32 maximum. for the NX26F011A and NX26F041A) that do not meet manufacturing programming criteria over the specified operating range. When such a sector is detected, the first byte is tagged with a pattern other than "C9H". In addition to individual sector tagging, all restricted sectors for a given device are listed in the "device information format" (see Device Initialization).

High Data Integrity Applications
Data storage applications that use Flash memory or other non-volatile media must take into consideration the possibility of noise or other adverse system conditions that may affect data integrity. For those applications that require higher levels of data integrity it is a recommended practice to use Error Correcting Code (ECC) techniques. The NexFlash Serial Flash Development Kit provides a software routine for a 32-bit ECC that can detect up to two bit errors and correct one. The ECC not only minimizes problems caused by system noise but can also extend Flash memory endurance. For those systems without the processing power to handle ECC algorithms, a simple "verification after write" is recommended. The NexFlash Serial Flash Development Kit software includes a simple Write/Verify routine that will compare data written to a given sector and rewrite the sector if the compare is not correct.

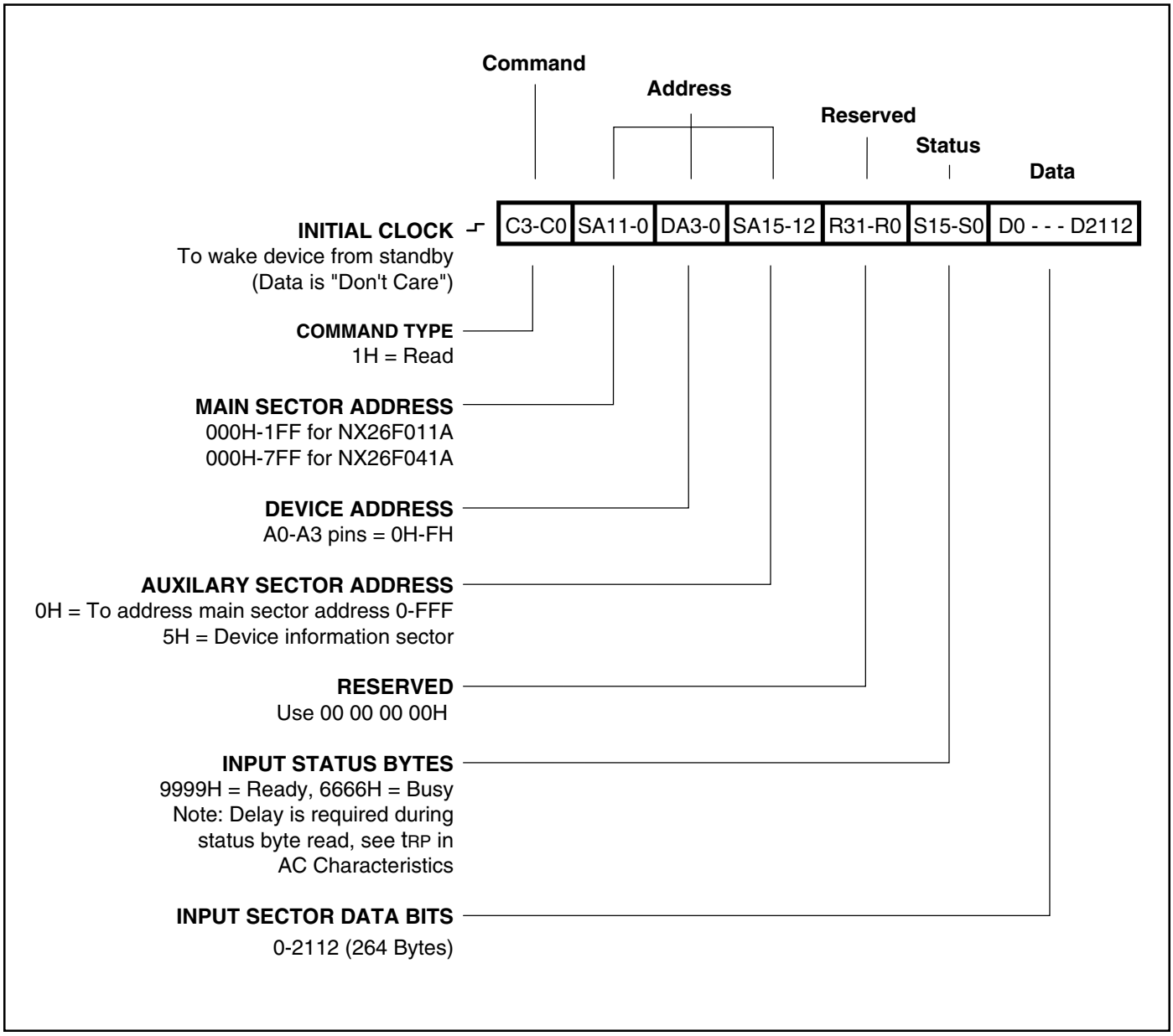


Figure 5. Sector Read Instruction - Sequence and Bit Instruction

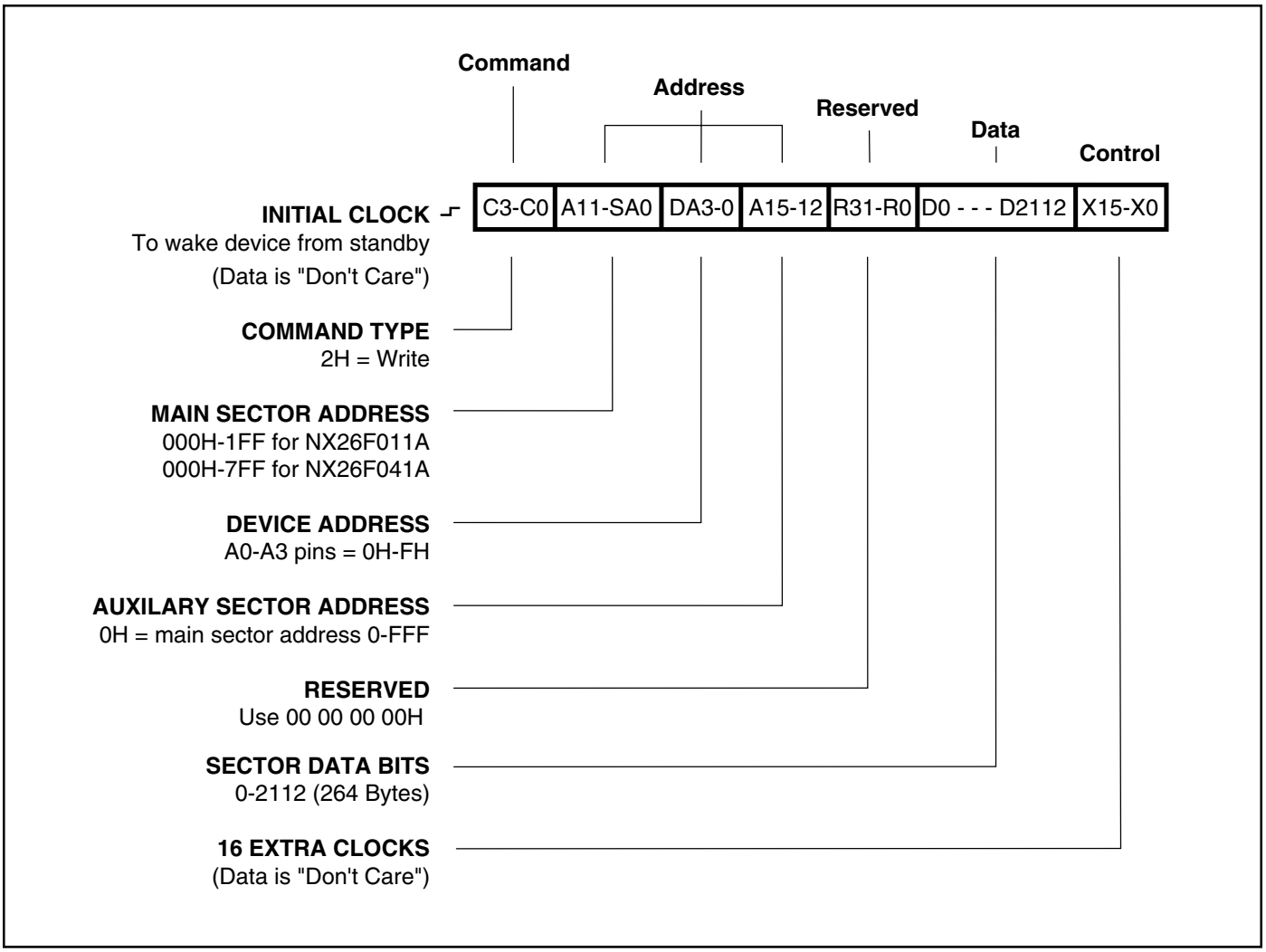


Figure 6. Sector Erase/Write Instruction - Sequence and Bit Format

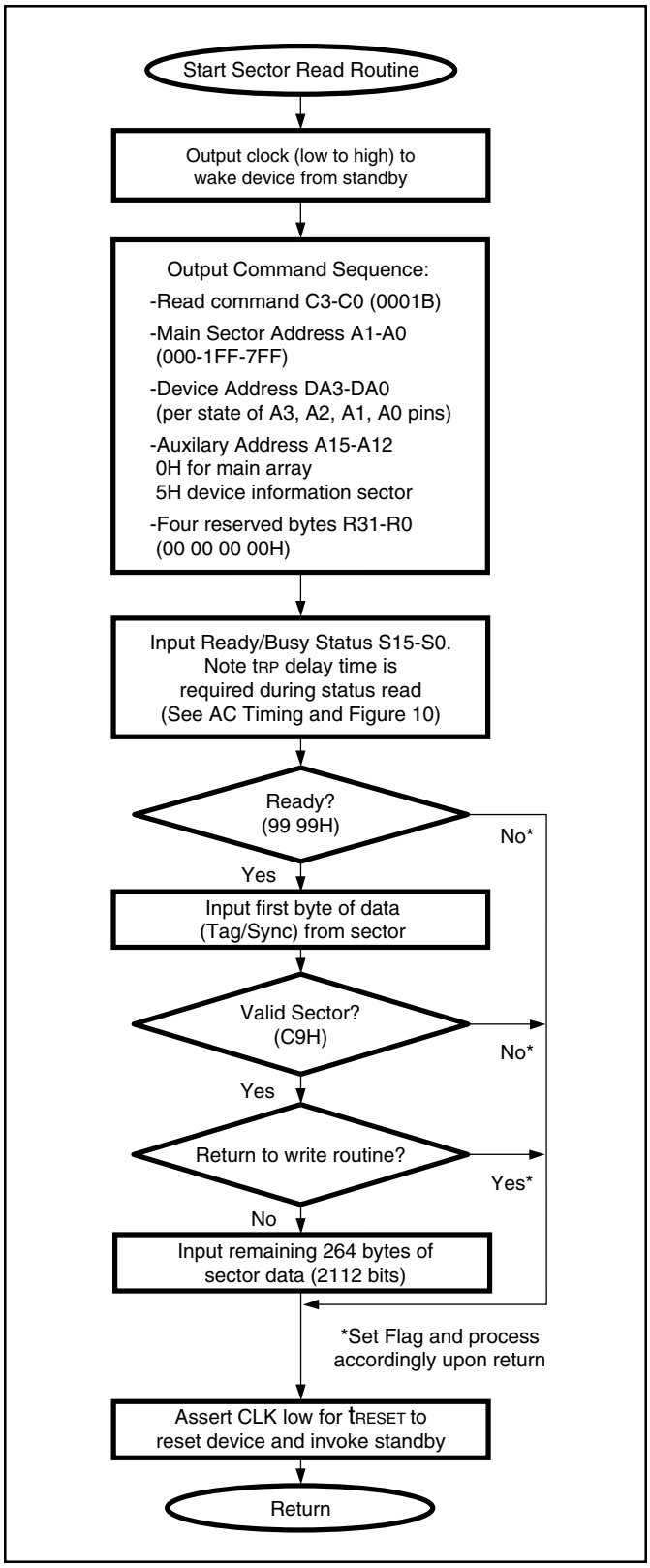


Figure 7. Sector Read Operation Flow Chart

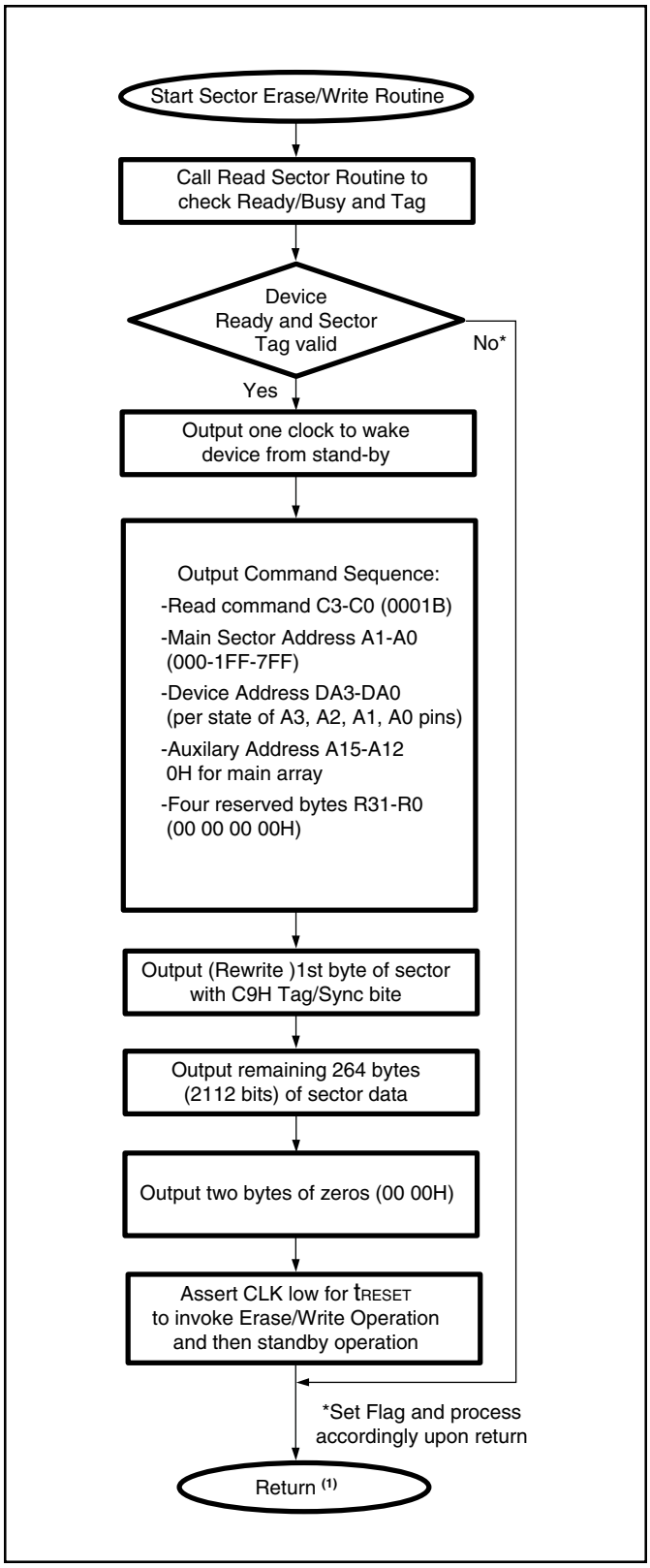


Figure 8. Sector Erase/Write Operation Flow Chart

Note:
1. To ensure higher data integrity verify each sector write with a sector read. See High Data Integrity Applications on Page 4.

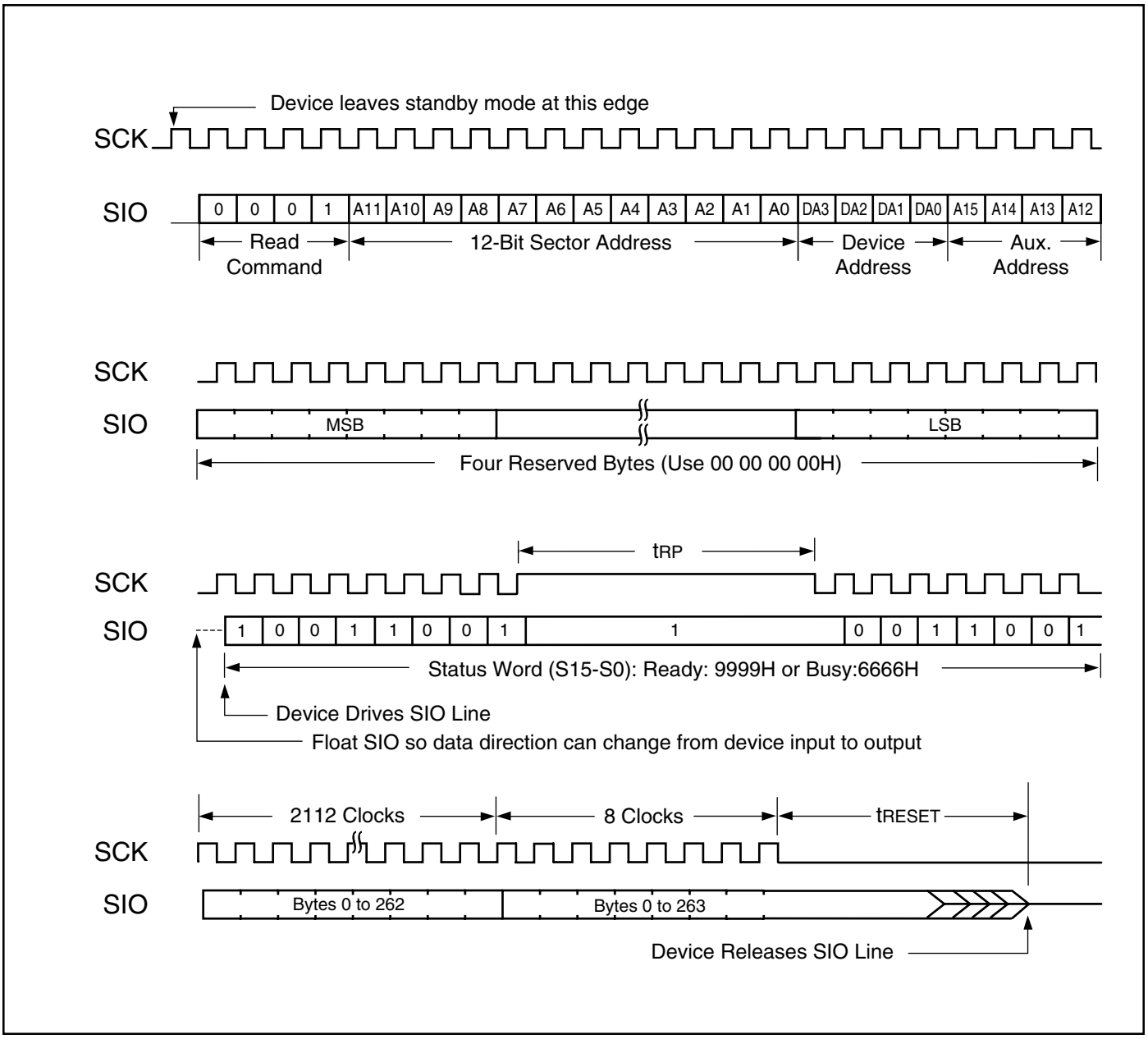


Figure 9. Read Instruction Sequence Clocking

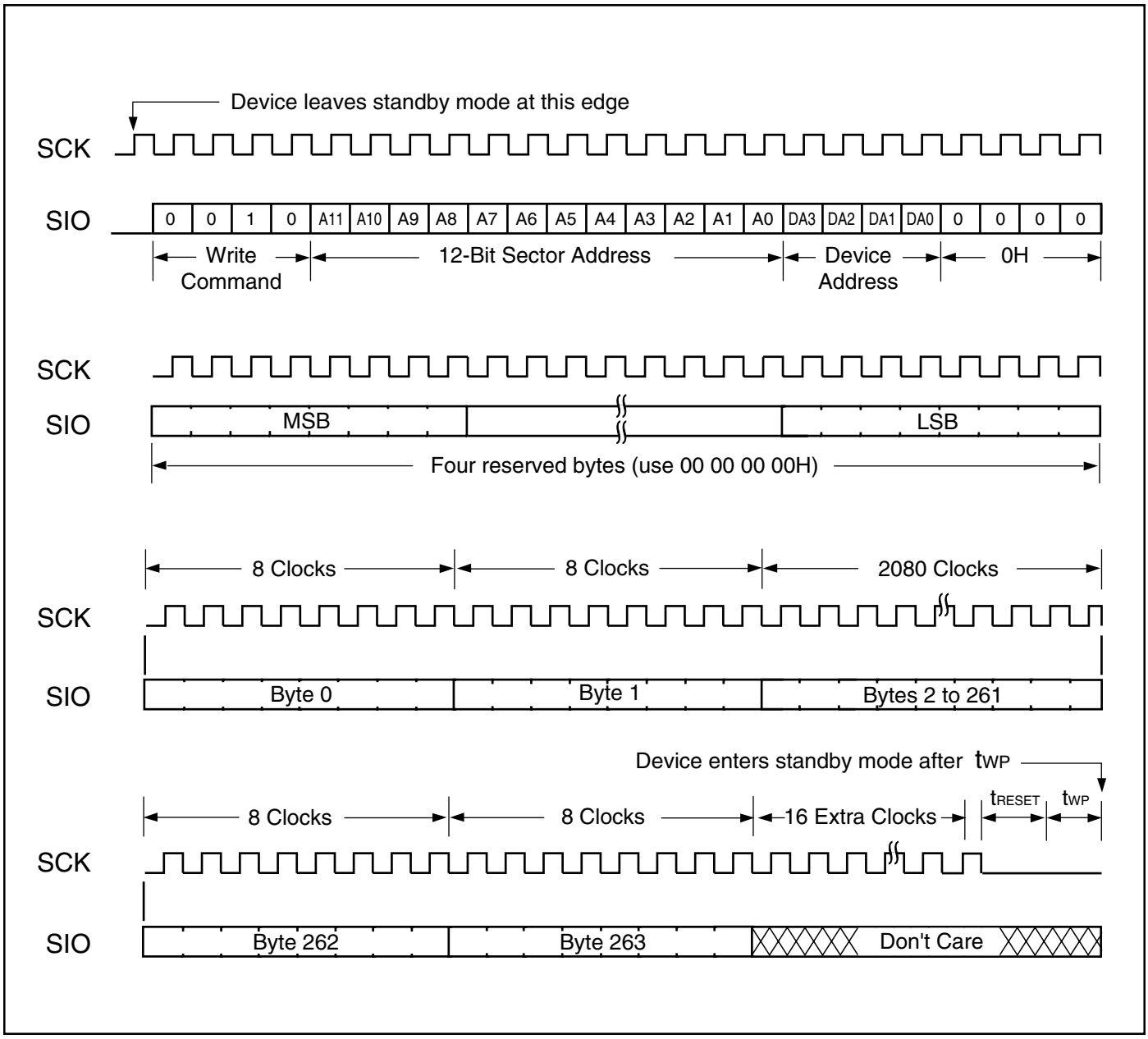


Figure 10. Erase/Write Instruction Sequence Clocking

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Conditions	Range	Unit
Vcc	Supply Voltage		0 to 7.0	V
VIN, VOUT	Voltage Applied to Any Pin	Relative to Ground	–0.5 to Vcc + 0.6	V
TSTG	Storage Temperature		–65 to +150	°C
TLEAD	Lead Temperature	Soldering, Ten Seconds	+300	°C

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage

OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage	5.0V 3.0V 3.0V	4.5 2.7	5.5 3.6	V V
TA	Ambient Temperature, Operating	Commercial Extended(1) Industrial(1)	0 –15 –40	+70 +80 +85	°C °C °C

Note:
1. Contact *NexFlash* for availability of extended or industrial grade devices.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Input Low Voltage		–0.4	—	Vcc x 0.2	V
VIH	Input High Voltage		Vcc x 0.6	—	Vcc + 0.5	V
VOL	Output Low Voltage	IOL = 2 mA, VCC = 4.5V	—	—	0.45	V
VOH	Output High Voltage	IOH = –400 µA, VCC = 4.5V	2.4	—	—	V
VOLC	Output Low Voltage CMOS(1)	VCC = Min, IOL = 10 µA	—	—	0.15	V
VOHC	Output High Voltage CMOS(1)	VCC = Min, IOH = –10 µA	VCC – 0.3	—	—	V
ILI	Input Leakage	0 < VIN < Vcc	–10	—	+10	µA
IOL	I/O Leakage	0 < VIN < Vcc, Output Disabled	–10	—	+10	µA
ICC (active)	Active Power Supply Current(2)	fCLK ≤ 8 MHz (1/tCP) VCC = 4.5V to 5.5V VCC = 2.7V to 3.3V	 — —	 15 5	 30 10	 mA
ICCSB (standby)	Standby Power Supply Current	SIO = 0V or VCC, SCK = 0V	—	<1	10	µA
CIN	Input Capacitance(1)	TA = 25°C, VCC = 5V or 3V Frequency = 1 MHz	—	—	10	pF
COUT	Output Capacitance(1)	TA = 25°C, VCC = 5V or 3V Frequency = 1 MHz	—	—	10	pF

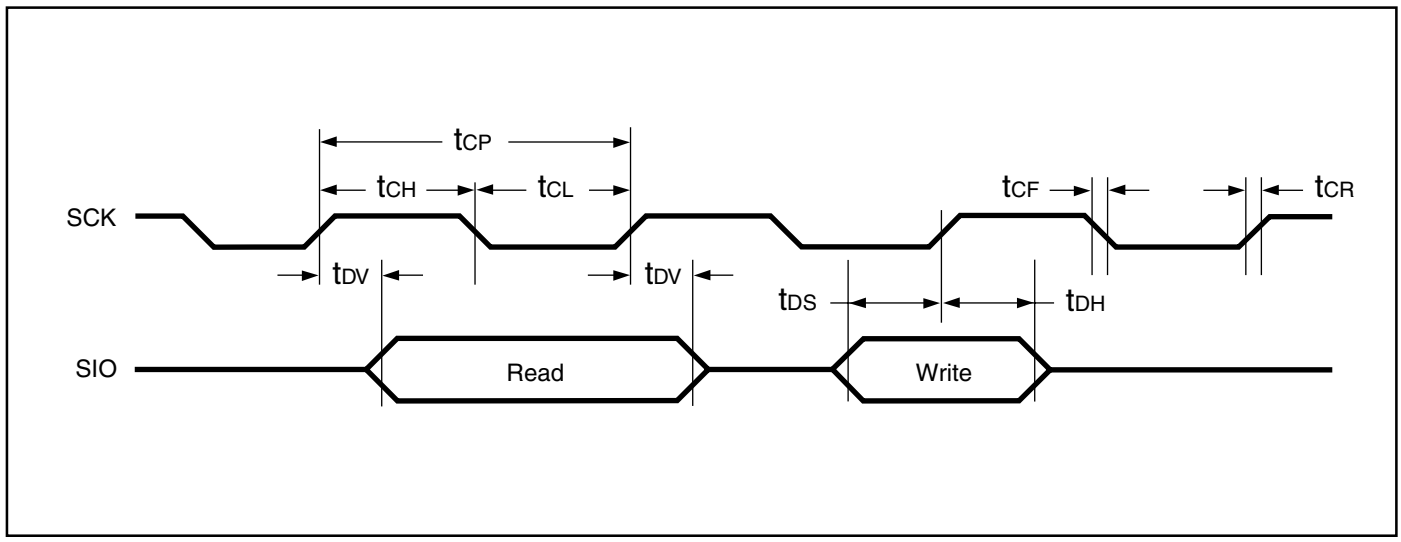
Notes:
1. Tested on a sample basis or specified via design or characterization data.
2. The device leaves “standby” power consumption after the clock transitions from low-to-high. Full “active” power consumption starts after the correct device address has been decoded during a sector read or write sequence.

AC ELECTRICAL CHARACTERISTICS

Symbol	Description	5V (16 MHz) Min	Typ	Max	3V (8 MHz) Min	Typ	Max	Unit
t_{CP}	SCK Serial Clock Period	62	—	—	125	—	—	ns
t_{CL}, t_{CH}	SCK Serial Clock High or Low Time	26	—	—	57	—	—	ns
t_{CR}	SCK Serial Clock Rise Time(1)	—	—	7	—	—	5	ns
t_{CF}	SCK Serial Clock Fall Time(1)	—	—	7	—	—	5	ns
t_{DS}	SIO Setup Time to SCK Rising Edge	40	—	—	100	—	—	ns
t_{DH}	SIO Hold Time From SCK Rising Edge	0	—	—	0	—	—	ns
t_{DV}	SIO Valid after SCK(2)	—	—	60	—	—	115	ns
t_{RESET}	SCK Low Duration for Valid Reset or Standby *(See Figures 9 & 10)*	1.5	—	5	3	—	10	µs
t_{RP}	Read Pre-data Delay *(See Figure 9)*	30	—	—	100	—	—	µs
t_{WP}	Erase/Write Program Time(3) *(See Figure 10)*	—	3	5	—	5	10	ms

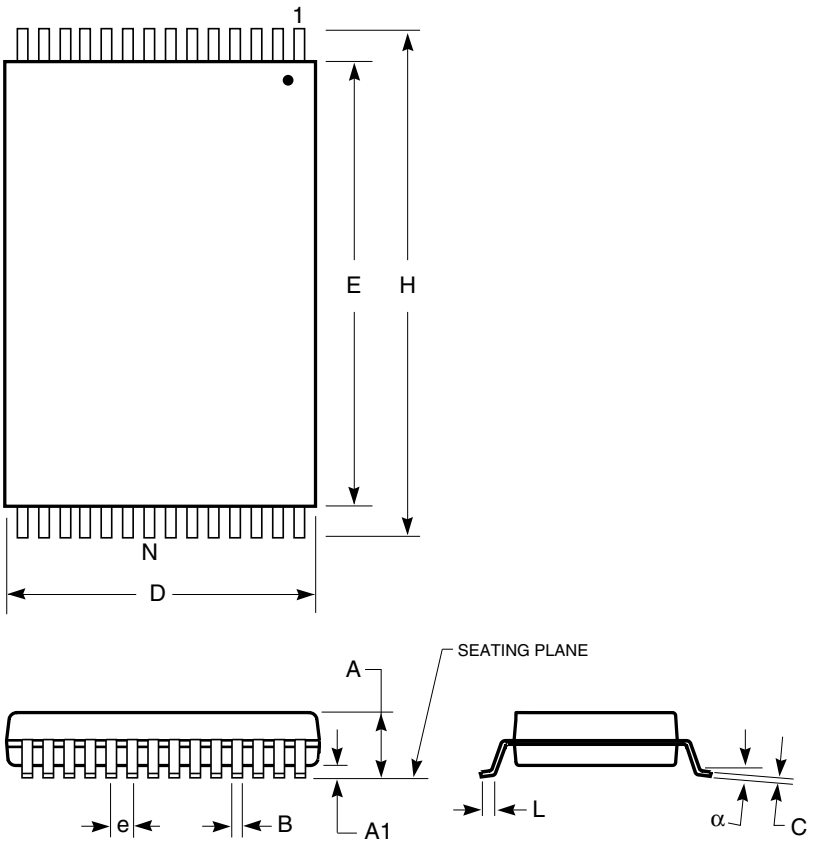
Notes:
1. Test points are 10% and 90% points for rise/fall times. All other timings are measured at the 50% point.
2. With 50 pF (8 MHz) or 30 pF (16 MHz) load SIO to GND.
3. The NX26F011A and NX26F041A are designed for Erase/Write endurances of 10K cycles. Endurance in the range of 100K cycles can be obtained using ECC software methods like those provided in the SFK Serial Flash Development Kit.

CLOCK AND DATA TIMING



PACKAGE INFORMATION

Plastic TSOP - 28-pin
Package Code: V (Type I)



Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		28		
A	1.00	1.20	0.039	0.047
A1	0.05	0.20	0.002	0.008
B	0.15	0.25	0.006	0.010
C	0.10	0.20	0.004	0.008
D	7.90	8.10	0.311	0.319
E	11.60	11.80	0.457	0.465
H	13.30	13.50	0.524	0.531
e	0.55 BSC		0.022 BSC	
L	0.50	0.70	0.020	0.028
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

ORDERING INFORMATION

Size	Order Part No.	Package/Description (2)
1M-bit	NX26F011A-3V-R (1)	NXS, 28-pin, TSOP (Type I) ≤32 RS, 3V Low Voltage
1M-bit	NX26F011A-5V-R (1)	NXS, 28-pin, TSOP (Type I) ≤32 RS, 5V Standard Voltage
4M-bit	NX26F041A-3V-R	NXS, 28-pin, TSOP (Type I) ≤32 RS, 3V Low Voltage
4M-bit	NX26F041A-5V-R (1)	NXS, 28-pin, TSOP (Type I) ≤32 RS, 5V Standard Voltage

Notes:
1. Add E (Extended) or I (Industrial) after package designator (V) for alternative temperature grades.
2. See 26Mxxx data sheet for Serial Flash Module package.

PRELIMINARY DESIGNATION

The "Preliminary" designation on an *NexFlash* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *NexFlash* or an authorized sales representative should be consulted for current information before using this product.

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NexFlash does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure in the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless *NexFlash* receives written assurances, to its satisfaction, that:

(a) the risk of injury or damage has been minimized;

(b) the user assumes all such risks; and

(c) potential liability of *NexFlash* is adequately protected under the circumstances.

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