NEXSEM

2A SOURCE/SINK LDO & SYNCHRONOUS SWITCHING CONTROLLER

PRELIMINARY DATA SHEET

DESCRIPTION

The NX2820 is a combination of synchronous Buck controller IC and 2A internal source/sink LDO regulator. It is designed for DDR memory application where typically synchronous controller provides either a 2.5V Vddq for DDR1 type memory(1.8V for DDRII) and the internal LDO supplies Vtt from the Vddq supply.

NX2820 features internal digital soft start,VCC undervoltage lock out, bus enable as well as over current limit by sensing low side MOSFET Rdson. The source and sink LDO is protected by thermal shutdown and current limit. The NX2820 is housed in 16 pin MLPQ Package which provides small yet good thermal capability ideal for computer or graphic card applications.

FEATURES

- Internal 2A Souce and Sink LDO
- Internal current Limit and thermal shutdown for LDO
- Shut down LDO by pulling down Refin pin
- Bus voltage operation from 4V to 25V
- Loss-Less Current Limit via Rdson of Low side FET
- Internal Digital Soft Start Function
- Programmable start up voltage for BUS Supply using Enable pin
- Shut Down PWM controller via EN pin

APPLICATIONS

- DDR I and II application
- Graphic Card on board converters
- Vddq and VTT Supply in mother board applications

TYPICAL APPLICATION

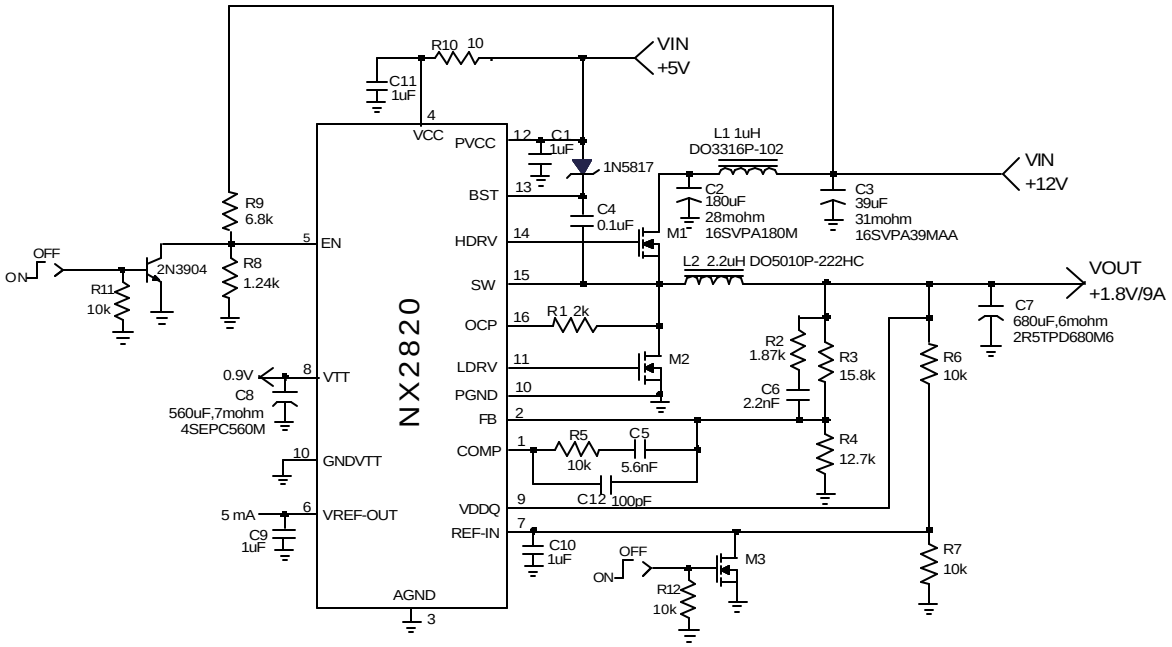


Figure1 - Typical application of 2820

ORDERING INFORMATION

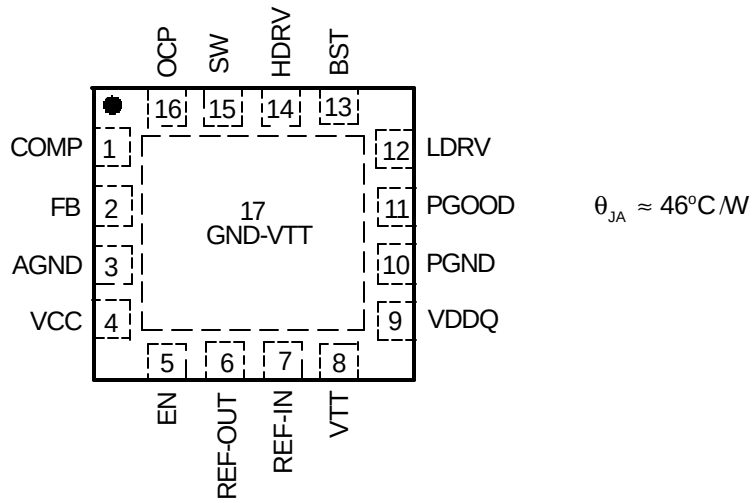
Device	Temperature	Package	Frequency
NX2820CMTR	0 to 70°C	MLPQ-16L	300kHz

ABSOLUTE MAXIMUM RATINGS(NOTE1)

Vcc to PGND & BST to SW voltage ..... -0.3V to 16V
BST to PGND Voltage ..... -0.3V to 35V
SW to PGND ..... -2V to 35V
All other pins ..... -0.3V to 6.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C
ESD Susceptibility 2kV

PACKAGE INFORMATION

16-LEAD PLASTIC MLPQ



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc =12V, V_{BST}-V_{SW}=12V, ENSW=3V, and T_A= 0 to 125°C. Typical values refer to T_A = 25°C.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
PWM Controller Section						
Reference Voltage						
Ref Voltage	V_{REF}			0.8		V
Ref Voltage line regulation				0.2		%
Supply Voltage(Vcc)						
V_{CC} recommended Voltage	V_{CC}		4.5		5.5	V
V_{CC} Supply Current (Static)	I_{CC} (Static)	Outputs not switching		5.5		mA
V_{CC} Supply Current (Dynamic)	I_{CC} (Dynamic)	Freq=300KHz, $C_{LOADHDRV}$=2500PF		14		mA
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		4		V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.2		V

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Oscillator (Rt)						
Frequency	F_S			300		KHz
Ramp-Amplitude Voltage	V_{RAMP}			1		V
Max Duty Cycle		F=300Khz		95		%
Min duty Cycle					0	%
Min ON time		NOTE2		70		nS
Error Amplifiers						
Open Loop Gain		NOTE2		65		dB
Input Bias Current	Ib			0.28		uA
EN & SS						
Soft Start time	Tss	Fs=300KHz		6.8		mS
Enable HI Threshold				1.2		V
Enable Hysterises				120		mV
High Side Driver, Hdrv, BST, SW (CL=3300pF)						
Output Impedance, Sourcing Current	R_{source}(Hdrv)	V_{BST}-V_{SW}=4.6V,I=200mA pulse		1.1		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	V_{BST}-V_{SW}=4.6V, I=200mA pulse		0.8		ohm
Rise Time	THdrv(Rise)	V_{BST}-V_{SW}=4.6V		20		ns
Fall Time	THdrv(Fall)	V_{BST}-V_{SW}=4.6V		20		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10% to 10%		50		ns
Low Side Driver , Ldrv,						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA pulse		1.1		ohm
Output Impedance , Sinking Current	R_{source}(Ldrv)	I=200mA pulse		0.5		ohm
Rise Time	TLdrv(Rise)	10% to 90%		20		ns
Fall Time	TLdrv(Fall)	90% to 10%		20		ns
Deadband Time	Tdead(H to L)	Hdrv going Low to Ldrv going High, 10% to 10%		50		ns
OCP Adjust						
Ocset current				100		uA
Blank time before activating		8 Clock cycles of 300 Khz		40		uS
Sounce and Sink LDO Section						
Reference Buffer						
Vref_out current driving capability		1uF at Vref_out		3		mA
Output Voltage						
Output Offset Voltage	V_{OS}	IOUT=0A	-20	0	20	mV
Load Regulation		I_L:From 0A to2A I_L:From 0A to-2A	-20	0	20	mV

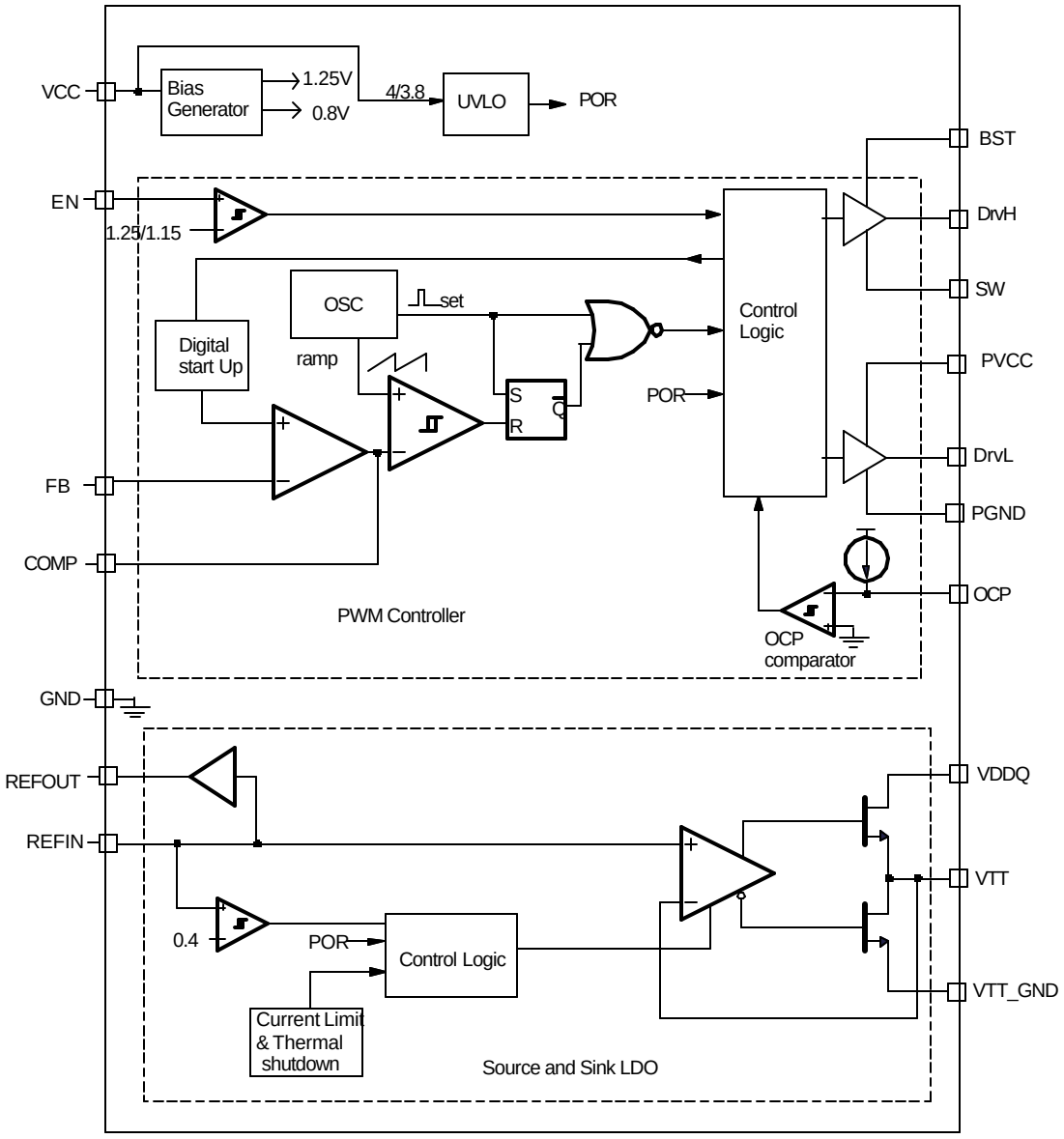
PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Input Voltage						
Input voltage Range (DDRI/II)	Vddq		1.7	2.5/1.8		V
Short Circuit Protection						
Current Limit	I_{LIMIT}		2.2	3.1		A
Over Temperature Protection						
Thermal Shutdown Temperature	T_{SD}	$3.3V<=V_{CNTL}<=5V$		150		°C
Thermal Shutdown Temperature hysteresis		$3.3V<=V_{CNTL}<=5V$		35		°C
Refin Shutdown Function						
Shutdown Threshold Trigger		Ouput=High	0.6			V
		Output=Low			0.2	

NOTE1: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
NOTE2: This parameter is guaranteed by design but not tested in production(GBNT).

PIN DESCRIPTIONS

Pin#	Pin Symbol	Pin Description
1	COMP	These pins are the outputs of error amplifiers and are used to compensate the respective voltage control feedback loops.
2	FB	This pin is the error amplifiers inverting input. These pins are connected via resistor dividers to the output of the switching regulators to set the output DC voltage.
3	AGND	Analog ground.
4	Vcc	IC's supply voltage. This pin biases the internal logic circuits. A high freq 1uF ceramic capacitor is placed as close as possible to and connected to this pin and ground pin. The maximum rating of this pin is 16V.
5	EN	A resistor divider is connected from the respective switcher BUS voltages to these pins that holds off the controllers soft start until this threshold is reached. An external low cost MOSFET can be connected to this pin for external enable control.
6	REF-OUT	Reference buffer output. It can driver up to 5mA load.
7	REF-IN	Source and Sink LDO reference input. A small ceramic capacitor is recommended to put this pin to ground. The LDO can be shut down by pulling this pin to be below 0.2V.
8	VTT	Output of source and sink LDO.
9	VDDQ	Input supply for the intenral source and sink LDO.
10	PGND	Power ground pin for low side drivers.
11	LDRV	Low side gate driver outputs.
12	PVcc	Supply voltage for the low side fet drivers. A high frequency 1uF ceramic cap must be connected from this pin to the PGND pin as close as possible to the pins.
13	BST	This pin supplies voltage to high side FET driver. A high freq 0.1uF ceramic capacitor is placed as close as possible to and connected to these pins and respected SW pins.
14	HDRV	High side gate driver outputs.
15	SW	These pin are connected to source of high side FETs and provide return path for the high side drivers. They are also used to hold the low side drivers low until this pin is brought low by the action of high side turning off. LDRVs can only go high if SW is below 1V threshold.
16	OCP	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection(OCP) comparator. An internal current source of 100uA is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET.
17(PAD)	GNDVTT	VTT ground.

BLOCK DIAGRAM



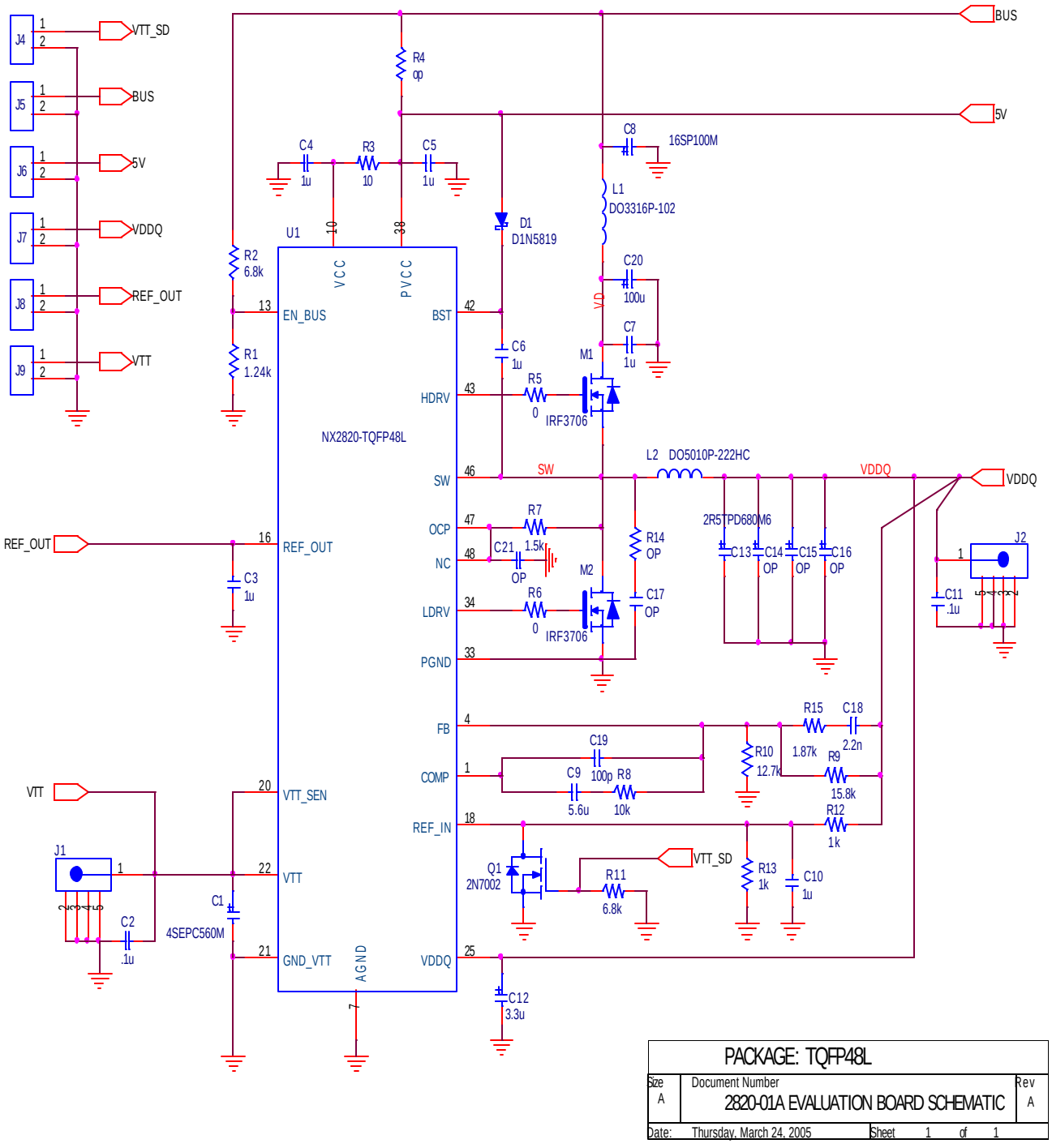


Figure 2 - Demo board schematic

Bill of Materials

Item	Quantity	Reference	Part	Manufacture
1	1	C1	4SEPC560M	SANYO
2	2	C2,C11	.1u	
3	6	C3,C4,C5,C6,C7,C10	1u	
4	1	C8	16SP100M	SANYO
5	1	C9	5.6u	
6	1	C12	3.3u	
7	1	C13	2R5TPD680M6	SANYO
8	6	R4,R14,C14,C15,C16,C17,C21	OPEN	
9	1	C18	2.2n	
10	1	C19	100p	
11	1	C20	100u	
12	1	D1	D1N5819	
13	2	J1,J2	SCOPE TP	Tektronics
14	6	J4,J5,J6,J7,J8,J9	CON2	
15	1	L1	DO3316P-102	Coilcraft
16	1	L2	DO5010P-222HC	Coilcraft
17	2	M1,M2	IRF3706	International Rectifier
18	1	Q1	2N7002	
19	1	R1	1.24k	
20	2	R2,R11	6.8k	
21	1	R3	10	
22	3	R5,R6	0	
23	1	R7	2k	
24	1	R8	10k	
25	1	R9	15.8k	
26	1	R10	12.7k	
27	2	R12,R13	1k	
28	1	R15	1.87k	
29	1	U1	NX2820-TQFP48L	NEXSEM INC

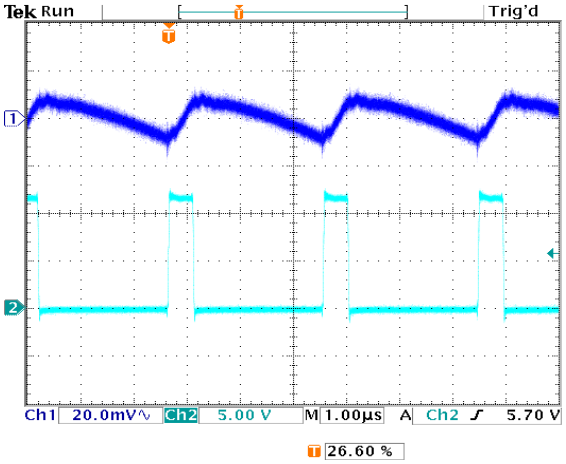


Figure 3 - Vddq output voltage ripple @ 1.8V

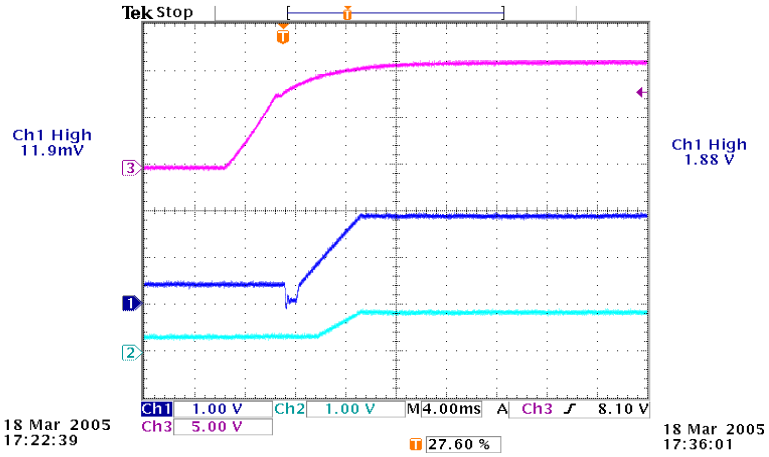


Figure 4 - Vin(CH3),VDddq(CH1),Vtt(CH2) @ softstart

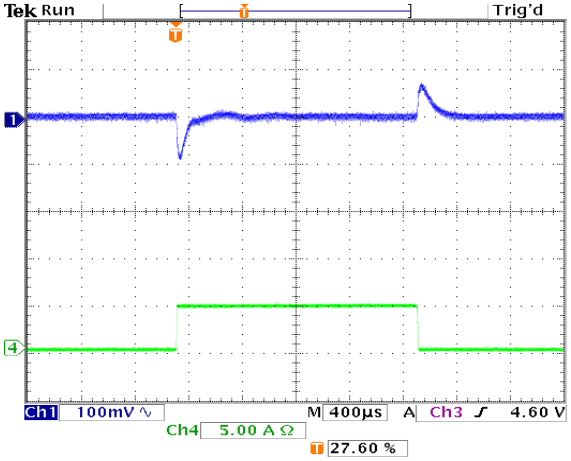


Figure 5 - Vddq change during transient

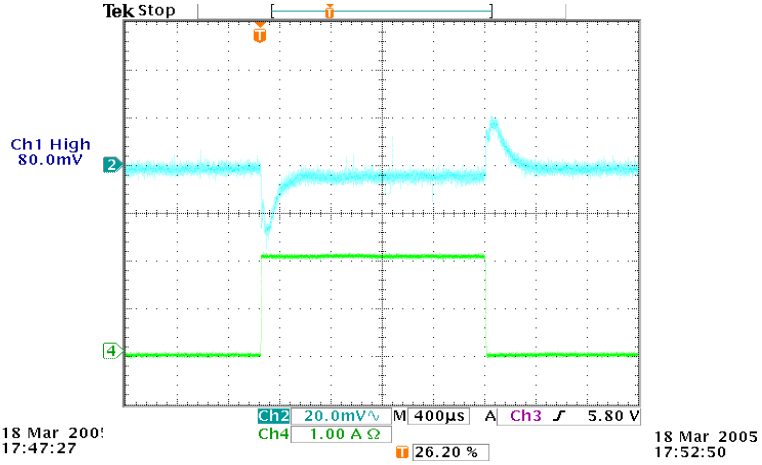


Figure 6 - Vtt change during transient

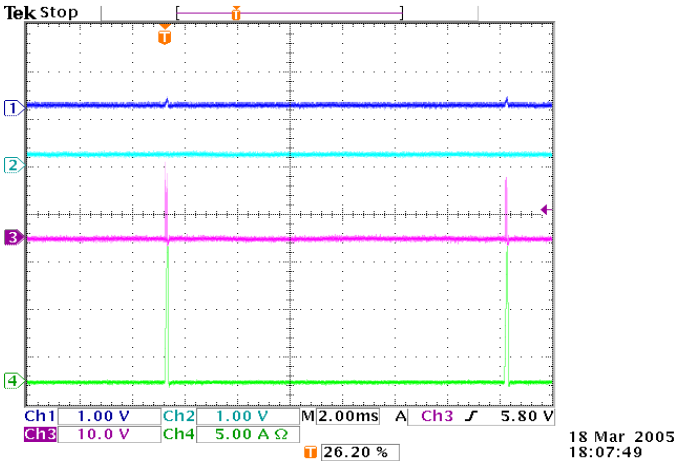


Figure 7 - Hiccup current limit with short circuit

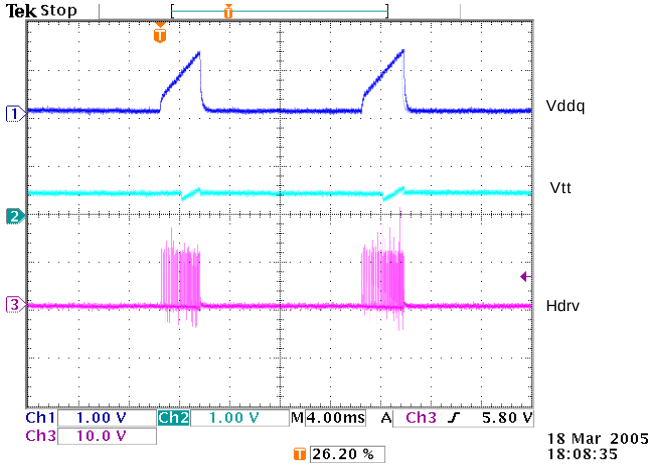


Figure 8 - Hiccup current limit with overload

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Switching frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

Power stage design requirements:
V_{IN}=12V
V_{OUT}=1.8V
I_{OUT} =9A
ΔV_{RIPPLE} <=20mV
ΔV_{TRAN}<=100mV @ 9A step
F_S=300kHz

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.3, then

$$L_{OUT}=\frac{12V-1.8V}{0.3\times 9A}\times\frac{1.8V}{12V}\times\frac{1}{300kHz}$$

L_{OUT}=1.9uH

Choose L_{OUT}=2.2uH, then coilcraft inductor DO5010P-222HC is a good choice.

Current Ripple is calculated as

$$I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$

$$=\frac{12V-1.8V}{2.2uH}\times\frac{1.8V}{12V}\times\frac{1}{300kHz}=2.3A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, POSCAP are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{20mV}{2.3A}=8.6m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 20mV output ripple, POSCAP 2R5TPD680M6 with 6mΩ are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N=\frac{6m\Omega\times 2.3A}{20mV}$$

N =0.7

The number of capacitor has to be round up to a integer. Choose N =1.

If ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors.

For example, one 100uF, X5R ceramic capacitor with 2mΩ ESR is used. The amount of output ripple is

$$\Delta V_{RIPPLE} = 2m\Omega \times 2.3A + \frac{2.3A}{8 \times 300kHz \times 100uF}$$
$$= 4.6mV + 9.6mV = 13.2mV$$

Although this meets DC ripple spec, however it needs to be studied for transient requirement.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$\Delta V_{droop} < \Delta V_{tran}$ @step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor,etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is mostly like to dependent on the ESR of capacitor.

Most case, the output capacitor is multiple capacitor in parallel. The number of capacitor can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 100mV for 15A load step.

If the POSCAP 2R5TPD680M6 (680uF, 6mohm ESR) is used, the crticial inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} =$$
$$\frac{6m\Omega \times 680\mu F \times 1.8V}{9A} = 0.82\mu H$$

The selected inductor is 2.2uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitor is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E$$
$$= \frac{2.2\mu H \times 9A}{1.8V} - 6m\Omega \times 680\mu F = 6.92us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2$$
$$= \frac{6m\Omega \times 9A}{100mV} +$$
$$\frac{1.8V}{2 \times 2.2\mu H \times 680\mu F \times 100mV} \times (6.92us)^2$$
$$= 0.83$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose N=1.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation is gives a good start. For more margin, more capacitors have to choose after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% up 100% (for ceramic) more capacitors have to chosen since the ESR of capacitors is so low that the PCB parasitics can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo OSCON and POSCAP, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by voltage mode amplifier.

$$F_{Z1} = \frac{1}{2\times p\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times p\times (R_2+R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times p\times R_3\times C_3} \quad ...(13)$$

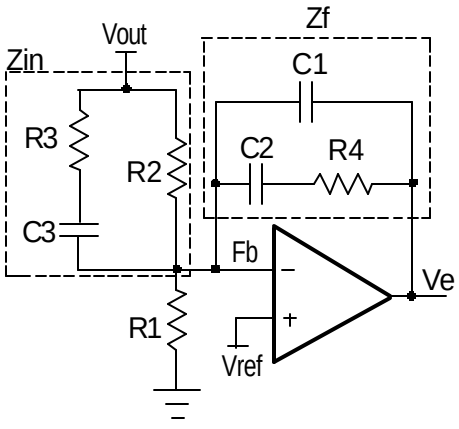
$$F_{P2} = \frac{1}{2\times p\times R_4\times \frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 15.

The transfer function of type III compensator is given by:

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

$$\frac{V_e}{V_{OUT}} = \frac{1}{sR_2\times(C_2+C_1)}\times\frac{(1+sR_4\times C_2)\times[1+s(R_2+R_3)\times C_3]}{(1+sR_4\times\frac{C_2\times C_1}{C_2+C_1})\times(1+sR_3\times C_3)}$$



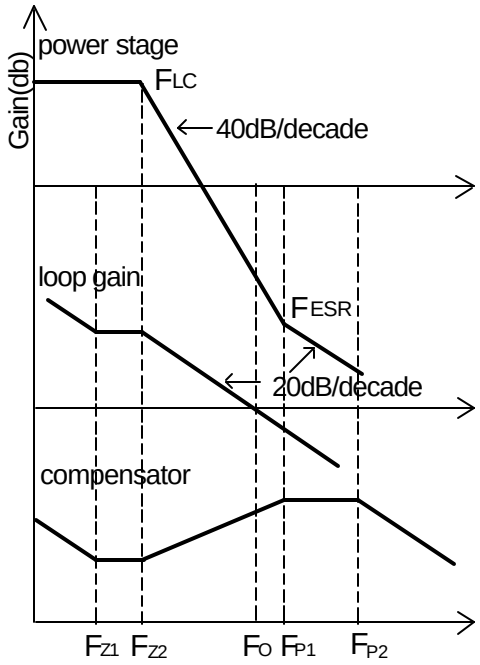


Figure 9 - Type III compensator and its bode plot

The crossover frequency has to be selected as $F_{LC}<F_O<F_{ESR,}$ and $F_O<=1/10\sim1/5F_s$ for type III compensator .

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR} .

$$F_{LC}=\frac{1}{2\times p\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times p\times\sqrt{2.2uH\times 680uF}}$$
$$=4.1kHz$$

$$F_{ESR}=\frac{1}{2\times p\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times p\times 6m\Omega\times 680uF}$$
$$=39kHz$$

2. Set F_O =25kHz < F_{ESR}

3. Set F_{z1} =0.75*$F_{LC,}$ F_{Z2} = $F_{LC,}$ F_{p1} =F_{ESR} and F_{p2} =0.5*F_S .

4. Set R_4 equal to 10kΩ.

5. Calculate C_1 and C_2.

$$C_2=\frac{1}{2\times p\times F_{Z1}\times R_4}$$
$$=\frac{1}{2\times p\times 0.75\times 4.1kHz\times 10k\Omega}$$
$$=5.2nF$$

Choose C_2=5.6nF.

$$C_1=\frac{1}{2\times p\times R_4\times F_{P2}}$$
$$=\frac{1}{2\times p\times 10k\Omega\times 150kHz}$$
$$=106pF$$

Choose C_1=100pF.

6. Calculate C_3 with the crossover frequency F_O=25kHz.

$$C_3=\frac{2\times p\times V_{osc}\times F_O\times L\times C}{V_{IN}\times R_4}$$
$$=\frac{2\times p\times 1V\times 25kHz\times 2.2uH\times 680uF}{12V\times 10k\Omega}$$
$$=1.9nF$$

Choose C_3=2.2nF.

7. Calculate R_2, R_3 .

$$R_3=\frac{1}{2\times p\times F_{P1}\times C_3}$$
$$=\frac{1}{2\times p\times 39kHz\times 2.2nF}$$
$$=1.85k\Omega$$

Choose R_3=1.87kΩ.

$$R_2=\frac{1}{2\times p\times F_{Z2}\times C_3}-R_3$$
$$=\frac{1}{2\times p\times 4.1kHz\times 2.2nF}-1.87k\Omega$$
$$=15.7k\Omega$$

Choose R_3=15.8kΩ.

8. Calculate R_1 .

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{15.8k\Omega\times 0.8V}{1.8V-0.8V}=12.6k\Omega$$

Choose R_3=12.7kΩ.

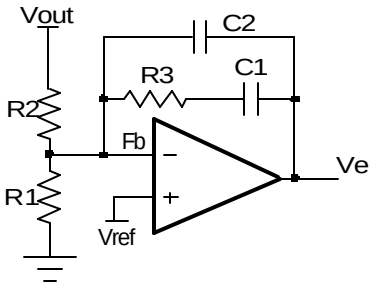
B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

$$Gain=\frac{R_3}{R_2} \quad \text{... (15)}$$

$$F_z=\frac{1}{2\times p\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p=\frac{1}{2\times p\times R_3\times C_2} \quad \text{... (17)}$$



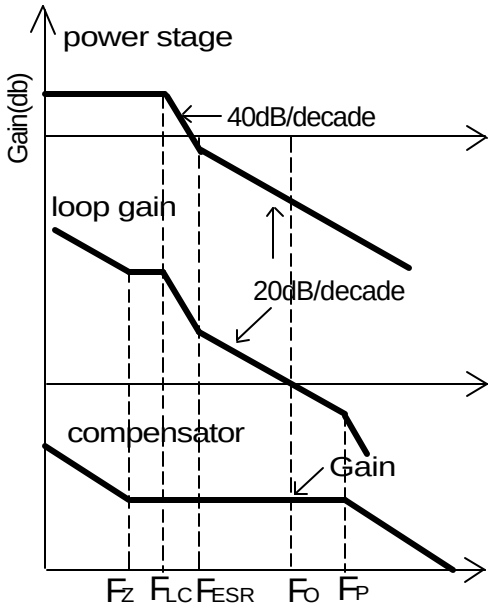


Figure 10 - Type II compensator and its bode plot

Type II compensator can be realized by simple RC circuit as shown in figure 16.R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

For type II compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10~1/5F_s$.

The following parameters are used as an example for type II compensator design, three 1500uF with 19mohm Sanyo electrolytic CAP 6MV1500WGL are used as output capacitors. Coilcraft DO5010P-152HC 1.5uH is used as output inductor. The other power stage information is that:

V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=15A, F_S=300kHz.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times p\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times p\times\sqrt{1.5uH\times 4500uF}}=1.94kHz$$

$$F_{ESR}=\frac{1}{2\times p\times ESR\times C_{OUT}}=\frac{1}{2\times p\times 6.33m\Omega\times 4500uF}=5.6kHz$$

2.Set crossover frequency F_O=20kHz>>F_{ESR}.

3. Set R_2 equal to10kΩ. Based on output voltage, using equation 18, the final selection of R_1 is 20kΩ.

4.Calculate R_3 value by the following equation.

$$R_3=\frac{V_{OSC}}{V_{in}}\times\frac{2\times p\times F_O\times L}{R_{ESR}}\times R_2=\frac{1V}{12V}\times\frac{2\times p\times 20kHz\times 1.5uH}{6.33m\Omega}\times 10k\Omega=24.8k\Omega$$

Choose R_3 =24.8kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1=\frac{1}{2\times p\times R_3\times F_z}=\frac{1}{2\times p\times 24.8k\Omega\times 0.75\times 1.94kHz}=4.4nF$$

Choose C_1=4.7nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{p \times R_3 \times F_s}$$
$$= \frac{1}{p \times 24.8k\Omega \times 300kHz}$$
$$= 64pF$$

Choose C_2=68pF

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Choose R_2=10kO, to set the output voltage at 1.8V, the result of R_1 is 8kΩ.

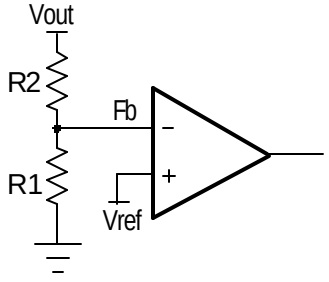


Figure 11 Voltage divider

In general, the minimum output load impedance including the resistor divider should be less than 5kΩ to prevent overcharge the output voltage by leakage current (e.g. Error Amplifier feedback pin bias current). A minimum load for 5kΩ less (<1/16w for most of application) is recommended to put at the output. For example, in this application,

Vout=1.6V

The power loss is 1/16W less

$R_{LOAD} = 1.6V \times 1.6V/(1/16W) = 40\Omega$

Select minimum load is 1kΩ should be good enough.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \quad ...(19)$$

V_{IN} = 12V, V_{OUT}=1.8V, I_{OUT}=9A, using equation (19), the result of input RMS current is 3.2A.

For higher efficiency, low ESR capacitors are recommended.

One Sanyo OS-CON 16SVPA180M 16V 180uF 28mΩ with 3.43A RMS rating are chosen as input bulk capacitors.

Power MOSFETs Selection

The NX2601 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example, two IRFR3706 are used. They have the following parameters: V_{DS}=30V, I_D =75A,R_{DSON} =9mΩ,Q_{GATE} =23nC.

There are three factors causing the MOSFET power loss:conduction loss, switching loss and gate driver loss.

Gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits.

It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_S \quad ...(20)$$

where Q_{HGATE} is the high side MOSFETs gate charge, Q_{LGATE} is the low side MOSFETs gate charge, V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

According to equation (3), P_{GATE} =0.07W. This power dissipation should not exceed maximum power dissipation of the driver device.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2 \times D \times R_{DS(ON)} \times K$$
$$P_{LCON} = I_{OUT}^2 \times (1 - D) \times R_{DS(ON)} \times K \quad ...(21)$$
$$P_{TOTAL} = P_{HCON} + P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K equals to 1.4 at 125°C according to IRFR3706 datasheet. Using equation (4), the result of P_{TOTAL} is 0.54W. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_S \quad ...(22)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. The result of P_{SW} is 1.5W. Swithing loss P_{SW} is frequency dependent.

Soft Start and Enable

NX2820 has digital soft start for switching controller and has one enable pin for this start up. When the Power Ready (POR) signal is high and the voltage at enable pin is above 1.25V, the internal digital counter starts to operate and the voltage at positive input of Error amplifier starts to increase, the feedback network will force the output voltage follows the reference and starts the output slowly. After 2048 cycles, the soft start is complete and the output voltage is regulated to the desired voltage decided by the feedback resistor divider.

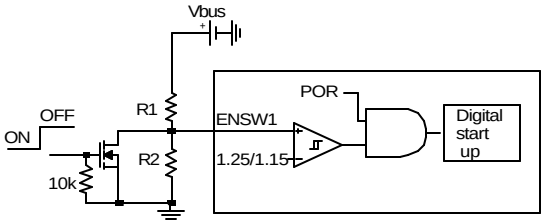


Figure 12 Enable and Shut down the NX2820 with Enable pin.

The start up of NX2820 can be programmed through resistor divider at Enable pin. For example, if the input bus voltage is 12V and we want NX2820 starts when Vbus is above 8V. We can select

R2=1.24k

$$R_1 = \frac{(8V - 1.25V) \times R_2}{1.25V} = 6.8k\Omega$$

The NX2820 can be turned off by pulling down the Enable pin by extra signal MOSFET as shown in the above Figure. When Enable pin (ENSW) is below 1.15V, the digital soft start is reset to zero. In addition, all the high side and low side driver is off and no negative spike will be generated during the turn off.

Over Current Limit Protection

Over current Limit for step down converter is achieved by sensing current through the low side MOSFET. For NX2820, the current through OCP pin is I_{OCP}=100uA. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over current occurs. The over current limit can be set by the following equation

$$I_{SET} = I_{RT} \times R_{OCP} / R_{DSON}$$

If the MOSFET R_{DSON}=9mΩ, and the current limit is set at 15A, then

$$R_{OCP} = \frac{I_{SET} \times R_{DSON}}{I_{RT}} = \frac{15A \times 9m\Omega}{100uA} = 1.35k\Omega$$

Choose ROCP=1.5kΩ

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced.

The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION