NX5P3090

USB PD and type C current-limited power switch

Rev. 1 — 1 August 2016 **Product data sheet**

1. General description

The NX5P3090 is a precision adjustable current-limited power switch for USB PD application. The device includes under voltage lockout, over-temperature protection, and reverse current protection circuits to automatically isolate the switch terminals when a fault condition occurs. The 29 V tolerance on VBUS pin ensures the device is able to work on a USB PD port; a current limit input (ILIM) pin defines the over-current limit threshold; an open-drain fault output ($\overline{\text{FAULT}}$) indicates when a fault condition has occurred.

The over-current limit threshold can be programmed from 400 mA to 3.3 A, using an external resistor between the ILIM pin and GND pin. In the over current condition, the device will clamp the output current to the value set by ILIM and keep the switch on while assert the FAULT flag. To minimize current surges during turn on, the device has built in soft start which controls the power switch rise time.

Surge protection has been integrated in the device to enhance system robustness. The enable input includes integrated logic level translation making the device compatible with lower voltage processors and controllers.

NX5P3090 is offered in a 12 bump 1.35 x 1.65 mm, 0.4 mm pitch WLCSP package.

2. Features and benefits

- VINT supply voltage range from 2.5 V to 5.5 V
- 29 V tolerance on VBUS and EN pin
- Adjustable current limit from 400 mA to 3.3 A
- Clamped current output in over-current condition
- Very low ON resistance: 34 mΩ (typical)
- Active HIGH EN pin with internal pull down resistor
- All time Reverse Current Protection
- Over Temperature Protection
- Surge protection: IEC61000-4-5 exceeds ±80 V on VBUS
- Safety approvals
  - UL 62368-1, 2nd Edition, File no. 20160526-E470128
  - IEC 62368-1 (ed.2), File no. DK-54536-UL
- ESD protection
  - IEC61000-4-2 contact discharge exceeds 8 kV on VBUS
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM AEC standard Q100-01 (JESD22-C101E) exceeds 500 V
- Specified from –40 °C to +85 °C ambient temperature

3. Applications

- Notebook and Ultrabook
- USB PD and Type C port/hubs
- Tablet and Smart phone

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NX5P3090UK	X5PT2	WLCSP12	wafer level chip-scale package; 12 bumps; 1.65 x 1.35 x 0.525 mm; 0.4 mm pitch (backside coating included)	SOT1390-5

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX5P3090UK	NX5P3090UKZ	WLCSP12	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	3000	T_{amb} = –40 °C to +85 °C

5. Marking

Table 3. Marking

Line	Marking	Description
A	X5PT2	basic type name
B	mmmmm	wafer lot code (mmmmm)
C	Z5YWW	manufacturing code Z = foundry location 5 = assembly location Y = assembly year code WW = assembly week code

6. Functional diagram

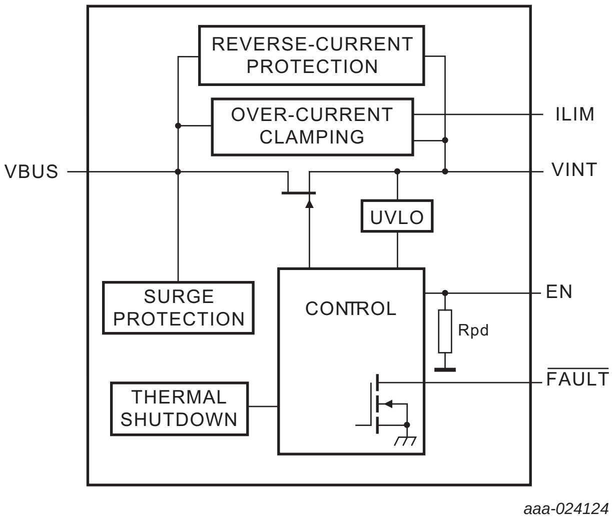


Fig 1. Logic diagram

7. Pinning information

7.1 Pinning

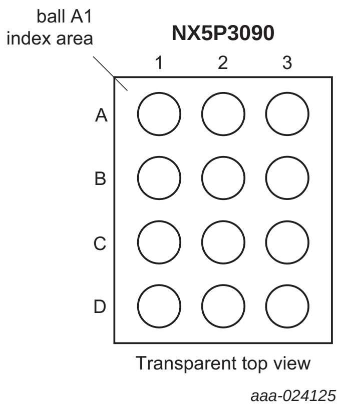


Fig 2. Pin configuration

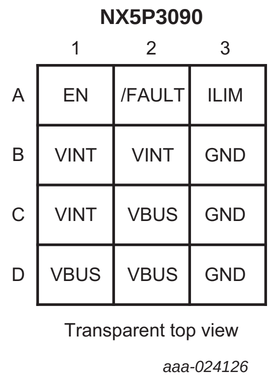


Fig 3. Pin map

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VBUS	C2, D1, D2	power output; 29 V tolerance
ILIM	A3	current limiter setting. connects a resistor to GND to set the threshold
$\overline{\text{FAULT}}$	A2	fault condition indicator (open-drain output)
EN	A1	enable input (active HIGH)
GND	B3, C3, D3	ground (0 V)
VINT	B1, C1, B2	power input

8. Functional description

Table 5. Function table[1]

EN	VINT	VBUS	FAULT	Switch
X	<2.5V	X	Z	under voltage lockout, switch open
L	2.5V to 5.5V	X	Z	disabled; switch open
H	2.5V to 5.5V	VBUS=VINT	Z	enabled; switch closed
H	2.5V to 5.5V	0V to VINT	L	over-current, clamped current output, switch closed
H	2.5V to 5.5V	VBUS>VINT+40mV (>4ms)	L	reverse current; switch open
H	2.5V to 5.5V	Z	L	Over-temperature; switch open

[1] H = HIGH voltage level; L = LOW voltage level.

8.1 EN Input

When the EN pin is set LOW, the N-channel MOSFET will be disabled, the device will enter low-power mode disabling all protection circuits and setting the FAULT pin high impedance. When EN is set HIGH, all protection circuits will be enabled and then, if no fault conditions exist, the N-channel MOSFET will be turn on. There is a 100 us de-glitch time on EN pin from LOW to HIGH.

8.2 Under-voltage lock-out

Independently of the logic level on the EN pin, the under-voltage lockout (UVLO) circuit disables the N-channel MOSFET and enters low power mode until the input voltage reaches the UVLO turn-on threshold level VUVLO.

8.3 ILIM

The over-current protection circuit's (OCP) trigger value I_{ocp} can be set using an external resistor R_{ILIM} connected between ILIM pin and GND pin. When EN is HIGH and the ILIM pin is pulled to ground, the N-channel MOSFET will be disabled and the FAULT output set LOW. The detailed IOCP setting is given in Section 8.4.

8.4 Over-current protection (OCP)

The device offers over current protection when enabled, three possible over-current conditions can occur. These conditions are:

- Over-current at start-up, $I_{SW} > I_{ocp}$ when enabling the N-channel MOSFET.
- Over-current after enabled, $I_{SW} > I_{ocp}$ when the N-channel MOSFET is already ON.
- Short circuit after enabled, I_{SW} > 10 A (typical).

In the over current condition, because the device clamps the output current rather than completely shut down the switch, the power dissipation on the device might be increased which could lead to over temperature protection (see Section 8.7).

8.4.1 Over-current at start-up

If the device senses a VBUS short to GND or over-current while enabling the N-channel MOSFET, OCP is triggered. It limits the output current to I_{ocp} and after the de-glitch time sets the FAULT output LOW.

8.4.2 Over-current when enabled

If the device senses $I_{SW} > I_{ocp}$ after enabled, OCP is triggered. It limits the output current to I_{ocp} and after the de-glitch time sets the $\overline{FAULT}$ output LOW. Limiting the output current reduces $V_{O(VOUT)}$.

8.4.3 Short circuit when enabled

If the device senses $I_{SW} > 10$ A after enabled, a short circuit is detected. The device disables the N-channel MOSFET immediately. It then re-enables the N-channel MOSFET and limit the output current to I_{ocp}, and after the de-glitch time the $\overline{FAULT}$ output is set LOW.

8.5 Reverse-Current protection (RCP)

When the VBUS pin voltage exceeds the input voltage by 40 mV (typical) the device will protect itself from damage by switching off the MOSFET after 4 ms de-glitch time.

When the VBUS pin voltage exceeds the VINT voltage by 100 mV, the device will shutdown the FET immediately without any de-glitch time.

FAULT pin will be set LOW in the reverse-current protection condition.

In the RCP state, when the VBUS voltage drops below VINT voltage, the device will exit the RCP state in 128 us and resume normal operation.

Before normal turn on, the device will always check the RCP condition first, if higher voltage is detected on VBUS pin, it will never turn on the power MOSFET even EN pin is pulled HIGH.

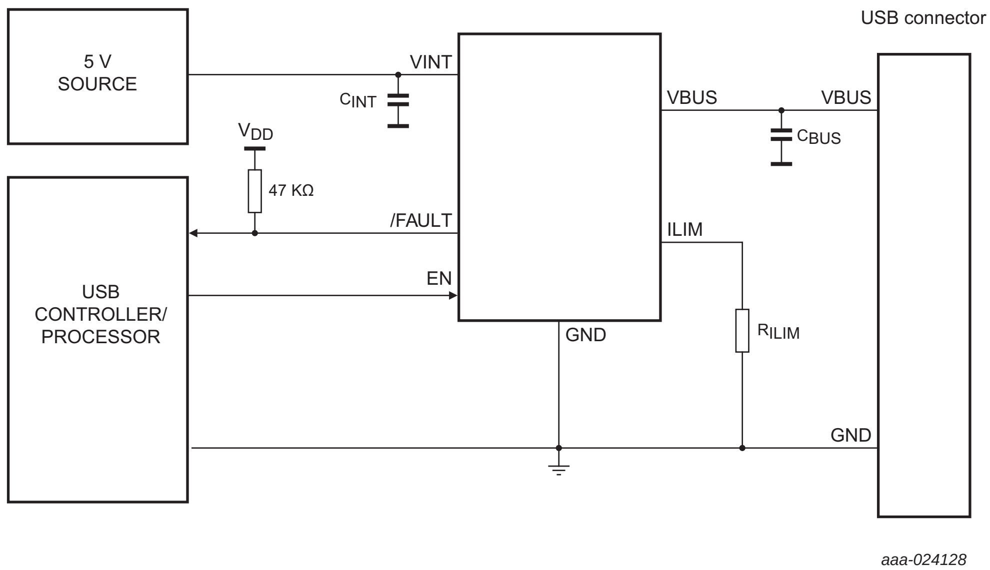
8.6 $\overline{FAULT}$ output

The $\overline{FAULT}$ output is an open-drain output that requires an external pull-up resistor. If any of the protection circuits is activated, the $\overline{FAULT}$ output will be set LOW to indicate a fault has occurred. The $\overline{FAULT}$ output will return to the high impedance state automatically once the fault condition is removed. An internal delay (de-glitch) circuit for the over-current protection (8 ms typical) and reverse-current protection (4 ms typical) is used when entering fault conditions. This ensures that $\overline{FAULT}$ is not accidentally asserted. Over-temperature condition will not be deglitched, the $\overline{FAULT}$ signal will be asserted immediately.

8.7 Over-temperature protection

When EN is HIGH, the device junction temperature exceeds 140 °C, the over-temperature protection (OTP) circuit will disable the N-channel MOSFET and indicate a fault condition by setting the $\overline{FAULT}$ pin LOW. Any transition on the EN pin will have no effect. Once the device temperature decreases below 115 °C the device will return to the defined state.

9. Application diagram



0.1 μF ceramic capacitor (C_{INT}) is required for local decoupling. Higher capacitor values C_{INT} further reduce the voltage drop at the input. When driving inductive loads, a larger capacitance C_{INT} prevents voltage spikes from exceeding absolute maximum voltage of VIN. The CBUS capacitor should be placed as closer as possible to VBUS pin.

Fig 4. Application diagram

10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VBUS, EN [1]	–0.5	+29	V
		VINT [2]	–0.5	+6	V
		ILIM	–0.5	+6	V
V_O	output voltage	$\overline{\text{FAULT}}$ [1]	–0.5	+6	V
I_{IK}	input clamping current	input EN: $V_{I(EN)} < -0.5$ V	–50	-	mA
		input ILIM: $V_{I(ILIM)} < -0.5$ V	–50	-	mA
$I_{I(source)}$	input source current	input IILIM	-	1	mA
I_{OK}	output clamping current	$V_O < 0$ V	–50	-	mA
I_{SK}	switch clamping current	input VIN: $V_{I(VIN)} < -0.5$ V	–50	-	mA
		output VOUT: $V_{O(VOUT)} < -0.5$ V	–50	-	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V [3]	-	3.6	A
$T_{j(max)}$	maximum junction temperature		–40	+150	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	[4]	-	910	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] Internally limited.

[4] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

11. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VINT	2.5	5.5	V
		EN; VBUS (OFF state)	0	20	V
VO	Output voltage	VBUS	0	5	V
I_{SW}	switch current	T_j = –40 °C to +85 °C	0	3	A
$I_{O(sink)}$	output sink current	output $\overline{\text{FAULT}}$	–10	-	mA
R_{ILIM}	current limit resistance	input ILIM [1]	16	140	kΩ
C_{dec}	decoupling capacitance	VIN to GND	0.1	-	µF
T_{amb}	ambient temperature		–40	+85	°C

[1] Current-limit threshold resistor range from ILIM to GND.

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	109	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13. Static characteristics

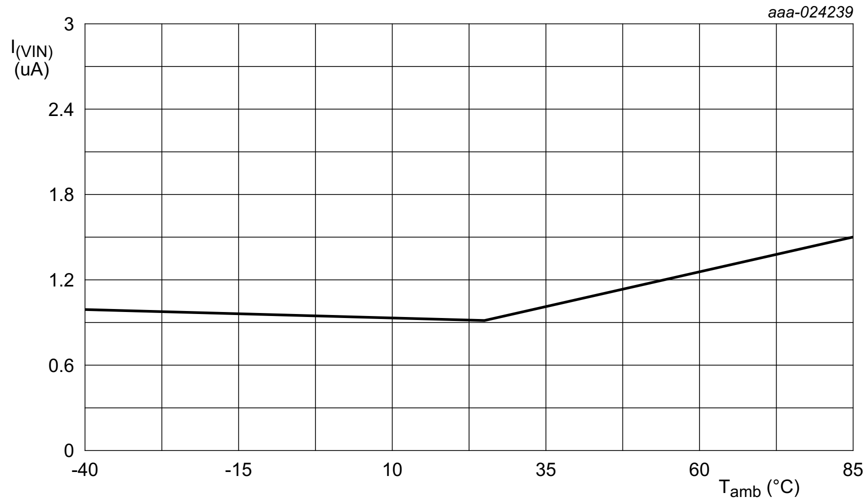
Table 9. Static characteristics

At recommended operating conditions; $V_{I(VINT)} = V_{I(EN)}$, $R_{FAULT} = 10$ kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 10

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	EN input; $V_{I(VINT)}$ = 2.5 V to 5.5 V;	1.2	-	-	V
V_{IL}	LOW-level input voltage	EN input; $V_{IVINT)}$ = 2.5 V to 5.5 V;	-	-	0.4	V
I_I	input leakage current	EN input; $V_{I(VINT)}$ = 5.0 V;	-	-	7.5	μA
$I_{(VIN)}$	supply current	VBUS open; $V_{I(VINT)}$ = 5.0 V				
		EN = GND (low power mode);	-	0.9	5	μA
		EN = $V_{I(VIN)}$; R_{ILIM} = 33 kΩ	-	196	280	μA
		EN = $V_{I(VIN)}$; R_{ILIM} = 16 kΩ	-	210	290	μA
$I_{S(OFF)}$	VBUS OFF-State leakage current	$V_{I(VINT)}$ = 5.0 V; $V_{I(VBUS)}$ = 0 V; EN = LOW	-	1	10	μA
	VINT OFF-state leakage current	VI(VBUS) = 5.0 V; $V_{I(VINT)}$ = 0 V; EN = LOW	-	1	10	μA
$I_{S(ON)}$	RCP leakage current	$V_{I(VINT)}$ = 0 V; $V_{I(VBUS)}$ = 5 V; EN = 5 V	-	0.9	10	μA
Rpd	EN pin Pull-down resistance	$V_{I(VINT)}$ = 5 V		1		MΩ
V_{trip}	trip level voltage	RCP; $V_{I(VINT)}$ = 2.5 V to 5.5 V	-	40	-	mV
V_{UVLO}	under voltage lockout voltage	VINT pin	-	2.27	2.45	V
$V_{hys(UVLO)}$	under voltage lockout hysteresis voltage		-	100	-	mV
V_{OL}	LOW-level output voltage	$\overline{FAULT}$; I_O = 8 mA	-	-	0.5	V
CI	EN pin		-	13.5	-	pF

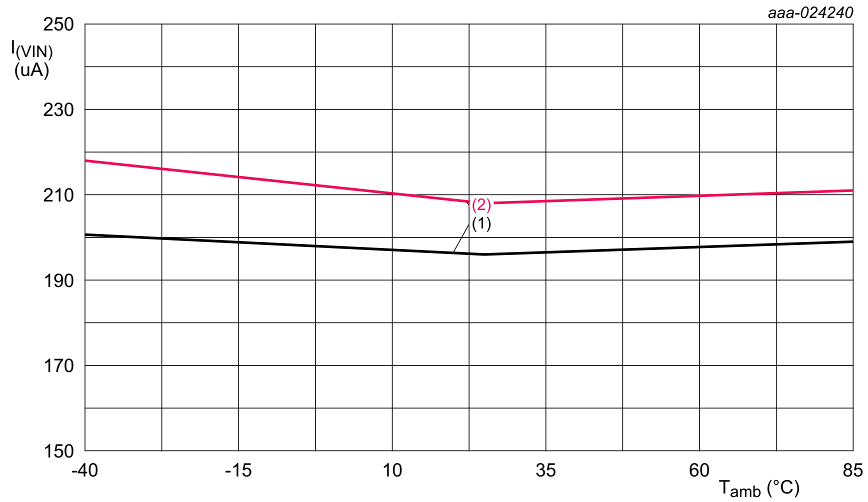
[1] Typical values are measured at T_{amb} = 25 °C.

13.1 Graphs



$V_{I(EN)}$ = GND; $V_{I(VINT)}$ = 5.0 V

Fig 5. OFF state supply current versus temperature

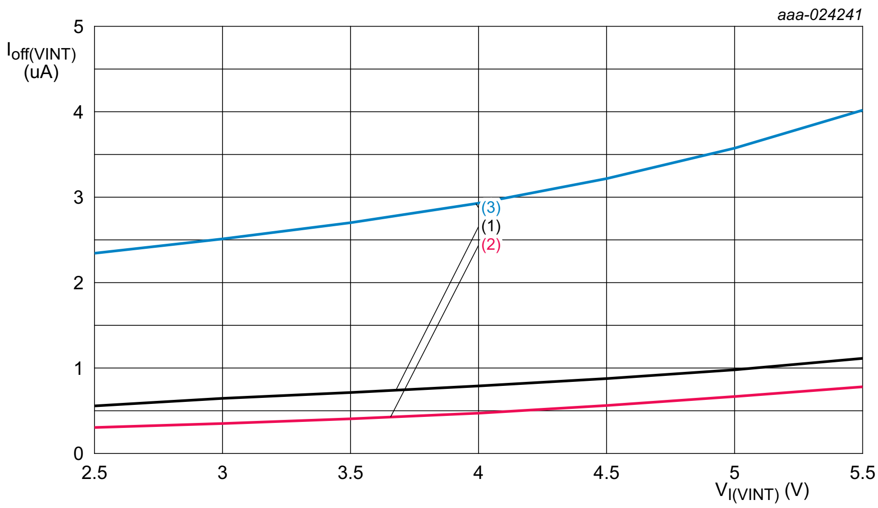


$V_{I(EN)} = V_{I(VINT)}$; $V_{I(VINT)}$ = 5.0 V

(1) R_{ILIM} = 33 KΩ

(2) R_{ILIM} = 16 KΩ

Fig 6. ON state supply current versus temperature



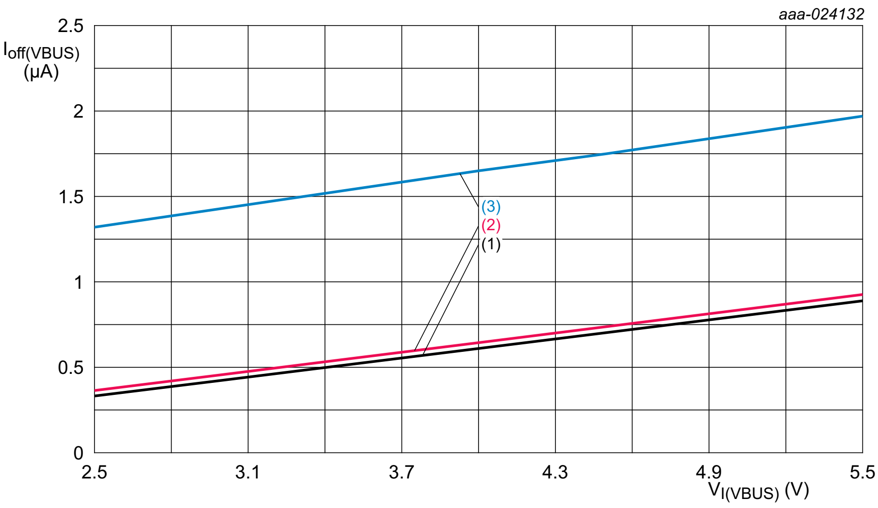
$V_{I(EN)}$ = GND; $V_{I(VBUS)}$ = 0 V; R_{ILIM} = 16 KΩ

(1) T_{amb} = -40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 7. VBUS off state leakage versus temperature



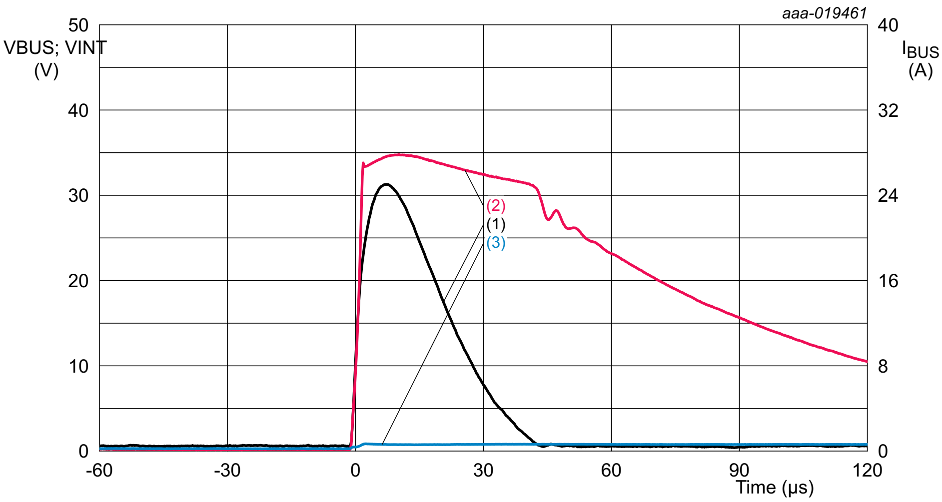
$V_{I(EN)}$ = GND; $V_{I(VINT)}$ = 0 V; R_{ILIM} = 16 KΩ

(1) T_{amb} = -40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 8. VINT off state leakage versus temperature



R_{ILIM} = 20 kΩ; $V_{I(VINT)}$ = 0 V

(1) Surge current

(2) Surge voltage on VBUS

Fig 9. Surge protection waveform

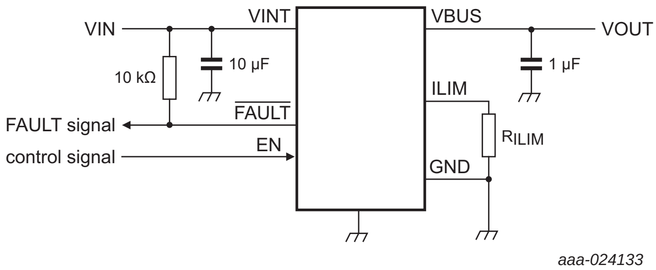


Fig 10. Typical characteristics reference schematic

13.2 Thermal shutdown

Table 10. Thermal shutdown

$V_{I(VINT)} = V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(ots)}$	over temperature shutdown threshold temperature	$V_{I(VINT)}$ = 2.5 to 5.5 V	-	140	-	°C
$T_{th(otp)hys}$	hysteresis of over temperature protection threshold temperature	$V_{I(VINT)}$ = 2.5 to 5.5 V	-	25	-	°C

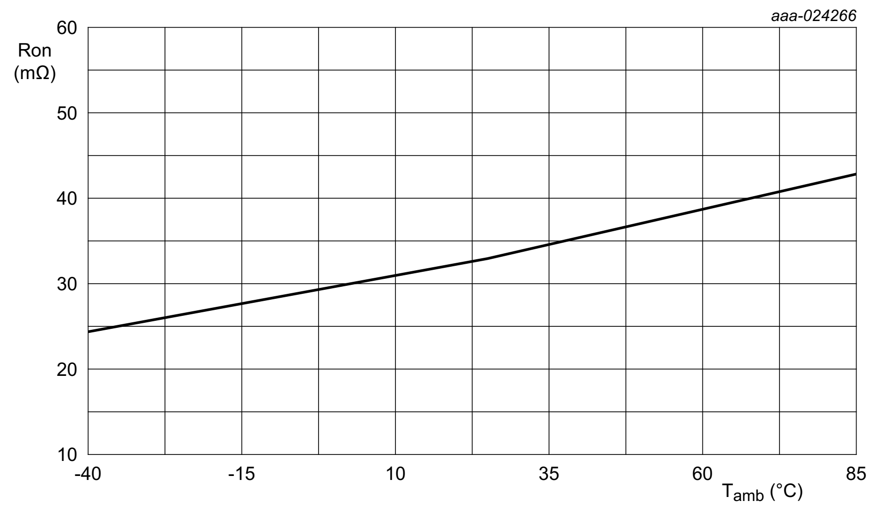
13.3 ON resistance

Table 11. ON resistance

$V_{I(VINT)}$ = $V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 10

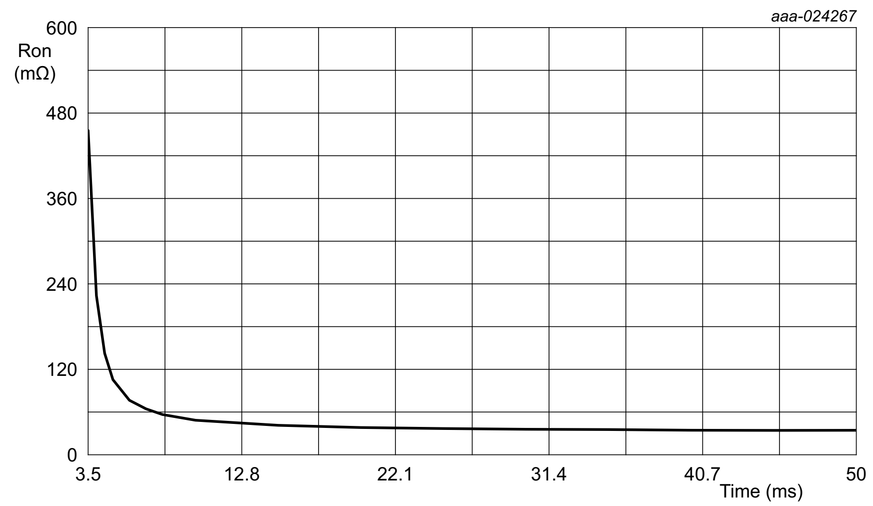
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	ON resistance	$V_{I(VINT)}$ = 2.5 to 5.5 V; see Figure 11				
		T_{amb} = 25 °C	-	34	37	mΩ
		T_{amb} = −40 °C to +85 °C	-	-	46	mΩ

13.4 ON resistance graphs



$V_{I(VINT)}$ = 5.0 V

Fig 11. Typical ON resistance versus temperature



$V_{I(VINT)}$ = 5.0 V

Fig 12. Typical ON resistance versus enable time

13.5 Current limit

Table 12. Current limit

$V_{I(VINT)} = V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 10

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{ocp}	over current protection current	$V_{I(VINT)}$ = 2.5 to 5.5 V; T_{amb} = –40 °C to +85 °C;				
		R_{ILIM} = 140 kΩ	330	421	465	mA
		R_{ILIM} = 100 kΩ	480	581	625	mA
		R_{ILIM} = 54 kΩ	915	1057	1107	mA
		R_{ILIM} = 33 kΩ	1505	1723	1780	mA
		R_{ILIM} = 24.5 kΩ	2085	2330	2398	mA
		R_{ILIM} = 20 kΩ	2567	2848	2920	mA
		R_{ILIM} = 16 kΩ	3186	3490	3585	mA
		ILIM shorted to VINT	125	180	220	mA

[1] Typical values are measured at T_{amb} = 25 °C. 1 % tolerance resistor is recommend for R_{ILIM}

I_{ocp} can be calculated with below equation, x = R_{ILIM} (kΩ):

$$I_{OCP(MAX)} = 49495x^{-0.948} \quad (1)$$

$$I_{OCP(TYP)} = 52775x^{-0.979} \quad (2)$$

$$I_{OCP(MIN)} = 57949x^{-1.042} \quad (3)$$

13.6 Current limit graphs

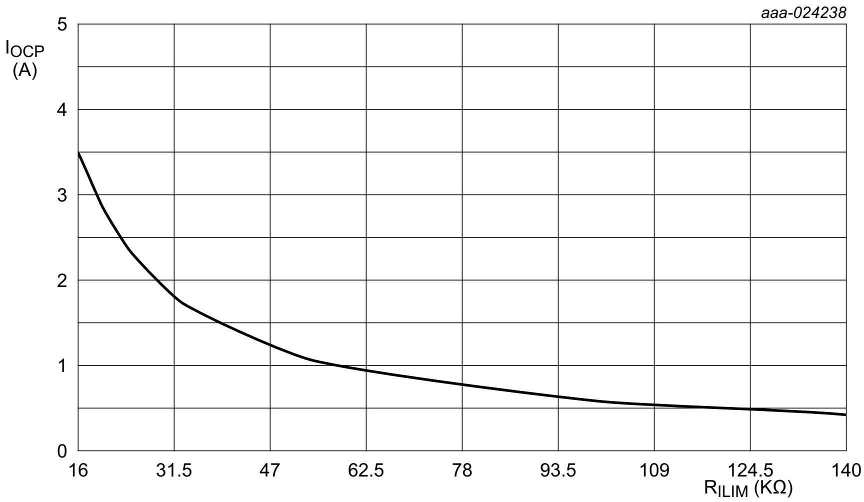


Fig 13. Typical over current protection current versus external resistor value R_{ILIM}

14. Dynamic characteristics

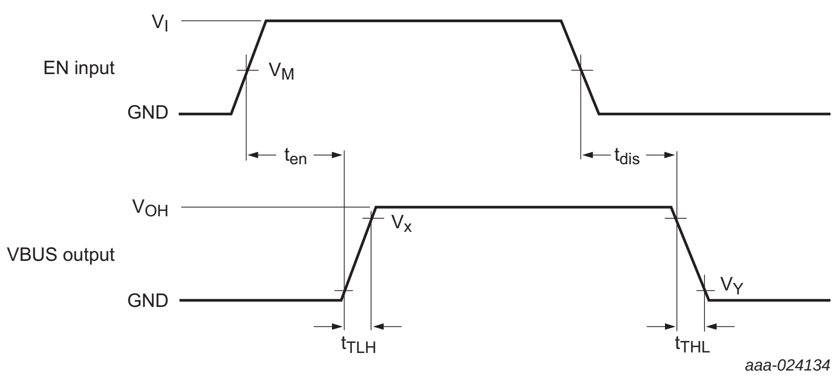
Table 13. Dynamic characteristics

At recommended operating conditions; $V_{I(VINT)} = V_{I(EN)}$, $R_{FAULT} = 10\ k\Omega$ unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{TLH}	LOW to HIGH output transition time	V_{OUT}; $C_L = 1\ \mu F$; $R_L = 100\ \Omega$; see Figure 14 and Figure 15				
		$V_{I(VINT)} = 5.0$ V	-	2.5	-	ms
		$V_{I(VINT)} = 2.5$ V	-	1.4	-	ms
t_{THL}	HIGH to LOW output transition time	V_{OUT}; $C_L = 1\ \mu F$; $R_L = 100\ \Omega$; see Figure 14 and Figure 15				
		$V_{I(VINT)} = 5.0$ V	-	0.2	-	ms
		$V_{I(VINT)} = 2.5$ V	-	0.2	-	ms
t_{en}	enable time	EN to V_{OUT}; $C_L = 1\ \mu F$; $R_L = 100\ \Omega$; seeFigure 14and Figure 15				
		$V_{I(VINT)} = 5.0$ V	-	1.5	-	ms
t_{dis}	disable time	EN to V_{OUT}; $C_L = 1\ \mu F$; $R_L = 100\ \Omega$; see Figure 14 and Figure 15				
		$V_{I(VINT)} = 5.0$ V	-	13	-	µs
t_{degl}	deglitch time	$\overline{FAULT}$ in OCP; $V_{I(VINT)} = 5$ V	-	8	-	ms
		RCP; FAULT in RCP; $V_{I(VINT)} = 5$ V	-	4	-	ms

[1] Typical values are measured at $T_{amb} = 25$ °C.

14.1 Waveform and test circuits



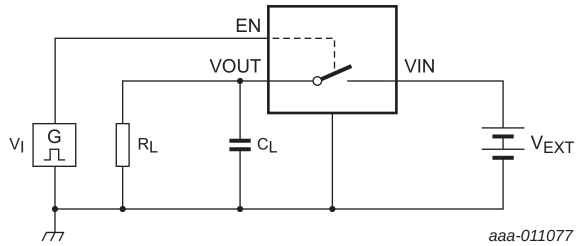
Measurement points are given in Table 14.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 14. Switching times and rise and fall times

Table 14. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VIN)}$	V_M	V_X	V_Y
5.0 V	$0.5 \times V_{I(EN)}$	$0.9 \times V_{OH}$	$0.1 \times V_{OH}$



Test data is given in Table 15.

Definitions test circuit:

R_L = Load resistance.

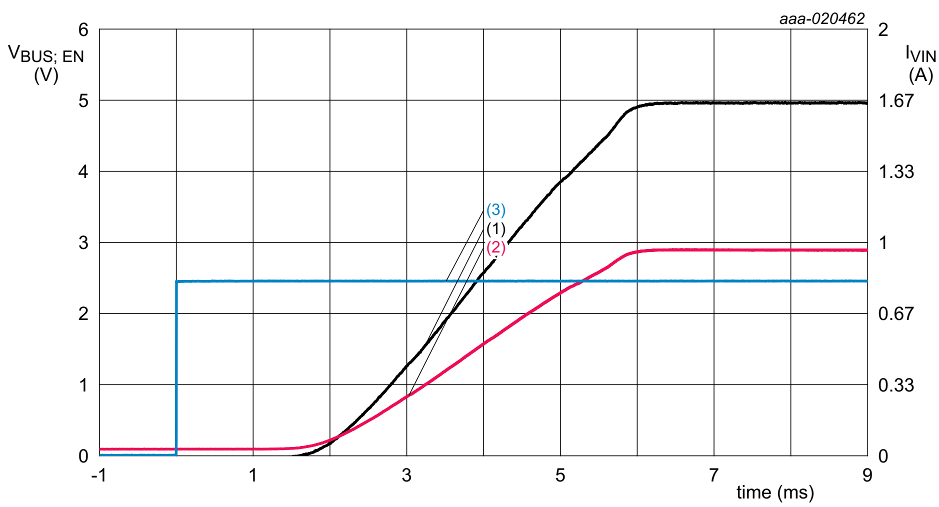
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 15. Test circuit for measuring switching times

Table 15. Test data

Supply voltage	EN Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_L
5.0 V	0 to $V_{I(VIN)}$	1 μF	100 Ω



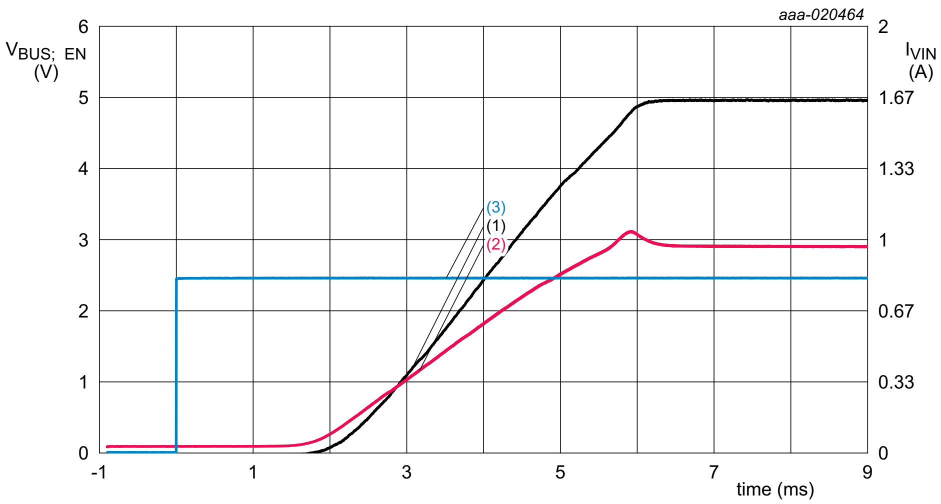
$V_{I(VINT)}$ = 5 V; R_L = 5.1 Ω; C_L = 1 μF;

(1) $V_{O(VBUS)}$

(2) $I_{(VIN)}$

(3) $V_{I(EN)}$

Fig 16. Typical 1 μF load enable time and inrush current



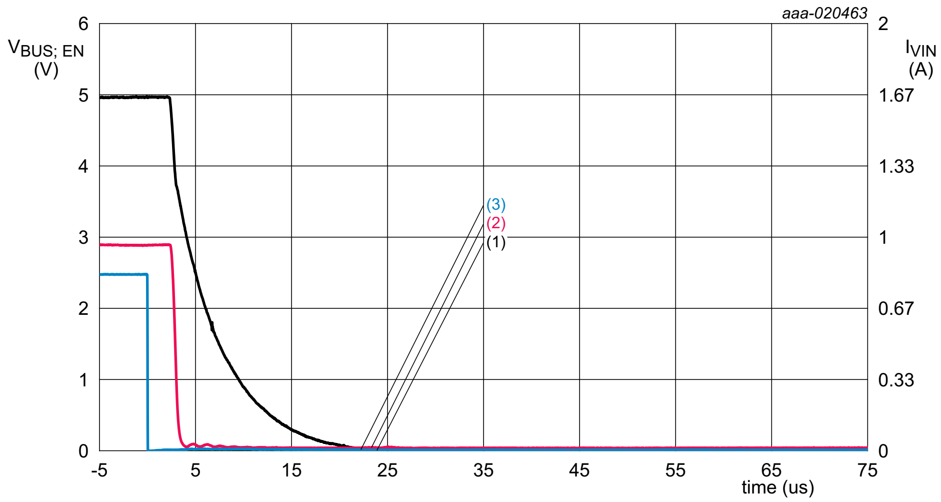
$V_{I(VIN)}$ = 5 V; R_L = 5.1 Ω; C_L = 100 μF;

(1) $V_{O(VBUS)}$

(2) $I_{(VIN)}$

(3) $V_{I(EN)}$

Fig 17. Typical 100 μF load enable time and inrush current



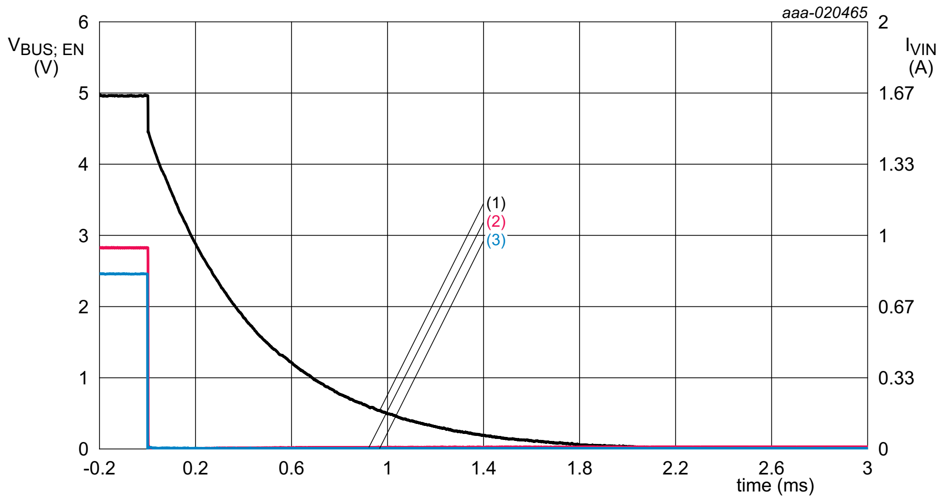
$V_{I(VINT)}$ = 5 V; R_L = 5.1 Ω; C_L = 1 μF;

(1) $V_{O(VBUS)}$

(2) $I_{(VIN)}$

(3) $V_{I(EN)}$

Fig 18. Typical 1 μF load turn off



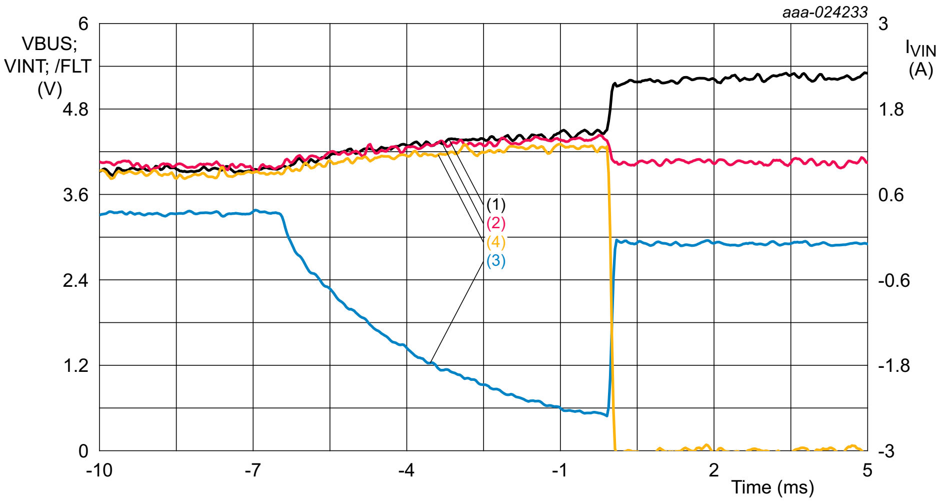
$V_{I(VIN)}$ = 5 V; R_L = 5.1 Ω; C_L = 100 μF

(1) $V_{O(VBUS)}$

(2) $I_{(VIN)}$

(3) $V_{I(EN)}$

Fig 19. Typical 100 μF load turn off



$V_{I(VINT)}$ = 4 V

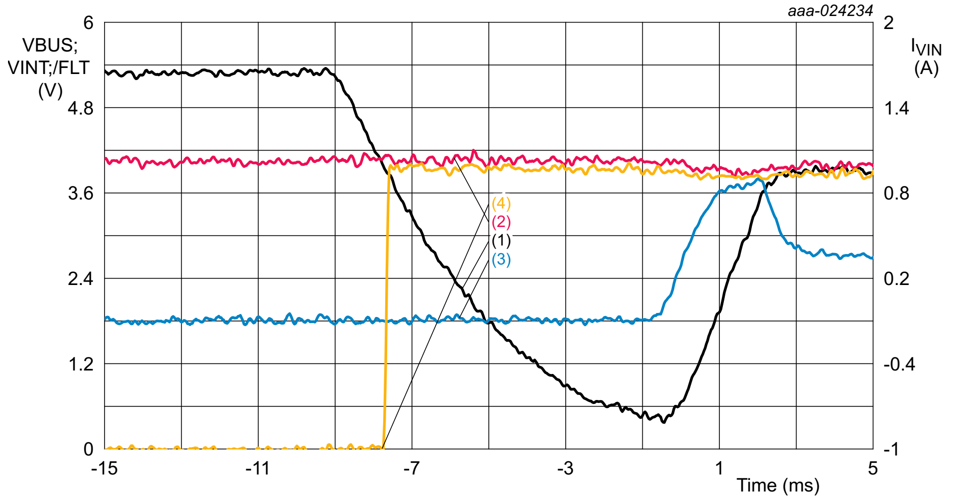
(1) $V_{O(VBUS)}$

(2) $V_{I(VINT)}$

(3) $I_{(VIN)}$

(4) $\overline{FAULT}$

Fig 20. Reverse-current protection response



$V_{I(VIN)}$ = 4V

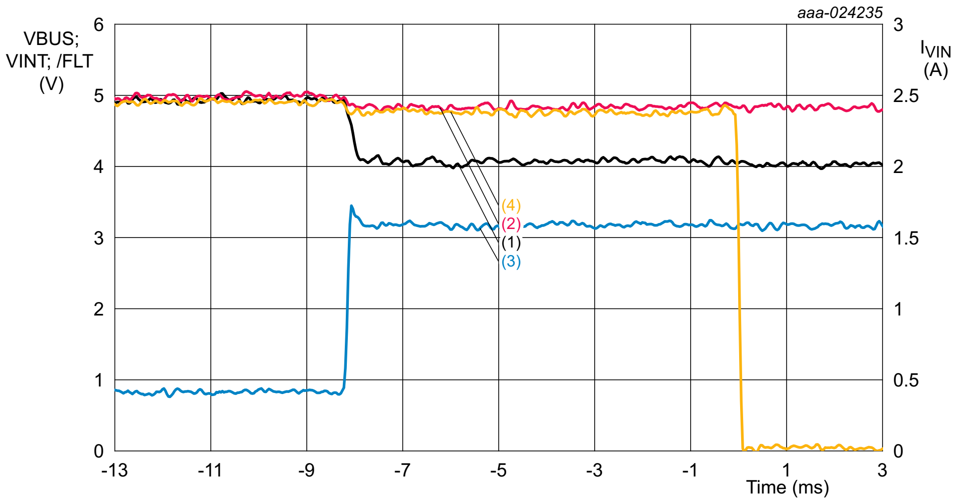
(1) $V_{O(VBUS)}$

(2) $V_{I(VINT)}$

(3) $I_{(VIN)}$

(4) $\overline{\text{FAULT}}$

Fig 21. Reverse-current protection recovery



$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ.

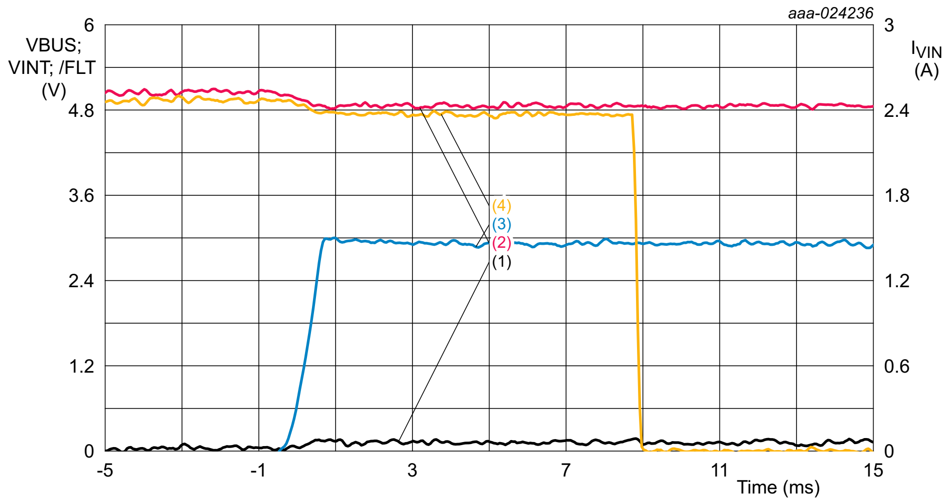
(1) $V_{O(VBUS)}$.

(2) $V_{I(VINT)}$

(3) $I_{(VIN)}$

(4) $\overline{\text{FAULT}}$

Fig 22. Device into current limit after enabled



$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ.

(1) $V_{O(VBUS)}$

(2) $V_{I(VINT)}$

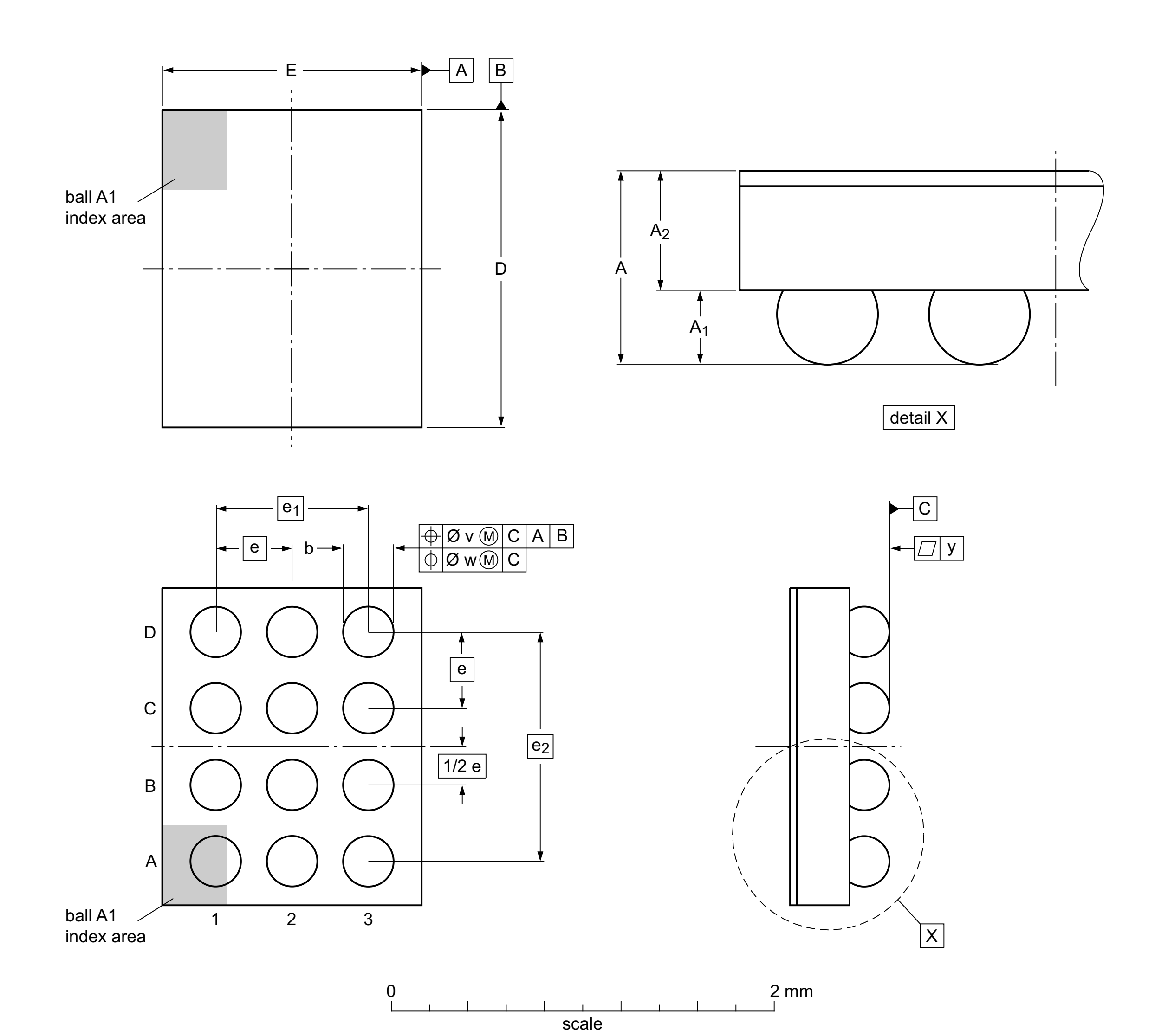
(3) $I_{(VIN)}$

(4) $\overline{FAULT}$

Fig 23. Device start up with VBUS short to GND

15. Package outline

WLCSP12: wafer level chip-scale package;
12 bumps; 1.65 x 1.35 x 0.525 mm (Backside coating included) **SOT1390-5**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.565	0.23	0.350	0.29	1.68	1.38						
mm	nom	0.525	0.20	0.325	0.26	1.65	1.35	0.4	0.8	1.2	0.05	0.15	0.03
	min	0.485	0.17	0.300	0.23	1.62	1.32						

Note: Backside coating 25 µm

sot1390-5_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1390-5		- - -				~~15-07-15~~ 15-11-03

Fig 24. Package outline WLCSP12

16. Packing information

16.1 Packing method

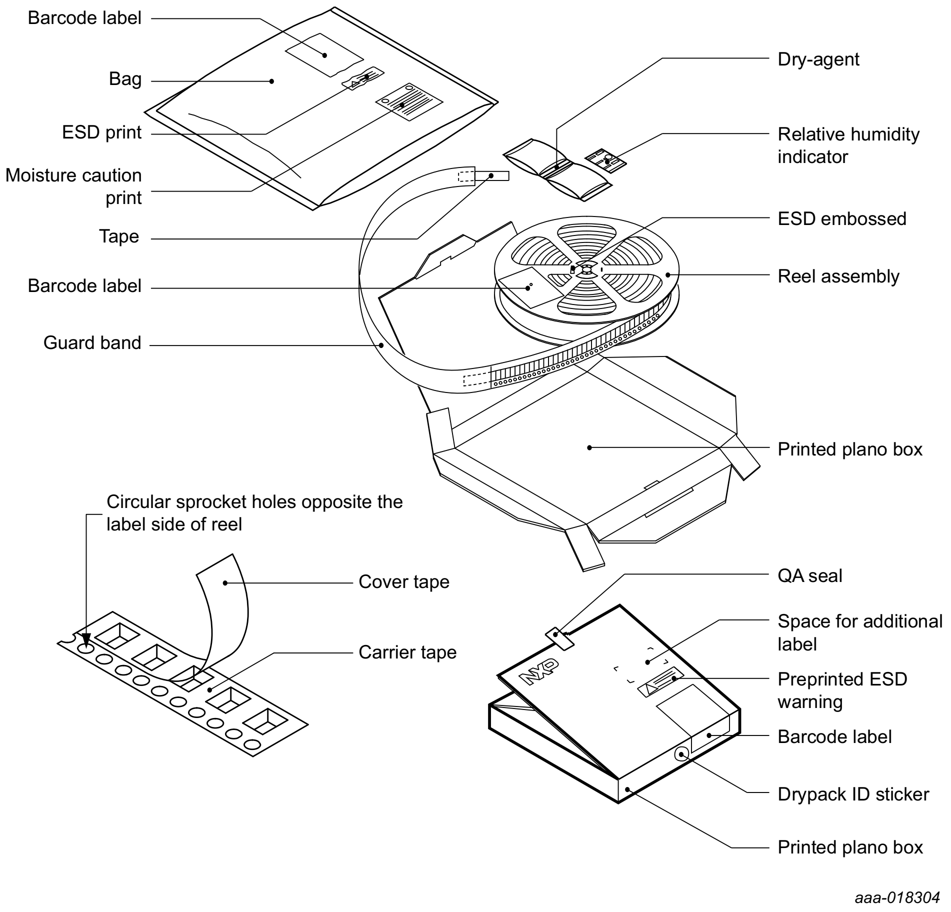


Fig 25. Reel dry pack for SMD: guard band; embossed tape

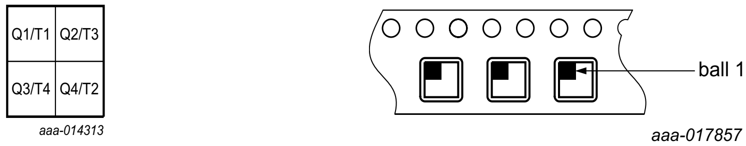
Table 16. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
180 × 8	3000	1	209 × 206 × 34

[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.
View ordering and availability details at NXP order portal, or contact your local NXP representative.

16.2 Product orientation



Tape pocket quadrants

Ball 1 is in quadrant Q1/T1

Fig 26. Product orientation in carrier tape

16.3 Carrier tape dimensions

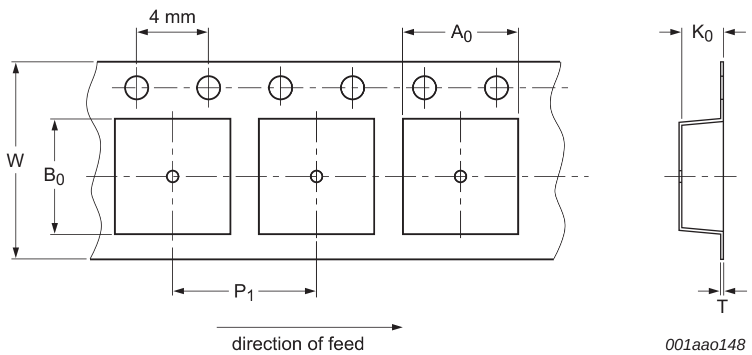


Fig 27. Carrier tape dimensions

Table 17. Carrier tape dimensions

In accordance with IEC 60286-3.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
1.61 ± 0.05	1.78 ± 0.05	0.73 ± 0.05	0.25 ± 0.02	4.0 ± 0.1	8 + 0.3 / – 0.1

16.4 Reel dimensions

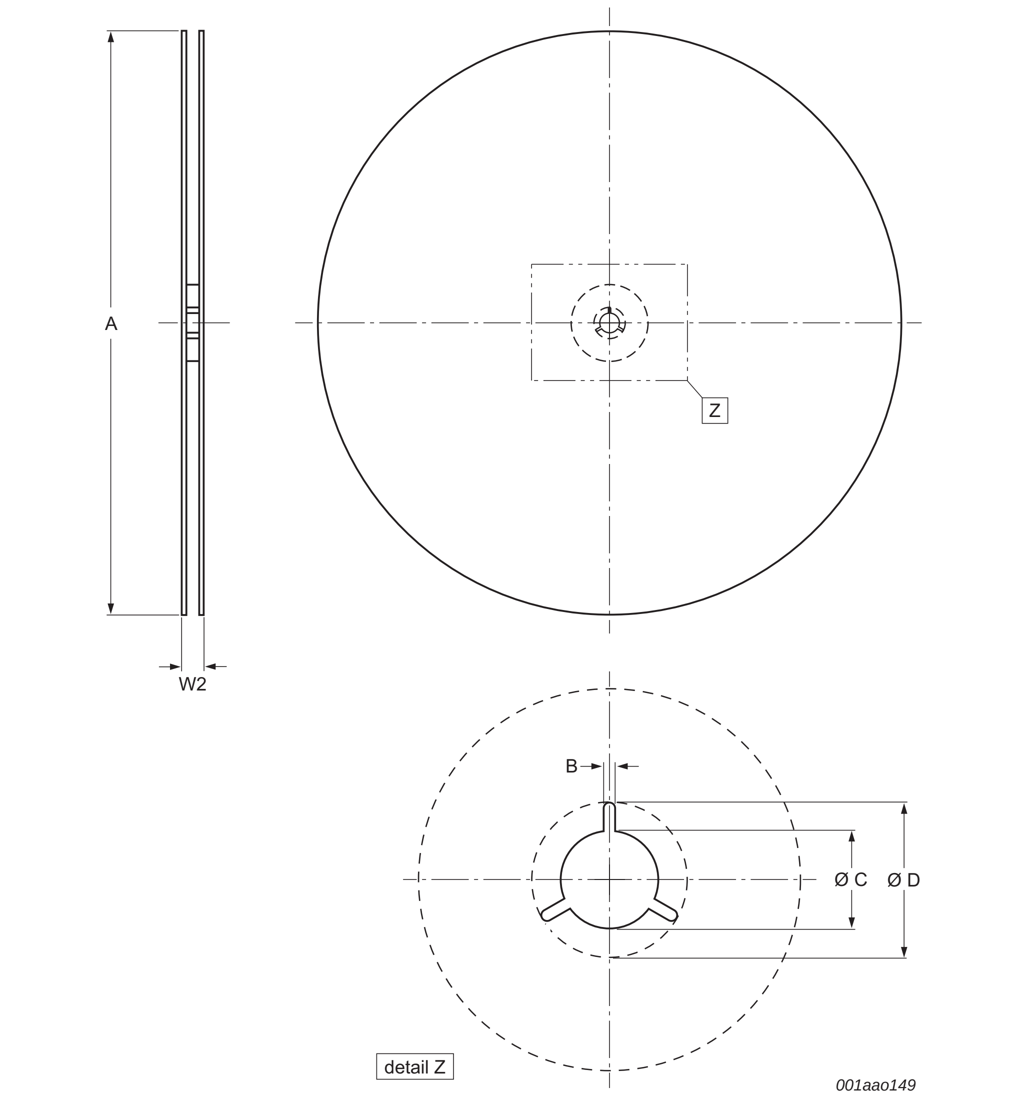


Fig 28. Schematic view of reel

Table 18. Reel dimensions

In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
180	14.4	1.5	12.8	20.2

16.5 Barcode label

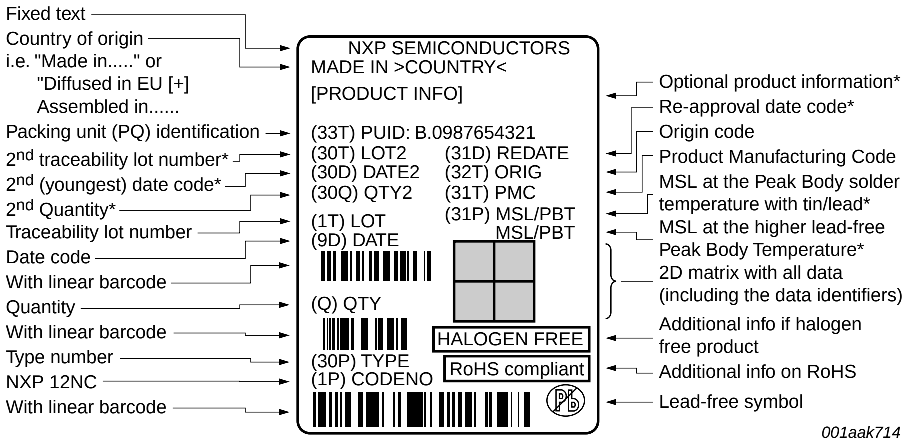


Fig 29. Example of typical box and reel information barcode label

Table 19. Barcode label dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	100 × 75

17. Soldering of WLCSP packages

17.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

17.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

17.3 Reflow soldering

Key characteristics in reflow soldering are:

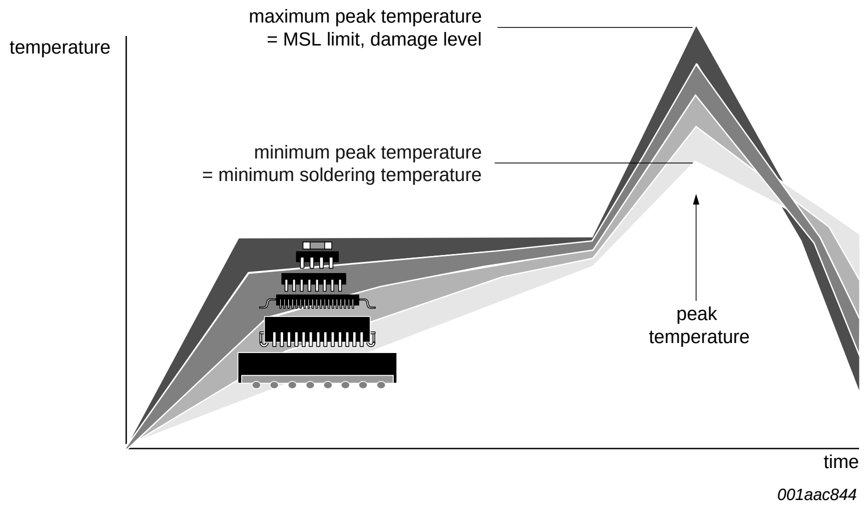
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 30) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 20.

Table 20. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 30.



MSL: Moisture Sensitivity Level

Fig 30. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

17.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

17.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

17.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

17.3.4 Cleaning

Cleaning can be done after reflow soldering.

18. Abbreviations

Table 21. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
CDM	Charged Device Model
HBM	Human Body Model
USB	Universal Serial Bus
VOIP	Voice over Internet Protocol

19. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5P3090 v.1	20160801	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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22. Contents

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