

NX5P3363/Q100

USB PD and Type-C current-limited power switch

Rev. 1.1 — 10 September 2024

Product data sheet

1 General description

The NX5P3363/Q100 is a precision adjustable current-limited power switch for USB PD application. The device includes undervoltage lockout, overtemperature protection, and reverse current protection circuits to automatically isolate the switch terminals when a fault condition occurs. The 29 V tolerance on VBUS pin ensures the device is able to work on a USB PD port; a current limit input (ILIM) pin defines the overcurrent limit threshold; an open-drain fault output (FLT) indicates when a fault condition has occurred.

The overcurrent limit threshold can be programmed from 400 mA to 3.3 A, using an external resistor between the ILIM pin and GND pin. In the overcurrent condition, the device clamps the output current to the value set by ILIM and keeps the switch on while asserting the FLT flag.

To minimize current surges during normal turn on, the device has built-in soft start by limiting the power switch turn on slew rate. However, user can disable the soft start and request a fast output by pulling FO pin HIGH.

A fast recovery reverse current protection (RCP) circuit has been added to the switch to prevent reverse current flowing back to power source at all times. When exiting from reverse current protection state, the power MOSFET turns on within 50 μ s. The fast RCP recovery ensures the voltage on VBUS doesn't drop too much in a power source swap application.

NX5P3363/Q100 is offered in a 2.2 x 2.2 mm, 16 bump WLCSP package.



2 Features and benefits

- VIN supply voltage range from 4.0 V to 5.5 V
- All time reverse current protection with ultra fast RCP recovery
- Adjustable current limit from 400 mA to 3.3 A
- Clamped current output in overcurrent condition
- 29 V high voltage tolerance on VBUS pin
- Low ON resistance of the power FETs: 35 mΩ (typical) in total
- Surge protection: IEC61000-4-5 exceeds ±80 V on VBUS
- Over temperature protection
- Qualified in accordance with AEC-Q100 Grade 3 compliance
- Safety approvals
 - UL 62368-1, 2nd edition, file no. 20170804-E470128
 - IEC 62368-1, 2nd edition, file no. DK-65509-UL
- ESD protection
 - IEC61000-4-2 contact discharge exceeds 8 kV on VBUS
 - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - CDM AEC standard Q100-01 (JESD22-C101E) exceeds 500 V
- Specified from -40 °C to +85 °C ambient temperature

3 Applications

- Automotive USB Type-C port
- Automotive power switch

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NX5P3363UK/Q100	X5PT7	WLCSP16	wafer level chip-scale package; 16 bumps; 2.2 x 2.2 mm x 0.555 mm (backside coating included)	SOT1394-3

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX5P3363UK/Q100	NX5P3363UKZ/Q100	WLCSP16	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	3000	T _{amb} = -40 °C to +85 °C

5 Marking

Table 3. Marking

Line	Marking	Description
A	X5PT7	basic type name
B	mmmmmmnn	wafer lot code (mmmmmm) and wafer number (nn)
C	XtDYYWW	manufacturing code: X = foundry location t = assembly location D = RoHS code (dark green) YY = assembly year code WW = assembly week code

6 Functional diagram

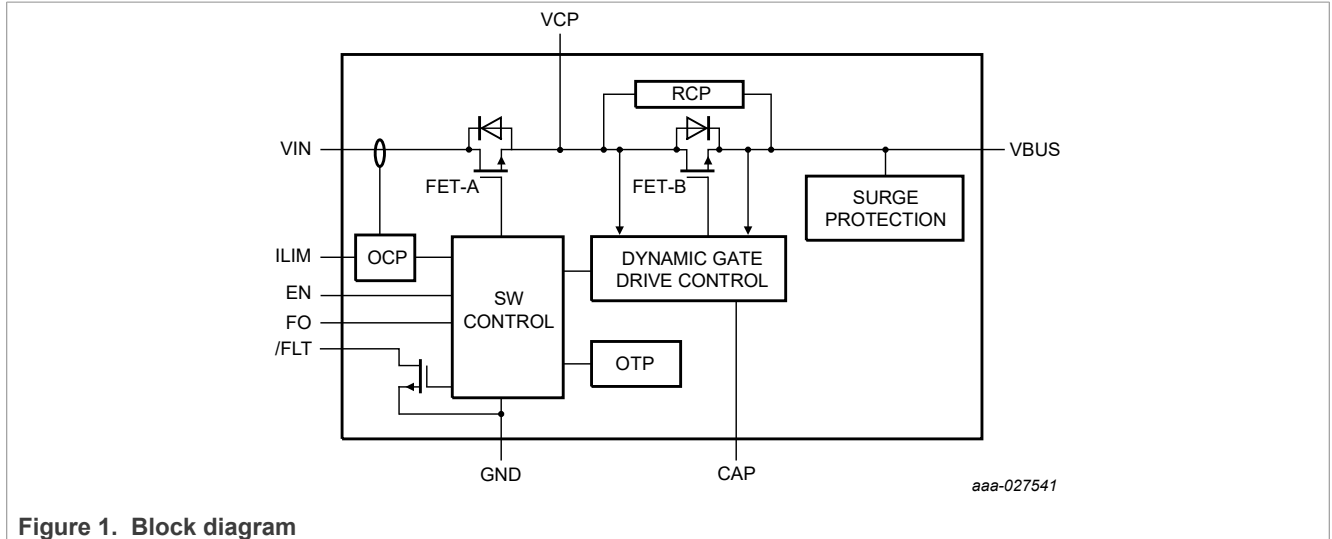


Figure 1. Block diagram

7 Pinning information

7.1 Pinning

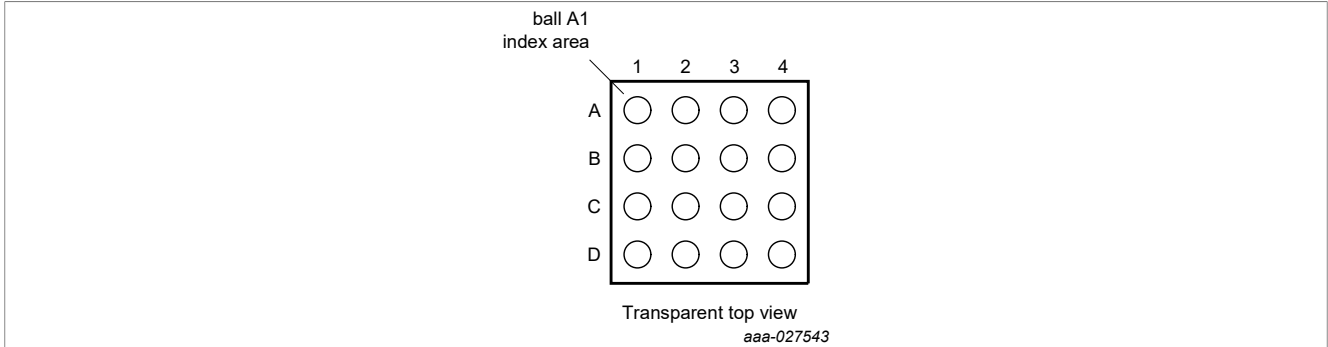


Figure 2. Pin configuration for WLCSP16

	1	2	3	4
A	VIN	VIN	ILIM	/FLT
B	VCP	VCP	GND	EN
C	VCP	VBUS	GND	FO
D	VBUS	VBUS	GND	CAP

Transparent top view
aaa-023807

Figure 3. Ball mapping for WLCSP16

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VIN	A1, A2	Input voltage
VCP	B1, B2, C1	Central point of two power MOSFETs
VBUS	C2, D1, D2	Output voltage
ILIM	A3	Current limiter. Connect a resistor to GND to adjust the current limit level
FLT	A4	Fault condition indicator (open-drain output)
EN	B4	Enable input (active HIGH with internal 1 MΩ pull down resistor)
GND	B3, C3, D3	Ground (0 V)
FO	C4	Fast turn on. Pull this pin HIGH to enable fast turn-on feature. 1 MΩ pull down resistor integrated.
CAP	D4	Connect a capacitor to GND

8 Functional description

Table 5. Function table

H = HIGH voltage level; L = LOW voltage level

EN	FO	VIN	FLT	Main Power Switch
X	X	< 4.0 V	Z	under voltage lockout, Switch open
L	X	4.0 V to 5.5 V	Z	disabled; switch open
H	L	4.0 V to 5.5 V	Z	enabled; switch turns on with slew rate control
H	H	4.0 V to 5.5 V	Z	enabled; switch turns on without slew rate control; fast turn on
H	X	4.0 V to 5.5 V	L	In current limit condition or over temperature protection
X	X	4.0 V to 5.5 V and VIN ≤ VBUS	Z	Reverse protection; switch open

8.1 EN input

When the EN is set LOW, all the FETs are disabled, and the device enters low-power mode disabling all protection circuits and setting the FLT output high impedance. When EN is set HIGH, all protection circuits are enabled and then, if no fault condition exists, the main power MOSFETs turn on.

8.2 Fast recovery RCP

NX5P3363/Q100 uses dynamic gate drive control loop to implement reverse-current protection. During normal operation, device always tries to regulate the VBUS output voltage to be VIN - 70 mV.

When the load current produces a drop voltage greater than 70 mV, the gate control loop drives the power MOS to lower its R_{DSon} to try to achieve the 70 mV. In the heavy load condition, the gate control loop keeps increasing the gate driving current of the MOSFET until it is fully on and remains fully on if the voltage drop at that time still exceeds 70 mV.

In light load condition, when the drop voltage is below 70 mV, the gate control loop reduces the gate driving current to increase the R_{DSon} to try to achieve the 70 mV drop voltage, which leads to the complete shutdown of the power MOSFET in reverse voltage condition.

If VBUS voltage is higher than VIN when enabling the device, the power MOSFET never turns on. The device always does a pre-check before switching on the power MOSFETs.

In the RCP state, EN is HIGH; when the VBUS drops below VIN, the device exits the RCP state and turns on the power FET again within 50 μs. The fast recovery of the power MOSFET is assisted by the external boost capacitor at CAP pin. The boost capacitor is charged whenever EN is pulled HIGH.

The input voltage level of FO pin has nothing to do with RCP recovery time.

8.3 VBUS hot plug-in RCP

The RCP circuit, together with dynamic gate drive control circuit, acts like an "ideal diode". This protects the VIN lifting from reverse current when VBUS has a hot plug-in during the following conditions and limits the VIN voltage lift < 400 mV. Refer to NX5P3363/Q100 ground pin.

- VBUS < 24 V, plug-in when NX5P3363/Q100 is on
- C_{IN} is in the range of 57 μF to 100 μF
- C_{BUS} is in the range of 10 μF to 22 μF

If the V_{BUS} , C_{IN} , C_{BUS} are not in the range or conditions, there may be more reverse current and the VIN voltage lift depends on the conditions.

8.4 Fast Turn ON

In order to reduce the power on inrush current, NX5P3363/Q100 deploys slew rate control for normal turn on; there is approximately 2 ms rising time. However, in the fast role swap application, fast turn on is requested. The customer achieves this by pulling FO pin HIGH. By doing this, rise time is reduced to the 100 μ S level. There is an internal 1 M Ω pull-down resistor on this pin. The fast turn on is achieved by turn off short circuit protection and OCP feature in the fast start stage; typically 220 μ s. It is recommended to add a 10 μ F capacitor close to VIN pin to limit the inrush current in fast turn on mode.

The feature only applies to fast role swap, and FO pin should be controlled by USB PD PHY. When a fast role swap event is detected by USB PD PHY, the FO pin should pull HIGH first, then enable the EN pin of NX5P3363/Q100 when the FRS is requested. Depending on the voltage on VBUS, there are two scenarios:

1. $V(V_{BUS}) > V(VIN)$: The switch enters RCP mode. Once the voltage on VBUS drops below VIN voltage, switch immediately turns on within 50 μ S.
2. $V(V_{BUS}) \leq V(VIN)$
The switch performs a fast turn ON as the FO is HIGH; the turn on time is 150 μ S.

When fast role swap is finished and NX5P3363/Q100 is in all the other conditions, FO pin should remain LOW to limit the inrush current.

8.5 Undervoltage lockout

Independently of the logic level on the EN pin, the undervoltage lockout (UVLO) circuit disables the N-channel MOSFET and enters low power mode until the input voltage reaches the UVLO turn-on threshold V_{UVLO} .

8.6 ILIM

The overcurrent protection circuit's (OCP) trigger value I_{OCP} can be set using an external resistor R_{ILIM} connected between ILIM pin and GND pin. When EN is set HIGH and the ILIM pin is grounded, the N-channel MOSFET is disabled. The I_{OCP} setting is given in [Table 12](#).

8.7 Main power FET overcurrent protection (OCP)

The device offers overcurrent protection when enabled. The three possible overcurrent conditions that can occur are:

1. Overcurrent at startup: $I_{SW} > I_{OCP}$ when enabling the N-channel MOSFET.
2. Overcurrent when enabled: $I_{SW} > I_{OCP}$ when the N-channel MOSFET is enabled.
3. Short circuit when enabled: I_{SW} exceeds short circuit conditions

In the overcurrent condition, because the device clamps the output current rather than the switch, the power dissipation on the device might be increased which could lead to overtemperature protection (see [Section 8.9](#)).

8.7.1 Overcurrent at startup

If the device senses a VBUS short to GND or overcurrent while enabling the N-channel MOSFET, OCP is triggered. It limits the output current to I_{OCP} and after the deglitch time sets the \overline{FLT} output LOW.

8.7.2 Overcurrent when enabled

If the device senses I_{SW} exceeds I_{OCP} when enabled, OCP is triggered. It limits the output current to I_{OCP} and after the deglitch time sets the \overline{FLT} output LOW. As a consequence, limiting the output current reduces $V_{O(VBUS)}$.

8.7.3 Short circuit when enabled

If the current through switch exceeds 7.5 A (typical), the short circuit protection is triggered. That disables the N-channel MOSFET immediately. It then enables the N-channel MOSFET again; output current is limited to I_{OCP} and after the deglitch time the \overline{FLT} output is set LOW. Thermal protection is triggered due to the big power consumption on the device.

In the customer specific application case, the short circuit protection ensures the V_{IN} voltage stays above 4.5 V at the following short circuit testing.

- $C_{IN} = 57 \mu\text{F}$, V_{BUS} short to GND directly by a metal tweezer; this means the short resistor to ground is typically 40 m Ω
- V_{IN} connected to customer specified DC-DC

8.8 \overline{FLT} output

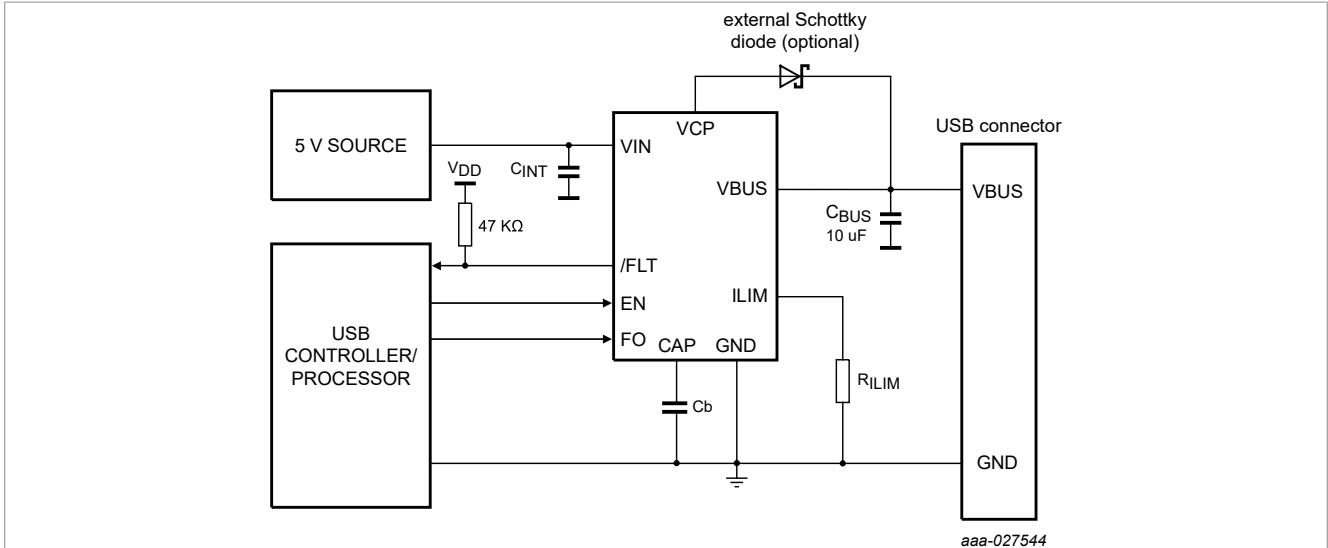
The \overline{FLT} output is an open-drain output that requires an external pull-up resistor. The \overline{FLT} output is set LOW to indicate an OCP or OTP condition has occurred. The \overline{FLT} output returns to the high impedance state automatically once the fault condition is removed. An internal 8 ms deglitch circuit for the overcurrent protection is used when entering fault conditions. Overtemperature condition doesn't have deglitch time, and the \overline{FLT} signal is asserted immediately. The RCP circuit won't trigger \overline{FLT} signal.

8.9 Overtemperature protection

If the device temperature exceeds 140 °C when EN is set HIGH, the overtemperature protection (OTP) circuit disables the Power MOSFET and indicates a fault condition by setting the \overline{FLT} pin LOW. Any transition on the EN pin has no effect. Once the device temperature decreases to below 115 °C the device returns to the defined state.

In the overcurrent limiting condition, the increased power dissipation on the device results in OTP, especially in the output-short-to-GND error.

9 Application diagram



A 0.1 μF ceramic capacitor (C_{INT}) is required for local decoupling. Higher capacitor values C_{INT} further reduce the voltage drop at the input. When driving inductive loads, a larger capacitance C_{INT} prevents voltage spikes from exceeding absolute maximum voltage of VIN. The CBUS capacitor should be placed as closer as possible to VBUS pin.

The recommended C_b is 1 nF with at least 16 V voltage tolerance.

The external Schottky diode is optional; NX5P3363/Q100 works well without it. To improve the lowest VBUS voltage during fast role swap, it is recommended to add a lower forward voltage diode, for example $V_F = 0.3$ V.

Figure 4. Application diagram

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _I	input voltage	VBUS	^[1] -0.5	+29	V
		VIN; VCP; ILIM; EN; FO	^[1] -0.5	+6	V
		CAP	^[1] -0.5	+12	V
	peak voltage tolerance	VBUS; 20 μs pulse width, 1 s interval	^[1] -0.5	+34	V
V _O	output voltage	$\overline{\text{FLT}}$	^[1] -0.5	+6	V
I _{IK}	input clamping current	input EN: V _{I(EN)} < -0.5 V	-50	-	mA
I _{I(source)}	input source current	input ILIM	-	1	mA
I _{SK}	switch clamping current	input VIN: V _{I(VIN)} < -0.5 V	-50	-	mA
		output VOUT: V _{O(VBUS)} < -0.5 V	-50	-	mA
I _{SW}	Main Power switch continuous current	V _{SW} > -0.5 V	^[2] -	3.6	A
T _{j(max)}	maximum junction temperature		-40	+125	°C
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		^[3] -	1.7	W

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] Internally limited.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _I	input voltage	V _{IN}	4.0	5.5	V
		EN; FO	0	5.5	V
		VBUS (OFF state)	0	23	V
V _O	Output voltage	VBUS; $\overline{\text{FLT}}$	0	5	V
I _{SW}	switch current	T _{amb} = -40 °C to +85 °C	0	3	A
I _{O(sink)}	output sink current	$\overline{\text{FLT}}$	0	10	mA
R _{ILIM}	current limit resistance	ILIM pin to GND	14.3	140	kΩ
C _{Bus}	VBUS output capacitance	VBUS to GND	10	100	μF
T _{amb}	ambient temperature		-40	+85	°C

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	58.4	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13 Static characteristics

Table 9. Static characteristics

At recommended operating conditions; $V_{I(VIN)} = V_{I(EN)}$, $R_{FAULT} = 10\text{ k}\Omega$ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See [Figure 9](#)

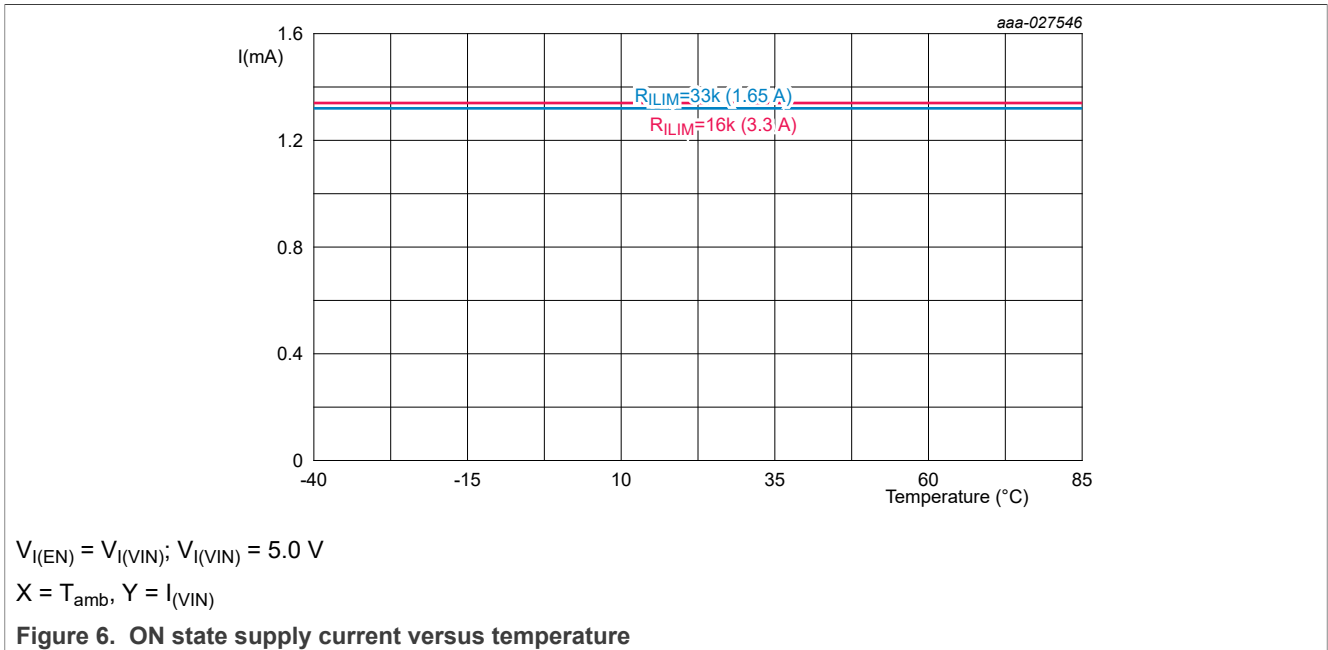
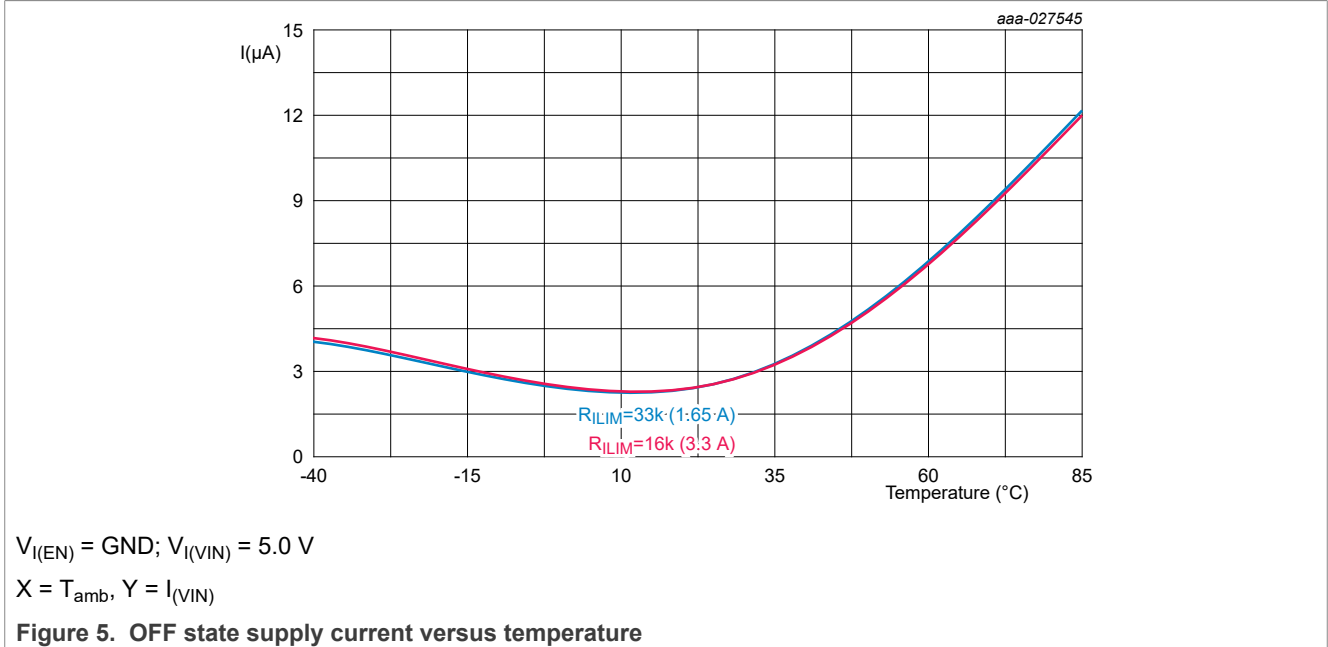
Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IH}	HIGH-level input voltage	EN; FO; $V_{I(VIN)} = 4.0\text{ V to }5.5\text{ V}$;	1.2	-	-	V
V_{IL}	LOW-level input voltage	EN; FO; $V_{I(VIN)} = 4.0\text{ V to }5.5\text{ V}$;	-	-	0.4	V
I_I	input leakage current	EN; FO; $V_{I(VIN)} = 5.0\text{ V}$;	-	-	7	μA
$I_{(VIN)}$	supply current	VBUS open; $V_{I(VIN)} = 5.0\text{ V}$				
		EN = GND (low power mode);	-	3	55	μA
		EN = $V_{I(VIN)}$; $R_{LIM} = 33\text{ k}\Omega$	-	1.3	1.7	mA
		EN = $V_{I(VIN)}$; $R_{LIM} = 16\text{ k}\Omega$	-	1.35	1.7	mA
$I_{S(OFF)}$	VBUS OFF-State leakage current	$V_{I(VIN)} = 5.0\text{ V}$; $V_{I(VBUS)} = 0\text{ V}$; EN = LOW	^[2] -5	-0.1	-	μA
		$V_{I(VBUS)} = 5.0\text{ V}$; $V_{I(VIN)} = 0\text{ V}$; EN = LOW	^[2] -2	-0.1	-	μA
		$V_{I(VBUS)} = 20\text{ V}$; $V_{I(VIN)} = 0\text{ V}$; EN = LOW	^[2] -2	-0.1	-	μA
$I_{S(ON)}$	FET-B leakage current in RCP	$V_{I(VIN)} = 5\text{ V}$; $V_{I(VBUS)} = 20\text{ V}$; EN = 5 V	^[2] ^[3] -2	-0.1	-	μA
R_{pd}	Pull-down resistance	EN; FO; $V_{I(VIN)} = 5\text{ V}$	-	1	-	M Ω
V_{UVLO}	under voltage lockout voltage	VIN pin	-	3.6	3.8	V
$V_{hys(UVLO)}$	under voltage lockout hysteresis voltage		-	100	-	mV
V_{OL}	LOW-level output voltage	FLT; $I_O = 4\text{ mA}$	-	-	0.3	V
$C_{I(EN)}$	EN pin		-	3	-	pF
$C_{I(FO)}$	FO pin		-	4	-	pF

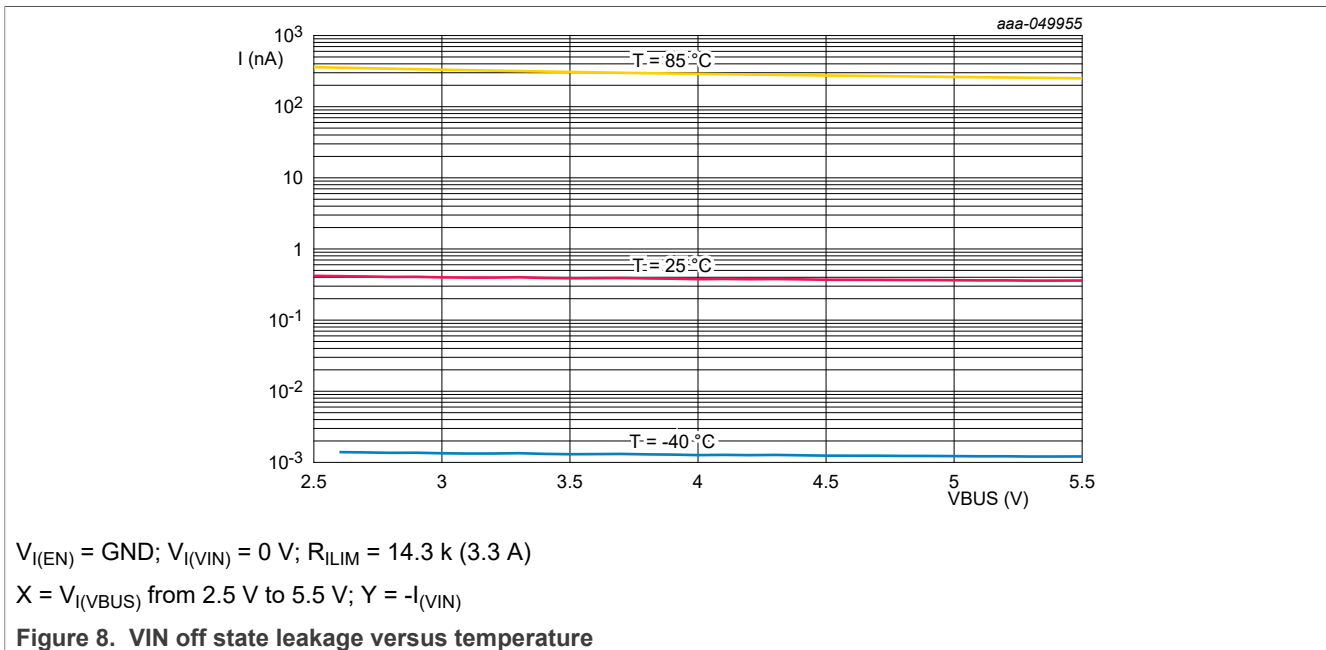
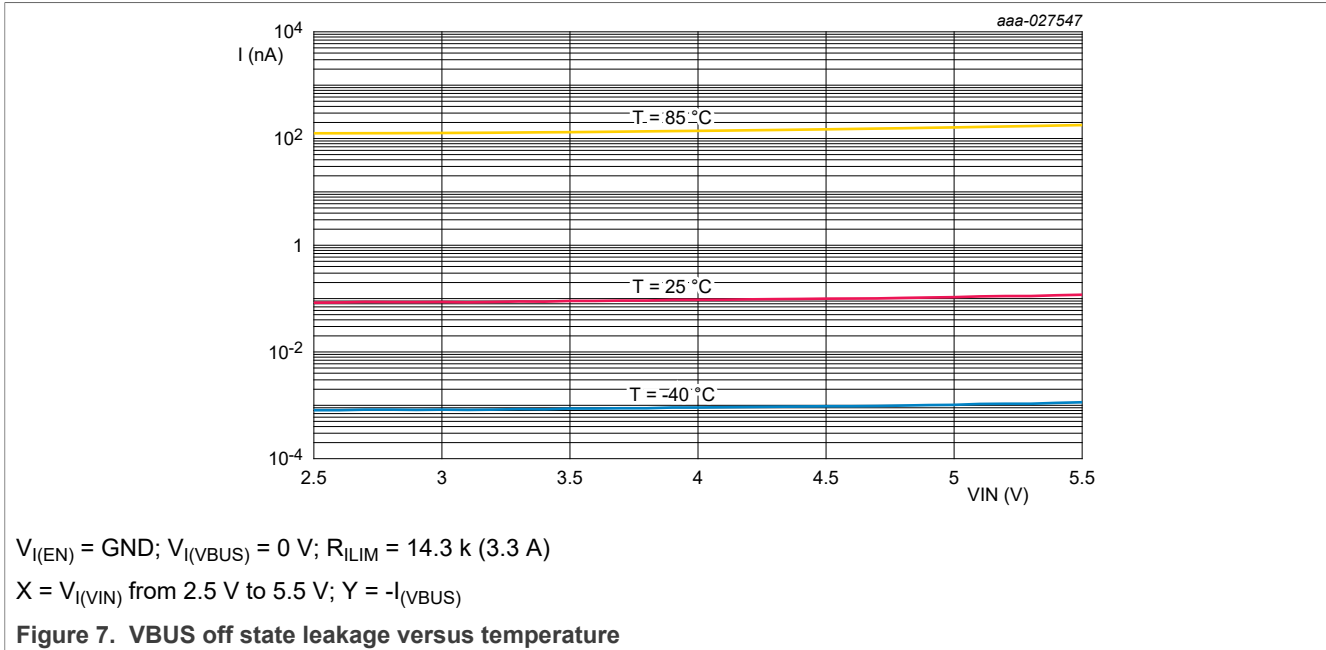
[1] Typical values are measured at $T_j = 25\text{ }^\circ\text{C}$.

[2] Currents are defined with respect to conventional current flow into the respective terminal. Negative value means the current flows out of the respective terminal of the chip.

[3] Guaranteed by design

13.1 Graphs





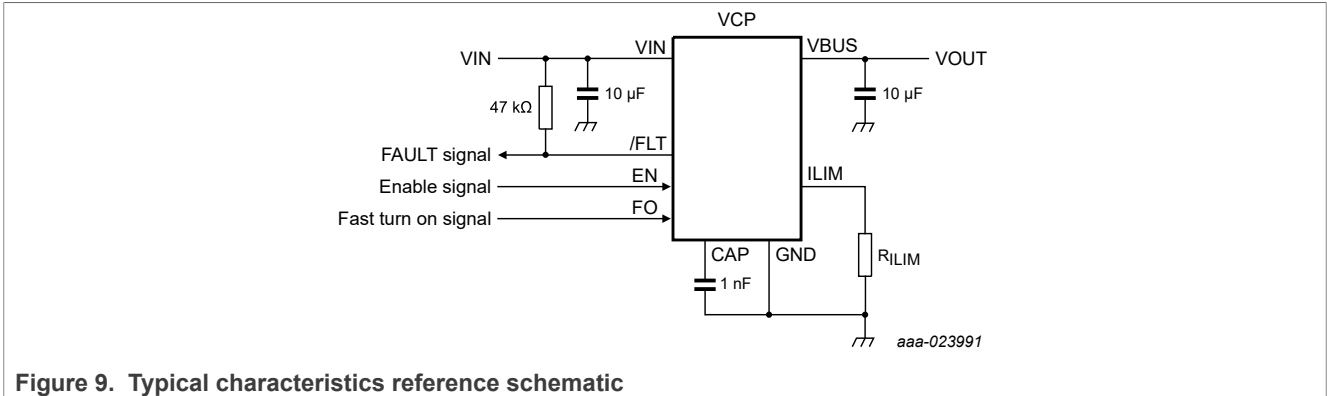


Figure 9. Typical characteristics reference schematic

13.2 Thermal shutdown

Table 10. Thermal shutdown

$V_{I(VIN)} = V_{I(EN)}$, $R_{FAULT} = 10\text{ k}\Omega$ unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(ots)}$	over temperature shutdown threshold temperature	$V_{I(VIN)} = 4.0\text{ V to }5.5\text{ V}$	-	140	-	°C
$T_{th(otp)hys}$	hysteresis of over temperature protection threshold temperature	$V_{I(VIN)} = 4.0\text{ V to }5.5\text{ V}$	-	25	-	°C

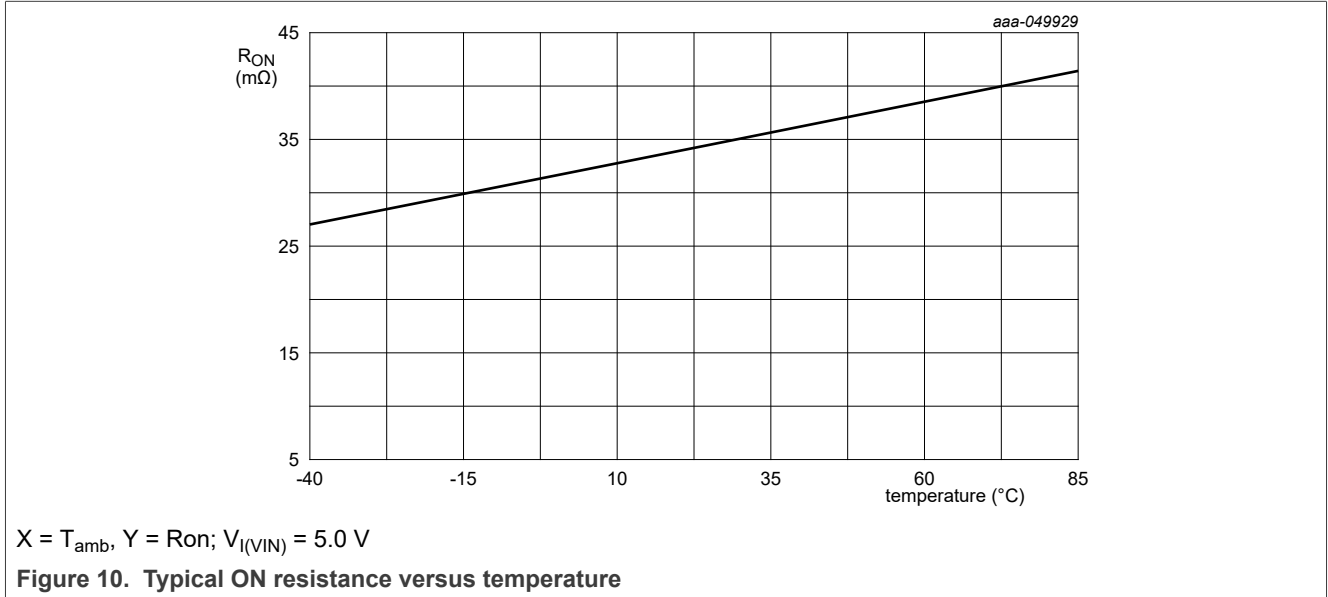
13.3 ON resistance

Table 11. ON resistance

$V_{I(VIN)} = V_{I(EN)}$, $R_{FAULT} = 10\text{ k}\Omega$ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See [Figure 9](#)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	ON resistance	$R_{FETA} + R_{FETB}$; $V_{I(VIN)} = 4.0\text{ to }5.5\text{ V}$; see Figure 10				
		$T_{amb} = 25\text{ °C}$	-	35	42	mΩ
		$T_{amb} = -40\text{ °C to }+85\text{ °C}$	-	-	49	mΩ

13.4 ON resistance graphs



13.5 Current limit

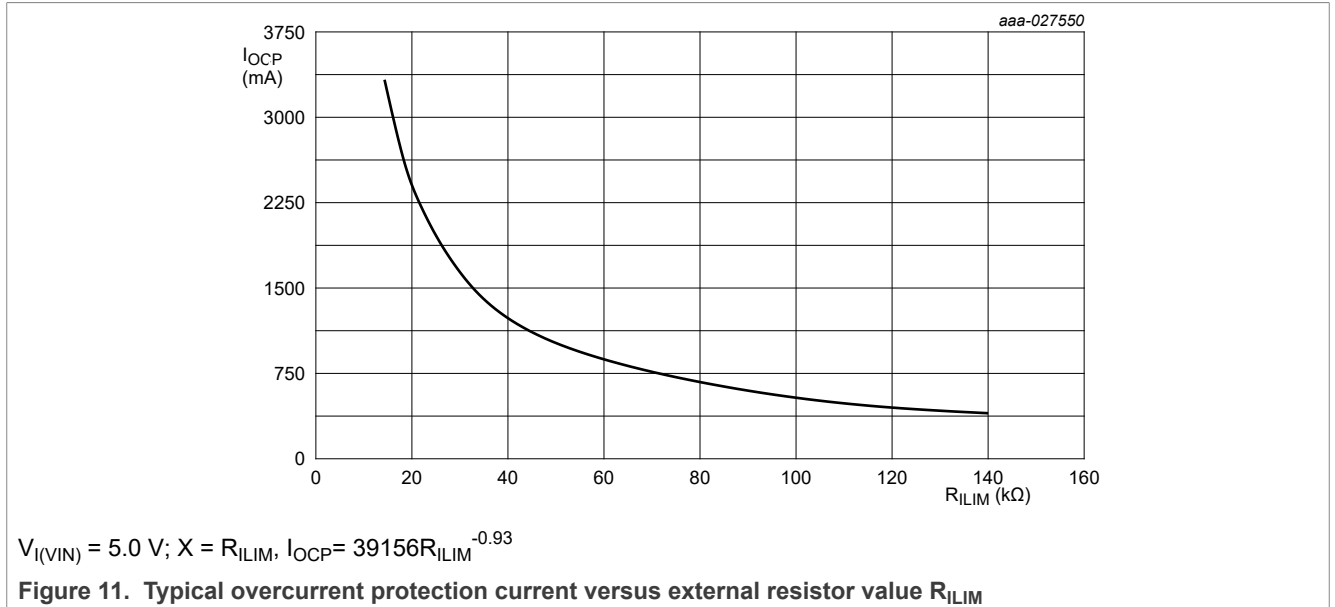
Table 12. Current limit

V_{I(VIN)} = V_{I(EN)}, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 9

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I _{OC} P	overcurrent protection current	V _{I(VIN)} = 4.0 to 5.5 V; T _{amb} = -40 °C to +85 °C; see Figure 11,				
		R _{LIM} = 140 kΩ	330	400	465	mA
		R _{LIM} = 97.6kΩ	480	550	625	mA
		R _{LIM} = 51 kΩ	915	1000	1107	mA
		R _{LIM} = 30 kΩ	1505	1640	1780	mA
		R _{LIM} = 22.1 kΩ	2024	2200	2398	mA
		R _{LIM} = 18.2kΩ	2450	2640	2820	mA
		R _{LIM} = 14.3 kΩ	3100	3300	3531	mA
	ILIM shorted to VIN	168	210	273	mA	

[1] 1% tolerance resistor is recommend for R_{LIM}

13.6 Current limit graphs



14 Dynamic characteristics

Table 13. Dynamic characteristics

At recommended operating conditions; $V_{I(VIN)} = V_{I(EN)}$, $R_{FAULT} = 10\text{ k}\Omega$ unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
t_{TLH}	LOW to HIGH output transition time	VBUS; $V_{I(VIN)} = 5.0\text{ V}$; $C_L = 10\text{ }\mu\text{F}$; $R_L = 100\text{ }\Omega$; see Figure 12 and Figure 13				
		$V_{I(FO)} = \text{GND}$	-	1.5	-	ms
		$V_{I(FO)} = 5.0\text{ V}$	-	50	100	μs
t_{THL}	HIGH to LOW output transition time	VOUT; $C_L = 10\text{ }\mu\text{F}$; $R_L = 100\text{ }\Omega$; see Figure 12 and Figure 13				
		$V_{I(VIN)} = 5.0\text{ V}$	-	2.2	-	ms
t_{en}	enable time	EN to VOUT; $C_L = 10\text{ }\mu\text{F}$; $R_L = 100\text{ }\Omega$; see Figure 14 and Figure 15				
		$V_{I(VIN)} = 5.0\text{ V}$; $V_{I(FO)} = \text{GND}$	-	0.75	-	ms
		$V_{I(VIN)} = 5.0\text{ V}$; $V_{I(FO)} = 5.0\text{ V}$	-	60	-	μs
t_{dis}	disable time	EN to VOUT; $V_{I(VIN)} = 5.0\text{ V}$; $C_L = 10\text{ }\mu\text{F}$; $R_L = 100\text{ }\Omega$; see Figure 16 and Figure 17	-	90	-	μs
$t_{on(RCP)}$	RCP recovery time	$V_{I(VIN)} = 5.0\text{ V}$; EN = HIGH; From VBUS drops below VIN to FET-B ON; $C_L = 10\text{ }\mu\text{F}$	-	15	50	μs
$t_{dis(RCP)}$	RCP turn off time	FET-B RCP turn OFF time	[2]	0.3	-	μs
t_{degl}	deglitch time	FLT in OCP; $V_{I(VIN)} = 5\text{ V}$; see Figure 20 to Figure 21	-	8	-	ms
$t_{short(OCP)}$	OCP short circuit protection response time	$V_{I(VIN)} = 5.0\text{ V}$; $C_{BUS} = 10\text{ }\mu\text{F}$; Measure current at VBUS side	-	5	-	μs

[1] Typical values are measured at $T_j = 25\text{ }^\circ\text{C}$.

[2] Guaranteed by design

14.1 Waveform and test circuits

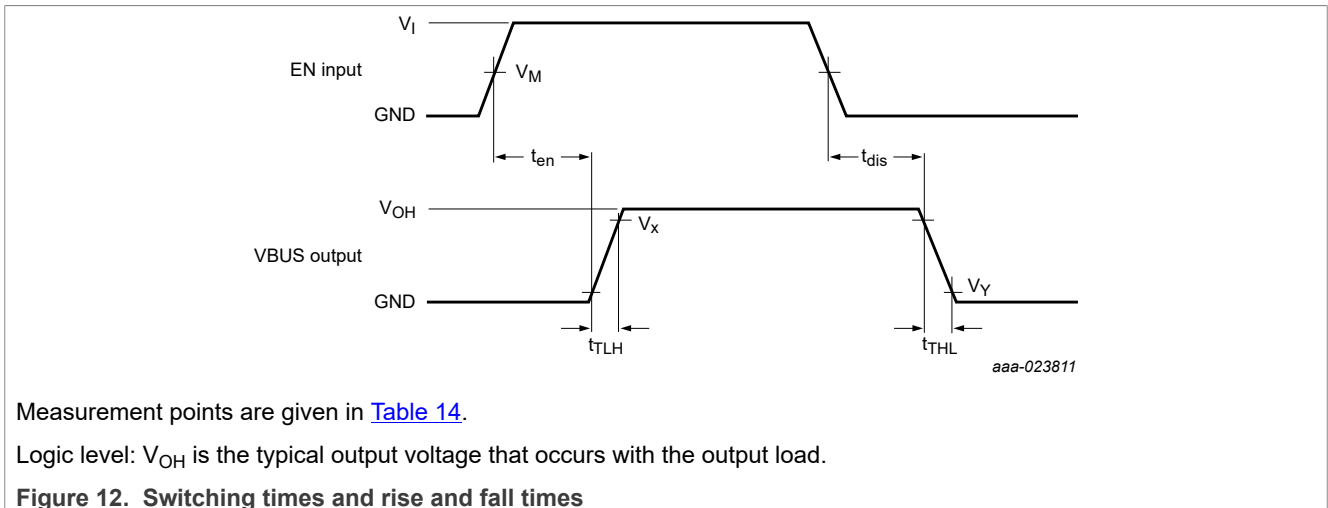
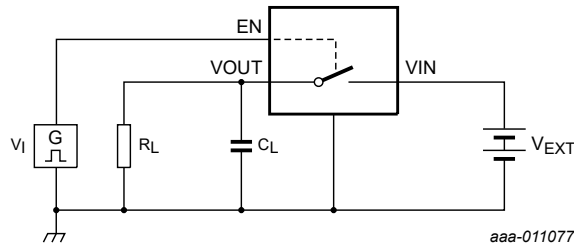


Table 14. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VIN)}$	V_M	V_X	V_Y
5.0 V	$0.5 \times V_{I(EN)}$	$0.9 \times V_{OH}$	$0.1 \times V_{OH}$



Test data is given in [Table 15](#).

Definitions test circuit:

R_L = Load resistance.

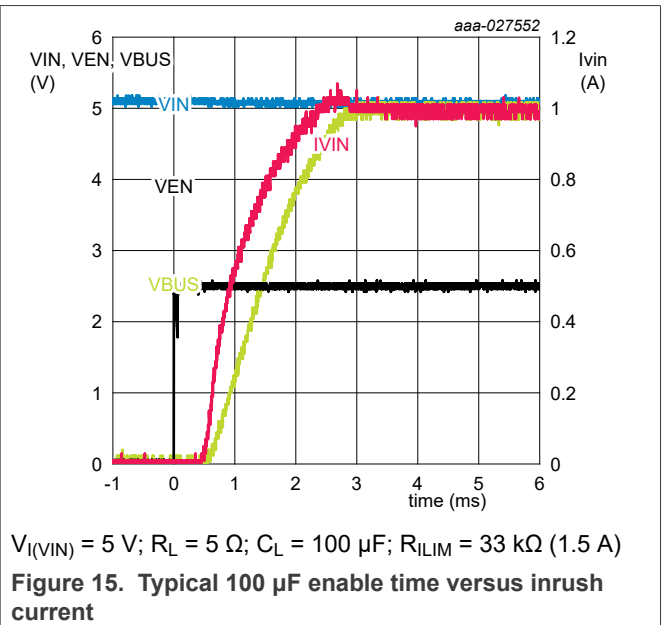
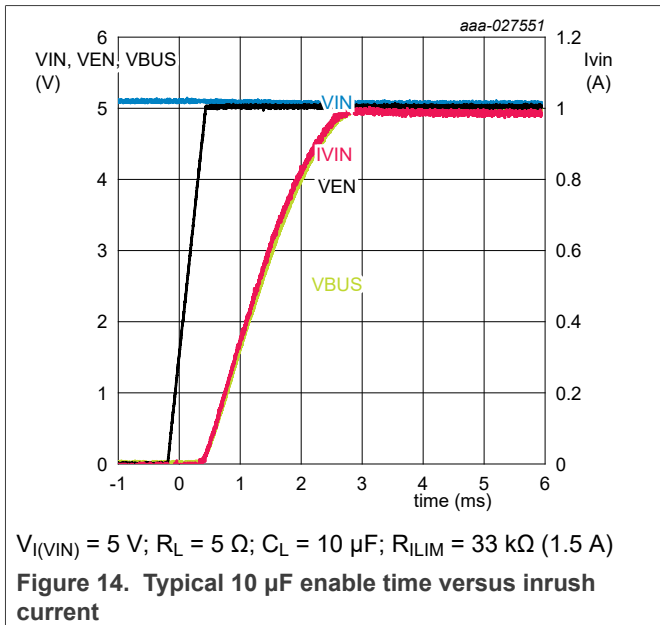
C_L = Load capacitance including jig and probe capacitance.

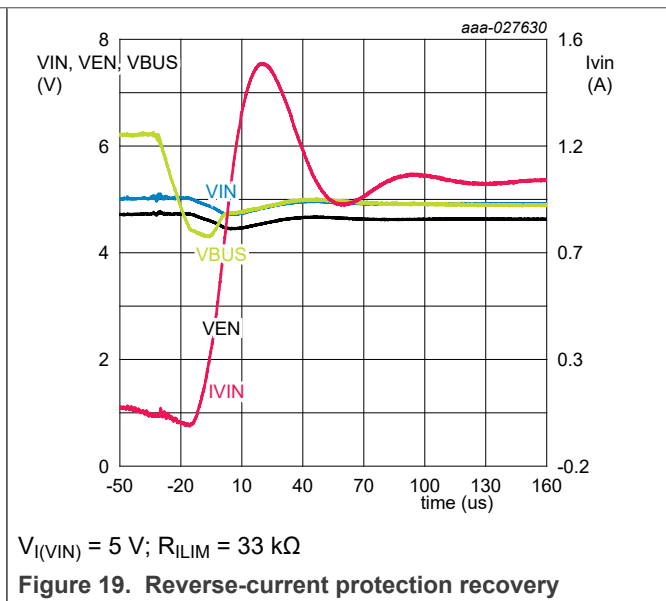
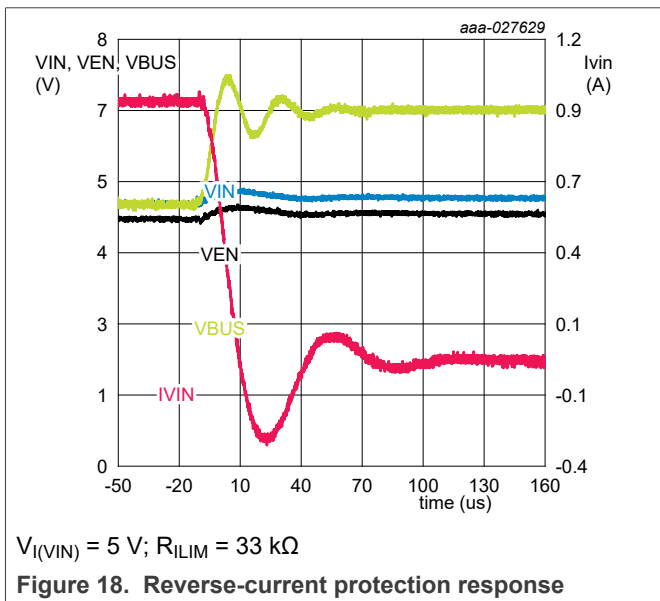
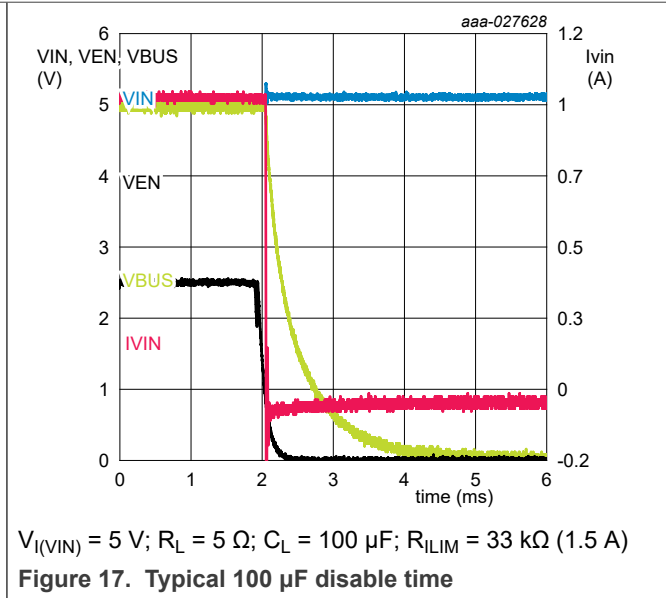
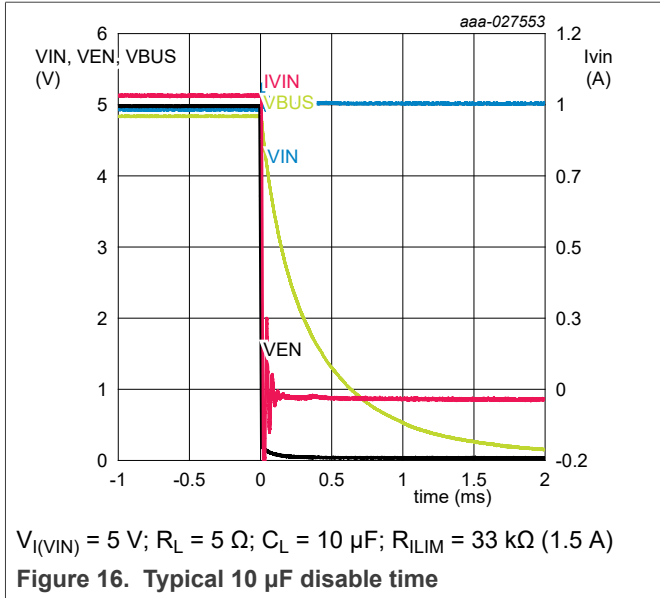
V_{EXT} = External voltage for measuring switching times.

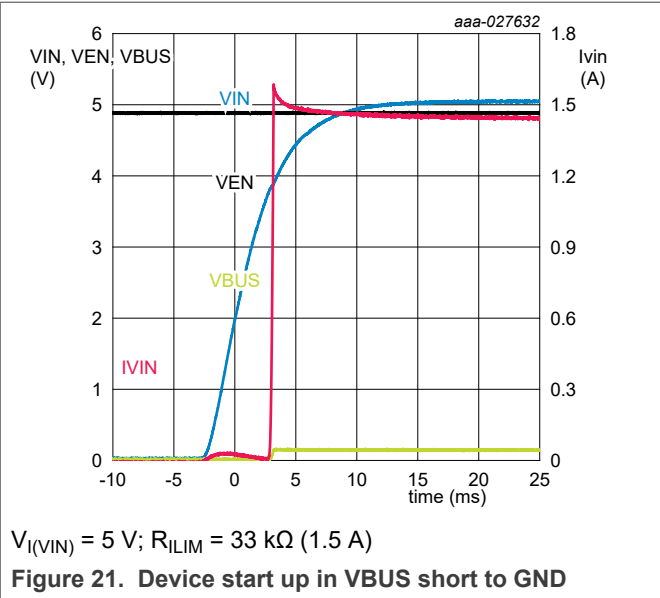
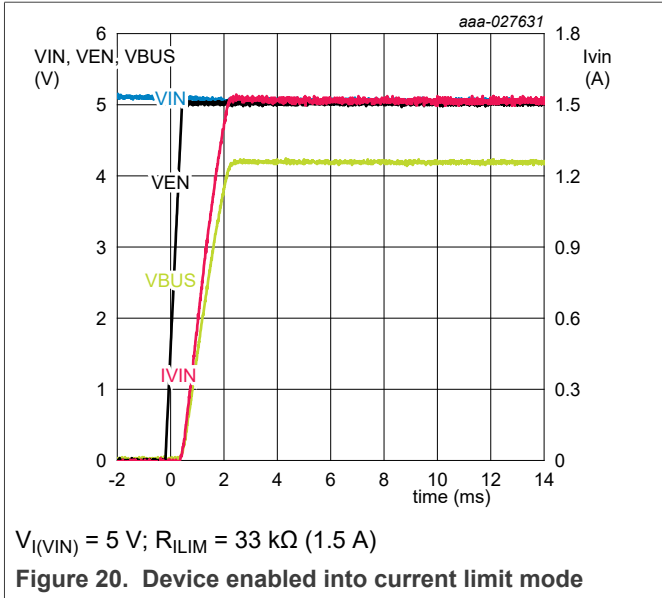
Figure 13. Test circuit for measuring switching times

Table 15. Test data

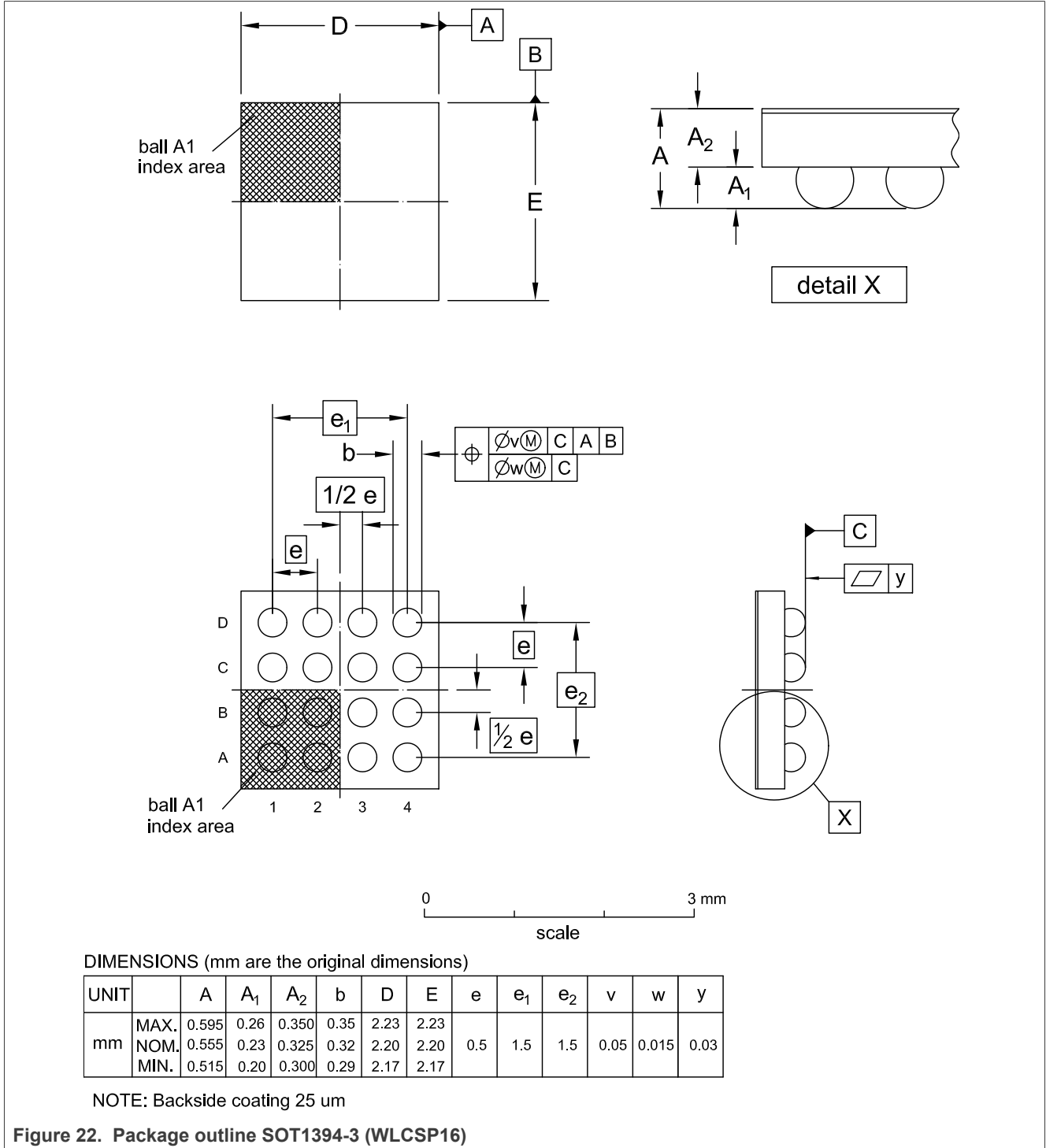
Supply voltage	EN Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_L
5.0 V	0 to $V_{I(VIN)}$	10 μF	100 Ω







15 Package outline



16 Abbreviations

Table 16. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
CDM	Charged Device Model
HBM	Human Body Model
USB	Universal Serial Bus

17 Revision history

Table 17. Revision history

Document ID	Release date	Description
NX5P3363_Q100 v.1.1	10 September 2024	• Changed Section 3
NX5P3363_Q100 v.1.0	31 May 2024	• Initial version

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Ordering information	4	Tab. 10.	Thermal shutdown	18
Tab. 2.	Ordering options	4	Tab. 11.	ON resistance	18
Tab. 3.	Marking	5	Tab. 12.	Current limit	19
Tab. 4.	Pin description	7	Tab. 13.	Dynamic characteristics	21
Tab. 5.	Function table	8	Tab. 14.	Measurement points	22
Tab. 6.	Limiting values	12	Tab. 15.	Test data	22
Tab. 7.	Recommended operating conditions	13	Tab. 16.	Abbreviations	26
Tab. 8.	Thermal characteristics	14	Tab. 17.	Revision history	27
Tab. 9.	Static characteristics	15			

Figures

Fig. 1.	Block diagram	6	Fig. 12.	Switching times and rise and fall times	21
Fig. 2.	Pin configuration for WLCSP16	7	Fig. 13.	Test circuit for measuring switching times	22
Fig. 3.	Ball mapping for WLCSP16	7	Fig. 14.	Typical 10 μ F enable time versus inrush current	22
Fig. 4.	Application diagram	11	Fig. 15.	Typical 100 μ F enable time versus inrush current	22
Fig. 5.	OFF state supply current versus temperature	16	Fig. 16.	Typical 10 μ F disable time	23
Fig. 6.	ON state supply current versus temperature	16	Fig. 17.	Typical 100 μ F disable time	23
Fig. 7.	VBUS off state leakage versus temperature	17	Fig. 18.	Reverse-current protection response	23
Fig. 8.	VIN off state leakage versus temperature	17	Fig. 19.	Reverse-current protection recovery	23
Fig. 9.	Typical characteristics reference schematic	18	Fig. 20.	Device enabled into current limit mode	24
Fig. 10.	Typical ON resistance versus temperature	19	Fig. 21.	Device start up in VBUS short to GND	24
Fig. 11.	Typical overcurrent protection current versus external resistor value RILIM	20	Fig. 22.	Package outline SOT1394-3 (WLCSP16)	25

Contents

1	General description	1
2	Features and benefits	2
3	Applications	3
4	Ordering information	4
4.1	Ordering options	4
5	Marking	5
6	Functional diagram	6
7	Pinning information	7
7.1	Pinning	7
7.2	Pin description	7
8	Functional description	8
8.1	EN input	8
8.2	Fast recovery RCP	8
8.3	VBUS hot plug-in RCP	8
8.4	Fast Turn ON	9
8.5	Undervoltage lockout	9
8.6	ILIM	9
8.7	Main power FET overcurrent protection (OCP)	9
8.7.1	Overcurrent at startup	9
8.7.2	Overcurrent when enabled	10
8.7.3	Short circuit when enabled	10
8.8	FLT output	10
8.9	Overtemperature protection	10
9	Application diagram	11
10	Limiting values	12
11	Recommended operating conditions	13
12	Thermal characteristics	14
13	Static characteristics	15
13.1	Graphs	16
13.2	Thermal shutdown	18
13.3	ON resistance	18
13.4	ON resistance graphs	19
13.5	Current limit	19
13.6	Current limit graphs	20
14	Dynamic characteristics	21
14.1	Waveform and test circuits	21
15	Package outline	25
16	Abbreviations	26
17	Revision history	27
	Legal information	28

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.