4.5 V to 24 V, 8 A Adaptive Constant On Time (COT) Synchronous Buck Regulator

Description

The NX9548 is a synchronous buck switching regulator with 21 mΩ internal N-channel MOSFETs, primarily intended for portable (mobile) applications. The NX9548 operates from 4.5 V to 24 V, and the output voltage range is from 0.75 V to 5 V, with output currents as high as 8 A. It can be selected to operate in synchronous mode, or non-synchronous (diode emulation or PSM) mode at light loads, to improve efficiency.

Adaptive constant on time (COT) control provides extremely fast transient response to line and load steps, while at the same time providing near-constant switching frequency over a wide input voltage range. The frequency is also externally adjustable.

The NX9548 features overcurrent protection (OCP), feedback under-voltage lockout (FB UVLO), and overvoltage protection (OVP). It also includes an integrated bootstrap Schottky diode, and provides low-voltage (5 V) gate-drive capability. In addition it provides a Power Good indicator and has adaptive dead time.

Features

- Adaptive COT Control
- Adjustable, Constant Switching Frequency up to 1 MHz
- Extremely Low-RDSON N-MOSFETs
- Bus Voltage 4.5 V to 24 V
- Selectable Diode Emulation Mode (PSM Mode)
- Current Limit, UVLO, OVP
- Gate Resistor Provision for EMI Reduction
- -40°C to +85°C Ambient Temperature
- -40°C to +150°C Junction Temperature
- RoHS Compliant
- 5×5 mm Very Thin Profile QFN (VQFN) Package

Applications

- Ultramobile/Notebook PCs
- Tablets/Slates
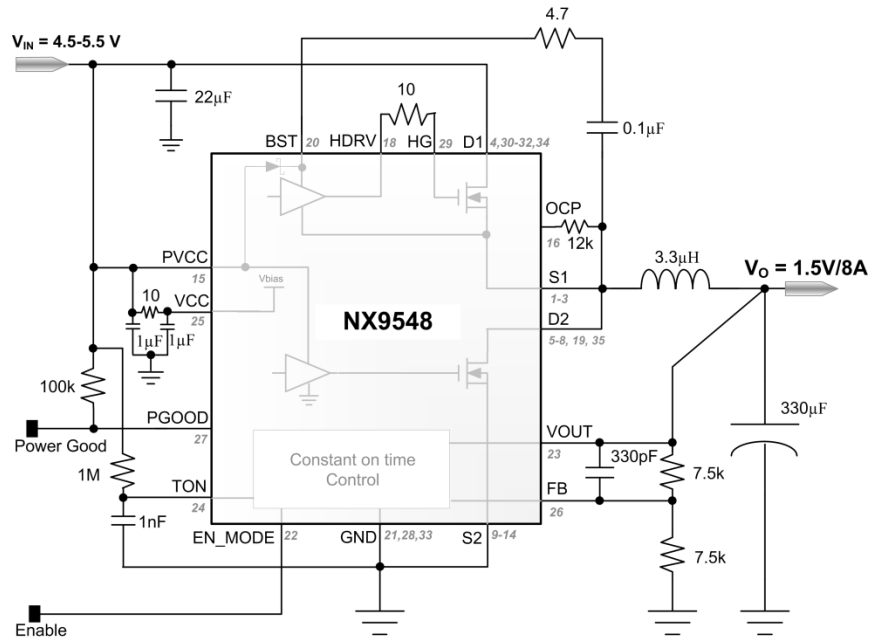- Hand-held Portable Instruments
- ADSL Modem

Typical Application Diagram

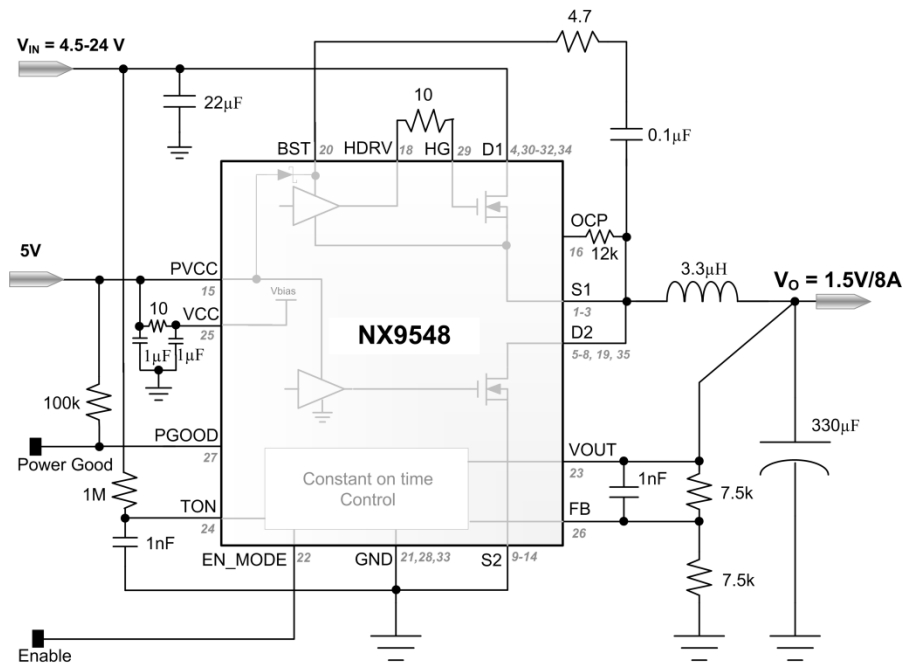Figure 1 · **Typical Application Diagram for Low-Input Voltages**

Figure 2 · **Typical Application Diagram for Wide Input Range**
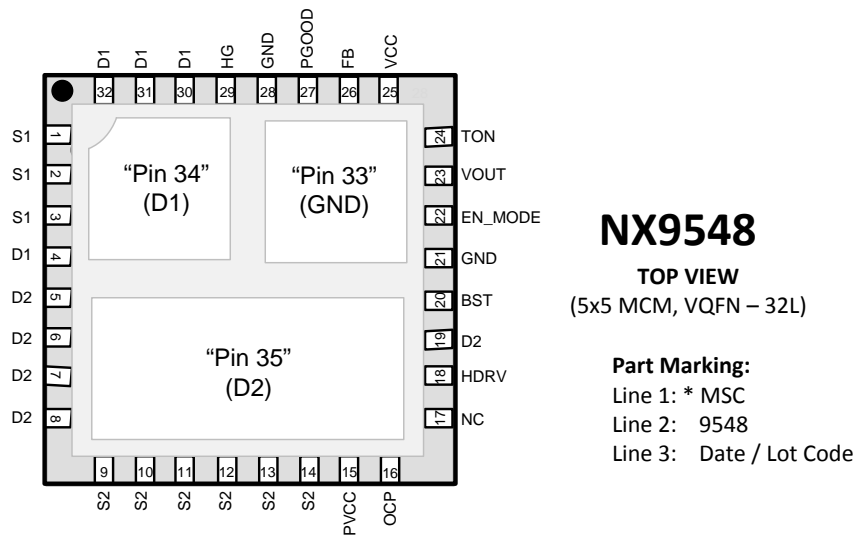
Pin Configuration and Pinout

NX9548

TOP VIEW
(5x5 MCM, VQFN – 32L)

Part Marking:
Line 1: * MSC
Line 2: 9548
Line 3: Date / Lot Code

Figure 3 · **Pinout**

Note: All Pins and PADs are at the bottom of the chip. * is the pin one dot.

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS Compliant Pb-free	VQFN-32L (MCM) 5 × 5 mm	NX9548ILQ	Bulk
			NX9548ILQ-TR	Tape and Reel

Pin Description

| Pin Number	Pin Designator	Description
1, 2, 3	S1	Source of the high side N-channel MOSFET. These pins must be connected directly to the Drain of low side MOSFET via a PCB plane connection.
4, 30, 31, 32, 34	D1	Drain of high side MOSFET.
5, 6, 7, 8, 19, 35	D2	Drain of low side MOSFET and the controller pin out SW.
9, 10, 11, 12, 13, 14	S2	Source of low side MOSFET and needs to be directly connected to power ground via multiple vias.
15	PVCC	This pin provides the voltage supply to the lower MOSFET drivers. Place a high frequency decoupling capacitor 1 µF/X5R from this pin to GND.
16	OCP	This pin is the input of the over current protection (OCP) comparator, and it should be connected to the Drain of the low side MOSFET via a resistor. An internal current source is supplied from this pin to an external resistor which sets the OCP voltage across the RDSON of the low side MOSFET. The current limit level is this voltage divided by the R_{DSON}. Once this threshold is reached the chip shuts off.
17	NC	Not connected internally.
18	HDRV	High side gate driver output which needs to be connected to high side MOSFET gate HG pin. A small value resistor may be placed in series to slow down the high side MOSFET, reducing the ringing on SW node.
20	BST	This pin supplies voltage to high side FET driver. A high frequency 0.1 µF ceramic capacitor should be placed as close as possible and connected pin 19. A 4.7 Ω resistor is recommended in series with this capacitor.
21, 28, 33	GND	Ground for the IC and the Buck topology.
22	EN_MODE	Switching converter enable input. Connect to VCC for PSM/Non synchronous mode, connect to an external resistor divider equaling 70% of VCC for ultrasonic mode, and connect to GND for shutdown mode, floating or connected to 2 V for synchronous mode.
23	VOUT	This pin is directly connected to the output of the switching regulator and senses the VOUT voltage. An internal MOSFET discharges the output during turn off.
24	TON	VIN sensing input. A resistor connected from this pin to VIN will program the frequency. A 1 nF capacitor from this pin to GND is recommended to ensure the proper operation.
25	VCC	This pin supplies the internal 5 V bias circuit. A 1 µF/X5R ceramic capacitor is placed as close as possible to this pin and ground pin.
26	FB	This pin is the error amplifier's inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage from 0.75 V to 5 V.
27	PGOOD	PGOOD indicator for switching regulator. It requires a pull up resistor to VCC or lower voltage. When FB pin reaches 90% of the reference voltage PGOOD transitions from LO to HI state.
29	HG	The Gate of the high side switching MOSFET. Can connect typically 10 Ω in series to improve EMI, at the expense of about 2-3 % in efficiency

Block Diagram
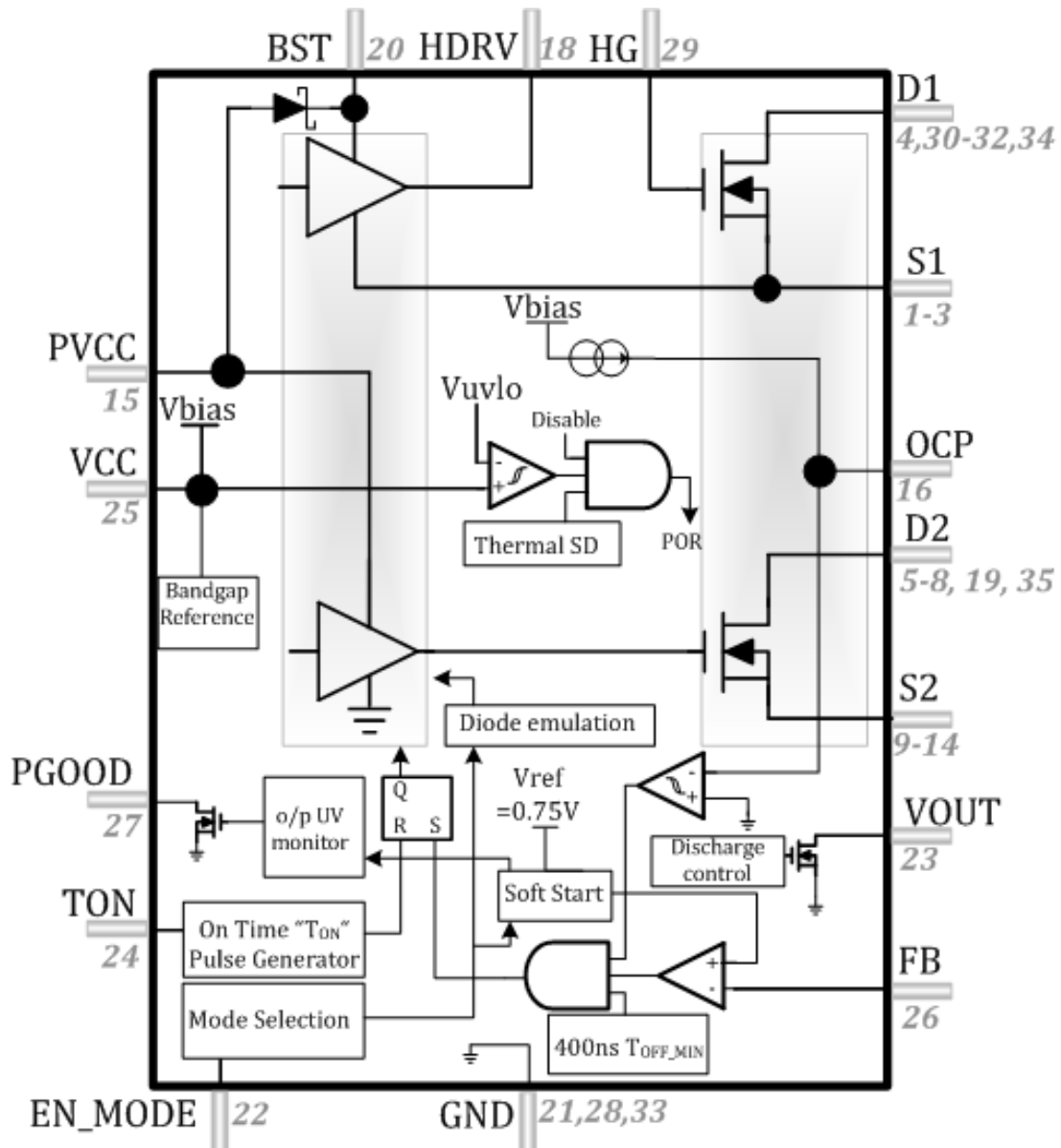
Figure 4 · **Simplified Block Diagram of NX9548**

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

Parameter	Min	Max	Units
VCC, PVCC to GND	-0.3	6.5	V
BST and HDRV to SW (S1-D2 node)	-0.3	6.5	V
TON to GND	-0.3	28	V
D1 to S1 and D2 to S2	–	30	V
All other Pins to GND	-0.3	VCC+0.3	V
Output Current	–	9	A
Junction Temperature	-40	150	°C
Storage Temperature	-65	150	°C
Lead Soldering Temperature (40s, reflow)	–	260	°C

Note: Pin 33 is connected by copper plane on PCB to GND (Pins 21 and 28), Pin 34 is similarly connected to D1, and Pin 35 is similarly connected to D2.

Operating Ratings

–	Min	Max	Units
VIN	4.5	24	V
V_{OUT}	4.5	5.5	V
Ambient Temperature	-40	85	°C
Output Current	0	8	A

Note: Corresponding Maximum Junction Temperature of 150°C

Thermal Properties

Thermal Resistance	Type	Units
θ_{JA}	35	°C/W
θ_{JC}	29	°C/W
θ_{JL}	1.2	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC). For θ_{JL}, the lead temperature is measured at the center of PAD2 at the bottom of the package. For θ_{JC}, the case temperature is measured at the center point of PAD2 on top of the package on the plastic with infinitely large heat sink on top of the device.

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperature of -40°C ≤ T_A ≤ 85°C except where otherwise noted, with the following test conditions: VCC = PVCC = 5 V, 4.5 V < V_{IN} < 24 V. Typical parameter refers to T_J=25°C, V_{IN}=12 V.

Symbol	Parameter	Test Condition	Min	Type	Max	Units
V_{IN}						
$I_{D1} + I_{TON}$	Shutdown current	V_{EN_MODE} = GND	–	20	–	nA
VCC, PVCC Supply						
I_{VCC}	Quiescent Current (switching no-load)	V_{FB} = 0.85 V, V_{EN_MODE} = 5 V	–	1.5	–	mA
$I_{VCC} + I_{PVCC}$	Shutdown current	V_{EN_MODE} = V_{SW} = V_{HG} = GND Note 1	–	45	–	µA
VCC UVLO						
$V_{CC\_UVLO\_HI}$	Undervoltage lockout threshold (rising)	–	3.87	4.1	4.5	V
$V_{CC\_UVLO\_LO}$	Undervoltage lockout threshold (falling)	–	3.67	3.9	4.3	V
ON and OFF Time						
I_{TON_OP}	T_{ON} operating current	V_{IN} = 15 V, R_{TON} = 1 MΩ	–	17	25	µA
T_{ON}	On-time	V_{IN} = 9 V, R_{TON} = 1 MΩ, V_{OUT} = 0.75 V	312	456	620	ns
T_{OFF_MIN}	Min off-time	–	380	496	700	ns
FB Voltage						
V_{REF}	Feedback voltage	–	0.739	0.75	0.761	V
I_{OFFSET}	Feedback pin bias current (into pin)	–	–	75	–	nA
–	Line regulation	VCC from 4.5 V to 5.5 V, V_{IN} = 12 V, Note 1	–	0.1	–	%
		VIN from 4.5 V to 24 V, VCC = 5 V, Note 1	–	0.3	–	
–	Load regulation	0 < I_{LOAD} < 8A, V_{IN} = 12 V, V_{OUT} = 1 V, V_{EN_MODE} = 2.5 V, Note 1.	–	0.07	–	%/A
Output Voltage						
V_{OUT}	Output voltage range	V_{IN} = 10.5 V	0.75	–	5	V
R_{VOUT_DIS}	Output voltage discharge resistance	V_{EN_MODE} = GND	–	30	–	Ω
T_{SS}	Soft-start time	–	–	1.5	–	ms
PGOOD						
$V_{FB\_GOOD\_HI}$	Power Good threshold (rising voltage on FB pin)	–	–	90	–	%V_{REF}
T_{PGOOD_DELAY}	Power Good deglitch time after Soft-start completed	Note 1	–	1.6	–	ms
T_{PGOOD_SPEED}	Propagation delay of Power Good signal	Note 1	–	2	–	µs
V_{PGOOD_HYS}	Power Good hysteresis	–	–	5	–	%
R_{PGOOD_LO}	Power Good low impedance	–	–	13	–	Ω
I_{PGOOD}	Power Good leakage current	V_{FB} > 0.9 ×V_{REF}	–	1	–	µA

Symbol	Parameter	Test Condition	Min	Type	Max	Units
EN_MODE Threshold and Bias Current						
$V_{EN\_MODE\_SKIP}$	EN_MODE pin threshold for PSM	–	81	–	100	%VCC
$V_{EN\_MODE\_US}$	EN_MODE pin threshold for ultrasonic mode	–	61	–	79	%VCC
V_{EN_SYNCH}	EN_MODE pin voltage to enable in synchronous mode (or leave pin floating)	–	2	0.3	59% VCC	V
V_{EN_SD}	EN_MODE pin voltage to disable switching	–	0	–	0.8	V
$I_{EN\_MODE\_HI}$	EN_MODE pin bias current, held high	V_{EN_MODE} = VCC	–	5	–	µA
$I_{EN\_MODE\_LO}$	EN_MODE pin bias current, held low	V_{EN_MODE} = GND	–	-5	–	µA
SW Zero Cross Comparator						
V_{ZERO}	SW node zero cross comparator offset voltage	–	–	5	–	mV
Current Limit						
I_{CLIM}	OCP pin current (out of pin)	–	19	24	30	µA
Over Temperature						
T_{SD}	Over-temperature shutdown threshold (T_J)	Note 1	138	152	165	°C
T_{SD_HYS}	Over-temperature shutdown threshold hysteresis (T_J)	Note 1	–	26	–	°C
Under Voltage						
V_{FB_UVLO}	V_{FB} Undervoltage lockout threshold	T_A = 25°C	–	70	75	%V_{REF}
Over Voltage						
V_{FB_OVP}	V_{FB} Overvoltage trip threshold	T_A = 25°C	114	125	–	%V_{REF}
Internal Schottky Diode						
V_{BST_DIODE}	Internal bootstrap diode forward drop	I_{BST_DIODE} = 50mA	–	660	–	mV
-	Reverse leakage current	T_A = 25°C, $V_{BST} - V_{PVCC}$ = 22 V	–	20	–	µA
Output Stage						
R_{DS_HI}	High-side FET R_{DS}	I_{SW} = -2 A	–	23	35	mΩ
R_{DS_LO}	Low-side FET R_{DS}	I_{SW} = -2 A	–	21	33	mΩ

Note: 1. This parameter is guaranteed by design but not tested in production (GBNT).

Typical Performance Curves

Step Response
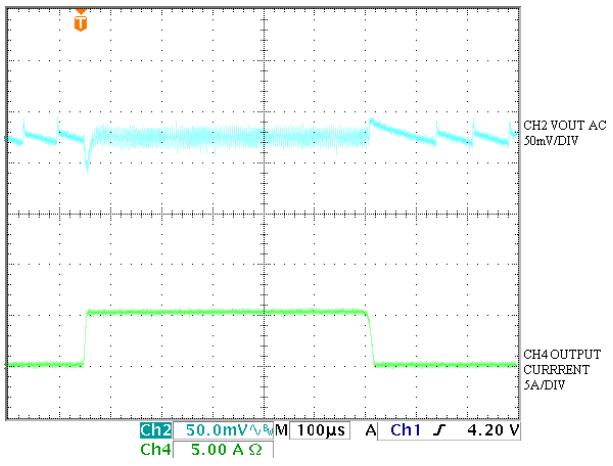
Figure 5 · **Step response in PSM mode when** V_{IN} = 5 V
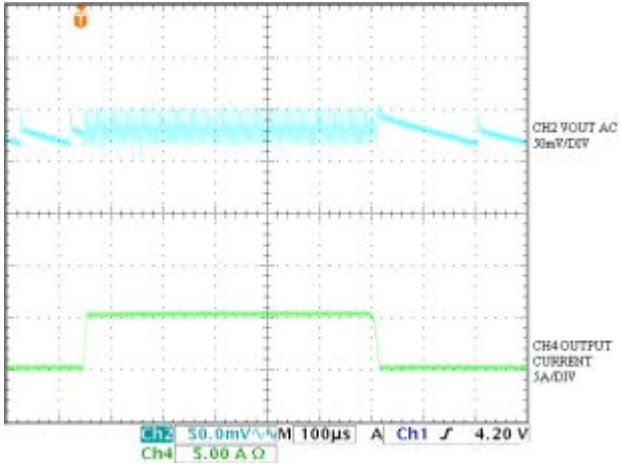
Figure 6 · **Step response in PSM mode when** V_{IN} = 20 V

Start-up
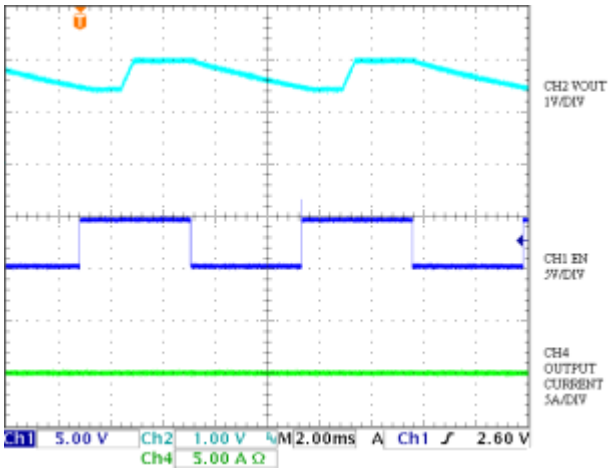
Figure 7 · **Start-up and Shut down, No Load**
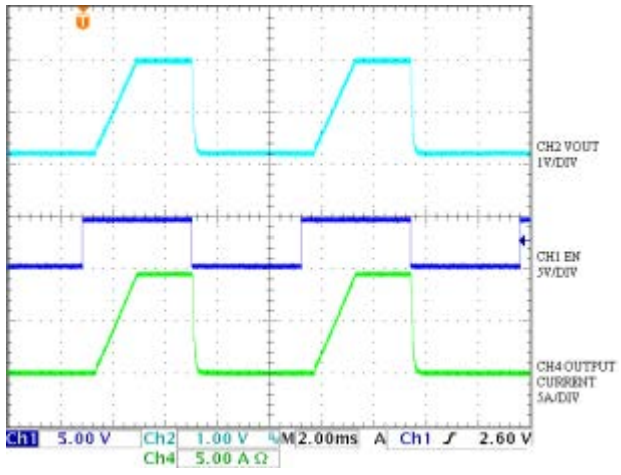

Figure 8 · **Start-up when 12 V bus is present and 5 V is started up**
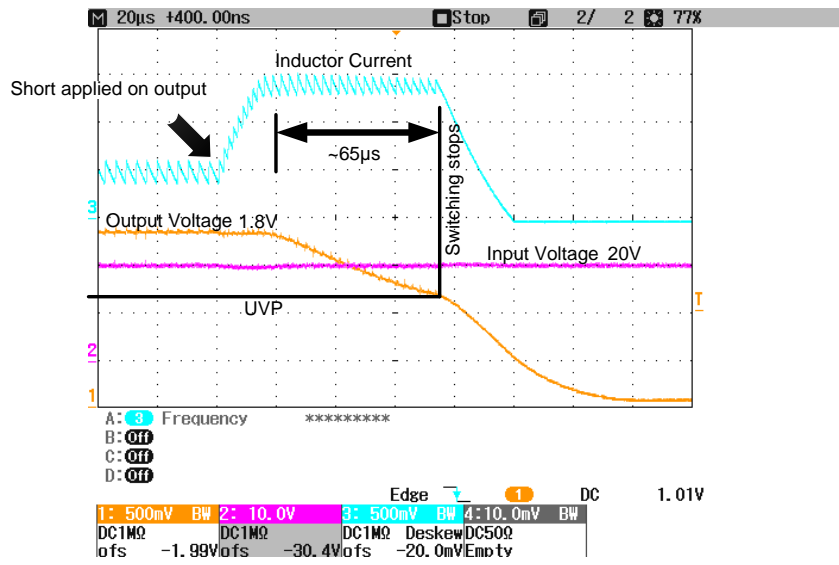
Short Circuit

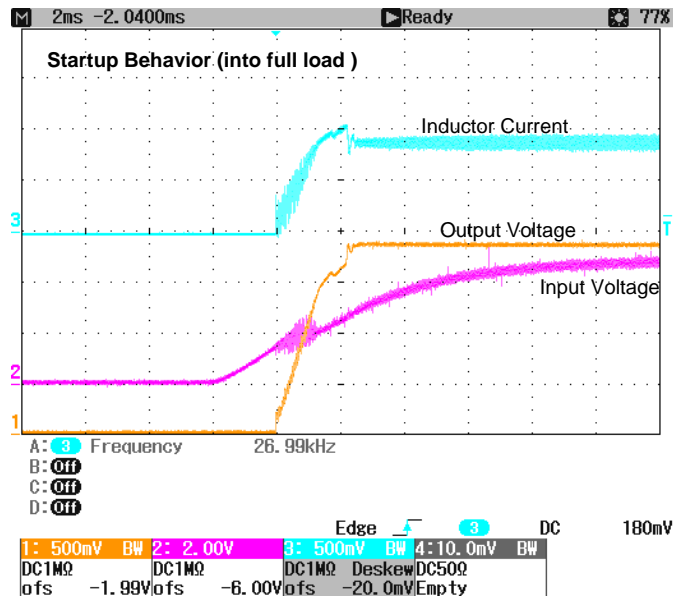Figure 9 · **Behavior under short circuit**

Start-Up into Full Load
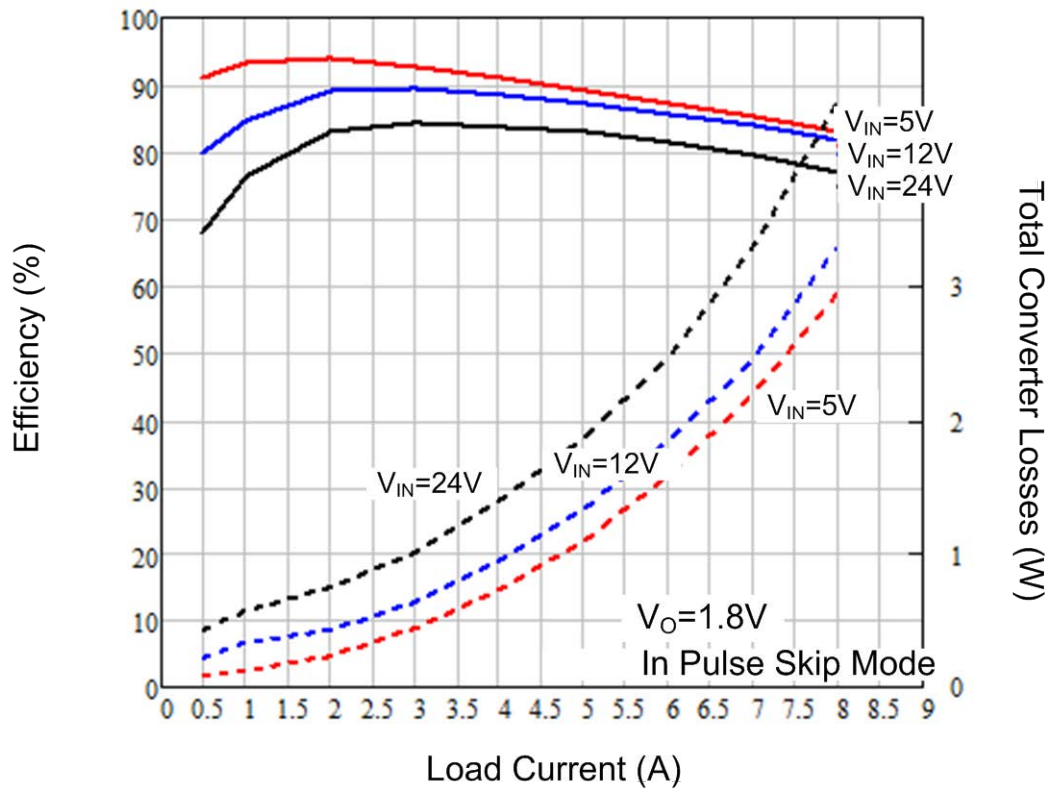

Figure 10 · **Start-up into full load**

Efficiency and Converter Losses

Figure 11 · **Efficiency and Converter Losses in PSM Mode**
V$_{OUT}$ = 1.8 V, F$_s$ = 300 kHz

Efficiency

Efficiency and Losses / VIN = 12 V, Fs = 600 kHz
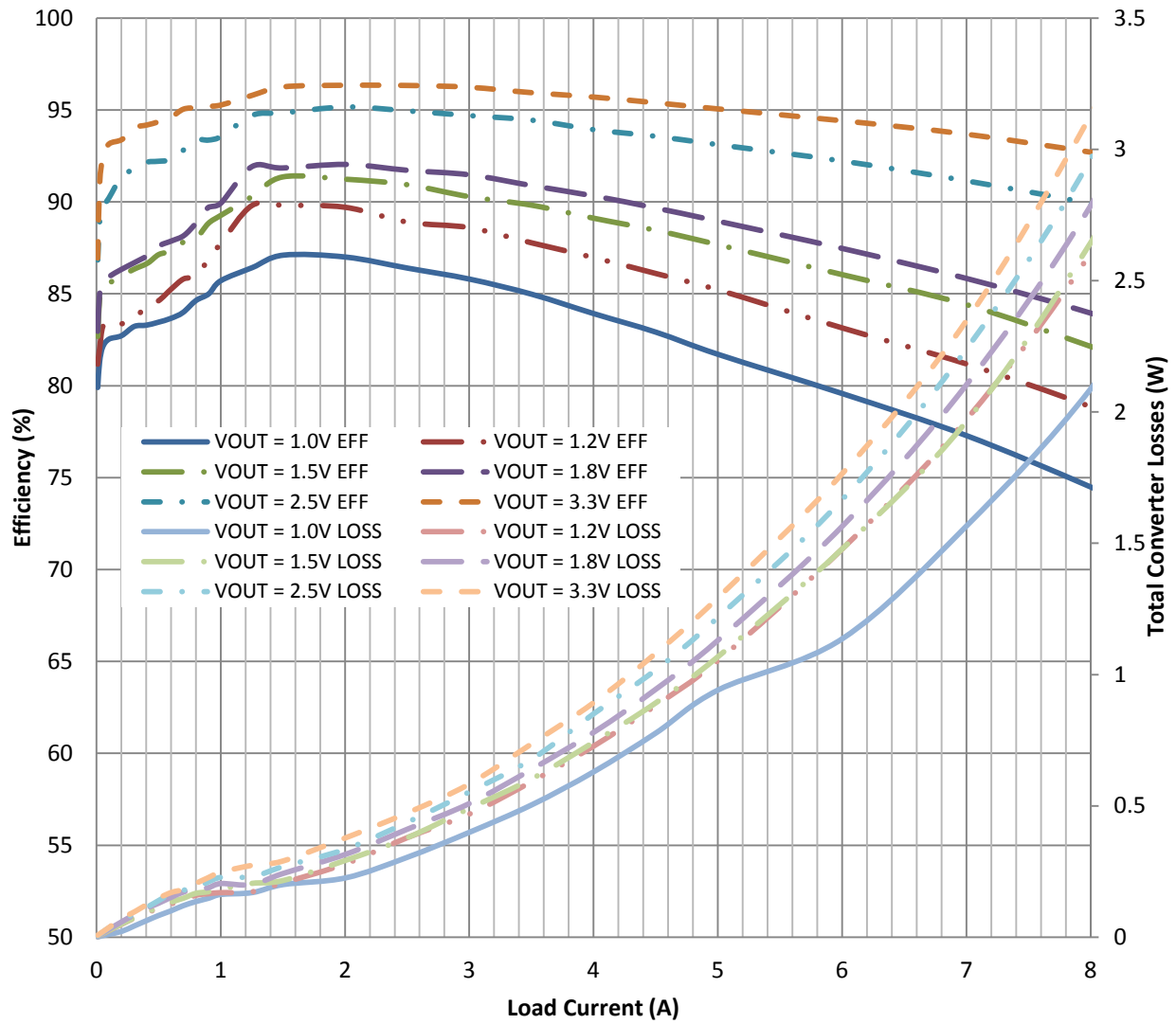
Output Voltage	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
Inductor Value	1.0 µH	1.5 µH	1.5 µH	2.2 µH	3.3 µH	3.3 µH	

Figure 12 · **Efficiency in PSM Mode with 12 V input @ 600 kHz switching frequency**

Microsemi

Efficiency

Efficiency / VIN = 12 V, Fs = 300 kHz
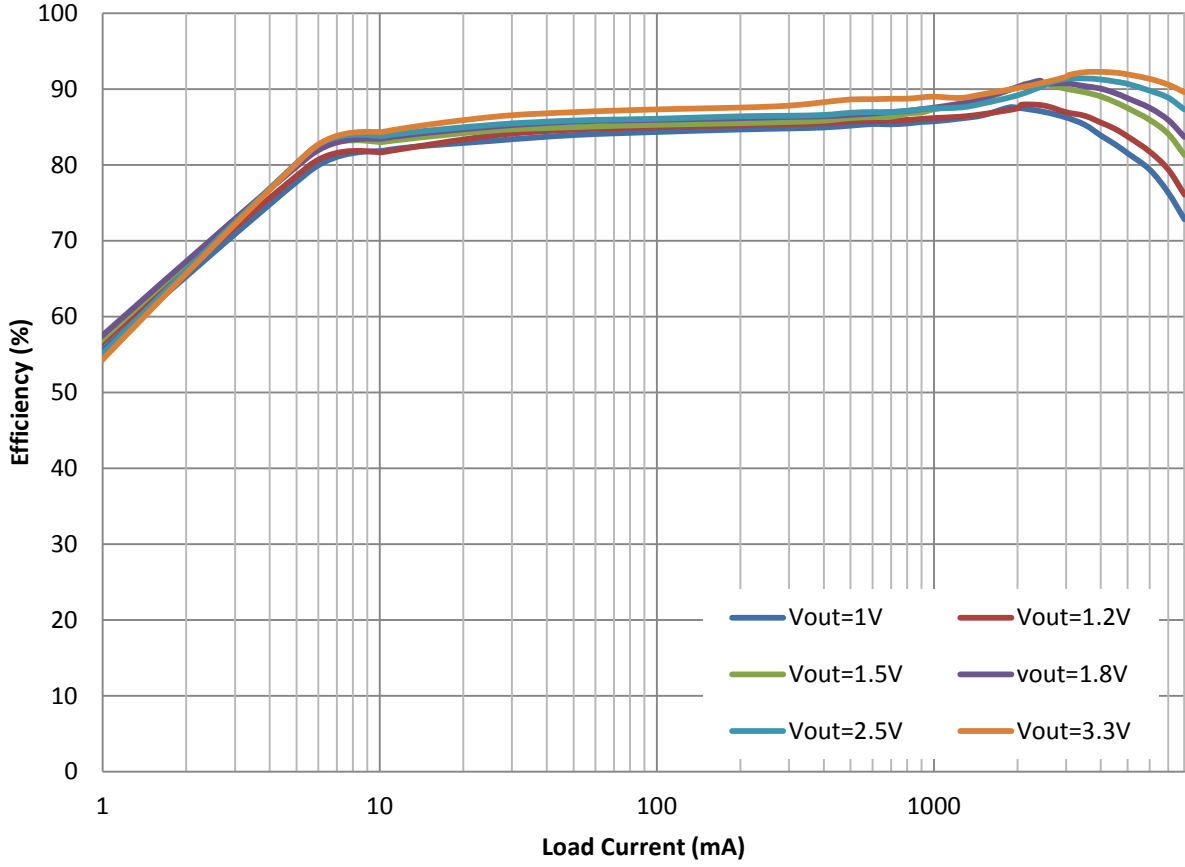
Figure 13 · **Efficiency in PSM Mode with 12 V input @ 300 kHz switching frequency**
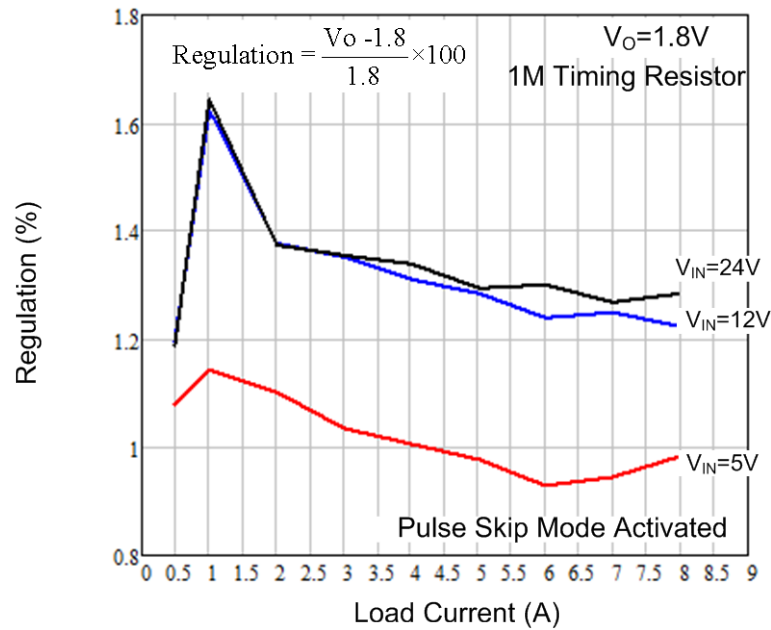
Figure 14 · **Regulation characteristics**
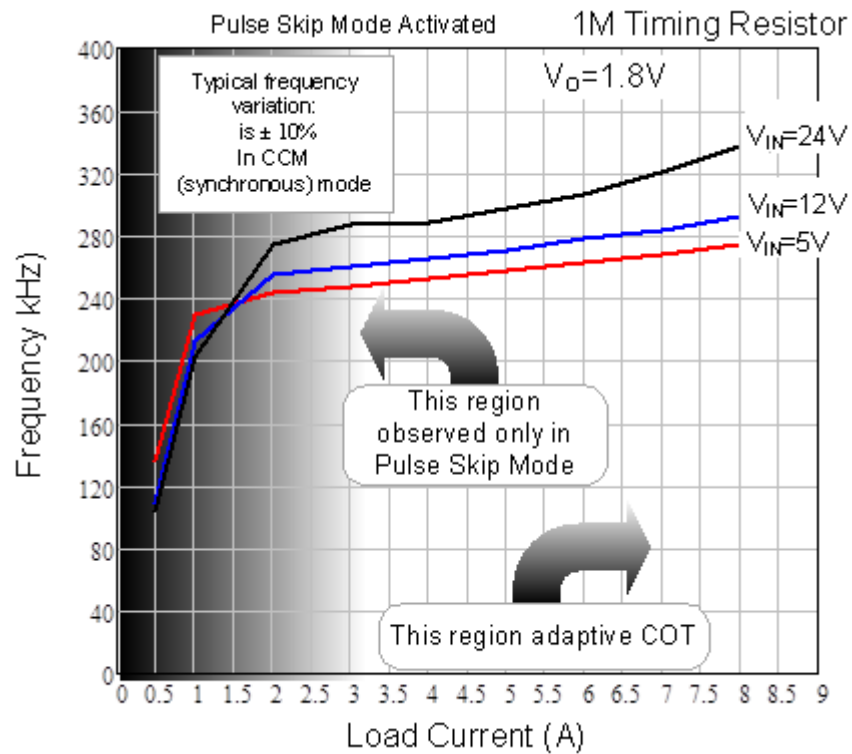
Figure 15 · **Frequency Stability**

Theory of Operation

Symbol Used In Application Information:

V_{IN}	Input voltage
V_{OUT}	Output voltage
I_{OUT}	Output current
ΔV_{RIPPLE}	Output voltage ripple
F_S	Working frequency
ΔI_{RIPPLE}	Inductor current ripple

Design Example

The following is typical application for NX9548, the schematic is Figure 1.

V_{IN} = 8 to 20 V

V_{OUT} = 1.5 V

F_S = 220 kHz

I_{OUT} = 7 A

ΔV_{RIPPLE} <=60 mV

ΔV_{DROOP}<=60 mV @ 3 A step

On-Time and Frequency Calculation

The constant on time control technique used in NX9548 delivers high efficiency, excellent transient dynamic response making it a good candidate for step-down notebook applications.

An internal one-shot timer turns on the high side driver with an on time which is proportional to the input supply VIN as well inversely proportional to the output voltage VOUT. During this time, the output inductor charges the output capacitor increasing the output voltage by the amount equal to the output ripple. Once the timer turns off, the HDRV turns off and causes the output voltage to decrease until reaching the internal FB voltage of 0.75 V on the PSM comparator. At this point, the comparator trips causing the cycle to repeat itself. A minimum off time of 400 ns is internally set.

The equations setting the On Time in second and frequency in Hertz are as follows:

$$T_{ON} = \frac{4.45 \times 10^{-12} \times R_{TON} \times V_{OUT}}{V_{IN} - 0.5 \text{ V}} \qquad \dots (1)$$

$$Fs = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \qquad \dots (2)$$

In this application example, the RTON is chosen to be 1 MΩ, when VIN = 20 V, the TON is 342 ns and FS is around 220 kHz.

Output Inductor Selection

The value of inductor is decided by the inductor ripple current and working frequency. Larger inductor value normally means smaller ripple current. However, if the inductance is chosen too large, it results in slow response and lower efficiency. The ripple current is a design freedom which can be determined by the design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}} \qquad \dots (3)$$

$$I_{RIPPLE} = k \times I_{OUT}$$

Where k is percentage of output current.

In this example, inductor from COILCRAFT DO5010H-332 with L=3.3 μH is chosen.

Current Ripple is recalculated as below:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L_{OUT}} \qquad \dots (4)$$

$$= \frac{(20\,V - 1.5\,V) \times 310ns}{3.3\,\mu H}$$

$$= 1.738\,A$$

Output Capacitor Selection

Output capacitor value is basically determined by the amount of the output voltage ripple allowed during steady state (DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both conditions.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation (5).

$$\Delta V_{RIPPLE} = ESR \times \Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \qquad \dots (5)$$

Where ESR is the output capacitors' equivalent series resistance, COUT is the value of output capacitors.

Typically POSCAP is recommended to use in NX9548's applications. The amount of the output voltage ripple is dominated by the first term in equation (5) and the second term can be neglected.

For this example, one POSCAP 2R5TPE330MC is chosen as output capacitor, the ESR and inductor current typically determines the output voltage ripple. When VIN reaches maximum voltage, the output voltage ripple is in the worst case.

$$ESR_{desire} = \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}} = \frac{30\,mV}{1.738\,A} = 17.2\,m\Omega \quad \dots (6)$$

If low ESR is required, for most applications, multiple capacitors in parallel are needed. The number of output capacitor can be calculating as the following:

$$N = \frac{ESR_E \times \Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \qquad \dots (7)$$

$$N = \frac{2\,m\Omega \times 1.738\,A}{30\,mV}$$

$$N = 0.70$$

The number of capacitor has to be round up to an integer. Choose N =1.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$$\Delta V_{droop} < \Delta V_{tran} @\text{step load } \Delta I_{STEP}$$

The voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor; the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \qquad \ldots (8)$$

Where, τ is a function of capacitor.

$$\tau = \begin{cases} 0 & if\ L \leq L_{crit} \quad \ldots (9) \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & if\ L \geq L_{crit} \end{cases}$$

Where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad \ldots (10)$$

Where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L < L_{crit}$ is true. In that case, the transient spec is mostly like to dependent on the ESR of capacitor.

In most cases, the output capacitor is multiple capacitors in parallel. The number of capacitors can be calculated by the following:

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \ldots (11)$$

Where

$$\tau = \begin{cases} 0 & if\ L \leq L_{crit} \quad \ldots (12) \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & if\ L \geq L_{crit} \end{cases}$$

For example, assume voltage droop during transient is 60 mV for 3 A load step.

If one POSCAP 2R5TPE330MC (330 µF, 12 mΩ ESR) is used, the critical inductance is given as:

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}}$$

$$= \frac{12\ m\Omega \times 3300\ \mu F \times 1.8\ V}{3\ A}$$

$$= 23.76\ \mu H$$

The selected inductor is 3.3 µH which is smaller than critical inductance. In that case, the output voltage transient mainly dependent on the ESR.

Number of capacitors is:

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} = \frac{12\ m\Omega \times 4.5\ A}{60\ mV} = 0.9$$

Choose N=1.

Based On Stability Requirement

ESR of the output capacitor cannot be chosen too low which will cause system instability. The zero caused by output capacitor's ESR must satisfy the requirement as below:

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{F_{SW}}{4} \qquad ...(13)$$

Besides that, ESR has to be big enough so that the output voltage ripple can provide enough voltage ramps to error amplifier through FB pin. If ESR is too small, the error amplifier is unable to correctly detect the ramp and the high side MOSFET will be only turned off for the minimum time of 400 ns. Double pulsing and bigger output ripple will be observed. In summary, the ESR of output capacitor has to be large enough to make the system stable, but also has to be small enough to satisfy the transient and DC ripple requirements.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually a 1 µF ceramic capacitor is chosen to decouple the high frequency noise. The bulk input capacitors are determined by voltage rating and RMS current rating. The input capacitors RMS current can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1 - D} \qquad ...(14)$$

$$D = T_{ON} \times F_S$$

When V_{IN} = 22 V, V_{OUT} = 1.5 V, I_{OUT} = 8 A, the resulting input RMS current calculates to 2.05 A.

For higher efficiency, low ESR capacitors are recommended. One 10 µF/X5R/25 V and two 4.7 µF/X5R /25 V ceramic capacitors are chosen as input capacitors.

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.75 V. The divider consists of two resistors so that the output voltage applied at the FB pin is 0.75 V when the output voltage is at the desired value.

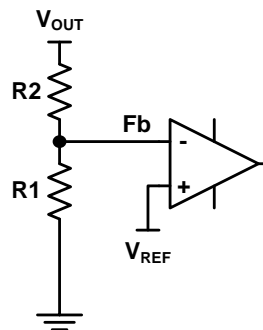Equation 14 applies to Figure 16, which shows the relationship between V_{OUT}, V_{REF} and voltage divider.

Figure 16 · **Voltage Divider**

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \qquad ...(14)$$

Where R2 is part of the compensator and the value of R1 value can be set by voltage divider.

Mode Selection

NX9548 can be operated in PSM mode, ultrasonic PSM mode, CCM mode and shutdown mode by applying different voltages to the EN_MODE pin.

When VCC is applied to EN_MODE pin the NX9548 is in PSM mode. The low side MOSFET emulates the function of a diode when discontinuous continuous mode happens, often in light load conditions. In this condition the inductor current crosses the zero amperes border and become negative current. When the inductor current reaches negative territory, the low side MOSFET is turned off and it takes longer for the output voltage to drop, the high side MOSFET waits longer to be turned on. At the same time regardless of the load level the on time of high side MOSFET remains constant. Therefore the lighter load, the lower the switching frequency will be. However in ultrasonic PSM mode, the lowest frequency is set to be 25 kHz to avoid audio frequency modulation. Thus in PSM mode this kind of reduction of frequency maintains high efficiency even at light loads.

In CCM mode the inductor current zero-crossing sensing is disabled and the low side MOSFET remains on even when inductor current becomes negative. This causes the efficiency to be lower compared with PSM mode at light load, but frequency will remain constant.

Over Current Protection

Over current protection for NX9548 is achieved by sensing current through the low side MOSFET. A typical internal current source of 24 µA flows through an external resistor connected from OCP pin to SW node and sets the over current protection threshold. When the synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over current occurs as shown in Figure 17.
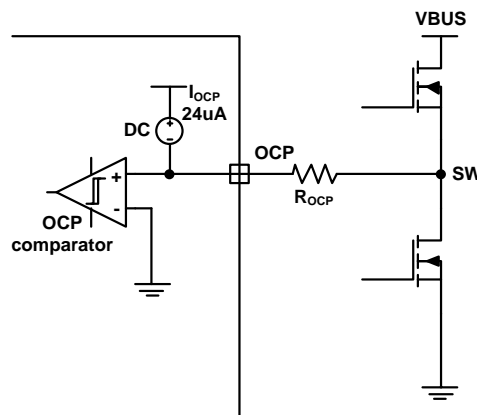
Figure 17 · **Over Voltage Protection**

The over current limit can be set by the following equation.

$$I_{SET} = I_{OCP} \times \frac{R_{OCP}}{R_{DSON}}$$

The typical low side MOSFET RDSON is 21 mΩ at the OCP threshold, and the current limit is set at 10 A, then:

$$R_{OCP} = \frac{I_{SET} \times R_{DSON}}{I_{OCP}} = \frac{10\,A \times 21\,m\Omega}{24\,\mu A} = 8.75\,k\Omega$$

Choose $R_{OCP} = 8.87\,k\Omega$.

Power Good Output

PGOOD output is an open drain output; a pull up resistor is needed. Typically when softstart is finished and FB pin voltage is over 90% of V_{REF}, the PGOOD pin is pulled to high after a 1.6 ms delay.

Output Over Voltage Protection

Typically when the FB pin voltage exceeds 125% of V_{REF}, the high side MOSFET will be turned off and the low side MOSFET will be latched on to discharge the output voltage. To resume the switching operation, a reset to VCC or EN_MODE is necessary.

Output Under Voltage Protection

When the FB pin voltage is typically under 70% of V_{REF}, the high side and low side MOSFET will be turned off. To resume the switching operation, VCC or EN_MODE has to be reset.

Setting Switching Frequency

The NX9548 has a frequency setting resistor "RFREQ" between Pin 24 and the input rail. The current through this resistor sets the theoretical switching frequency of the regulator as shown in Figure 18 and Figure 19. Both of these are the same, but the latter is on a log versus log scale to clarify the extremities. Keep in mind that these are valid curves provided the minimum ON-time (T_{ONMIN}), or the minimum OFF-time (T_{OFFMIN}) of the COT regulator does not come into play, causing significant deviation from the frequency programmed as per Figure 18 and Figure 19 . In all cases, if a T_{ONMIN} or T_{OFFMIN} brickwall is encountered, the switching frequency will trail off negating typical expectations of constant frequency operation (in CCM mode). This veering away of frequency is discussed in more detail in the following section. If however that does not happen, the curves in Figure 18 and Figure 19 are nominal and the typical spread as input voltage varies, is ±10% (not including process variation which typically adds another ±10%).

The equation to use (for nominal frequency) as verified on the bench is, (using fsw in Hz, RFREQ in Ω):
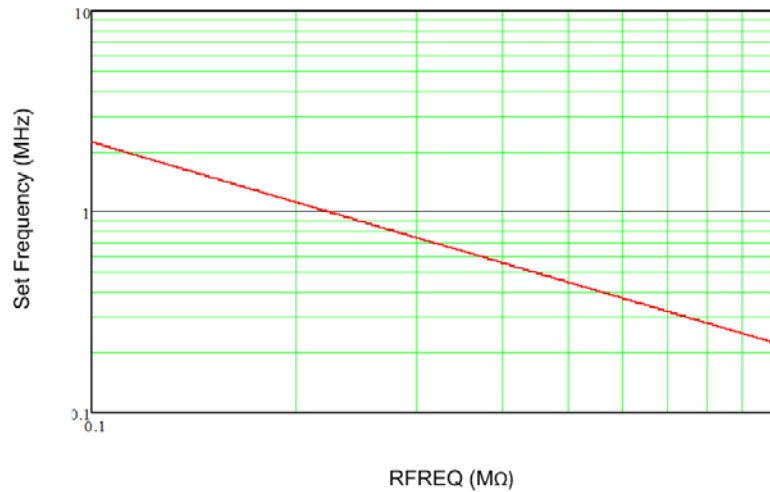
$$fsw(Hz) = \frac{10^{12}}{4.5 \times RFREQ(\Omega)}$$

Figure 18 · **Setting Frequency (Linear axes)**

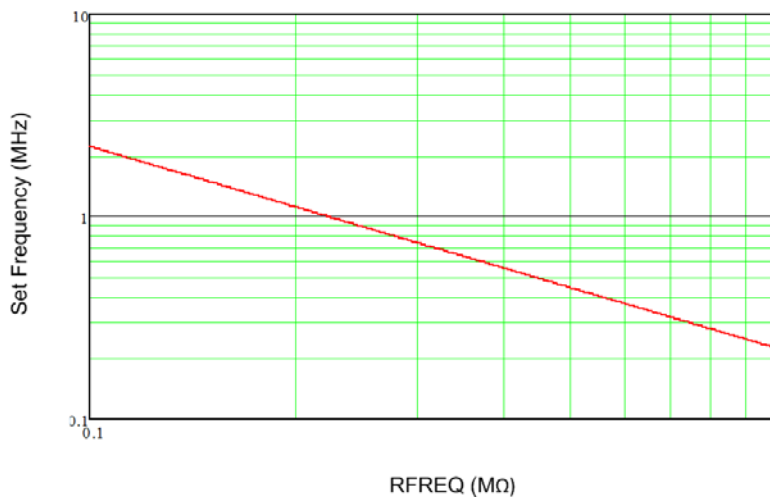Figure 19 · **Setting Frequency (Log axes)**

Safe Operating Regions (for constant frequency in CCM mode)

As mentioned above, if the T_{ONMIN} or T = brickwalls are encountered, the typically constant frequency of any adaptive COT regulator is affected. Though the regulator "works", all calculated predictions are off since the frequency can drop abruptly at those brick wall contention points. In other words, the natural duty cycle demand cannot be met at the programmed frequency because T_{ON} = D/fsw is less than T_{ONMIN}. Therefore fsw must decrease as a result, otherwise output regulation would suffer. Note that this behavior is not the pulse-skipping (power saving) mode, which only occurs at very light loads. This is definitely an avoidable mode, because it occurs even at max load. By lowering the frequency suddenly at max load, we run the risk of a huge increase in output ripple for example. In some cases, this reduced frequency can also cause inductor saturation and consequential field reliability issues. So these regions should be avoided by careful design.

A simple Mathcad file was created, using a T_{ONMIN} brickwall of 100 ns (typically measured on the bench to be 80 ns), and a T_{OFFMIN} (guaranteed max value) of 800 ns to find this safe operating region. Note that although the latter number seems large, it is not a device limitation. It is in fact an important design-in parameter for ensuring proper response of the COT regulator under abnormal operating conditions. It provides enough time for the inductor current to slow down under such strange conditions, rather than causes flux staircasing. The results of the Mathcad file are presented in Figure 20 to Figure 25 which shows the limitations on input/output voltage combinations vis-à-vis switching frequency.
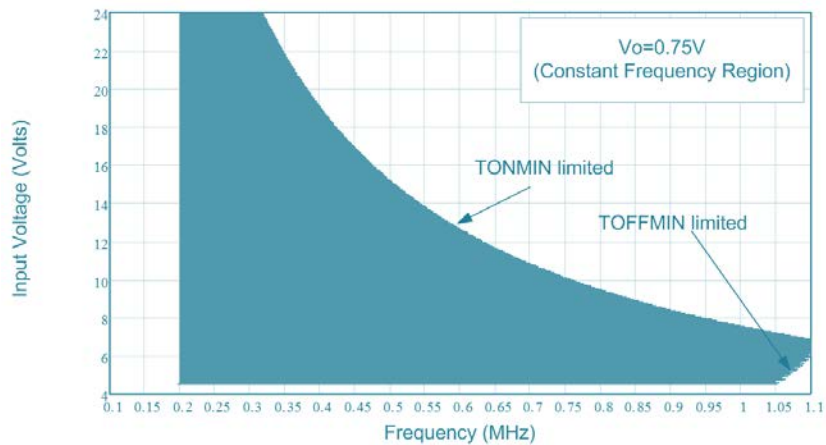
Figure 20 · **Setting switching frequency correctly for V_{OUT} = 0.75 V, and its safe input operating region**
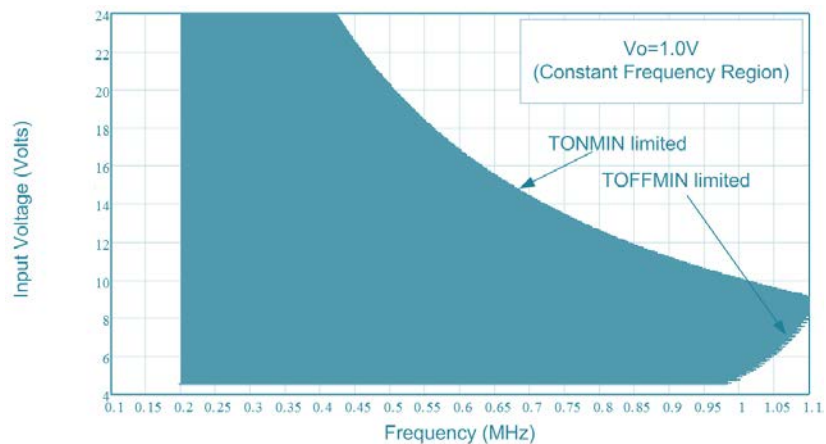
Figure 21 · **Setting switching frequency correctly for V_{OUT} = 1.0 V, and its safe input operating region**
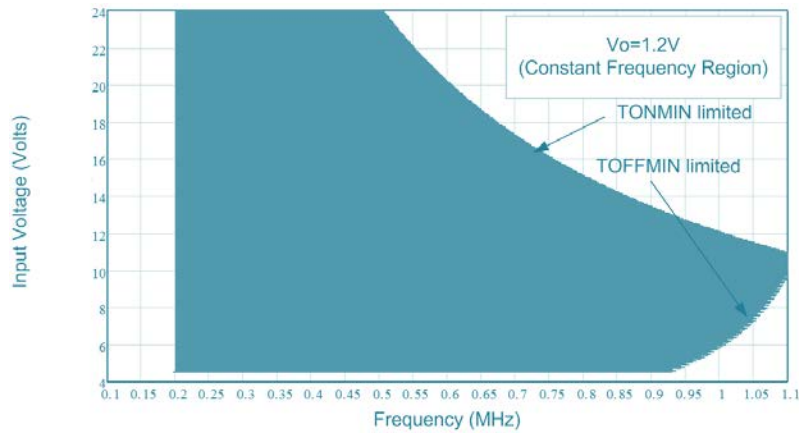
Figure 22 · **Setting switching frequency correctly for V$_{OUT}$ = 1.2 V, and its safe input operating region**
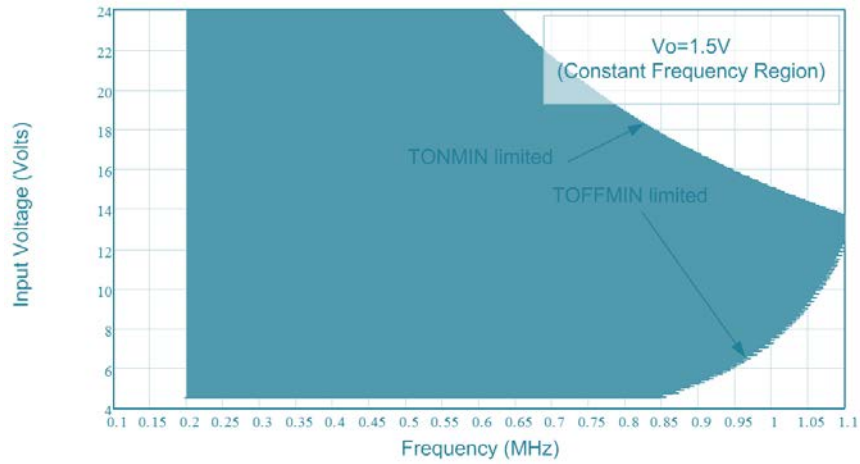
Figure 23 · **Setting switching frequency correctly for V$_{OUT}$ = 1.5 V, and its safe input operating region**
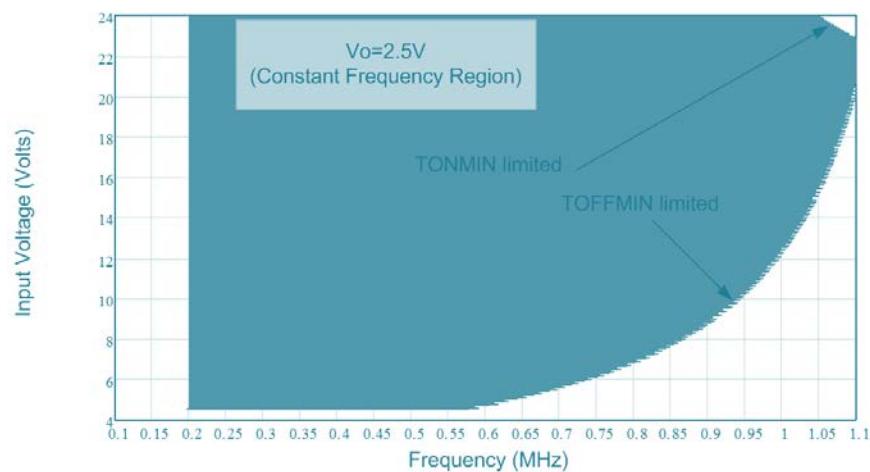
Figure 24 · **Setting switching frequency correctly for V$_{OUT}$ = 2.5 V, and its safe input operating region**
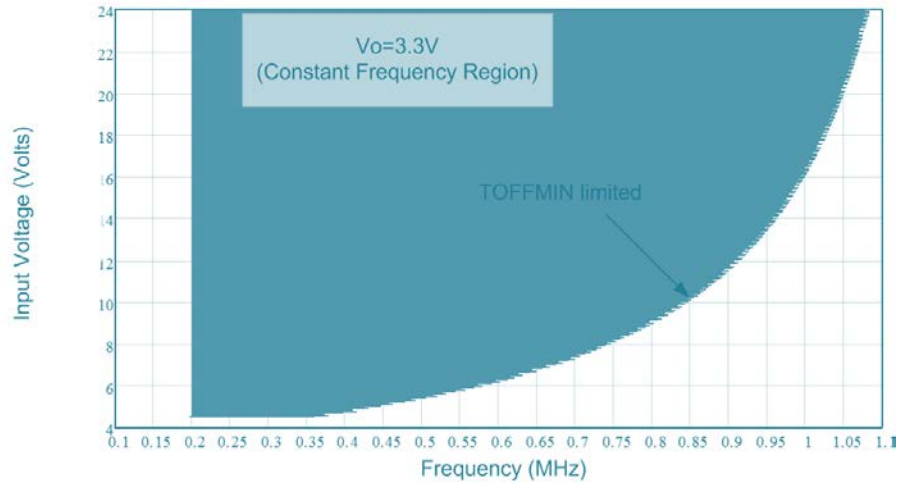
Figure 25 · **Setting switching frequency correctly for V$_{OUT}$ = 3.3 V, and its safe input operating region**

Package Dimensions
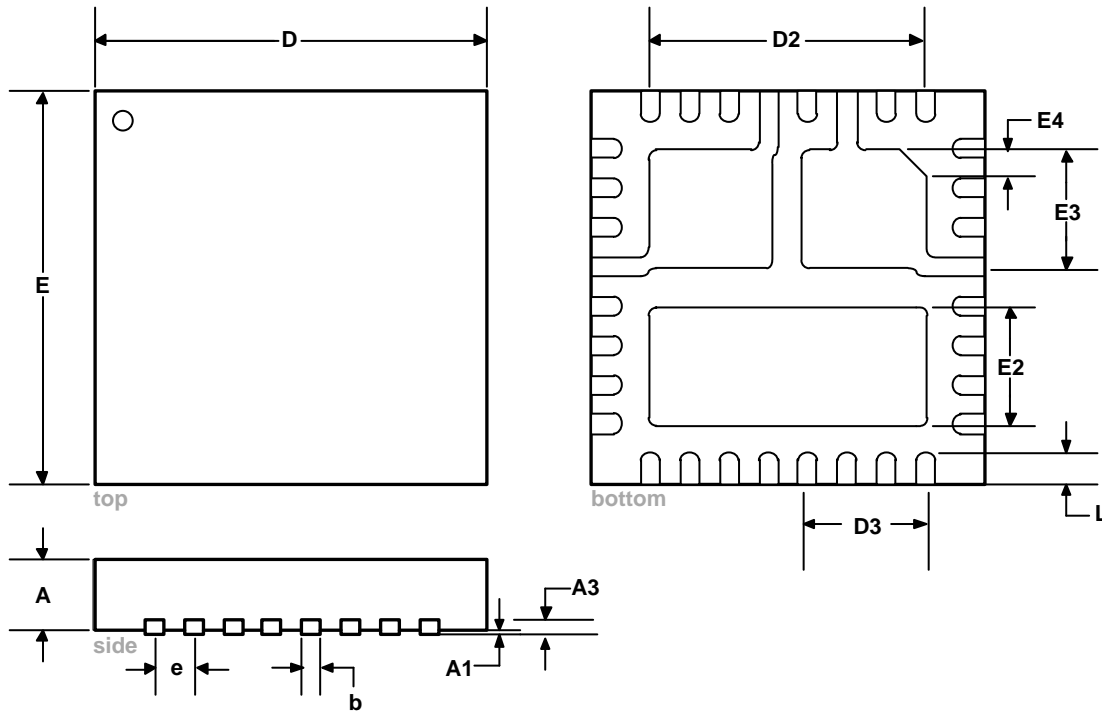
Figure 26 · **VQFN 5x5 mm 32L with 3 Exposed Pads**

Note: 1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

2. Dimensions are in mm, inches are for reference only

DIM	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
A	0.800	1.000	0.035	
A1	0	0.05	0	0.002
A3	0.203 REF		0.008 REF	
e	0.50Bsc		0.020	
D	4.950	5.050	0.195	0.199
E	4.950	5.050	0.195	0.199
D2	3.400	3.500	0.134	0.138
D3	1.475	1.575	0.058	0.062
L	0.350	0.450	0.014	0.018
E2	1.475	1.575	0.058	0.062
E3	1.475	1.575	0.058	0.062
E4	0.300x45°		0.012x45°	
b	0.200	0.300	0.008	0.012

Land Pattern Recommendation
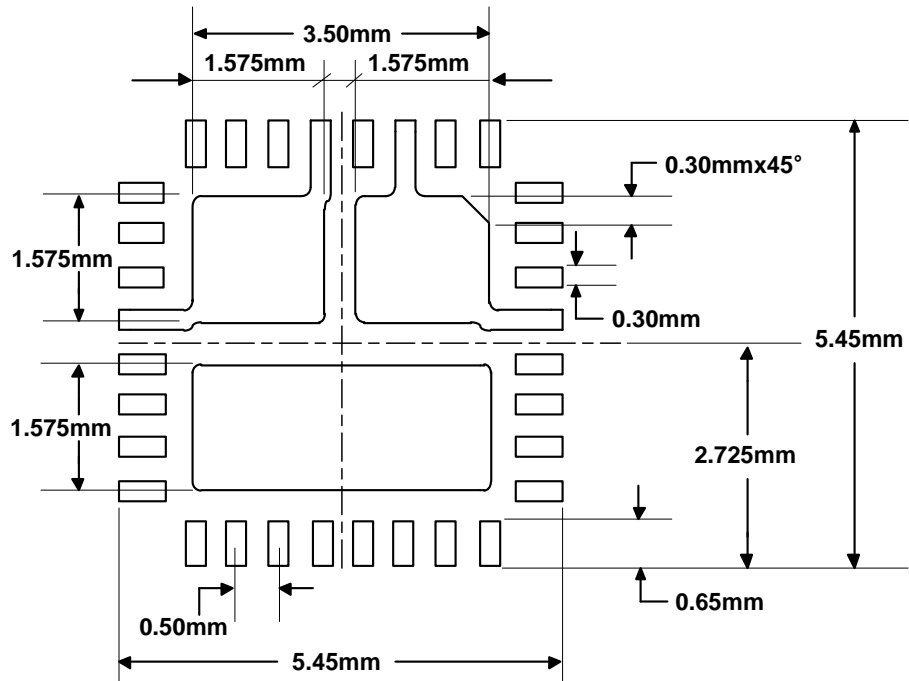
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