NXF6505A-Q100; NXF6505B-Q100

Low-noise, 1.2 A transformer driver for isolated power supplies

Rev. 2 — 22 August 2025 **Product data sheet**

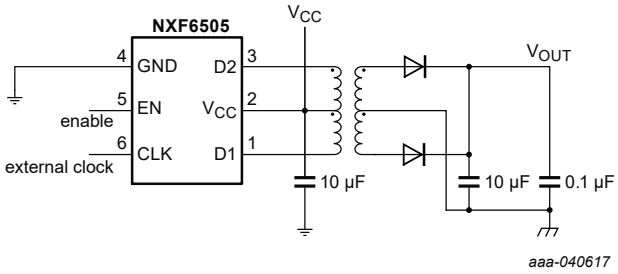
1. General description

The NXF6505A/B-Q100 is a specialized push-pull transformer driver that is designed for isolated power supplies in small form factors. This driver is capable of driving low-profile, center-tapped transformers from a 2.25 V to 5.5 V DC power supply, while achieving ultra-low noise and EMI using slew rate control and Spread Spectrum Clocking (SSC).

The NXF6505A/B-Q100 features internal protection features such as current limiting, undervoltage lockout, thermal shutdown, and break-before-make circuitry, ensuring the device operates within safe limits. The device also includes a soft-start feature that prevents high inrush current during power-up with large load.

The NXF6505A/B-Q100 is constructed using an oscillator and a gate drive circuit that produces complementary output signals to drive ground-referenced N-channel power switches. These two complementary 1.2 A Power-MOSFET switches can be used to provide >6 W power. The 440 kHz internal oscillator is for applications that require higher efficiency and smaller transformers. The NXF6505A/B-Q100 is available in a small 6 pin SOT8061-1 package and is characterized for operation within a temperature range of -55 °C to 125 °C.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.



2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -55 °C to +125 °C
- Push-pull driver for transformers, optimized for low EMI:
  - Slew-rate control output
  - Spread Spectrum Clocking (SSC)
- Wide input voltage range: 2.25 V to 5.5 V
- High output drive: 1.2 A at 5 V supply
- Low R_{ON} 0.2 Ω maximum at 5 V supply
- Internal switching frequency:
  - for NXF6505A-Q100: 160 kHz
  - for NXF6505B-Q100: 440 kHz
- Synchronization of multiple devices with external clock input
- 2.2 A current limit at 5 V
- Enable pin to put device in low shutdown current: <1 µA
- Thermal shutdown protection
- Soft-start start-up
- Packages
  - Small 6 pin SOT8061-1 (SC-74; TSOP-6) package
  - Small 6 pin SOT8120-1 (LSOT6) package
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 6000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- Functional Safety-capable

3. Applications

- Isolated power supply for automotive and industrial applications including:
  - CAN, RS-485, RS-422, RS-232, SPI, I²C, low-power LAN
- Low-noise isolated USB supplies
- Process control
- Telecom supplies
- Radio supplies
- Distributed supplies
- Medical instruments
- Precision instruments
- Low-noise filament supplies

- Motor control
- Isolated power supplies for automotive (AEC-Q100)
  - Traction inverter
  - DC-DC converter
  - Battery management system
  - On-board charger

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXF6505ADA-Q100	-55 °C to +125 °C	TSOT23-6	Plastic, surface-mounted package; 6 leads	SOT8061-1
NXF6505BDA-Q100	-55 °C to +125 °C	TSOT23-6	Plastic, surface-mounted package; 6 leads	SOT8061-1
NXF6505ADM-Q100/G	-55 °C to +125 °C	LSOT6	Plastic, 6 pins; 0.95 mm pitch; 2.9 mm × 1.6 mm × 1.45 mm body	SOT8120-1
NXF6505BDM-Q100/G	-55 °C to +125 °C	LSOT6	Plastic, 6 pins; 0.95 mm pitch; 2.9 mm × 1.6 mm × 1.45 mm body	SOT8120-1

5. Marking

Table 2. Marking

Type number	Marking code
NXF6505ADA-Q100	N5A
NXF6505BDA-Q100	N5B
NXF6505ADM-Q100/G	G5A
NXF6505BDM-Q100/G	G5B

6. Functional diagram

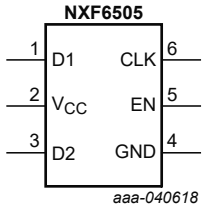


Fig. 1. Logic symbol

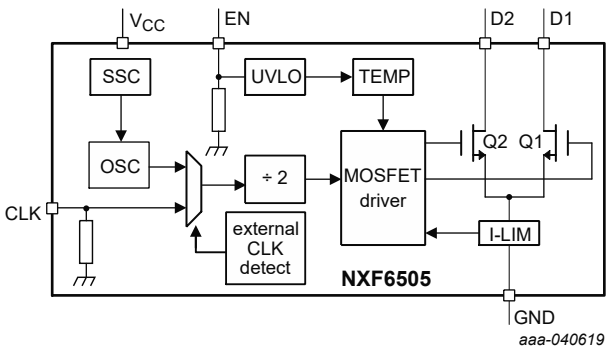
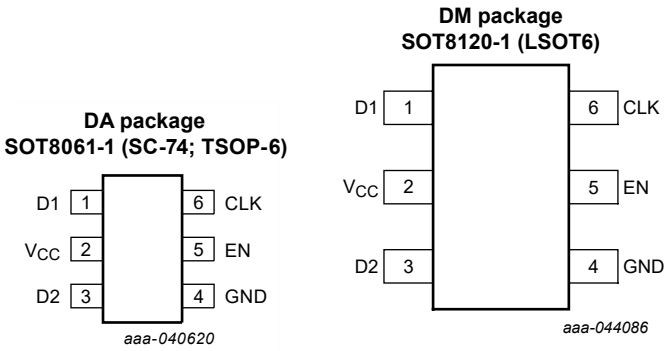


Fig. 2. Functional diagram

7. Pinning information

7.1. Pinning information



7.2. Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
D1	1	O	Open-drain output of the first power MOSFETs. Usually connected to one of the outer terminals of the center tap transformer. Because large currents flow through this pin, its external trace should be kept short.
V_{CC}	2	P	This is the device supply pin. It should be bypassed with a 4.7 µF or greater, low ESR capacitor. When $V_{CC} \leq 2.25$ V, an internal undervoltage lockout circuit trips and turns both outputs off.
D2	3	O	Open-drain output of the second power MOSFETs. Usually connected to the other one of the outer terminals of the center tap transformer. Because large currents flow through this pin, its external trace should be kept short.
GND	4	G	GND is connected to the source of the power MOSFET switches via an internal sense circuit. Because large currents flow through it, the GND terminals must be connected to a low-inductance quality ground plane.
EN	5	I	The EN pin turns the device on or off. Grounding or leaving this pin floating disables all internal circuitry. This pin is recommended to be tied directly to V_{CC} for always on operation.
CLK	6	I	This pin is used to run the device with external clock. Internally it is pulled down to GND. If valid clock is not detected on this pin, the device shifts automatically to internal clock.

8. Functional description

8.1. Overview

The NXF6505-Q100 is a specialized transformer driver designed to cater to low-cost, small form-factor, and isolated DC-DC converters. It utilizes push-pull topology to provide efficient power conversion to such systems. The device includes an oscillator that provides a signal to a gate-drive circuit, which generates two complementary output signals that control the switching of two output transistors alternatively.

The gate-drive circuit consists of a frequency divider and a break-before-make (t_{b-m}) logic, which work together to ensure the efficient and safe operation of the device. The frequency divider reduces the oscillator frequency by two, allowing the device to operate at a frequency that is appropriate for its intended use.

8.2. Functional block diagram

The NXF6505-Q100 functional block diagram is shown below:

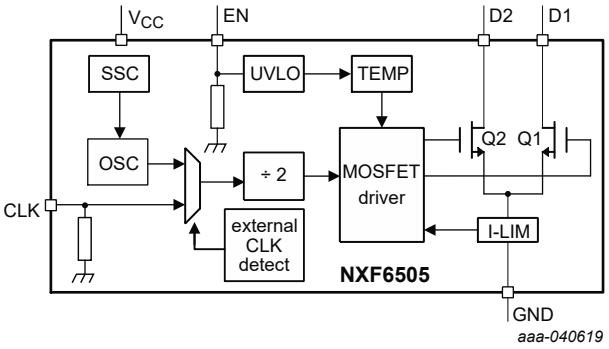


Fig. 3. Functional block diagram

8.3. Feature description

Push-pull converter

A push-pull converter is a type of DC-DC converter that uses a transformer with a center-tap to transfer power from the primary to the secondary. The converter uses two switches, Q1 and Q2, to alternately switch current through the two halves of the transformer primary. See Fig. 4 below.

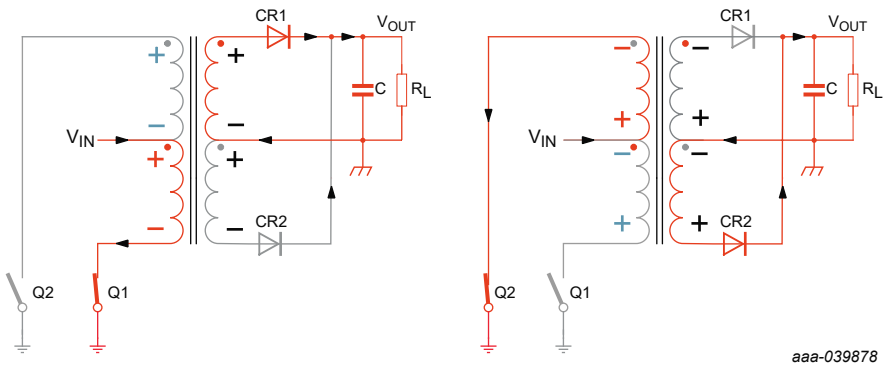


Fig. 4. Switching cycles of a push-pull converter

When Q1 conducts, it drives a current through the lower half of the primary to ground, creating a negative voltage potential at the lower primary end with respect to the V_{IN} potential at the center-tap. At the same time, the voltage across the upper half of the primary is such that the upper primary end is positive with respect to the center-tap in order to maintain the previously established current flow through Q2, which is now in a high-impedance state.

The two voltage sources, each equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2 \times V_{IN}$ with respect to ground. Per dot convention, the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR1. The secondary current starting from the upper secondary end flows through CR1, charges capacitor C, and returns through the load impedance RL back to the center-tap.

During the off-time of Q1, Q2 conducts, and the current flow in the primary is reversed. This creates a negative voltage potential at the upper primary end with respect to the center-tap, and a positive voltage potential at the lower primary end. The same voltage polarities occur at the secondary, and the lower secondary end is now forward biased, causing the secondary current to flow through CR2, charging capacitor C, and returning through the load impedance R_L back to the center-tap.

By alternately switching current through the two halves of the transformer primary, the push-pull converter can step up or step down the input voltage to the desired output voltage. The capacitor C acts as a filter, smoothing out the output voltage ripple.

During the operation of a push-pull converter, when Q2 conducts, Q1 turns off and the voltage polarities at both primary and secondary sides of the transformer reverse. The lower end of the primary now presents an open end with a voltage potential of 2 × V_{IN} against ground. Consequently, diode CR2 becomes forward biased, while diode CR1 becomes reverse biased. As a result, the current flows from the lower end of the secondary through CR2, charges the capacitor, and then returns through the load impedance RL to the center-tap of the transformer. This completes one cycle of operation of the push-pull converter, and the process repeats for subsequent cycles.

Core magnetization

Fig. 5 depicts the magnetizing curve for an ideal push-pull converter, where B and H represent magnetic flux density and field strength, respectively. During Q1 conduction, the magnetic flux moves from point A to A', and during Q2 conduction, it moves back to point A. The difference in flux density is proportional to the product of the primary voltage, V_P, and the on-time, t_{ON}. This V-t product determines the core magnetization during each switching cycle. Any imbalance in the V-t products of both phases cause an offset from the B-H curve's origin, leading the transformer towards saturation gradually. It is necessary to maintain balance in push-pull converters for optimal efficiency and reliability, which can be achieved by adjusting the primary voltage, duty cycle, or using a larger core transformer. By carefully designing and selecting the transformer and its components, reliable and efficient operation can be ensured over a wide range of load conditions.

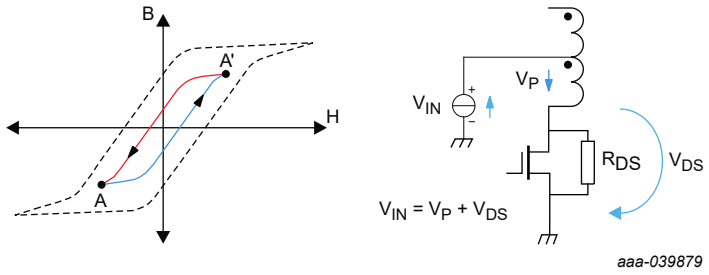


Fig. 5. Core magnetization and self-regulation through positive temperature coefficient of $R_{DS(on)}$

8.4. Functional modes

Start-up mode

The internal oscillator of a circuit initiates operation when the supply voltage at V_{CC} ramps up to 2.25 V. The output stage then starts switching, but the amplitude of the drain signals at D1 and D2 is not yet at its maximum level.

Soft-Start

The NXF6505A-Q100 and NXF6505B-Q100 devices are designed to support the soft-start feature. When the power is turned on or the EN pin changes from Low to High, the gate drive of the output power-MOSFET gradually increases from 0 V to V_{CC} over a period of time defined by t_{SS} parameter. This gradual increase in gate drive prevents high inrush current from V_{CC} while charging large secondary side decoupling capacitors. It also prevents overshoot in secondary voltage during power-up. Soft-start is an essential feature for power supplies to ensure reliable and stable operation. By gradually increasing the gate drive, the circuit can avoid sudden current spikes that may damage the MOSFET or other components in the circuit. Moreover, the soft-start feature prevents overshoot in secondary voltage, which could cause damage to sensitive components connected to the power supply. The NXF6505A-Q100 and NXF6505B-Q100 devices are well-suited for applications that require soft start, making them an ideal choice for power supply designs where reliability and stability are critical factors.

Operating mode

When the device supply has reached its nominal value 2.25 V, the oscillator is fully operating. However, variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2.

Disable mode

To conserve power when not in use, the device includes an enable pin that can be utilized to place the device into an ultra-low-power state. The enable pin comes equipped with an internal pull-down resistor that automatically disables the device when the pin is not being driven. Additionally, if the device is disabled or if the power supply voltage falls below 1.7 V, both D1 and D2 drain outputs will be in high-impedance OFF-state and disconnected from the internal circuitry to prevent any unwanted power consumption or interference with other connected devices.

Spread Spectrum Clocking (SSC)

In high current switching power supplies, radiated emissions are a significant issue to consider. To mitigate this, the NXF6505-Q100 employs a technique known as spread spectrum clocking, which involves modulating the internal clock to spread the emitting energy over multiple frequency bins. This feature significantly enhances the emissions performance of the entire power supply block, which relieves the system designer of a major concern in designing an isolated power supply.

External clock mode

The NXF6505-Q100 includes a clock pin (CLK) that enables synchronization of the device with the system clock and other NFX6505-Q100 devices, allowing the system to control the exact switching frequency of the device. The CLK rising edge is utilized to divide a clock by two, which drives the gates, and the timing diagram is illustrated in Fig. 79. Additionally, the device features an external clock fail-safe function that automatically switches to the internal clock if a valid input clock is not detected for an extended period ($t_{CLK(time)}$). However, the built-in emissions reduction scheme of Spread Spectrum clocking is disabled when an external clock is utilized.

Overcurrent protection mode (OPM)

The NXF6505-Q100 incorporates a protective mechanism against overcurrent, designed to safeguard the system from enduring permanent damage due to excessive current situations. Upon detecting an overcurrent scenario where the current surpasses the predefined threshold ($I_{th(DET)}$) while flowing through the D1 and D2 MOSFET, the NXF6505-Q100 initiates its current limit mode (CLM). This mode regulates the pulse width of the D1 and D2 to reduce the average current passing through them, thus mitigating the risk of damage. Once the overcurrent condition subsides, the NXF6505-Q100 seamlessly returns to its normal operating mode. However, if the overcurrent persists beyond 10 milliseconds (t_{oc}), the NXF6505-Q100 shifts into dead time mode (DTM). In this mode, both D1 and D2 are deactivated to prevent any harm to the system, or its components caused by the prolonged overcurrent situation. Following the 10 millisecond (typical) dead time, the NXF6505-Q100 initiates a soft start mode before transitioning back into its standard operating mode. Fig. 6 shows the state machine flow for the overcurrent protection mode.

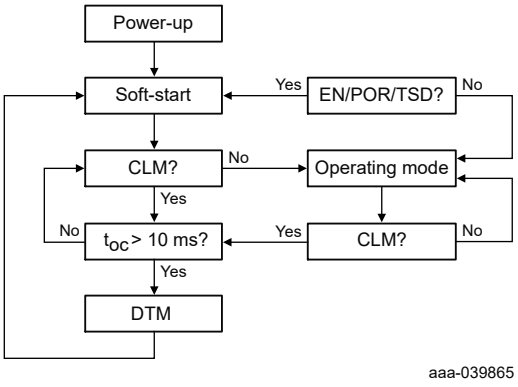


Fig. 6. State machine flow for the overcurrent protection mode

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	6	V
V_I	input voltage	pin EN, CLK	–0.5	6	V
V_O	output voltage	pin D1, D2	–	17	V
$I_{O(peak)}$	peak output current	pin D1, D2	–	20	A
T_J	maximum junction temperature		-55	150	°C
T_{stg}	storage temperature		-65	150	°C

10. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 3A	±6000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3	±1500	V

11. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.25	5.5	V
I_O	output current	pin D1, D2			
		2.25 V ≤ V_{CC} ≤ 2.8 V	-	0.8	A
		2.8 V < V_{CC} ≤ 5.5 V	-	1.2	A
T_{amb}	ambient temperature		-55	125	°C

12. Thermal characteristics

Table 7. Thermal information

The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated

Symbol	Parameter	SOT8061-1 (SC-74; TSOP-6)	SOT8120-1 (LSOT6)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.5	117.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122.9	122.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.6	33.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.5	13.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32	32	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

13. Electrical characteristics

Table 8. Electrical characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -55 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Supply voltage						
I_{CC}	supply current	2.25 V ≤ V_{CC} ≤ 5.5 V; R_L = 50 Ω [2]				
		NXF6505A-Q100	-	1	1.4	mA
		NXF6505B-Q100	-	1.56	2.3	mA
I_{LIH}	HIGH-level input leakage current	pins EN, CLK = V_{CC}	-	10	20	µA
$I_{CC(DIS)}$	supply current	EN = GND	-	0.1	-	µA
I_{LI}	input leakage current	pins D1, D2; EN = GND; D1, D2 = V_{CC}	-	0.1	-	µA
$V_{CC(UVLO)}$	undervoltage lockout supply voltage	positive-going UVLO threshold	-	-	2.25	V
		negative-going UVLO threshold	1.7	-		V
$V_{hys(UVLO)}$	undervoltage lockout hysteresis voltage		-	0.3	-	V
$V_{th(on)}$	on threshold voltage	EN, CLK pin HIGH	-	-	0.7 × V_{CC}	V
$V_{th(off)}$	on threshold voltage	EN, CLK pin LOW	0.3 × V_{CC}	-	-	V
$V_{th(hys)}$	hysteresis threshold voltage	EN, CLK pin hysteresis	-	0.2 × V_{CC}	-	V
CLK input						
$f_{sw(av)}$	average switching frequency	pin D1, D2; R_L = 50 Ω; see Fig. 9				
		NXF6505A-Q100	139	160	209	kHz
		NXF6505B-Q100	374	440	511	kHz
f_{ext}	external frequency	pin CLK				
		NXF6505A-Q100	100	-	600	kHz
		NXF6505B-Q100	100	-	1600	kHz
Output stage						
Δt_{ON}	average ON time mismatch	mismatch between D1 and D2; R_L = 50 Ω	-	0	-	%
R_{ON}	ON resistance	output switch ON resistance; see Fig. 9				
		V_{CC} = 5 V, I_{D1}, I_{D2} = 1 A	-	0.16	0.2	Ω
		V_{CC} = 2.25 V, I_{D1}, I_{D2} = 0.5 A	-	0.21	0.4	Ω
V_{SR}	slew rate voltage	pin D1, D2; R_L = 50 Ω; see Fig. 9				
		NXF6505A-Q100	-	57	-	V/µs
		NXF6505B-Q100	-	155	-	V/µs
$I_{th(DET)}$	current detect threshold	2.8 V < V_{CC} ≤ 5.5V	-	2.2	-	A
		2.25 V < V_{CC} ≤ 2.8 V	-	1.42	-	A
$I_{LIM(AV)}$	average current limit	2.8 V < V_{CC} ≤ 5.5 V	-	404	-	mA
		2.25 V ≤ V_{CC} ≤ 2.8 V	-	224	-	mA

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5 V.
[2] Does not include load current.

14. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);
For timing diagrams and test circuit see Section 14.1; See also additional graphs in Section 14.2.

Symbol	Parameter	Conditions	T_{amb} = -55 °C to +125 °C			Unit
			Min	Typ[1]	Max	
CLK						
$t_{CLK(time)}$	Duration after which device switches to internal clock in case of invalid external clock		10	-	25	µs
Output stage						
t_{b-m}	break-before-make time	measured as voltage with R_L = 50 Ω; see Fig. 9				
		NXF6505A-Q100	-	128	-	ns
		NXF6505B-Q100	-	90	-	ns
Soft-start						
t_{SS}	soft-start time	10% to 90% transition time on V_{OUT} with transformer C_{LOAD} = 40 µF; R_L = 5 Ω	-	5	-	ms
$t_{SS(delay)}$	soft-start time delay	from power up to 90% transition time on V_{OUT} with transformer C_{LOAD} = 40 µF; R_L = 5 Ω	-	8.5	-	ms

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5 V.

14.1. Waveforms and test circuits

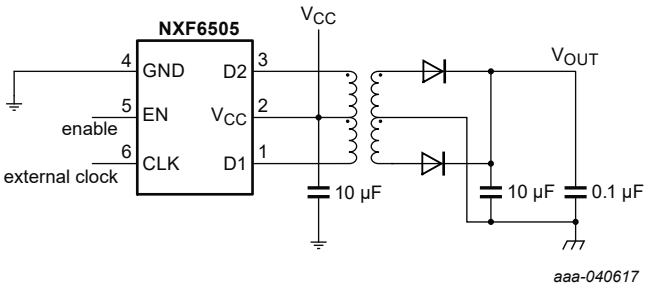


Fig. 7. Test circuit for unregulated output (TP1)

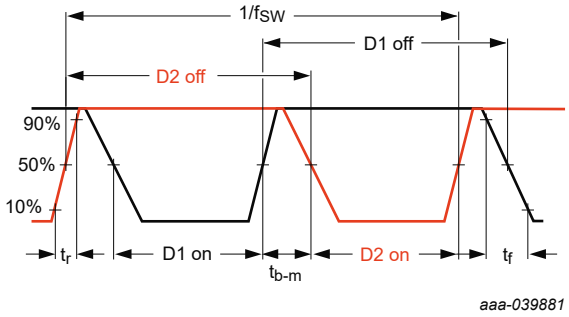


Fig. 8. Timing diagram

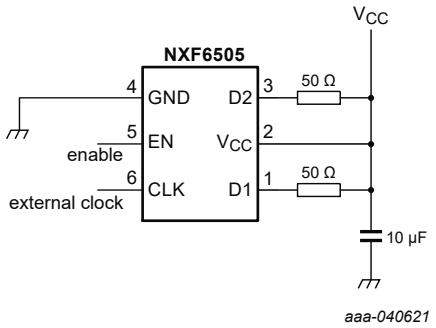
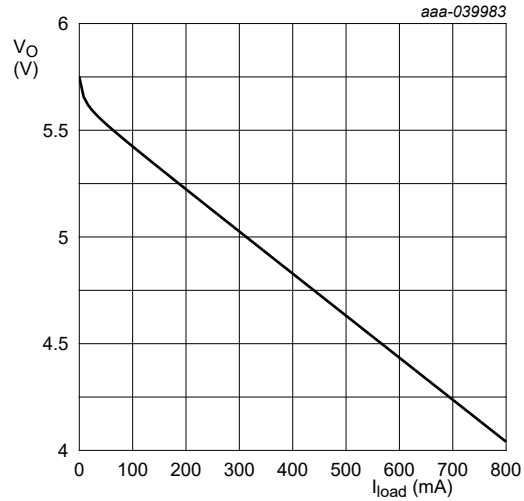


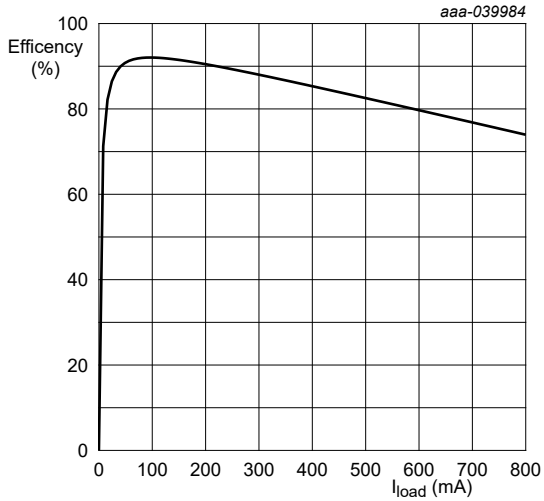
Fig. 9. Test circuit for average switching frequency, slew rate voltage, ON resistance and break-before-make time

14.2. Typical characteristics NXF6505A-Q100



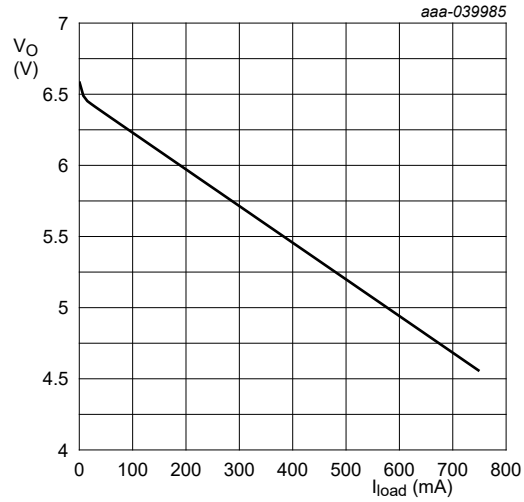
NXF6505A + Wurth 750316031
V_{CC} = 3.3 V

Fig. 10. Output voltage versus load current



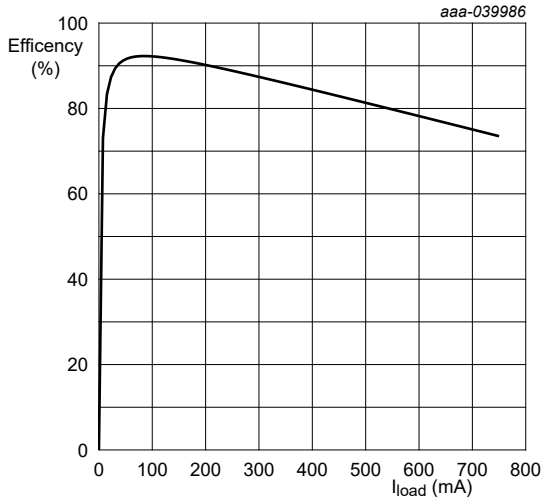
NXF6505A + Wurth 750316031
V_{CC} = 3.3 V

Fig. 11. Efficiency versus load current



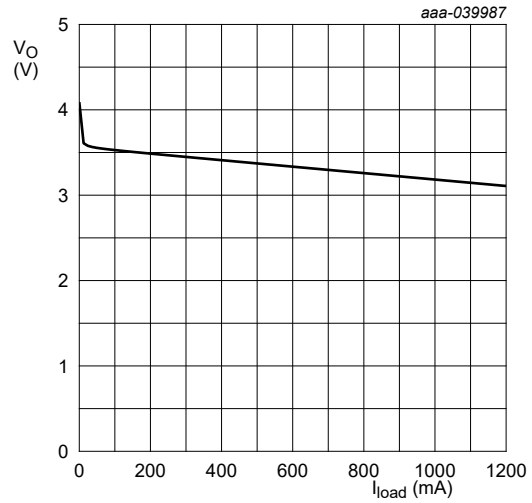
NXF6505A + Wurth 750316032
V_{CC} = 3.3 V

Fig. 12. Output voltage versus load current



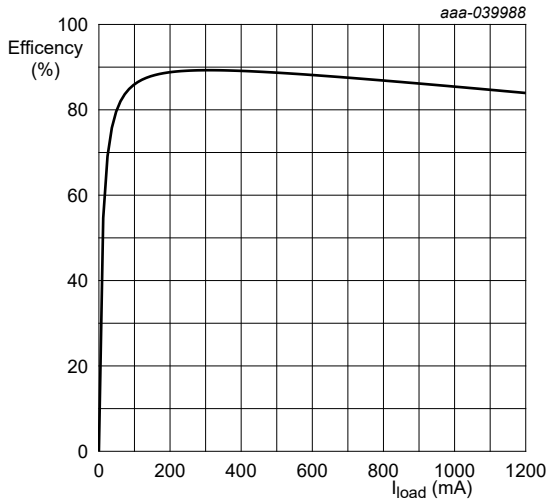
NXF6505A + Wurth 750316032
V_{CC} = 3.3 V

Fig. 13. Efficiency versus load current



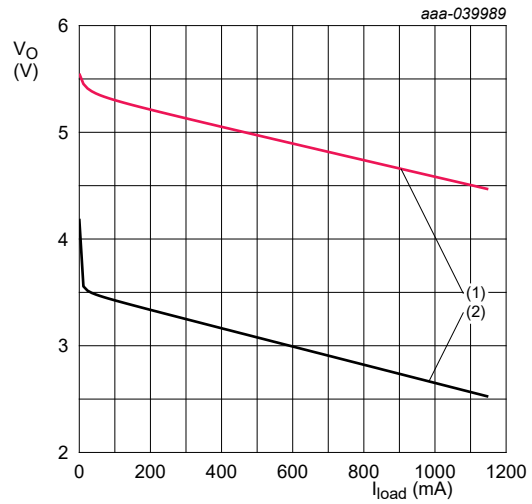
NXF6505A + Wurth 750316033
V_{CC} = 3.3 V

Fig. 14. Output voltage versus load current



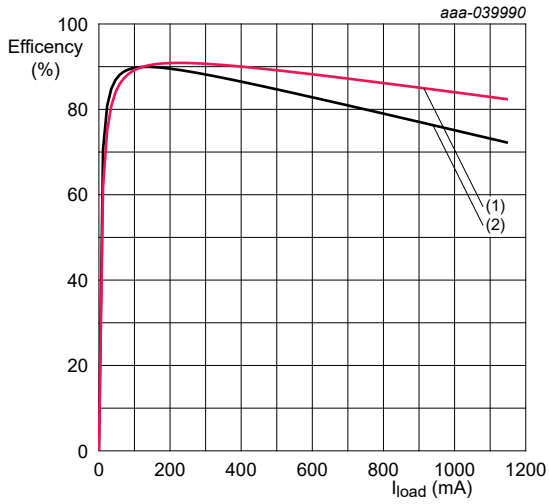
NXF6505A + Wurth 750316033
V_{CC} = 3.3 V

Fig. 15. Efficiency versus load current



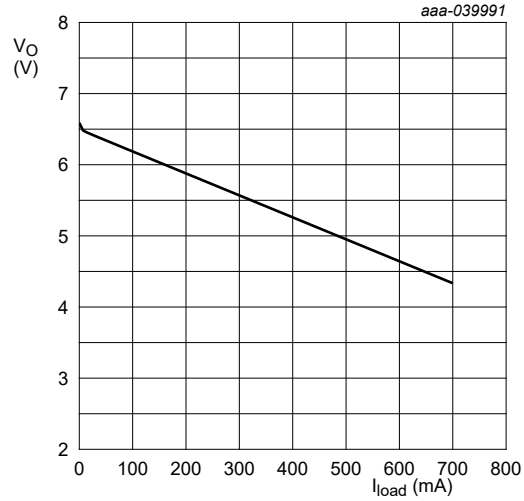
NXF6505A + Wurth 750315240
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 16. Output voltage versus load current



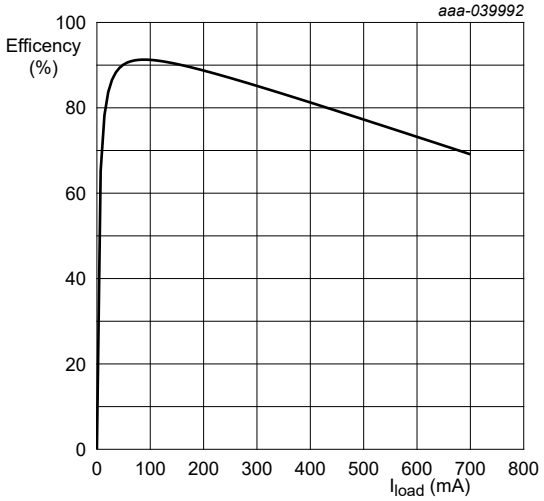
NXF6505A + Wurth 750315240
(1) V_{CC} = 3.3 V
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 17. Efficiency versus load current



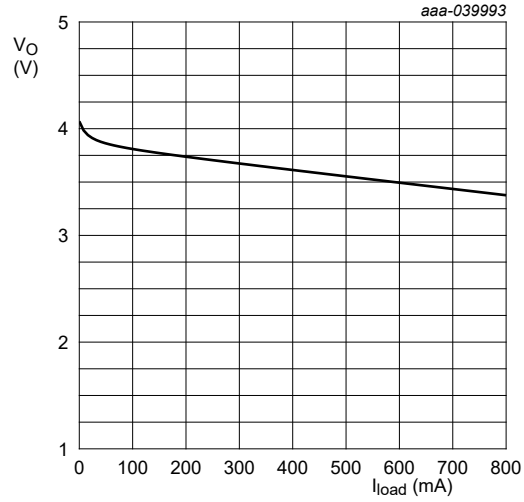
NXF6505A + SunLord ALTWR-H47TF
V_{CC} = 5 V

Fig. 18. Output voltage versus load current



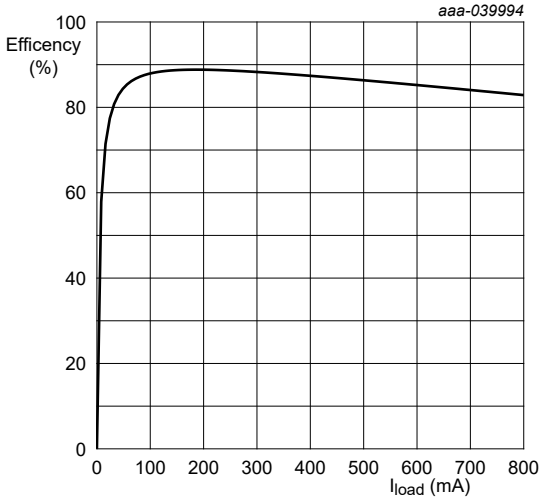
NXF6505A + SunLord ALTWR-H47TF
V_{CC} = 5 V

Fig. 19. Efficiency versus load current



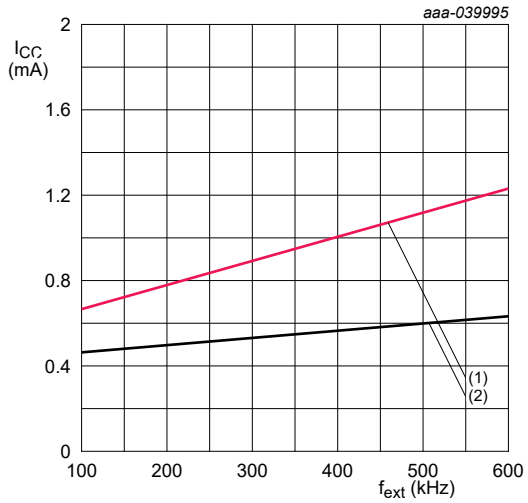
NXF6505A + SunLord ALTWR-H94TF
V_{CC} = 5 V

Fig. 20. Output voltage versus load current



NXF6505A + SunLord ALTWR-H94TF
V_{CC} = 5 V

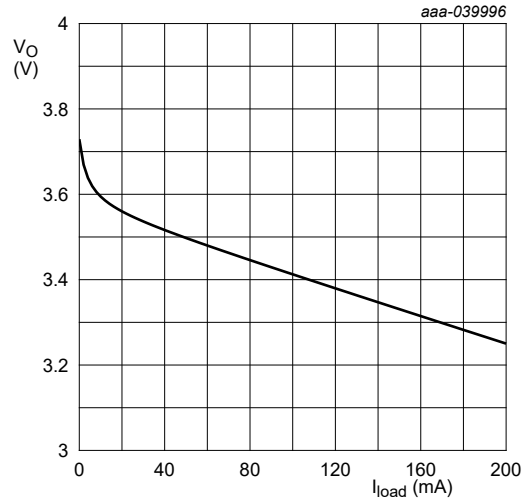
Fig. 21. Efficiency versus load current



NXF6505A
(1) V_{CC} = 5.5 V
(2) V_{CC} = 2.25 V

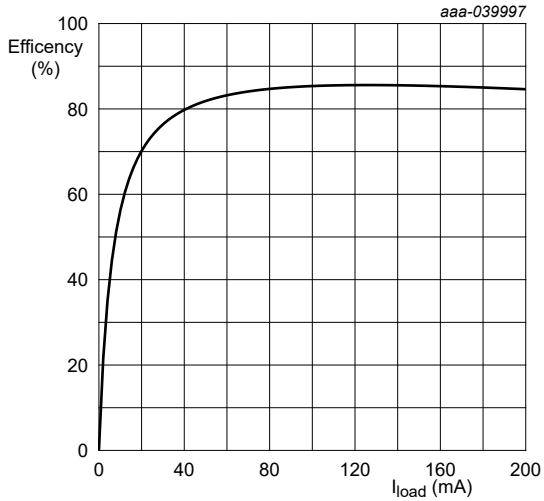
Fig. 22. Supply current versus external frequency

14.3. Typical characteristics NXF6505B-Q100



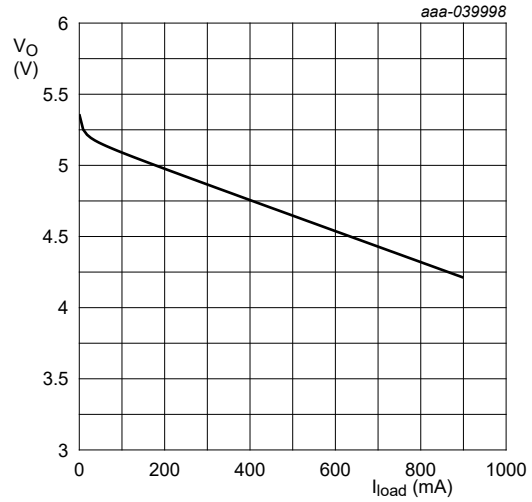
NXF6505B + Wurth 760390011
V_{CC} = 3.3 V

Fig. 23. Output voltage versus load current



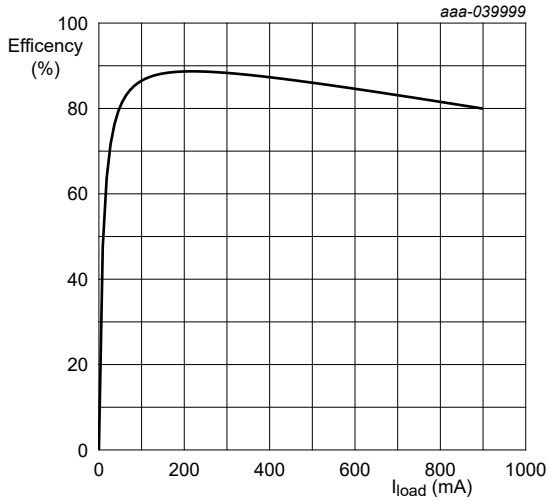
NXF6505B + Wurth 760390011
V_{CC} = 3.3 V

Fig. 24. Efficiency versus load current



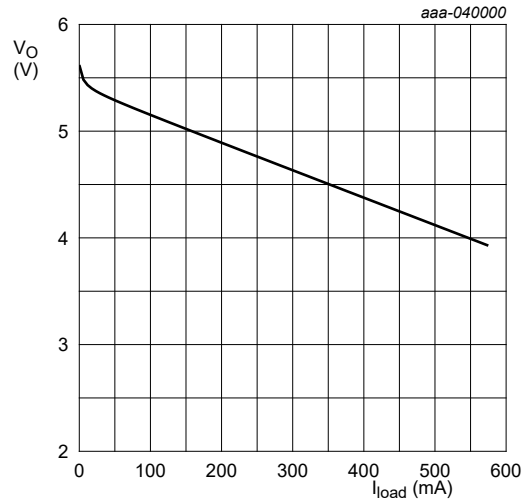
NXF6505B + Wurth 760390012
V_{CC} = 5 V

Fig. 25. Output voltage versus load current



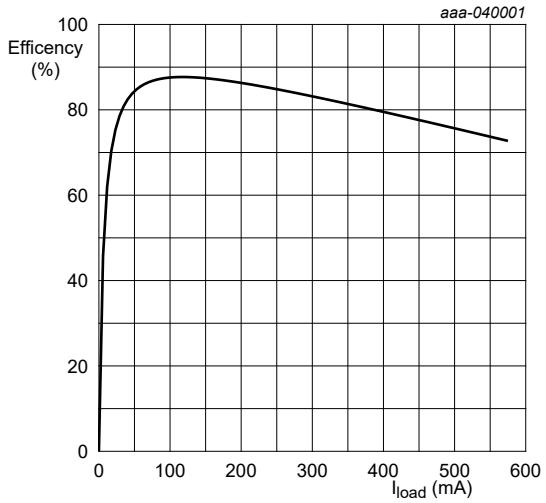
NXF6505B + Wurth 760390012
V_{CC} = 3.3 V

Fig. 26. Efficiency versus load current



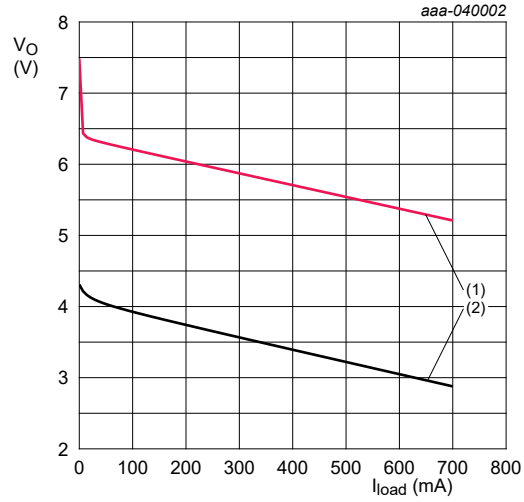
NXF6505B + Wurth 760390013
V_{CC} = 3.3 V

Fig. 27. Output voltage versus load current



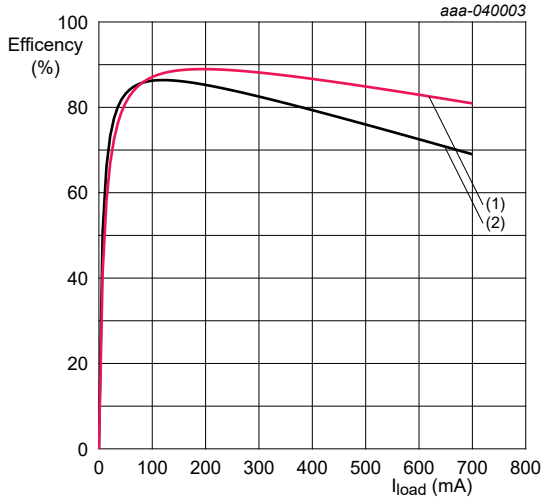
NXF6505B + Wurth 760390013
V_{CC} = 3.3 V

Fig. 28. Efficiency versus load current



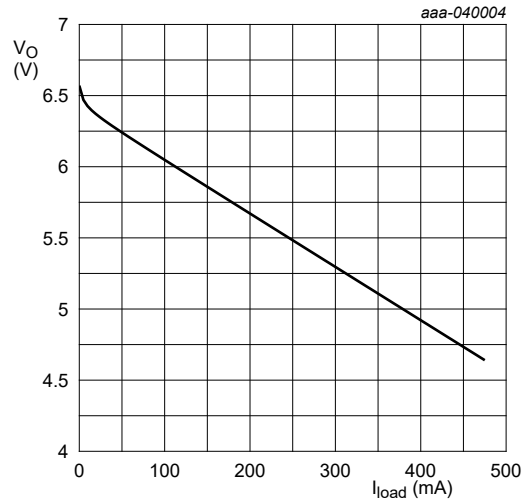
NXF6505B + Wurth 760390014
(1) V_{CC} = 5 V
(2) V_{CC} = 3.3 V

Fig. 29. Output voltage versus load current



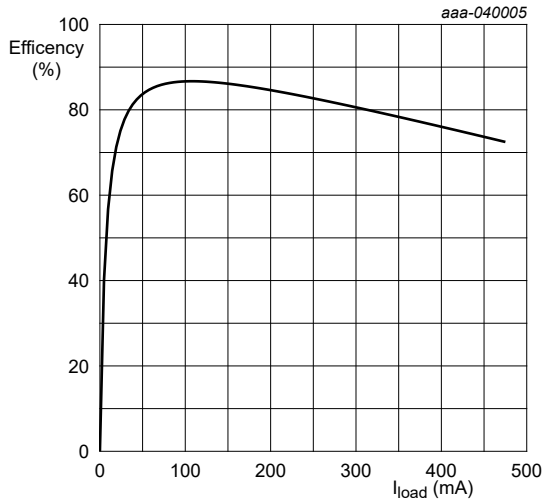
NXF6505B + Wurth 760390014
(1) V_{CC} = 5 V
(2) V_{CC} = 3.3 V

Fig. 30. Efficiency versus load current



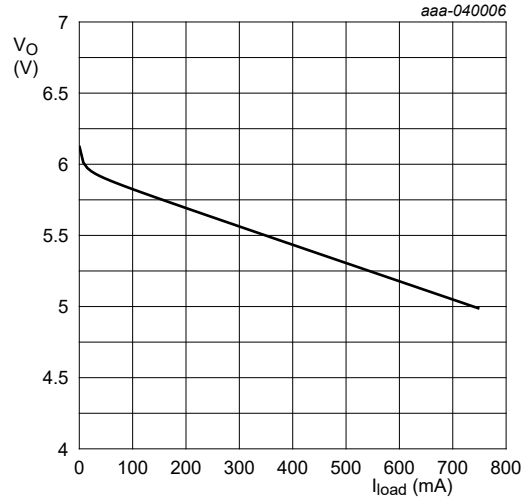
NXF6505B + Wurth 760390015
V_{CC} = 3.3 V

Fig. 31. Output voltage versus load current



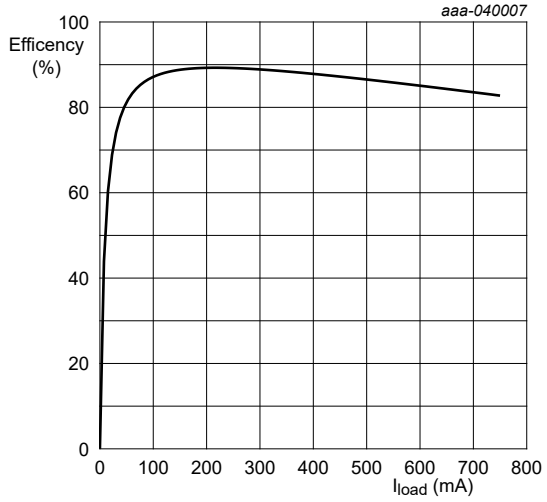
NXF6505B + Wurth 760390015
V_{CC} = 3.3 V

Fig. 32. Efficiency versus load current



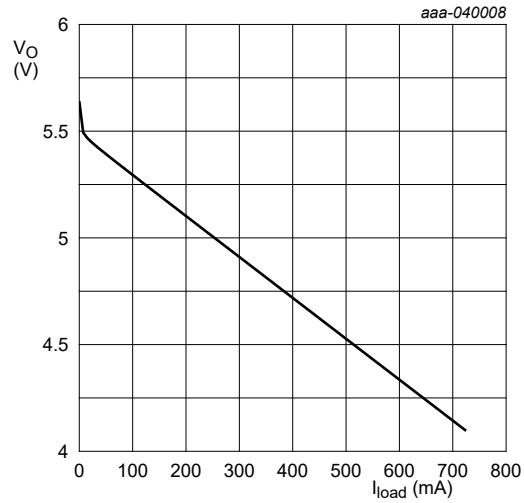
NXF6505B + Wurth 750313710
V_{CC} = 3.3 V

Fig. 33. Output voltage versus load current



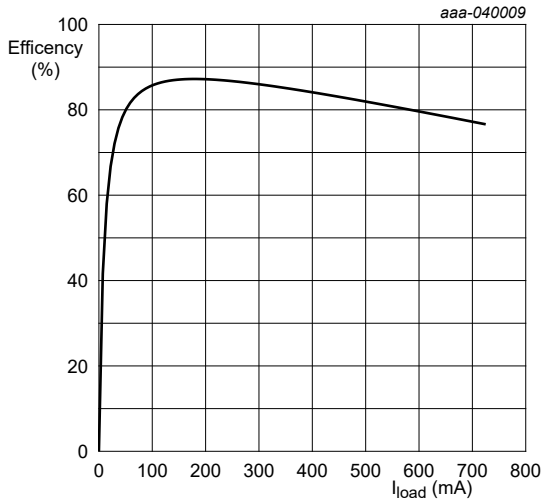
NXF6505B + Wurth 750313710
V_{CC} = 3.3 V

Fig. 34. Efficiency versus load current



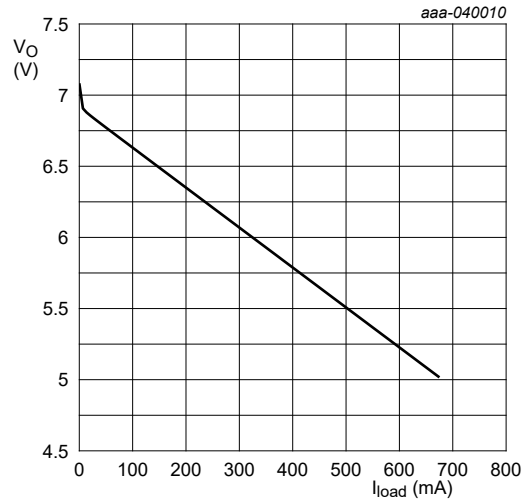
NXF6505B + Wurth 750316028
V_{CC} = 3.3 V

Fig. 35. Output voltage versus load current



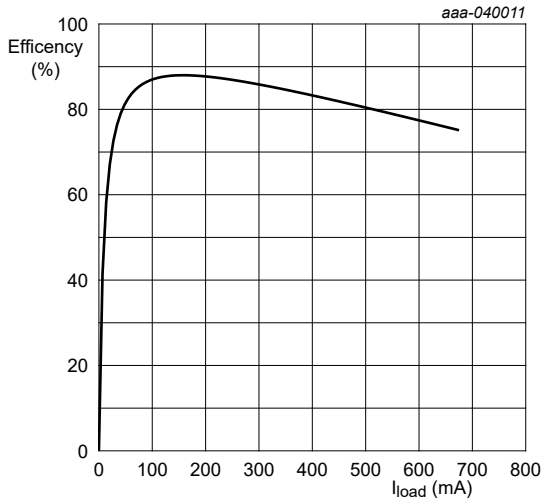
NXF6505B + Wurth 750316028
V_{CC} = 3.3 V

Fig. 36. Efficiency versus load current



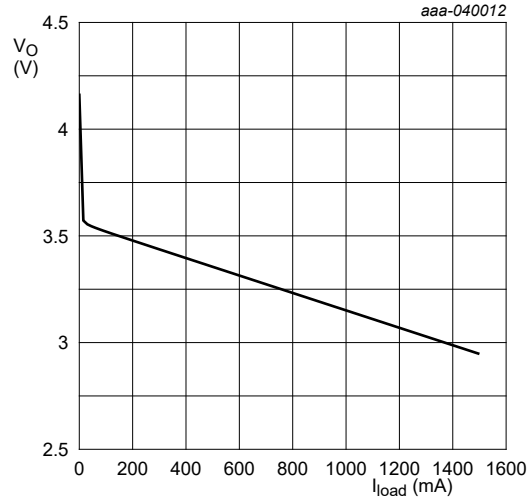
NXF6505B + Wurth 750316029
V_{CC} = 3.3 V

Fig. 37. Output voltage versus load current



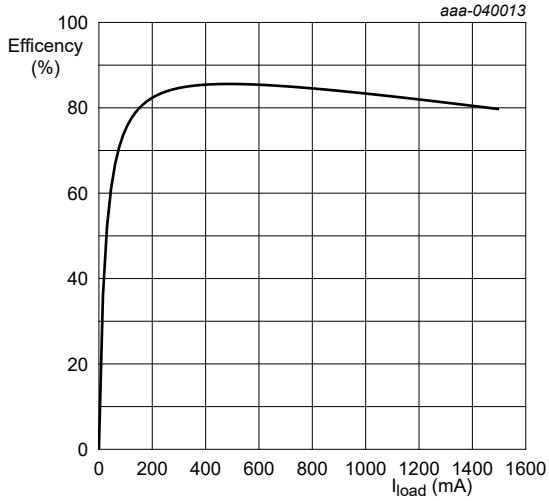
NXF6505B + Wurth 750316029
V_{CC} = 3.3 V

Fig. 38. Efficiency versus load current



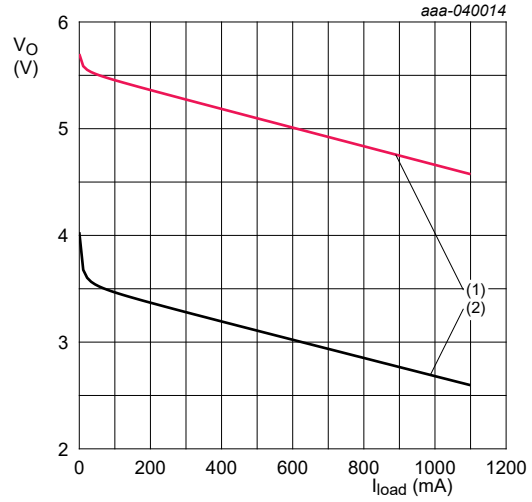
NXF6505B + Wurth 750316030
V_{CC} = 3.3 V

Fig. 39. Output voltage versus load current



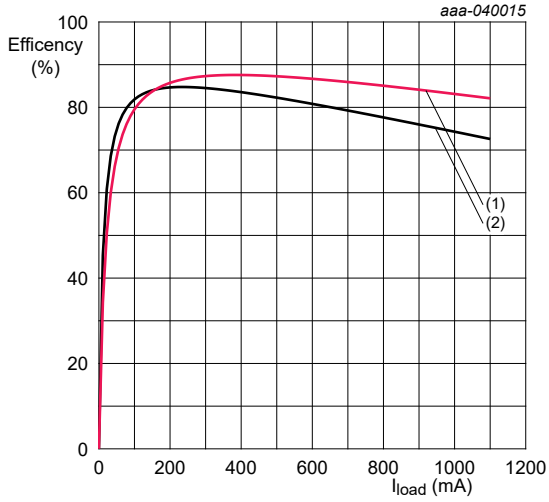
NXF6505B + Wurth 750316030
V_{CC} = 3.3 V

Fig. 40. Efficiency versus load current



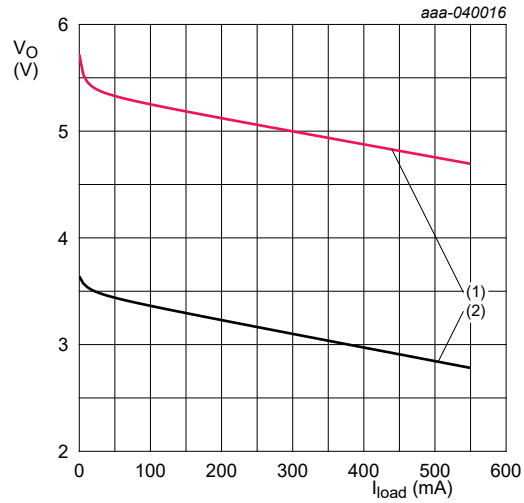
NXF6505B + Wurth 750315371
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 41. Output voltage versus load current



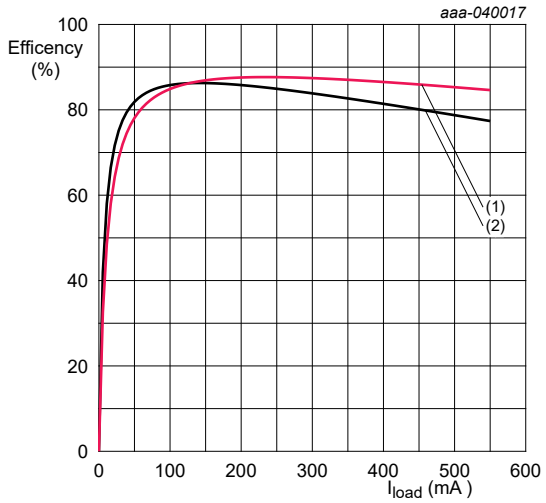
NXF6505B + Wurth 750315371
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 42. Efficiency versus load current



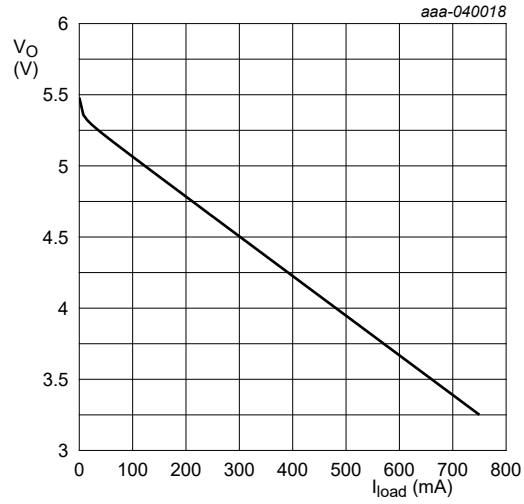
NXF6505B + Wurth 750313734
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 43. Output voltage versus load current



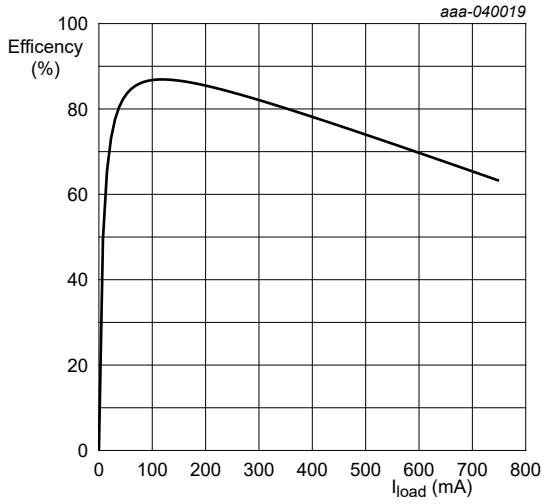
NXF6505B + Wurth 750313734
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 44. Efficiency versus load current



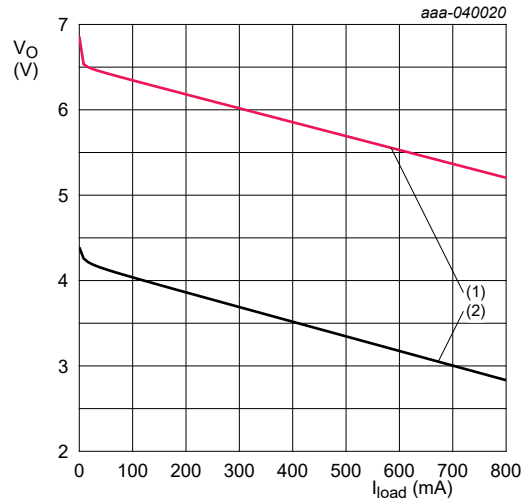
NXF6505B + Wurth 750313769
V_{CC} = 3.3 V

Fig. 45. Output voltage versus load current



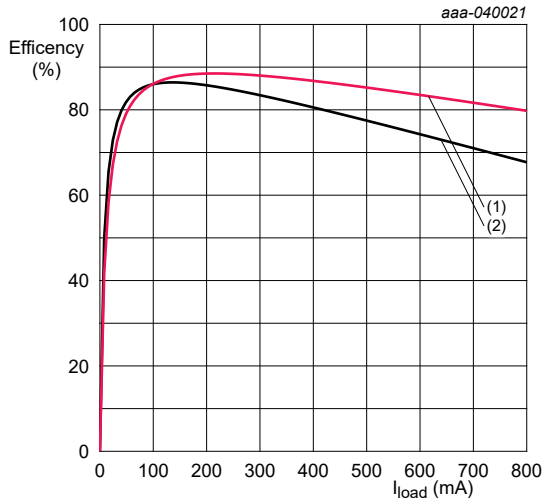
NXF6505B + Wurth 750313769
V_{CC} = 3.3 V

Fig. 46. Efficiency versus load current



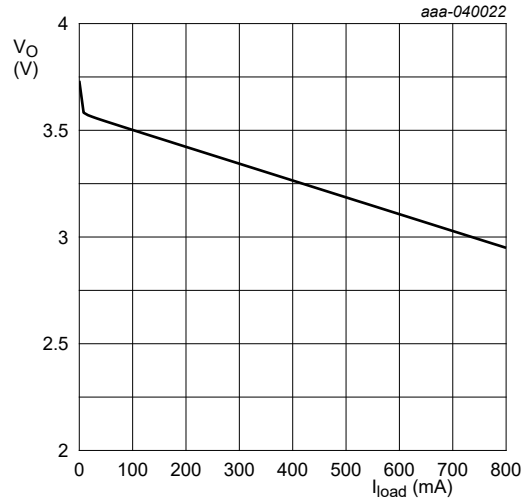
NXF6505B + Wurth 750313638
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 47. Output voltage versus load current



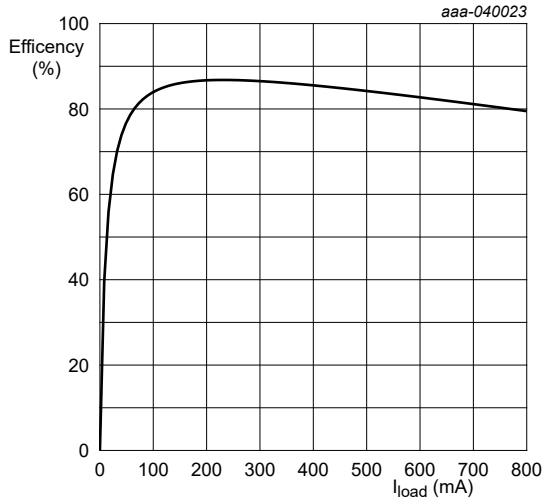
NXF6505B + Wurth 750313638
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 48. Efficiency versus load current



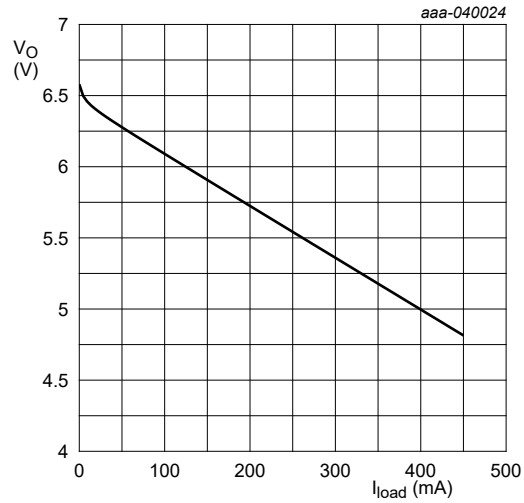
NXF6505B + Wurth 750313638
V_{CC} = 5.5 V

Fig. 49. Output voltage versus load current



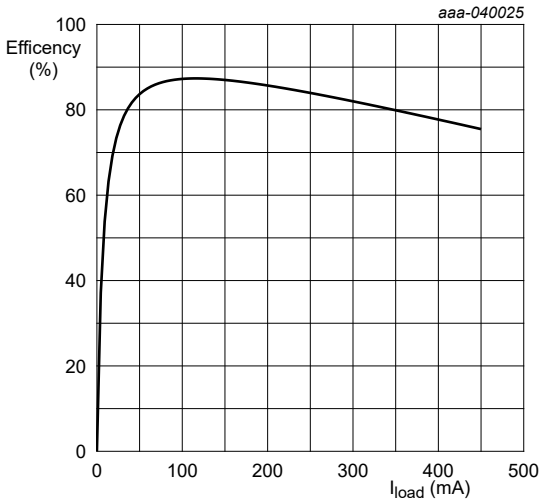
NXF6505B + Wurth 750313638
V_{CC} = 5.5 V

Fig. 50. Efficiency versus load current



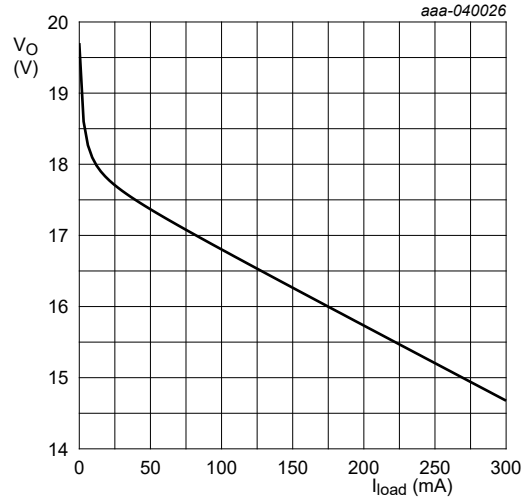
NXF6505B + Wurth 750313626
V_{CC} = 3.3 V

Fig. 51. Output voltage versus load current



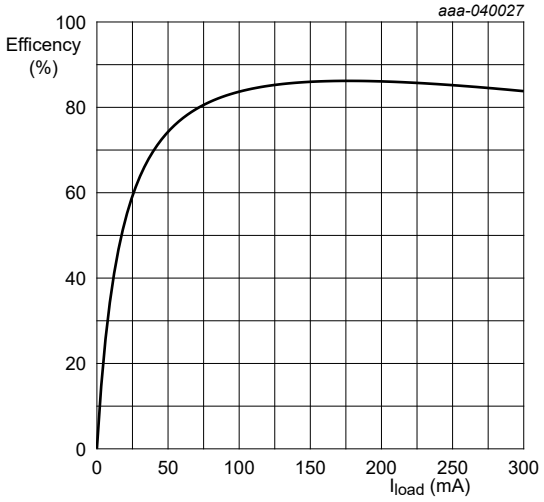
NXF6505B + Wurth 750313626
V_{CC} = 3.3 V

Fig. 52. Efficiency versus load current



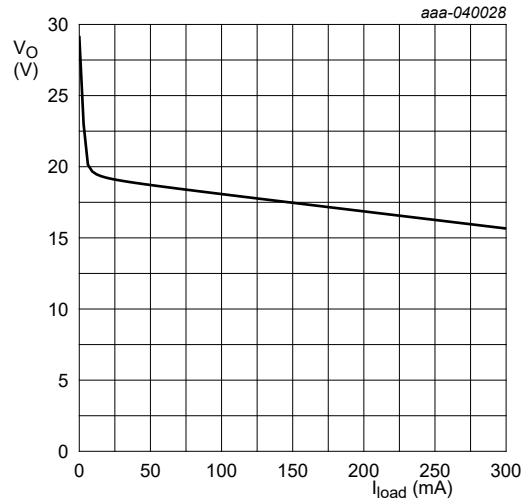
NXF6505B + Wurth 750342879
V_{CC} = 5 V

Fig. 53. Output voltage versus load current



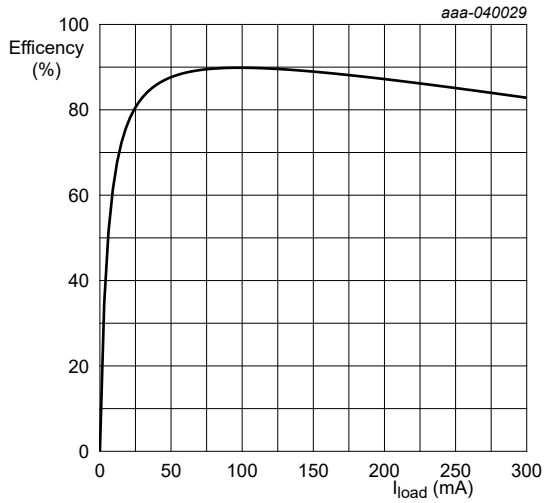
NXF6505B + Wurth 750342879
V_{CC} = 5 V

Fig. 54. Efficiency versus load current



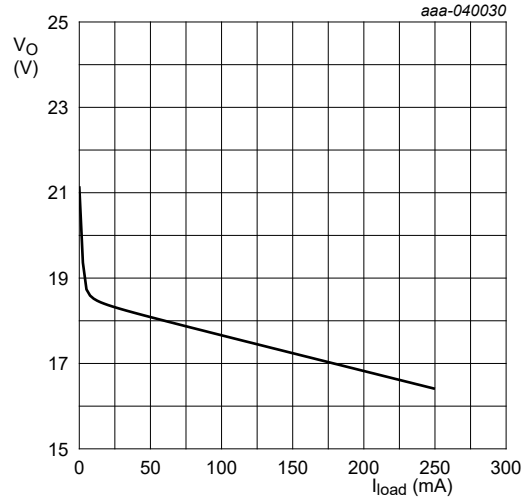
NXF6505B + Wurth 750343725
V_{CC} = 5 V

Fig. 55. Output voltage versus load current



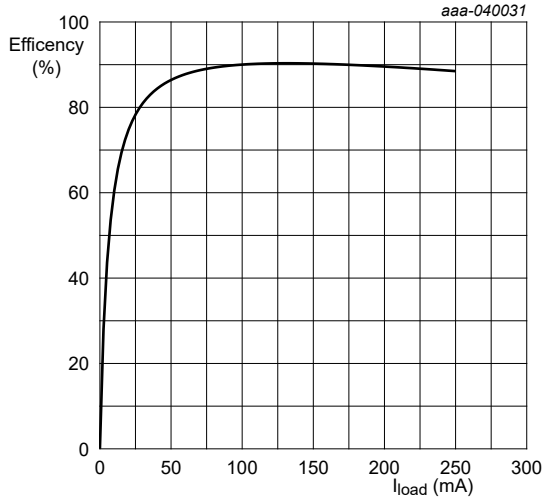
NXF6505B + Wurth 750343725
V_{CC} = 5 V

Fig. 56. Efficiency versus load current



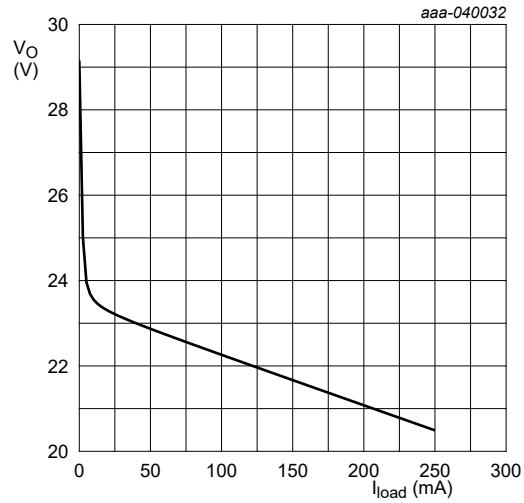
NXF6505B + Wurth 78931812518
V_{CC} = 5 V

Fig. 57. Output voltage versus load current



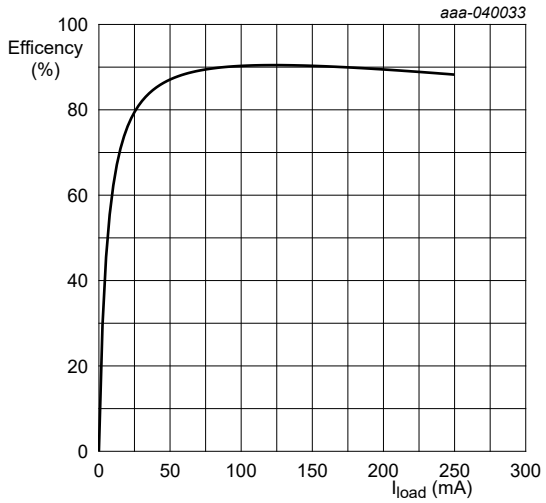
NXF6505B + Wurth 78931812518
V_{CC} = 5 V

Fig. 58. Efficiency versus load current



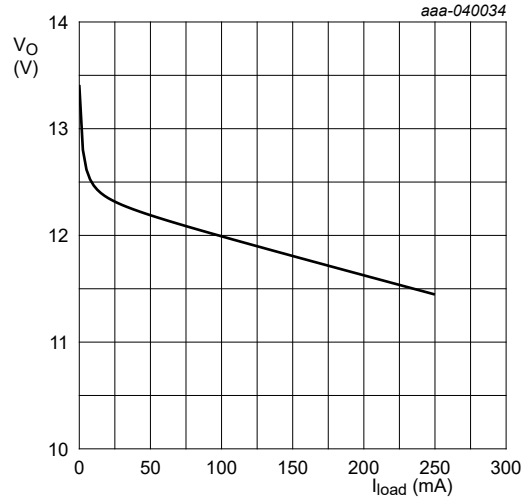
NXF6505B + Wurth 78931812523
V_{CC} = 5 V

Fig. 59. Output voltage versus load current



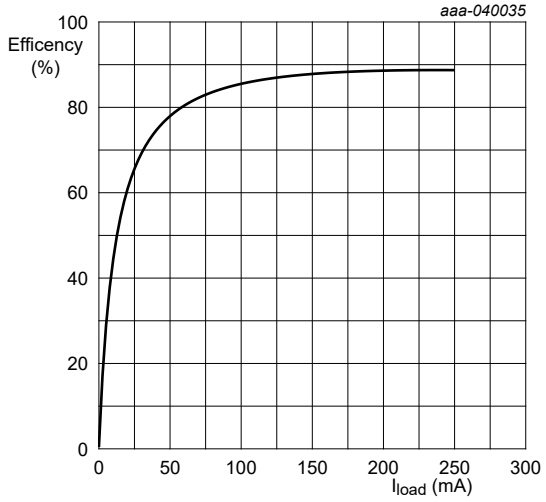
NXF6505B + Wurth 78931812523
V_{CC} = 5 V

Fig. 60. Efficiency versus load current



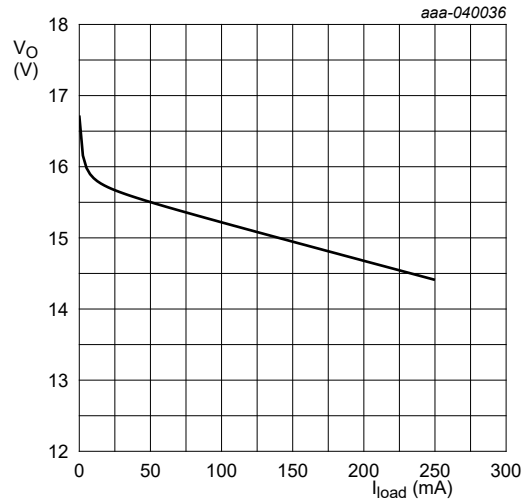
NXF6505B + Wurth 78931812512
V_{CC} = 5 V

Fig. 61. Output voltage versus load current



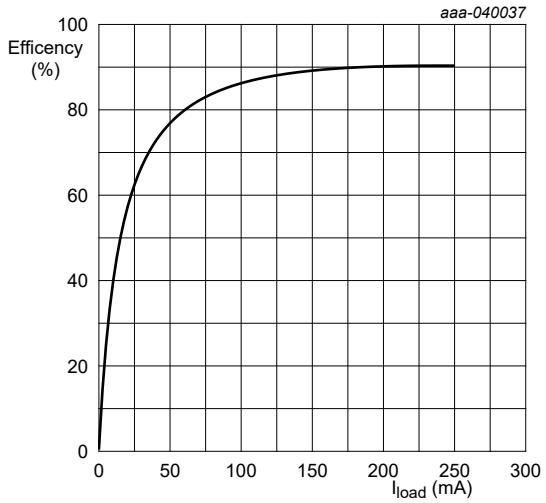
NXF6505B + Wurth 78931812512
V_{CC} = 5 V

Fig. 62. Efficiency versus load current



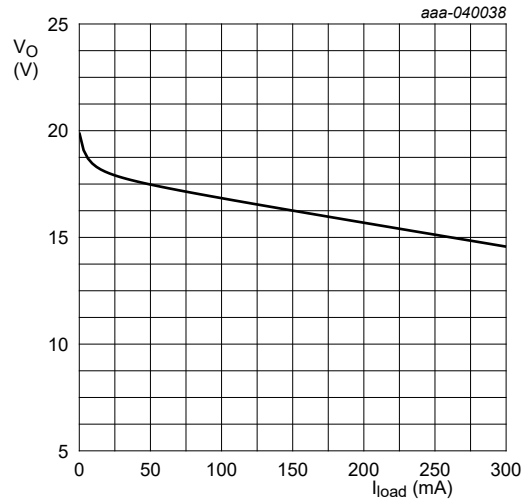
NXF6505B + Wurth 78931812515
V_{CC} = 5 V

Fig. 63. Output voltage versus load current



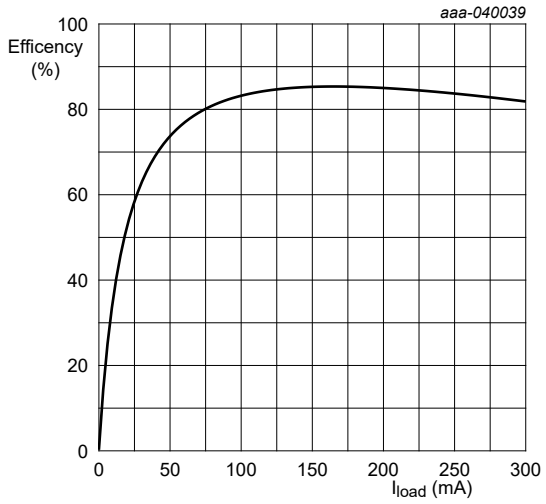
NXF6505B + Wurth 78931812515
V_{CC} = 5 V

Fig. 64. Efficiency versus load current



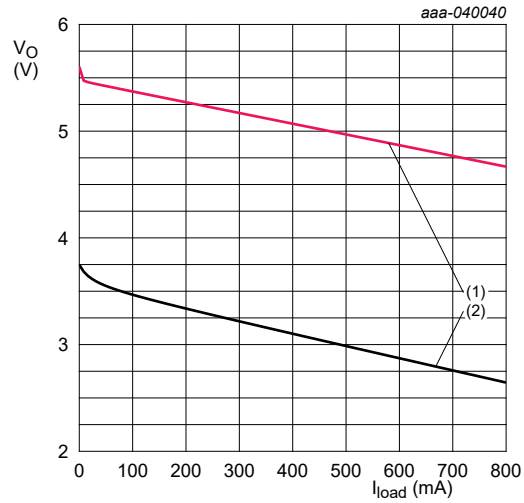
NXF6505B + Wurth 750320340
V_{CC} = 5 V

Fig. 65. Output voltage versus load current



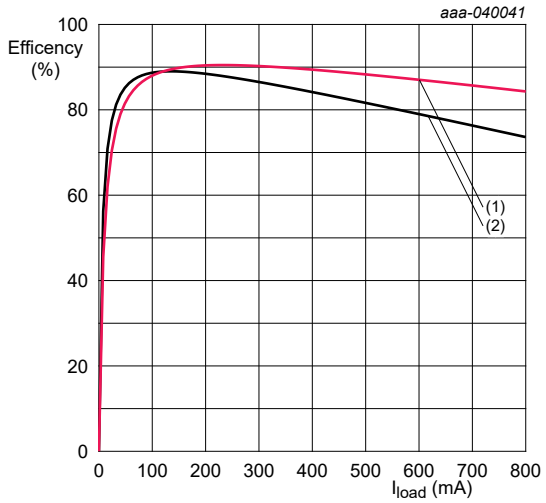
NXF6505B + Wurth 750320340
V_{CC} = 5 V

Fig. 66. Efficiency versus load current



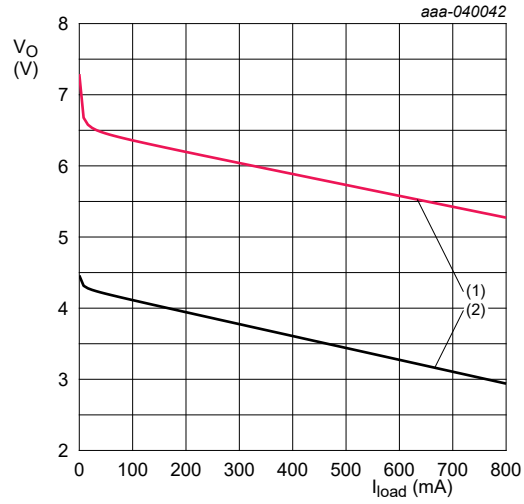
NXF6505B + SunLord ALTWR-H02TF
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 67. Output voltage versus load current



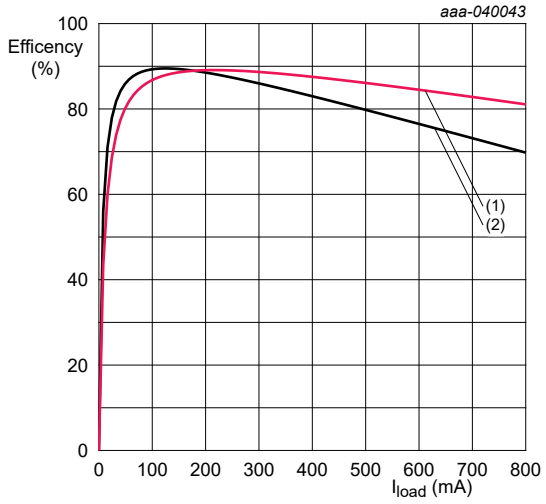
NXF6505B + SunLord ALTWR-H02TF
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 68. Efficiency versus load current



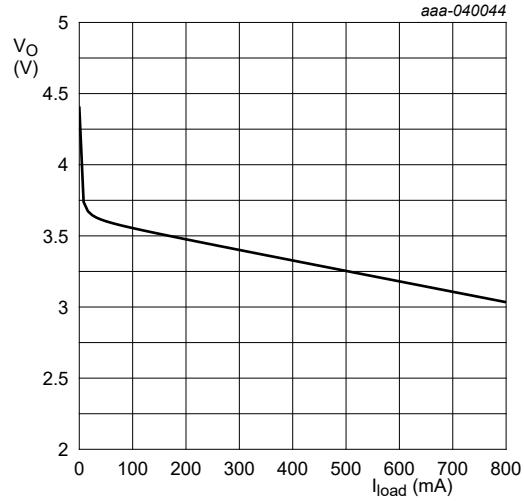
NXF6505B + SunLord ALTWR-H06TF
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 69. Output voltage versus load current



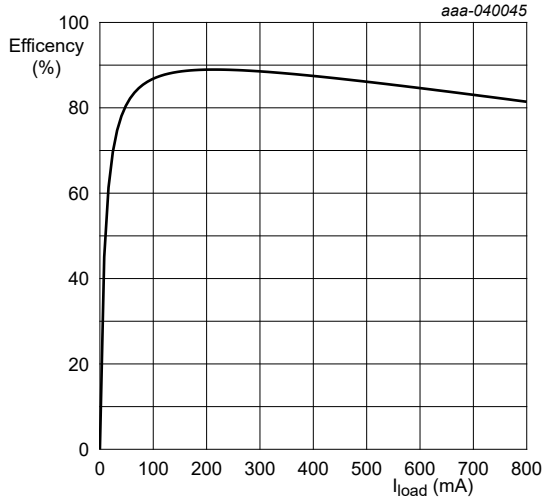
NXF6505B + SunLord ALTWR-H06TF
(1) V_{CC} = 5.5 V
(2) V_{CC} = 3.3 V

Fig. 70. Efficiency versus load current



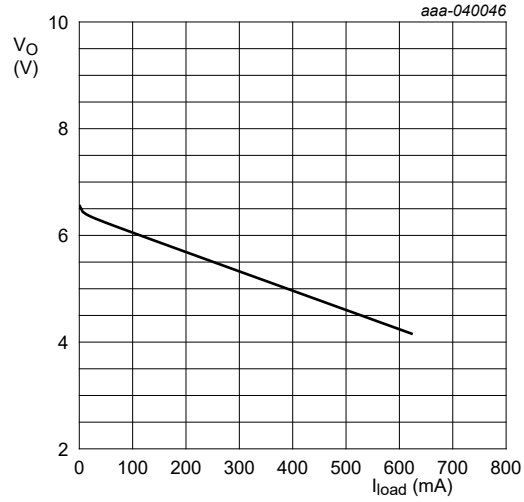
NXF6505B + SunLord ALTWR-H06TF
V_{CC} = 5 V

Fig. 71. Output voltage versus load current



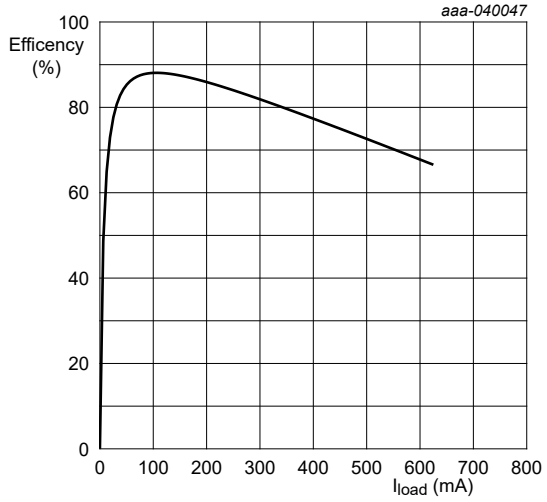
NXF6505B + SunLord ALTWR-H06TF
V_{CC} = 5 V

Fig. 72. Efficiency versus load current



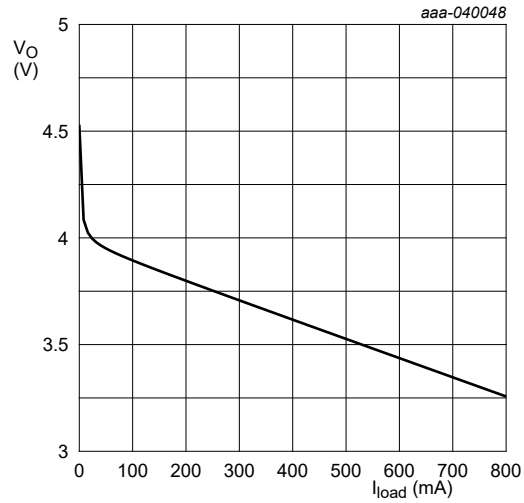
NXF6505B + SunLord ALTWR-H47TF
V_{CC} = 5 V

Fig. 73. Output voltage versus load current



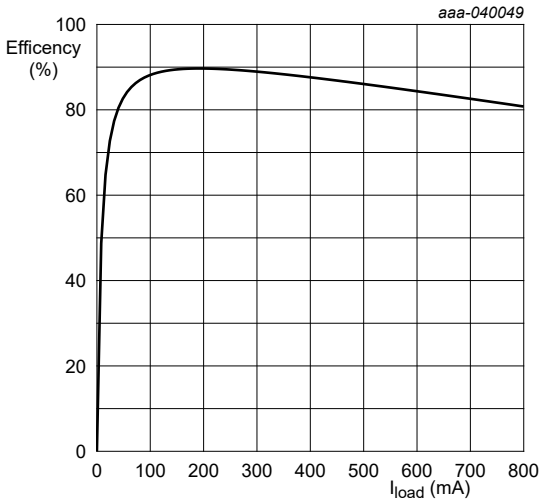
NXF6505B + SunLord ALTWR-H47TF
V_{CC} = 5 V

Fig. 74. Efficiency versus load current



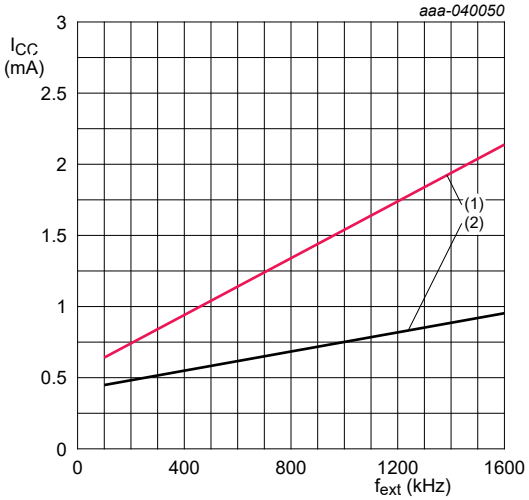
NXF6505B + SunLord ALTWR-H94TF
V_{CC} = 5 V

Fig. 75. Output voltage versus load current



NXF6505B + SunLord ALTWR-H94TF
V_{CC} = 5 V

Fig. 76. Efficiency versus load current



NXF6505B
(1) V_{CC} = 5.5 V; T_{amb} = 25 °C
(2) V_{CC} = 2.25 V; T_{amb} = 25 °C

Fig. 77. Typical supply current versus external frequency

15. Application information

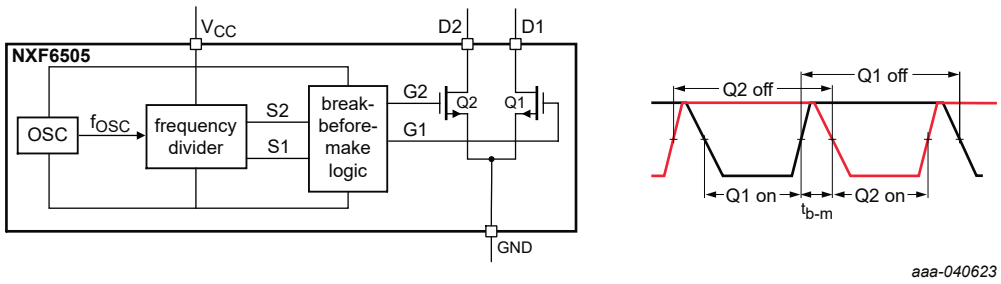


Fig. 78. Block diagram and output timing with break-before-make action

The NXF6505-Q100 is a driver for transformers that has been specifically designed for isolated DC-DC converters with a push-pull topology. It has been created with a focus on being cost-effective and having a small form-factor. The device features an oscillator that is responsible for feeding a gate-drive circuit. The gate-drive circuit consists of a frequency divider and break-before-make (t_{b-m}) logic, which together produce two complementary output signals that switch the output transistors on and off alternately. An asynchronous divider divides the output frequency of the oscillator and provides two complementary output signals, S1 and S2, with a 50% duty cycle. The break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting signals, G1 and G2, provide the gate drive signals for the output transistors Q1 and Q2. In order to prevent shorting out both ends of the primary, both signals must be low and both transistors must be high-impedance during a short time period before either one of the gates can assume logic high. This brief interval is known as the break-before-make time and is illustrated in Fig. 78.

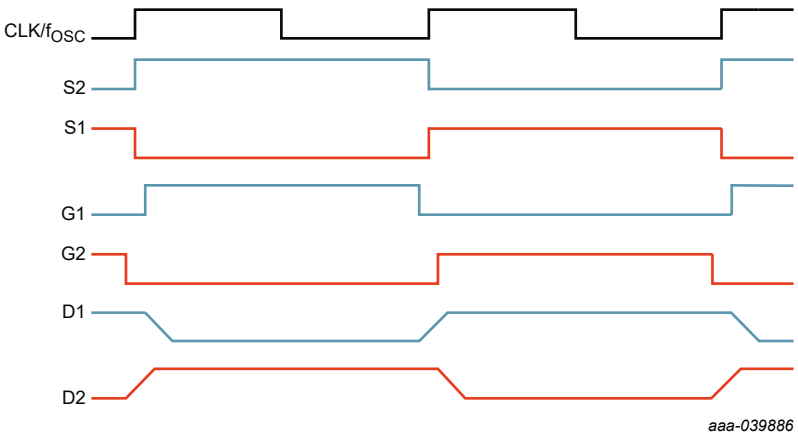


Fig. 79. Output signal waveforms

15.1. Typical Application

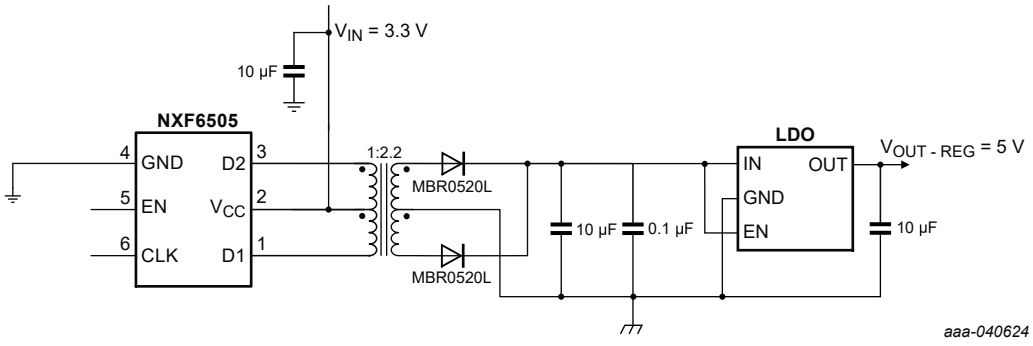


Fig. 80. NXF6505-Q100 typical application schematic

Design requirements

For this design example, use the parameters listed in Table 10 as design parameters.

Table 10. Design parameters

Parameters	Values
Input voltage range	3.3 V ± 3%
Output voltage	5 V
Maximum load current	100 mA

Detailed design procedure

These guidelines for selecting components are focused on creating a push-pull converter that is efficient and capable of handling high current drive. It's important to note that the output voltage of an unregulated converter drops significantly across a wide range of load currents. Fig. 10 and Fig. 16 illustrate this characteristic curve, which demonstrates that the voltage difference between minimum and maximum loads exceeds the range of a transceiver's supply. To ensure a stable, load-independent power supply while maximizing efficiency, we strongly recommend implementing a low dropout regulator (LDO). Fig. 80 depicts the final converter circuit, and Fig. 41 and Fig. 42 display the measured output voltage and efficiency characteristics for both regulated and unregulated outputs.

Drive capability

The transformer driver is intended for low-power push-pull converters that have input and output voltages ranging from 2.25 V to 5.5 V. Although it's feasible to create converter designs with higher output voltages, it's important to exercise caution to prevent primary currents from exceeding the device's specified current limits when using higher turns ratios.

Diode selection

To maximize the voltage output of a converter, it's important for a rectifier diode to have low-forward voltage. In high-frequency switching applications like the NXF6505-Q100, a diode with a short recovery time is also necessary. Schottky diodes fulfill both requirements and are highly recommended for push-pull converter designs. For low-voltage applications with ambient temperatures up to 85 °C, the affordable MBR0520L Schottky rectifier is a great option with a typical forward voltage of 275 mV at 100 mA forward current. If higher output voltages such as ±10 V are needed, the MBR0530 is a better choice with a higher DC blocking voltage of 30 V. However, lab tests have shown that at temperatures above 100 °C, the above Schottky diodes experience a significant increase in leakage currents. This can cause thermal runaway and the output voltage of the rectifier to collapse. To prevent this, use low-leakage Schottky diodes like RB168MM-40 for ambient temperatures exceeding 85 °C.

Capacitor selection

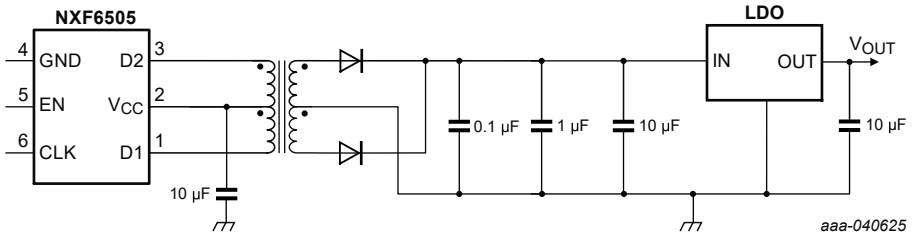


Fig. 81. Regulated output for stable supplies and high current load

The converter circuit shown in Fig. 81 employs multi-layer ceramic chip (MLCC) capacitors as its capacitors. For proper functioning of the high-speed CMOS ICs, a bypass capacitor within 10 nF to 100 nF range is required. The input bulk capacitor, located at the center-tap of the primary, is responsible for supporting high currents during fast switching transients. For minimal ripple, it is recommended to use a 1 µF to 10 µF capacitor. In a 2-layer PCB design with a dedicated ground plane, this capacitor should be positioned near the primary center-tap to reduce trace inductance. In a 4-layer board design, where low-inductance reference planes are available for ground and V_{IN}, the capacitor can be placed at the entrance of

the board. Two parallel vias should be used to ensure low-inductance paths for each connection to a reference plane or to the primary center-tap. To smooth out the output voltage, a bulk capacitor should be placed at the rectifier output. A capacitor with a value of 1 µF to 10 µF is recommended. Although not always necessary, using a small capacitor with a value of 47 nF to 100 nF at the regulator input can improve the regulator's transient response and noise rejection. The LDO output capacitor is used to buffer the regulated output for subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements, as stated in the data sheet. However, in most cases, a low-ESR ceramic capacitor within the 4.7 µF to 10 µF range is sufficient to meet these requirements.

Transformer selection

In order to avoid transformer saturation, the V-t product should exceed the highest V-t product generated by the device. The device's maximum voltage output is determined by adding 10% to the nominal converter input. The primary voltage should not exceed this maximum value for more than half the period of the lowest frequency specified for the input voltage. As a result, the minimum V-t product required for the transformer can be calculated by:

$$V \times t_{min} \geq V_{IN\text{-}max} \times \frac{T_{max}}{2} = \frac{V_{IN\text{-}max}}{2 \times f_{min}}$$

Equation 1

Assuming a 5 V supply, and considering the values of f_{min} as 139 kHz for NXF6505A-Q100 and 374 kHz for NXF6505B-Q100, the minimum V-t products can be obtained by applying the equation above, resulting in:

$$V \times t_{min} \geq \frac{5.5\,V}{2 \times 139\,kHz} = 19.7\ V\mu s$$ for NXF6505A-Q100, and

$$V \times t_{min} \geq \frac{5.5\,V}{2 \times 374\,kHz} = 7.3\ V\mu s$$ for NXF6505B-Q100.

Low-power center-tapped transformers typically have common V-t values that fall within the range of 22 Vµs to 150 Vµs, and they usually have a standard footprint size of 10 mm x 12 mm. However, for transformers specifically intended for PCMCIA applications, V-t values as low as 6 Vµs can be obtained, and their footprint is significantly smaller at 6 mm x 6 mm. While the device can drive any of these transformers in terms of V-t values, there are other critical factors that must be taken into account before deciding on the most suitable transformer, such as isolation voltage, transformer wattage, and turns ratio.

Table 11. Recommended isolation transformers optimized for the NXF0506-Q100

Turns ratio	VxT Vμs	Isolation V_{RMS}	Dimensions (mm)	Application	LDO[1]	Order no.	Manufactuer
1:1.1 ±2%	7	2500	6.73x10.05x4.19	3.3 V → 3.3 V, 100 mA, NXF6505B; see Fig. 23 and Fig. 24	No	760390011	Wurth Electronics/ Midcom
1:1.1 ±2%	11			5V → 5 V, 750 mA, NXF6505B; see Fig. 25 and Fig. 26		760390012	
1:1.7 ±2%				3.3 V → 5 V, 500 mA, NXF6505B; see Fig. 27 and Fig. 28		760390013	
1:1.3 ±2%				3.3 V → 3.3 V, 600 mA, NXF6505B; see Fig. 29 and Fig. 30	Yes	760390014	
1:1.3 ±2%				5 V → 5 V, 600 mA, NXF6505B; see Fig. 31 and Fig. 32		760390014	
1:2.1 ±2%				3.3V → 5 V, 450 mA, NXF6505B; see Fig. 31 and Fig. 32		760390015	
1.23:1±2%				5 V → 3.3 V, 650 mA, NXF6505B; see Fig. 33 and Fig. 34		750313710	
1:1.7 ±2%	8.9		8.3x12.6x4.1	3.3 V → 3.3 V, 800 mA, NXF6505B; see Fig. 35 and Fig. 36		750316028	
1:2.1 ±2%				3.3 V → 5 V, 600 mA, NXF6505B; see Fig. 37 and Fig. 38	No	750316029	
1.3:1 ±2%	10.8			5 V → 3.3 V, 1.2 A, NXF6505B; see Fig. 39 and Fig. 40		750316030	
1:1.1 ±2%	8.6			3.3 V → 3.3 V, 1 A, NXF6505B; 5 V → 5 V, 1 A, NXF6505B; see Fig. 41 and Fig. 42		750315371	
1:1.1 ±2%	11	5000	9.14x12.7x7.37	3.3 V → 3.3 V, 800 mA, NXF6505B; see Fig. 43 and Fig. 44		750313734	
1:1.1 ±2%				5 V → 5 V, 600 mA, NXF6505B; see Fig. 43 and Fig. 44		750313734	
1:1.7 ±2%				3.3 V → 5 V, 600 mA, NXF6505B; see Fig. 45 and Fig. 46		750313769	
1:1.3 ±2%				3.3 V → 3.3 V, 650 mA, NXF6505B 5 V → 5 V, 100 mA, NXF6505B; see Fig. 47 and Fig. 48	Yes	750313638	
1:2.1 ±2%				3.3 V → 5 V, 500 mA, NXF6505B; see Fig. 51 and Fig. 52		750313626	
1.3:1 ±2%				5 V → 3.3 V, 650 mA , NXF6505B; see Fig. 49 and Fig. 50	No	750313638	
1:1.75±2%	41		12.32x15.41x11.05	3.3 V → 3.3 V, 1 A, NXF6505A; see Fig. 10 and Fig. 11	Yes	750316031	
1:2±2%				3.3 V → 5 V, 1 A, NXF6505A; see Fig. 12 and Fig. 13	No	750316032	
1.3:1 ±2%	42			5.0 V → 3.3 V, 1 A, NXF6505A; see Fig. 14 and Fig. 15		750316033	
1:1.1 ±2%	23		12.32x15.41x11.89	3.3 V → 3.3 V, 1 A, NXF6505A; 5 V → 5 V, 1 A, NXF6505A; see Fig. 16 and Fig. 17		750315240	
1:1.3 ±3%	11	5000	10.4x12.2x6.1	3.3 V → 3.3 V, 300 mA, NXF6505B 5 V → 5 V, 300 mA, NXF6505B	No	HCT-SM-1.3-8-2	Bourns
1:1.1 ±2%	9.2	2500	7.01x11x4.19	3.3 V → 3.3 V, 150 mA, NXF6505B 5 V → 5 V, 150 mA, NXF6505B	No	EPC3668G-LF	PCA Electronics

Turns ratio	VxT Vμs	Isolation V_{RMS}	Dimensions (mm)	Application	LDO[1]	Order no.	Manufactuer
1:1.3 ±5%	18	5000	12.5 x 9.2 x 7.6	3.3 V → 3.3 V, 600 mA, NXF6505A	Yes	ALTWR-H09TF	SunLord
1:2 ±5%	11	5000	12.5 x 9.2 x 7.6	3.3 V → 5 V, 600 mA, NXF6505A; see Fig. 18 and Fig. 19	Yes	ALTWR-H47TF	
11:9 ±5%	16	5000	12.5 x 9.2 x 7.6	5 V → 3.3 V, 600 mA, NXF6505A; see Fig. 20 and Fig. 21	Yes	ALTWR-H94TF	
1:1.3 ±5%	18	5000	12.5 x 9.2 x 7.6	5 V → 5 V, 600 mA, NXF6505A	Yes	ALTWR-H09TF	
3:4 ±5%	10	5000	12.5 x 9.2 x 7.6	3.3 V → 3.3 V, 600 mA, NXF6505B; see Fig. 69 and Fig. 70	Yes	ALTWR-H06TF	
1:2 ±5%	11	5000	12.5 x 9.2 x 7.6	3.3 V → 5 V, 600 mA, NXF6505B	Yes	ALTWR-H47TF	
11:9 ±5%	16	5000	12.5 x 9.2 x 7.6	5 V → 3.3 V, 600 mA, NXF6505B	Yes	ALTWR-H94TF	
3:4 ±5%	10	5000	12.5 x 9.2 x 7.6	5 V → 5 V, 600 mA, NXF6505B; see Fig. 71 and Fig. 72	Yes	ALTWR-H06TF	
1:1.1 ±5%	15	5000	12.5 x 9.2 x 7.6	3.3 V → 3.3 V, 600 mA, NXF6505A	No	ALTWR-H33TF	
1:1.55 ±5%	13	5000	12.5 x 9.2 x 7.6	3.3 V → 5 V, 600 mA, NXF6505A	No	ALTWR-H61TF	
1.3:1 ±5%	18	5000	12.5 x 9.2 x 7.6	5 V → 3.3 V, 600 mA, NXF6505A	No	ALTWR-H95TF	
1:1.1 ±5%	15	5000	12.5 x 9.2 x 7.6	5 V → 5 V, 600 mA, NXF6505A	No	ALTWR-H33TF	
8:9 ±5%	11	5000	12.5 x 9.2 x 7.6	3.3 V → 3.3 V, 600 mA, NXF6505B	No	ALTWR-H02TF	
1:1.55 ±5%	13	5000	12.5 x 9.2 x 7.6	3.3 V → 5 V, 600 mA, NXF6505B	No	ALTWR-H61TF	
3:4 ±5%	10	5000	12.5 x 9.2 x 7.6	5 V → 3.3 V, 600 mA, NXF6505B	No	ALTWR-H06TF	
8:9 ±5%	11	5000	12.5 x 9.2 x 7.6	5 V → 5 V, , 600 mA, NXF6505B	No	ALTWR-H02TF	
1:1.5 ±3%	34.4	2500	10x12.07x5.97	3.3 V → 3.3 V, 1 A, NXF6505A/B 5 V → 5 V, 1 A, NXF6505A/B	Yes	DA2303-AL	Coilcraft
1:2.2 ±3%	21.5	2500	10x12.07x5.97	3.3 V → 5 V, 1 A, NXF6505A/B		DA2304-AL	

[1] For configurations with LDO, a higher voltage than the required output voltage is generated, to allow for LDO drop-out.

15.2. Power supply recommendations

The equipment is intended to function within a range of input voltage supply between 2.5 V and 5 V nominal, which requires regulation within ±10 %. When the input supply is situated farther than a few inches from the device, it is advisable to connect a 0.1 µF by-pass capacitor as near as possible to the device's V_{CC} pin, and a 10 µF capacitor near the transformer center-tap pin.

15.3. Layout guidelines

To ensure proper functioning, the V_{IN} pin requires a low-ESR ceramic bypass-capacitor, with a recommended capacitor value ranging from 1 µF to 10 µF. The capacitor should have a voltage rating of at least 10 V and use X5R or X7R dielectric material.

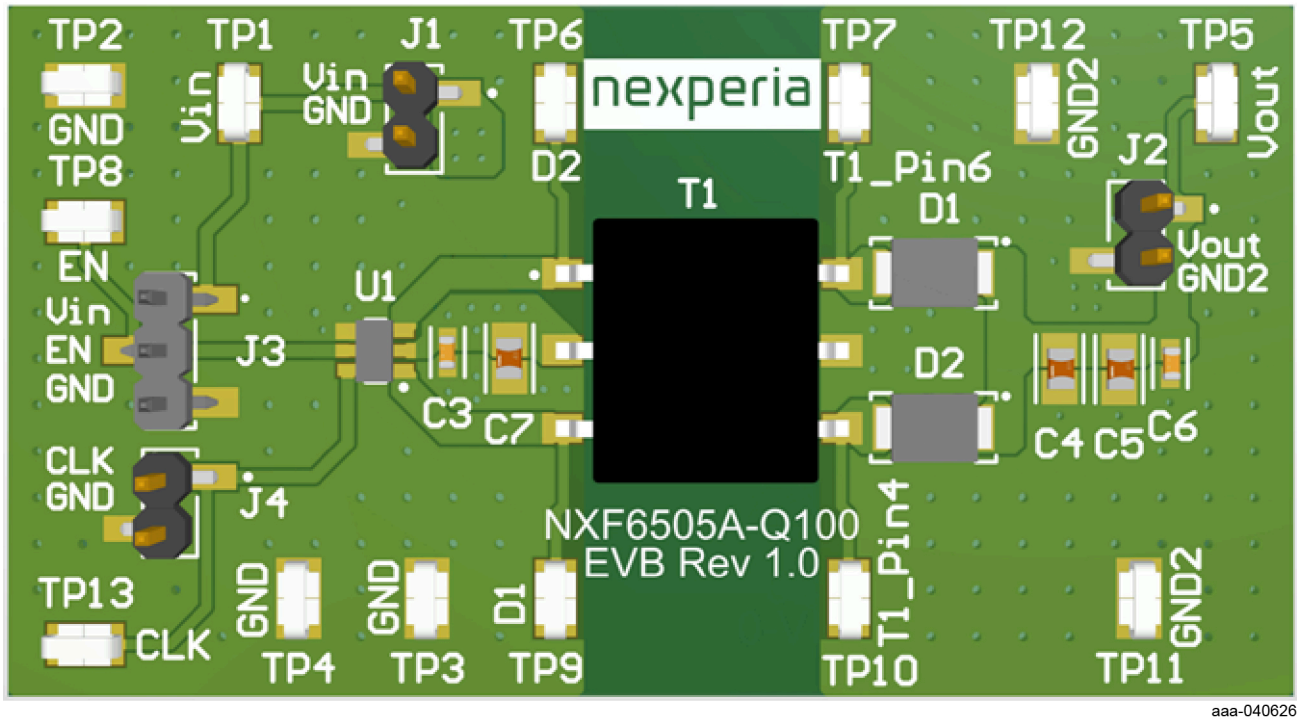
The optimal placement for the capacitor is closest to the V_{IN} and GND pins at the board entrance, minimizing the loop area formed by the bypass-capacitor connection, the V_{IN} terminal, and the GND pin, as demonstrated in Fig. 82 of the PCB layout example.

Furthermore, the connections between the device's D1 and D2 pins and the transformer primary endings, and the connection of the device V_{CC} pin and the transformer center-tap should be as close as possible to minimize trace inductance.

The device V_{CC} pin and transformer center-tap should be buffered to ground using a low-ESR ceramic bypass-capacitor with a recommended capacitor value ranging from 1 µF to 10 µF. The capacitor should have a voltage rating of at least 16 V and use X5R or X7R dielectric material.

Additionally, the device GND pins must be tied to the PCB ground plane using at least two vias to minimize inductance. The ground connections of the capacitors and the ground plane should also use at least two vias for the same reason.

Finally, the V_{OUT} pin also requires buffering to ISO-Ground with a low-ESR ceramic bypass-capacitor, with a recommended capacitor value ranging from 1 µF to 10 µF. The capacitor should have a voltage rating of at least 16 V and use X5R or X7R dielectric material.

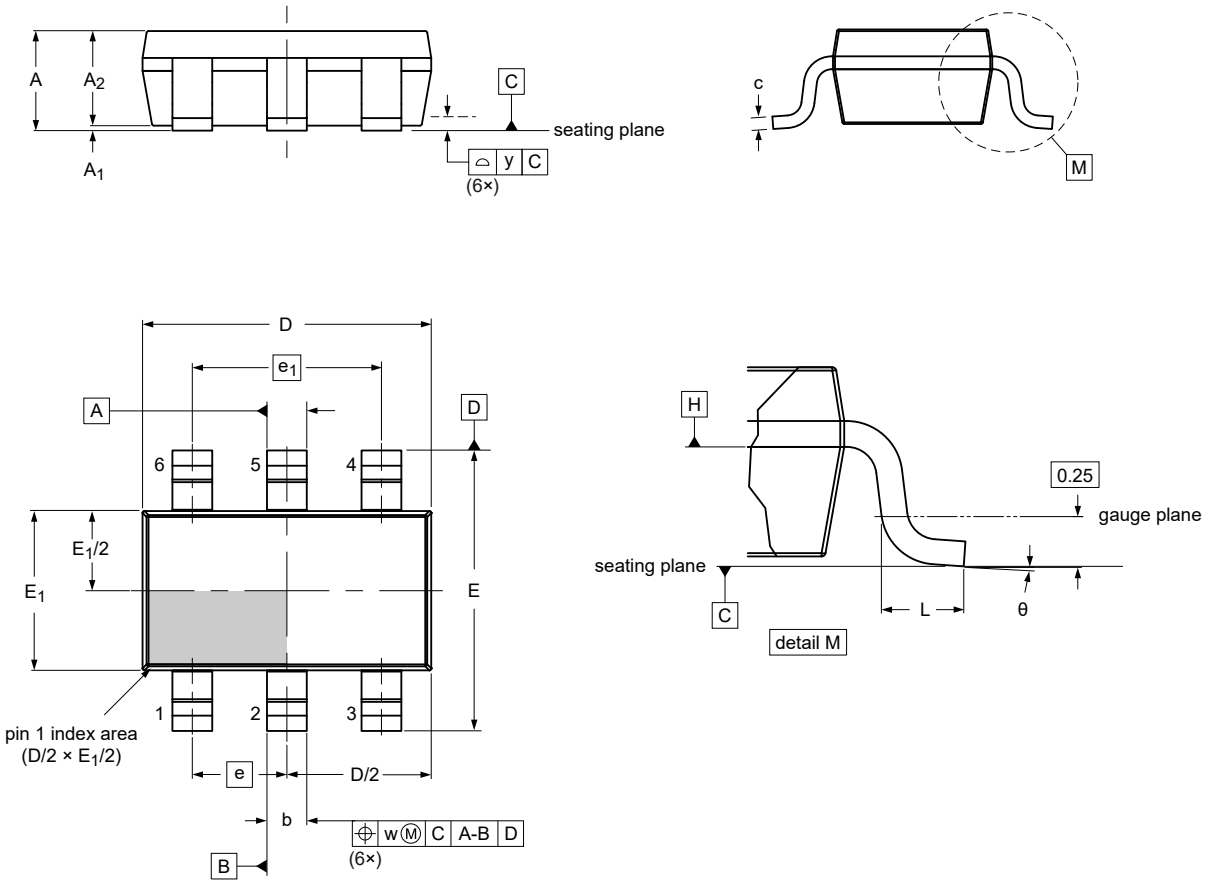


aaa-040626

Fig. 82. Layout example

16. Package outline

Plastic, surface-mounted package (TSOT23-6); 6 leads **SOT8061-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	e_1	L	y	w	θ
mm	max	1.10	0.10	1.00	0.50	0.20	3.05	3.00	1.75	0.95 BSC	1.90 BSC	0.60	0.10	0.20	8°
	nom						2.90	2.80	1.60						
	min		0.00	0.70	0.30	0.08	2.75	2.60	1.45			0.30			0°

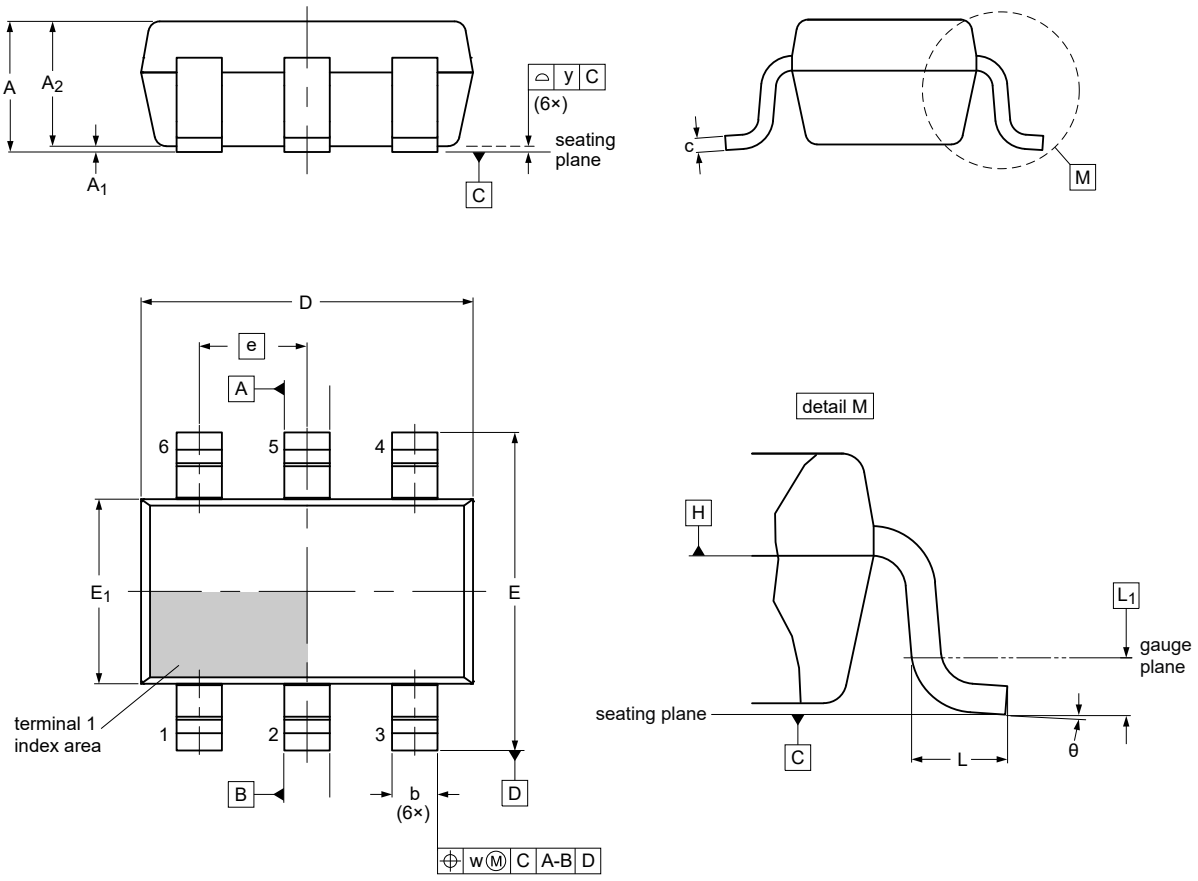
Note
Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per end.
Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0. 25 mm per side.
D and E_1 dimensions are determined at datum H.

sot8061-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8061-1		MO-193				~~24-09-04~~ 24-09-16

Fig. 83. Package outline SOT8061-1 (TSOT23-6)

plastic, SOT23-6, 6 pins; 0.95 mm pitch; 2.9 mm x 1.6 mm x 1.45mm body **SOT8120-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	L	L_1	y	w	θ
mm	max	1.45	0.15	1.30	0.50	0.20	3.05	3.00	1.75	0.95 BSC	0.55	0.25 BSC	0.10	0.20	8°
	nom						2.90	2.80	1.60						
	min	0.90	0.00	0.90	0.30	0.14	2.75	2.60	1.45		0.30				0°

Note
1. Dimension D does not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burr shall not exceed 0.25 mm per end. Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side. D and E_1 dimensions are determined at datum H.
2. Datums A and B to be determined at datum H.

sot8120-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8120-1		MO-178				25-05-06

Fig. 84. Package outline SOT8120-1 (LSOT6)

17. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
EMI	Electromagnetic Interference
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
UVLO	Undervoltage Lockout
SSC	Spread Spectrum Clocking
HBM	Human Body Model
ESD	ElectroStatic Discharge
MLCC	Multi-Layer Ceramic Capacitors

18. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXF6505_Q100 v.2	20250822	Product data sheet	-	NXF6505_Q100 v.1
Modifications:	• Type number NXF6505ADM-Q100/G and NXF6505BDM-Q100/G (SOT8120-1/LSOT6) added. • Section 9: The $I_{O(peak)(max)}$ value has changed.			
NXF6505_Q100 v.1	20240917	Product data sheet	-	-

19. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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