

Si/SiC Hybrid Modules – EliteSiC, Dual Boost, 1200 V, 50 A IGBT + 1200 V, 20 A SiC Diode, Q0 Package

NXH100B120H3Q0, NXH100B120H3Q0PG-R

The NXH100B120H3Q0 is a power module containing a dual boost stage. The integrated field stop trench IGBTs and SiC Diodes provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- 1200 V Ultra Field Stop IGBTs
- Low Reverse Recovery and Fast Switching SiC Diodes
- 1600 V Bypass and Anti-parallel Diodes
- Low Inductive Layout
- Solderable Pins or Press-Fit Pins
- Thermistor
- Options with Pre-Applied Thermal Interface Material (TIM) and Without Pre-Applied TIM

Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Energy Storage Systems

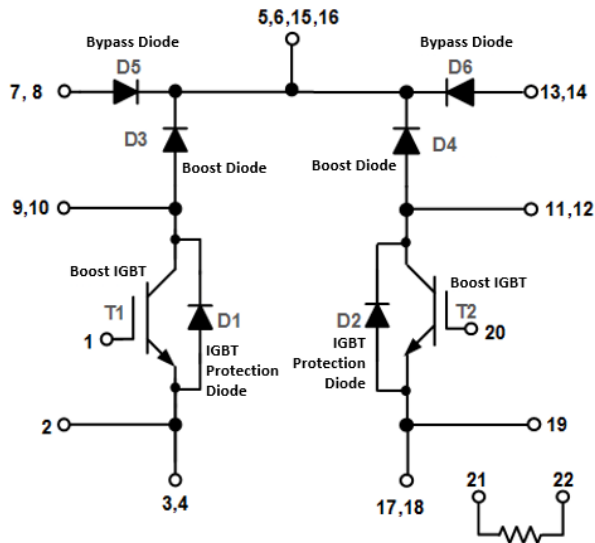
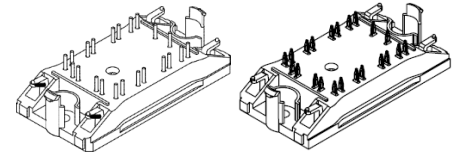


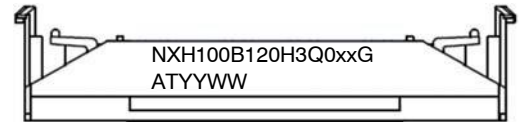
Figure 1. NXH100B120H3Q0xG/PG-R Schematic Diagram



Q0BOOST
CASE 180AJ
SOLDER PINS

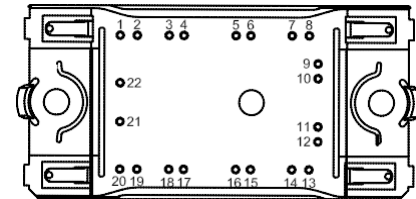
Q0BOOST
CASE 180BF
PRESS-FIT PINS

MARKING DIAGRAM



- xx = P, PT, S or ST
- YYWW = Year and Work Week Code
- A = Assembly Site Code
- T = Test Site Code
- G = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

NXH100B120H3Q0, NXH100B120H3Q0PG-R

ABSOLUTE MAXIMUM RATINGS (Note 1) $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Rating	Symbol	Value	Unit
BOOST IGBT			
Collector–Emitter Voltage	V_{CES}	1200	V
Gate–Emitter Voltage	V_{GE}	± 20	V
Continuous Collector Current @ $T_C < 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_{C1}	61	A
Continuous Collector Current @ $T_C < 102^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_{C2}	50	A
Pulsed Collector Current ($T_J = 175^\circ\text{C}$)	I_{Cpulse}	150	A
Maximum Power Dissipation @ $T_C = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	P_{tot}	186	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	150	$^\circ\text{C}$

BOOST DIODE

Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Continuous Forward Current @ $T_C < 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_{F1}	34	A
Continuous Forward Current @ $T_C < 132^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_{F2}	20	A
Maximum Power Dissipation @ $T_C = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	P_{tot}	114	W
Surge Forward Current (60 Hz single half–sine wave)	I_{FSM}	185	A
I^2t – value (60 Hz single half–sine wave)	I^2t	142	A^2s
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	150	$^\circ\text{C}$

BYPASS DIODE / IGBT PROTECTION DIODE

Peak Repetitive Reverse Voltage	V_{RRM}	1600	V
Continuous Forward Current @ $T_C < 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_{F1}	58	A
Continuous Forward Current @ $T_C < 141^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_{F2}	25	A
Repetitive Peak Forward Current ($T_J = 175^\circ\text{C}$, t_p limited by T_{Jmax})	I_{FRM}	75	A
Maximum Power Dissipation @ $T_C = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	P_{tot}	91	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	150	$^\circ\text{C}$

THERMAL PROPERTIES

Storage Temperature range	T_{stg}	-40 to 125	$^\circ\text{C}$
---------------------------	-----------	------------	------------------

INSULATION PROPERTIES

Isolation test voltage, $t = 1$ sec, 60 Hz	V_{is}	3000	VRMS
Creepage distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	-40	150	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NXH100B120H3Q0, NXH100B120H3Q0PG-R

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
BOOST IGBT CHARACTERISTICS						
Collector–Emitter Cutoff Current	$V_{GE} = 0\text{ V}, V_{CE} = 1200\text{ V}$	I_{CES}	–	–	200	μA
Collector–Emitter Saturation Voltage	$V_{GE} = 15\text{ V}, I_C = 50\text{ A}, T_J = 25^\circ\text{C}$	$V_{CE(sat)}$	–	1.77	2.3	V
	$V_{GE} = 15\text{ V}, I_C = 50\text{ A}, T_J = 150^\circ\text{C}$		–	1.93	–	
Gate–Emitter Threshold Voltage	$V_{GE} = V_{CE}, I_C = 1\text{ mA}$	$V_{GE(TH)}$	4.6	5.27	6.5	V
Gate Leakage Current	$V_{GE} = 20\text{ V}, V_{CE} = 0\text{ V}$	I_{GES}	–	–	800	nA
Turn–on Delay Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 700\text{ V}, I_C = 50\text{ A}, V_{GE} = \pm 15\text{ V},$ $R_G = 4\ \Omega$	$t_{d(on)}$	–	44	–	ns
Rise Time		t_r	–	16	–	
Turn–off Delay Time		$t_{d(off)}$	–	203	–	
Fall Time		t_f	–	23	–	
Turn–on Switching Loss per Pulse		E_{on}	–	700	–	
Turn–off Switching Loss per Pulse		E_{off}	–	1500	–	
Turn–on Delay Time	$T_J = 125^\circ\text{C}$ $V_{CE} = 700\text{ V}, I_C = 50\text{ A}, V_{GE} = \pm 15\text{ V},$ $R_G = 4\ \Omega$	$t_{d(on)}$	–	43	–	ns
Rise Time		t_r	–	18	–	
Turn–off Delay Time		$t_{d(off)}$	–	233	–	
Fall Time		t_f	–	58	–	
Turn–on Switching Loss per Pulse		E_{on}	–	800	–	
Turn–off Switching Loss per Pulse		E_{off}	–	2600	–	
Input Capacitance	$V_{CE} = 20\text{ V}, V_{GE} = 0\text{ V}, f = 10\text{ kHz}$	C_{ies}	–	9075	–	pF
Output Capacitance		C_{oes}	–	173	–	
Reverse Transfer Capacitance		C_{res}	–	147	–	
Total Gate Charge	$V_{CE} = 600\text{ V}, I_C = 40\text{ A}, V_{GE} = 15\text{ V}$	Q_g	–	409	–	nC
Thermal Resistance – chip–to–case		R_{thJC}	–	0.51	–	$^\circ\text{C/W}$
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness $\approx 100\ \mu\text{m}$, $\lambda = 2.87\text{ W/mK}$	R_{thJH}	–	0.82	–	$^\circ\text{C/W}$

BOOST DIODE CHARACTERISTICS

Diode Reverse Leakage Current	$V_R = 1200\text{ V}$	I_R	–	–	300	μA
Diode Forward Voltage	$I_F = 20\text{ A}, T_J = 25^\circ\text{C}$	V_F	–	1.44	1.8	V
	$I_F = 20\text{ A}, T_J = 150^\circ\text{C}$		–	1.93	–	
Reverse Recovery Time	$T_J = 25^\circ\text{C}$ $V_{CE} = 700\text{ V}, I_C = 50\text{ A}, V_{GE} = \pm 15\text{ V},$ $R_G = 4\ \Omega$	t_{rr}	–	15	–	ns
Reverse Recovery Charge		Q_{rr}	–	108	–	nC
Peak Reverse Recovery Current		I_{RRM}	–	11	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	1500	–	$\text{A}/\mu\text{s}$
Reverse Recovery Energy		E_{rr}	–	20	–	μJ
Reverse Recovery Time		$T_J = 125^\circ\text{C}$ $V_{CE} = 700\text{ V}, I_C = 50\text{ A}, V_{GE} = \pm 15\text{ V},$ $R_G = 4\ \Omega$	t_{rr}	–	16	–
Reverse Recovery Charge	Q_{rr}		–	115	–	nC
Peak Reverse Recovery Current	I_{RRM}		–	12	–	A
Peak Rate of Fall of Recovery Current	di/dt		–	1400	–	$\text{A}/\mu\text{s}$
Reverse Recovery Energy	E_{rr}		–	22	–	μJ
Thermal Resistance – chip–to–case			R_{thJC}	–	0.83	–
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness $\approx 100\ \mu\text{m}$, $\lambda = 2.87\text{ W/mK}$	R_{thJH}	–	1.15	–	$^\circ\text{C/W}$

NXH100B120H3Q0, NXH100B120H3Q0PG-R

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
BYPASS DIODE/IGBT PROTECTION DIODE CHARACTERISTICS						
Diode Reverse Leakage Current	$V_R = 1600\text{ V}, T_J = 25^\circ\text{C}$	I_R	–	–	100	μA
Diode Forward Voltage	$I_F = 25\text{ A}, T_J = 25^\circ\text{C}$	V_F	–	1.0	1.4	V
	$I_F = 25\text{ A}, T_J = 150^\circ\text{C}$		–	0.90	–	
Thermal Resistance – chip-to-case		R_{thJC}	–	1.04	–	$^\circ\text{C/W}$
Thermal Resistance – chip-to-heatsink	Thermal grease, Thickness $\approx 100\ \mu\text{m}$, $\lambda = 2.87\ \text{W/mK}$	R_{thJH}	–	1.41	–	$^\circ\text{C/W}$

THERMISTOR CHARACTERISTICS

Nominal resistance		R_{25}	–	22	–	$\text{k}\Omega$
Nominal resistance	$T = 100^\circ\text{C}$	R_{100}	–	1486	–	Ω
Deviation of R_{25}		$\Delta R/R$	–5	–	5	%
Power dissipation		P_D	–	200	–	mW
Power dissipation constant			–	2	–	mW/K
B-value	B(25/50), tolerance $\pm 3\%$		–	3950	–	K
B-value	B(25/100), tolerance $\pm 3\%$		–	3998	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH100B120H3Q0PG, NXH100B120H3Q0PG-R	NXH100B120H3Q0PG, NXH100B120H3Q0PG-R	Q0BOOST – Case 180BF (Pb-Free and Halide-Free) Press-Fit Pins	24 Units / Blister Tray
NXH100B120H3Q0SG	NXH100B120H3Q0SG	Q0BOOST – Case 180AJ (Pb-Free and Halide-Free) Solder Pins	24 Units / Blister Tray
NXH100B120H3Q0PTG	NXH100B120H3Q0PTG	Q0BOOST – Case 180BF (Pb-Free and Halide-Free) Press-Fit Pins, Thermal Interface Material (TIM)	24 Units / Blister Tray
NXH100B120H3Q0STG	NXH100B120H3Q0STG	Q0BOOST – Case 180AJ (Pb-Free and Halide-Free) Solder Pins, Thermal Interface Material (TIM)	24 Units / Blister Tray

NXH100B120H3Q0, NXH100B120H3Q0PG-R

TYPICAL CHARACTERISTICS Boost IGBT & IGBT Protection Diode / Bypass Diode

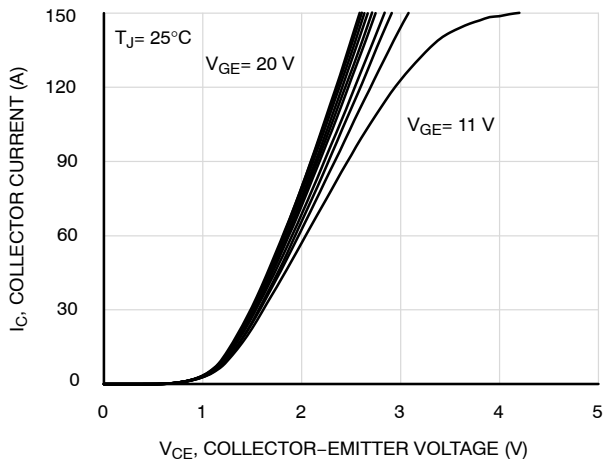


Figure 2. IGBT Typical Output Characteristics

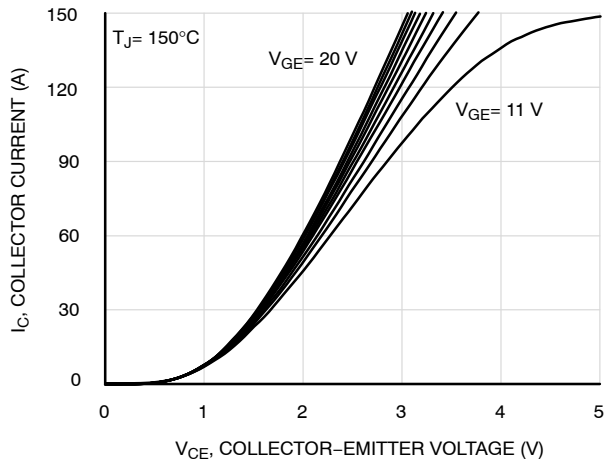


Figure 3. IGBT Typical Output Characteristics

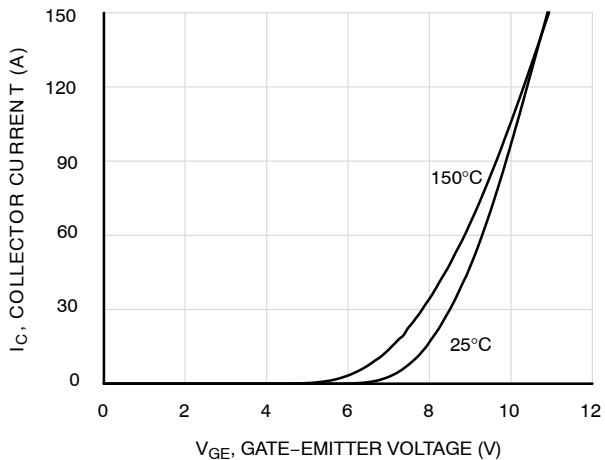


Figure 4. IGBT Typical Transfer Characteristics

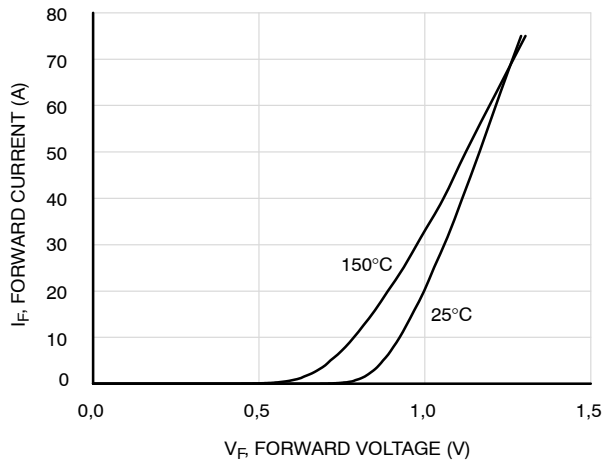


Figure 5. Diode Forward Characteristics

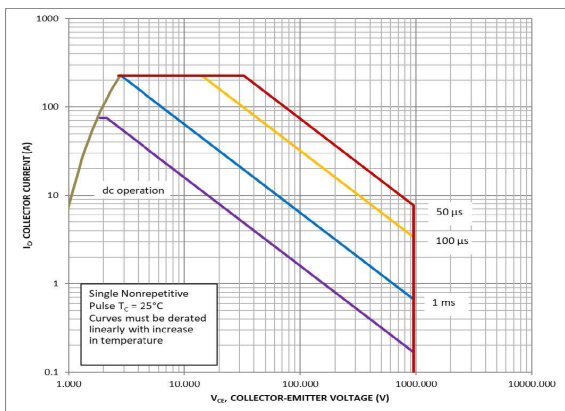


Figure 6. FBSOA

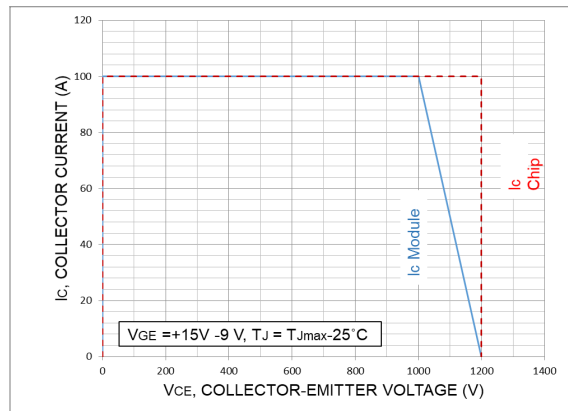


Figure 7. RBSOA

NXH100B120H3Q0, NXH100B120H3Q0PG-R

TYPICAL CHARACTERISTICS Boost IGBT & IGBT Protection Diode / Bypass Diode

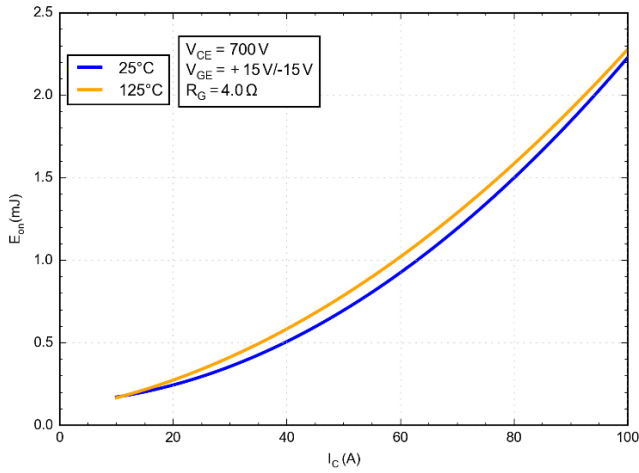


Figure 8. Typical Switching Loss Eon vs. IC

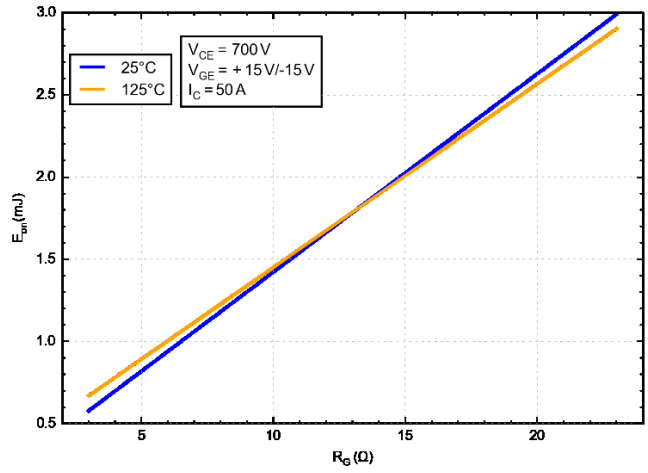


Figure 9. Typical Switching Loss Eon vs. R_G

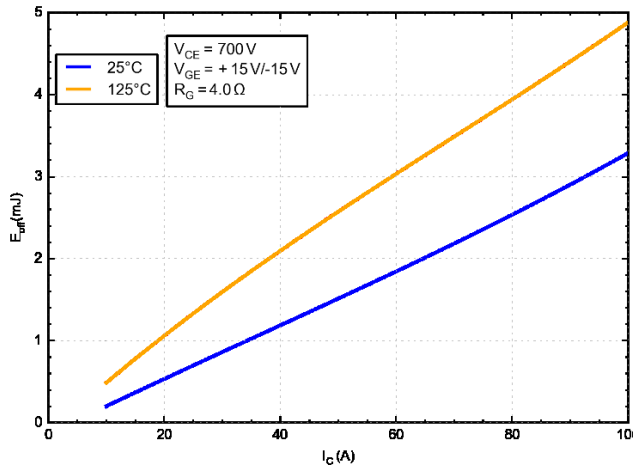


Figure 10. Typical Switching Loss Eoff vs. IC

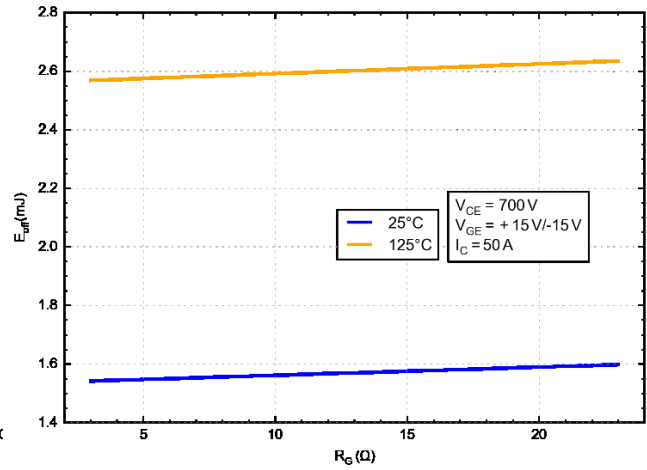


Figure 11. Typical Switching Loss Eoff vs. R_G

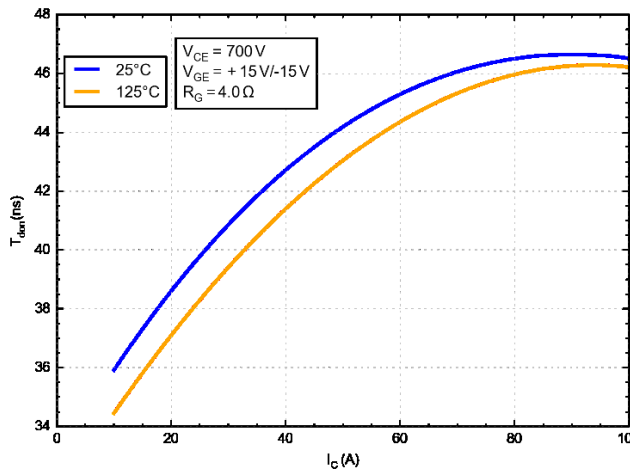


Figure 12. Typical Switching Time Tdon vs. IC

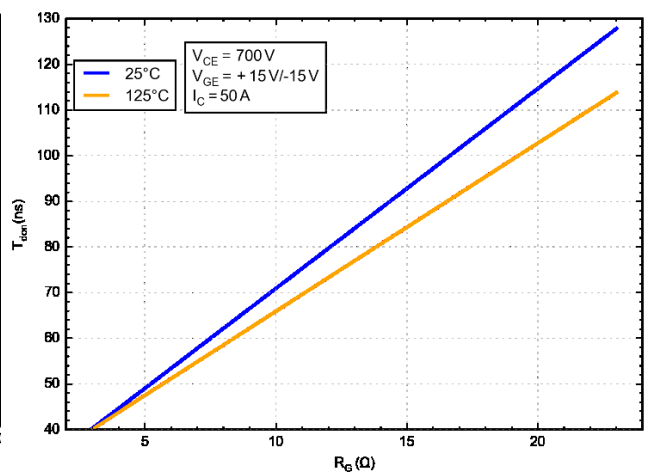


Figure 13. Typical Switching Time Tdon vs. R_G

NXH100B120H3Q0, NXH100B120H3Q0PG-R

TYPICAL PERFORMANCE CHARACTERISTICS

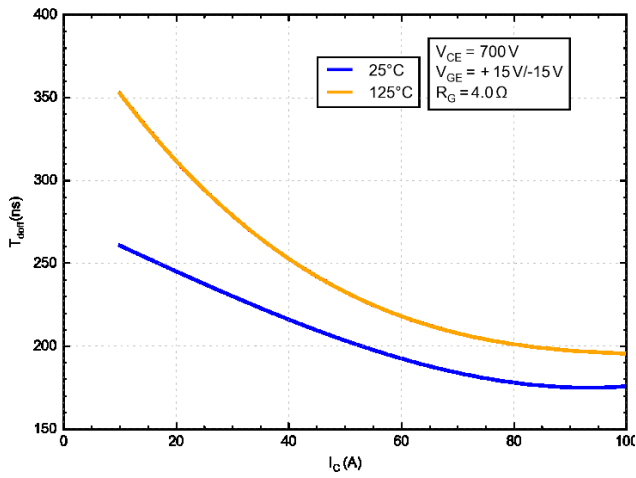


Figure 14. Typical Switching Time Tdoff vs. IC

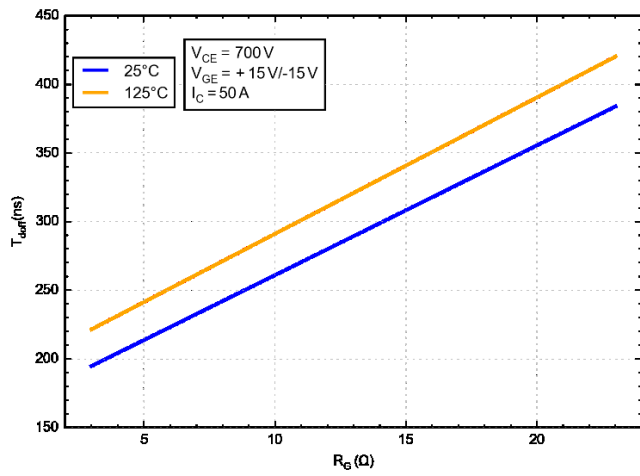


Figure 15. Typical Switching Time Tdoff vs. R_G

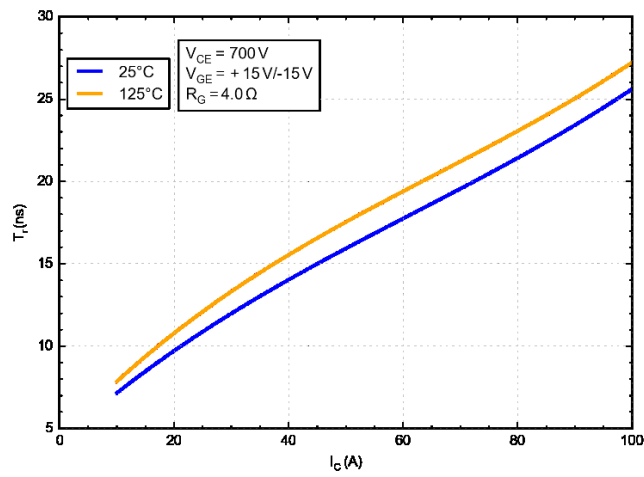


Figure 16. Typical Switching Time Tron vs. IC

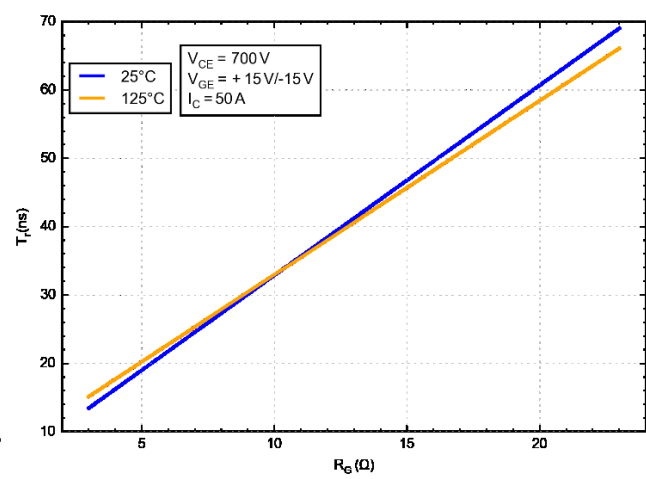


Figure 17. Typical Switching Time Tron vs. R_G

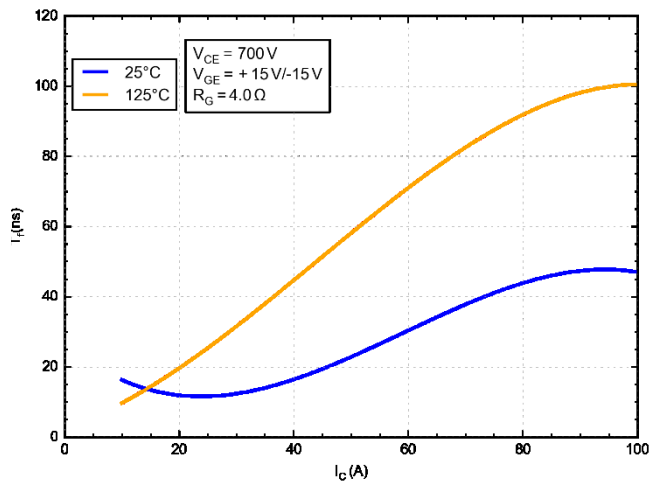


Figure 18. Typical Switching Time Tf vs. IC

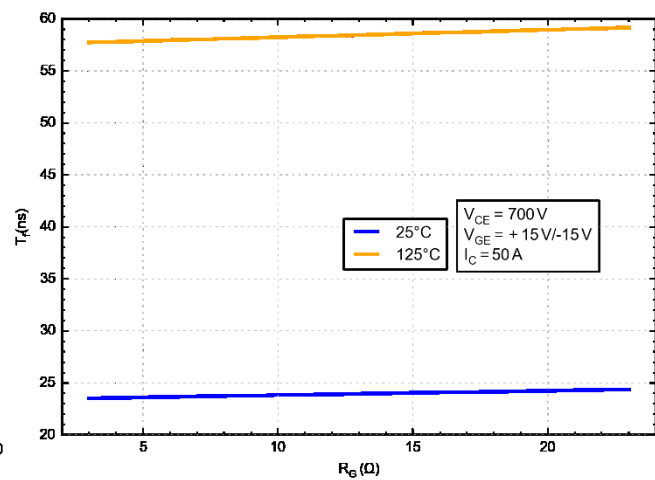


Figure 19. Typical Switching Time Tf vs. R_G

NXH100B120H3Q0, NXH100B120H3Q0PG-R

TYPICAL PERFORMANCE CHARACTERISTICS

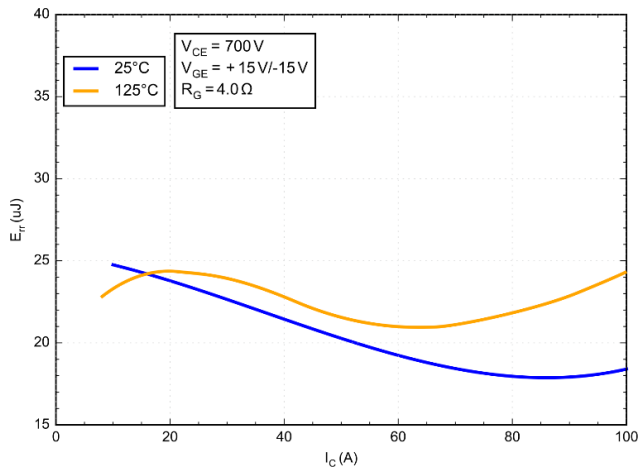


Figure 20. Typical Reverse Recovery Energy vs. IC

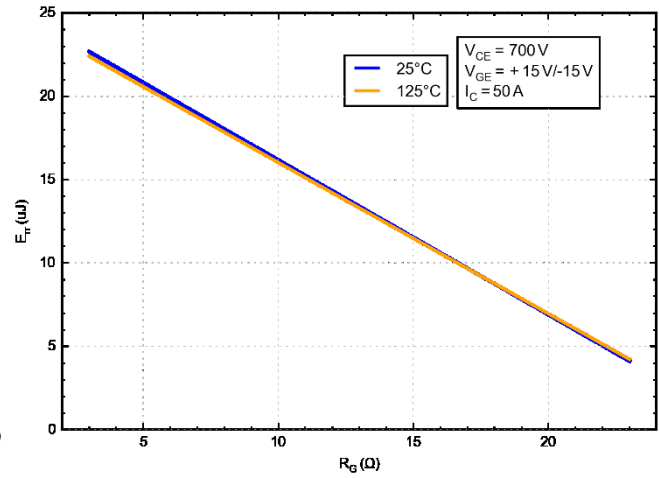


Figure 21. Typical Reverse Recovery Energy vs. RG

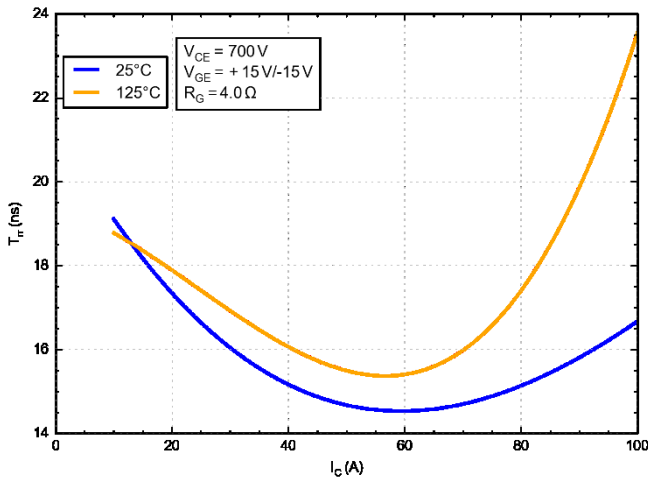


Figure 22. Typical Reverse Recovery Time vs. IC

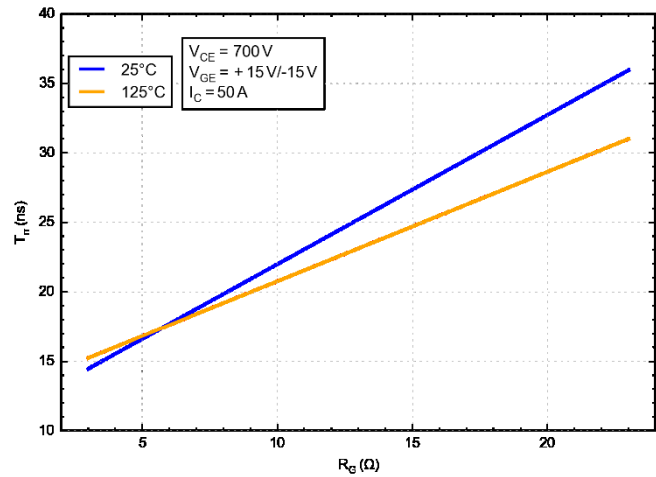


Figure 23. Typical Reverse Recovery Time vs. RG

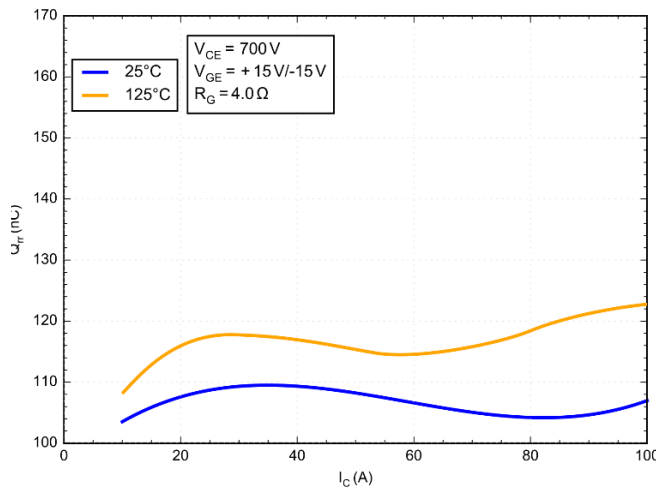


Figure 24. Typical Reverse Recovery Charge vs. IC

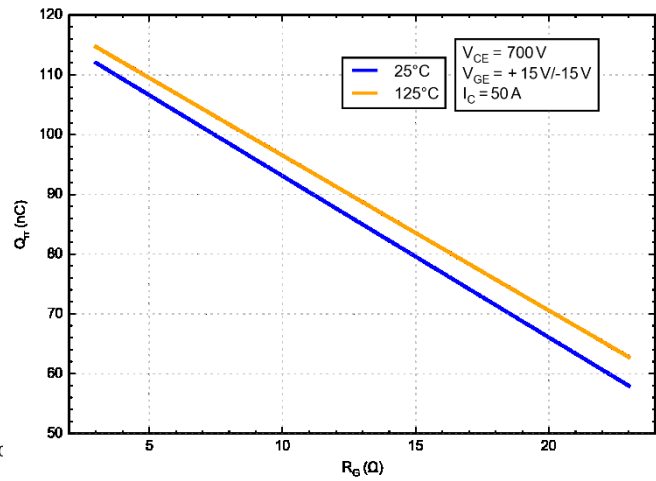


Figure 25. Typical Reverse Recovery Charge vs. RG

NXH100B120H3Q0, NXH100B120H3Q0PG-R

TYPICAL PERFORMANCE CHARACTERISTICS

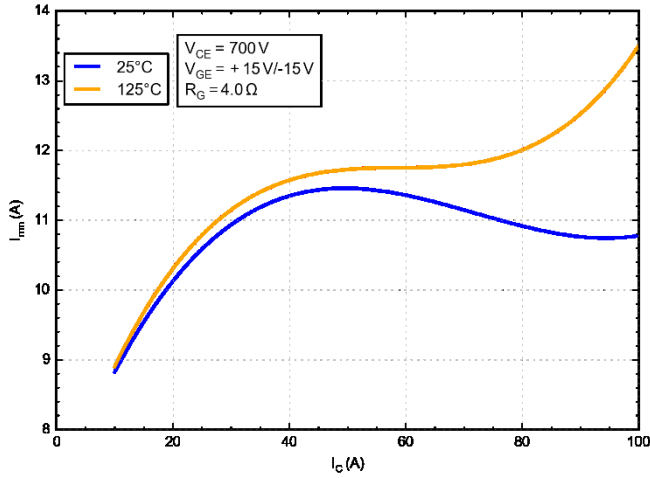


Figure 26. Typical Reverse Recovery Current vs. IC

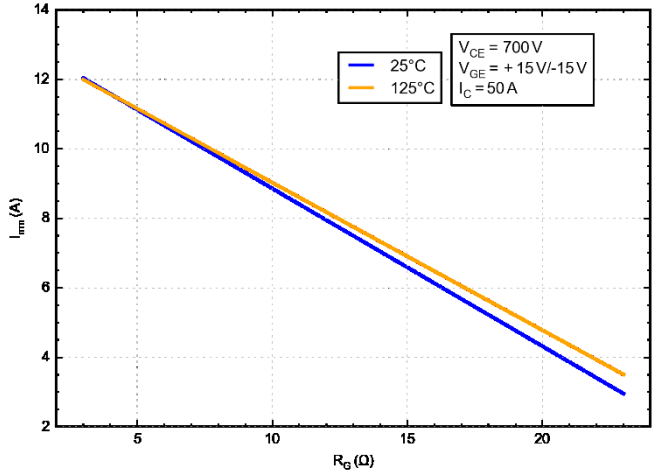


Figure 27. Typical Reverse Recovery Current vs. RG

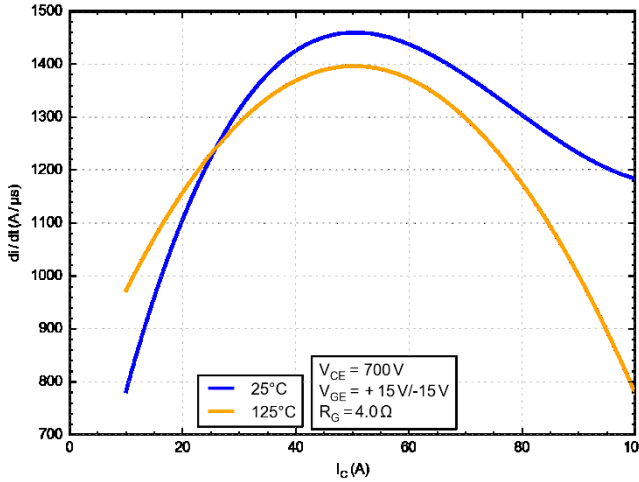


Figure 28. Typical di/dt vs. IC

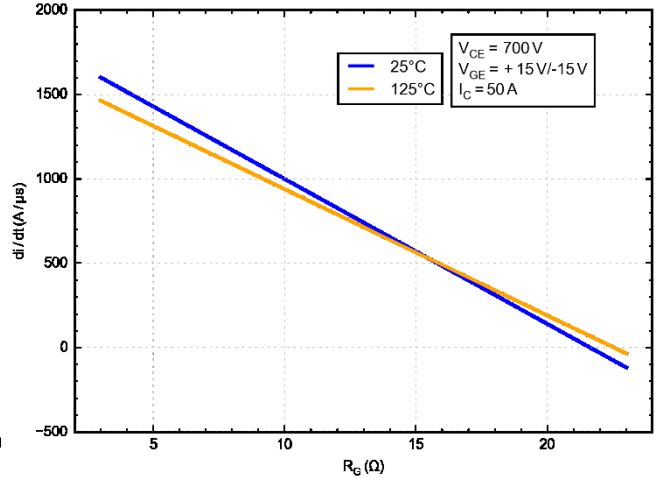


Figure 29. Typical di/dt vs. RG

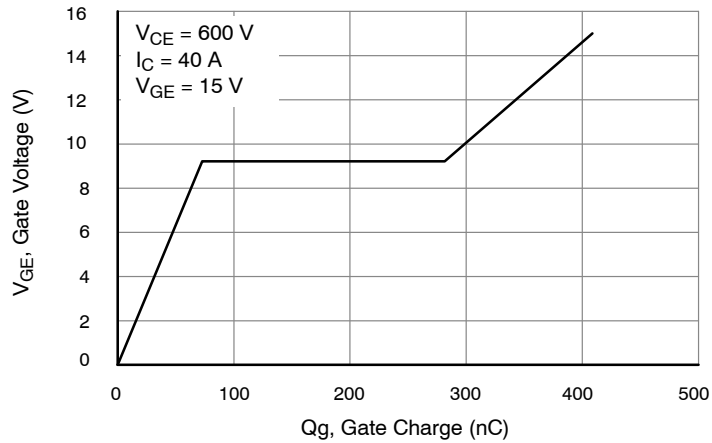


Figure 30. Gate Voltage vs. Gate Charge

NXH100B120H3Q0, NXH100B120H3Q0PG-R

TYPICAL PERFORMANCE CHARACTERISTICS

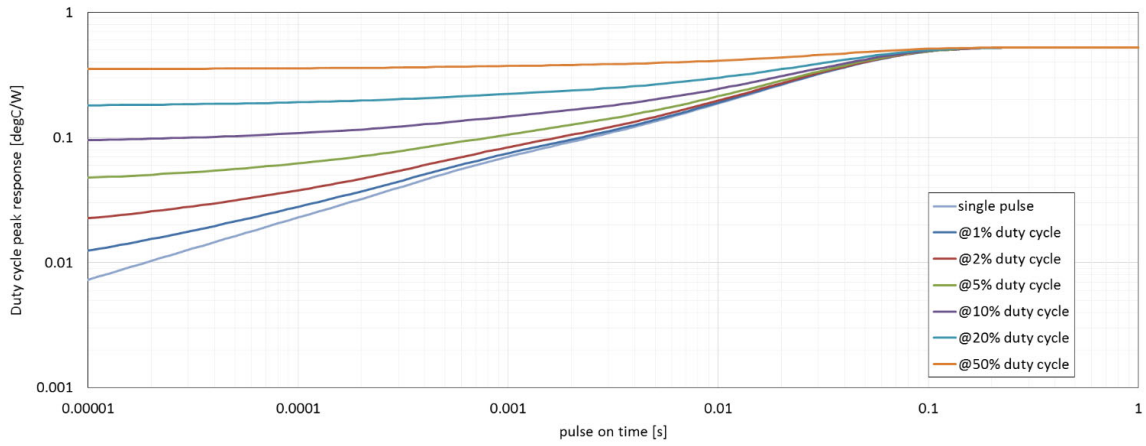


Figure 31. IGBT Junction-to-Case Transient Thermal Impedance

NXH100B120H3Q0, NXH100B120H3Q0PG-R

TYPICAL PERFORMANCE CHARACTERISTICS – Boost Diode

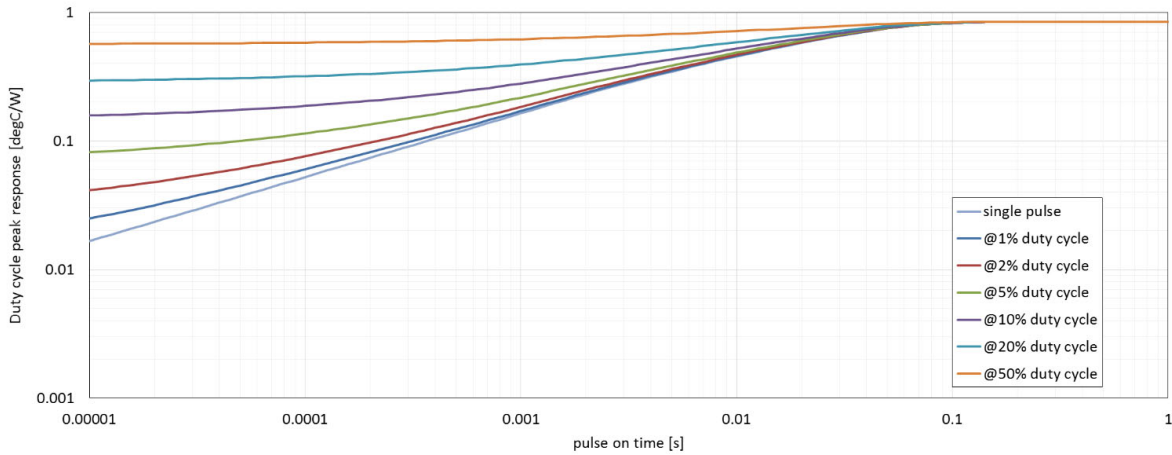


Figure 32. Diode Junction-to-Case Transient Thermal Impedance

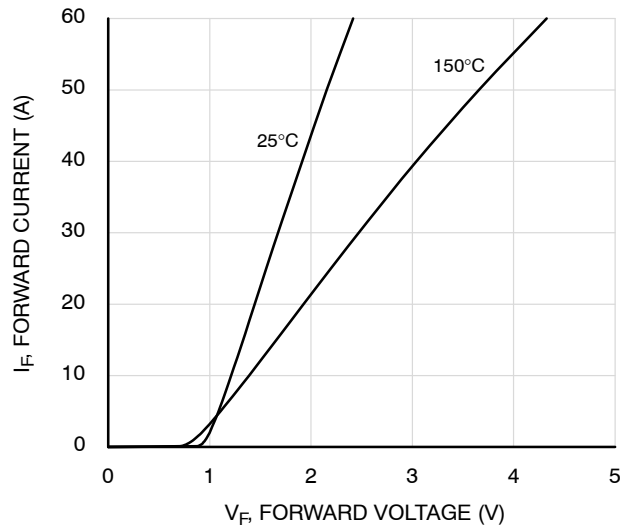


Figure 33. Diode Forward Characteristic

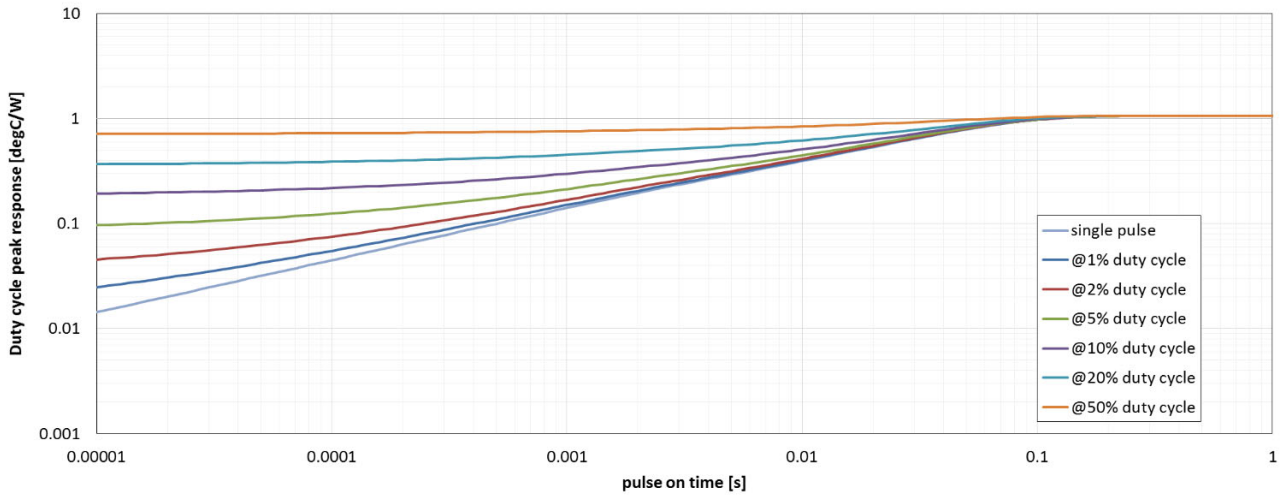


Figure TBD: Transient Thermal Impedance

Figure 34. Diode Junction-to-Case Transient Thermal Impedance

MECHANICAL CASE OUTLINE

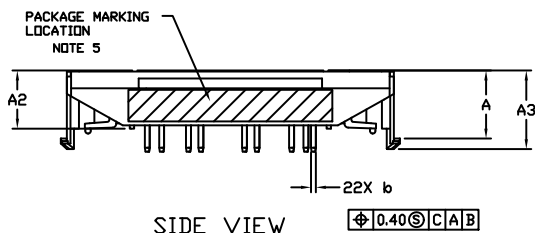
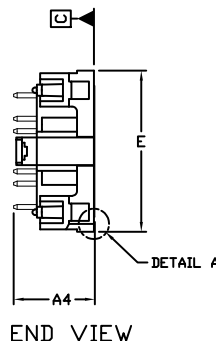
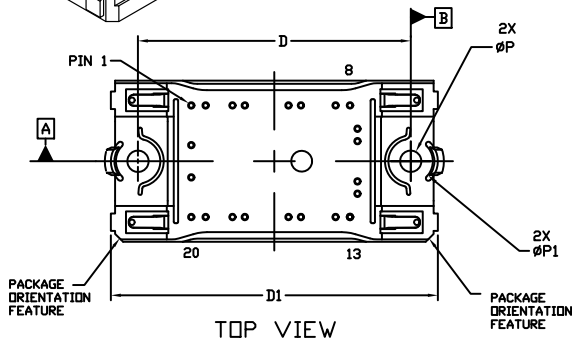
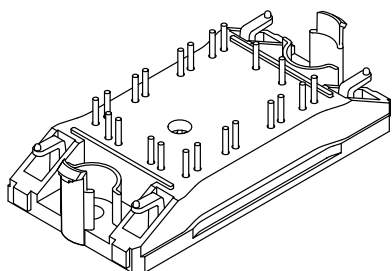
PACKAGE DIMENSIONS

ON Semiconductor®



PIM22, 55x32.5 / Q0BOOST CASE 180AJ ISSUE B

DATE 08 NOV 2017



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 1.00 AND 3.00 FROM THE TERMINAL TIP.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

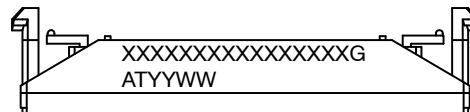
DIM	MILLIMETERS	
	MIN.	NDM.
A	13.50	13.90
A1	0.10	0.30
A2	11.50	11.90
A3	15.65	16.05
A4	16.35	REF
b	0.95	1.05
D	54.80	55.20
D1	65.60	66.20
E	32.20	32.80
P	4.20	4.40
P1	8.90	9.10

MOUNTING HOLE POSITION

NOTE 4

PIN	HOLE POSITION		PIN	PIN POSITION		PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y		X	Y		X	Y
1	-16.75	-11.25	12	16.75	6.55	1	-16.75	11.25	12	16.75	-6.55
2	-13.85	-11.25	13	15.25	11.25	2	-13.85	11.25	13	15.25	-11.25
3	-8.45	-11.25	14	12.35	11.25	3	-8.45	11.25	14	12.35	-11.25
4	-5.95	-11.25	15	5.35	11.25	4	-5.95	11.25	15	5.35	-11.25
5	2.85	-11.25	16	2.85	11.25	5	2.85	11.25	16	2.85	-11.25
6	5.35	-11.25	17	-5.95	11.25	6	5.35	11.25	17	-5.95	-11.25
7	12.35	-11.25	18	-8.45	11.25	7	12.35	11.25	18	-8.45	-11.25
8	15.25	-11.25	19	-13.85	11.25	8	15.25	11.25	19	-13.85	-11.25
9	16.75	-6.55	20	-16.75	11.25	9	16.75	6.55	20	-16.75	-11.25
10	16.75	-4.05	21	-16.75	3.25	10	16.75	4.05	21	-16.75	-3.25
11	16.75	4.05	22	-16.75	-3.25	11	16.75	-4.05	22	-16.75	3.25

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 G = Pb-Free Package
 AT = Assembly & Test Site Code
 YYWW = Year and Work Week Code

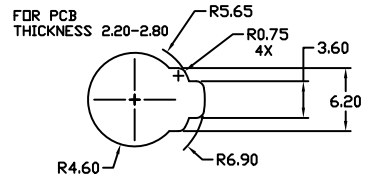
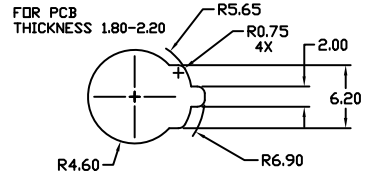
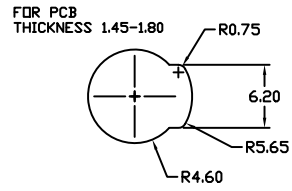
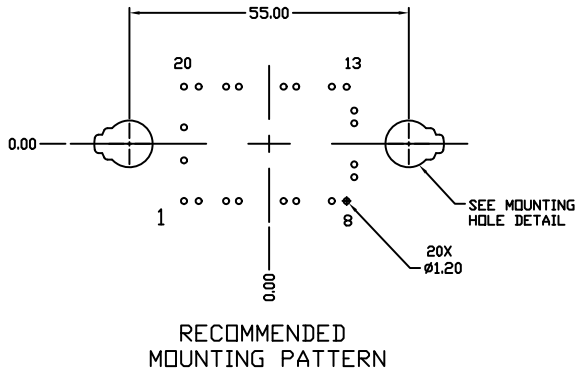
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON63481G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PIM22 55X32.5 / Q0BOOST (SOLDER PIN)	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.


PIM22, 55x32.5 / Q0BOOST
CASE 180AJ
ISSUE B

DATE 08 NOV 2017



MOUNTING HOLE DETAIL

DOCUMENT NUMBER:	98AON63481G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PIM22 55X32.5 / Q0BOOST (SOLDER PIN)	PAGE 2 OF 2

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

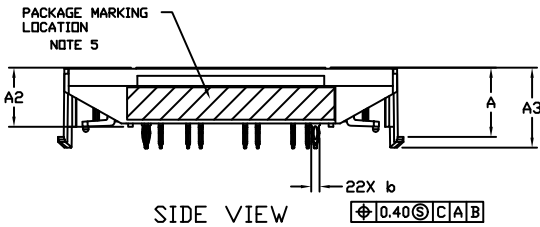
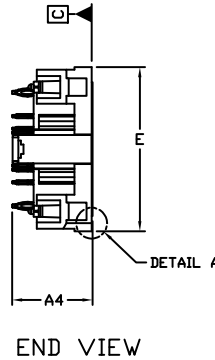
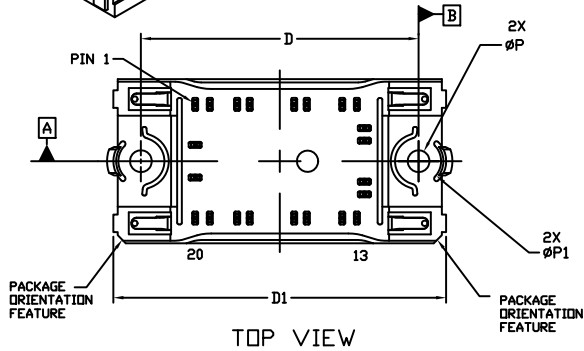
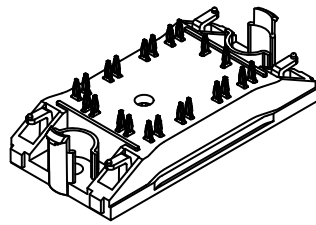
PACKAGE DIMENSIONS

ON Semiconductor®



PIM22 55x32.5 (PRESSFIT PIN) CASE 180BF ISSUE O

DATE 21 MAY 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 1.00 AND 3.00 FROM THE TERMINAL TIP.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO EACH TERMINAL IN BOTH DIRECTIONS.
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	13.50	13.70	13.90
A1	0.10	0.20	0.30
A2	11.50	11.70	11.90
A3	15.65	15.85	16.05
A4	15.95 REF		
<i>b</i>	1.61	1.66	1.71
D	54.80	55.00	55.20
D1	65.60	65.90	66.20
E	32.20	32.50	32.80
P	4.20	4.30	4.40
P1	8.90	9.00	9.10

NOTE 4

PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	-16.75	11.25	12	16.75	-6.55
2	-13.85	11.25	13	15.25	-11.25
3	-8.45	11.25	14	12.35	-11.25
4	-5.95	11.25	15	5.35	-11.25
5	2.85	11.25	16	2.85	-11.25
6	5.35	11.25	17	-5.95	-11.25
7	12.35	11.25	18	-8.45	-11.25
8	15.25	11.25	19	-13.85	-11.25
9	16.75	6.55	20	-16.75	-11.25
10	16.75	4.05	21	-16.75	-3.25
11	16.75	-4.05	22	-16.75	3.25

DOCUMENT NUMBER:	98AON07824H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PIM22 55x32.5 (PRESSFIT PIN)	PAGE 1 OF 2

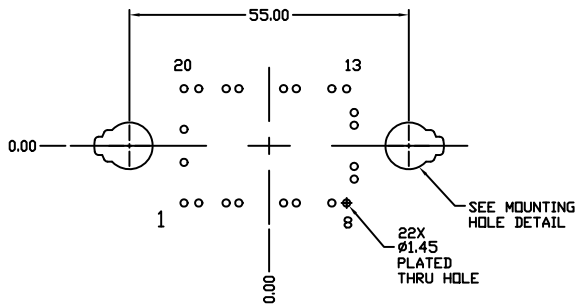
ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

PIM22 55x32.5 (PRESSFIT PIN)
CASE 180BF
ISSUE O

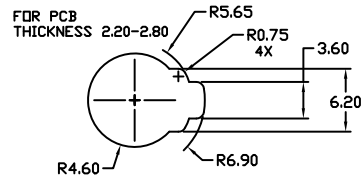
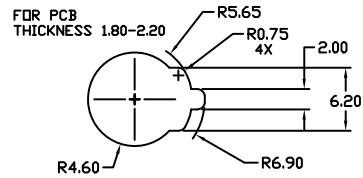
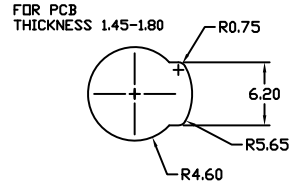
DATE 17 MAY 2019

MOUNTING HOLE POSITION

PIN	HOLE POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	-16.75	-11.25	12	16.75	6.55
2	-13.85	-11.25	13	15.25	11.25
3	-8.45	-11.25	14	12.35	11.25
4	-5.95	-11.25	15	5.35	11.25
5	2.85	-11.25	16	2.85	11.25
6	5.35	-11.25	17	-5.95	11.25
7	12.35	-11.25	18	-8.45	11.25
8	15.25	-11.25	19	-13.85	11.25
9	16.75	-6.55	20	-16.75	11.25
10	16.75	-4.05	21	-16.75	3.25
11	16.75	4.05	22	-16.75	-3.25

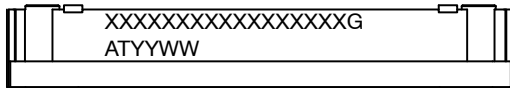


**RECOMMENDED
MOUNTING PATTERN**



MOUNTING HOLE DETAIL

**GENERIC
MARKING DIAGRAM***



XXXXX = Specific Device Code
 G = Pb-Free Package
 AT = Assembly & Test Site Code
 YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON07824H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PIM22 55x32.5 (PRESSFIT PIN)	PAGE 2 OF 2

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

