

Three Level NPC Q2Pack Module

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

The NXH400N100L4Q2 is a power module containing a I-type neutral point clamped three-level inverter. The integrated field stop trench IGBTs and FRDs provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- Neutral Point Clamped Three-level Inverter Module
- Extreme Efficient Trench with Field Stop Technology
- Low Inductive Layout
- Low Package Height
- Thermistor

Typical Applications

- Solar Inverters
- Energy Storage System
- Uninterruptable Power Supplies Systems

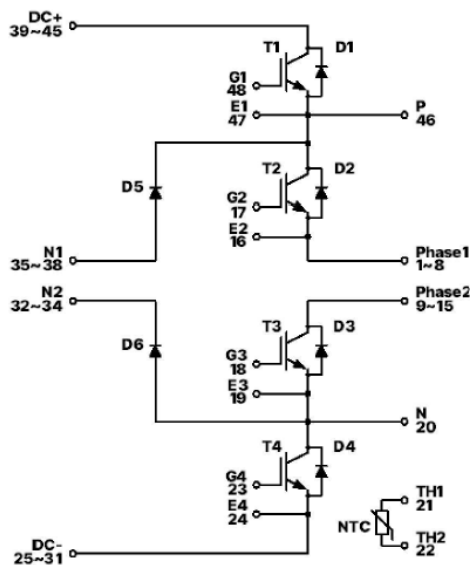
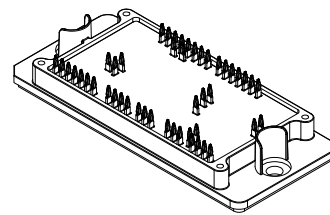
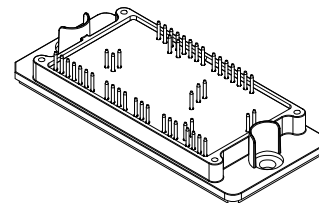


Figure 1. NXH400N100L4Q2F2 Schematic Diagram

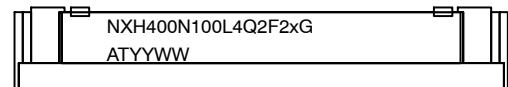


Q2PACK PRESS FIT PINS
PIM48, 93x47
CASE 180CR



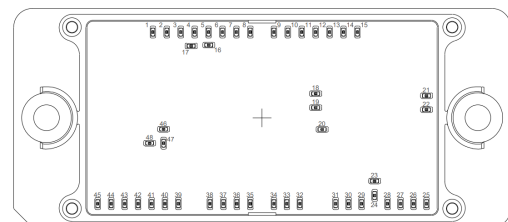
Q2PACK SOLDER PINS
PIM48, 93x47
CASE 180BL

MARKING DIAGRAM



NXH400N100L4Q2F2xG = Specific Device Code
x = P or S
G = Pb-Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 1)

Rating	Symbol	Value	Unit
IGBT (T1, T2, T3, T4)			
Collector-Emitter Voltage	V_{CES}	1000	V
Gate-Emitter Voltage Positive Transient Gate-Emitter Voltage ($T_{pulse} = 5 \mu\text{s}$, $D < 0.10$)	V_{GE}	± 20 30	V
Continuous Collector Current @ $T_C = 80^\circ\text{C}$	I_C	360	A
Pulsed Peak Collector Current @ $T_C = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	$I_{C(Pulse)}$	1080	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	980	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature (Note 2)	T_{JMAX}	175	$^\circ\text{C}$

IGBT INVERSE DIODE (D1, D2, D3, D4)

Peak Repetitive Reverse Voltage	V_{RRM}	1000	V
Continuous Forward Current @ $T_C = 80^\circ\text{C}$	I_F	276	A
Repetitive Peak Forward Current ($T_J = 175^\circ\text{C}$)	I_{FRM}	828	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	680	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	175	$^\circ\text{C}$

NEUTRAL POINT DIODE (D5, D6)

Peak Repetitive Reverse Voltage	V_{RRM}	1000	V
Continuous Forward Current @ $T_C = 80^\circ\text{C}$	I_F	291	A
Repetitive Peak Forward Current ($T_J = 175^\circ\text{C}$)	I_{FRM}	873	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	734	W
Minimum Operating Junction Temperature	T_{JMIN}	-40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. THERMAL AND INSULATION PROPERTIES ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 1)

Rating	Symbol	Value	Unit
THERMAL PROPERTIES			
Operating Temperature under Switching Condition	T_{VJOP}	-40 to 150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to 125	$^\circ\text{C}$
INSULATION PROPERTIES			
Isolation Test Voltage, $t = 1 \text{ s}$, 50 Hz (Note 2)	V_{is}	4000	V_{RMS}
Creepage Distance		12.7	mm
Comparative Tracking Index	CTI	>600	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to [ELECTRICAL CHARACTERISTICS](#), RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. 4000 V_{ACRMS} for 1 second duration is equivalent to 3333 V_{ACRMS} for 1 minute duration.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	
OUTER IGBT (T1, T4) CHARACTERISTICS							
Collector-Emitter Cutoff Current	I _{CES}	V _{GE} = 0 V, V _{CE} = 1000 V	-	-	25	μA	
Collector-Emitter Saturation Voltage	V _{CE(sat)}	V _{GE} = 15 V, I _C = 400 A, T _J = 25°C	-	1.65	2.2	V	
		V _{GE} = 15 V, I _C = 400 A, T _J = 150°C	-	2.1	-		
Gate-Emitter Threshold Voltage	V _{GE(TH)}	V _{GE} = V _{CE} , I _C = 400 mA	3.6	4.9	6.2	V	
Gate Leakage Current	I _{GES}	V _{GE} = ±20 V, V _{CE} = 0 V	-	-	±1.0	μA	
Turn-on Delay Time	t _{d(on)}	T _J = 25°C V _{CE} = 600 V, I _C = 200 A V _{GE} = -9 V, 15 V, R _{Gon} = 9 Ω, R _{Goff} = 19 Ω	-	170.46	-	ns	
Rise Time	t _r		-	54.38	-		
Turn-off Delay Time	t _{d(off)}		-	696.63	-		
Fall Time	t _f		-	12.91	-		
Turn-on Switching Loss per Pulse	E _{on}		-	8.96	-		mJ
Turn-off Switching Loss per Pulse	E _{off}		-	6	-		
Turn-on Delay Time	t _{d(on)}		T _J = 125°C V _{CE} = 600 V, I _C = 200 A V _{GE} = -9 V, 15 V, R _{Gon} = 9 Ω, R _{Goff} = 19 Ω	-	163.09		-
Rise Time	t _r	-		61.38	-		
Turn-off Delay Time	t _{d(off)}	-		771.31	-		
Fall Time	t _f	-		18.23	-		
Turn-on Switching Loss per Pulse	E _{on}	-		14.54	-	mJ	
Turn-off Switching Loss per Pulse	E _{off}	-		9.8	-		
Input Capacitance	C _{ies}	V _{CE} = 20 V, V _{GE} = 0 V, f = 1 MHz		-	26060	-	pF
Output Capacitance	C _{oes}		-	1182	-		
Reverse Transfer Capacitance	C _{res}		-	146	-		
Total Gate Charge	Q _g	V _{CE} = 600 V, I _C = 300 A, V _{GE} = -15 V~15 V	-	1410	-	nC	
Thermal Resistance – Chip-to-Heatsink	R _{thJH}	Thermal grease, Thickness = 100 μm ±2% λ = 2.9 W/mK	-	0.17	-	K/W	
Thermal Resistance – Chip-to-Case	R _{thJC}		-	0.0969	-	K/W	

NEUTRAL POINT DIODE (D5, D6) CHARACTERISTICS

Diode Forward Voltage	V _F	I _F = 225 A, T _J = 25°C	-	2.1	2.7	V	
		I _F = 225 A, T _J = 150°C	-	1.9	-		
Reverse Recovery Time	t _{rr}	T _J = 25°C V _{CE} = 600 V, I _C = 200 A V _{GE} = -9 V, 15 V, R _G = 9 Ω	-	91.65	-	ns	
Reverse Recovery Charge	Q _{rr}		-	5109	-	nC	
Peak Reverse Recovery Current	I _{RPM}		-	117.19	-	A	
Peak Rate of Fall of Recovery Current	di/dt		-	3.02	-	A/ns	
Reverse Recovery Energy	E _{rr}		-	1504	-	μJ	
Reverse Recovery Time	t _{rr}		T _J = 125°C V _{CE} = 600 V, I _C = 200 A V _{GE} = -9 V, 15 V, R _G = 9 Ω	-	168.8	-	ns
Reverse Recovery Charge	Q _{rr}			-	15979	-	nC
Peak Reverse Recovery Current	I _{RPM}	-		183.14	-	A	
Peak Rate of Fall of Recovery Current	di/dt	-		2.64	-	A/ns	
Reverse Recovery Energy	E _{rr}	-		5463	-	μJ	
Thermal Resistance – Chip-to-Heatsink	R _{thJH}	Thermal grease, Thickness = 100 μm ±2% λ = 2.9 W/mK		-	0.21	-	K/W
Thermal Resistance – Chip-to-Case	R _{thJC}		-	0.1295	-	K/W	

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	
INNER IGBT (T2, T3) CHARACTERISTICS							
Collector–Emitter Cutoff Current	I_{CES}	$V_{GE} = 0\text{ V}, V_{CE} = 1000\text{ V}$	–	–	25	μA	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$	$V_{GE} = 15\text{ V}, I_C = 400\text{ A}, T_J = 25^\circ\text{C}$	–	1.65	2.2	V	
		$V_{GE} = 15\text{ V}, I_C = 400\text{ A}, T_J = 150^\circ\text{C}$	–	1.9	–		
Gate–Emitter Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}, I_C = 400\text{ mA}$	3.9	4.6	5.8	V	
Gate Leakage Current	I_{GES}	$V_{GE} = \pm 20\text{ V}, V_{CE} = 0\text{ V}$	–	–	± 1.0	μA	
Turn–on Delay Time	$t_{d(on)}$	$T_J = 25^\circ\text{C}$ $V_{CE} = 600\text{ V}, I_C = 200\text{ A},$ $V_{GE} = -9\text{ V}, 15\text{ V},$ $R_{Gon} = 9\ \Omega, R_{Goff} = 28\ \Omega$	–	171.27	–	ns	
Rise Time	t_r		–	52.54	–		
Turn–off Delay Time	$t_{d(off)}$		–	1153.7	–		
Fall Time	t_f		–	34.88	–		
Turn–on Switching Loss per Pulse	E_{on}		–	8.16	–		mJ
Turn off Switching Loss per Pulse	E_{off}		–	10.25	–		
Turn–on Delay Time	$t_{d(on)}$		$T_J = 125^\circ\text{C}$ $V_{CE} = 600\text{ V}, I_C = 200\text{ A},$ $V_{GE} = -9\text{ V}, 15\text{ V},$ $R_{Gon} = 9\ \Omega, R_{Goff} = 28\ \Omega$	–	160.21		–
Rise Time	t_r	–		59.83	–		
Turn–off Delay Time	$t_{d(off)}$	–		1274.8	–		
Fall Time	t_f	–		26.46	–		
Turn–on Switching Loss per Pulse	E_{on}	–		12.37	–	mJ	
Turn off Switching Loss per Pulse	E_{off}	–		13.42	–		
Input Capacitance	C_{ies}	$V_{CE} = 20\text{ V}, V_{GE} = 0\text{ V}, f = 1\text{ MHz}$		–	26060	–	μF
Output Capacitance	C_{oes}		–	1182	–		
Reverse Transfer Capacitance	C_{res}		–	146	–		
Total Gate Charge	Q_g	$V_{CE} = 600\text{ V}, I_C = 300\text{ A},$ $V_{GE} = -15\text{ V} \sim 15\text{ V}$	–	1410	–	nC	
Thermal Resistance – Chip–to–heatsink	R_{thJH}	Thermal grease, Thickness = $100\ \mu\text{m} \pm 2\%$ $\lambda = 2.9\text{ W/mK}$	–	0.17	–	K/W	
Thermal Resistance – Chip–to–case	R_{thJC}		–	0.0969	–	K/W	

IGBT INVERSE DIODE (D1, D2, D3, D4) CHARACTERISTICS

Diode Forward Voltage	V_F	$I_F = 225\text{ A}, T_J = 25^\circ\text{C}$	–	2.1	2.7	V	
		$I_F = 225\text{ A}, T_J = 150^\circ\text{C}$	–	1.9	–		
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$ $V_{CE} = 600\text{ V}, I_C = 200\text{ A},$ $V_{GE} = -9\text{ V}, 15\text{ V}, R_G = 9\ \Omega$	–	90.31	–	ns	
Reverse Recovery Charge	Q_{rr}		–	5653	–	nC	
Peak Reverse Recovery Current	I_{RRM}		–	123.4	–	A	
Peak Rate of Fall of Recovery Current	di/dt		–	3.178	–	A/ns	
Reverse Recovery Energy	E_{rr}		–	1860	–	μJ	
Reverse Recovery Time	t_{rr}		$T_J = 125^\circ\text{C}$ $V_{CE} = 600\text{ V}, I_C = 200\text{ A},$ $V_{GE} = -9\text{ V}, 15\text{ V}, R_G = 9\ \Omega$	–	167.18	–	ns
Reverse Recovery Charge	Q_{rr}			–	16627	–	nC
Peak Reverse Recovery Current	I_{RRM}	–		182.8	–	A	
Peak Rate of Fall of Recovery Current	di/dt	–		2.734	–	A/ns	
Reverse Recovery Energy	E_{rr}	–		6512	–	μJ	
Thermal Resistance – Chip-to-Heatsink	R_{thJH}	Thermal grease, Thickness = $100\ \mu\text{m} \pm 2\%$ $\lambda = 2.9\text{ W/mK}$		–	0.22	–	K/W
Thermal Resistance – Chip-to-Case	R_{thJC}			–	0.1397	–	K/W

THERMISTOR CHARACTERISTICS

Nominal Resistance	R_{25}	$T = 25^\circ\text{C}$	–	5	–	k Ω
Nominal Resistance	R_{100}	$T = 100^\circ\text{C}$	–	490.6	–	Ω

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
THERMISTOR CHARACTERISTICS						
Deviation of R25	$\Delta R/R$		-1	-	1	%
Power Dissipation	P_D		-	5	-	mW
Power Dissipation Constant			-	1.3	-	mW/K
B-value		B (25/85), tolerance $\pm 1\%$	-	3435	-	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Part Number	Marking	Package	Shipping
NXH400N100L4Q2F2PG	NXH400N100L4Q2F2PG	Q2PACK PRESS FIT PINS PIM48, 93x47 (Pb-Free and Halide-Free)	12 Units / Blister Tray
NXH400N100L4Q2F2SG	NXH400N100L4Q2F2SG	Q2PACK SOLDER PIN PIM48, 93x47 (Pb-Free and Halide-Free)	12 Units / Blister Tray

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – IGBT, INVERSE DIODE AND NEUTRAL POINT DIODE

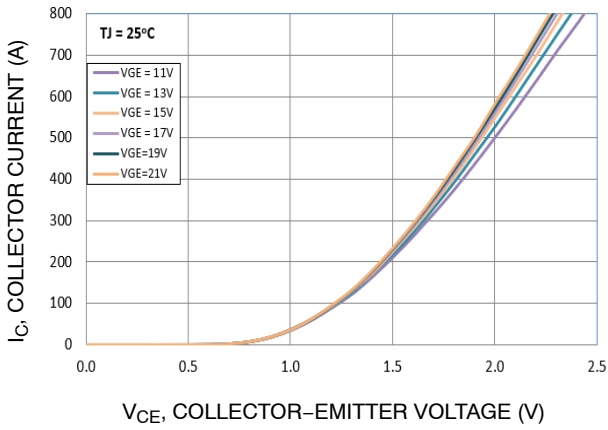


Figure 2. Typical Output Characteristics – IGBT

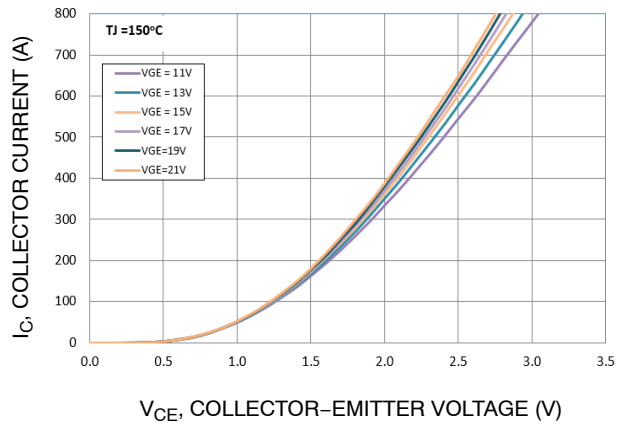


Figure 3. Typical Output Characteristics – IGBT

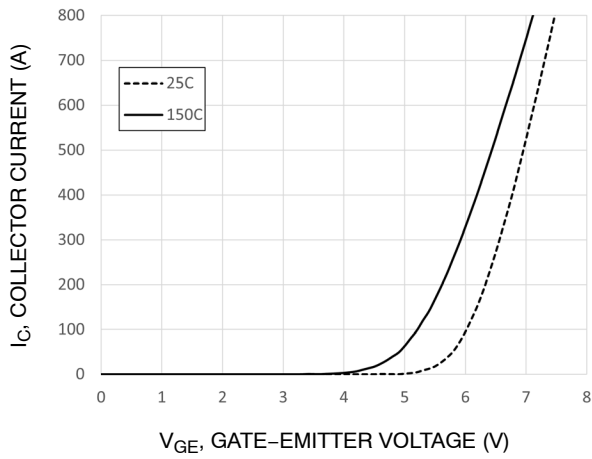


Figure 4. Transfer Characteristics – IGBT

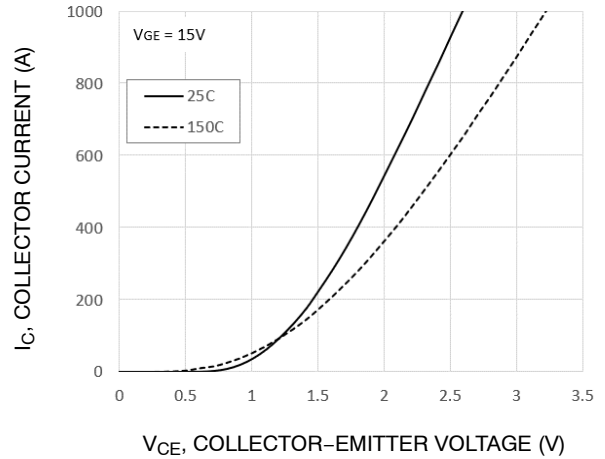


Figure 5. Saturation Voltage Characteristics

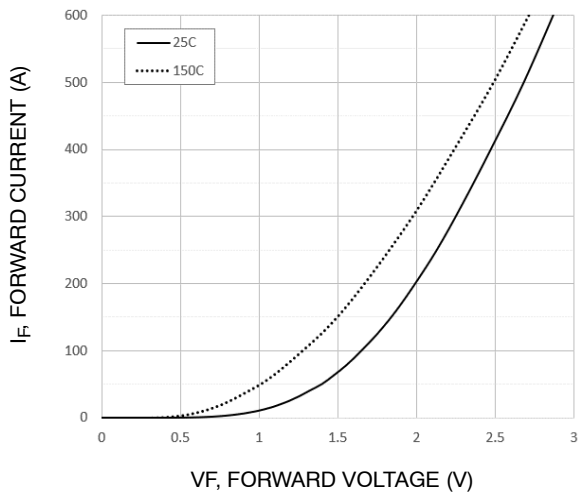


Figure 6. Inverse Diode Forward Characteristics

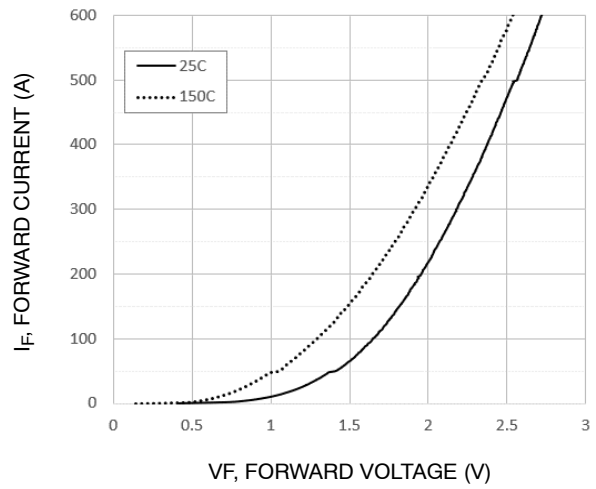


Figure 7. Buck Diode Forward Characteristics

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TYPICAL CHARACTERISTICS – OUTER IGBT (T1, T4)

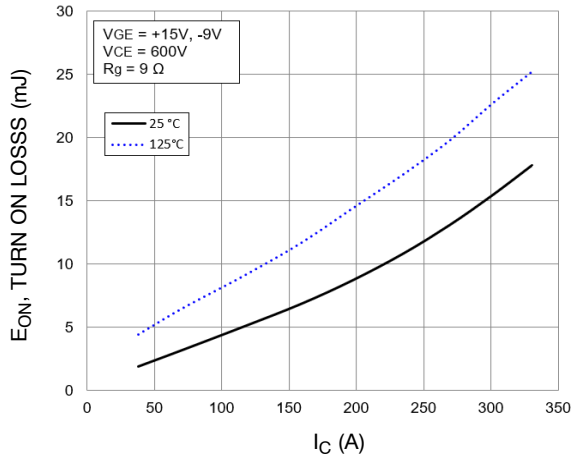


Figure 8. Typical Turn ON Loss vs. IC

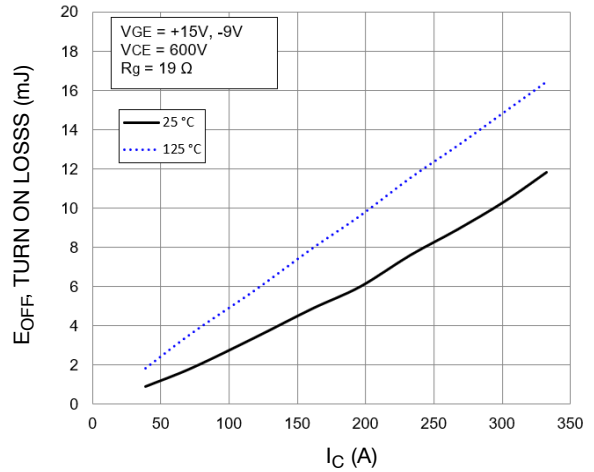


Figure 9. Typical Turn OFF Loss vs. IC

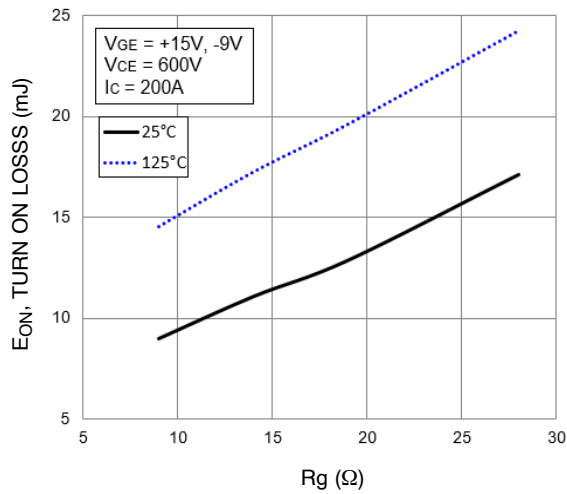


Figure 10. Typical Turn ON Loss vs. Rg

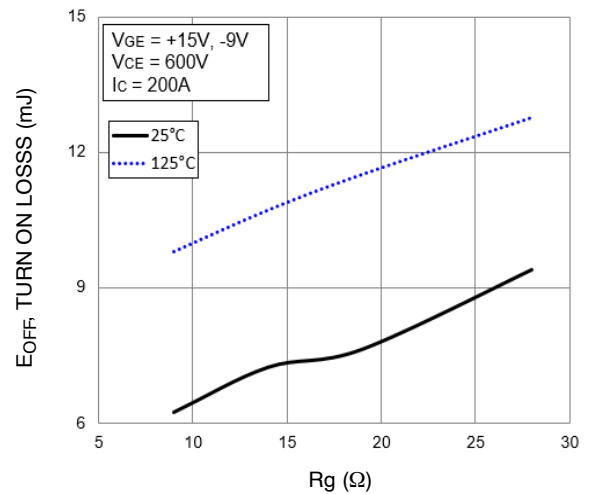


Figure 11. Typical Turn OFF Loss vs. Rg

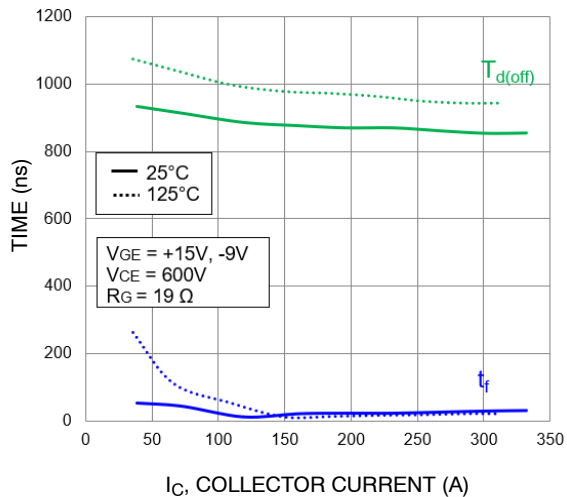


Figure 12. Typical Turn-Off Switching Time vs. IC

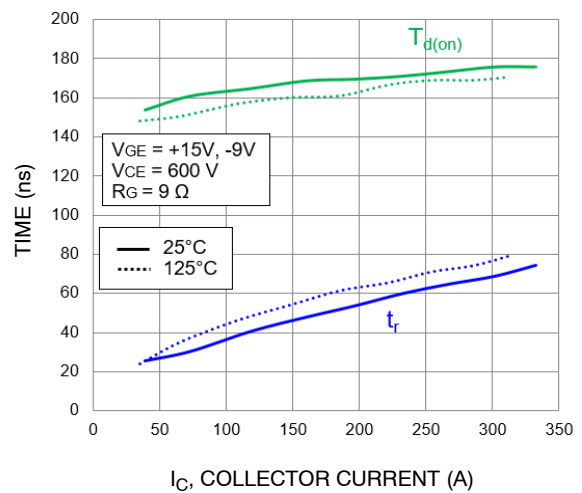


Figure 13. Typical Turn-On Switching Time vs. IC

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – OUTER IGBT (T1,T4) (continued)

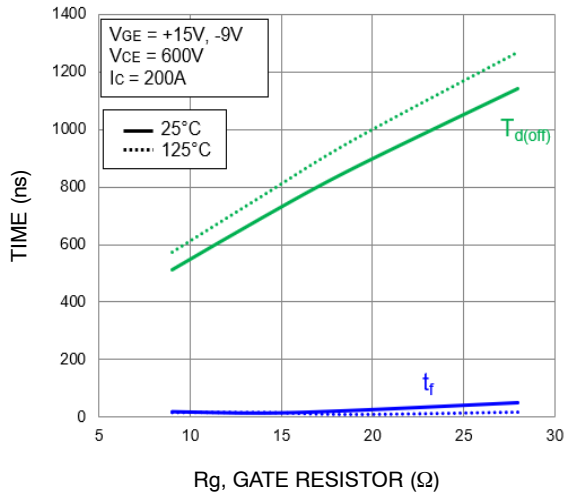


Figure 14. Typical Turn-Off Switching Time vs. R_G

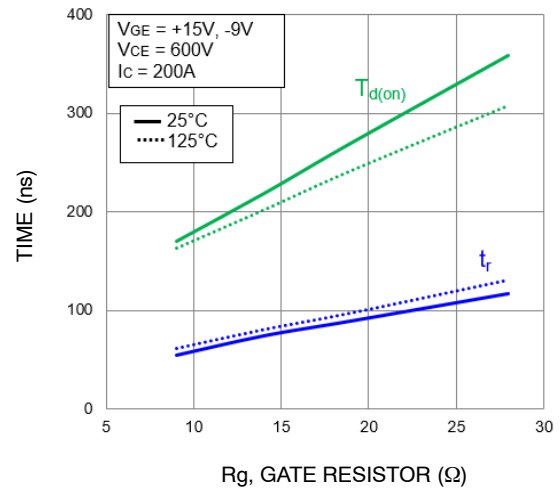


Figure 15. Typical Turn-On Switching Time vs. R_G

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – INNER IGBT (T2, T3)

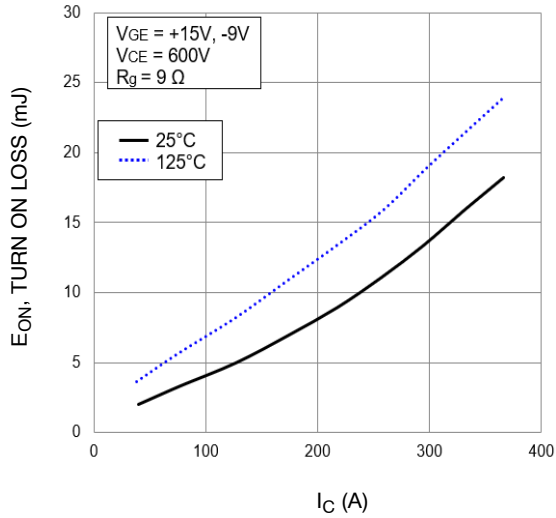


Figure 16. Typical Turn ON Loss vs. IC

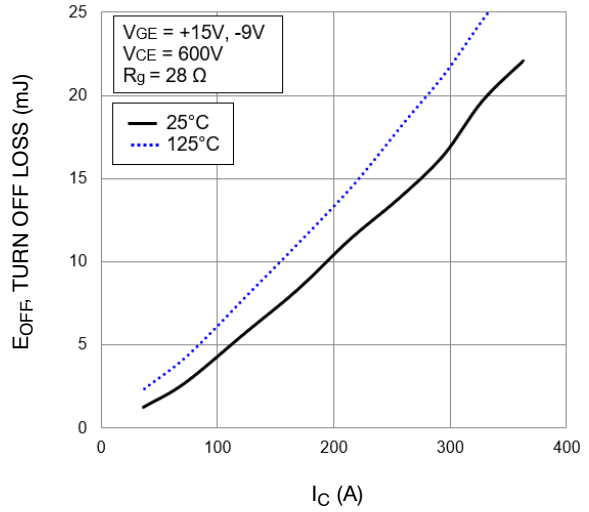


Figure 17. Typical Turn OFF Loss vs. IC

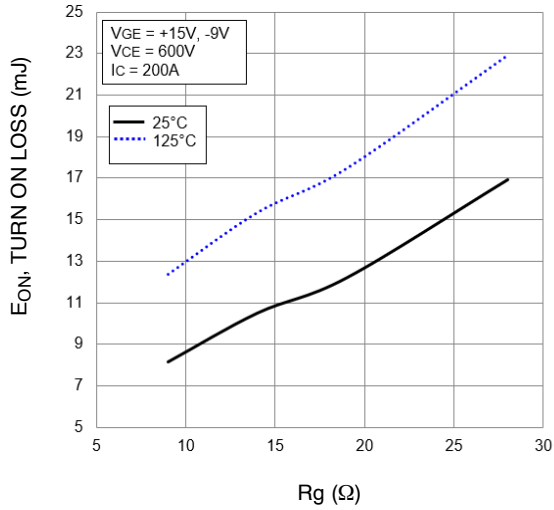


Figure 18. Typical Turn ON Loss vs. Rg

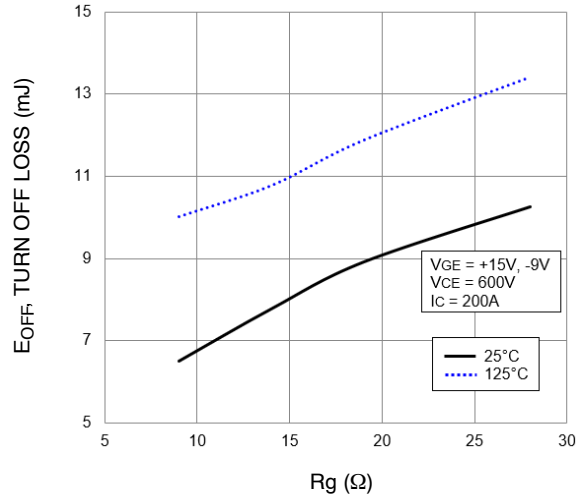


Figure 19. Typical Turn OFF Loss vs. Rg

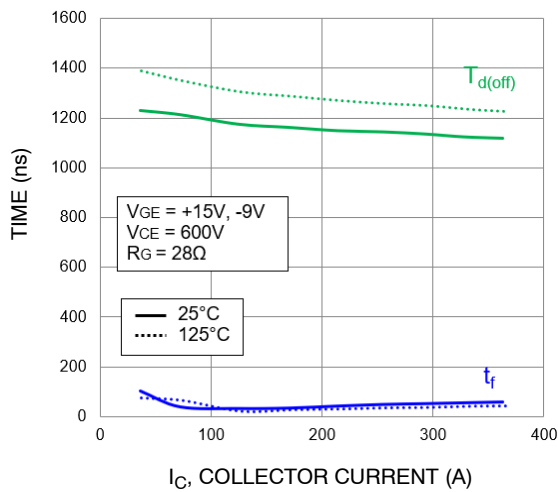


Figure 20. Typical Turn-Off Switching Time vs. IC

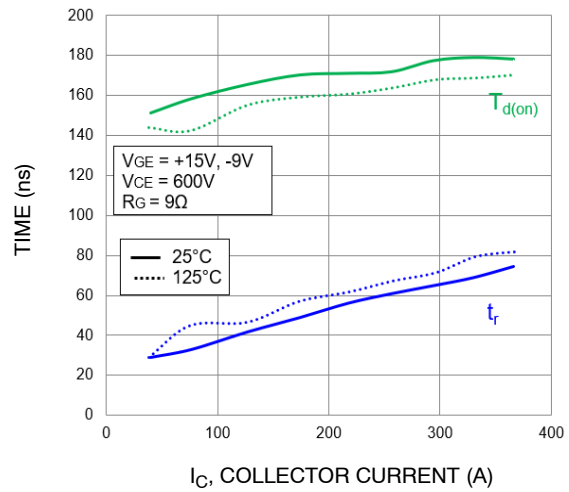


Figure 21. Typical Turn-On Switching Time vs. IC

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – INNER IGBT (T2, T3) (continued)

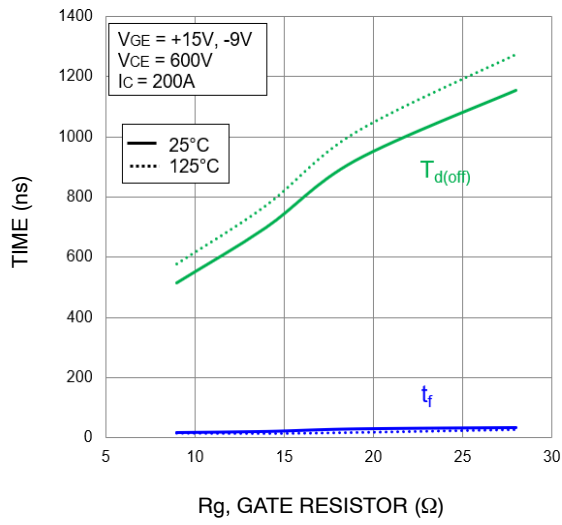


Figure 22. Typical Turn-Off Switching Time vs. RG

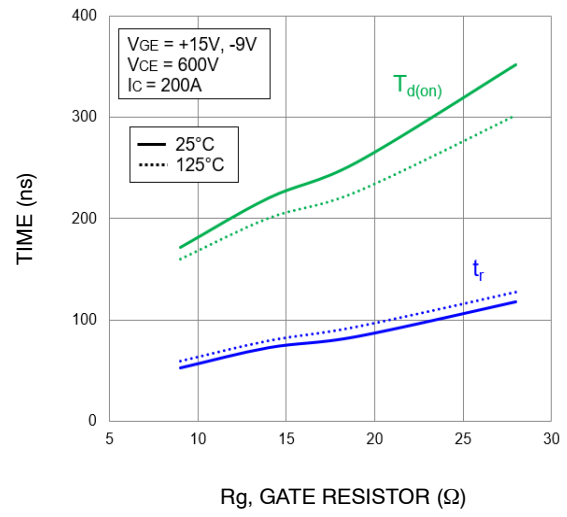


Figure 23. Typical Turn-On Switching Time vs. RG

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TYPICAL SWITCHING CHARACTERISTICS – NEUTRAL POINT DIODE

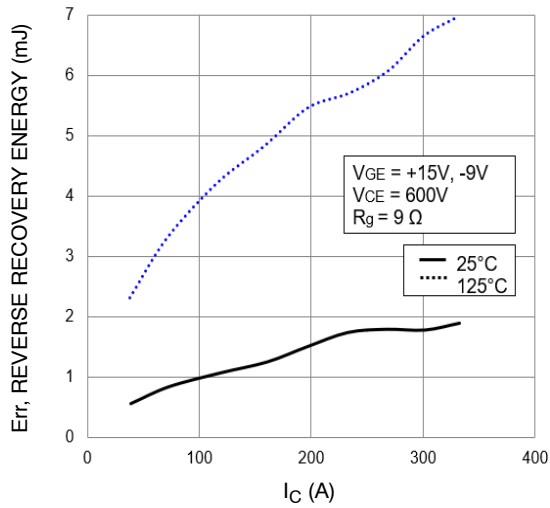


Figure 24. Typical Reverse Recovery Energy Loss vs. IC

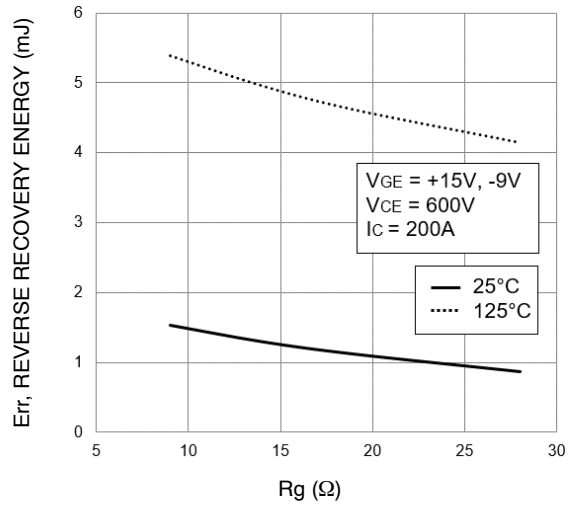


Figure 25. Typical Reverse Recovery Energy Loss vs. Rg

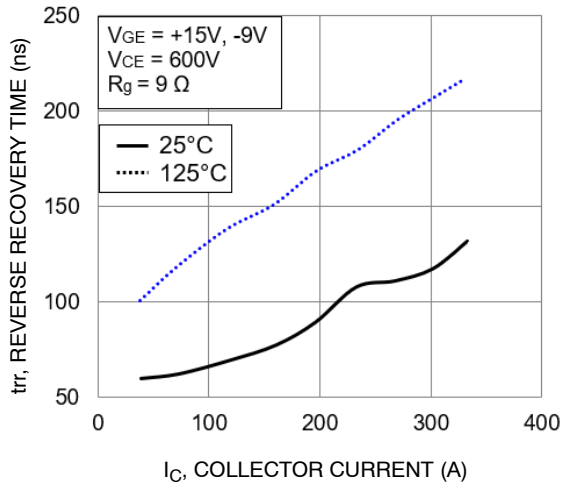


Figure 26. Typical Reverse Recovery Time vs. IC

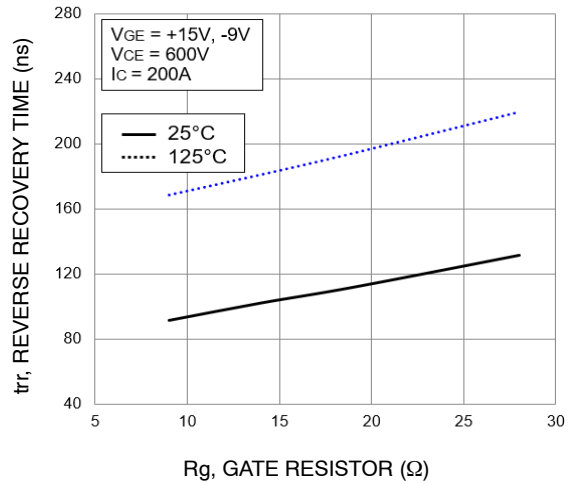


Figure 27. Typical Reverse Recovery Time vs. Rg

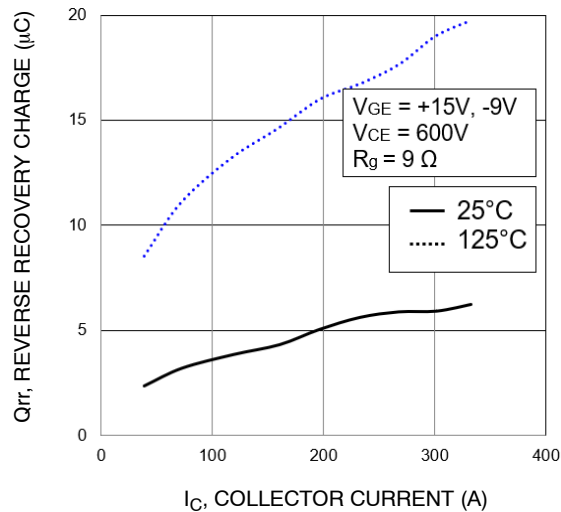


Figure 28. Typical Reverse Recovery Charge vs. IC

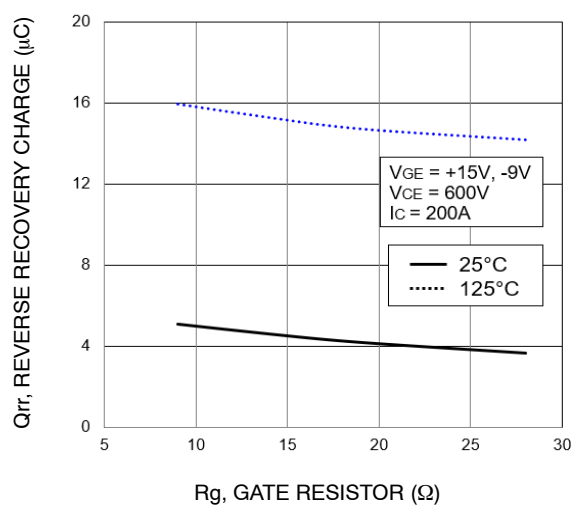


Figure 29. Typical Reverse Recovery Charge vs. Rg

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL SWITCHING CHARACTERISTICS – NEUTRAL POINT DIODE (continued)

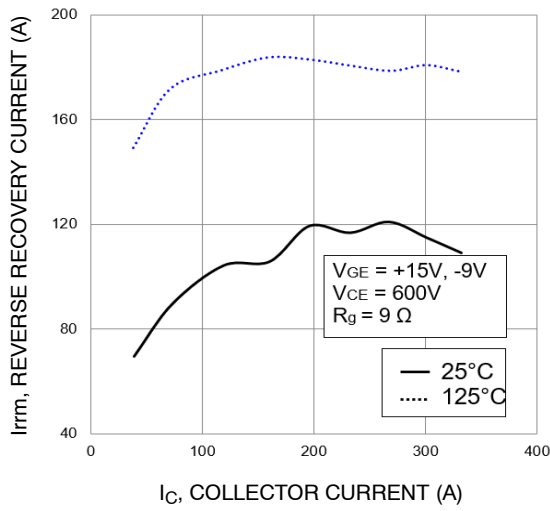


Figure 30. Typical Reverse Recovery Peak Current vs. I_C

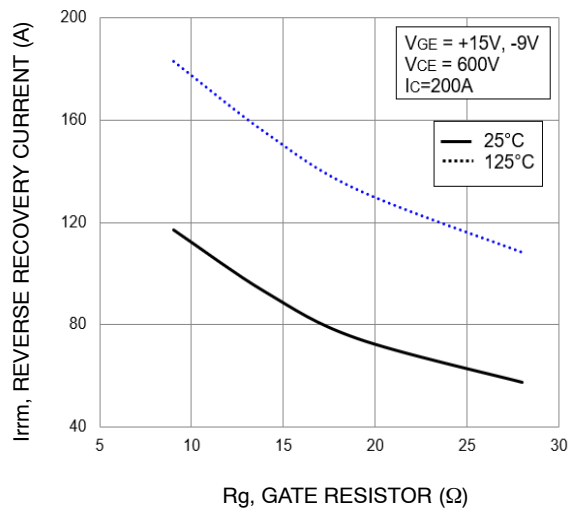


Figure 31. Typical Reverse Recovery Peak Current vs. R_g

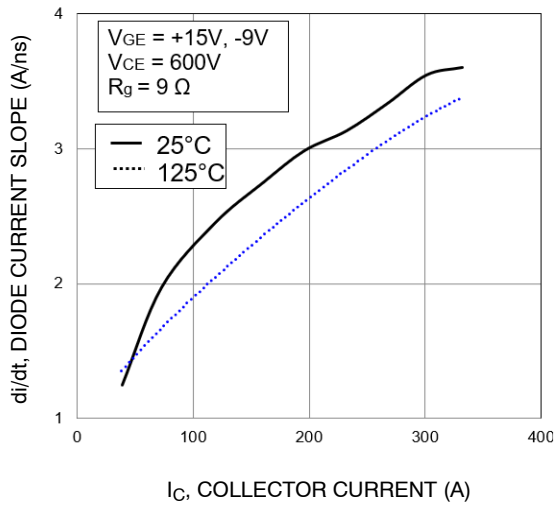


Figure 32. Typical di/dt vs. I_C

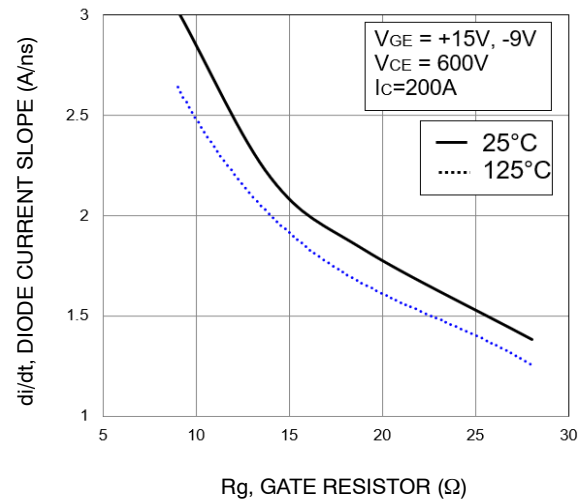


Figure 33. Typical di/dt vs. R_g

TYPICAL CHARACTERISTICS – INVERSE DIODE

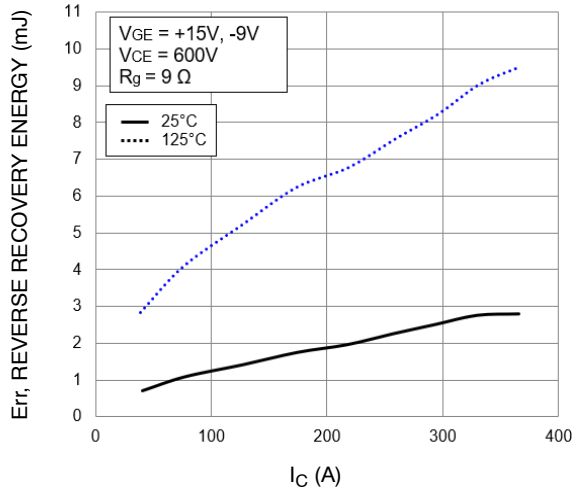


Figure 34. Typical Reverse Recovery Energy Loss vs. IC

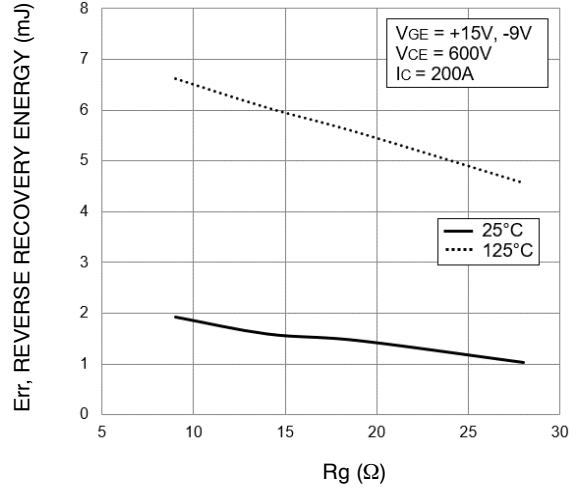


Figure 35. Typical Reverse Recovery Energy Loss vs. Rg

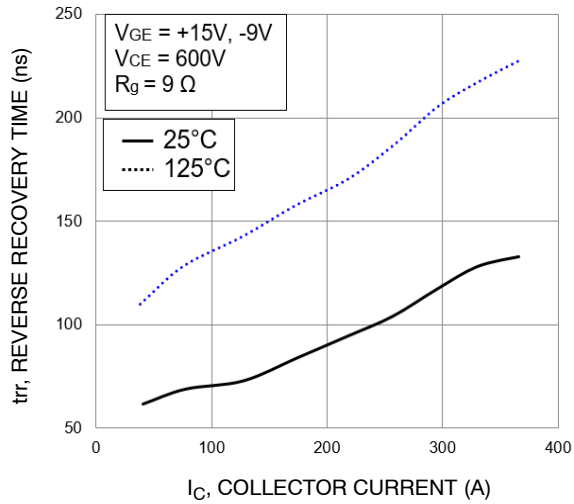


Figure 36. Typical Reverse Recovery Time vs. IC

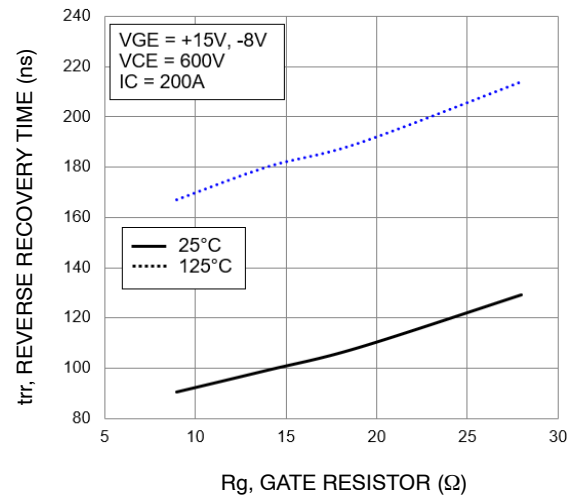


Figure 37. Typical Reverse Recovery Time vs. Rg

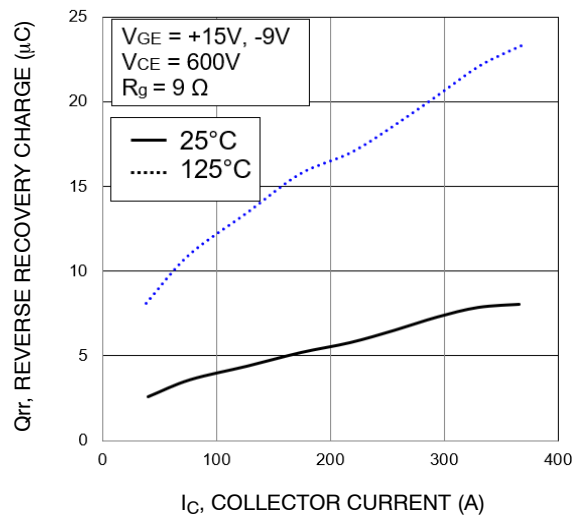


Figure 38. Typical Reverse Recovery Charge vs. IC

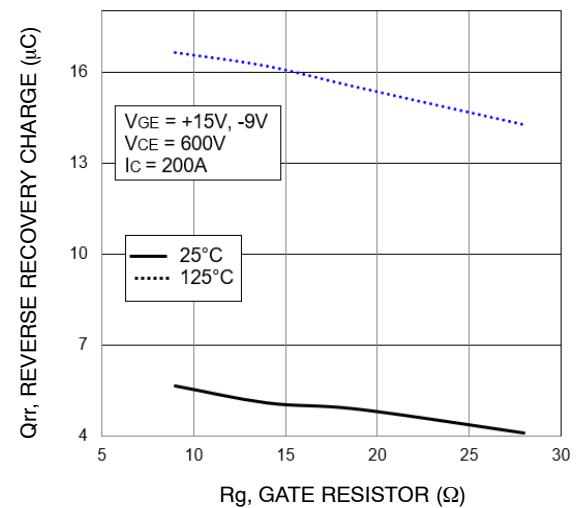


Figure 39. Typical Reverse Recovery Charge vs. Rg

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – INVERSE DIODE (continued)

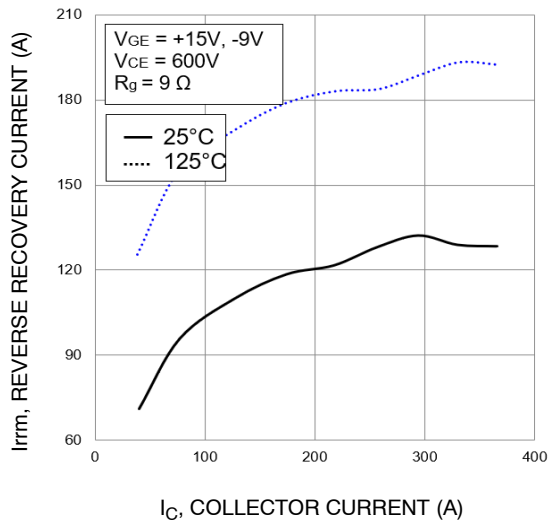


Figure 40. Typical Reverse Recovery Peak Current vs. IC

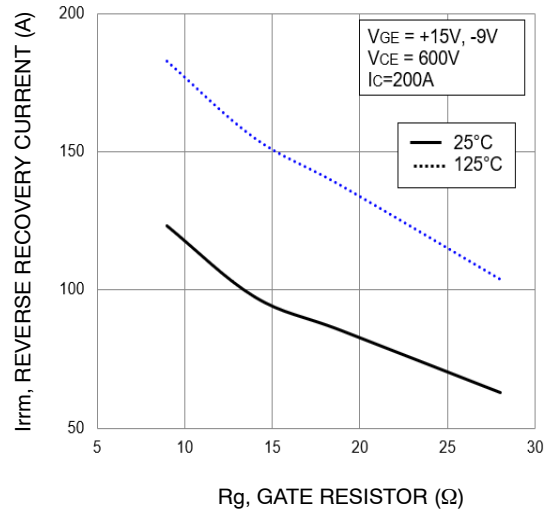


Figure 41. Typical Reverse Recovery Peak Current vs. Rg

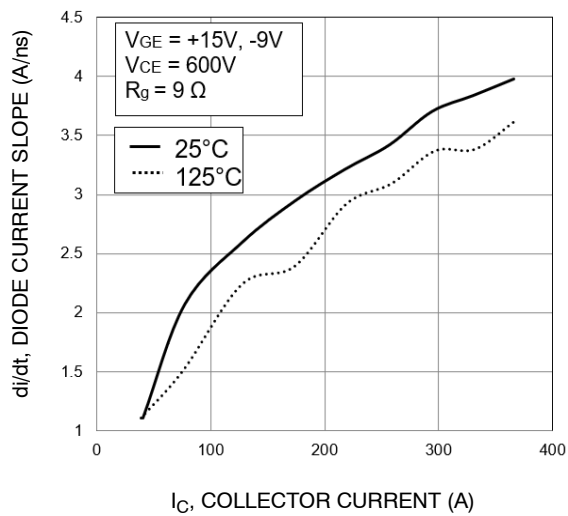


Figure 42. Typical di/dt vs. IC

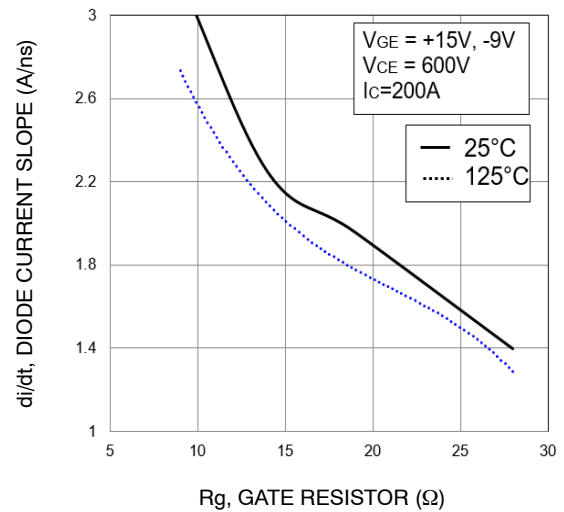


Figure 43. Typical di/dt vs. Rg

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – IGBT, INVERSE DIODE AND NEUTRAL POINT DIODE

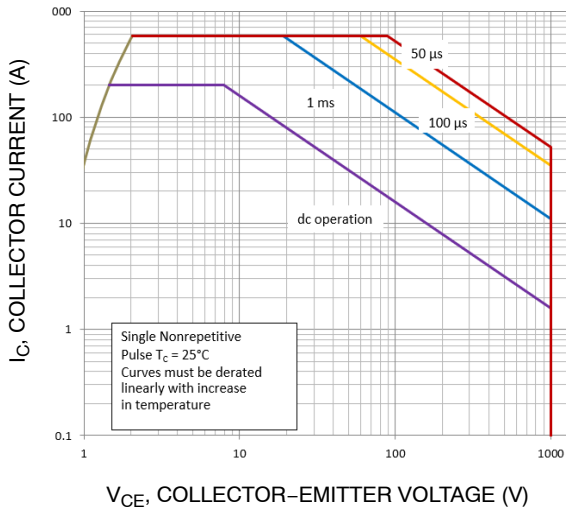


Figure 44. FBSOA – Outer IGBT

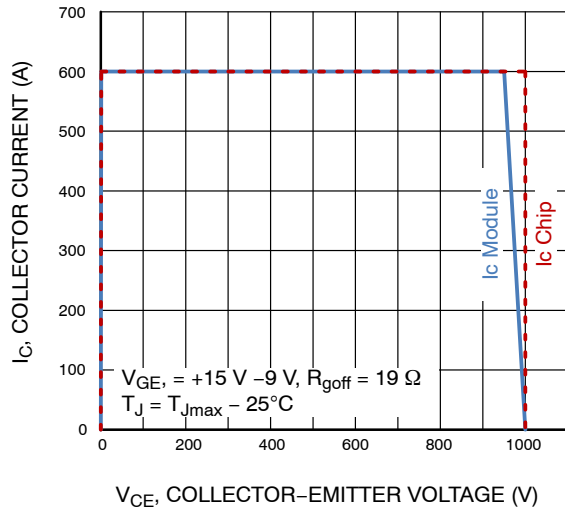


Figure 45. RBSOA – Outer IGBT

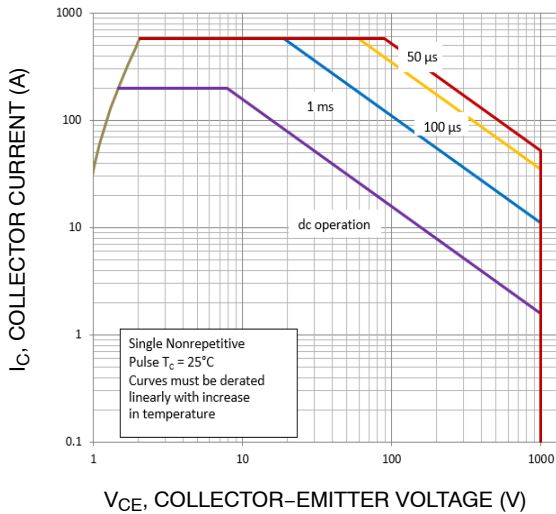


Figure 46. FBSOA – Inner IGBT

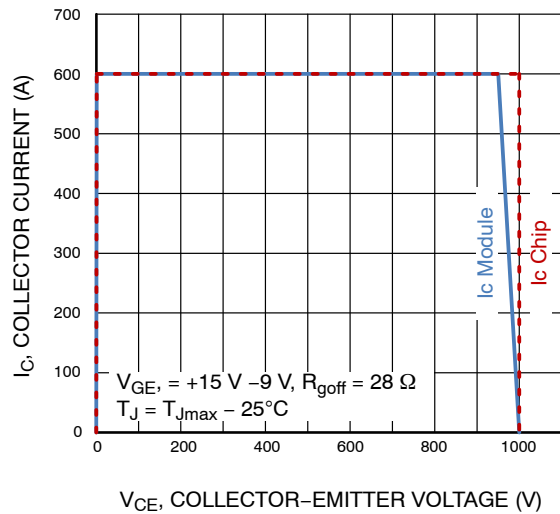


Figure 47. RBSOA – Inner IGBT

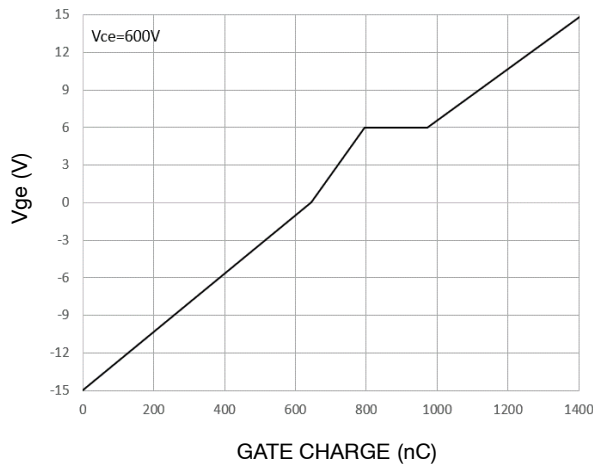


Figure 48. Gate Voltage vs. Gate Charge

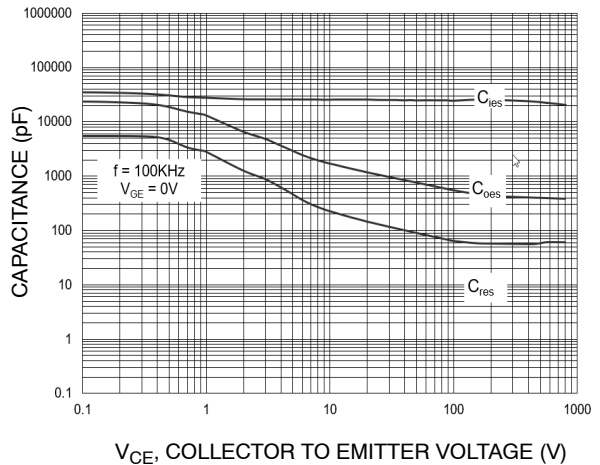


Figure 49. Capacitance Charge

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – IGBT, INVERSE DIODE AND NEUTRAL POINT DIODE (continued)

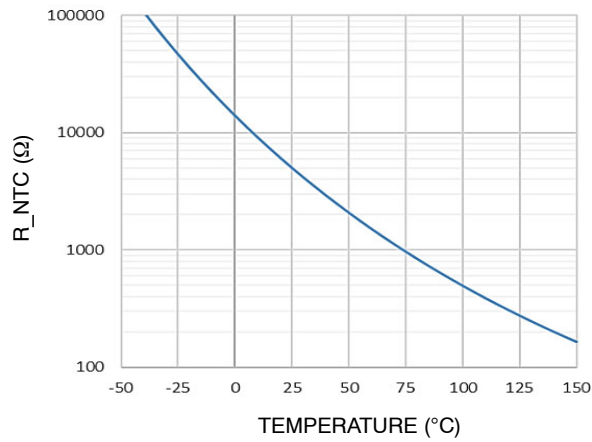


Figure 50. Thermistor Characteristics

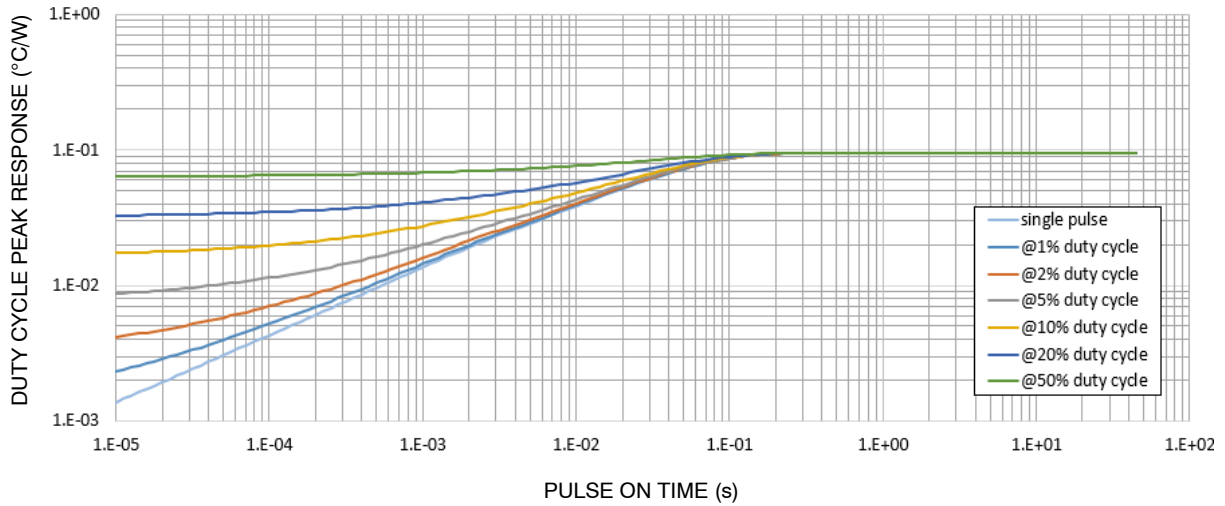


Figure 51. Transient Thermal Impedance – IGBT

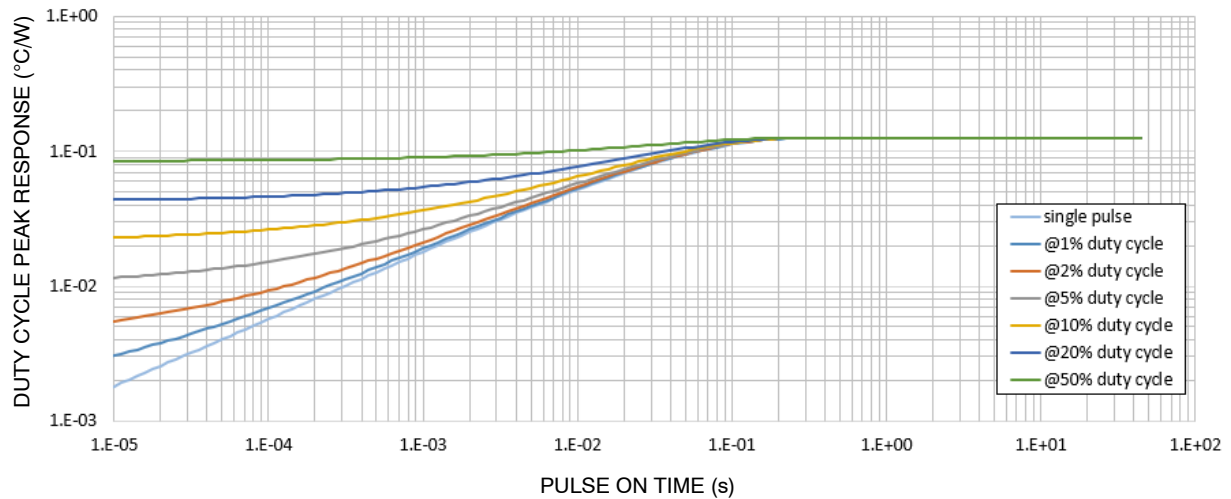


Figure 52. Transient Thermal Impedance – Inverse Diode

NXH400N100L4Q2F2SG, NXH400N100L4Q2F2PG

TYPICAL CHARACTERISTICS – IGBT, INVERSE DIODE AND NEUTRAL POINT DIODE (continued)

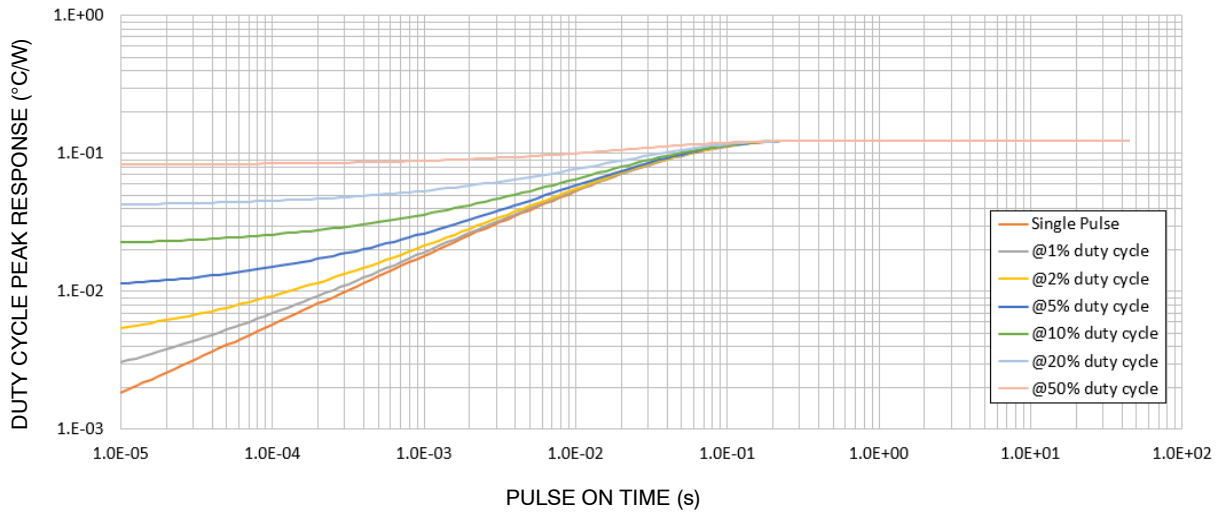
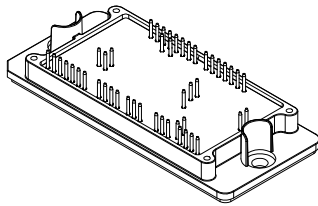


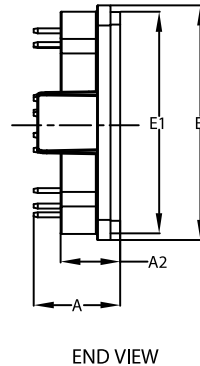
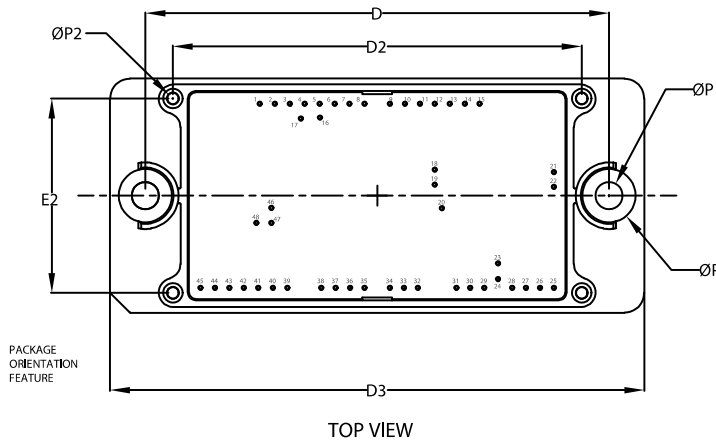
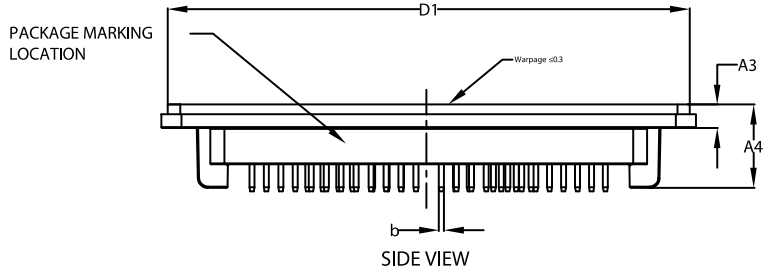
Figure 53. Transient Thermal Impedance – Neutral Point Diode

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**PIM48, 93x47 (SOLDER PIN)
CASE 180BL
ISSUE A**

DATE 08 DEC 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009
2. CONTROLLING DIMENSION : MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A1
4. PIN POSITION TOLERANCE IS $\pm 0.4\text{mm}$
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	16.80	17.20	17.60
A2	11.70	12.00	12.30
A3	4.40	4.70	5.00
A4	16.40	16.70	17.00
b	0.95	1.00	1.05
D	92.90	93.00	93.10
D1	104.45	104.75	105.05
D2	81.80	82.00	82.20
D3	106.90	107.20	107.50
E	46.70	47.00	47.30
E1	44.10	44.40	44.70
E2	38.80	39.00	39.20
P	5.40	5.50	5.60
P1	10.60	10.70	10.80
P2	1.80	2.00	2.20

S Pin position

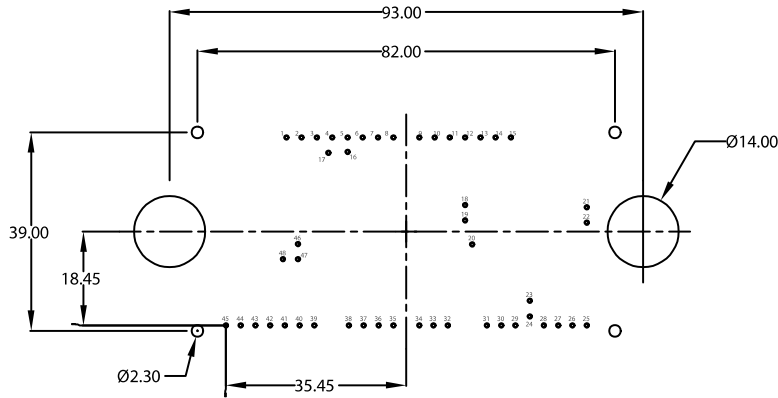
Pin table				Pin table			
Pin	X	Y	Function	Pin	X	Y	Function
1	11.9	36.9	Phase1	25	70.9	0	DC-
2	14.9	36.9	Phase1	26	68.1	0	DC-
3	17.9	36.9	Phase1	27	65.3	0	DC-
4	20.9	36.9	Phase1	28	62.5	0	DC-
5	23.9	36.9	Phase1	29	59.7	0	DC-
6	26.9	36.9	Phase1	30	56.9	0	DC-
7	29.9	36.9	Phase1	31	54.1	0	DC-
8	32.9	36.9	Phase1	32	51.3	0	DC-
9	38	36.9	Phase2	33	48.5	0	N2
10	41	36.9	Phase2	34	45.7	0	N2
11	44	36.9	Phase2	35	42.9	0	N1
12	47	36.9	Phase2	36	40.1	0	N1
13	50	36.9	Phase2	37	37.3	0	N1
14	53	36.9	Phase2	38	34.5	0	N1
15	56	36.9	Phase2	39	31.7	0	DC+
16	23.95	34.1	E2	40	28.9	0	DC+
17	20.15	33.9	G2	41	26.1	0	DC+
18	47	23.65	G3	42	23.3	0	DC+
19	47	20.65	E3	43	20.5	0	DC+
20	48.4	15.95	N	44	17.7	0	DC+
21	70.9	23.2	TH1	45	14.9	0	DC+
22	70.9	20.2	TH2	46	12.1	16	P
23	59.7	4.85	G4	47	9.3	13	E1
24	59.7	1.75	E4	48	6.5	13	G1

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DESCRIPTION:	PIM48, 93x47 (SOLDER PIN)	PAGE 1 OF 2

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PIM48, 93x47 (SOLDER PIN)
CASE 180BL
ISSUE A

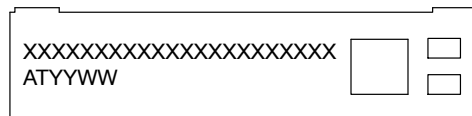
DATE 08 DEC 2022



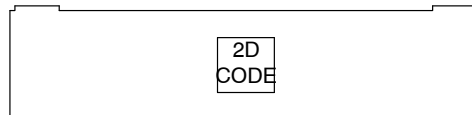
RECOMMENDED
MOUNTING PATTERN

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



FRONTSIDE MARKING



BACKSIDE MARKING

XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	PIM48, 93x47 (SOLDER PIN)	PAGE 2 OF 2

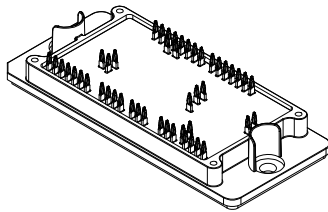
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

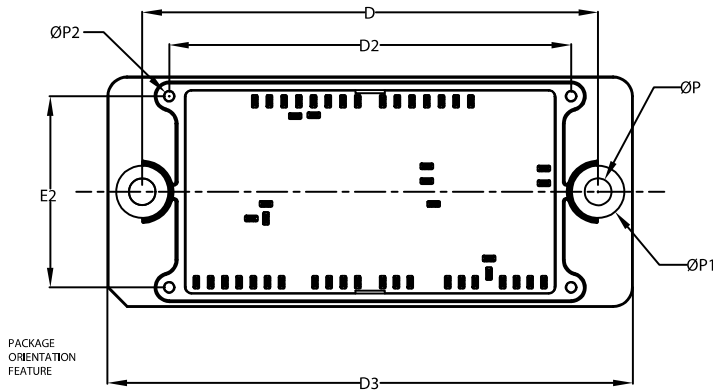
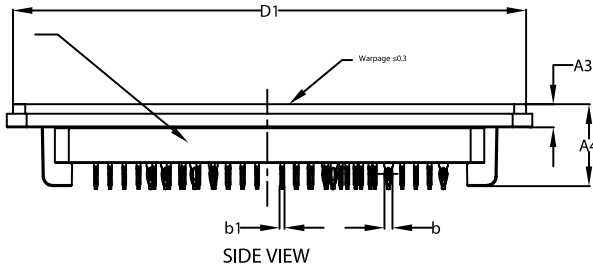


PIM48, 93x47 (PRESS-FIT PIN) CASE 180CR ISSUE A

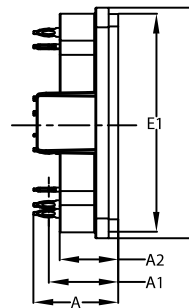
DATE 08 DEC 2022



PACKAGE MARKING LOCATION



TOP VIEW



END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009
2. CONTROLLING DIMENSION : MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A1
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DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	16.90	17.30	17.70
A1	13.97	14.18	14.39
A2	11.70	12.00	12.30
A3	4.40	4.70	5.00
A4	16.40	16.70	17.00
b	1.61	1.66	1.71
b1	0.75	0.80	0.85
D	92.90	93.00	93.10
D1	104.45	104.75	105.05
D2	81.80	82.00	82.20
D3	106.90	107.20	107.50
E	46.70	47.00	47.30
E1	44.10	44.40	44.70
E2	38.80	39.00	39.20
P	5.40	5.50	5.60
P1	10.60	10.70	10.80
P2	1.80	2.00	2.20

S Pin position

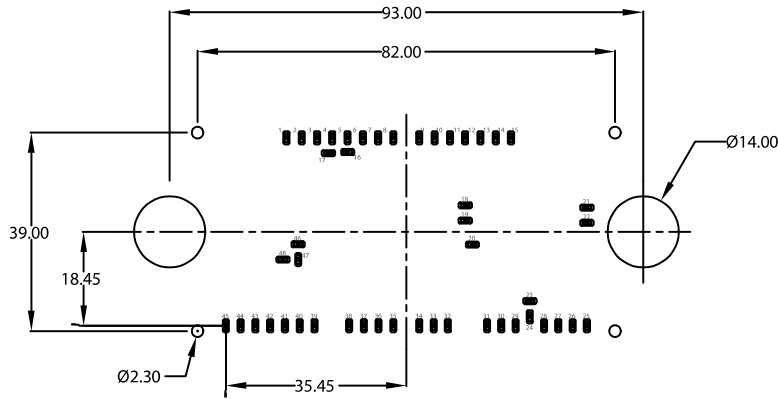
Pin table				Pin table			
Pin	X	Y	Function	Pin	X	Y	Function
1	11.9	36.9	Phase1	25	70.9	0	DC-
2	14.9	36.9	Phase1	26	68.1	0	DC-
3	17.9	36.9	Phase1	27	65.3	0	DC-
4	20.9	36.9	Phase1	28	62.5	0	DC-
5	23.9	36.9	Phase1	29	59.7	0	DC-
6	26.9	36.9	Phase1	30	56.9	0	DC-
7	29.9	36.9	Phase1	31	54.1	0	DC-
8	32.9	36.9	Phase1	32	51.3	0	DC-
9	38	36.9	Phase2	33	48.5	0	DC-
10	41	36.9	Phase2	34	45.7	0	DC-
11	44	36.9	Phase2	35	42.9	0	DC-
12	47	36.9	Phase2	36	40.1	0	DC-
13	50	36.9	Phase2	37	37.3	0	DC-
14	53	36.9	Phase2	38	34.5	0	DC-
15	56	36.9	Phase2	39	31.7	0	DC-
16	23.95	34.1	E2	40	28.9	0	DC-
17	20.15	33.9	G2	41	26.1	0	DC-
18	47	23.65	G3	42	23.3	0	DC-
19	47	20.65	E3	43	20.5	0	DC-
20	48.4	15.95	N	44	17.7	0	DC-
21	70.9	23.2	TH1	45	14.9	0	DC-
22	70.9	20.2	TH2	46	12.1	16	P
23	59.7	4.85	G4	47	9.3	13	E1
24	59.7	1.75	E4	48	6.5	13	G1

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PIM48, 93x47 (PRESS-FIT PIN)
CASE 180CR
ISSUE A

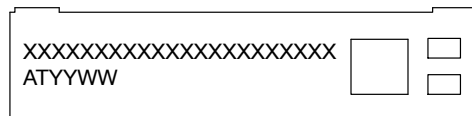
DATE 08 DEC 2022



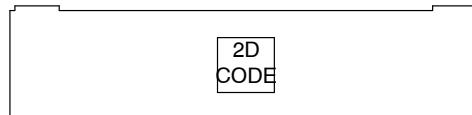
RECOMMENDED
MOUNTING PATTERN

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



FRONTSIDE MARKING



BACKSIDE MARKING

XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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