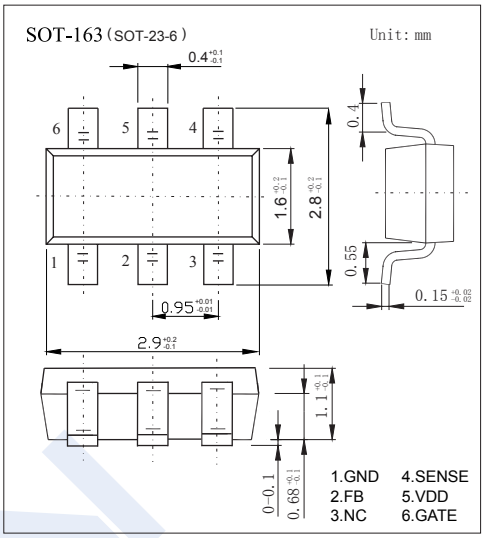
Current Mode PWM Controller

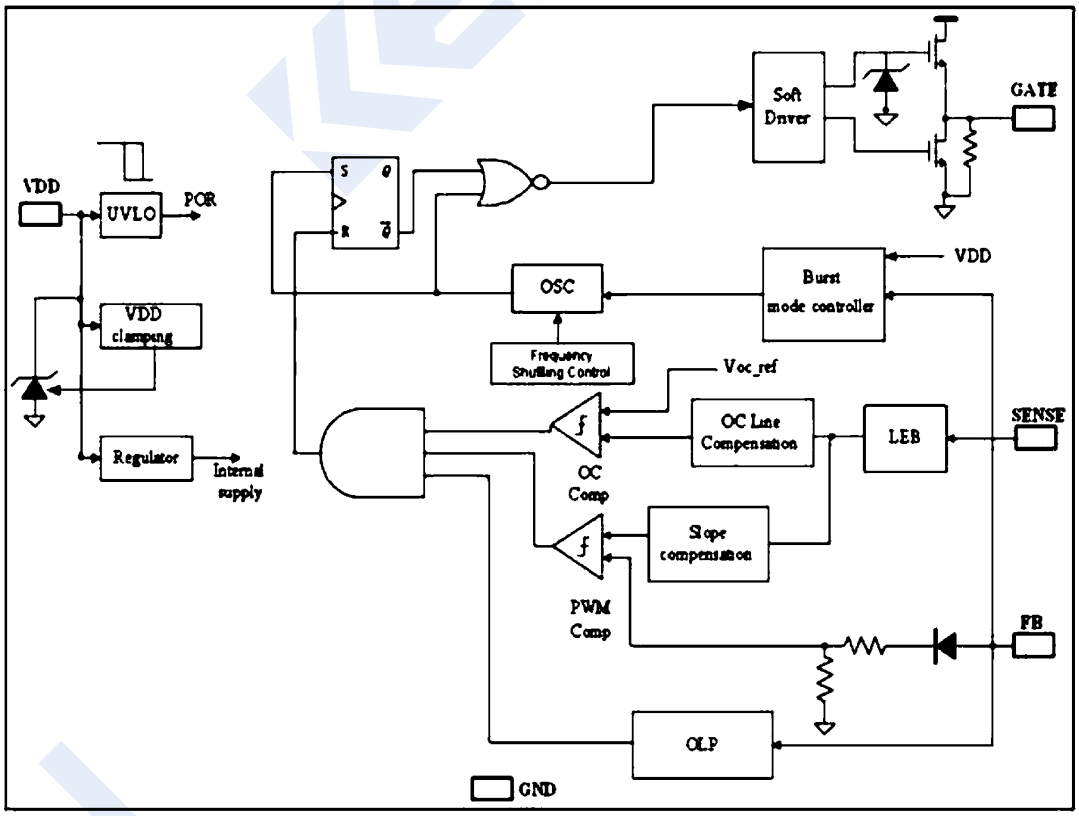
OB2263



■ Features

- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current (1.4mA)
- Leading Edge Blanking on Current Sense Input
- Good Protection Coverage With Auto Self-Recovery
- Gate Output Maximum Voltage Clamp (13V)
- Overload Protection (OLP)

■ Block Diagram



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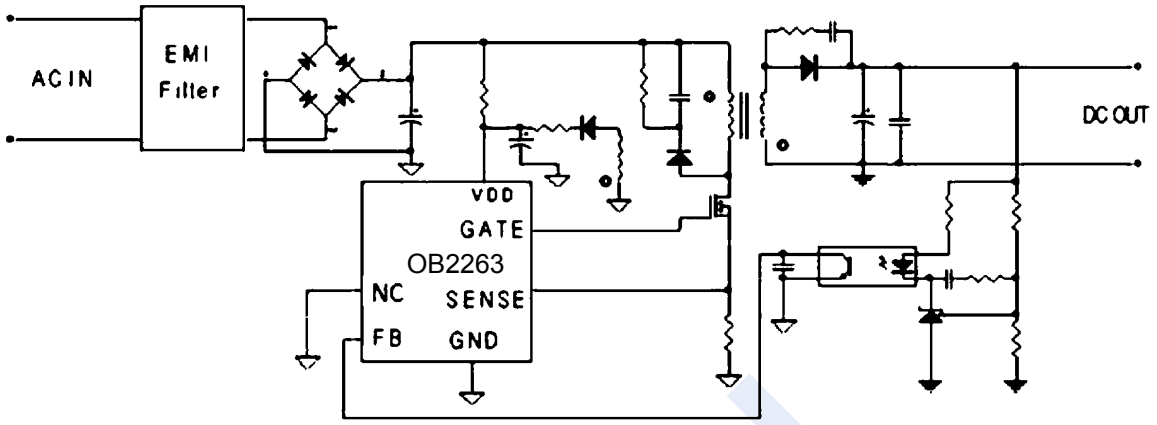
■ Typical Applicattion



■ Terminal Assignments

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
NC		
SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
VDD	P	Chip DC power supply pin.
GATE	O	Totem-pole gate drive output for the power MOSFET.

■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
DC supply voltage	V_{DD}	10 to 30	V
VDD Zener Clamp Voltage FB	V_{CC}	VDD_Clamp+0.1V	
V_{FB} Input Voltage	V_{FB}	-0.3 to 7	
V_{SENSE} Input Voltage to Sense Pin	V_{SENSE}	-0.3 to 7	
VCC DC clamp current	I_{CC}	10	mA
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	200	℃/W
Junction Temperature	T_J	-20 to 150	℃
Operating temperature	T_{OPT}	-20 to 85	
Storage Temperature Range	Tstg	-55 to 160	

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn on threshold Voltage	UVLO_ON		7.5	8.5	9.5	V
Turn-off threshold Voltage	UVLO_OFF		13.5	14.5	15.5	
Start up current	I_VCC_ST	V_{DD} =12.5V			20	uA
Operation Current	I_VCC_OP	V_{DD}=16V, V_{FB}=3V		1.4		mA
VCC Zener Clamp	VCC_Clamp	I_{VCC}= 5 mA		34		V
V_{FB} Open Loop Voltage	V_{FB}_Open	ΔV_{FB} /ΔVcs		4.8		
PWM input gain ΔVfb/ΔVcs	Avcs			2		V/V
FB Pin Short Current	IFB_Short	FB Shorted to GND		0.4		mA
Zero Duty Cycle FB Threshold Voltage	V_{TH}_0D	V_{DD} =16V			0.75	V
Power limiting FB Threshold	V_{TH}_PL			3.7		
Power limiting Debounce	T_D_PL			47		mS
Input Impedance	Z_{FB}_IN			6		kΩ
Maximum duty cycle	Max_Duty	V_{DD}=18V, FB=3V, CS=0		75		%
Leading edge Blanking Time	TLEB			330		nS
Input impedance	Z_{CS}			40		kΩ
OCP control delay	T_D_OC	GATE with 1nF to GND		120		nS
OCP threshold	V_{TH}_OC	FB=3.3V	0.75	0.8	0.85	V
Normal Oscillation Frequency	Fosc		60		70	KHz
Burst Mode Base Frequency	Fosc_BM	V_{DD} = 16V		22		
Frequency variation versus temp. Deviation	Δf_temp	V_{DD}=16V,Ta = -20 to 85℃		5		%
Frequency variation versus V_{CC}	Δf_V_{CC}	V_{CC} = 12 to 25V		5		
Frequency Jittering	Δf_OSC		-3		3	
Shuffling Frequency	F_shuffling			65		Hz
Output voltage Low	VOL	V_{CC} = 16V, Io = -20mA			0.8	V
Output High Level	VOH	V_{DD} = 16V, Io = 20 mA	10			
Output clamp voltage	Vclamp			13		
Rising time	Tr	V_{DD} = 16V, CL = 1nf		200		ns
Falling time	Tf	V_{DD} = 16V, CL = 1nf		70		

■ Marking

Marking	63**

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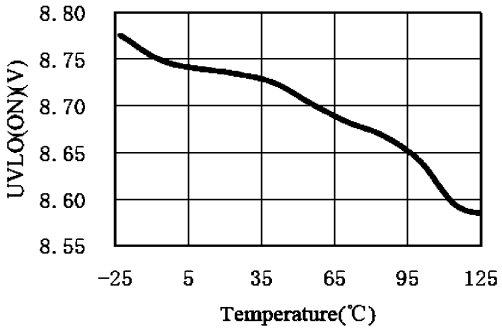
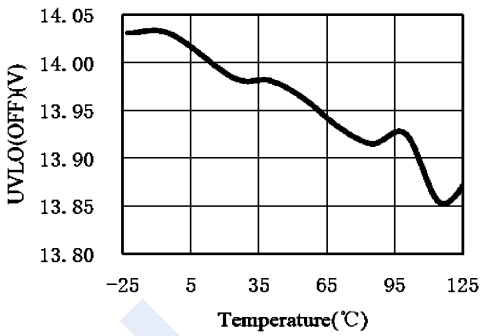
■ Typical Characterisitics

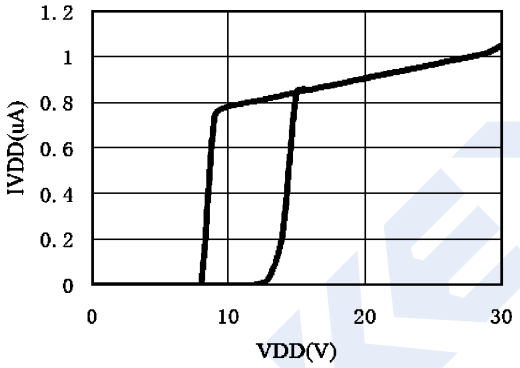
UVLO(ON) vs Temperature



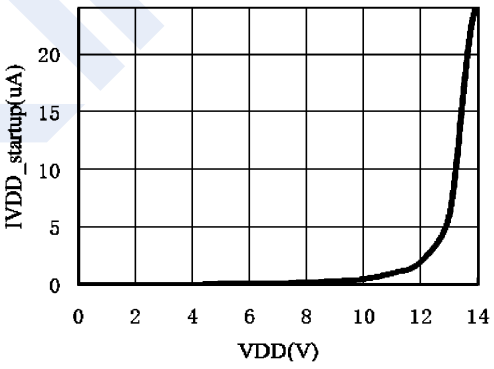
UVLO(OFF) vs Temperature



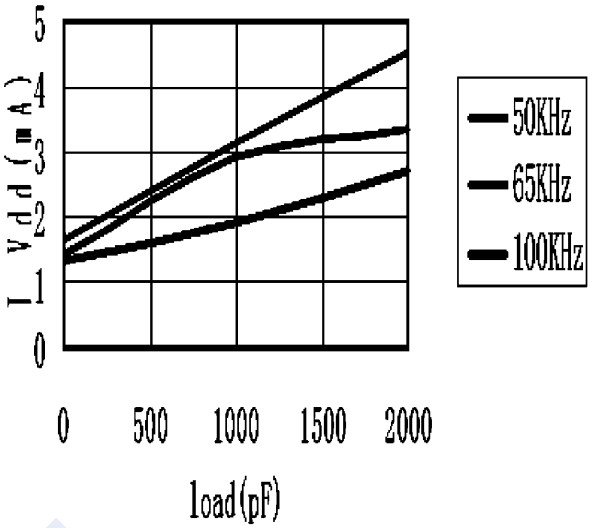
IVDD vs VDD



IVDD_startup vs VDD



I_Vdd vs Gate load



Fosc vs Temperature