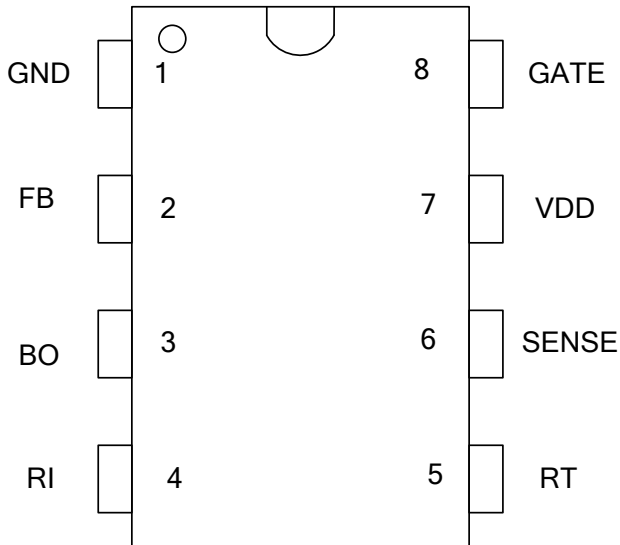


GENERAL INFORMATION

Pin Configuration

The pin map of OB2288 in DIP8 and SOP8 package is shown as below.



Ordering Information

Part Number	Description
OB2288AP	DIP8, Pb-free in Tube
OB2288CP	SOP8, Pb-free in Tube
OB2288CPA	SOP8, Pb-free in Taping

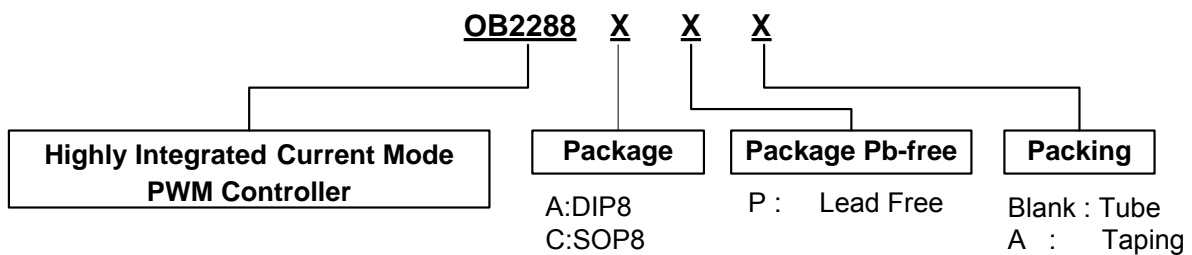
Package Dissipation Rating

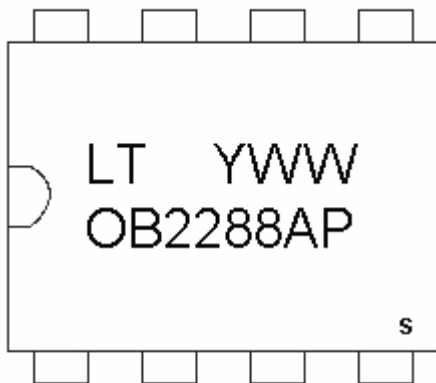
Package	R θ JA (°C/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

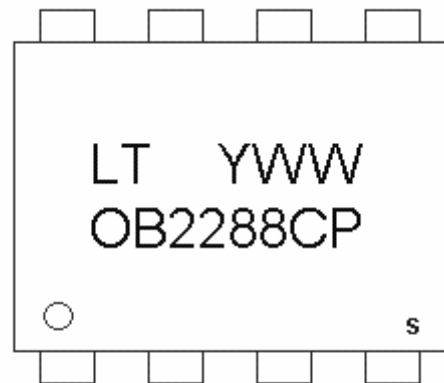
Parameter	Value
VDD Zener Clamp Voltage (V _{clamp})	31 V
VDD Zener Clamp Continuous Current	10 mA
BO Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
SENSE Input Voltage	-0.3 to 7V
RT Input Voltage	-0.3 to 7V
RI Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T _j	-20 to 150 °C
Min/Max Storage Temperature T _{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information
DIP8


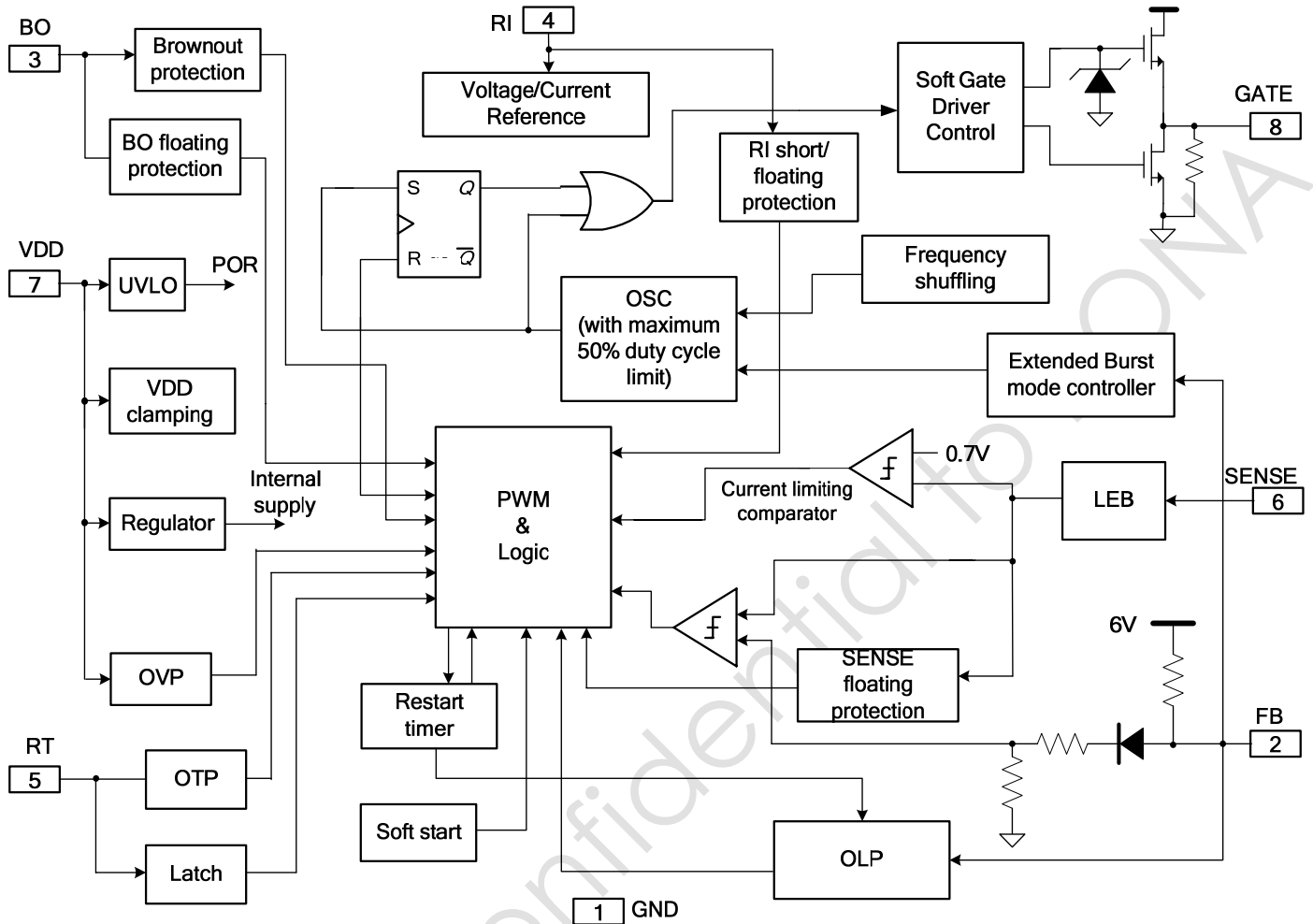
A: DIP8 Package
 P: Pb-free Package
 Y: Year Code(0-9)
 WW: Week Code(01-52)
 S: Internal Code

SOP8


C: SOP8 Package
 P: Pb-free Package
 Y: Year Code(0-9)
 WW: Week Code(01-52)
 S: Internal Code

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground.
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level at this pin and current-sense signal level at Pin 6.
3	BO	I/O	Brownout detection pin. Detects line voltage through a resistor divider. If the voltage at this pin drops below 1.05V and lasts 50ms, brownout is triggered and PWM output will be disabled.
4	RI	I	Internal oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Dual function pin. Either connected through a NTC resistor to GND for over temperature shutdown control or used as latch shutdown control input.
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	P	DC power supply pin.
8	GATE	O	Totem-pole gate drive output for power MOSFET.

BLOCK DIAGRAM

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	11.5	25	V
RI	RI Resistor Value	10	40	Kohm
T _A	Operating Ambient Temperature	-20	85	°C

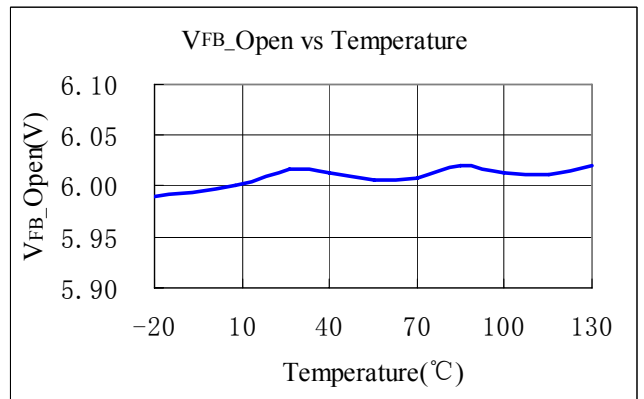
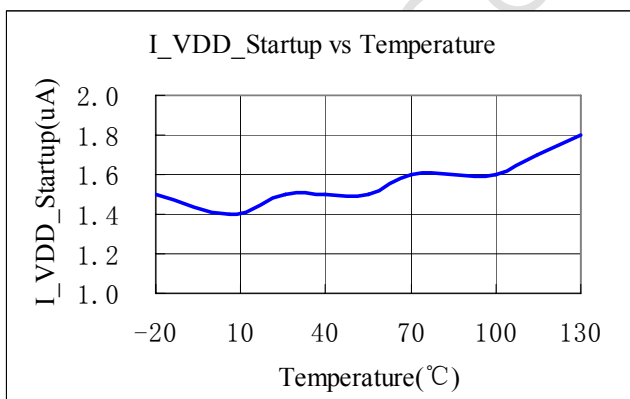
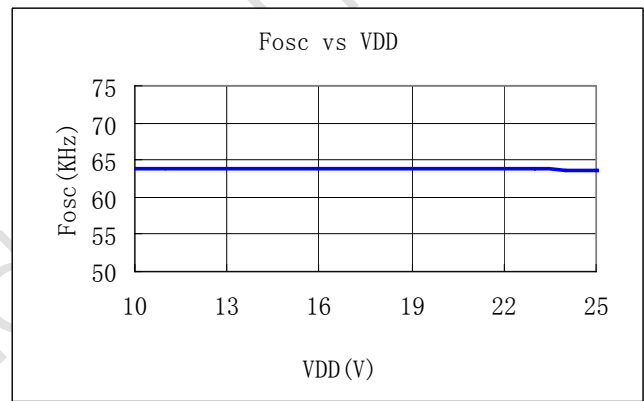
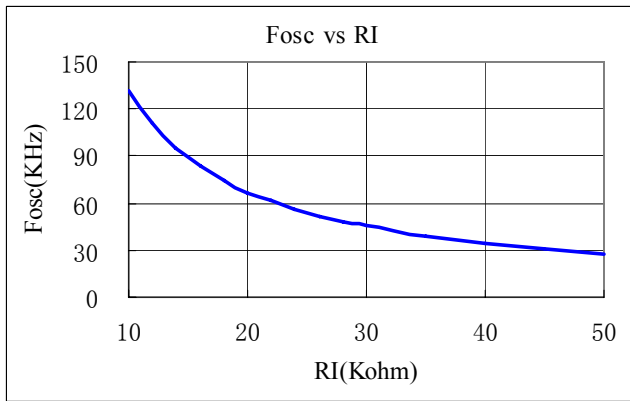
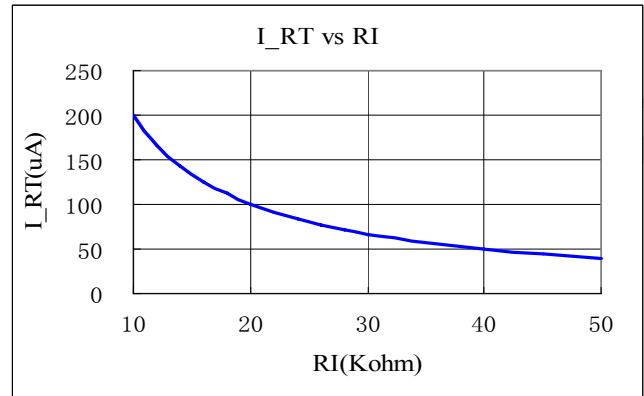
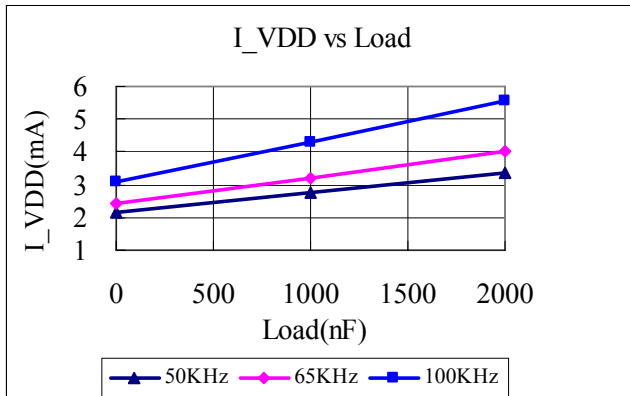
ELECTRICAL CHARACTERISTICS

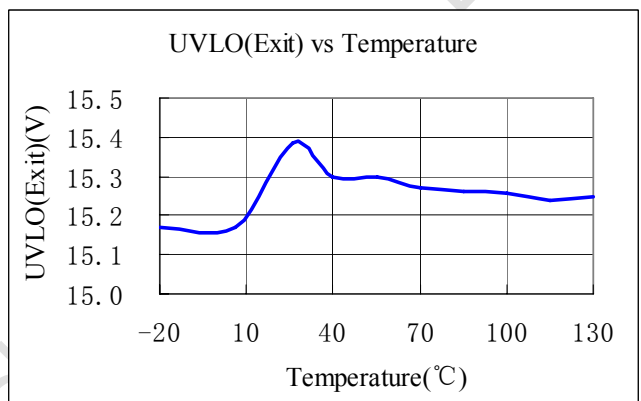
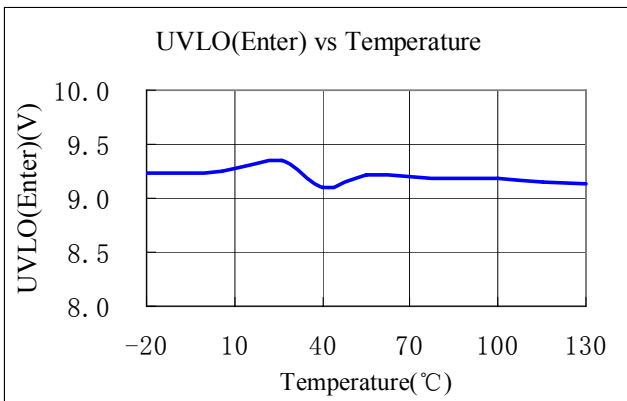
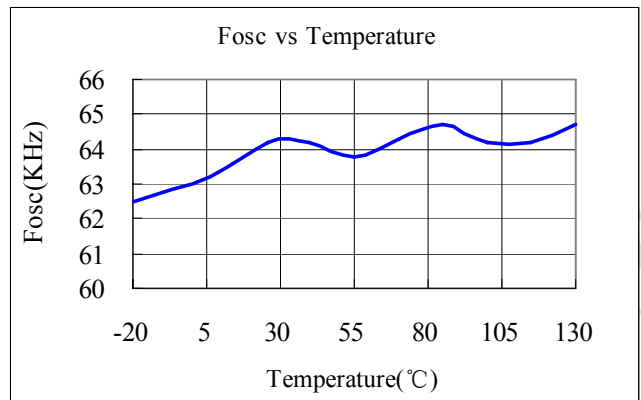
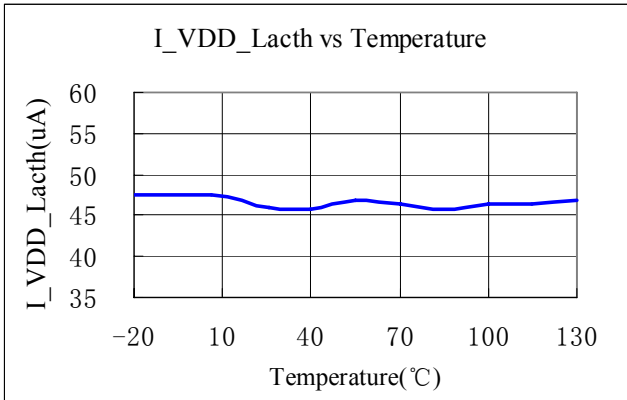
 (T_A = 25°C, R_I=20K ohm, V_{DD}=16V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
I _{VDD_Startup}	VDD Startup Current	VDD=13.5V		5	20	uA
I _{VDD_Ops}	Operation Current	V _{FB} =3V		2.3		mA
UVLO(Enter)	VDD Under Voltage Lockout Enter		8	9	10	V
UVLO(Exit)	VDD Under Voltage Lockout Exit		14.2	15.2	16.2	V
OVP	VDD Over Voltage Protection		26	28	30	V
T _{D_OVP}	VDD OVP Debounce Time			100		uSec
VDD_De-Latch	Latch Release Voltage Threshold			6.5		V
I _{VDD_Latch}	VDD Current at Latch Shutdown	VDD=8V		45		uA
V _{DD_Clamp}	V _{DD} Zener Clamp Voltage	I(V _{DD}) = 15 mA		31		V
T _{Softstart}	Soft Start Time			4		mSec
Feedback Input Section(FB Pin)						
A _{VCS}	PWM Input Gain	$\Delta V_{FB} / \Delta V_{cs}$		2.2		V/V
V _{FB_Open}	FB Pin Open Voltage	VDD=18V		6		V
I _{FB_max}	FB Pin Maximum Source Current	VDD=18V, Short FB pin to GND.		1.1		mA
V _{FB_TH}	Zero Duty Cycle Threshold Voltage	VDD=9.5V, V _{sense} =0V	0.9	1	1.1	V
V _{TH_BM}	Burst Mode FB Threshold Voltage			1.6		V
V _{TH_PL}	Power Limiting FB Threshold Voltage			4.4		V
T _{D_PL}	Power Limiting Debounce Time			250		mSec
Z _{FB_IN}	Input Impedance			6		Kohm
Current Sense Input(Sense Pin) Section						
T _{blanking}	Sense Input Leading Edge Blanking Time	VDD=18V		300		nSec
V _{TH_OC}	Internal Current Limiting Comparator Threshold		0.67	0.7	0.73	V
T _{D_OC}	Propagation delay to GATE	CL=1nF at GATE		70		nSec
Oscillator Section						
F _{osc}	Normal Oscillation Frequency		60	65	70	KHz
ΔF(shuffle)/Fosc	Frequency Shuffling Range		-4		4	%
F _{shuffle}	Frequency Shuffling Cycling Frequency			32		Hz
Δf_Temp	Frequency Temperature Stability	-20°C to 100°C		3		%

Δf_{VDD}	Frequency Voltage Stability	VDD = 12-25V		3		%
Dmax	Max Duty Cycle		45	48	50	%
Dmin	Min Duty Cycle		-	-	0	%
RI_range	Operating RI Range		10	20	40	Kohm
V_RI	RI Operation Voltage			2.0		V
F_BM	Burst Mode Pulse Switching Frequency			22		KHz
Gate Drive Output						
VOL	Low Output Voltage	Io = 30 mA (sink)			0.3	V
VOH	High Output Voltage	Io = 30 mA (source)	11			V
VG_Clamp	Output Clamp Voltage	VDD=25V		17		V
T_r	Rising Time	CL = 1nF, 10-90%.		70		nSec
T_f	Falling Time	CL = 1nF, 10-90%.		30		nSec
Over Temperature Protection						
I_RT	RT Pin Source Current	VDD = 18V		100		uA
V _{TH_OTP}	OTP Threshold Voltage	VDD = 18V	1.0	1.05	1.1	V
V _{TH_OTP_off}	OTP Recovery Threshold Voltage	VDD = 18V		1.15		V
V _{TH_RT_latch}	RT Input Latch Threshold Voltage	VDD = 18V		0.6		V
T _{D_OTP}	OTP De-bounce Time	VDD = 18V		100		uSec
V_RT_Open	RT Pin Floating Voltage	VDD = 18V		3.2		V
Brownout Section						
V _{th_BO}	Brownout Threshold		1.0	1.05	1.1	V
T _{D_BO}	Brownout Debounce Time			50		mSec
IBO_hys	Source Current for Brownout Hysteresis Programming			2		uA
Restart Timer Section						
RST_auto	Auto Recovery Restart Timer			1		Sec

CHARACTERIZATION PLOT





OPERATION DESCRIPTION

OB2288 is a highly integrated PWM controller IC optimized for forward mode converter applications. The versatile protections and high performance make it very suitable for large power applications.

● Startup Current and Startup Control

Startup current of OB2288 is designed to be very low so that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

● Operating Current

The Operating current of OB2288 is low at 2.3mA. Good efficiency is achieved with OB2288 low operating current together with extended burst mode control schemes at zero or light load condition.

● Extended Burst Mode Operation

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is proportional to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy.

OB2288 self adjusts the switching mode according to the loading condition. At no load or light load conditions, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend.

The nature of high frequency switching also reduces the audio noise at any loading conditions.

● Oscillator/Frequency Shuffling Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation

within the specified RI in Kohm range at nominal loading operational condition.

$$F_{osc} = \frac{1300}{RI(Kohm)} (Khz)$$

In OB2288, the proprietary frequency shuffling method can soften the EMI signature by spreading the energy in the vicinity of the main switching component and its harmonics. The magnitude of shuffling lies in the range of ±4% of the main switching frequency.

● Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2288 current mode PWM control. The switch current is detected by a sense resistor into the SENSE pin. An internal leading edge blanking circuit chops off the SENSE voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on SENSE input is no longer needed. The current limit comparator is disabled and can not turn off the external MOSFET during the blanking period. The PWM duty cycle is determined by the current SENSE input voltage and the FB input voltage.

● Over Temperature Protection with Latch Shutdown

A NTC resistor in series with a regular resistor should be connected between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With a fixed internal current I_{RT} flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shuts down the MOSFET when the sensed input voltage is lower than V_{TH_OTP} . It is selectable for auto recover or latched shutdown.

● RT Pin Used as Latch Shutdown Input Control

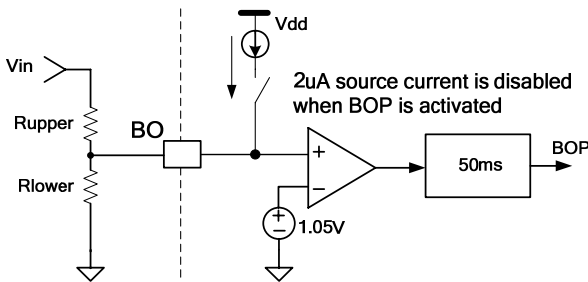
RT pin could also be used as a control input to implement system latch shutdown function.

An example is to implement system OVP protection with a latch shutdown function through a photo coupler and affiliated circuits. When OVP detection signal connected to RT is lower than V_{TH_OTP} OB2288 controls system into latch shutdown. The recovery of the AC/DC system could only be realized by resetting internal latch when VDD voltage drops below VDD_De-latch

value. This could be achieved by unplugging/re-plugging of AC source in AC start-up configuration.

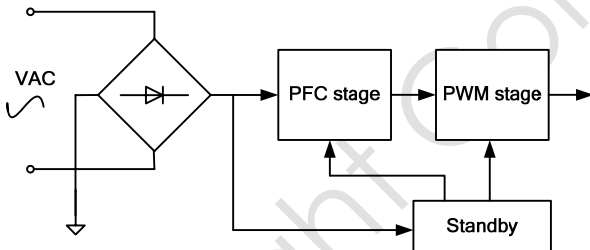
● **Brownout Protection**

By monitoring the voltage level on pin BO during normal operation, the controller protects the SMPS against low main condition. When BO voltage level falls below 1.05V, and if it lasts for about 50ms, the controller stops pulsing until this level goes back and the operation resumes. By adjusting the resistor divider connected between the high input voltage and this pin, start and stop levels are programmable.



● **Restart Timer**

In some special applications, such as LCDTV, the power supply of PWM stage is provided by other DC source and it is always on. The following diagram shows an AC/DC part of the LCDTV. The front end is a PFC stage, followed by a PWM stage. A stand alone standby converter provides the DC power supply for both PWM and PFC stages.



In such conditions, for example, when the over loading protection (OLP) occurs, PWM stage will be latched of and it will not recover since it is powered by the standby DC supply. OB2288 overcomes this shortcoming by an internal restart timer. When OLP occurs, the timer begins counting. When counting over, the OLP states will be cleared. System tends to restart and auto-recover. If OLP

still exists, then another counting cycle begins. The counting time in OB2288 is 1 second. Therefore, the nominal operation of OLP is not disturbed.

● **Pin Floating and Short Protection**

OB2288 provides pin floating protection for RI, SENSE, FB, etc., and RI pin short protection. In cases when the pin are floating or RI pin is shorted to ground, PWM switching is disabled, thus protect the power system.

● **Overload Operation**

When over load (for example, short circuit) occurs, a fault is detected. If this fault is present for more than 250ms, OB2288 enters an auto-recovery soft burst mode. All pulses are stopped, VDD will drops below UVLO and the controller will try to restart, with the power-on soft start. The SMPS resumes operation if the fault has gone. Otherwise, a burst sequence starts again.

● **Soft Start**

OB2288 features an internal 4ms soft start to soften the constraints occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(exit), the peak current is gradually increased from nearly zero to the maximum clamping level 0.7V. The soft start is also activated during OLP sequence. Every restart attempt is followed by soft start.

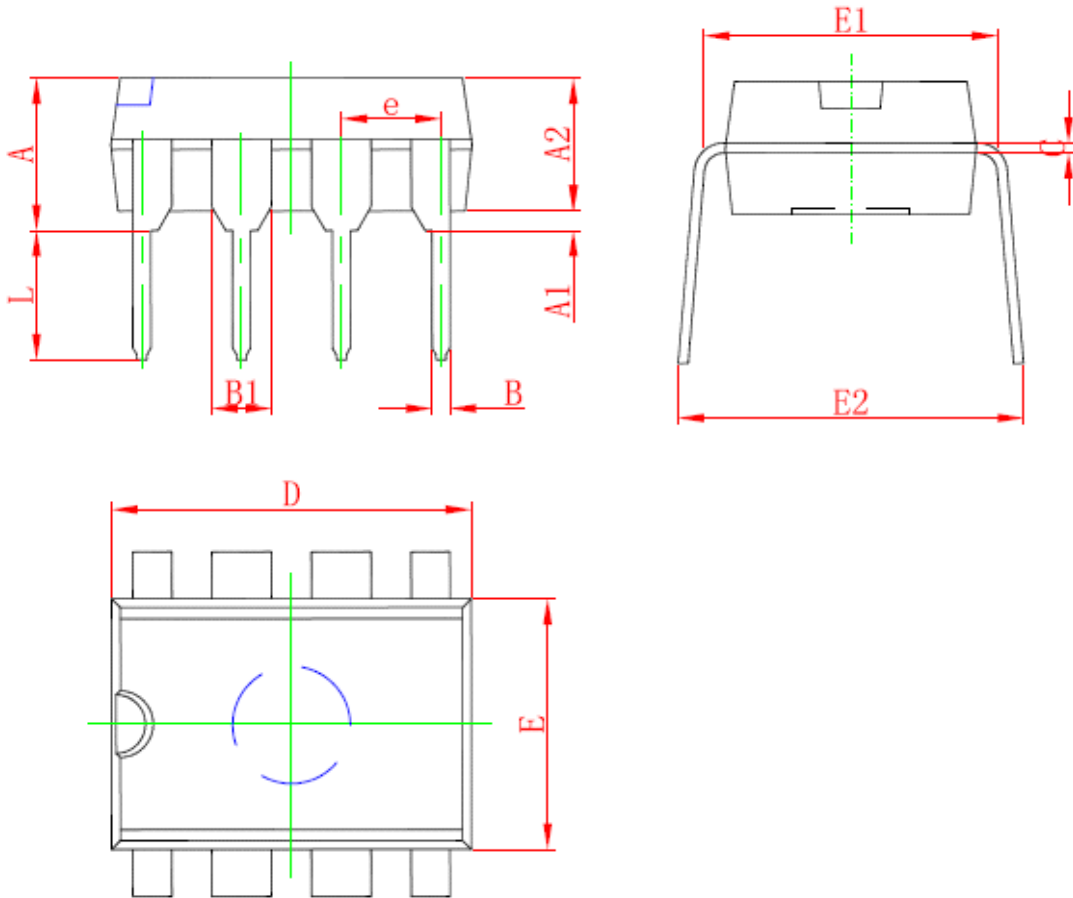
● **Gate Drive**

The PWM output is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET, on the another hand, too strong gate drive output will compromise EMI.

Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easy to be achieved with this dedicated control scheme. An internal 17V clamp is added for MOSFET gate protection at higher than expected VDD input.

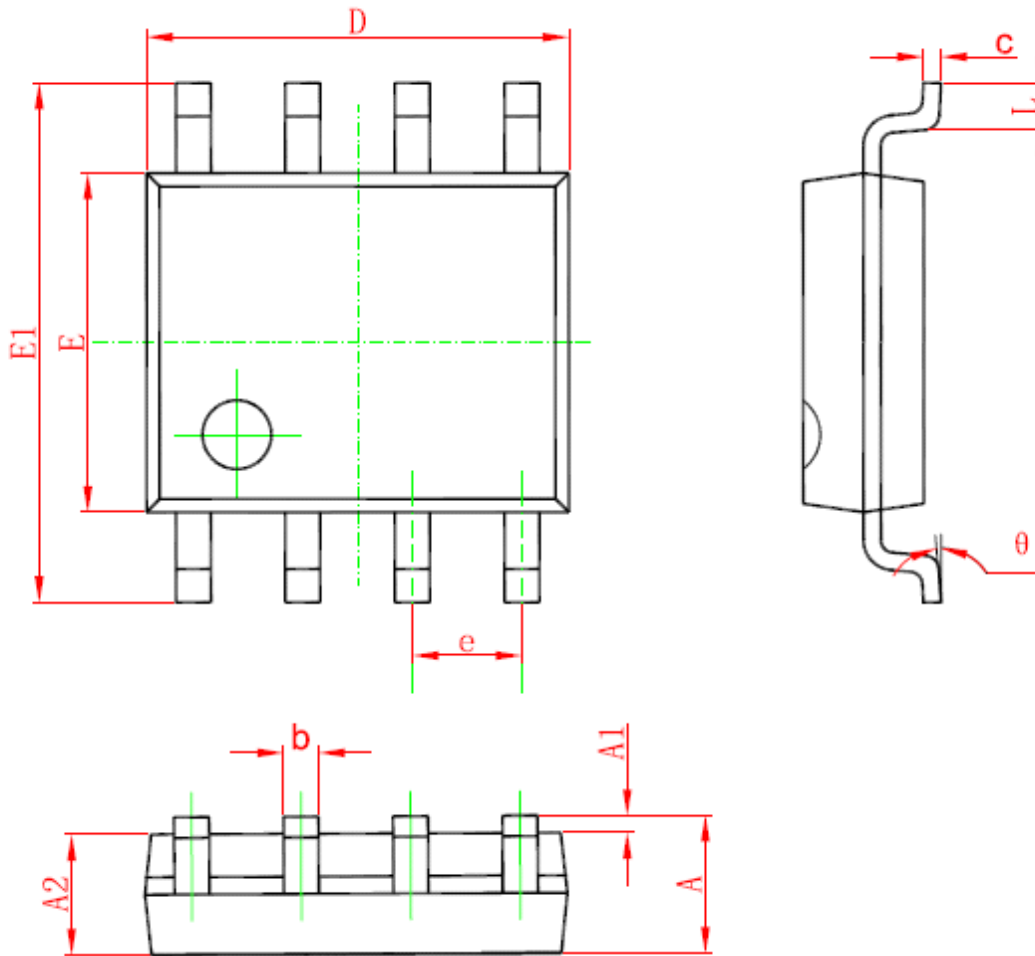
PACKAGE MECHANICAL DATA

8-Pin Plastic DIP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

8-Pin Plastic SOP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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