GENERAL DESCRIPTION

OB2362 is a high performance flyback adaptive multi-mode(CCM/QR) PWM controller, optimized to achieve high efficiency and low standby power with effective system cost.

At heavy load, the IC operates in fixed frequency(65kHz) CCM mode in the low line input voltage. At medium load, it operates in QR mode , at light load ,it operates in green mode with valley skip, and at no load the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VCC low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2362.

OB2362 offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), and VCC under voltage lockout (UVLO). It also provides the protections with latched shut down including over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 25KHz is minimized in the design and audio noise is eliminated during operation.

OB2362 is offered in SOT23-6 package.

APPLICATIONS

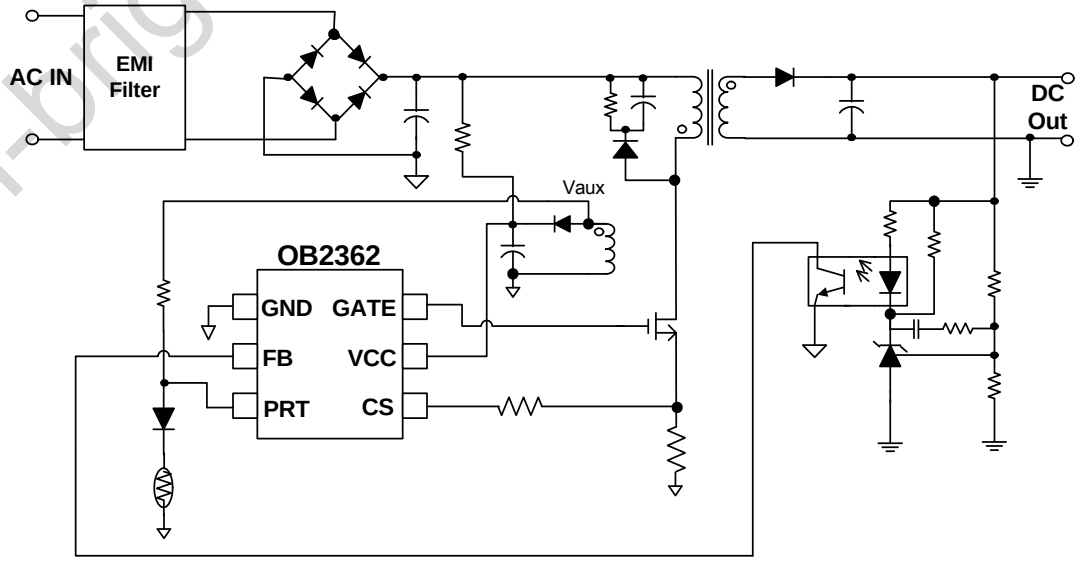
Offline AC/DC flyback converter for

- Power Adapter
- Set-Top Box Power Supplier
- Open-frame SMPS

FEATURES

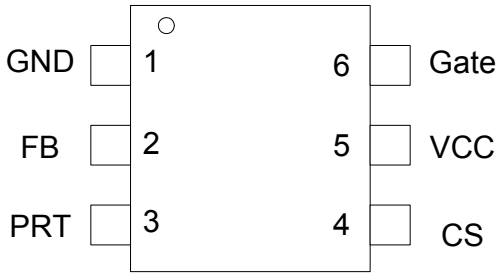
- Power on soft start reducing MOSFET Vds stress
- Multi-Mode Operation
  CCM @ Heavy Load and Low Line
  Quasi-Resonant operation @ Medium Load
  Green mode with valley skip @ Light Load
  Burst Mode @ No Load
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and low standby power design
- Audio noise free operation
- Comprehensive protection coverage
  - o VCC Under Voltage Lockout with hysteresis (UVLO)
  - o VCC Over Voltage Protection (VCC OVP)
  - o Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
  - o Over Load Protection (OLP) with auto-recovery
  - o External (if NTC resistor is connected at PRT pin)or internal Over Temperature Protection (OTP) with latched shut down
  - o Output Over Voltage Protection(Output OVP) with latched shut down, and the OVP triggered voltage can be adjusted by the resistor connected between auxiliary winding and PRT pin
  - o Output diode short protection with auto-recovery

TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration



Ordering Information

Part Number	Description
OB2362MP	SOT23-6, Pb-free in T&R

Package Dissipation Rating

Package	RθJA(℃/W)
SOT23-6	200

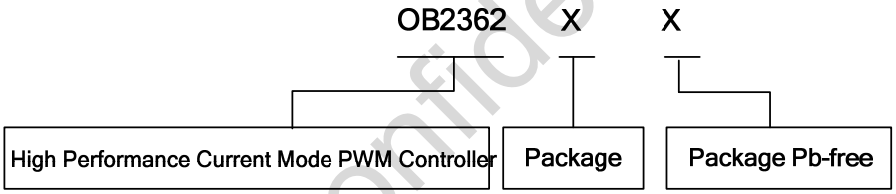
Recommended operating condition

Symbol	Parameter	Range
VCC	VCC Supply Voltage	12 to 26V

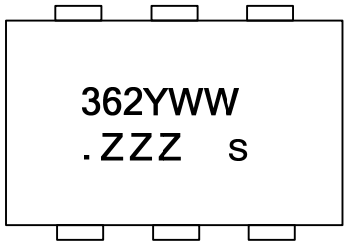
Absolute Maximum Ratings

Parameter	Value
VCC DC Supply Voltage	V_{OVP}-1V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Operating Ambient Temperature T_A	-40 to 85 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

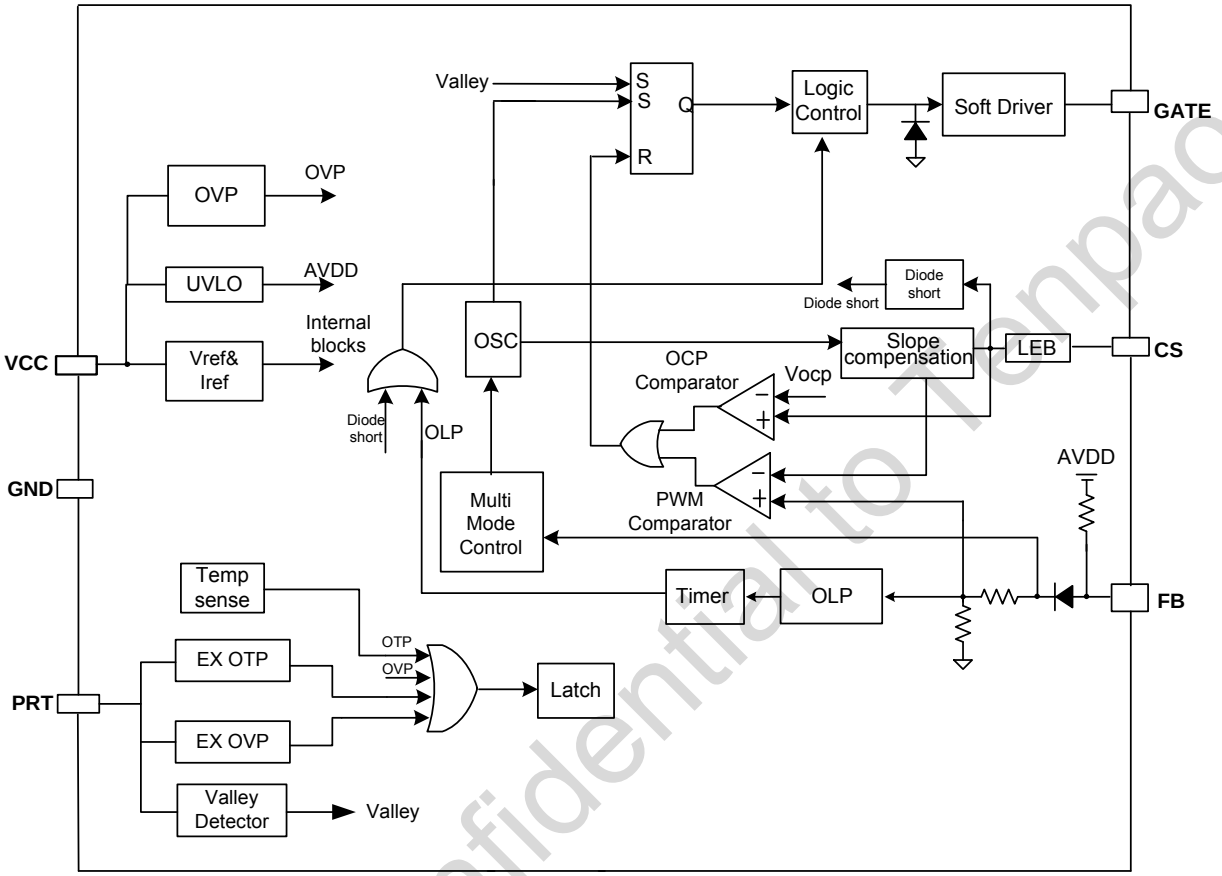


Y:Year Code
WW:Week Code(01-52)
S: Internal code
ZZZ: Lot code

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
VCC	P	Power Supply
CS	I	Current sense input
Gate	O	Totem-pole gate driver output for power MOSFET
GND	P	Ground
PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust OVP trigger voltage and detect transformer core demagnetization. If both OTP and OVP are needed, a diode should be connected between PRT pin and the NTC resistor.
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin CS.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(T_A = 25℃, VCC=18V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
Istartup	VCC Start up Current	VCC=UVLO(OFF)-1V, measure leakage current into VCC		2	10	uA
I_VCC_Operation	Operation Current	VDD=18V,CS=4V, FB=3.5V,measure I(VCC)		2.5	3	mA
I_VCC_Burst	Burst Current	CS=0V,FB=0.5V, measure I(VCC)		0.6	0.7	mA
UVLO(ON)	VCC Under Voltage Lockout Enter		6	7	8	V
UVLO(OFF)	VCC Under Voltage Lockout Exit (Recovery)		19	21	23	V
Vpull-up	Pull-up PMOS active			10		V
OVP	VCC Over Voltage Protection threshold voltage	FB=3V,CS=0V. Slowly ramp VCC, until no gate switching.	26	27	28	V
Vlatch_release	Latch release voltage			5		V
Feedback Input Section(FB Pin)						
V_{FB} Open	V_{FB} Open Loop Voltage			5.1		V
Avcs	PWM input gain ΔVFB/ΔVCS			3.5		V/V
Maximum duty cycle	Max duty cycle @ VCC=18V,VFB=3V,VCS=0V		75	78	81	%
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		0.3		mA
V_{TH}_OLP	Open loop protection, FB Threshold Voltage			4.4		V
Td_OLP	Open loop protection, Debounce Time			60		ms
Z_{FB}_IN	Input Impedance			16		KΩ
Current Sense Input(CS Pin)						
SST_CS	Soft start time for CS peak			4		ms
T_blanking	Leading edge blanking time			300		ns
Td_OC	Over Current Detection and Control Delay	From Over Current Occurs till the Gate driver output start to turn off		90		ns
V_{TH}_OC	Internal Current Limiting Threshold Voltage with zero duty cycle		0.43	0.45	0.47	V
V_{TH}_OC_Clamp	OCP CS voltage clamper			0.72		V
PRT pin						
IRT	Output current for external OTP detection		95	100	105	uA
VOTP	Threshold voltage for external OTP		0.95	1	1.05	V
Ioutput_ovp	Current threshold for adjustable output OVP			180		uA

Td_output_ovp	Output OVP debounce time			5		Cycles
In-chip OTP						
OTP enter				150		℃
OTP exit				120		℃
Oscillator						
F_{OSC}	Normal Oscillation Frequency	VDD=18V,FB=3V, CS=0V	60	65	70	KHz
∆f_OSC	Frequency jittering			+/-6		%
F_shuffling	Shuffling frequency			32		Hz
∆f_Temp	Frequency Temperature Stability			1		%
∆f_VCC	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			25		KHz
Gate driver						
VOL	Output low level @ VDD=18V, Io=5mA				1	V
VOH	Output high level @ VCC=18V, Io=20mA		6			V
V_clamping	Output clamp voltage			12		V
T_r	Output rising time 1.2V ~ 10.8V @ CL=1000pF			100		ns
T_f	Output falling time 10.8V ~ 1.2V @ CL=1000pF			30		ns

OPERATION DESCRIPTION

OB2362 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of OB2362 is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

- **Operating Current**

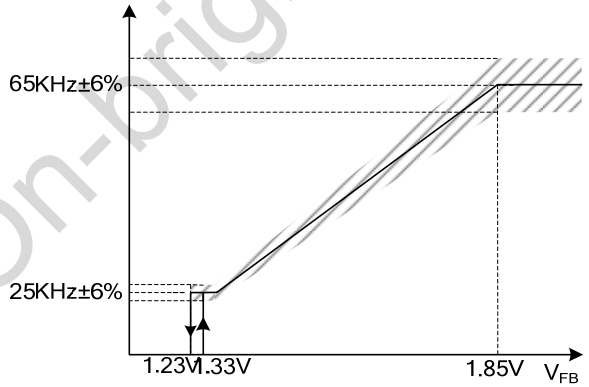
The Operating current of OB2362 is low at 2.5mA (typical). Good efficiency is achieved with OB2281 low operation current together with the 'extended burst mode' control features.

- **Soft Start**

OB2362 features an internal 2ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

- **Frequency shuffling for EMI improvement**

The frequency shuffling (switching frequency modulation) is implemented in OB2362. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.



- **Multi Mode Operation for High Efficiency**

OB2362 is a multi mode QR/CCM controller. The controller changes the mode of operation according to the FB pin voltage. At the normal operating condition, the IC operates in traditional PWM mode.

As the output load current is decreased , the IC enter into green mode smoothly from the PWM mode. In this mode , the switching frequency will start to linearly decrease from 65KHz to 25KHz, meanwhile the valley turn on can be realized by monitoring the voltage activity on auxiliary windings through the PRT pin. So the switching loss is minimized and the high conversion efficiency can be achieved.

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2362 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

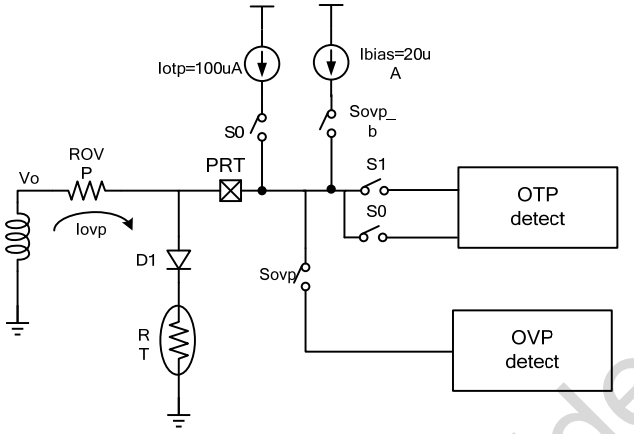
- **Internal Synchronized Slope Compensation**

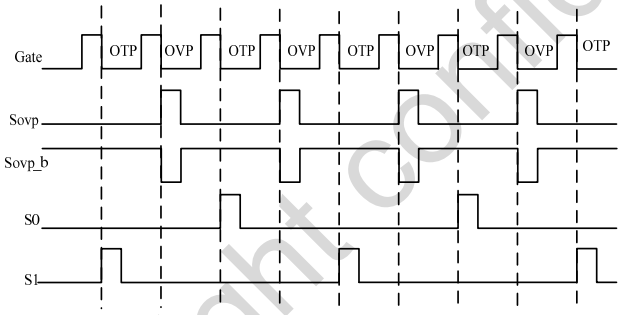
Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Driver**

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.
A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

- **Dual Function of External OTP and Output OVP**





On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the figure.

For external OTP detection, when switch control signal S1= “1”, about 20uA (typical) current flows out from PRT pin. When switch control signal S0= “1”,about 120uA (typical) current flows out from PRT pin. The PRT pin voltage difference △Votp at phase S0 and S1 phase is equal to

$$\Delta V_{OTP} = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 100uA \cdot$$

When △Votp<1V , external OTP latch protection is triggered after 30 Gate cycles debounce.

For output OVP detection, when Sovp= “1”, Iovp is equal to Vo/ROVP. If Iovp is larger than 180uA (typical), OVP latch protection is triggered after 5 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

- **Protection Controls**

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), and Under Voltage Lockout on VDD (UVLO), and latched shutdown features including Over Temperature Protection (OTP), VCC and output Over Voltage Protection (OVP).
With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

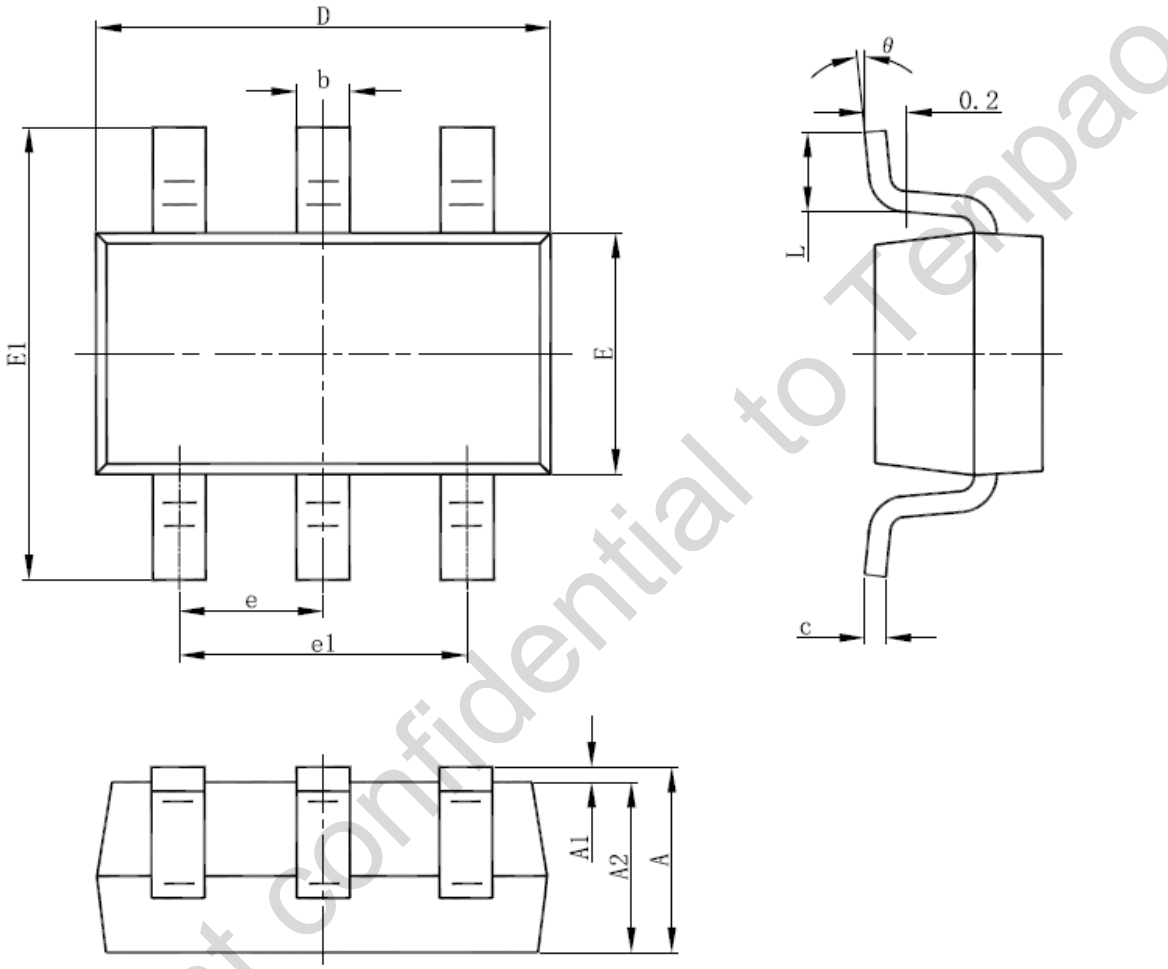
At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit. For protection with latched shut down mode, control circuit shuts down (latch) the power MOSFET when an over temperature condition or over voltage condition is detected until VDD drops below 5V (typical) (Latch release voltage), and the device enters power on restart-up sequence thereafter.

- **Pin Floating and Short Protection**

OB2362 provides PIN floating protection for all the pins and pin short protection for adjacent pins. In the cases when a pin is floating or two adjacent pins are shorted, Gate switching is disabled.

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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