

GENERAL DESCRIPTION

OB2362C is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

At full loading, the IC operates in fixed frequency (65KHz) mode. When the loading goes low, it operates in Green mode with valley switching for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

VCC low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2362C.

OB2362C offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VCC under voltage lockout (UVLO), over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 23KHz is minimized in the design and audio noise is eliminated during operation.

OB2362C is offered in SOT23-6 package.

APPLICATIONS

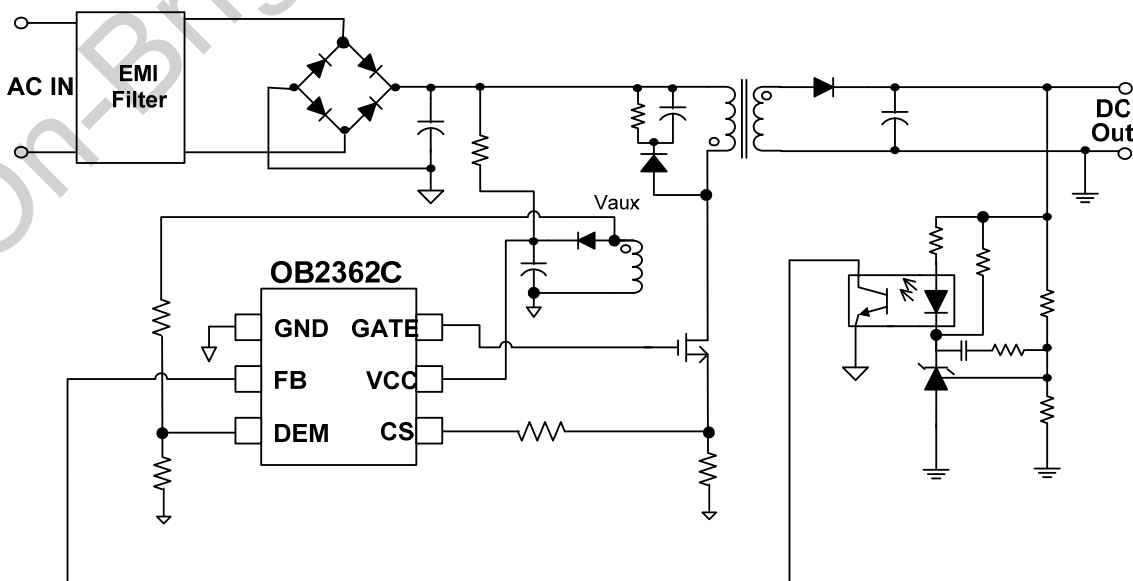
Offline AC/DC flyback converter for

- General power supply
- Power Adapter

FEATURES

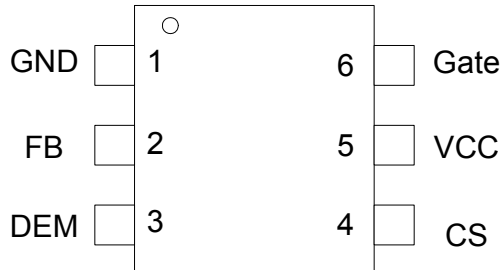
- Power on soft start reducing MOSFET Vds stress
- Multi-Mode Operation
 - 65KHz fixed frequency mode @ Full Load
 - Valley switching operation @ Green mode
 - Burst Mode @ Light Load & No Load
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and low standby power design
- Audio noise free operation
- Comprehensive protection coverage
 - VCC Under Voltage Lockout with hysteresis (UVLO)
 - VCC Over Voltage Protection (VCC OVP)
 - Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
 - Over Load Protection (OLP) with auto-recovery
 - Brownout protection with auto-recovery
 - Line Over Voltage Protection (Line OVP)
 - Output Over Voltage Protection (Output OVP) with auto-recovery, and the OVP triggered voltage can be adjusted by the resistors connected between auxiliary winding and ground
 - Output diode short protection with auto-recovery

TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration



Ordering Information

| Part Number | Description |
|-------------|-------------------------|
| OB2362CMP | SOT23-6, Pb-free in T&R |

Package Dissipation Rating

| Package | R θ JA(°C/W) |
|---------|---------------------|
| SOT23-6 | 200 |

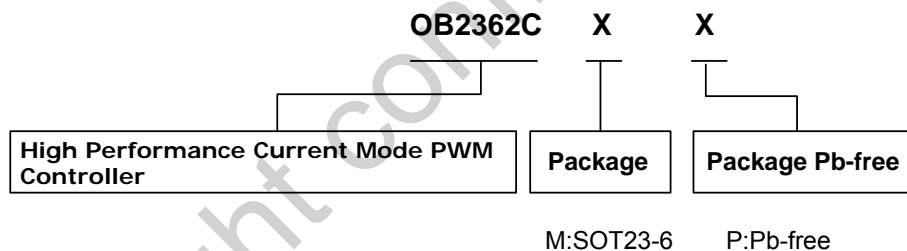
Recommended operating condition

| Symbol | Parameter | Range |
|--------|--------------------|-----------|
| VCC | VCC Supply Voltage | 12 to 26V |

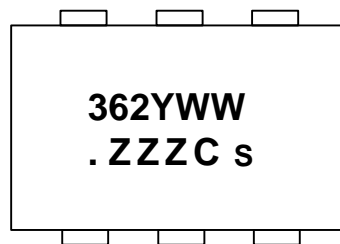
Absolute Maximum Ratings

| Parameter | Value |
|---|----------------------|
| VCC DC Supply Voltage | V _{OV} P-1V |
| FB Input Voltage | -0.3 to 7V |
| CS Input Voltage | -0.3 to 7V |
| DEM Input Voltage | -0.3 to 7V |
| Min/Max Operating Junction Temperature T _J | -40 to 150 °C |
| Operating Ambient Temperature T _A | -40 to 85 °C |
| Min/Max Storage Temperature T _{stg} | -55 to 150 °C |
| Lead Temperature (Soldering, 10secs) | 260 °C |

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

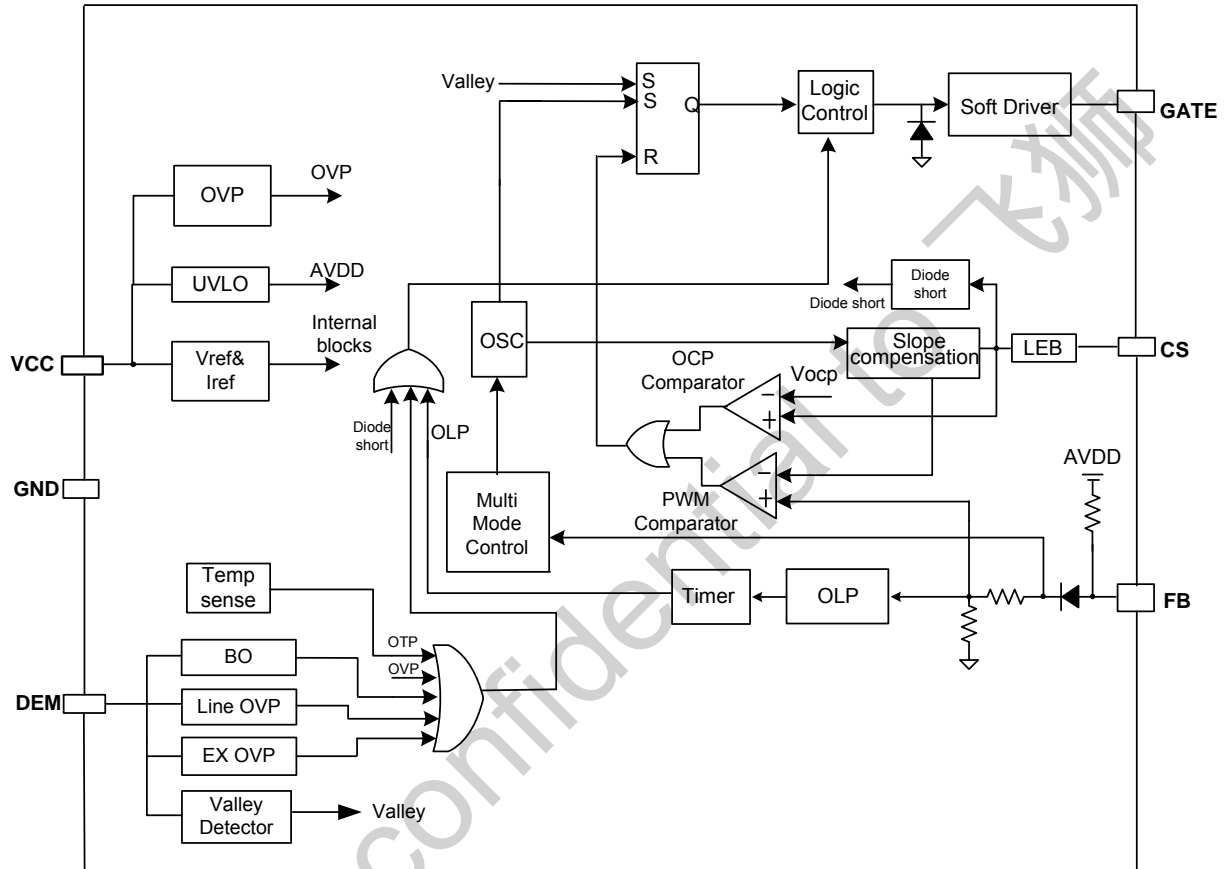


Y:Year Code
 WW:Week Code(01-52)
 ZZZ: Lot code
 C:Character Code
 S: Internal code

TERMINAL ASSIGNMENTS

| Pin Name | I/O | Description |
|----------|-----|---|
| VCC | P | Power Supply |
| CS | I | Current sense input |
| Gate | O | Totem-pole gate driver output for power MOSFET |
| GND | P | Ground |
| DEM | I | Multiple functions pin. Connecting two resistors from Vaux to ground can adjust output OVP trigger voltage, Brown-in/Brown-out trigger voltage, Line OVP trigger voltage and detect transformer core demagnetization. |
| FB | I | Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin CS. |

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

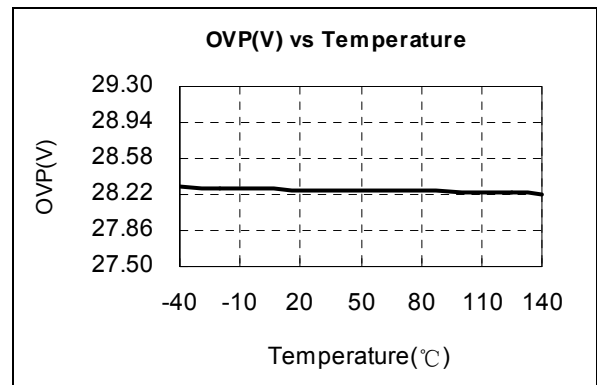
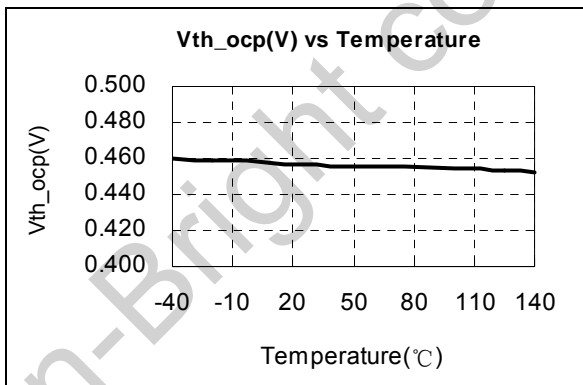
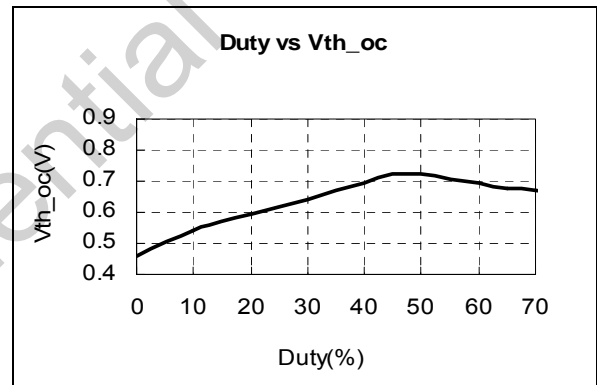
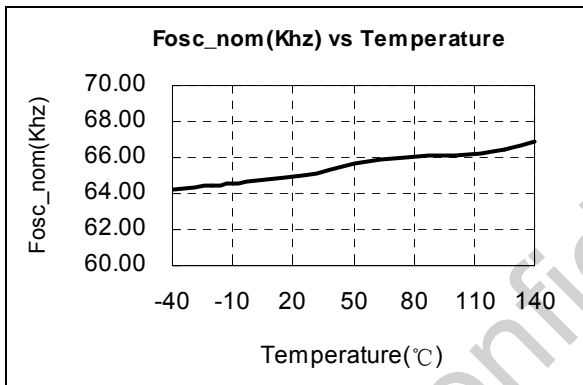
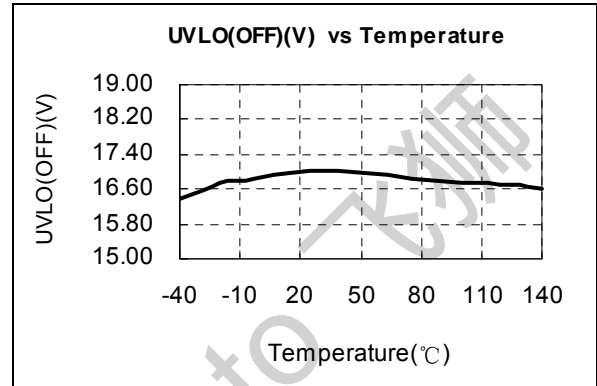
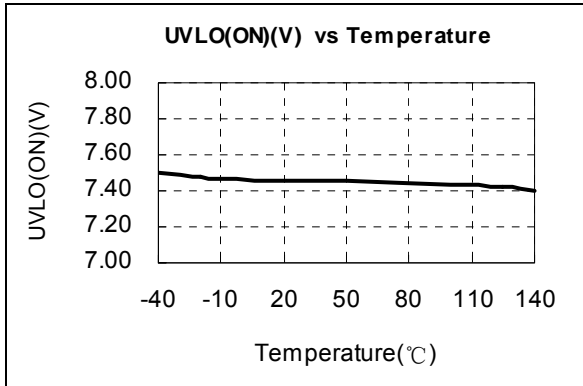
 (T_A = 25°C, VCC=18V, unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---------------------------------------|--|--|------|------|------|------------|
| Supply Voltage (VDD) | | | | | | |
| I _{startup} | VCC Start up Current | VCC=UVLO(OFF)-1V, measure leakage current into VCC | | 2 | 5 | uA |
| I _{VCC_Operation} | Operation Current | VDD=18V,CS=4V, FB=3.5V,measure I(VCC) | | 2.6 | 3.1 | mA |
| I _{VCC_Burst} | Burst Current | CS=0V,FB=0.5V, measure I(VCC) | | 0.6 | 0.7 | mA |
| UVLO(ON) | VCC Under Voltage Lockout Enter | | 6.8 | 7.3 | 7.8 | V |
| UVLO(OFF) | VCC Under Voltage Lockout Exit (Recovery) | | 16 | 17 | 18 | V |
| V _{pull-up} | Pull-up PMOS active | | | 10 | | V |
| OVP | VCC Over Voltage Protection threshold voltage | FB=3V,CS=0V. Slowly ramp VCC, until no gate switching. | 26.5 | 28 | 29.5 | V |
| Feedback Input Section(FB Pin) | | | | | | |
| V _{FB_Open} | V _{FB} Open Loop Voltage | | | 5.1 | | V |
| A _{vcs} | PWM input gain $\Delta V_{FB}/\Delta V_{CS}$ | | | 3.5 | | V/V |
| Maximum duty cycle | Max duty cycle @ VCC=18V,VFB=3V,VCS=0V | | 77 | 80 | 83 | % |
| V _{ref_green} | The threshold enter green mode | | | 2.1 | | V |
| V _{ref_burst_H} | The threshold exits burst mode | | | 1.33 | | V |
| V _{ref_burst_L} | The threshold enters burst mode | | | 1.23 | | V |
| I _{FB_Short} | FB pin short circuit current | Short FB pin to GND and measure current | | 0.21 | | mA |
| V _{TH_OLP} | Open loop protection, FB Threshold Voltage | | | 4.4 | | V |
| T _{d_OLP} | Open loop protection, Debounce Time | | | 60 | | ms |
| Z _{FB_IN} | Input Impedance | | | 30 | | K Ω |
| Current Sense Input(CS Pin) | | | | | | |
| SST_CS | Soft start time for CS peak | | | 2.5 | | ms |
| T _{blanking} | Leading edge blanking time | | | 300 | | ns |
| T _{d_OC} | Over Current Detection and Control Delay | From Over Current Occurs till the Gate driver output start to turn off | | 90 | | ns |
| V _{TH_OC} | Internal Current Limiting Threshold Voltage with zero duty cycle | | 0.43 | 0.45 | 0.47 | V |
| V _{TH_OC_Clamp} | OCP CS voltage clamper | | | 0.72 | | V |
| DEM pin | | | | | | |
| I _{brown-in} | Brown-in threshold current | | | 110 | | uA |
| I _{brown-out} | Brown-out threshold current | | 95 | 100 | 105 | uA |

| | | | | | | |
|------------------------|---|----------------------|------|------|------|--------|
| Td_BO | Brown-out protection debounce Time | | 25 | 29 | 33 | ms |
| I_lineovp | Line OVP threshold current | | 405 | 440 | 475 | uA |
| Td_lineovp | Line OVP debounce time | | | 120 | | ms |
| Voutput_ovp | Voltage threshold for adjustable output OVP | | 2.85 | 3 | 3.15 | V |
| Td_output_ovp | Output OVP debounce time | | | 6 | | Cycles |
| In-chip OTP | | | | | | |
| OTP enter | | | | 150 | | °C |
| OTP exit | | | | 120 | | °C |
| Oscillator | | | | | | |
| F _{osc} | Normal Oscillation Frequency | VDD=18V,FB=3V, CS=0V | 60 | 65 | 70 | KHz |
| Δf _{OSC} | Frequency jittering | | | +/-6 | | % |
| F _{shuffling} | Shuffling frequency | | | 32 | | Hz |
| Δf _{Temp} | Frequency Temperature Stability | | | 1 | | % |
| Δf _{VCC} | Frequency Voltage Stability | | | 1 | | % |
| F _{Burst} | Burst Mode Switch Frequency | | | 23 | | KHz |
| Gate driver | | | | | | |
| VOL | Output low level @ VDD=18V, I _o =5mA | | | | 1 | V |
| VOH | Output high level @ VCC=18V, I _o =20mA | | 6 | | | V |
| V _{clamping} | Output clamp voltage | | | 11 | | V |
| T _r | Output rising time 1.2V ~ 10.8V @ CL=1000pF | | | 100 | | ns |
| T _f | Output falling time 10.8V ~ 1.2V @ CL=1000pF | | | 30 | | ns |

CHARACTERIZATION PLOTS

VDD = 18V, TA = 25°C condition applies if not otherwise noted.



OPERATION DESCRIPTION

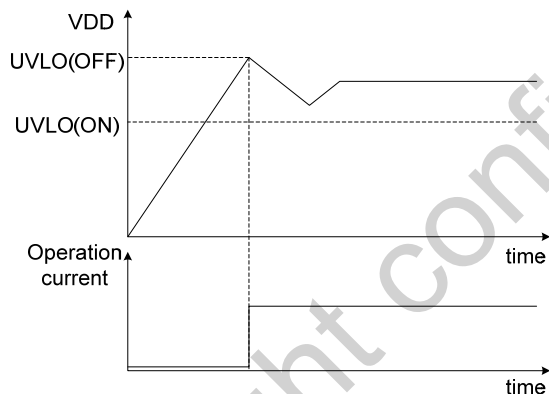
OB2362C is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of OB2362C is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of OB2362C is low at 2.5mA (typical). Good efficiency is achieved with OB2362C low operation current together with the 'extended burst mode' control features.

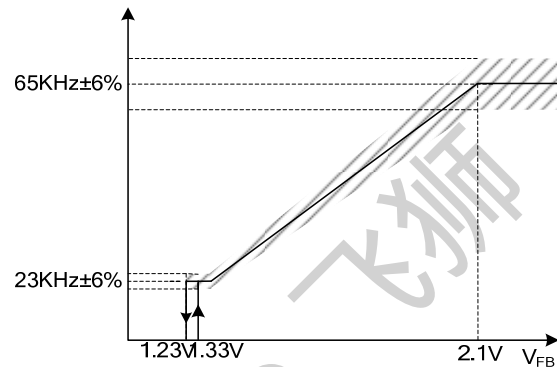


Soft Start

OB2362C features an internal 2.5ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in OB2362C. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.



Multi Mode Operation for High Efficiency

OB2362C is a multi mode controller. The controller changes the mode of operation according to the FB pin voltage. At the normal operating condition, the IC operates in traditional fix frequency (65KHz) PWM mode.

As the output load current is decreased, the IC enter into green mode smoothly from the PWM mode. In this mode, the switching frequency will start to linearly decrease from 65KHz to 23KHz, meanwhile the valley turn on can be realized by monitoring the voltage activity on auxiliary windings through the DEM pin. So the switching loss is minimized and the high conversion efficiency can be achieved.

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

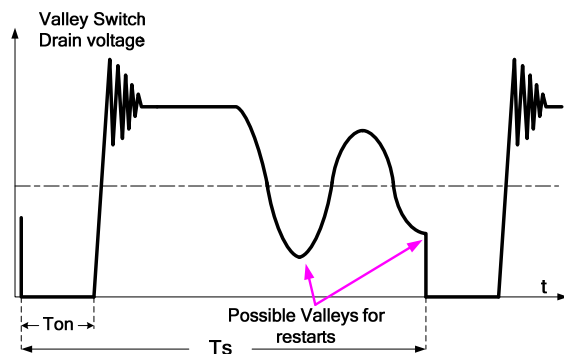
The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below V_{ref_burst_L} (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to V_{ref_burst_H} (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off

and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_p C_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.

The typical detection level is fixed at -50mV at the DEM pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at DEM is below -50mV in falling edge.



Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2362C current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

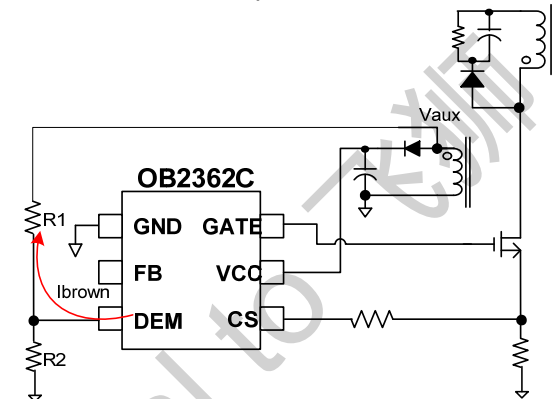
Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Multiple Functions of Brown-in/Brown-out, Line OVP in/Line OVP out and Output OVP

When the power MOSFET is turn on, the voltage on auxiliary windings is negative which make our Brown-in/Brown-out protection feasible.



$$I_{AUX} = \frac{0.1}{R2} + \frac{0.1 - V_{AUX}}{R1}$$

R1: The resistor connected from DEM to AUX.

R2: The resistor connected from DEM to ground.

When system starts up, if $I_{AUX} < I_{brown_in}$, Brown-in auto-recovery protection is triggered after 2 Gate cycles debounce. When the system enters the normal operation mode, if $I_{AUX} < I_{brown_out}$, Brown-out auto-recovery protection is triggered after 29ms debounce.

When the system enters the normal operation mode, if $I_{AUX} > I_{Line_OVP}$, Line OVP auto-recovery protection is triggered after 120ms debounce.

For output OVP detection, when Gate is off, V_{DEM} is equal to $V_{AUX} * R2 / (R1 + R2)$. If V_{DEM} is larger than 3V (typical), OVP auto-recovery protection is triggered after 6 Gate cycles debounce. By selecting proper R1 and R2 resistance, output OVP level can be programmed.

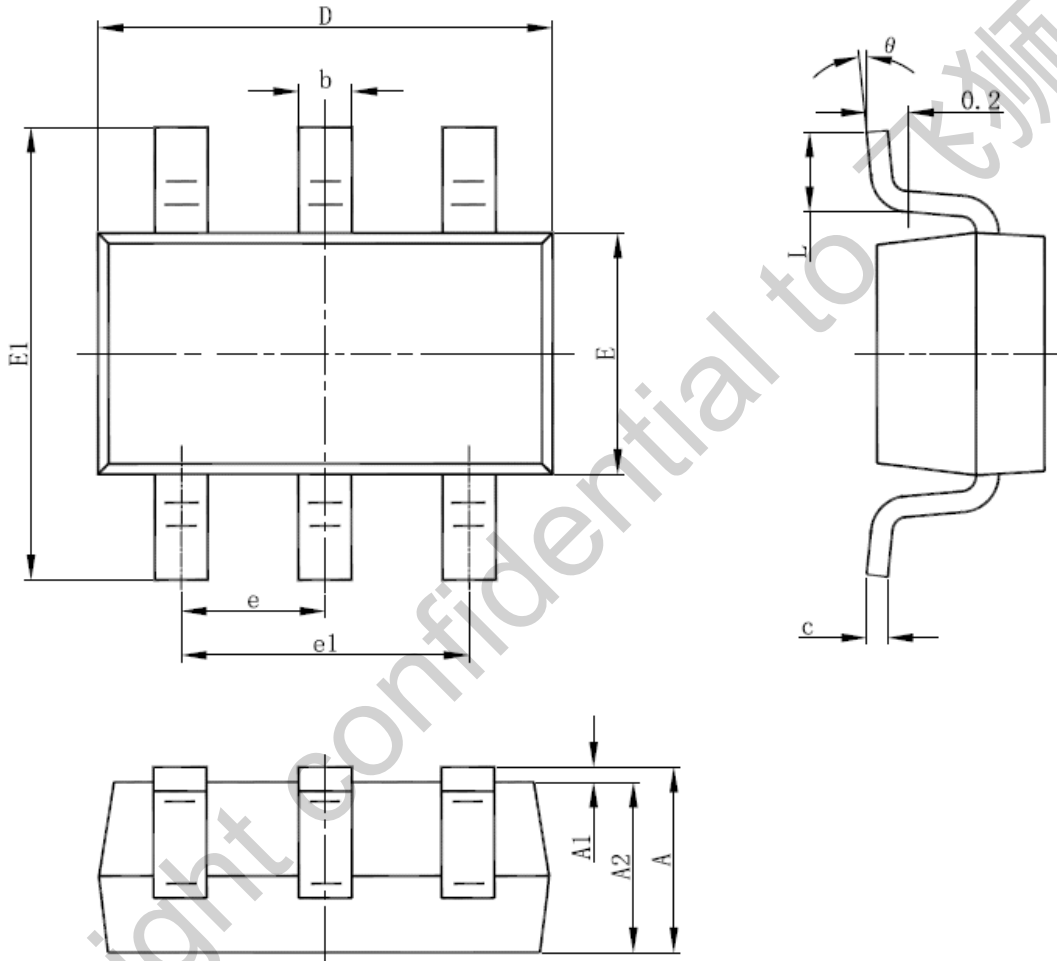
$$V_{AUX} = \frac{3 * (R1 + R2)}{R2}$$

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), Brownout Protection, VCC and output Over Voltage Protection (OVP).

With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP , control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

PACKAGE MECHANICAL DATA
SOT-23-6L PACKAGE OUTLINE DIMENSIONS


| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 1.000 | 1.450 | 0.039 | 0.057 |
| A1 | 0.000 | 0.150 | 0.000 | 0.006 |
| A2 | 0.900 | 1.300 | 0.035 | 0.051 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.080 | 0.220 | 0.003 | 0.009 |
| D | 2.800 | 3.020 | 0.110 | 0.119 |
| E | 1.500 | 1.726 | 0.059 | 0.068 |
| E1 | 2.600 | 3.000 | 0.102 | 0.118 |
| e | 0.950 (BSC) | | 0.037 (BSC) | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |

IMPORTANT NOTICE

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