

#### GENERAL DESCRIPTION

OB2633 is a highly integrated Quasi-Resonant(QR) controller with adaptive multi-mode regulation, optimized for high performance, low EMI, low standby power consumption and wide output voltage range Quick Charger(QC) solutions, together with secondary -side controllers, such as OB200x and OB2603x supporting Qualcomm Quick Charge QC3.0 protocol. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range.

At normal load condition, it operates in QR mode in high line input voltage. To minimize switching loss, the maximum switching frequency in QR mode is internally limited to 75 KHz. When the loading goes low, it operates in PFM mode with valley switching for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. Additionally, in the low line input voltage, the IC operates in fixed frequency (55KHz) CCM mode at the heavy loading. As a result, high conversion efficiency can be achieved in the whole loading range.

OB2633 offers complete protection including cycle-by-cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), output short protection (SCP), output under voltage protection (UVP), output and VDD over voltage protection. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 22KHz is minimized to avoid audio noise during operation.

OB2633 is offered in SOT23-6 package.

#### **FEATURES**

- Very wide range of supply voltage
- Multi-Mode Operation

75KHz maximum clamping frequency in QR mode @ Full Load in high line voltage

55KHz minimum clamping frequency in CCM mode @ Heavy Load in low line voltage

Valley switching operation @ Green mode Burst Mode @ Light Load & No Load

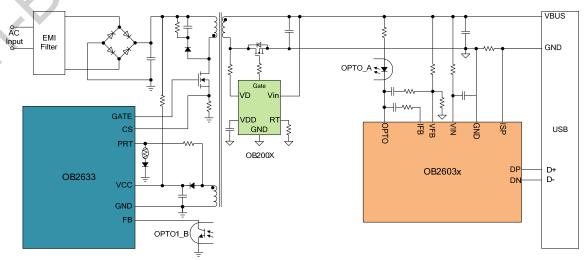
- Power on soft start reducing MOSFET Vds stress
- Extended burst mode control for improved efficiency and low standby power
- Soft Start for elimination output over shoot
- Adaptive loop gain compensation with lovp current detection
- Adaptive Frequency shuffling for EMI
- Low operating current at no/light load
- Audio noise free operation
- Comprehensive auto-recovery protection
  - VDD under voltage lockout with hysteresis (UVLO)
  - Cycle-by-cycle over current protection (OCP)
  - Overload protection (OLP)
  - Over temperature protection (OTP)
  - o VDD over voltage protection
  - Output over voltage protection
  - Output short protection (SCP)
  - Output under voltage protection (UVP)
  - Output diode short protection

#### **APPLICATIONS**

Offline AC/DC flyback converter for

- Quick-charging AC/DC charges
- AC/DC Adapters with wide output range

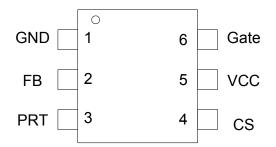
## TYPICAL APPLICATION





### **GENERAL INFORMATION**

## **Pin Configuration**



**Ordering Information** 

Part Number	Description
OB2633MP	SOT23-6, Halogen-free in T&R

**Package Dissipation Rating** 

	3
Package	RθJA(℃/W)
SOT23-6	200

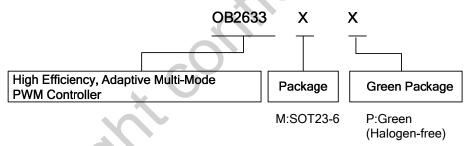
**Recommended operating condition** 

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Symbol	Parameter	Range		
VCC	VCC Supply Voltage	12 to 48V		

**Absolute Maximum Ratings** 

Absolute Maximum Ratings					
Parameter	Value				
VCC DC Supply Voltage	54V				
FB Input Voltage	-0.3 to 7V				
CS Input Voltage	-0.3 to 7V				
PRT Input Voltage	-0.3 to 7V				
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃				
Operating Ambient Temperature T <sub>A</sub>	-20 to 85 ℃				
Min/Max Storage Temperature Tstg	-55 to 150 ℃				
Lead Temperature (Soldering, 10secs)	260 ℃				

**Note:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



## **Marking Information**



Y:Year Code

WW:Week Code(01-52)

ZZZ: Lot code A:Character Code S: Internal code

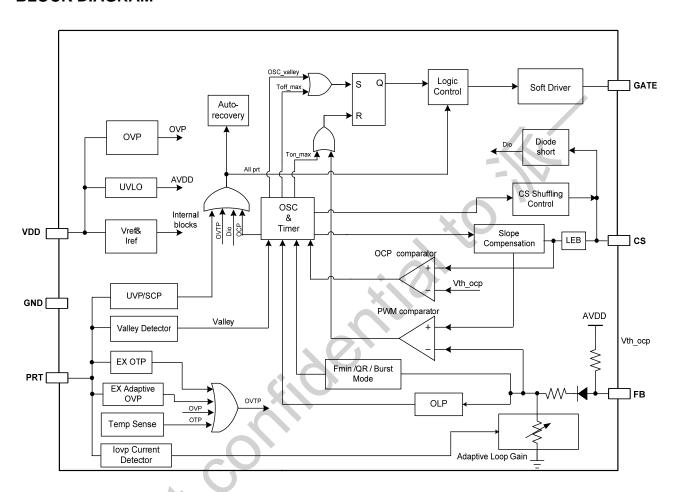


## **TERMINAL ASSIGNMENTS**

Pin Num.	Pin Name	1/0	Description
1	GND	Р	Ground
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin CS.
3	PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust IOVP, ISCP, IUVP trigger current and detect transformer core demagnetization. If all protections are needed, a diode should be connected between PRT pin and the NTC resistor.
4	CS	1	Current sense input
5	VCC	Р	Power Supply
6	Gate	0	Totem-pole gate driver output for power MOSFET



## **BLOCK DIAGRAM**





## **ELECTRICAL CHARACTERISTICS**

 $(T_A = 25^{\circ}C, VDD=18V, unless otherwise noted)$ 

Startup   VDD Start up Current   VDD=UVLO(OFF)	Symbol	Parameter	Test Conditions	Min	Тур.	Max	Unit
VDD Start up Current   11,	Supply Voltage (VDD					•	
VDD Burst   Burst Operation Current   VFB=0.5V, CL=1nF   0.4   0.5   mA	Istartup		1V, measure leakage current into VDD		5	20	uA
JVLO(OFF)   VDD Under Voltage Lockout Exit (Recovery)   15.5   16.5   17.5   V     JVLO(ON)   VDD Under Voltage Lockout Enter   7.2   V     JVLO(ON)   VDD Under Voltage Lockout Enter   7.2   V     JVLO(ON)   VDD Under Voltage Lockout Enter   7.2   V     JVLO(ON)   VDD Under Voltage   10   V     JVLO(ON)   VDD Under Voltage   10   V     JVLO(ON)   VDD Under Voltage   10   V     JVLO(ON)   VDP Over vol	I_VDD_Operation	Normal Operation Current			2.8	3.2	mA
Sylve   Syl	I_VDD_Burst	Burst Operation Current	$V_{FB}$ =0.5V, CL=1nF		0.4	0.5	mA
Filter	UVLO(OFF)	Exit (Recovery)		15.5	16.5	17.5	V
OVP   Over voltage protection voltage   Potential gate clock is off   S2.5   V	UVLO(ON)		*		7.2		V
OVP   Over Voltage protection voltage protection voltage protection (gate clock is off pate clock i	Vpull-up	Pull-up PMOS active			10		V
VFB Open     VFB Open Loop Voltage     5.1     V       AVCS     PWM input gain ΔVFB/ΔVCS     lovp>96uA with Hysteresis lovp<90uA with Hysteresis	VOVP		Ramp up VDD until		52.5		V
Avcs  PWM input gain ΔVFB/ΔVCS  PWM input gain ΔVFB/ΔVCS  Fon_max  Max Ton time @ VDD=18V,VFB=3V,VCS=0.3V  Avef_green  The threshold enter green mode  The threshold enter burst mode  The threshold enter burst mode  The threshold enter burst mode  FB_Short  FB pin short circuit current  Short FB pin to GND and measure current  FB_DIN  Input Impedance  The open loop FB Threshold voltage  The open loop protection debounce Time  Current Sense Input(CS Pin)  SST_CS  Soft start time of CS threshold  Control Delay  To_OC  Cover Current Detection and Control Delay  The open loop and measure current  From Over Current Occurrent  Cover Current Detection and Control Delay  The open loop on the poon on time on time threshold on time current  Internal current limiting @ Zero switching on time current internal current limiting on time current internal current limiting on time current internal current limiting on time intern	Feedback Input Sect	ion(FB Pin)					
Avcs  PWM input gain ΔVFB/ΔVCS    PWM input gain ΔVFB/ΔVCS   Hysteresis   S.5   V/V     Fon_max	V <sub>FB</sub> Open	V <sub>FB</sub> Open Loop Voltage			5.1		V
Hysteresis   Hy	Δνισε	PW/M input gain AV/FR/AV/CS	Hysteresis		3.5		V/V
VDD=18V,VFB=3V,VCS=0.3V   12   US     Vref_green	AVCS	CO			4.5		V/V
Vref_burst_H       The threshold exit burst mode       1.25       V         Vref_burst_L       The threshold enter burst mode       1.15       V         FB_Short       FB pin short circuit current       Short FB pin to GND and measure current       210       uA         ZFB_IN       Input Impedance       25       KΩ         VTH_Openloop       The open loop FB Threshold Voltage       4.5       V         TD_Openloop       The open loop protection debounce Time       40       ms         Current Sense Input(CS Pin)       SST_CS       Soft start time of CS threshold       4       ms         T_blanking       Leading edge blanking time       250       ns         TD_OC       Over Current Detection and Control Delay       Occurs till the gate driver output starts to turn off       90       ns         Vh_OCP_min       Internal current limiting threshold       May switching on time       0.55       V	Ton_max	VDD=18V,VFB=3V,VCS=0.3V			12		us
Vref_burst_L     The threshold enter burst mode     1.15     V       FB_Short     FB pin short circuit current     Short FB pin to GND and measure current     210     uA       ZFB_IN     Input Impedance     25     KΩ       VTH_Openloop     The open loop FB Threshold Voltage     4.5     V       TD_Openloop     The open loop protection debounce Time     40     ms       Current Sense Input(CS Pin)     SST_CS     Soft start time of CS threshold     4     ms       TD_OC     Over Current Detection and Control Delay     From Over Current Occurs till the gate driver output starts to turn off     90     ns       Vth_OCP_min     Internal current limiting threshold     ② Zero switching on time     0.55     V	VIET NIEEN				2.2		V
Mode   Short FB pin to GND and measure current   Short FB pin to GND	Vref_burst_H	The threshold exit burst mode			1.25		V
FB_Short  FB pin short circuit current  Cyreal IN  Input Impedance  The open loop FB Threshold Voltage  To_Openloop  The open loop protection debounce Time  Current Sense Input(CS Pin)  SST_CS  Soft start time of CS threshold  To_OC  Cover Current Detection and Control Delay  Control Delay  ST_DCP_min  Internal current limiting of threshold	Vref_burst_L				1.15		V
The open loop FB Threshold Voltage  The open loop protection debounce Time  The open l	I <sub>FB</sub> _Short FB pin short circuit current		GND and measure		210		uA
The open loop FB Threshold Voltage  The open loop protection debounce Time  The open l	Z <sub>FB</sub> _IN	Input Impedance			25		ΚΩ
The open loop protection debounce Time  The open loop protection debounce Time  Touriert Sense Input(CS Pin)  SST_CS  Soft start time of CS threshold  T_blanking  Leading edge blanking time  Touriert  Over Current Detection and Control Delay  Touriert  Touriert  Occurs till the gate driver output starts to turn off  The open loop protection and protection and control Delay  Touriert  Touriert  Touriert  Internal current limiting on time  Touriert  Tour	V <sub>TH</sub> _Openloop	The open loop FB Threshold			4.5		٧
SST_CS Soft start time of CS threshold Leading edge blanking time  T_blanking  Cover Current Detection and Control Delay  Cont	T <sub>D</sub> _ Openloop				40		ms
T_blanking  Leading edge blanking time  Over Current Detection and Control Delay  To_OC  To_OC  Over Current Detection and Control Delay  From Over Current Occurs till the gate driver output starts to turn off  Over Current limiting on time  Over Current Occurs till the gate driver output starts to turn off  Over Current limiting on time  Over Current Occurs till the gate driver output starts to turn off  Over Current limiting on time  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off  Over Current Occurs till the gate driver output starts to turn off	Current Sense Input(CS Pin)						
T_blanking  Leading edge blanking time  Over Current Detection and Control Delay  To_OC  To_OC  Over Current Detection and Control Delay  To_OC Delay  To_OC  Over Current Detection and Coccurs till the gate driver output starts to turn off  Over Current Detection and Over Current Delay  To_OC Delay  To_	SST_CS Soft start time of CS threshold  T_blanking Leading edge blanking time  Over Current Detection and Control Delay  Vtb_OCP_min Internal current limiting				4		ms
Over Current Detection and Control Delay  Occurs till the gate driver output starts to turn off  Oth_OCP_min  Internal current limiting on time  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off  Occurs till the gate driver output starts to turn off					250		ns
Vth_OCP_min			Occurs till the gate driver output starts				
Internal current limiting @ May switching			@ Zero switching		0.55		V
threshold on time 0.83	Vth_OCP_max	@ Max. switching		0.83		V	
<b>Dscillator</b>	Oscillator						

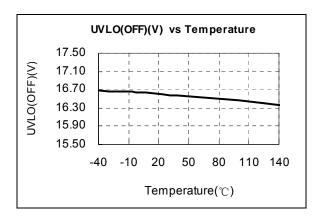


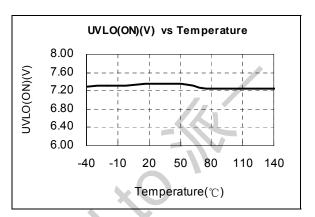
	T	1				
Fosc_max_QR	Average max clamp oscillation frequency in QR mode	VDD=15V, FB=3V,		75		KHz
Δf_OSC_QR	Frequency jittering of average clamp fmax_QR			±11		%
Fosc_min_CCM	Min clamp oscillation frequency in CCM mode	VDD=15V,FB=3V,		55		KHz
Δf_OSC_CCM	Frequency jittering of clamp fmin_CCM			±6.5		%
F_shuffling_CCM	Shuffling frequency clamp fmin_CCM			60		Hz
Δf_Temp	Frequency Temperature Stability			1		%
$\Delta f_VDD$	Frequency Voltage Stability			1		%
F Burst	Burst Mode Switch Frequency	X		22		KHz
Gate driver	, ,		,	L		
VOL	Output low level @ VDD=15V, Io=20mA	. 0			1	V
VOH	Output high level @ VDD=18V, lo=20mA		8			V
V_clamping	Output clamp voltage			11.5		V
T_r	Output rising time 1.2V ~ 10.8V @ CL=1000pF			140		ns
T_f	Output falling time 10.8V ~ 1.2V @ CL=1000pF			55		ns
PRT pin						
Ibias	Output bias current expect during OVP detection			30		uA
IRT	Output current for external OTP detection		114	120	126	uA
VOTP	Threshold voltage for external OTP		1.14	1.2	1.26	V
Td_ex_OTP	EX OTP debounce time			60		Cycles
loutput_ovp	Current threshold for	When T_start<30ms		90		uA
	adjustable output OVP	When T_start>30ms		216		uA
Td_output_ovp	Output OVP debounce time			8		Cycles
Iscp	SCP threshold			24		uA
Td_scp	SCP detect after startup			7.5		ms
luvp	UVP threshold			40		uA
Td_uvp	UVP detect after startup			15	L	ms
On Chip OTP					_	_
OTP Level				155		$^{\circ}$
OTP exit				125		$^{\circ}$ C
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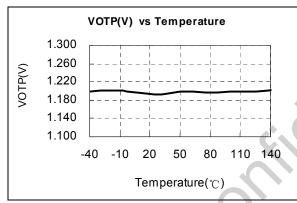


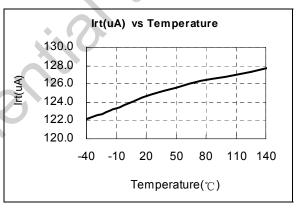
### **CHARACTERIZATION PLOTS**

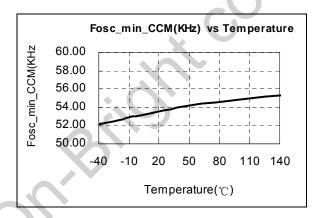
VDD = 18V, TA =  $25^{\circ}$ C condition applies if not otherwise noted.

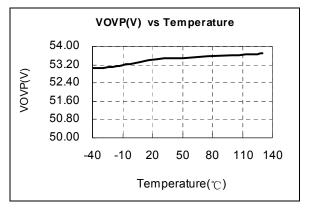


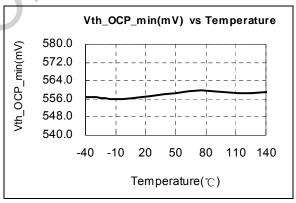


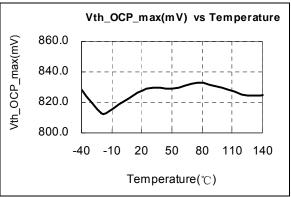




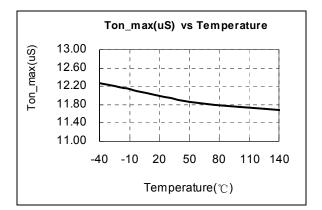














#### OPERATION DESCRIPTION

Quasi-Resonant (QR) converter typically features lower EMI and higher power conversion efficiency conventional compared to hard-switched converter with a fixed switching frequency. OB2633 is highly integrated Quasiа Resonant(QR) controller with adaptive multi-mode regulation, optimized for high performance wide output voltage range Quick Charger(QC) solutions, together with secondary-side controllers, such as OB200x and OB2603x supporting Qualcomm Quick Charge QC3.0 protocol. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

#### **Startup Current and Start up Control**

Startup current of OB2633 is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

## **Operating Current**

The Operating current of OB2633 is low at 2.8mA (typical). Good efficiency is achieved with OB2633 low operation current together with the 'extended burst mode' control features.

#### **Soft Start**

OB2633 features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0 V to the maximum level. Every restart up is followed by a soft start.

## **Adaptive Loop Gain Compensation**

With On-Bright proprietary technology, an adative loop compensation is implemented to ensure the system loop stability for wide output voltage range according to lovp current detection.

# Adaptive Frequency shuffling for EMI improvement

In OB2633, Adaptive frequency shuffling (switching frequency modulation) is implemented over the universal input voltage and load range. when the fixed frequency CCM mode is reached, the triangular frequency shuffling will be automatically added to the system to improve the EMI performance. The magnitude of shuffling lies in the range of  $\pm 6.5\%$ . When the system exits fixed frequency CCM mode, the random

frequency shuffling will automatically replace the triangular frequency shuffling, and the range magnitude of shuffling increases by ±11%. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

## **Extended Burst Mode Operation**

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref\_burst\_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref\_burst\_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

#### Multi Mode Operation for High Efficiency

OB2633 is a multi-mode QR/PWM controller. The controller changes the mode of operation according to line voltage and load conditions.

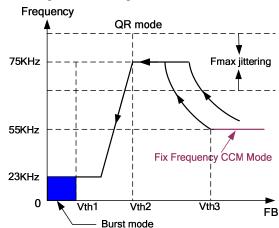


Fig. 1 Frequency vs Feedback voltage

At full load conditions (FB>Vth3, Figure 1), there are two situations: firstly, if the system input is in low line input range, the IC operates in fixed frequency CCM mode. Thus, small size



transformer can be used with high power conversion efficiency. Secondly, if the system input is in high line input range, the IC operates in QR mode. In this way, high power conversion efficiency can be achieved in the universal input range when system is at full loading conditions.

At normal operating conditions (Vth2<VFB<Vth3, Figure 1), the system operates in QR mode. The frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when the average 75KHz frequency clamping is reached.

At light load conditions (Vth1<VFB<Vth2, Figure 1), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. Generally, in flyback converter, the decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold-back is realized and high power conversion efficiency is achieved.

At no load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In the extended burst mode, the switching frequency at below 22KHz is minimized to avoid audio noise during operation.

## **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2633 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense voltage and the FB voltage.

#### **Demagnetization Detection**

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with

a frequency of approximately  $1/2\pi\sqrt{L_pC_d}$  ,

where  $L_p$  is the primary self inductance of primary winding of the transformer and  $C_d$  is the capacitance on the drain node.

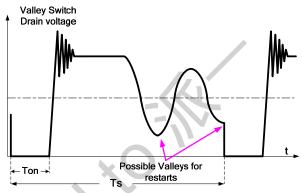
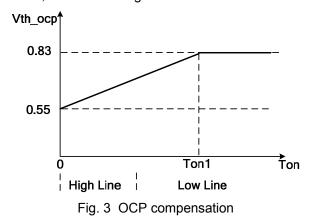


Fig. 2 Valley detection

The typical detection level is fixed at 85mV(typical) at the PRT pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at PRT is below 85mV in falling edge.

## **Adaptive OCP Compensation**

The variation of max output power in QR system can be rather large if no compensation is provided. The OCP threshold value is self adjusted lower at higher AC voltage. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage. In OB2633, with On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. a proprietary OCP compensation block is integrated and no external components are needed. The OCP threshold is a function of the switching ON time. For the ON time less than Ton1, the OCP threshold changes linearly from 0.55V to 0.83V. For the ON time larger than Ton1, the OCP threshold is clamped to 0.83V, as shown in Figure 3.



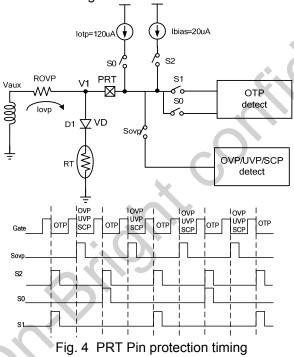


## Adaptive Internal Synchronized Slope Compensation

In OB2633, when the fixed frequency CCM mode is reached, the slope compensation will be automatically added to the system. Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage. When the system exits fixed frequency CCM mode, the slope compensation will automatically disappear.

## Dual Function of External OTP and Output OVP/UVP/SCP

On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the figure 4.



There is a 30uA(typical) bias current outflow when S2=1, that's S0= "1" or S1= "1". For external OTP detection, when switch control signal S1= "1", the 30uA (typical) current flows out from PRT pin. When switch control signal S0= "1", another 120uA (typical IRT) current flows out from PRT pin in addition to 30uA.

So the PRT pin voltage V1(s0) at phase S1="1" is:

$$V1(s1) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP \cdot 30uA}{ROVP + RT}$$

The PRT pin voltage V1(s1) at phase S0="1" is

$$V1(s0) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP(30uA + 120uA)}{ROVP + RT}$$

Vaux is the auxiliary winding demagnetization voltage.

VD is D1 forward voltage.

ROVP and RT are shown in fig4.

Voltage difference of  $\Delta Votp$  at phase S0 and S1 phase is

$$\Delta V_{otp} = V1(s0) - V1(s1) = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 120uA$$

This voltage difference cancels the effect of D1 diode forward voltage.

When  $\triangle$ Votp< VOTP (1.2V typical), external OTP auto-recovery protection is triggered after 60 (typical) PWM cycles debounce.

For output OVP detection, when Sovp= "1", lovp is equal to (Naux/Nsec)\*(Vo+Vdiode)/ROVP. During the IC startup 30ms, If lovp is larger than 90uA (typical loutput\_ovp), lower output OVP is triggered. After 30ms, if lovp is larger than 216uA (typical loutput\_ovp), larger output OVP is triggered. The output OVP voltage is calculated as

$$V_{outovp} = \frac{Iovp\_th \cdot N_{sec}.ROVP}{N_{aux}} - V_{diode}$$

Nsec is transformer secondary winding turns, Naux is transformer auxiliary winding turns, Vdiode is the secondary output diode forward voltage.

OVP auto-recovery protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

For output UVP detection, when Sovp= "1", luvp is equal to (Naux/Nsec)\*(Vo+Vdiode)/ROVP. After 15ms of the IC startup, If luvp is less than 40uA (typical luvp), UVP is triggered. The output UVP voltage calculation method is the same as output OVP detection. UVP auto-recovery protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output UVP level can be programmed.

For output SCP detection, when Sovp= "1", Isvp is equal to (Naux/Nsec)\*(Vo+Vdiode)/ROVP. After 7.5ms of the IC startup, If Iscp is less than 24uA (typical Iscp), SCP is triggered. The output SCP voltage calculation method is the same as output OVP detection. SCP auto-recovery protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output SCP level can be programmed.

#### **Protection Controls**

Good power supply system reliability is achieved with auto-recovery protection features including



Cycle-by-Cycle current limiting (OCP), and Under Voltage Lockout on VDD (UVLO), output short protection (SCP), output under voltage protection (UVP), Over Temperature Protection (OTP), VCC and output Over Voltage Protection (OVP).

## **Pin Floating and Short Protection**

OB2633 provides pin floating protection for CS, FB, PRT, etc., In cases when the pins are floating, Gate switching is disabled, thus protect the power system.

#### **Driver**

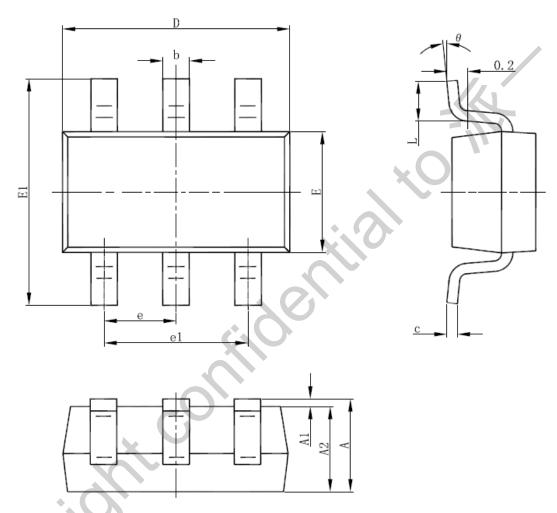
The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.



## PACKAGE MECHANICAL DATA

## SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Cumb at	Dimensions In	Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	1.000	1.450	0.039	0.057	
A1	0.000	0.150	0.000	0.006	
A2	0.900	1.300	0.035	0.051	
b	0.300	0.500	0.012	0.020	
С	0.080	0.220	0.003	0.009	
D	2.800	3.020	0.110	0.119	
П	1.500	1.726	0.059	0.068	
E1	2.600	3.000	0.102	0.118	
е	0.950 (BSC)		0.037 (	BSC)	
e1	1.800	2.000	0.071	0.079	
L	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	



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