OB3309

Highly Integrated U Type CCFL Backlight Controller

Product Specification

GENERAL DESCRIPTION

OB3309 is a highly integrated and high performance U-type Cold Cathode Fluorescent Lamp (CCFL) controller optimized for LCD display backlight application. Comprehensive protection functions are integrated, thus it provides a cost effective yet high reliability LCD backlight solution.

Operating in push pull configuration, OB3309 converts DC input voltage to the pure sinusoidal voltage and current waveforms, to ignite and operate CCFL lamps.

It provides a high degree of design flexibility by offering great programmability for key parameters which include operating frequency, striking frequency, striking time, dimming polarity, burst dimming frequency, soft-start time, and soft on/off time for burst dimming.

Various dimming modes control and dimming polarity programmability are offered. Both internal burst and external low frequency PWM (LPWM) dimming methods are available for a wide range of dimming control. Analog dimming is also provided through external DC input control to achieve wide dimming range.

The highly integrated OB3309 provides complete protection features covering output over voltage, over output current protection, lamp fail safe function, and IC under voltage lockout.

The OB3309 is available in SOP-16 Packages.

FEATURES

- High performance push pull topology
- Optimized for U type CCFL solution
- Adjustable dimming polarity
- Adjustable striking frequency & time
- Flexible Dimming mode Control:
  - Analog dimming control
  - Internal burst dimming control
  - External burst (LPWM) dimming control
- Adjustable minimum duty for internal burst dimming
- Adjustable minimum reference voltage for analog dimming
- 0-2V DC voltage direct dimming control without external circuits
- Comprehensive Protection Coverage:
  - Output over voltage protection (OVP)
  - Output over current protection (OCP)
  - Open lamp protection and short lamp protection
  - Arcing protection

APPLICATIONS

- LCD Monitor
- LCD TV
- Flat panel display

TYPICAL APPLICATION

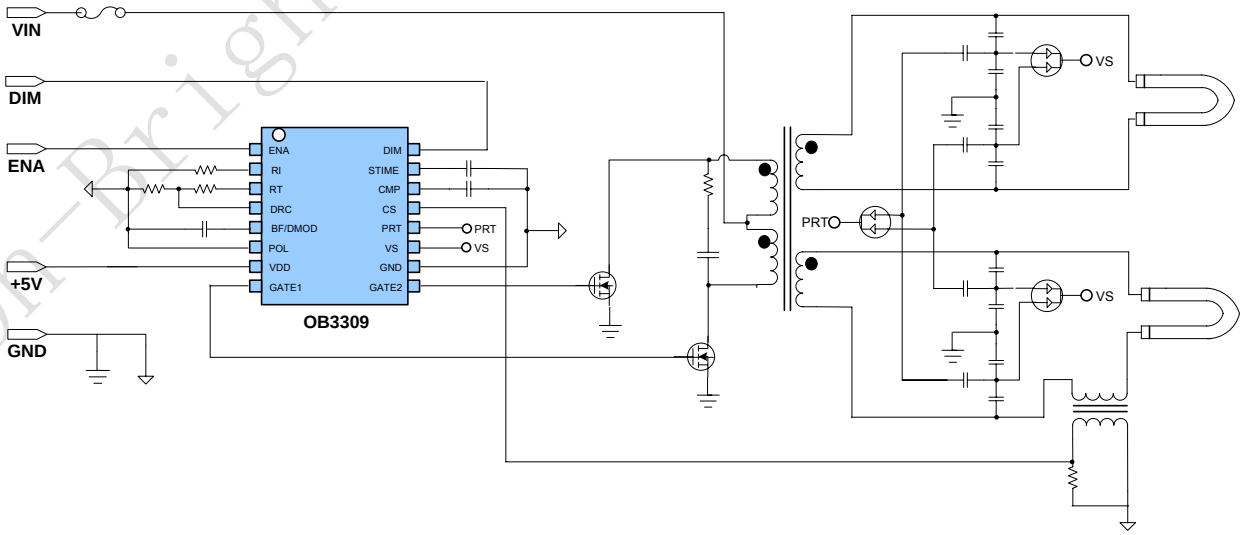


Figure1. OB3309 Typical Application Schematic

Absolute Maximum Ratings

Parameter	Value
VDD Input Voltage to GND	7V
CS to GND	-1.5V to VDD+0.3V
I/O to GND	-0.3V to VDD + 0.3V
Operating Ambient Temp. T_A	-20 °C ~ 85°C
Operating Junction Temp. T_J	150°C
Min/Max Storage Temp. T_{stg}	-55 °C ~150°C
Lead Temp. (10 Sec)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Range

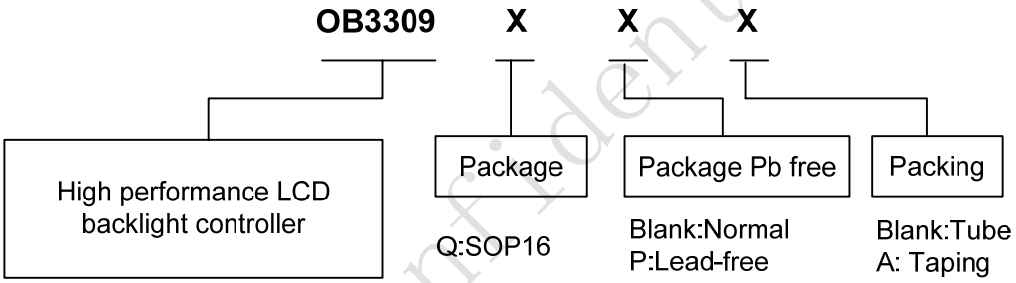
Parameter	Value
VDD Voltage	4.5V to 5.5V
Operating Frequency	30K to 150KHz

Package Thermal Characteristics

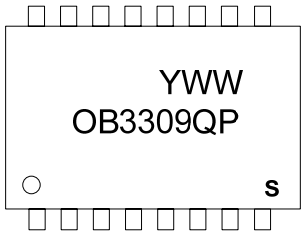
Parameter	Value
Thermal resistance θJA (SOP)	85 °C /W

Ordering Information

Part Number	Description
OB3309QP	SOP16, pb-free in tube
OB3309QPA	SOP16, pb-free in T&R

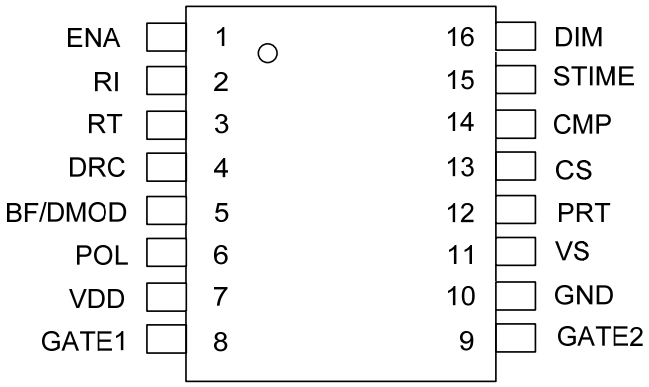


Package Marking Information



Y:Year Code
WW:Week Code(01-52)
Q:SOP16 Package
P:Pb-free Package
S:Internal Code(Optional)

Pin Configuration



Terminal Assignment

Number	Pin Name	I/O	Pin Function
1	ENA	Input	Enable control input, active high
2	RI	I/O	Connected an external resistor to ground to set striking frequency (No Floating)
3	RT	I/O	Connected an external resistor to ground to set operation frequency
4	DRC	Input	Dimming range setting. • Connect 0.2V to 2V DC voltage can set minimum burst duty from 100% to 0% for bust dimming; • Connect 0V to 1.25V DC voltage can set minimum Vref_ea from 0V to 1.25V for analog dimming;
5	BF/DMOD	I/O	Connected to VDD to set analog dimming mode Connected to GND to set external LPWM dimming mode Connect an external capacitor to GND to set internal burst dimming mode. The burst mode frequency is determined by the external capacitor
6	POL	Input	PWM Dimming polarity selection : • POL<2V: Negative analog / burst mode , positive LPWM dimming • POL>2V: Positive burst mode , negative analog / LPWM dimming
7	VDD	Power	+5V Power supply
8	GATE 1	Output	Output drive
9	GATE 2	Output	Output drive
10	GND	Ground	Power ground
11	VS	Input	Lamp voltage feedback
12	PRT	Input	Lamp fault detection
13	CS	Input	Lamp current feedback
14	CMP	I/O	Loop compensation and soft start time setting
15	STIME	I/O	Connect an external capacitor to GND to set striking time
16	DIM	Input	Dimming signal input

Functional Block Diagram

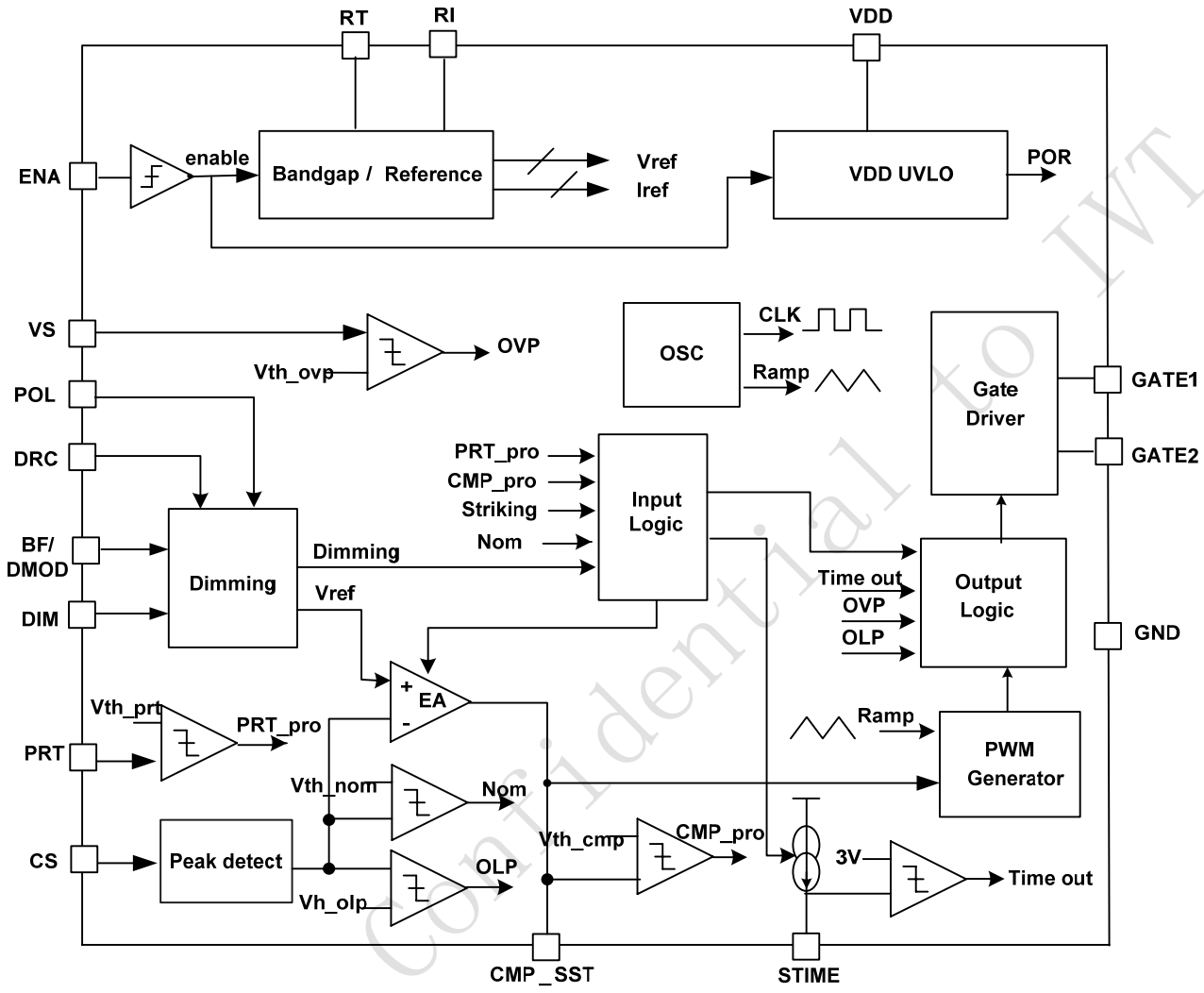


Figure2. OB3309 Functional Block Diagram

Electrical Characteristics

VDD=5V, ENA=5V, RT=36Kohm, RI=120Kohm, T_A=25℃, if not otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Consumption						
Standby current	$I_{standby}$	ENA=0V	-	-	8	uA
Operating supply current	I_{VDD}	No loading, CMP=5V	-	4.5	6	mA
Operating supply current	I_{VDD}	C_{load}=2nF, CMP=5V	-	5.5	8	mA
VDD UVLO						
UVLO on			3.6			V
UVLO off					4.4	V
Enable / Disable						
ENA (Enable) threshold voltage	ON		2.0			V
	OFF				0.8	
	R_{ENA}	Pull down resistor		100		Kohm
High Frequency Oscillator						
Operating frequency	F_{OP}		-	50	-	KHz
Striking frequency	F_{STK}			65		KHz
Max. (overlap) duty cycle				45		%
Low Frequency Oscillator for Burst Mode Dimming						
Burst frequency		$C_{BF/DMOD}$=22nF	-	200	-	Hz
Max. burst duty	D_{MAX}	$C_{BF/DMOD}$=22nF, DIM<0.2V	-	100	-	%
Min. burst duty 1 (set by DRC) [1]	D_{MIN1}	$C_{BF/DMOD}$=22nF, POL=0V, V_{DRC}=V_{RT}, DIM>2V	-	0	-	%
Min. burst duty 2 (set by DRC) [1]	D_{MIN2}	$C_{BF/DMOD}$=22nF, POL=0V, V_{DRC}=92%V_{RT} , V_{DRC} <DIM<2V	-	9	-	%
Min. burst duty 3 (set by DRC) [1]	D_{MIN1}	$C_{BF/DMOD}$=22nF, POL=5V, V_{DRC} =0V, DIM<0.2V	-	0	-	%
Min. burst duty 4 (set by DRC) [1]	D_{MIN2}	$C_{BF/DMOD}$=22nF, POL=5V, V_{DRC}=9%VRT+0.2,DIM< V_{DRC}	-	9	-	%
Analog Dimming Control						
Min. Lamp Current Reference Voltage 1 (set by DRC) [1]	$V_{ref\_EA\_MIN1}$	BF/DMOD=VDD, V_{DRC}=0V , DIM>2V	-	0	-	V
Min. Lamp Current Reference Voltage 2 (set by DRC) [1]	$V_{ref\_EA\_MIN2}$	BF/DMOD=VDD, V_{DRC}=25%V_{RT} , DIM>1.28V	-	0.5	-	V
Max. Lamp Current Reference Voltage	$V_{ref\_EA\_MAX}$	BF/DMOD=VDD, DIM<0.2V	-	1.25	-	V
External LPWM Dimming Control						
External LPWM duty		BF/DMOD=0V	0	-	100	%
External LPWM Logic input level	high	BF/DMOD=0V	2.0			V
	low	BF/DMOD=0V			0.8	V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Error Amplifier						
Reference voltage	V_{ref_EA}	$C_{BF/DMOD}$=22nF or BF/DMOD=0V	1.2	1.25	1.3	V
Open loop voltage gain				60		dB
Unity gain bandwidth		CMP=15nF		350		Hz
Soft on current	I_{SOFT_ON}			60		uA
Soft off current	I_{SOFT_OFF}			120		uA
Soft start						
Soft start current	I_{SST}			1.3		uA
Striking time						
Striking timer current	I_{STIME1}			1.3		uA
Striking timer threshold	V_{th_STIME1}			3		V
Control and Protection Threshold / Debounce time						
Ignition completion threshold	V_{th_CS}			0.85		V
	V_{th_PRT}			1.25		
VS regulate voltage at Striking	V_{th_REG}	Striking		2.0		V
Threshold voltage for PRT	V_{th_PRT}	Normal		1.25		V
Fault timer currnet	I_{STIME2}	Normal		14		uA
Fault timer threshold	V_{th_STIME2}	Normal		3		V
CS threshold voltage for OLP (open lamp protection)	V_{th_OLP}	Normal, BF/DMOD=0V or $C_{BF/DMOD}$=22nF		0.8		V
		Normal, BF/DMOD=VDD		60%*V_{ref_EA}		
OLP debounce time	T_{OLP}	Normal		160		ms
VS threshold voltage for OVP (over voltage protection)	V_{th_OVP}	Normal		2.0		V
OVP debounce time	T_{OVP}	Normal		160		ms
Normal protection blanking time	T_nom	Normal		0.48		Sec
Dimming_on time for OLP disable	T_dim_on	Normal, BF/DMOD=0V or $C_{BF/DMOD}$=22nF		480		uS
Dimming Polarity Control						
Dimming Polarity Selection	V_{th_POL}	Negative internal burst mode or positive external PWM dimming	-	-	2.0	V
		Positive internal burst mode or negative external PWM dimming	2.05	-	-	
	R_{POL}	Pull down resistor		45K		ohm
Gate Driver Output						
Gate1	R_{ON}	$I_{sink/Isource}$=70mA	-	8	12	ohm
Gate2	R_{ON}	$I_{sink/Isource}$=70mA	-	8	12	ohm

Note: *[1] Detail description to see Figure4 of page 8;*

[2] For analog dimming mode, V_{th_OLP} tracks with V_{ref_EA}. V_{ref_EA} can be calculated by the following equation:

$$V_{ref\_EA} = \frac{25}{36} \times (2 - V_{DIM}) \quad \text{for} \quad 0.2V \le V_{DIM} \le 2V$$

Function Description

General Operation

OB3309 CCFL controller is designed for U-type CCFL's LCD backlight system applications configured in push pull topology; it converts the DC input voltage to pure sinusoidal waveforms for CCFL operating with high efficiency and low EMI emission. The resonant frequency of the tank is set by the transformer leakage inductance and secondary parallel capacitor.

The lamp fault protection functions are integrated to provide a high reliability & simplifier solution with low system cost. Dimming polarity selection can be achieved by setting the voltage level at POL Pin. A typical application scheme is shown in figure 8 on page 10.

Enable the Controller

OB3309 is activated by applying logic high to the ENA input. It is TTL logic compatible. The controller is enabled when the voltage at ENA pin is higher than 2.0V. Toggling the ENA signal resets the state machine hence restarts the inverter system.

Normal Operation and Striking Frequency

The normal operation frequency, F_{OP}, is set by the resistor connected to RT pin. It is given by

$$F_{OP}(KHz) = \frac{1800}{RT(Kohm)}$$

The striking frequency, $F_{striking}$, is set by the resistors connected to both RI and RT pins. It can be calculated by the following equation:

$$F_{STRIKING}(KHz) = \frac{1800}{RT//RI(Kohm)}$$

Lamp Ignition and Striking Voltage Regulation

To ignite CCFL, a much higher voltage than that in normal operation is required, especially for aged lamp or in low ambiance temperature. The output voltage is divided by the capacitive voltage divider. A voltage signal is fed into VS pins with diodes and their peaks are compared with internal 2.0V threshold voltage. Consequently, the maximum output voltage is regulated and limited.
During ignition, OB3309 monitors the peak voltage levels at CS & PRT pins, it is recognized that all lamps are lit If the peak voltage of CS pin is higher than 0.85V and the voltage level at PRT pin is lower than 1.25V, then the system enters normal operating mode. Otherwise, the duty cycle of the gate drive signal will increase further to deliver more power to ignite the lamp. Once the duty cycle of gate drive signal reaches maxima of 45%, the internal striking timer will be triggered. If the lamps are lit before the time out, OB3309 enters the normal operation mode. Otherwise, it enters the shutdown mode. The striking time is given by:

$$T(sec) = 2.31 \times C[uF]$$

After the striking time out, the striking frequency will be switched to normal frequency and last for 64ms, if any one of the lamps still can not be lit, OB3309 will enters the shutdown mode as show in Figure 3.

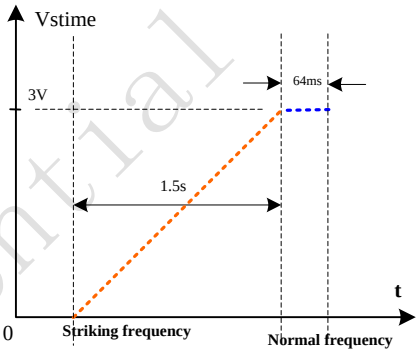


Figure 3 Striking mode control

Soft Start and Soft On/off

External capacitor connected to CMP pin provides soft start and soft on/off control. At start up, an internal current source starts to charge the capacitor. Consequently, voltage at CMP pin increases gradually and so as to the pulse width of the PWM Gate signals. This soft start control helps to reduce the MOSFET inrush current and voltage stresses, thus expand the lamp life time. The slope of the soft start $\Delta V / \Delta T$ can be approximated as:

$$\frac{\Delta V[V]}{\Delta T[mS]} = \frac{217}{C_{CMP}[nF] \times RT//RI[kohm]}$$

Once lamps are ignited, the capacitor connected to CMP pin performs the loop compensation function. In internal burst mode dimming or external burst (PWM) mode dimming conditions, the voltage ramping up and down at this pin performs a soft on/off control function in each burst cycle.

Lamp Current Regulation

Lamp current is regulated by the currents feedback loop with an internal transconductance error amplifier.

The AC lamp currents are sensed by the sense resistors (refer to R24 in figure 8) connected in series with high voltage coupling inductance. The AC voltage across the sense resistors are fed into the CS pins. The peak of the sensed AC voltage is detected. The peak value is compared with an internal reference voltage. The error is amplified that controls the on time of the push pull switches, as a result, the lamp current is regulated. The lamp current can be calculated by the following equation:

$$I_{lamp}(A) = N * \frac{1.33}{\sqrt{2} \times R_{sense}}$$

Where N is the coupling inductance turns ratio, $N=N_{LV}/N_{HV}$, the inductance T2 ,as shown in figure8.

Dimming Control

Three commonly used dimming modes, analog mode dimming, internal burst mode dimming and external burst (PWM) dimming functions, are supported without any additional components. Different dimming modes are selected by BF/DMOD pin. The lamp brightness is determined by the control signal at DIM pin. Both in internal burst mode dimming and external PWM mode dimming, the polarity can be set by the voltage level at POL pin as shown in the following table:

Function	Polarity	
	POL< 2V	POL >2V
Analog dimming	Negative	Negative
Internal Burst	Negative	Positive
External LPWM	Positive	Negative

External LPWM burst dimming mode is selected by shorting BF/DMOD pin to ground. OB3309 accepts an external LPWM signal to DIM pin with a swing voltage of 0V to a level greater than 2V. The lamp brightness is controlled by the duty cycle of the LPWM signal. The burst frequency is equal to LPWM frequency.

Connecting BF/DMOD pin to VDD selects analog mode dimming. A DC voltage ranging from 0.2V to 2V at DIM pin performs analog mode dimming control. The voltage at DIM pin modulates internal error amplifier reference voltage V_{ref_EA} from 1.25V to V_{DRC}, which corresponds to a lamp current of approximately 100% to (V_{DRC}/1.25)×100%. V_{ref_EA} can be calculated by the following equation:

$$V_{ref\_EA}(V) = \frac{25}{36} \times (2 - V_{DIM}) \quad \text{for}$$

$$0.2V \le V_{DIM} \le 2 - \frac{36}{25} \times V_{DRC}$$

The minimum voltage of V_{ref_EA} is determined by the voltage at DRC which should be set in the range from 0V to 1.25V for analog dimming mode.

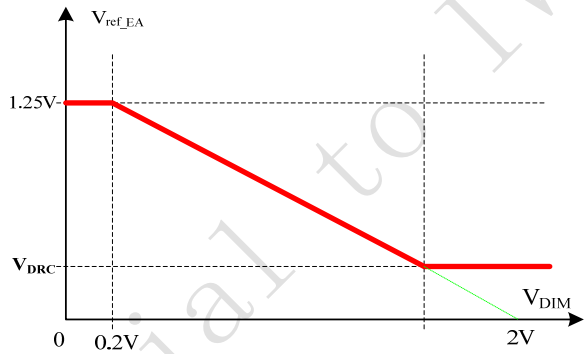


Figure. 4 Vref of EA vs DIM voltage

Internal burst mode dimming is obtained by connecting a capacitor to BF/DMOD pin. A low frequency triangular waveform generator is formed by the capacitor and internal circuit of IC. The triangular voltage waveform with peak of 2V and valley of 0.2V at this pin is used for the internal low frequency burst PWM generation. Duty cycle so as to lamp brightness is controlled by the analog signal at DIM pin. The burst mode dimming frequency F_{burst} is set by the following equation:

$$F_{burst}(Hz) = \frac{158400}{C_{BF}[nF] \times RT[Kohm]}$$

A DC voltage ranging from 0.2V to 2V at DIM pin corresponds to a lamp brightness of approximately 100% to $\frac{(2 - V_{DRC})}{1.8} \times 100\%$, as shown in Figure 5.

$$Duty = \frac{(2 - V_{DIM})}{1.8} \times 100\% \quad \text{for} \quad 0.2V \le V_{DIM} \le V_{DRC}$$

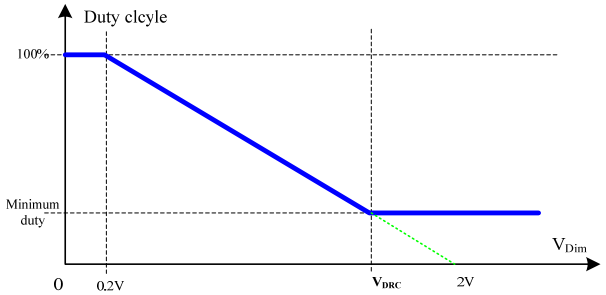


Figure. 5 Duty of burst vs DIM voltage

(Negative internal burst mode dimming)

If the voltage of POL is higher than 2.05V, the dimming polarity is changed, and DC voltage from 0.2V to 2V at DIM pin corresponds to the lamp's brightness of approximately minimum duty cycle of burst dimming to 100%, as shown in Figure 6. The minimum duty cycle of burst dimming can be calculated by the following equation:

$$\begin{cases} \dfrac{(V_{DRC}-0.2)}{1.8}\times 100\% & \text{for } V_{DRC} > 0.2V \\ 0\% & \text{for } V_{DRC} \le 0.2V \end{cases}$$

$$Duty = \frac{(V_{DIM}-V_{DRC})}{2-V_{DRC}}\times 100\% \text{ for } 0.2V < V_{DRC} < V_{DIM}$$

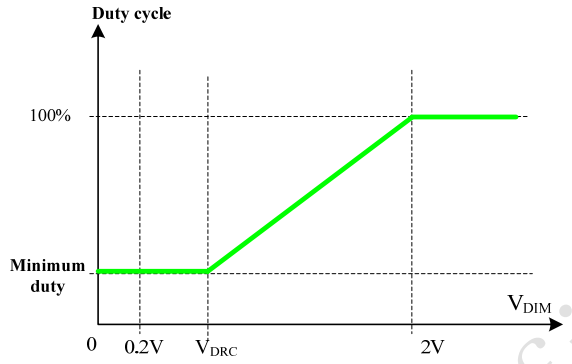


Figure. 6 Duty of burst vs DIM voltage

(Positive internal burst mode dimming)

Function	Pin Connection		Ratio
	BF/DMOD	DIM	
Analog dimming	>4.5V	0.2V-2V	Set by customer
Internal Burst	Capacitor	0.2V-2V	Set by customer
External LPWM	<0.2V	PWM	Set by customer

A DC voltage at DRC pin determines the minimum dimming thus it is used to adjust dimming range for analog mode dimming or internal burst mode dimming. Because the voltage of RT pin is fixed 2V when OB3309 is in operation, the voltage of DRC can be set by RT divided resistors, as shown in Figure 7. (Patent pending)

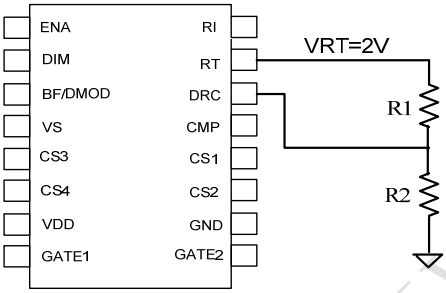


Figure. 7 Use DRC PIN to set Dimming Range

$$V_{DRC}(V) = 2\times\frac{R2}{R1+R2}$$

$$RT = R1+R2$$

Lamp Fail Safe Functions

The OB3309 provides complete protection features that cover all common lamp fault conditions including:

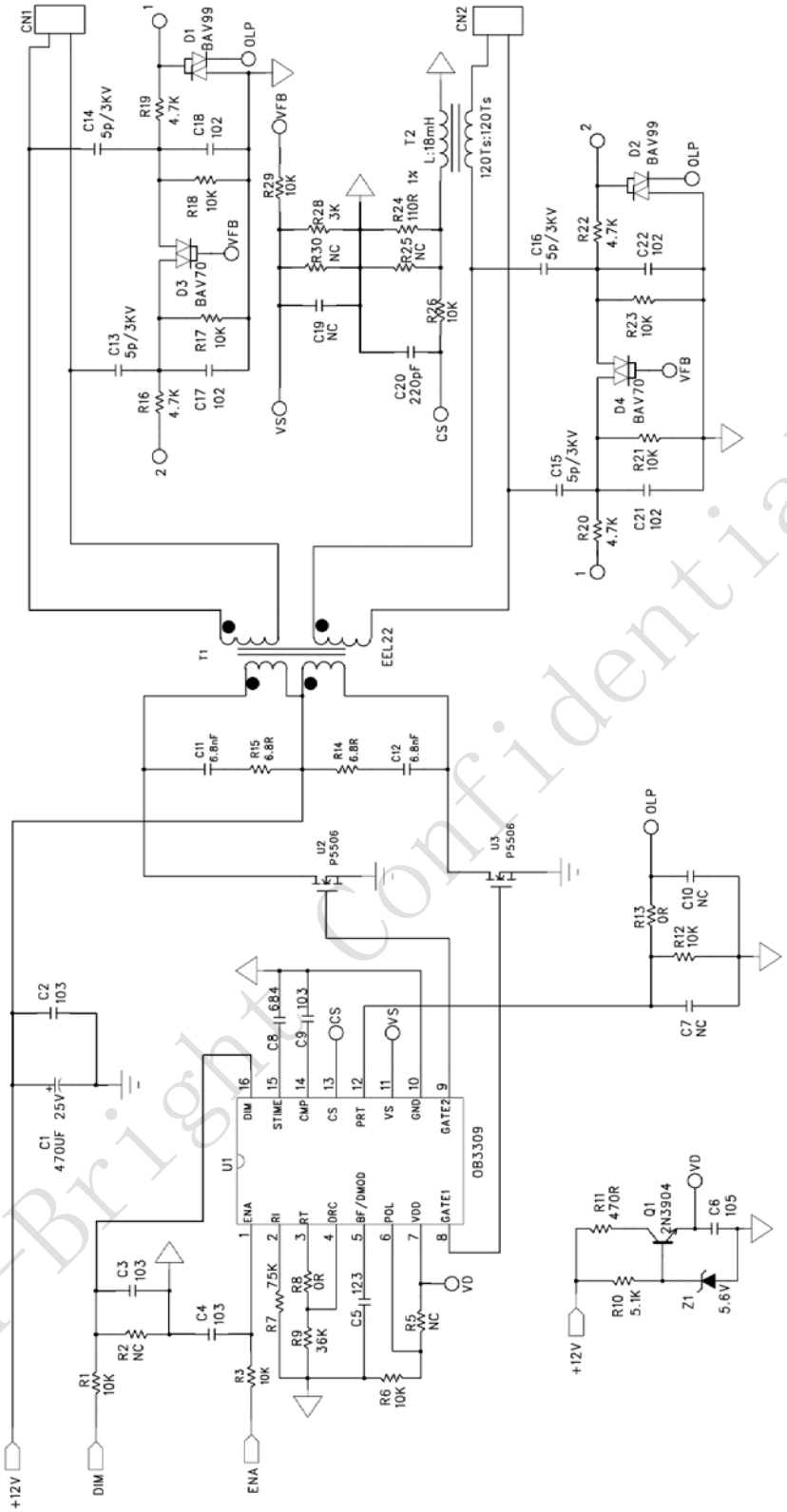
- Lamp open or broken
- Two terminals of lamp are short together
- High voltage terminal of lamp is short to ground

The sensed lamp voltage and current signals, CS, VS and PRT are used to monitor and detect the faults.

During normal operation, if the peak voltage level at CS pin is less than V_{th_OLP}, the lamp open or lamp broken is recognized and the system will shutdown after 160ms. If the peak voltage level at PRT pin is higher than V_{th_PRT}, an internal source current (14uA) charges the capacitor which connected STIME pin to ground. Once the voltage at STIME pin reaches 3V, the IC will shut down. But in internal burst mode dimming or external PWM mode dimming, if the dimming_on time is less than 480uS, these two protections are disabled.

During normal operation, if VS peak voltage is more than 2.0V, it enters latched shutdown mode.

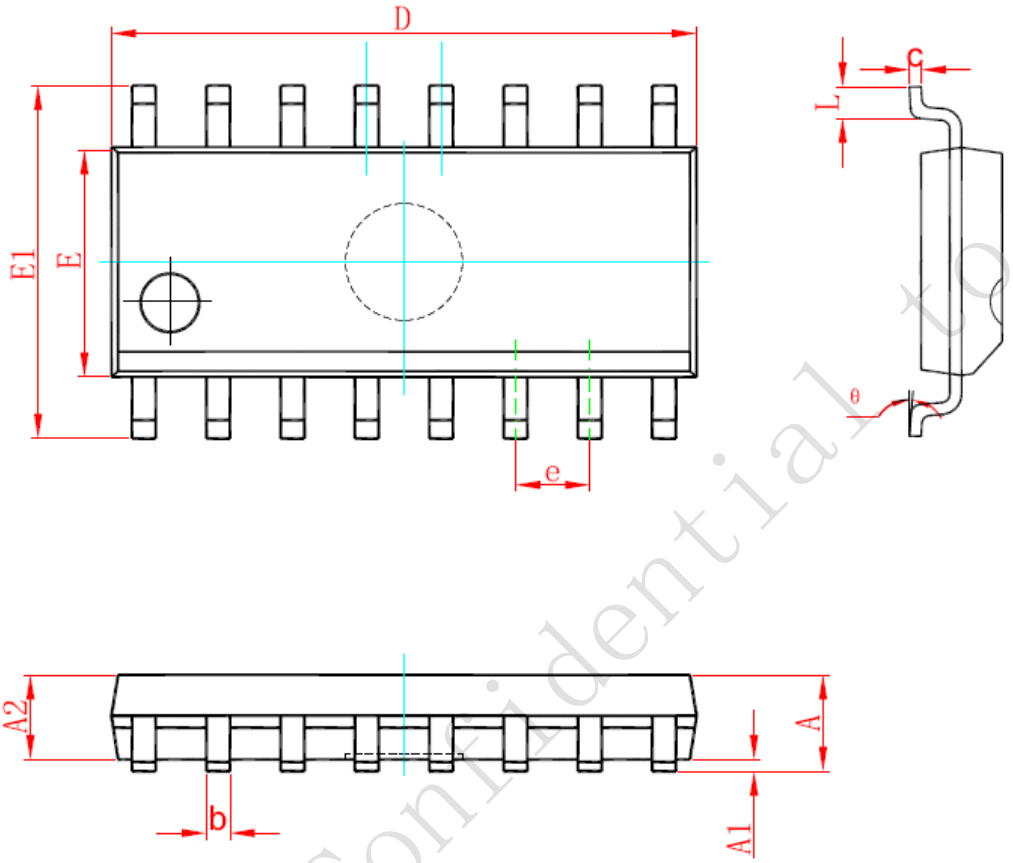
Reference Application Circuit for 2U Lamps



VIN: 10.8-13.2V
ADIM: 0V, Max. Brightness; 5V, Min. Brightness (for analog mode dimming)
PWM: 0V, Max. Brightness; 5V, Min. Brightness (for internal burst mode dimming)
100%, Max. Brightness; 30%Min. Brightness (for external burst mode dimming)
ENA: Disable, 0-0.8V; Enable, 2-5V

Figure8.OB3309 Reference Application Schematic

SOP16 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.400	0.386	0.409
E	3.800	4.040	0.150	0.159
E1	5.800	6.240	0.228	0.246
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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