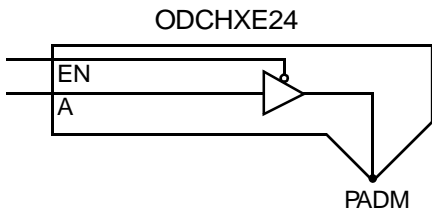


AMI5HG 0.5 micron CMOS Gate Array

Description

ODCHXE24 is a high performance, 24 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol	Truth Table	Pin Loading																				
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>3.5 eqI</td> </tr> <tr> <td>EN</td> <td>6.5 eqI</td> </tr> <tr> <td>PADM</td> <td>4.93 pF</td> </tr> </tbody> </table>		Load	A	3.5 eqI	EN	6.5 eqI	PADM	4.93 pF
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A	3.5 eqI																					
EN	6.5 eqI																					
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HDL Syntax

Verilog ODCHXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXE24 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	TBD	nA
EQL_{pd}	297.0	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	100	200	300 (max)
A		PADM	t_{PLH}	1.00	1.46	2.10	3.41	4.76
			t_{PHL}	0.57	1.38	1.82	2.65	3.55
EN		PADM	t_{HZ}	1.06				
			t_{LZ}	1.02				
			t_{ZH}	0.86	1.33	2.00	3.33	4.65
			t_{ZL}	0.99	1.35	1.78	2.63	3.53

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Pad Loading